

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INNOSCIENCE (ZHUHAI) TECHNOLOGY COMPANY, LTD.,
AND
INNOSCIENCE AMERICA, INC.
Petitioner,

v.

EFFICIENT POWER CONVERSION CORPORATION,
Patent Owner

Case IPR2023-01383
U.S. Patent No. 8,404,508

PATENT OWNER'S RESPONSE

TABLE OF CONTENTS

	Page
I. Introduction	1
II. Background	3
A. The '508 Patent	3
B. Two-Mask vs. One-Mask Ohmic Contact Process.....	11
III. Level of Ordinary Skill in the Art.....	17
IV. Claim Construction	17
V. Response to Alleged Statement of Facts.....	26
VI. Overview of References Relied Upon.....	26
A. Yoshida.....	26
B. Beach.....	27
C. Sheppard	29
D. Hikita347.....	31
E. Hikita023.....	33
VII. Ground 1: <i>Yoshida</i> in View of <i>Sheppard</i> and <i>Beach</i> Does Not Render Claims 1-3 Unpatentable.....	34
A. A POSA Would not have been Motivated to Combine the References.....	34
B. Petitioner’s “Mix and Match” Approach is Premised on Impermissible Hindsight.....	41
C. Petitioner Provides No Motivation to Replace <i>Yoshida</i> ’s One Mask Ohmic Formation with <i>Beach</i> ’s Two Mask Process	43
D. Petitioner’s Purported Combination/Modification Fails to Meet the Separate and Distinct “gate photo resistant pattern” and “metal photo resistant pattern” Limitations.....	48

VIII.	Ground 2: Hikita347, Sheppard, and Beach	53
A.	Petitioner Never Provides a Description of Incorporating Beach into Hikita347	54
B.	A POSA would Not be Motivated to Replace <i>Hikita347</i> ’s Gate-Last Process with <i>Beach</i> ’s Gate-Simultaneous Process	54
C.	There is No Motivation to Replace <i>Hikita347</i> ’s One Mask Ohmic Formation with a Two-Mask Process.....	56
D.	It Would Not have Been Obvious to Combine <i>Hikita347</i> ’s Enhancement Mode Device with <i>Beach</i> ’s Depletion Mode Device..	58
E.	<i>Hikita347</i> ’s Fabrication Process is Incompatible with <i>Beach</i> ’s Simultaneous Gate and Ohmic Contact Formation Process.....	59
F.	Ground 2 Fails to Teach a “Gate-First” Process	60
G.	Ground 2 Does not Teach Separate Steps of “applying a gate photo resistant pattern” and “applying a metal photo resistant pattern”	61
IX.	Ground 3: Hikita023, Sheppard, and Beach	63
A.	A POSA Would Not be Motivated to Replace <i>Hikita023</i> ’s “Gate-Last” Process with <i>Beach</i> ’s “Gate-Simultaneous” Process.....	63
B.	No Motivation to Replace <i>Hikita023</i> ’s Single-Mask Ohmic Formation with a Two-Photo Mask Formation.....	64
C.	It Would Not have Been Obvious to Combine <i>Hikita023</i> ’s Enhancement Mode Device with <i>Beach</i> ’s Depletion Mode Device..	65
D.	<i>Hikita023</i> ’s Fabrication Process is Incompatible with <i>Beach</i> ’s “Gate-Simultaneous” Process.....	65
E.	Ground 3 Fails to Teach a “Gate-First” Process	66
F.	Ground 3 Does not Teach Separate Steps of Applying a “gate photo resistant pattern” and “fourth photo resistant pattern”.....	67
X.	Conclusion.....	69

TABLE OF AUTHORITIES

	Page(s)
Cases	
<i>Aylo Freesites Ltd., v. Dish Techs. L.L.C.</i> , No. IPR2024-00147, 2024 Pat. App. LEXIS 1528 (PTAB Apr. 25, 2024)	35
<i>Becton, Dickinson & Co. v. Tyco Healthcare Grp., LP</i> , 616 F.3d 1249 (Fed. Cir. 2010).....	48
<i>Belden Inc. v. Berk-Tek LLC</i> , 805 F.3d 1064, 1073 (Fed. Cir. 2015)	35
<i>Function Media, LLC v. Google, Inc.</i> , 708 F.3d 1310 (Fed. Cir. 2013).....	18
<i>Gemalto S.A. v. HTC Corp.</i> , 754 F.3d 1364 (Fed. Cir. 2014).....	21
<i>In re Kahn</i> , 441 F.3d 977 (Fed. Cir. 2006).....	35
<i>InTouch Techs., Inc. v. VGo Commc'ns., Inc.</i> , 751 F.3d 1327 (Fed. Cir. 2014).....	34, 35, 36
<i>KSR Int'l Co. v. Teleflex Inc.</i> , 550 U.S. 398 (2007)	35
<i>Medicines Co. v. Mylan, Inc.</i> , 853 F.3d 1296 (Fed. Cir. 2017).....	20
<i>Mformation Techs., Inc. v. Research in Motion Ltd.</i> , 764 F.3d 1392 (Fed. Cir. 2014).....	17, 18
<i>Personal Web Technologies v. Apple</i> , 848 F.3d 987 (Fed. Cir. 2017).....	39, 47
<i>Renishaw PLC v. Marposs Societa'</i> <i>per Azioni</i> , 158 F.3d 1243 (Fed. Cir. 1998).....	21
<i>Retractable Techs., Inc. v. Becton, Dickinson & Co.</i> , 653 F.3d 1296 (Fed. Cir. 2011).....	18, 20

<i>Wi-Fi One, LLC v. Broadcom Corp.</i> , 887 F.3d 1329 (Fed. Cir. 2018).....	20
--	----

Other Authorities

37 C.F.R. § 42.22(c).....	26
---------------------------	----

LISTING OF EXHIBITS

Exhibit 2001	Declaration of Dr. E. Fred Schubert
Exhibit 2002	Deposition Transcript of Dr. James Shealy, May 23, 2024
Exhibit 2003	Exhibit prepared by Dr. Shealy at Deposition
Exhibit 2004	U.S. Patent 6,478,871, filed Oct. 2, 2000
Exhibit 2005	U.S. Patent 9,991,360, filed Mar. 5, 2012
Exhibit 2006	U.S. Patent Application Publication 2008/0087915, filed Jul. 24, 2007
Exhibit 2007	U.S. Patent D715,107, filed Jul. 26, 2013

CLAIM LISTING¹

Element Designation	Claim Language
Claim 1	
[1pre]	A method of forming an enhancement mode GaN transistor, the method comprising:
[1a]	nucleating and growing transition layers on a substrate;
[1b]	growing an III Nitride EPI layer over the transistor layers;
[1c]	growing an III Nitride barrier layer over the EPI layer;
[1d]	growing a GaN layer with acceptor type dopants over the barrier layer;
[1e]	
[1e1]	depositing a gate contact layer on the doped GaN layer;
[1e2]	applying a gate photo resistant pattern;
[1e3]	etching away the gate contact layer outside the gate region;
[1e4]	etching away the doped GaN layer, except a portion of the doped GaN layer beneath the gate contact;
[1e5]	removing the gate photo resistant pattern;
[1f]	
[1f1]	depositing a dielectric layer;
[1f2]	applying a contact photo resistant pattern;
[1f3]	etching the dielectric layer to open the drain and source contact area;
[1f4]	removing the contact photo resistant pattern;
[1g]	
[1g1]	depositing an Ohmic contact metal;
[1g2]	applying a metal photo resistant pattern;
[1g3]	etching the Ohmic contact metal;
[1g4]	removing the metal photo resistant pattern; and
[1g5]	performing rapid thermal annealing to form Ohmic drain and source contacts.
Claim 2	
[Claim 2]	wherein the EPI layer is comprised of InAlGaN.
Claim 3	

¹ Patent Owner utilizes the same designations as Innoscience for ease of reference.

[Claim 3]	wherein the barrier layer is comprised of InAlGa _N with a larger band gap than the buffer layer.
Claim 4	
[4pre]	A method of forming an enhancement mode GaN transistor, the method comprising:
[4a]	nucleating and growing transition layers on a substrate;
[4b]	growing an InAlGa _N EPI layer over the transistor layers;
[4c]	growing an InAlGa _N barrier layer over the InAlGa _N EPI layer;
[4d]	growing an InAlGa _N layer with acceptor type dopants over the InAlGa _N barrier layer;
[4e]	growing a GaN layer with acceptor type dopants over the doped InAlGa _N layer;
[4f]	
[4f1]	depositing a gate contact layer on the doped GaN layer
[4f2]	applying a gate photo resistant pattern;
[4f3]	etching away the gate contact layer outside the gate region;
[4f4]	etching away the doped GaN layer and the doped InAlGa _N layer, except for portions of the doped GaN layer and the doped InAlGa _N layer beneath the gate contact;
[4f5]	removing the gate photo resistant pattern;
[4g]	
[4g1]	depositing a dielectric layer;
[4g2]	applying a contact photo resistant pattern;
[4g3]	etching the dielectric layer to open the drain and source contact area;
[4g4]	removing the contact photo resistant patter;
[4h]	
[4h1]	depositing an Ohmic contact metal;
[4h2]	applying a metal photo resistant pattern;
[4h3]	etching the Ohmic contact metal;
[4h4]	removing the metal photo resistant pattern; and
[4h5]	performing rapid thermal annealing to form Ohmic drain and source contacts.
Claim 5	
[5pre]	A method of forming an enhancement mode GaN transistor, the method comprising:
[5a]	nucleating and growing transition layers on a substrate;
[5b]	growing an InAlGa _N EPI layer over the transistor layers;
[5c]	growing an AlGa _N barrier layer over the InAlGa _N EPI layer;

[5d]	growing an AlGa _N layer with acceptor type dopants over the AlGa _N barrier layer;
[5e]	growing a Ga _N layer with acceptor type dopants over the doped AlGa _N layer;
[5f]	
[5f1]	depositing a gate contact layer on the doped Ga _N layer
[5f2]	applying a gate photo resistant pattern;
[5f3]	etching away the gate contact layer outside the gate region;
[5f4]	etching away the doped Ga _N layer, except for portions of the doped Ga _N layer and the doped AlGa _N layer beneath gate contact;
[5f5]	removing the gate photo resistant pattern;
[5g]	
[5g1]	applying another photo resistant pattern;
[5g2]	etching the doped AlGa _N layer such that the doped AlGa _N extends outside the gate region towards the drain;
[5g3]	removing the photo resistant pattern;
[5h]	
[5h1]	depositing a dielectric layer;
[5h2]	applying a contact photo resistant pattern;
[5h3]	etching the dielectric layer to open the drain and source contact area;
[5h4]	removing the contact photo resistant pattern;
[5i]	
[5i1]	depositing an Ohmic contact metal;
[5i2]	applying a fourth photo resistant pattern;
[5i3]	etching the Ohmic contact metal
[5i4]	removing the fourth photo resistant pattern; and
[5i5]	performing rapid thermal annealing to form Ohmic drain and source contacts.

I. INTRODUCTION

Patent Owner Efficient Power Conversion Corporation hereby submits this response to the Petition (the “Petition” or “Pet.”) filed by Petitioner Innoscience (Zhuhai) Technology Company, Ltd., and Innoscience America, Inc. (collectively, “Petitioner”) for *Inter Partes* Review of claims 1-5 of U.S. Patent No. 8,404,508 (the “’508 patent”) (EX1001). Petitioner fails to demonstrate that any claim of the ’508 patent is unpatentable.

The ’508 patent describes novel methods to form gate, source, and drain contacts in an enhancement mode (normally OFF) gallium nitride (GaN) high electron mobility transistor (HEMT). The ’508 patent teaches methods to form the gate structure, including the gate material and gate contact, resulting in a self-aligned gate that minimizes the critical dimension of the gate structure *and* reduces cost of manufacture. The ’508 patent further teaches protecting its gate structure, by depositing a dielectric material over the formed gate structure, *before* it deposits and forms its ohmic contacts – a “gate-first” process. The ohmic contacts are uniquely formed through patterning and etching the ohmic metals in a two-photo mask process permitting the simultaneous formation of a field plate at source potential with the ohmic contacts, which reduces the electric field at its gate corner.

The Petition ignores the explicitly described “present invention” and instead presents an overly simplistic view of the process steps of the ’508 patent and the

cited prior art, ignoring claim steps that logically must be performed in order and construing the claims excessively broadly. The entire Petition is tainted by obvious hindsight to combine disparate prior art references to allegedly achieve the claimed methods, without *ever presenting a description of the actual proposed modified prior art process*. Rather, Petitioner simply picks and chooses different *elements* of the prior art and abstractly asserts that the combination renders the claim obvious, without explaining how the proposed combination would fit into an overall process to arrive at the claimed inventions.

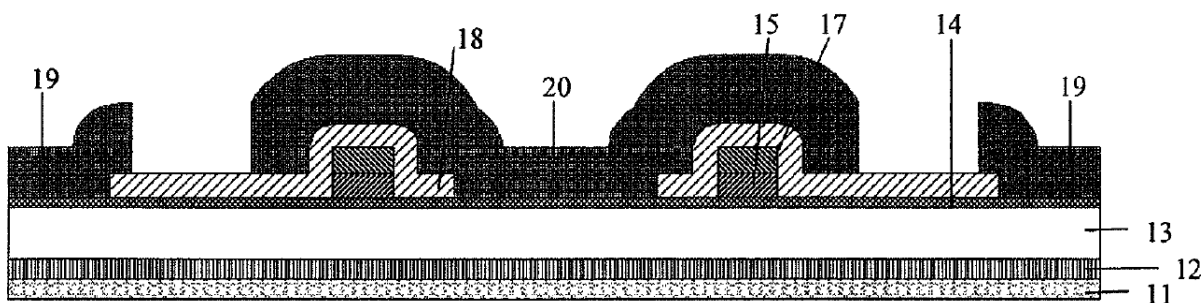
The three invalidity grounds rely on the same two secondary references International Publication WO2005/057624 (“*Beach*”) (EX1005), a “gate-simultaneous” process, and US 7,238,560 (“*Sheppard*”) (EX1006), a “gate-last” process, but different primary references, namely JPH11261053A (“*Yoshida*”) (EX1004) for Ground 1, US 2006/0273347 (“*Hikita347*”) (EX1007) for Ground 2, and US 2008/0079023 (“*Hikita023*”) (EX1008) for Ground 3. All of the primary references, *Yoshida*, *Hikita347* and *Hikita023* are “gate-last” processes. In all three grounds, the proposed combination fails to teach a “gate-first” process and fails to teach a process using the separately claimed steps to: (1) apply a patterned photoresist to form the gate structure and (2) apply a photoresist to form the ohmic contacts. Moreover, due to the differences in the prior art and the lack of motivation to combine the references with an expectation of achieving a successful

operable enhancement mode GaN HEMT, a POSA would not have sought to combine the references as proposed by Petitioner to arrive at the claimed invention.

II. BACKGROUND

A. The '508 Patent

The '508 patent describes and claims methods for making enhancement-GaN HEMT devices, including using a single-photo mask to pattern and form a self-aligned gate structure of gate material and gate metal, and using a two-mask process to form ohmic contacts, including simultaneously forming a field plate at source potential. The process results in an enhancement mode GaN HEMT with a self-aligned gate structure and a field plate at source potential. *See* EX1001 3:1-9, 3:21-23; 3:45-47, 3:57-4:19, 4:41-44, 4:55-59. An exemplary embodiment is depicted below in FIG. 2.



EX1001 FIG. 2

The enhancement mode GaN HEMT includes substrate 11, transition layers 12, buffer material 13, barrier material 14, GaN with acceptor type dopants (p-type GaN) 15, gate metal 17, dielectric material 18, drain ohmic contact 19, and source

ohmic contact 20 serving also as a field plate extending over the gate and towards the drain contact. EX1001 3:10-25.

The '508 patent discloses a method for forming a GaN HEMT device in which the gate metal 17 and the p-type GaN material 15 are patterned and etched using a single photo mask. EX1001 4:41-44. Because multiple layers of the gate are patterned and etched with a single photo mask, the resulting gate structure is “self-aligned.” *Id.* at 4:55-59; 4:6-9.

The single-mask self-aligned gate prevents misalignment between the gate metal and the gate material, reduces manufacturing cost, allows minimum gate length to be the same as the photo/etch minimum critical dimension, reducing gate charge and cell pitch. *Id.* at 4:7-19; EX2001 ¶48. Misalignment occurs, as explained below in §II.B, when two layers are patterned and etched using two photo masks due to unavoidable alignment errors. EX2001 ¶49. A two-photo mask process results in either misalignment between the two gate elements or requires a wider lower element (gate material) than the critical dimension to accommodate inevitable misalignment of the upper element (gate contact metal). *Id.*

The two-photo mask process to simultaneously form source and drain contacts with a field plate at source potential is part of the “present invention.” EX1001 3:6-9. Forming these structures together reduces the overall number of

steps to achieve a field plate and reduces the electric field at the gate corner. *Id.*; EX2001 ¶52.

As illustrated in Figures 3A-3C (below), after epitaxial growth (of elements 12-15 shown in Fig. 3A), the fabrication process proceeds. EX2002 35:24-36:2. The fabrication process is the patterning and forming of the structures above the epitaxial layers. EX2001 ¶53. In the fabrication process, gate metal 17 is deposited on p-type GaN layer 15. EX1001 3:39-44. Then, using photolithography, (the process of depositing a photoresist, exposing it to pattern the photoresist, and developing the photoresist to form the patterned photoresist mask on the wafer surface defining the pattern to be etched into the layers) (*id.* at 3:45-56; EX2001 ¶¶41, 54), gate metal 17 is etched, and subsequently, p-type GaN gate layer 15 is etched using the same mask pattern, resulting in the device of Fig. 3C. EX1001 3:45-56. Because the two etching processes are performed using the same patterned photoresist mask, the resulting gate structure is self-aligned. *Id.* at 3:45-56, 4:6-9, 4:20-44, FIGS. 2, 3A-E, 4, 5A-E; EX2001 ¶¶45, 54.

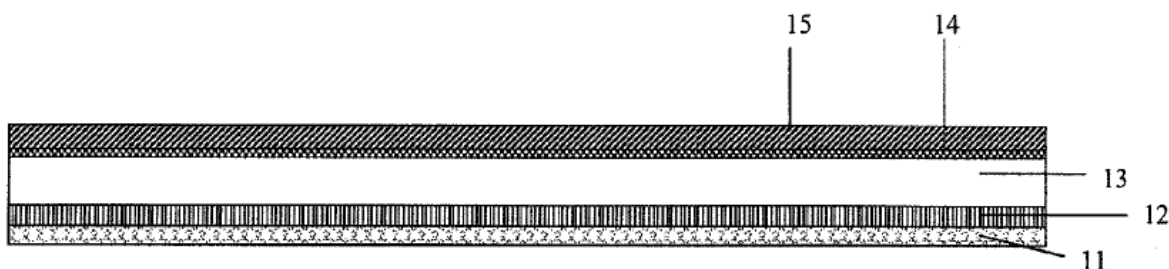


FIG. 3A

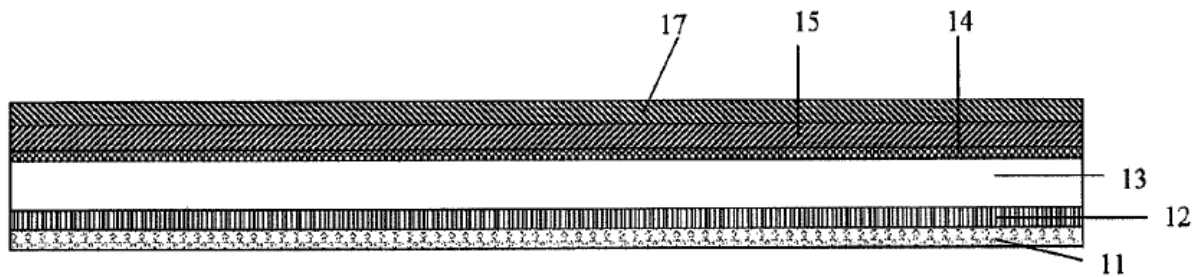


FIG. 3B

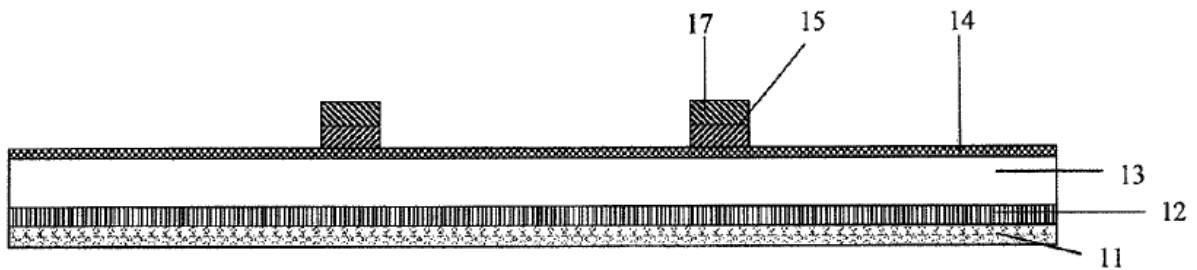


FIG. 3C

EX1001 Figs. 3A-3C

Importantly, the gate structure of the '508 patent is formed before the formation or deposition of the ohmic contacts. That is, the '508 patent is directed to a “gate-first” process. EX2001 ¶¶58, 75.² Figure 3C illustrates a gate structure formed using a single photo mask before the presence of ohmic contacts (shown in Fig. 3E). EX1001 3:45-47, Fig. 3C.

² In contrast to a “gate-first” process, a “gate-simultaneous” process is one in which the gate contact and source and/or drain contacts are formed in a single process step, and a “gate-last” process is one in which the gate contact is formed after the formation of the source and drain metals. EX2001 ¶¶58, 76-77.

Subsequently, dielectric material 18 is deposited over the formed gate structure. *Id.* at 3:57-58. After deposition of the dielectric, the two-photo mask process to form the ohmic contacts is performed. First, a contact photo mask is used to pattern and etch the dielectric to open regions for deposition of the source and drain metal. *Id.* at 3:58-61. Then, drain and source contact metal (19 and 20, respectively) is deposited over the wafer, a patterned photo mask is formed, and the metal is etched to simultaneously form the ohmic contacts and source connected field plate extending over the gate and at source potential. *Id.* at Figs. 3D, 3E, 3:61-4:3.

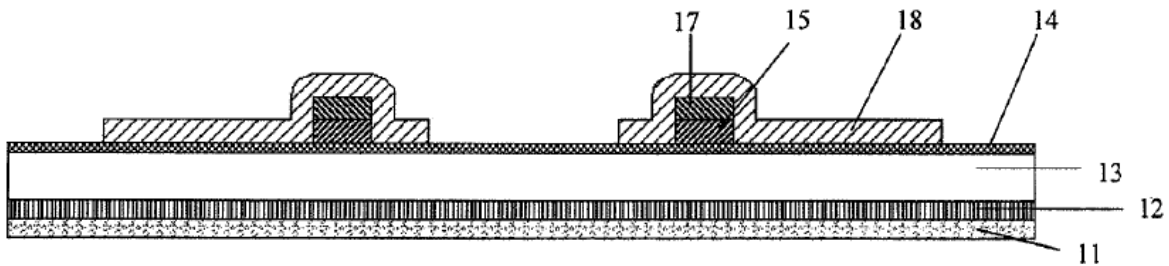


FIG. 3D

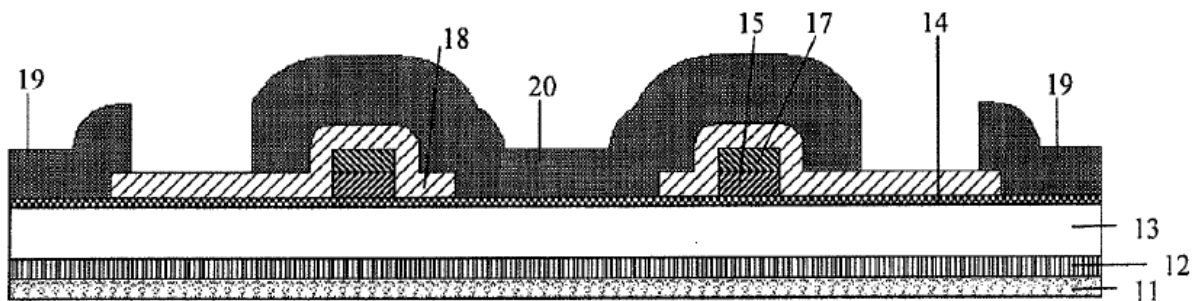
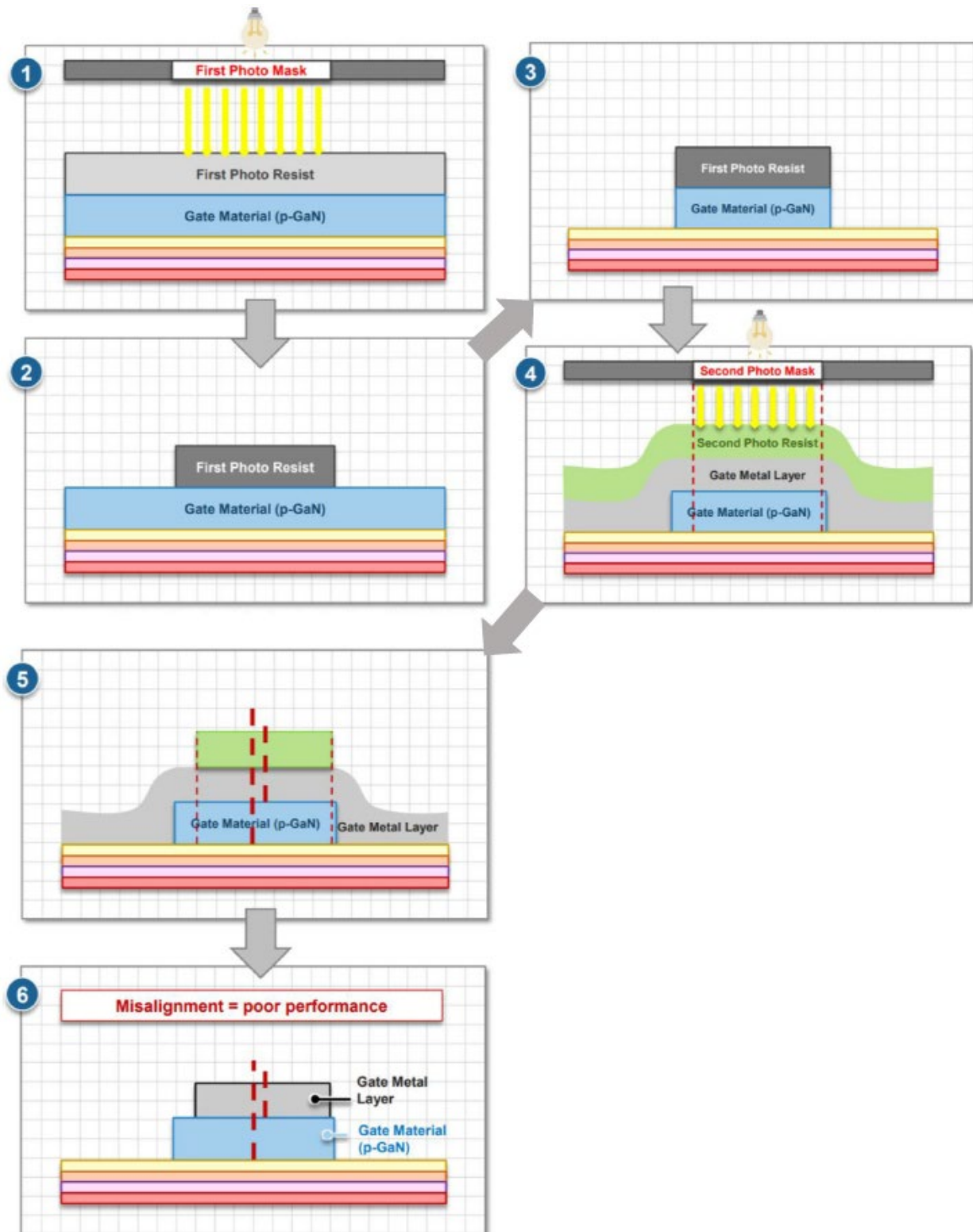


FIG. 3E

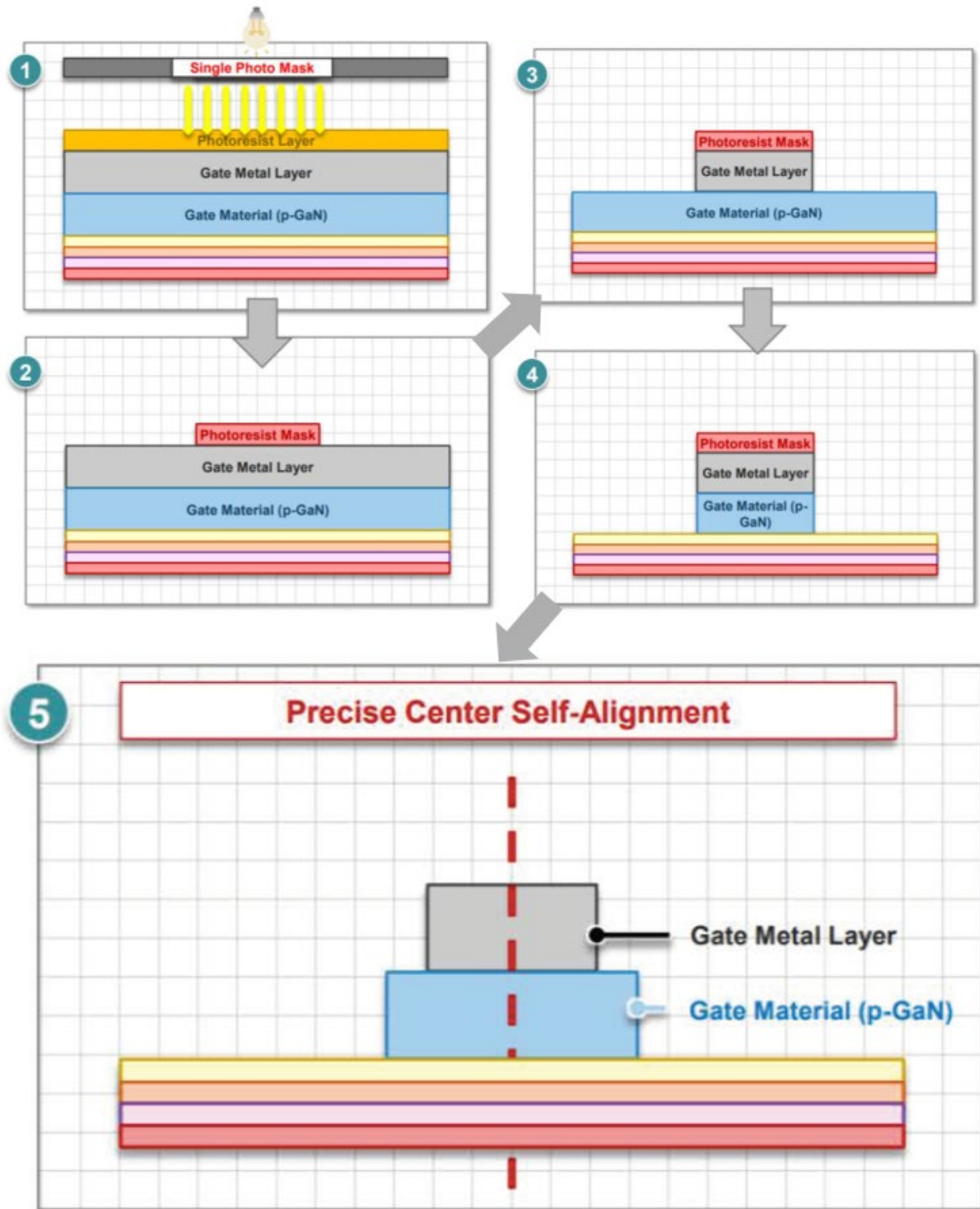
EX1001 Figs. 3D-3E

A self-aligned process is one in which a single patterned photo mask is used to etch more than one feature. Although self-aligned processes were generally known in semiconductor manufacturing, prior to the present invention, a self-aligned process had never been used to form a gate for an enhancement mode GaN transistor, i.e., a single-photo mask used to etch both the gate metal and the gate material of an enhancement mode GaN transistor. EX2001 ¶59; EX1001 3:1-6. In accordance with the present invention, self-alignment of the gate permits the minimal critical dimension (“CD”) to be achieved because the gate material does not need to be wider than the gate metal to accommodate for misalignment. EX2001 ¶60; EX1001 2:5-8.

An example of misalignment is shown below. The two-photo mask gate formation process results in the centers of the two features being out of alignment, while a single-photo mask self-aligned process results in precise center alignment.



EX2001 ¶61 (discussing a two-photo mask process)



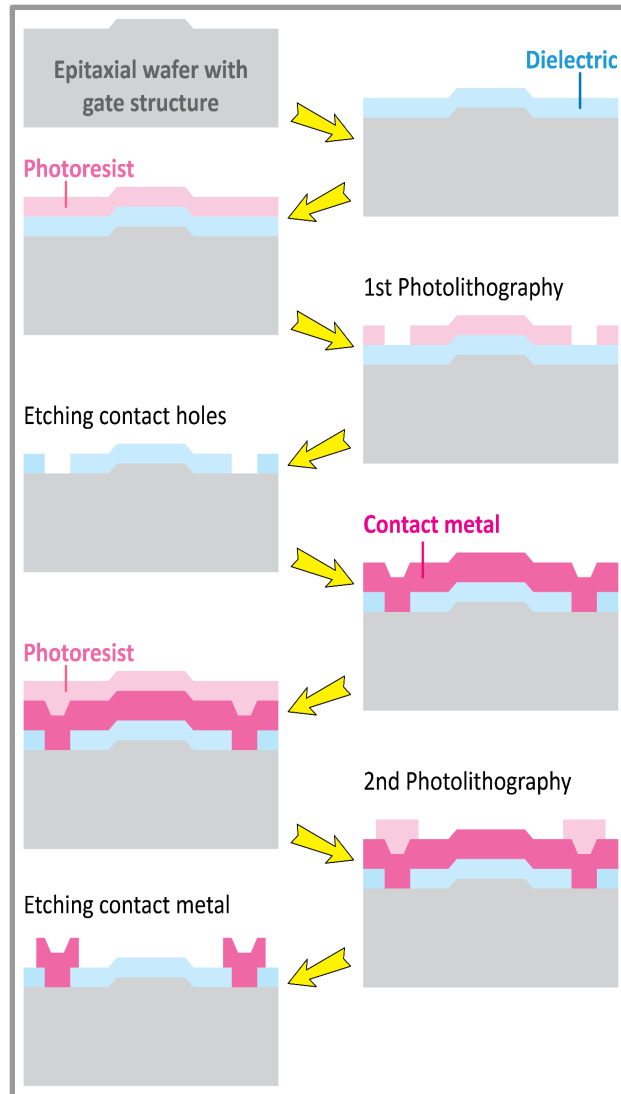
EX2001 ¶62 (discussing a single photo mask process)

B. Two-Mask vs. One-Mask Ohmic Contact Process

Forming Ohmic contacts for the source and drain of a transistor can be performed by at least two different processes. The '508 patent describes and claims a two-mask process for forming the ohmic contacts. EX2001 ¶¶65-66. In contrast, the formation can alternatively be achieved in a single-mask process, for example, a lift-off process. *Id.* at ¶65.

The '508 patent discloses and claims a two-mask ohmic contact process. The first mask is used in the step of patterning and etching holes into the dielectric layer, which defines the width of the lower portion of the ohmic contacts. EX1001 3:59-61, Claim 1, FIG. 3D; *see also* Claim Elements [4g], [5h]; EX2001 ¶66. The second photo mask is used to pattern and etch the contact metal defining the structure of the ohmic contacts above the dielectric layer including the field plate. EX1001 3:62-4:3, Claim 1, Fig, 3E; *see also* Claim Elements [4h], [5i].

Below is an illustrative representation of a two-mask process:

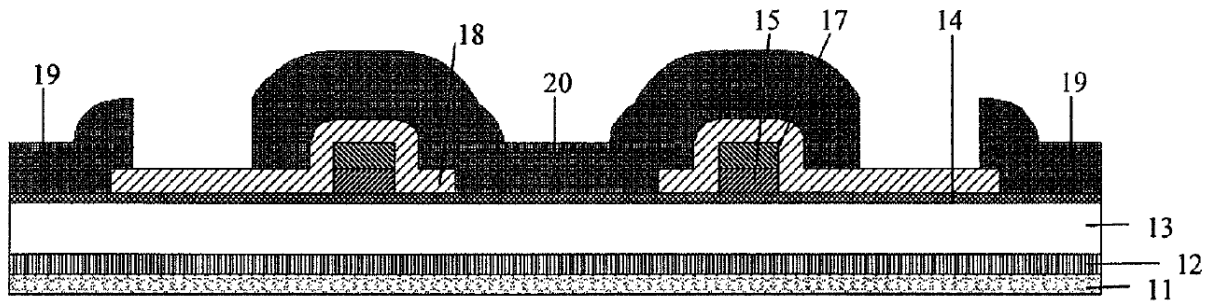


EX2001 ¶¶67-68

A first photolithography process³ creates a patterned photoresist on the wafer above the dielectric layer, as shown in the second figure on the right. EX2001 ¶68. The first patterned photoresist is used to etch the dielectric layer and create contact areas for ohmic contacts. *Id.* The photoresist is then removed (Claim Elements [1f], [4g], [5h]).

The contact metal is next deposited across the wafer followed by the second mask process. The second photolithography process patterns a second photoresist for etching the contact metal deposited in and above the dielectric layer. The two-mask process does not result in a contact metal sidewall aligned with the edges of the dielectric material defining the contact holes, but instead the contact metal can be seen extending laterally above the dielectric. *See also* EX1001 FIG. 2 (contact metal 19, 20 over dielectric 18).

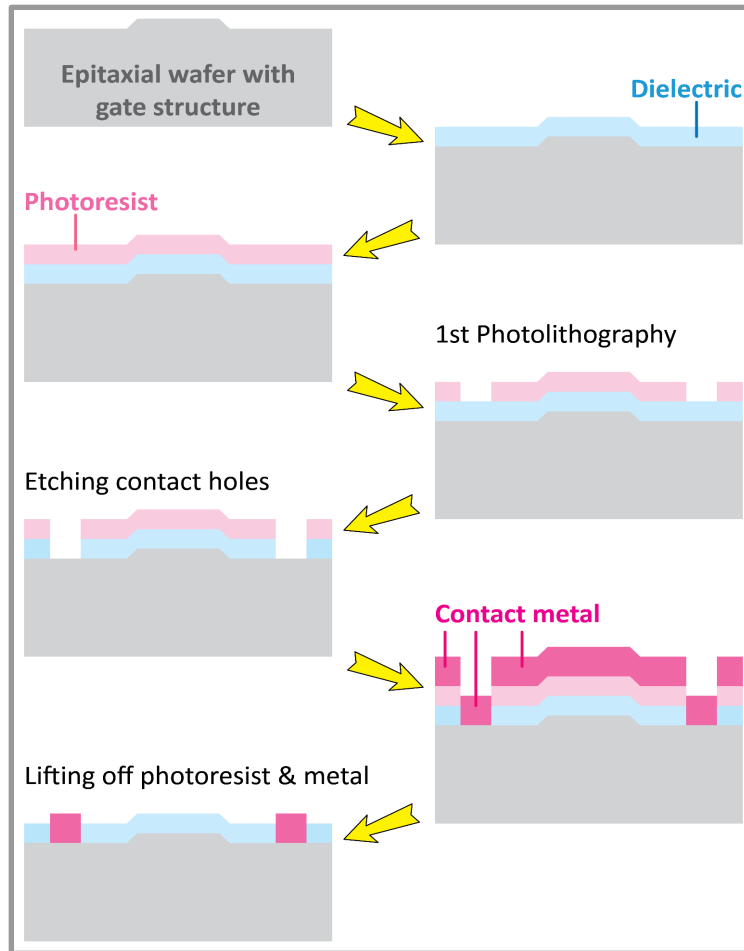
³ A photolithographic process is the process by which a photoresist is deposited, patterned, and developed on a layer to be etched. EX2001 ¶41. The patterned photoresist allows the etching process to remove specific material and form the desired structure. *Id.*



EX1001 FIG. 2

The sidewall edges of the dielectric do not align with the edges of the metal contact, thus forming a misaligned structure. EX2001 ¶69.

Alternatively, a single-photo mask process can be used to open the dielectric layer and form source and drain contacts. *Id.* at ¶71. The photo mask is used to pattern and create openings in the dielectric layer. *Id.* Then the contact metal is deposited across the wafer on the photo mask and the ohmic contacts are formed through a lift-off process, as shown below. This results in a structure where the edges of the contacts align with the edges of the dielectric material, as shown below. *Id.* However, the lift-off process does not allow the simultaneous formation of the field plate over the gate structure. *Id.*

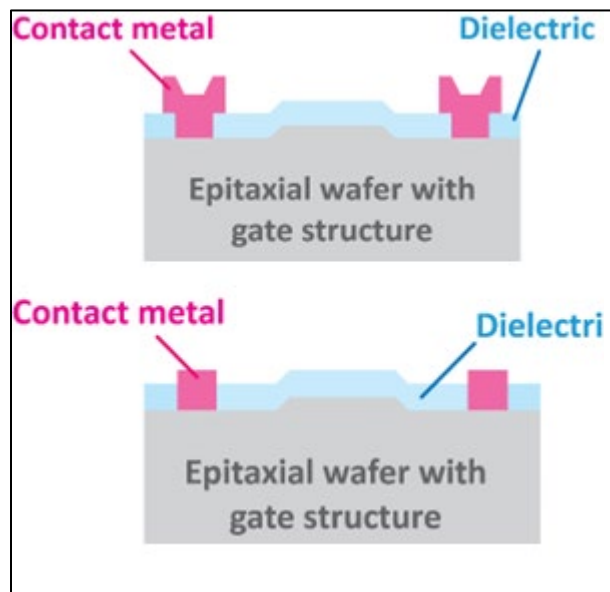


EX2001 ¶¶71-72

After the dielectric layer is deposited, the sole photolithography process proceeds to pattern and etch the contact holes. *Id.* The patterned photoresist remains in place when the contact metal is deposited. *Id.* The ohmic contacts are formed through the lift-off process that removes the contact metal above the patterned photoresist, leaving the ohmic contacts projecting vertically from the contact openings in the dielectric. *Id.* The process results in an aligned structure evident by both the use of a single photo mask for patterning and from alignment of the edges of the contacts with the edges of the dielectric. *Id.*

A two-photo-mask process for forming Ohmic contacts is substantially different in both process steps and resulting structure than a one-photo-mask process. *Id.* at ¶72-73. The two-mask process includes additional steps, including additional lithography steps, but permits the simultaneous formation of the source contact and field plate at source potential. The one-mask process includes fewer steps and results in an aligned sidewall structure. The two independent photolithography processes increase cost and time of manufacturing. *Id.*; EX2002 43:15-19. Finally, the resulting structure of the one-mask process is sidewall aligned (bottom figure below) in contrast to the two-mask process which results in overlap of the contact metal above the dielectric material (top figure below).

EX2001 at ¶72.



EX2001 ¶73

III. LEVEL OF ORDINARY SKILL IN THE ART

Patent Owner submits that a person of ordinary skill in the art would have possessed at least a four-year degree in electrical engineering, physics, material science, or a closely related field, and three years of professional work experience in the epitaxial growth, design, and fabrication of semiconductor electronic devices, including those of GaN. EX2001 ¶80. Relevant graduate education could substitute for the professional work experience. *Id.* Dr. Schubert opines, however, that the difference between Petitioner’s proposed POSA and Patent Owner’s would not affect his opinion or the outcome of this proceeding or change his opinion in any manner. *Id.* at ¶81.

IV. CLAIM CONSTRUCTION

The claims of the ’508 patent require a “gate-first” process. Based on the incomplete record presented by Petitioner, the Board preliminarily found that the dielectric layer must be deposited before the ohmic metal, but did not require the gate structure be formed before the source and drain contacts. Paper 11 at 12. As explained below, a more developed record conclusively demonstrates the ’508 patent requires a “gate-first” process to achieve the advantages of the “present invention,” and therefore the gate *must* be formed before the ohmic contacts.

Steps of a method claim are not ordinarily construed to require an order. *Mformation Techs., Inc. v. Research in Motion Ltd.*, 764 F.3d 1392, 1398 (Fed.

Cir. 2014). But a claim requires an ordering of steps when the claim language, as a matter of logic or grammar, requires that the steps be performed in the order written, or the specification directly or implicitly requires an order of steps. *Id.*; *see also Function Media, LLC v. Google, Inc.*, 708 F.3d 1310, 1320 (Fed. Cir. 2013). Indeed, the proper construction is to “capture the scope of the actual invention,” rather than allowing the claim language to become “divorced from what the specification conveys is the invention.” *Retractable Techs., Inc. v. Becton, Dickinson & Co.*, 653 F.3d 1296, 1305 (Fed. Cir. 2011).

In this case, the Board correctly reasoned that logic dictates that the dielectric layer steps [1f] must occur before the ohmic contact steps [1g]. Paper 11 at 12-13.

Similarly, when read in context of the specification, the gate formation [1e] must occur before the ohmic formation [1g]. The '508 patent describes the “present invention” as “an enhancement mode GaN HEMT with a ... self-aligned [gate], and a method for making such a device.” EX1001 3:1-4. The '508 patent further describes, as an additional feature to the “present invention”; “[f]urthermore, a field plate at source potential is patterned and etched together with drain and source ohmic contact metal.” *Id.* at 3:6-9.

Petitioner attempts to divorce the claim language from the disclosed “present invention” and impermissibly broadens the claim to include processes that cannot

achieve the formation of the field plate. Formation of the field plate is only achievable if the gate structure is formed before the ohmic metal is deposited (“gate-first”) such that the ohmic metal can be deposited *over* the formed gate structure. EX2001 ¶¶58, 74-75, 83; *see also* EX1001 at 3:21-23 (“The source metal 20 also serves as a field plate that extends over the gate and toward the drain contact”) (emphasis added). The field plate is simply the portion of the source ohmic contact metal that extends over the gate and *acts as* a field plate, as opposed to a separate element. EX1001 4:2-4:3. This is shown in every figure (except the prior art) in the ’508 patent. A field plate cannot be deposited over the gate structure, as shown in the figures, without the presence of the formed gate structure. EX2001 ¶¶58, 74-75, 83.

The claim language further recites every process step required to form the field plate feature of the present invention; specifically, “depositing an Ohmic contact metal; applying a metal photo resistant pattern; etching the Ohmic contact metal...performing rapid thermal annealing to form Ohmic drain and source contact.” The steps of depositing the ohmic metal and etching the Ohmic contact metal directly result in forming the source contact, a portion of which “acts as a field plate.” No additional unstated steps need to be performed for a portion of the source contact to serve as a field plate.

Proper construction must “capture the scope of the actual invention,” rather than allowing the claim language to become “divorced from what the specification conveys is the invention.” *Retractable Techs.*, 653 F.3d at 1305. Thus, Patent Owner’s proposed construction – that the claims require formation of the self-aligned gate structure [1e] before formation of the ohmic contacts [1g] – is the correct construction because it is consistent with every embodiment disclosed in the ’508 patent.

The ’508 patent describes two compatible features of the “present invention.”⁴ EX1001 3:1-9. A “gate-first” construction that permits the simultaneous formation of source and drain contacts with a field plate at source potential that extends over the gate structure is necessary to “tether the claims to what the specifications indicate the inventor actually invented.” *Retractable Techs.*, 653 F.3d at 1305; *see also Wi-Fi One, LLC v. Broadcom Corp.*, 887 F.3d 1329, 1346 (Fed. Cir. 2018) (“the claim must be read ... in order to be faithful to the invention disclosed in the specification”); *Medicines Co. v. Mylan, Inc.*, 853 F.3d 1296, 1305 (Fed. Cir. 2017) (restricting the claim to a specific process to avoid “the impermissible result of extending [the] monopoly beyond the invention

⁴ Indeed, the parties agree the “present invention” requires a self-aligned gate, even though claim 1 does not recite such language.

disclosed, and potentially to the prior art.”) (internal quotations omitted); *Gemalto S.A. v. HTC Corp.*, 754 F.3d 1364, 1369-71 (Fed. Cir. 2014) (affirming narrow construction based on purpose of invention and distinctions over prior art because “the claims cannot be of broader scope than the invention that is set forth in the specification.”) (internal quotations omitted); *Renishaw PLC v. Marposs Societa’ per Azioni*, 158 F.3d 1243, 1250 (Fed. Cir. 1998) (“construction that stays true to the claim language and most naturally aligns with the patent’s description of the invention will be, in the end, the correct construction.”).

In *all* embodiments described in the ’508 patent, the single photo mask self-aligned process is first used to produce the gate structure, and subsequently, the ohmic contact formation process includes simultaneously forming a field plate. Petitioner’s proposed claim construction allows the gate formation process (e.g., [1e]) to occur at any point in the process, including after the formation of the gate contacts (e.g., [1g]), thereby **preventing** the simultaneous formation of the source and drain contacts with a field plate at source potential and extending over the gate structure to reduce the electric field at the drain corner of the gate. Such a broad construction is inconsistent and contrary to the disclosed invention. Regardless of the “comprising” nature of claim 1, only a “gate-first” process can achieve the “present invention” and meet the claim language. See EX2001 ¶¶82-83; EX2002 84:19-101:12 (discussing EX2003 at 2 (illustrating dielectric, ohmic, gate process

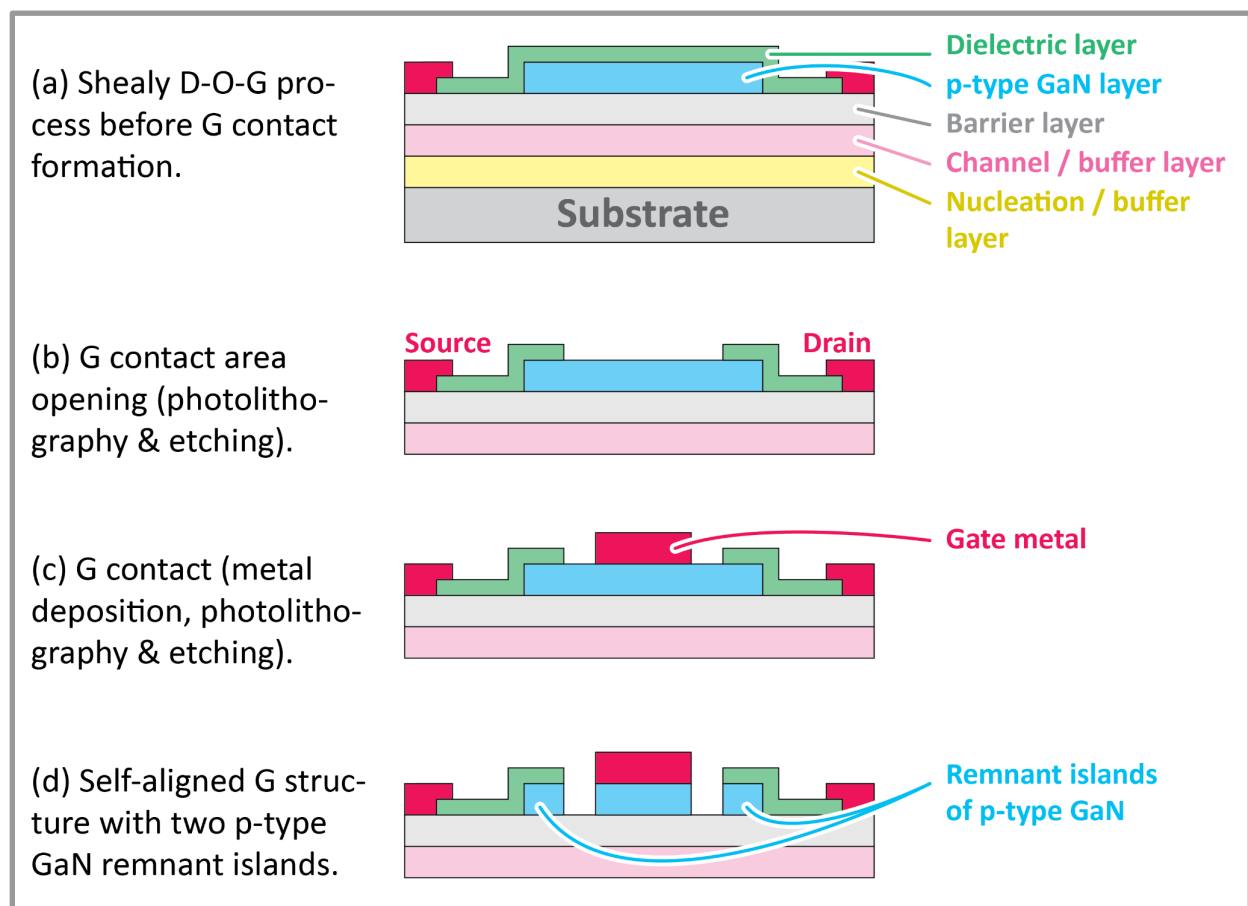
not being able to simultaneously form a field plate with ohmic contact), 3 (illustrating gate, dielectric, ohmic permitting the formation of a field plate together with ohmic contacts), 4 (illustrating ohmic, gate, dielectric not permitting formation of field plate together with dielectric)).

During re-direct examination at his deposition, Petitioner's expert, Dr. Shealy, for the first time, opined that the claims of the '508 patent do not require any particular fabrication process order. *See, e.g.*, EX2002 82:1-25. Indeed, Dr. Shealy testified that any process order would be within the scope of the claims, and that, therefore, Petitioner did not identify a particular order in the Petition.

Dr. Shealy provided three figures illustrating forming GaN devices according to different orders of gate formation, dielectric formation, and ohmic formation: 1) a dielectric, ohmic, gate process (referenced as a "D, O, G" process); 2) a gate, dielectric, ohmic process (referenced as a "G, D, O" process); and 3) an ohmic, gate, dielectric process (referenced as an "O, G, D" process). *See* EX2002 84:19-101:12 (referring to **D**ielectric, **O**hmic, and **G**ate); EX2003 2-4. Each of these would require significant modifications to the prior art relied on, which Petitioner failed to address.

Dr. Shealy first described the "D, O, G" process, or a dielectric first, ohmic contact formation second, and gate contact third. *See* EX2002 92: 4-93:13, 94:8-95:23. The D-O-G process would require multiple modifications—none of which

are explained by the Petition – to the prior art of record, does not follow any of the prior art references, and in some instances is contrary to the teachings of the cited prior art. EX2001 ¶¶89-90. Importantly, the gate electrode process as described by Dr. Shealy would not work because it would leave remnant islands of the p-type semiconductor, for example, p-type GaN in the context of the '508 patent, between the source and gate as well as between the gate and drain. Such remnant islands (shown below) are detrimental to the function of an enhancement mode HEMT and a POSA would not proceed in such a manner. *Id.* at ¶90.



EX2001 ¶90

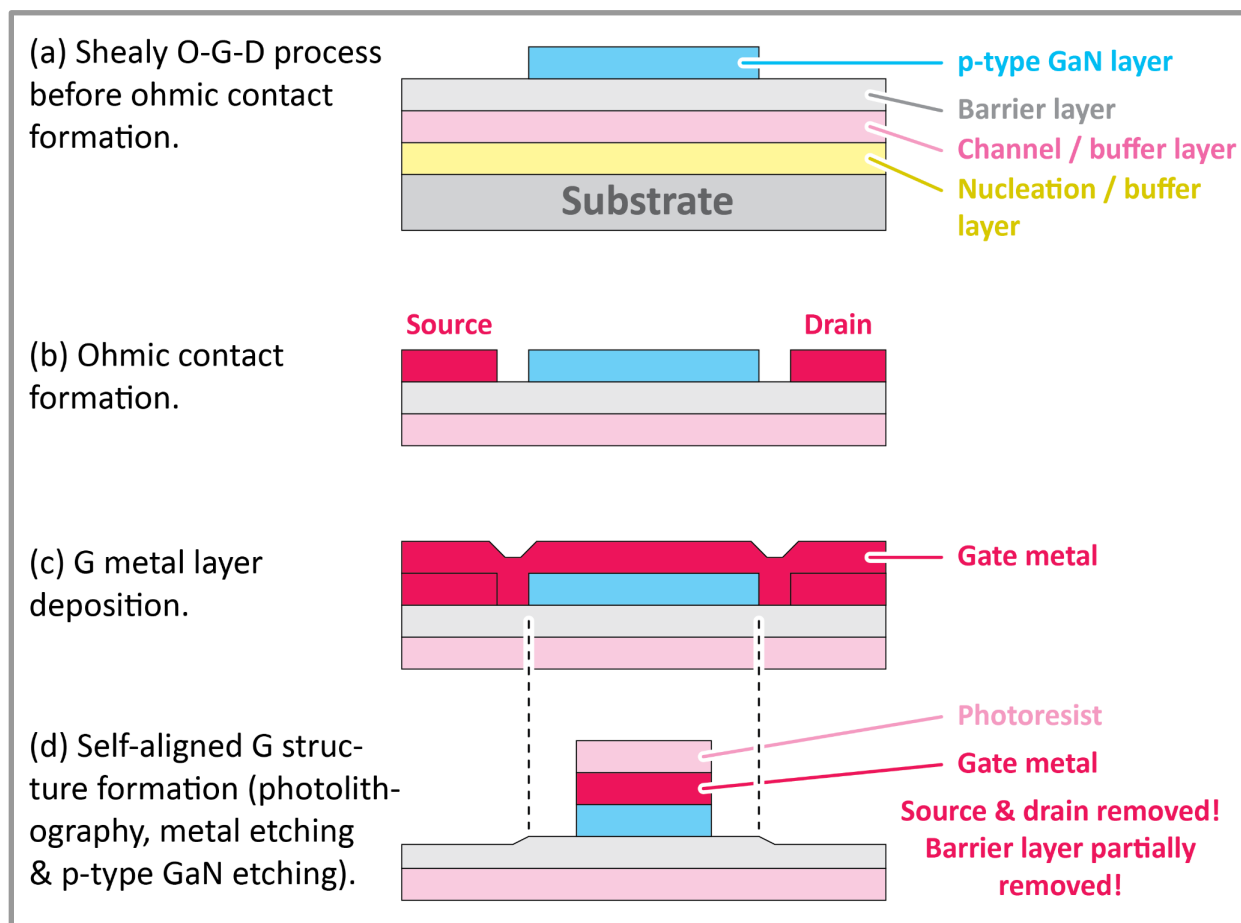
Accordingly, as explained in Dr. Schubert's Declaration, Dr. Shealy's proposed "D-O-G" process not a viable process. EX2001 ¶¶90-91.

Dr. Shealy next described the "G, D, O" process, where the gate is formed first, followed by the dielectric and the ohmic process last. EX2002 96:9-98:9; Exhibit 2003. This is the process described and claimed in the '508 patent. Indeed, Dr. Shealy's G-D-O process is a carbon copy of the '508 patent's process. EX2001 ¶¶92. That makes sense since the Petition is based on impermissible hindsight using the '508 patent's disclosure as a roadmap.

Finally, Dr. Shealy testified about the hypothetical "O, G, D" process. EX2002 98:18-100:21; Exhibit 2003. But there are multiple technical issues with Dr. Shealy's O-G-D process, as illustrated below. In the process, the source and drain contacts are deposited on the barrier layer after the p-type GaN layer has been removed. Subsequently, a gate metal layer is deposited. A photoresist pattern is applied on the gate metallization and the metal layer outside the gate contact region is etched away. Importantly, the metal etch will not only remove the gate metallization, but also the source and drain contact metallization, as shown in the figure below. Furthermore, when performing the self-aligned gate structure process, the p-type GaN layer has already been removed in regions outside the general gate area (see top sub-image of process sequence below), so that the semiconductor etching process will etch not only the p-type GaN layer, but also

detrimentally etch the barrier layer (see bottom sub-image sequence below).

EX2001 ¶96 (discussing EX2002 98:11-100:14). Thus, Dr. Shealy's O-G-D process suffers from multiple conflicts and incompatibilities that deteriorate the device properties to the degree that it is non-functional. *Id.*



EX2001 ¶96

Hence, for all of the above reasons, regardless of the “comprising” transition claim structure, only a “gate-first” process can achieve the “present invention,” meet the claim language, and result in a functional transistor.

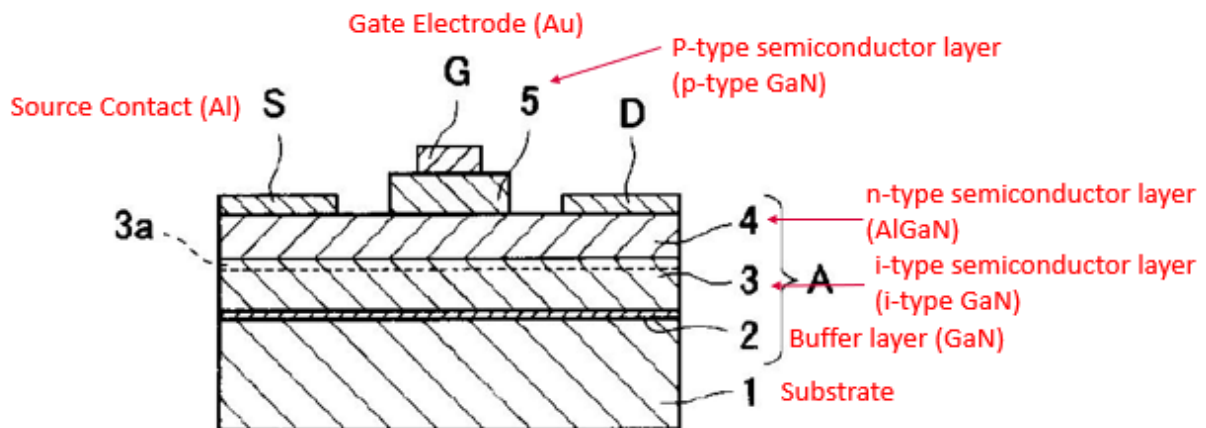
V. RESPONSE TO ALLEGED STATEMENT OF FACTS

Petitioner's alleged Statement of Material Facts (Pet. 11-13) is misleading and facially deficient. The Board should give the Statement of Material Facts no weight. Moreover, Petitioner fails to include any citations to the record supporting any of its alleged facts (*see* 37 C.F.R. § 42.22(c)), and therefore, the alleged facts should not be assumed into evidence.

VI. OVERVIEW OF REFERENCES RELIED UPON

A. Yoshida

The GaN device of *Yoshida* includes substrate 1, buffer layer (GaN) 2, i-type semiconductor layer (iGaN) 3, n-type semiconductor layer (n-type AlGaN) 4, p-type semiconductor layer (p-type GaN) 5, gate electrode G, and source S and drain D electrodes. EX1004 ¶¶[0011]-[0016], [0019]-[0023]; EX2001 ¶100.



EX2001 ¶85

Yoshida forms its gate electrode G *after* first etching p-type GaN layer 5 and forming source S and drain D electrodes. EX1004 ¶¶[0022]-[0023]; EX2001 ¶101;

EX2002 56:25-57:20. The gate electrode is the final electrode formed, thereby rendering Yoshida a “gate-last” process. *Id.*

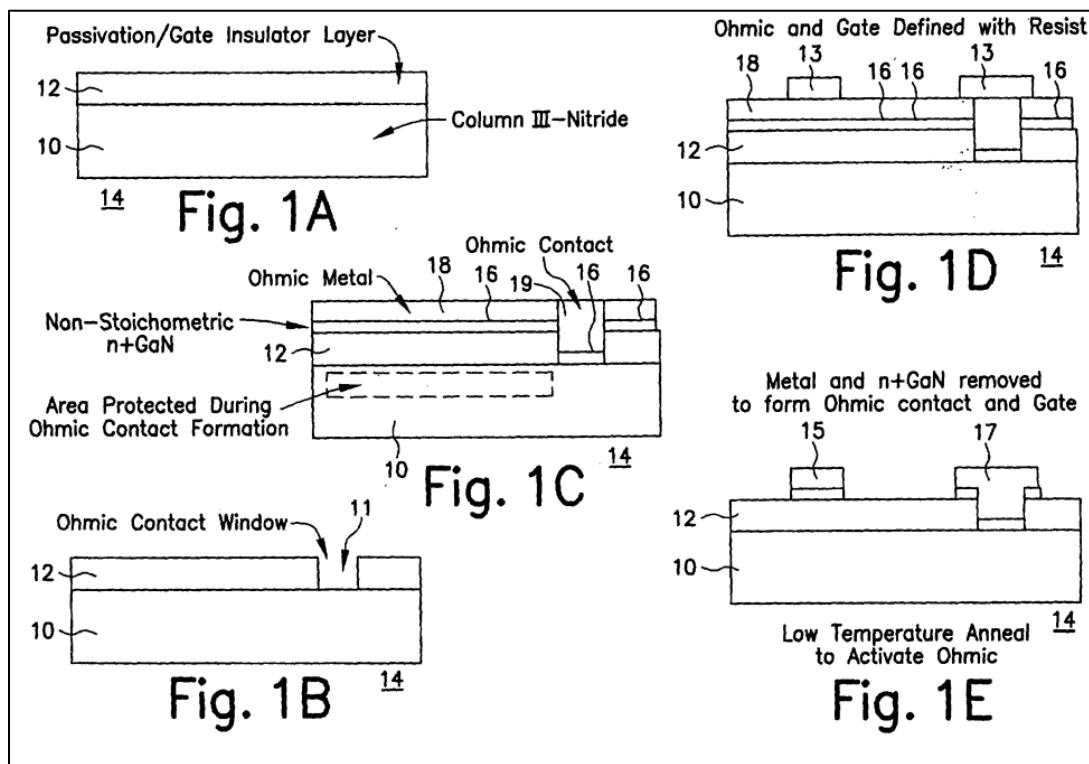
Yoshida describes an epitaxial process by which p-type GaN layer 5 is grown across the wafer. EX1004 ¶¶[0011]-[0015], [0019]-[0021]; *see also* EX2001 ¶102. The fabrication process begins with etching the p-type GaN layer. EX1004 ¶[0022]; EX2001 ¶103. Then, a SiO₂ layer is deposited over the wafer and the etched p-type GaN layer. EX1004 ¶[0022]; EX2001 ¶104. The SiO₂ layer is then patterned with a photoresist and etched to open areas for the source and drain electrodes. *Id.*

Once deposited and formed, the source and drain electrodes are masked and an opening in the SiO₂ over the etched p-type GaN material is formed, and the gate electrode metal is deposited over the etched p-type GaN and etched to form the gate electrode and complete the process. EX1004 ¶¶[0016], [0023]; EX2001 ¶¶104-105. *Yoshida's* process for forming the source and drain electrodes is a single-mask ohmic formation process applying a lift-off process. EX1004 ¶[0022]; EX2001 ¶104.

B. Beach

Beach describes a “gate-simultaneous” process for forming a depletion mode transistor, whereby the gate 15 and ohmic 17 contacts (Figure 1E) are formed

simultaneously in the same process step from the same ohmic metal. This process is shown in Figures 1A-1E below.



EX1005 FIGS. 1A-1E.

Beach describes a process of manufacturing a *depletion mode* transistor, not an enhancement mode transistor as claimed. As discussed below, *Beach* does not include a p-type GaN layer between the gate contact and its barrier layer, but instead discloses an n-type material (EX2002 63:10-14); therefore, its transistor would not deplete the 2DEG below the gate at 0V. EX2001 ¶107.

As shown in Figure 1A, III-nitride layer 10 and gate insulator layer 12 are formed on a substrate. EX1005 ¶¶[0039]-[0040]. Next, “an ohmic contact window 11 is opened in layer 12 to provide access to layer 10 for the deposition of

an ohmic contact.” *Id.* at ¶[0042]. Subsequently, as shown in Figure 1C, a non-diffusive protective n-type material 16 is deposited over the surface of insulator layer 12 and in ohmic contact window 11. EX1005 ¶[0043]; EX2002 63:19-24. Next, ohmic metal layer 18 is deposited. EX1005 ¶[0045].

Beach initiates its photolithographic process to simultaneously pattern, etch, and form the gate 15 and ohmic 17 contacts. *Id.* at ¶[0045]; EX2001 ¶¶108-112. As shown in Figure 1D, “resist material 13 is deposited in a pattern to permit the formation of a gate 15 and ohmic contact 17” in a coupled fabrication process using a single photolithographic process to deposit resist material 13 over the ohmic material. EX1005 at ¶[0047]. Then ohmic metal layer 18 and material layer 16 are etched to form gate 15 and ohmic contact 17 simultaneously out of ohmic metal layer (“gate-simultaneous”). *Id.*; EX2001 ¶111.

C. Sheppard

Sheppard describes a “gate-last” process, as depicted by Figures 1A-1F, reproduced below.

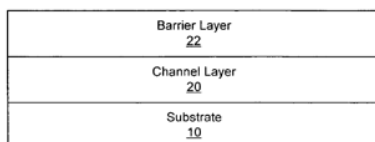


Figure 1A

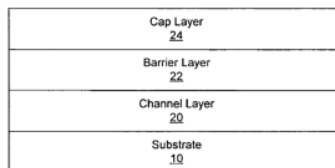


Figure 1B

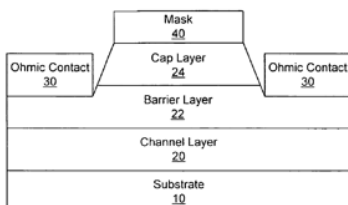


Figure 1C

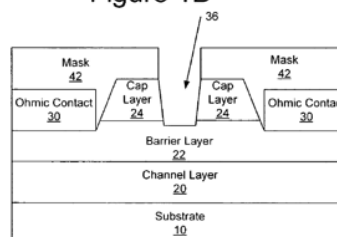


Figure 1D

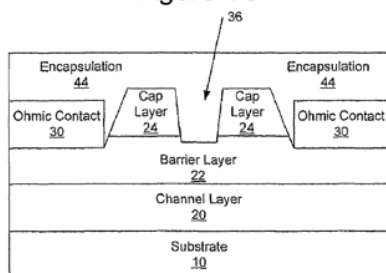


Figure 1E

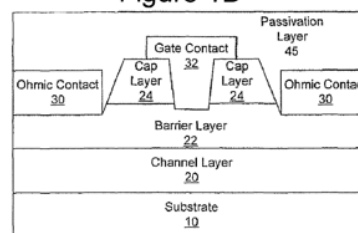


Figure 1F

EX1006 FIGS. 1A-1F

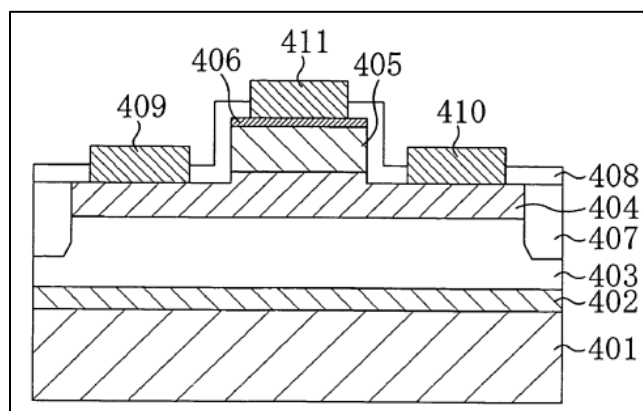
After deposition of channel layer 20, barrier layer 22, and cap layer 24 on substrate 10 (EX1006 7:26-28 and 7:47-54), mask layer 40 is deposited and cap layer 24 is patterned and etched to open windows for forming ohmic contacts 30, as shown in Figure 1C. *Id.* at 8:55-63. Notably, the gate has not been formed.

The subsequent gate formation is shown in Figures 1D-1F reflecting *Sheppard's* process of forming the gate contact 32 *after* forming the ohmic contacts 30. EX2002 69:3-70:18. Indeed, as shown in Figure 1F, the gate contact 32 is formed last. EX1006 at 4:58-5:2, 10:46-50. Because *Sheppard* forms the

gate contact *after* the ohmic contacts, it is a “gate-last” process. EX2001 ¶¶113-117.

D. Hikita347

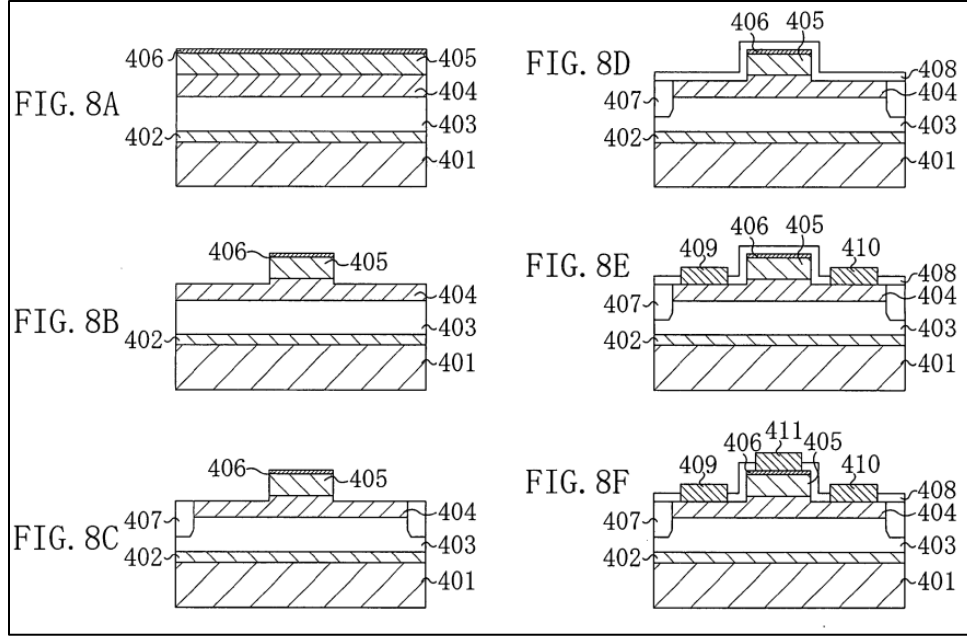
Hikita347 describes an enhancement mode GaN transistor made by a “gate-last” process. EX1007 ¶¶[0001], [0011]; EX2001 ¶¶124-126. *Hikita347*’s transistor includes substrate 401, AlN buffer layer 402, undoped GaN layer 403, undoped AlGaN layer 404, p-type AlGaN layer 405, heavily doped p-type GaN layer 406, gate electrode 411, source electrode 409, and drain electrode 410. EX1007 at ¶[0048], Fig. 4.



EX1007 FIG. 4

Notably, *Hikita347* corresponds to the device identified in Fig. 1 of the ’508 patent as “Prior Art” and was also considered by the USPTO during prosecution. Compare EX1007 Fig. 4 with EX1001 1:53-2:14, Fig. 1; see also EX1001 [56] (references cited).

Hikita347 describes its gate-last process of making the Figure 4 transistor, as shown in Figures 8A-8F. EX1007 ¶¶[0055]-[0061].



EX1007 FIGS. 8A-8F

After the epitaxial layers 402-406 are sequentially grown on the substrate, p-type GaN layer 406, p-type AlGaIn layer 405 and a portion of AlGaIn layer 404 are etched. EX1007 ¶¶[0035], [0040], [0056]-[0057], Fig. 8B. Notably absent is any gate contact.

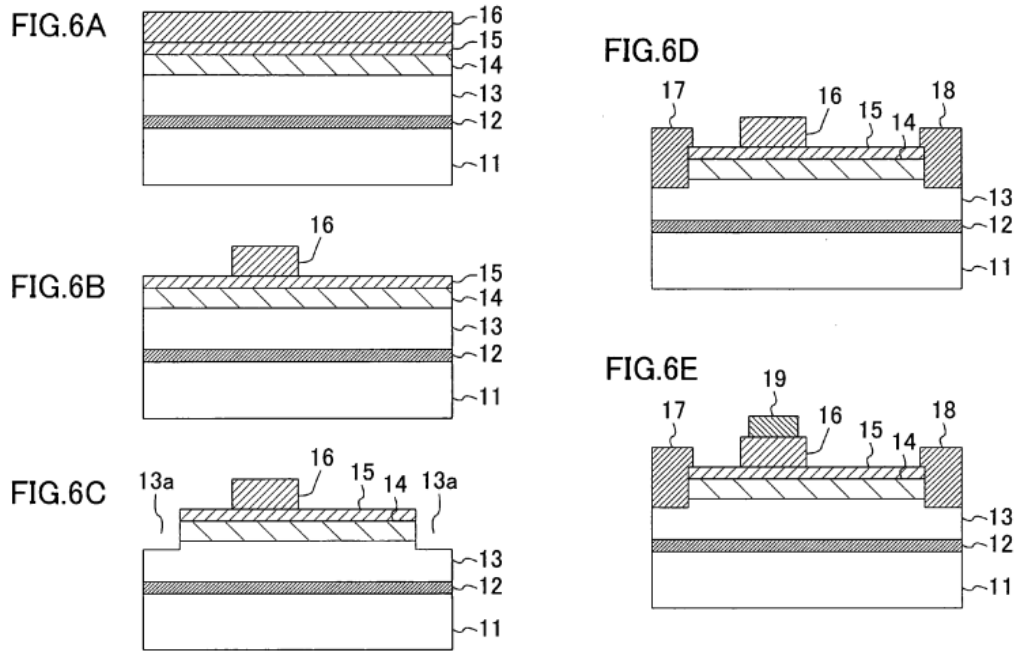
Figures 8D-8F illustrate the formation of ohmic contacts (409, 410) *before* forming gate contact 411. As shown in these figures, SiN film 408 is deposited over the entire structure (Figure 8D), is selectively etched to create openings for the ohmic contacts (409, 410) which are deposited in the openings. *Id.* at ¶¶[0059]-[0060]; EX2001 ¶¶123-124. Finally, after forming source and drain electrodes, an opening is created in SiN film 408 above etched semiconductor layers 405 and 406. EX1007 at ¶[0061].

Hikita347 only describes a single photo mask ohmic contact formation process (opening the SiN film), which infers to a POSA that a lift-off process occurs to pattern the ohmic contact. EX2001 ¶123. Figure 8E illustrates a sidewall aligned ohmic structure resulting from a lift-off process. *Id.* ¶¶123-124.

In an embodiment, *Hikita347* describes that “[t]he source electrode 409, the drain electrode 410 and the gate electrode 411 may be formed before formation of the SiN film 408” (EX1007 ¶[0061]), but *Hikita347*’s source and drain contacts are always formed *before* the gate metal is deposited. Therefore, *Hikita347* describes forming the gate electrode after the source and drain electrodes, i.e., a “gate-last” process. EX2001 ¶¶124-126; EX2002 71:22-72:12.

E. Hikita023

Hikita023 discloses an enhancement mode GaN transistor made by a “gate-last” process, as illustrated by Figures 6A-6E, reproduced below. EX1008 ¶¶[0014], [0037], [0076], [0080].



EX1008 FIGS. 6A-6E

Like all the other “gate-last” processes, ohmic contact 17 and 18 are formed *before* gate contact 19. *See id.*, at Figures 6D and 6E; EX2001 ¶¶116-18; EX2002 80:3-8.

Like *Hikita347*, *Hikita023* describes forming source electrode 17 and drain electrode 18 by a liftoff method. EX2001 ¶132-134; EX1008 ¶[0078].

VII. GROUND 1: *YOSHIDA* IN VIEW OF *SHEPPARD* AND *BEACH* DOES NOT RENDER CLAIMS 1-3 UNPATENTABLE

A. A POSA Would not have been Motivated to Combine the References

“A party seeking to invalidate a patent on obviousness grounds must demonstrate ... that a skilled artisan would have been motivated to combine the teachings of the prior art reference to achieve the claimed invention....” *InTouch Techs., Inc. v. VGo Commc’ns., Inc.*, 751 F.3d 1327, 1347 (Fed. Cir. 2014); *see*

also *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418, (2007) (“[R]ejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.”) (quoting *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)).⁵ In *InTouch*, the Federal Circuit vacated a finding of invalidity because the defendant’s expert opined that the elements of the claim existed in the prior art but failed to explain how to combine the elements:

Dr. Yanco’s testimony was nothing more than impermissible hindsight; she opined that all the elements of the claims disparately existed in the prior art, but failed to provide the glue to combine these references. While she opined that the references were like separate pieces of a simple jigsaw puzzle, she did not explain what reason or motivation one

⁵ Although *InTouch* applies the district court burden of proof, the remainder of the analysis remains applicable. See also *Aylo Freesites Ltd., v. Dish Techs. L.L.C.*, No. IPR2024-00147, 2024 Pat. App. LEXIS 1528 at *19 (P.T.A.B. Apr. 25, 2024) (finding that because a POSA *could* have modified a prior art reference instead of *would* have modified a prior art reference insufficient to establish obviousness) (citing *Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1073 (Fed. Cir. 2015) (citing *InTouch*, 751 F.3d at 1352))).

of ordinary skill in the art at the time of the invention would have had to place those pieces together.

Id. at 1348-49.

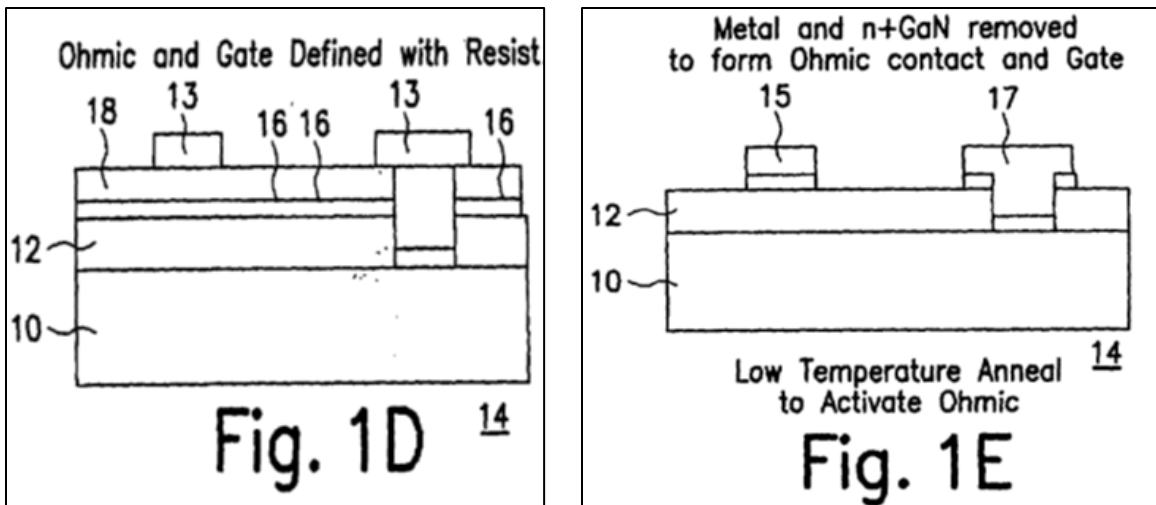
In this case, Petitioner does not explain how the pieces of the puzzle fit together, much less why a POSA would have been motivated to combine the pieces. Petitioner goes from one limitation to the next, picking and choosing the reference it is relying on to meet that limitation without tying any motivation to the particular references and their processes or explaining how the “pieces of the jigsaw” actually even fit together to allegedly achieve the elements of the claim. EX2001 ¶135. Simply put, even if one were to have been motivated to combine the references identified by Petitioner, because Petitioner failed to particularly explain the combination, it is impossible to determine whether a POSA would have expected to successfully combine the references, and whether that unidentified process flow would yield an operable device.

Yoshida and *Sheppard* both describe “gate-last” processes. EX2001 ¶¶101, 113-117, 143; EX2002 56:25-57:20; EX1004 ¶¶[0022]-[0023]; EX1006 8:55-63, 4:58-5:2, 10:46-50. *Beach* describes a “gate-simultaneous” process applying and using a single photo resist to form both the gate and ohmic contacts. EX2001 ¶¶111-112, 141; EX1005 ¶[0047].

Petitioner argues a POSA would have been motivated to use *Beach*'s single-mask process to form the gate structure to improve *Yoshida*'s device and process. Pet. 21. But Petitioner never proposes modifying *Yoshida* in view of *Beach* to obtain a "gate-first" process nor does Petitioner provide any motivation to modify *Yoshida*'s "gate-last" process to have the gate formation process occur before ohmic contact formation. Further, Petitioner fails to explain why it would have been obvious to modify *Yoshida* in view of *Beach* to obtain a "gate-first" process – especially given that neither *Yoshida* nor *Beach* disclose a "gate-first" process. Indeed, a POSA would not have been motivated to perform a "gate-first" process due to known detriments of an ohmic contact anneal affecting the gate contact, such as deterioration of the contact due to the excessive heating. EX2001 ¶144. Petitioner's expert on redirect examination readily concedes that "there are good reasons not to necessarily choose that path." EX2002 85:19-86:8, 95:11-23.

Moreover, *Beach*'s teaching of simultaneously forming the gate contact and ohmic contacts is inconsistent and contrary to the teachings of *Yoshida*, which etches the p-type GaN prior to depositing the gate metal, unlike *Beach* which does not etch the n-doped gate region prior to etching the gate electrode. EX2001 ¶145; EX1004 ¶[0022] ("where the gate electrode was to be loaded").

Beach's "gate-simultaneous" process is shown in the figures below.



EX1005 FIGS. 1D-1E

As seen in these figures, *Beach* describes a transistor having III-N channel layer 10, and gate insulator 12. *Beach* forms openings in gate insulator 12 and deposits protective layer 16. EX1005 ¶¶[0042]-[0043], [0048]. Then, *Beach* deposits metal layer 18 and applies photoresist pattern 13 on the metal layer. *Id.* at ¶¶[0046]-[0047]. These steps result in the device in *Beach* Figure 1D. Subsequently, *Beach* simultaneously forms the gate and ohmic contacts through a single etching process. *Id.* at ¶[0048]; EX2001 ¶146. Notably, *Beach* forms both contacts from the same metal layer 18. *Id.*

Conversely, *Yoshida* discloses a significantly different process and has a significantly different structure at both the time of forming its gate electrode and at the time of forming its ohmic contact. EX2001 ¶150. *Yoshida* forms the drain and source contacts *before* the formation of a gate electrode. See EX1004 ¶¶[0021]-[0023]. As such, *Yoshida* discloses a “gate-last” process, in which the gate is

fabricated after the source and drain contacts have been fabricated, and is not an applicable starting point for combining the “gate-simultaneous” process of Beach. *Id.*

Petitioner fails to provide a particular motivation for abandoning *Yoshida*’s distinctly different “gate-last” formation process and substituting *Beach*’s “gate-simultaneous” formation process or portions thereof. EX2001 ¶148. It is not enough to simply “pick out ... two references and combine them to arrive at the claimed invention.” *Personal Web Technologies v. Apple*, 848 F.3d 987, 993-94 (Fed. Cir. 2017).

Indeed, *Beach*’s “gate-simultaneous” formation is uncommon and results in additional restrictions on the process. EX2001 ¶149. Importantly, contrary to the claims of the ’508 patent, Beach’s “gate-simultaneous” process requires the same metal for the gate contact and ohmic contacts. *Id.* It further requires the gate contact to be subject to the detrimental anneal process to form the gate contact. *Id.* These factors make it unfavorable, if not impossible, to modify *Yoshida*’s “gate-last” process with *Beach*’s “gate-simultaneous” process. *Id.*

Further, the proposed combination of a “gate-last” and “gate-simultaneous” process would result in an inoperable device. If the gate metal is deposited on the p-type GaN layer of *Yoshida*, followed by the process of *Beach* of simultaneously forming the gate and ohmic contacts, the ohmic contacts would be formed on the

p-type GaN material rather than on the AlGaN barrier layer. *Id.* at ¶150.

Petitioner's proposed combination thus calls for such an inoperable device. *Id.*

Petitioner's alleged motivation to combine fails to cure these deficiencies. Petitioner argues that a POSA would be motivated to combine *Yoshida* and *Beach*, because the combination achieves *Yoshida*'s objective of etching the doped GaN layer except where the gate contact is to be loaded, and that self-aligned gate etching processes, such as in *Beach*, were "well-known" in the art and "conventional." Pet. 21-22. But a "gate-simultaneous" process would obviously not etch away the doped GaN layer under the ohmic contact, which is also formed in the same process. EX2001 ¶152. In addition, although self-aligned processes in other contexts may have been known, Petitioner does not explain why a POSA would have any expectation of success in modifying *Yoshida*'s process that deposits the gate metal on an *already etched* p-type GaN layer. As *Yoshida* describes an etching process to pattern the p-type GaN layer prior to gate metal deposition, there is no benefit in reducing the overall number of etching steps or simplifying the process. EX2001 ¶153. Indeed, incorporating a self-aligned process into the process of *Yoshida* would necessitate removing *Yoshida*'s dielectric layer to open an area for gate electrode deposition and self-alignment. Therefore, a POSA would not have been motivated to modify *Yoshida* to incorporate teachings from the "gate-simultaneous" process of *Beach* because it

provides no benefit, and instead further complicates the process. *Id.* And even if a POSA sought to combine the two references, it would not have been obvious to combine a “gate-simultaneous” process with a “gate-last” process to obtain a “gate-first” process.

B. Petitioner’s “Mix and Match” Approach is Premised on Impermissible Hindsight

Petitioner’s hindsight reasoning is apparent. Petitioner essentially divides the claim into different formation/masking processes (*see, e.g.*, Pet. 13 (citing [1e] and [1g])), but does not describe how the respective processes could be combined to form a step-by-step cohesive process meeting claim 1. Moreover, Petitioner fails to explain how such modifications would affect the process described in *Yoshida* or form an operable device. EX2001 ¶154.

At no point does Petitioner actually propose modifying a specific step in *Yoshida* to incorporate *Beach*; instead, Petitioner simply adopts *Beach*’s “gate-simultaneous” process without any explanation of how to incorporate the process in *Yoshida*’s “gate-last” process or what portions of *Beach*’s process to incorporate into *Yoshida*’s process. *See, e.g.*, Pet. 21-24, 30-33, 35-39. Petitioner’s failure to articulate how the proposed combination would be implemented is fatal to its argument and highlights its reliance on impermissible hindsight.

As best understood, Petitioner proposes applying the source and drain contact formation process of *Beach* to *Yoshida*’s lift-off process. EX2001 ¶155;

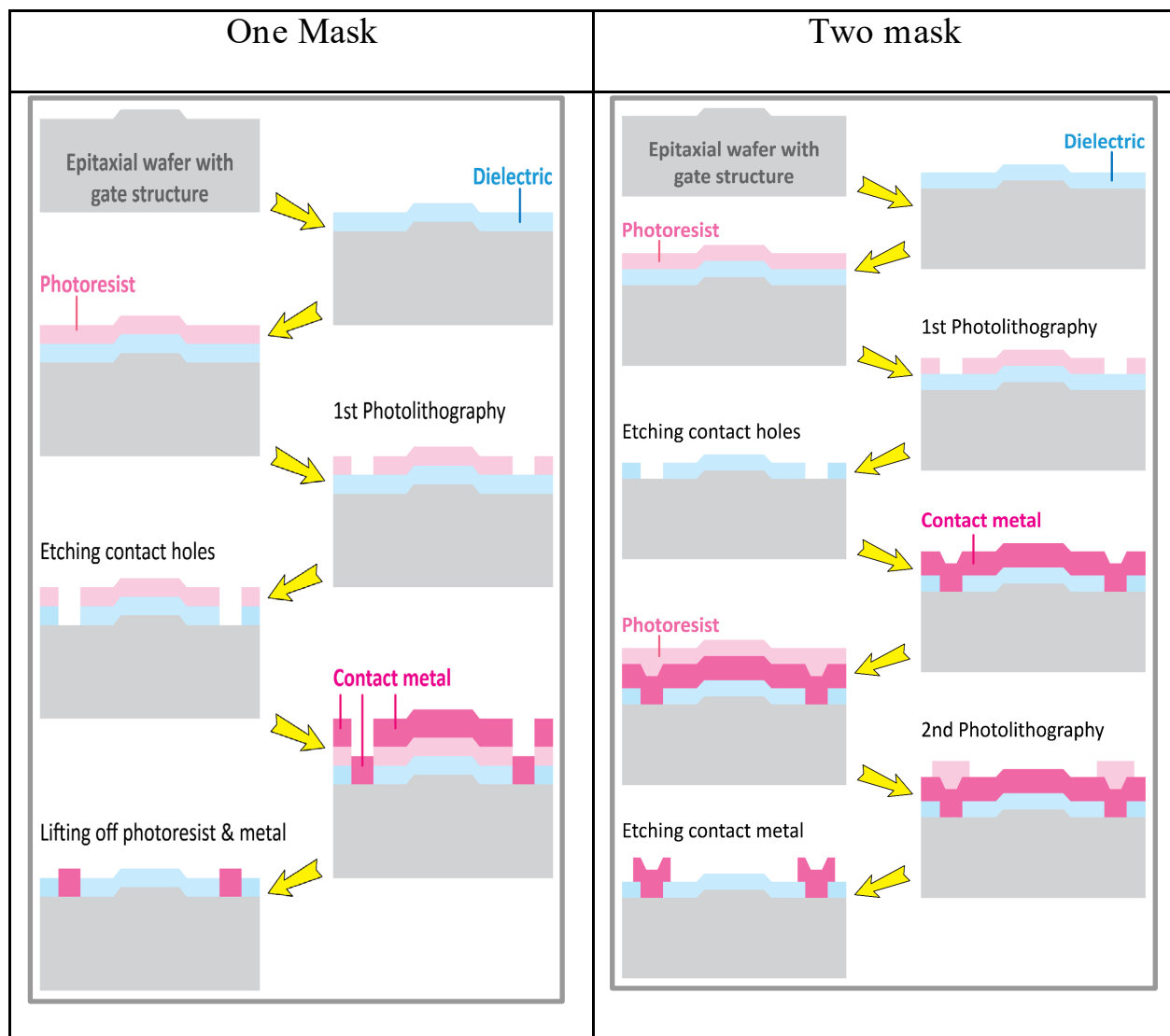
Pet. 23-24, 35-39. But Petitioner provides no detail as to when or how Beach's "gate-simultaneous" process would be incorporated in *Yoshida*'s "gate-last" process, e.g., after the gate material is etched but before the gate contact is deposited, or before or after modified *Yoshida* has etched both the gate contact and gate material with a single patterned photoresist. EX2001 ¶155.

As another example, *Yoshida* describes etching its p-type GaN layer, depositing a SiO₂ material, and forming its ohmic contacts before depositing its gate electrode. EX1004 ¶¶[0022]-[0023]. Petitioner fails to explain how it would modify *Yoshida* and *Beach* to perform a self-aligned etching process on the deposited gate electrode and already etched p-type GaN layer given the intervening SiO₂ materials and ohmic source and drain contact. EX2001 ¶156. Indeed, *Beach*'s "gate-simultaneous" process does not contemplate the process of *Yoshida*, where the ohmic materials are already formed at the time of gate electrode patterning. *Id.* Hindsight is the only explanation to make such a substitution.

Ultimately, Petitioner's hindsight cobbling together of elements from multiple prior art sources without explaining the hypothetical process itself, or why a POSA would be motivated to perform the *combined* hypothetical process, is insufficient to meet its burden. As such, absent hindsight, a POSA would not have been motivated to incorporate the teachings of *Beach* into *Yoshida* to meet limitations [1e2] and [1g2].

C. Petitioner Provides No Motivation to Replace *Yoshida*'s One Mask Ohmic Formation with *Beach*'s Two Mask Process

Yoshida describes a single-mask ohmic formation process applying a lift-off process. EX1004 ¶¶[0022]; EX2001 ¶157. In contrast, *Beach* describes a two-mask process that deposits and etches multiple materials. As Dr. Schubert explains, these are two fundamentally different processes that result in different structures. EX2001 ¶¶157-160.



EX2001 ¶157

As shown, *Yoshida* first deposits SiO₂ over the etched p-type GaN layer, applies a photoresist, etches both SiO₂ and photoresist to create openings for ohmic metal deposition. EX1004 ¶¶[0022]-[0023]; EX2001 ¶158. After deposition, the excess contact metal layer and the photoresist are removed by lifting off those layers. EX2001 ¶158 (explaining that the figures and specification of *Yoshida* inform a POSA that a lift-off process is used to form the ohmic materials). The resulting structure, as shown in *Yoshida*'s figure (below), has ohmic contacts having vertical linear sidewalls entirely aligned with the etched dielectric material indicative of a self-aligned lift-off process. *Id.*

In contrast, *Beach* describes a two-mask ohmic formation process. EX2001 ¶159. A dielectric layer is deposited, a photoresist is deposited, using a first mask, the photoresist is patterned and ohmic contact openings in the dielectric layer are formed. *Id.* The photoresist is removed and contact metal material is deposited. *Id.* A second photoresist layer is deposited, and using a second mask, is patterned (*Beach*'s resist 13) for removal of the excess metal contact material resulting in the ohmic contacts. *Id.*

The difference between *Yoshida* and *Beach* is evident from the figures of the references. EX2001 ¶160.

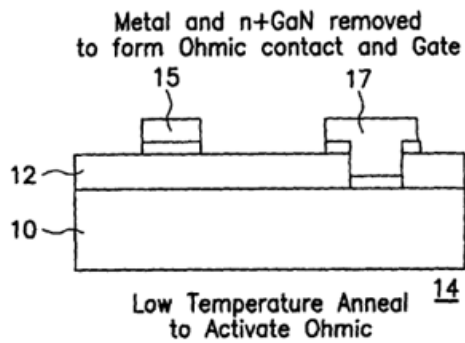
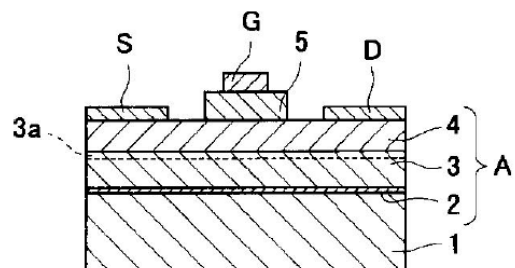


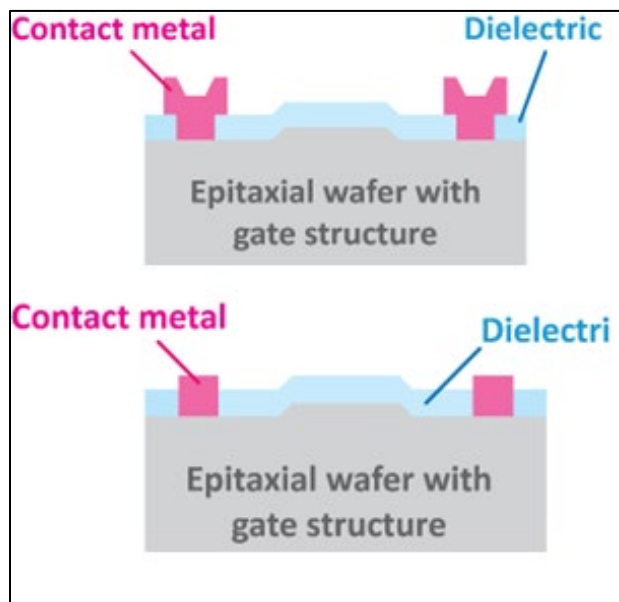
Fig. 1E

EX1005 FIG. 1E



EX1004

A single-mask process is materially different than a two-mask process, resulting in different structures, as shown below. EX2001 ¶160.



EX2001 ¶160

Petitioner fails to provide any motivation for a POSA to replace the faster, cheaper, and more efficient single-mask ohmic formation process of *Yoshida* with *Beach*'s two-photo mask process. *Id.* at ¶161. Indeed, substituting a two photo-

mask process for a one photo-mask process is contrary to Petitioner's own position that a POSA would seek to use a simpler single-mask process to simplify manufacturing process and save costs. Pet. 21-22; *see also* EX1003 ¶126 (Shealy); EX2002 42:5-43:19.

A lift-off process as in *Yoshida* provides a simpler patterning process, advantageously self-aligning the ohmic contacts with the SiO₂, which also allows complete removal of the dielectric as shown in *Yoshida*. EX2001 ¶162. In contrast, a two-mask ohmic contact formation process, as in *Beach*, results in remaining non-self-aligned ohmic material shielding underlying material, as shown in *Beach* (annotated below in red), thereby preventing complete removal of that material, which stands in stark contrast to *Yoshida*. *Id.*

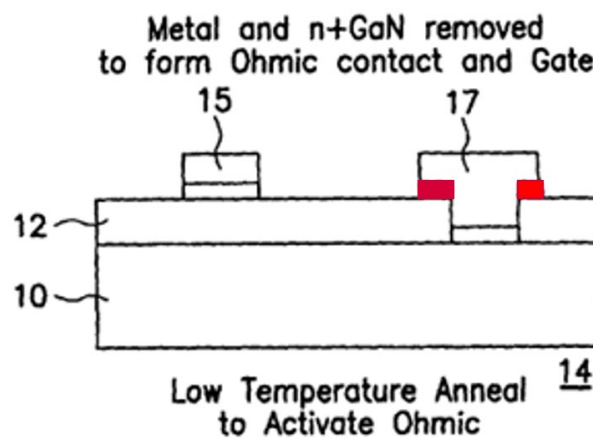


Fig. 1E

EX2001 ¶162

Petitioner also contends that a two-mask ohmic metal formation technique was well known, and that it would also permit formation of a field plate. Pet. 23-24. Petitioner disparages an aligned ohmic structure. *Id.* Not only are Petitioner's motivation to combine arguments contrary to its own prior position concerning gate formation, but in fact, lift-off is a common practice that Dr. Shealy himself utilizes. *See, e.g.*, EX2004 4:7-15; EX2005 7:64-67, 11:27-41. Moreover, Petitioner's motivation to combine argument is clearly based on hindsight to the extent it contends that a two-mask process permits the formation of a field plate (Pet. 24), which Petitioner apparently recognizes is part of the disclosed "present invention" in the '508 patent. Neither *Yoshida*, *Beach*, nor *Sheppard* discloses a field plate in their devices. EX2001 ¶163. Importantly, Petitioner never asserts that a POSA would (rather than could) modify *Yoshida* in view of *Beach* to achieve a process including providing a field plate. *See Personal Web*, 848 F.3d at 993-94.

Thus, a POSA would not have been motivated to replace the single-mask process of *Yoshida* with a more time intensive, costly, non-self-aligned process of *Beach*. EX2001 ¶153.

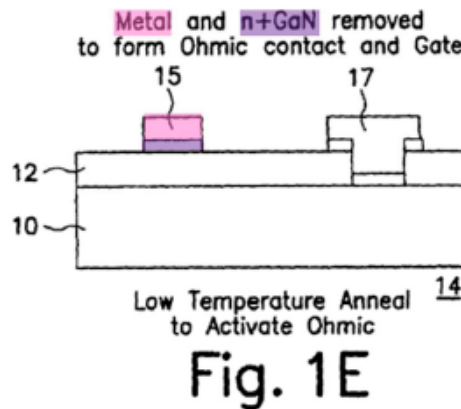
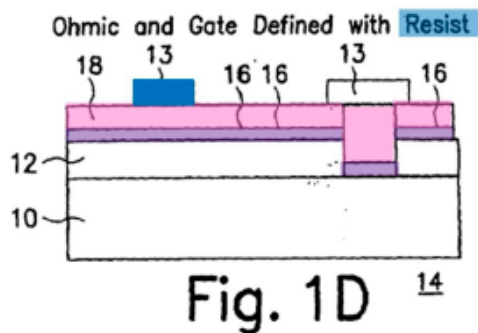
D. Petitioner’s Purported Combination/Modification Fails to Meet the Separate and Distinct “gate photo resistant pattern” and “metal photo resistant pattern” Limitations

Petitioner concedes that *Yoshida* does not disclose “applying a gate photo resistant pattern” [1e2] or “applying a metal photo resistant pattern” [1g2]. See Pet. 30-33, 35-39. Instead, Petitioner relies on *Beach* as disclosing these steps. See *id.* But *Beach* does not disclose or suggest separate steps (as claimed) of applying a gate photo resistant pattern and a metal photo resistant pattern.

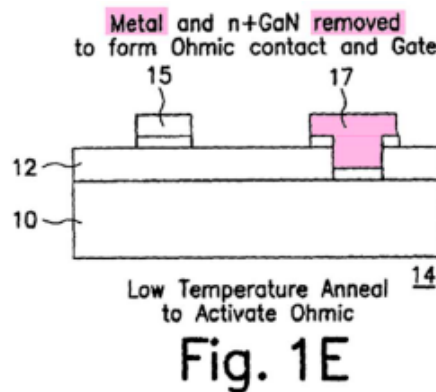
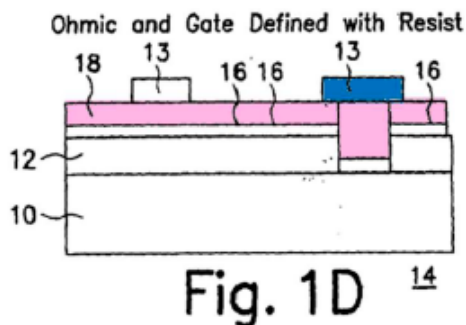
“Where a claim lists elements separately, the clear implication of the claim language is that those elements are distinct components of the patented invention.” *Becton, Dickinson & Co. v. Tyco Healthcare Grp., LP*, 616 F.3d 1249, 1254 (Fed. Cir. 2010). In *Becton*, the Federal Circuit reasoned that where limitations of a hinged arm and spring means connected to the hinged arm were listed as separate elements, prior art in which these structures were not separate would not invalidate the claims. *Id.* at 1254-55. Although claim 1 is a method claim, the logic holds: Petitioner’s proposed reliance on a single process step of the prior art cannot meet two individual steps (e.g., “applying a gate photo resistant pattern” ([1e2]) and “applying a metal photo resistant pattern” ([1g2])), especially here, where the specification makes clear that the steps are separate.

Petitioner provides the following annotated figures which make clear that it is referring to the single photoresist of *Beach* (photoresist 13), the result of a single

photolithography process of *Beach*, as the proposed modification to *Yoshida* as both the “gate photo resistant pattern” and “metal photo resistant pattern”:



Pet. 33

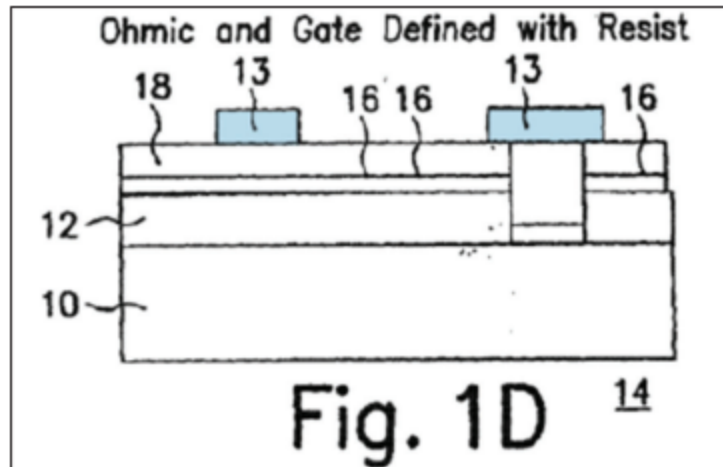


Pet. 37

With respect to claim element [1e], Petitioner admits that *Yoshida* does not disclose using a single mask to etch the p-type GaN layer, and instead relies on *Beach* stating: “*Beach* discloses step [1e2], i.e., applying a gate photo resistant pattern 13.” Pet. 31-32. Similarly, with respect to claim element [1g], the Petition again admits *Yoshida* does not disclose a process for forming the source and drain electrodes, but again relies on *Beach*: “*Beach* discloses that a metal photo resistant

pattern 13 (mask) is applied over the ohmic contact metal 18.” Pet. 35. Again, the Petition simply asserts that a POSA “would have been motivated to apply *Beach*’s masking process to form *Yoshida*’s ohmic source and drain contacts.” Pet. 39; *see also id.* at 23. Notably, the Petition never explicitly sets forth the proposed modifications to *Yoshida* to allegedly achieve the claimed process steps.

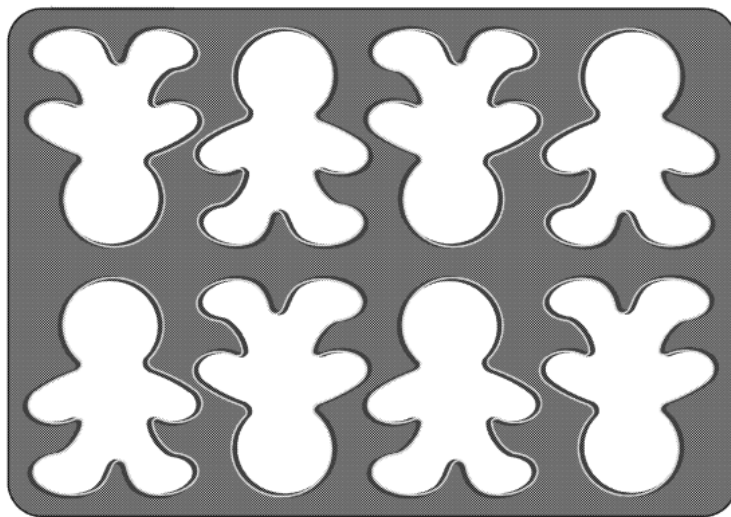
Beach is relied on as describing the two distinctly claimed method steps of “applying a gate photo resistant pattern” ([1e2]) and “applying a metal photo resistant pattern” ([1g2]). However, *Beach* clearly describes a single process step of forming both gate electrode 15 and ohmic electrode 17 in a single step with a single resist pattern 13. EX1005 ¶[0047]; EX2001 ¶152. Notably, although *Beach* describes and depicts resist pattern 13 formed over layer 18, a POSA would have understood that resist pattern 13 is made by applying a single photoresist, exposing the single photoresist with a pattern, and developing the single photoresist to result in resist pattern 13 formed over layer 18, which, when selectively etched, will form the gate contact and the ohmic contact. EX2001 ¶152; *see also* EX2002 18:25-22:5. Hence, resist 13 is applied in one process step in the prior art and the fact that the single prior art step results in two structural elements 13 is immaterial as to whether *Beach* teaches the claimed *process*.



EX1005 FIG. 1D

Petitioner ignores that element 13 of FIG. 1D of *Beach* is deposited in a *single* process step and does not correspond to two discrete *structural* elements or result from two discrete process steps. EX2001 ¶¶166-167. *Beach*'s use of the singular word, "pattern," in conjunction with the described single deposition step, would inform a POSA that one, and only one, pattern is deposited in a single step to permit the *simultaneous* formation of the gate contact 15 and ohmic contact 17. EX1005 ¶[0047]; EX2001 ¶¶166-167. As such, Petitioner cannot claim this single prior art step corresponds to two discrete applying steps and two discrete removing steps. *Beach* describes a process similar to applying a cookie cutter sheet to simultaneously cut out multiple cookies; there is only one step of applying the cookie cutter sheet to the dough, but the result may be many independent cookies. EX2001 ¶167 (showing Exacts a, reproduced below). The fact that there are multiple cookies is immaterial to the relevant process.

FIG. 1



EX2007

Petitioner has not asserted it would be obvious to modify *Beach* to “apply” patterned resist 13 in separate process steps. Indeed, Petitioner itself explains that a POSA would be motivated to eliminate a multi-photoresist pattern sequence in order to simplify the manufacturing process and reduce costs. Pet. 21-22; EX2002 43:15-19. Therefore, Petitioner has failed to explain how any such modification could or would be incorporated into *Yoshida*.

Beach’s “gate-simultaneous” process further cannot teach claim elements [1e2] and [1g2] because under the proper construction of the claims of the ’508 patent, the gate formation process [1e] *must* occur *before* the ohmic formation process [1g]. Therefore, because the claims require applying the gate photoresistant pattern before applying the metal resistant pattern, *Beach*’s simultaneous process cannot disclose both steps. EX2001 ¶169.

A critical deficiency of Petitioner’s proposed combination is that it relies on structures rather than processes. The ’508 patent claims two distinct process steps: “applying a gate resistant pattern” and “applying a metal resistant pattern.” These process steps are claimed as distinct process steps (which must occur at different times in the claimed invention (*see supra* §IV)). *Beach* uses a single resist 13 to pattern both the gate and ohmic electrodes, and likewise, the process by which it is applied – the aspect relevant to the claims – is a single process step. EX2001 ¶¶167-169. Even if one assumes that the single resist 13 of *Beach* can meet both the “gate photo resistant pattern” and “metal photo resistant pattern” limitations (*see, e.g.*, Paper 11 at 27-28), *Beach* only teaches one applying step, not two - both elements of resist 13 are applied in the same location through a single patterning step. *Id.*

For at least the same reasons discussed above, the proposed combination cannot invalidate claims 2 or 3.

VIII. GROUND 2: HIKITA347, SHEPPARD, AND BEACH

Petitioner’s proposed combination of *Hikita347*, *Beach*, and *Sheppard* suffers the same deficiencies as those discussed above with respect to Ground 1 since Petitioner largely relies upon a similar combination as Ground 1. Petitioner essentially replaces *Yoshida* with *Hikita347*. EX2001 ¶171. Thus, Ground 2

cannot render claim 1 or claim 4 unpatentable for at least the same reason as Ground 1.

A. Petitioner Never Provides a Description of Incorporating Beach into Hikita347

As in Ground 1, Petitioner fails to particularly describe its proposed combination sufficient to permit any analysis as to how the “jigsaw puzzle” is assembled. *See* §VII.A. Generally, Petitioner proposes the same modifications to *Hikita347* as it proposed to *Yoshida* with respect to gate formation and ohmic contact formation and identified the same motivations to combine.

Similar to *Yoshida*, *Hikita347* describes a “gate-last” process where the gate contact is formed after the ohmic electrode. EX1007 ¶¶60-61, FIGS. 8E-8F; EX2001 ¶171. Thus, for the same reasons discussed above with respect to Ground 1, Petitioner fails to meet its burden to clearly define the allegedly invalidating process or how the combined process produces an operable GaN device. *See supra* Section §§VII.A-B; EX2001 ¶156.

B. A POSA would Not be Motivated to Replace *Hikita347*’s Gate-Last Process with *Beach*’s Gate-Simultaneous Process

Similar to *Yoshida* in Ground 1, *Hikita347* describes a “gate-last” process. *Compare* EX1004 ¶¶[0022]-[0023] with EX1007 ¶¶[0060]-[0061]. As such, for the same reason discussed *supra* §§VII.A-B, a POSA would not have been motivated to replace *Hikita347*’s “gate-last” process with *Beach*’s “gate-

simultaneous” process and therefore would not have modified *Hikita347* in view of *Beach*. EX2001 ¶174.

In addition, with respect to *Hikita347*, Petitioner misconstrues *Hikita347*'s teaching of its electrodes being formed before the SiN layer, which Petitioner relies on to imply a different order of electrode deposition. EX2001 ¶175. But, *Hikita347* only states the gate, source, and drain electrodes can be deposited before the SiN layer; it does not disclose or even suggest that the deposition of the gate electrode can occur before the deposition of the source/drain electrodes. *Id.*; EX1007 ¶[0061] (“The source electrode 409, the drain electrode 410 and the gate electrode 411 may be formed before formation of the SiN film 408”). As discussed *supra* §§VII.A-B (*see also* §§VI.A-B), Petitioner provides no explanation of how *Beach*'s “gate-simultaneous” process would integrate into *Hikita347* or how a POSA would modify *Hikita347* in view of *Beach*. EX2001 ¶176. For example, the claims specifically require “etching the dielectric layer to open the drain and source contact areas” (steps [1f3], [4g3]), but under Petitioner's potential proposed combination and citation to *Hikita347*, there would be no dielectric to etch prior to deposition of the electrodes. *Id.*

It simply makes no sense to combine a “gate-last” process with a “gate-simultaneous” process. *Id.*

C. There is No Motivation to Replace *Hikita347*'s One Mask Ohmic Formation with a Two-Mask Process

Similar to Ground 1, Petitioner proposes modifying *Hikita347*'s ohmic formation process with *Sheppard* and *Beach*. Pet. 49-51, 56-61. As best understood, Petitioner proposes applying the masking process of *Sheppard* (steps [1f], [4g]) to open source and drain areas in the SiN of *Hikita347* and then applying *Beach*'s ohmic masking process (steps [1g], [4h]) to obtain the presently claimed two-mask ohmic contact process. Pet. 49-51, 58-61. Petitioner's proposed combination is premised on impermissible hindsight, which seeks to modify a one-mask process into a more complicated, time consuming, and costly two-mask process using disparate references that teach drastically different ohmic formation processes. EX2001 ¶177.

Petitioner asserts that a POSA would further modify the ohmic deposition process of modified *Hikita347* and *Sheppard* with *Beach*'s ohmic masking and etching process. Pet. 51. This would result in a first mask used to open SiN film and a second mask used to pattern and etch ohmic metal. EX2001 ¶178. In short, Petitioner proposes replacing the entire fabrication process of opening electrode areas and depositing metal of *Hikita347* by combining two disparate processes, a "gate-simultaneous" process and a "gate-last" process. *Id.* Such a significant modification, using two different prior art references, to 1) substitute a disclosed opening of a silicon oxide for *Sheppard*, 2) substitute a known lift-off process for a

second photo mask process of *Beach*, and 3) switching from a more efficient and quicker one mask process of *Hikita347* to a two-mask process, evidences the application of impermissible hindsight. *Id.*

Petitioner's proposed combination is a further modification (with *Beach*) of an already modified process (*Hikita347* and *Sheppard*). *See id.* at ¶¶177-78.

Petitioner's sole justification to combine *Hikita347* and *Beach* for source and drain masking is based on Petitioner's argument that a POSA would be motivated to combine *Yoshida* and *Beach*. Pet. 51, 60-61. Petitioner simply alleges that *Hikita347*, like *Yoshida*, teaches ohmic metal, and thus, a POSA would have been motivated to combine *Beach* with *Hikita347* for the same reason as combining *Beach* with *Yoshida*. *Id.* However, Petitioner provides no explanation beyond *Hikita347* teaching ohmic metal to justify applying the same motivation. In short, Petitioner fails to address the differences in *Hikita347* and *Yoshida* and therefore does not meet its burden to establish a particular motivation to combine *Hikita347* and *Beach*. Because Petitioner fails to address the motivation to combine modified *Hikita347* and *Sheppard* with *Beach*'s ohmic masking process, the combination is fatally flawed and cannot disclose or suggest steps [1g], [4h].

Finally, for the same reasons explained in §§VII.A-B, Petitioner's double modification of *Hikita347*'s ohmic formation process results from nothing more than impermissible hindsight. It would not have been obvious for a POSA to

modify *Hikita347* in view of *Sheppard* and *Beach* as proposed by Petitioner. The proposed combination goes against a POSA's motivation to achieve a cheaper more efficient process and is solely based on hindsight. The hindsight reasoning is evidenced by Petitioner's reliance upon the '508 patent's own teaching of forming a field plate together with the source contact as its motivation for a two-mask process. Pet. 24, 51. Therefore, Petitioner cannot establish claims 1 or 4 are unpatentable.

D. It Would Not have Been Obvious to Combine *Hikita347*'s Enhancement Mode Device with *Beach*'s Depletion Mode Device

There is no dispute that *Hikita347* describes "normally OFF" enhancement mode transistors. EX1007 ¶¶7-8, 11, 14, 38; EX2001 ¶180. There appears to be no dispute that *Beach* describes depletion mode devices, as Dr. Shealy acknowledges protective layer 16 is n-type (n+)⁶ and not p-type GaN (EX2002

⁶ *Beach*'s protective layer is identified solely for preventing the outdiffusion of nitrogen from the underlying layers and "can be thought of as an encapsulant for surface protection and passivation of the resulting device." EX1005 ¶[0055]. A POSA would recognize this protection layer does not contain acceptor type dopants and does not deplete the 2DEG and therefore cannot render the device of *Beach* enhancement mode. EX2001 ¶182.

63:10-24), which a POSA would recognize does not deplete the 2DEG and would result in a depletion mode device. EX2001 ¶¶146, 182.

Enhancement mode devices such as *Hikita347* have significant incompatibilities with depletion mode devices such as *Beach*; most notably, the devices have different structures and, therefore, different epitaxial growth and fabrication processes. Compare EX1007 FIGS. 8A-8E with EX1005 FIGS. 1A-1E; EX2001 ¶183. Hence a POSA would not have been motivated to combine the fabrication teachings of *Hikita347* with the fabrication teachings of *Beach* to obtain an operable enhancement mode device, as required by *Hikita347*. EX2001 ¶183.

E. *Hikita347*'s Fabrication Process is Incompatible with *Beach*'s Simultaneous Gate and Ohmic Contact Formation Process

Hikita347's gate contact and source and drain contacts are formed of different materials and are therefore incompatible with *Beach*'s "gate-simultaneous" process, which would prevent a POSA from seeking to combine the references. EX2001 ¶184.

Hikita347 gate contact can be nickel (Ni) or palladium (Pd) and its ohmic contacts are a titanium layer and an aluminum layer. EX1007 ¶¶[0034], [0040], [0060]-[0061]; EX2001 ¶184. *Beach* requires the same electrode metal for both its gate contact and its ohmic contact, as it forms the gate and ohmic contacts simultaneously from one metal layer. EX2001 at ¶185. Therefore, due to the dissimilarity of metals, a POSA would not have combined *Hikita347* and *Beach*

with any expectation of success in connection with the formation of the electrodes.
Id. at ¶185.

Accordingly, Petitioner cannot establish that the cited prior art renders obvious at least claim elements [1e2], [1g2], [4f2] or [4h2].

F. Ground 2 Fails to Teach a “Gate-First” Process

Hikita347 in view of *Sheppard* and *Beach* fail to disclose or suggest a “gate-first” process as required under the proper construction of Claim 1. *See supra* §IV. *Hikita347* and *Sheppard* both describe “gate-last” processes. EX2001 ¶¶186-188; EX2002 69:3-70:18, 71:22-72:12; EX1007 ¶¶[0060]-[0061]; EX1006 8:55-63, 4:58-5:2, 10:46-50. *Beach* describes a “gate-simultaneous” process. EX2001 ¶186 EX1005 ¶[0047].

Although Petitioner proposes modifying *Hikita347* with *Beach* and *Sheppard*, none of the references disclose or suggest a process to form an enhancement mode GaN device that patterns and etches a self-aligned gate structure *before* forming ohmic contacts. EX2001 ¶187. Indeed, Petitioner never proposes modifying *Hikita347*’s “gate-last” process to become a “gate-first” process or identifies any motivation to do so. In fact, Dr. Shealy testified to the negative aspects of a “gate-first” process, further demonstrating it would not have been obvious to a POSA to modify *Hikita347* in such a manner because “there are good reasons not to necessarily choose that path.” EX2002 85:19-86:8, 95:11-23;

see also EX2001 ¶187 (describing known detriments to gate contact from being exposed to ohmic contact anneal).

Alone or in combination, *Hikita*347 in view of *Sheppard* and *Beach* cannot render obvious a “gate-first” gate formation process as required by claims 1 and 4 of the ’508 patent.

G. Ground 2 Does not Teach Separate Steps of “applying a gate photo resistant pattern” and “applying a metal photo resistant pattern”

Petitioner concedes that *Hikita*347 does not disclose the claimed “applying a gate photo resistant pattern” ([1e2] [4f2]) or “applying a metal photo resistant pattern” ([1g2], [4h2]). *See* Pet. 56-58, 60-61. Instead, Petitioner alleges that *Beach* teaches these steps, and therefore the combination renders obvious the claimed steps. *See id.* For the same reasons discussed above regarding Ground 1, Petitioner is wrong.

As in Ground 1, Petitioner identifies the same photo resist pattern 13 of *Beach* for both the applying a “gate photo resistant pattern” and “metal photo resistant pattern” in the proposed combination. Pet. 61; *supra* VII.A. As in Ground 1, Petitioner conflates the structural element 13 of *Beach* with the distinct claimed process steps. EX2001 ¶190; *supra* VII.A.1.

The claimed step of “applying a gate photo resistant pattern” is used to form a gate structure using a single mask. EX1001 3:45-50, 4:41-44, claims 1, 4;

EX2001 ¶191. Separately, the claimed step of “applying a metal photo resistant pattern” is used to pattern and etch the claimed ohmic contacts, which occurs temporally after completion of forming the gate structure and the step of “applying a gate photo resistant pattern.” EX1001 3:64-67, 4:49-52, claims 1, 4; EX2001 ¶191.

As explained above (*supra* §VI.B), *Beach* describes a single photolithography process and application of a single patterned photoresist that is illustrated as two separate structural elements formed by a single process; as such, contrary to Petitioner’s argument, *Beach* does not teach “applying a gate photo resistant pattern” ([1e2], [4f2]) and “applying a metal photo resistant pattern” ([1g2], [4h2]). EX2001 ¶192.

Petitioner’s proposed secondary references and reasons to combine are the same as Ground 1. Similar to *Yoshida*, *Hikita347* describes a “gate-last” process. *Id.* at ¶192. In addition, *Hikita347* has generally the same process and resulting structure as *Yoshida*. *Id.* Therefore, the reasons that *Yoshida* in view of *Beach* fail to disclose or suggest steps [1e2] and [1g2] applies equally to Ground 2 and the proposed combination of *Hikita347* and *Beach*. *Id.*; *supra* §VII.D. Accordingly, *Hikita347* and *Beach* cannot render obvious the separately claimed steps of “applying a gate photo resistant pattern” [1e2], [4f2] and “applying a metal photo

resistant pattern” [1g2], [4h2] for the reasons discussed above. EX2001 ¶193; *supra* §VII.D.

IX. GROUND 3: HIKITA023, SHEPPARD, AND BEACH

Hikita023 is a reference filed a year after *Hakita347* and lists the same inventors. Compare Exhibit 1007 with Exhibit 1008. The two *Hikita* references describe similar “normally OFF” “gate-last” transistors and methods of manufacture. EX1008 ¶¶[0014], [0037], [0072]-[0073], [0109]; EX1007 ¶¶[0007]-[0008], [0011], [0014], [0038]; EX2001 ¶194. The only material difference between the references relates to the etching process associated with the p-type AlGaN layer of *Hikita023*, which is not relevant to the issues in this case.

A. A POSA Would Not be Motivated to Replace *Hikita023*’s “Gate-Last” Process with *Beach*’s “Gate-Simultaneous” Process

Petitioner proposes modifying *Hikita023*’s gate-last process with *Beach*’s gate-simultaneous process. Pet. 77-78, 84-86. Petitioner relies on the arguments presented in its Ground 1 to support its position that it would have been obvious to modify *Hikita023*’s “gate-last” process with *Beach*’s “gate-simultaneous” process, even though Ground 1 relates to *Yoshida*, which does not disclose the same device or fabrication process as *Hikita023*. Pet. 77-78, 84-86; EX2001 ¶196.

However, *Hikita023* is a “gate-last” process (*see supra* §§VII.A-B, VIII.A-B; EX2001 ¶197) just like *Yoshida* and *Hikita347*. For at least the reasons discussed above with respect to Grounds 1 and 2 (§§VII.A-B, VIII.A-B), a POSA

would not have been motivated to replace *Hikita023*'s gate-last process with *Beach*'s "gate-simultaneous" process, including for the reasons discussed *infra* §IX.D to achieve the claimed "gate-first" single-photo mask process, with any expectation of success. EX2001 ¶197.

B. No Motivation to Replace *Hikita023*'s Single-Mask Ohmic Formation with a Two-Photo Mask Formation

As discussed above with respect to Grounds 1 and 2, Petitioner fails to establish a motivation to replace *Yoshida*'s or *Hikita347*'s "gate-last" single-mask ohmic formation process, which includes a lift-off step, with a more complicated, less accurate, non-self-aligned two-photo mask process. *See supra* §§VII.C, VIII.C. Petitioner relies on the same motivation to combine arguments presented in Grounds 1 and 2 for Ground 3. Pet. 78 (citing *Hikita347* and *Sheppard* for SiN masking process and *Yoshida* and *Beach* for ohmic masking process).

Hikita023 includes a single-mask process to pattern the ohmic contacts like *Yoshida* and *Hikita347* (EX1008 ¶¶[0078], [0079] (lift-off process to form source and drain contacts; EX1007 ¶[0060]; EX2001 ¶¶104-105, 157, 199 (explaining *Hikita347* practices lift-off); EX1004 ¶¶[0022]-[0023]; EX2001 ¶¶123, 177-178, 199 (explaining *Yoshida* practices lift-off)). For the same reasons explained above in §§VII.C and VIII.C, Petitioner fails to establish a motivation to replace *Hikita023*'s single-mask ohmic formation process with *Sheppard*'s and *Beach*'s combined two-mask process. *See supra* §§VII.C, VIII.C. Accordingly, for the

same reasons explained above, a POSA would not have sought to replace the single-mask process of *Hikita023* with *Sheppard* and *Beach*, and it would not have been obvious to arrive at claim elements [5h] and [5j].

C. It Would Not have Been Obvious to Combine *Hikita023*'s Enhancement Mode Device with *Beach*'s Depletion Mode Device

There is no dispute that *Hikita023*, like *Hikita347*, is an enhancement mode, or normally OFF transistor. EX1008 ¶¶[0014], [0037], [0072]-[0073], [0109]; EX2001 ¶200; *supra* §VIII.D. Further, as explained above, *Beach* is a depletion mode device. *See supra* §VIII.D.

Therefore, for at least the same reasons explained with respect to claim elements [1e], [1g], [4f], and [4h] explained above, it would not have been obvious to a POSA to combine *Hikita023*'s enhancement mode device with *Beach*'s depletion mode device, especially given that a gate fabrication process could materially affect the functionality and operability of an enhancement mode device. *See supra* §VIII.D; EX2001 ¶201.

D. *Hikita023*'s Fabrication Process is Incompatible with *Beach*'s "Gate-Simultaneous" Process

As with *Hikita347*, discussed above respectively in §VIII.E, *Hikita023*'s gate and ohmic contacts are formed of different materials; and are therefore incompatible with *Beach*'s simultaneous gate and ohmic contact process. EX2001 ¶202.

Hikita023, like *Hikita347*, has a palladium gate contact and ohmic contacts made of a titanium layer and an aluminum layer. EX1008 ¶¶[0056], [0080], [0087], [0054]; EX2001 ¶202; *see also* EX1007 ¶¶[0034], [0040], [0060]-[0061]. As such, similar to *Hikita347*, *Hikita023* does not identify materials that can be used to simultaneously form all contacts. EX2001 ¶202.

Therefore, for the reasons explained above in §VIII.E; *Hikita023* is similarly incompatible with *Beach* as *Hikita347*. Therefore, a POSA would not have modified *Hikita023*'s ohmic formation process in view of *Beach* for at least the same reasons discussed above with any expectation of success. *See supra* §VIII.E; EX2001 ¶203. For this additional reason, a POSA would not have been motivated to combined *Hikita023*'s and *Beach*'s incompatible processes with any expectation of success to form operable gate and ohmic contacts; and hence, Petitioner cannot establish that *Hikita023* in view of *Beach* renders obvious steps [5f2] or [5i2]. EX2001 ¶203.

E. Ground 3 Fails to Teach a “Gate-First” Process

Hikita023 in view of *Sheppard* and *Beach* fail to disclose or suggest a “gate-first” process as required under the proper construction of Claim 5. *See supra* §IV. *Hikita023* describes a “gate-last” process. EX2001 ¶204; EX2002 80:3-8; EX1008 ¶¶[0079]-[0080]. *Beach* describes a “gate-simultaneous” process. EX2001 ¶204; EX1005 ¶[0047].

Although Petitioner proposes modifying *Hikita023* with *Beach* and *Sheppard*, none of the references discloses or suggests a process to form an enhancement mode GaN device that patterns and etches a self-aligned gate structure *before* forming ohmic contacts. EX2001 ¶204. Indeed, Petitioner never proposes modifying *Hikita023*'s "gate-last" process to become a "gate-first" process or identifies any motivation to do so. In fact, Dr. Shealy testified to the negative aspects of a "gate-first" process, further demonstrating it would not have been obvious to a POSA to modify *Hikita023* in such a manner. EX2001 ¶205; EX2002 85:19-86:8, 95:11-23 ("So there are good reasons not to necessarily choose that path."). Further, for the same reasons it would not have been obvious to modify *Hikita347* in view of *Beach* to obtain a "gate-first" process, the same is true here. Therefore, *Hikita023* in view of *Beach* and *Sheppard* cannot render obvious element ([5f]) as properly construed to occur before element ([5i]).

F. Ground 3 Does not Teach Separate Steps of Applying a "gate photo resistant pattern" and "fourth photo resistant pattern"

As explained above in §VIII.G, *Hikita347* in view of *Beach* and *Sheppard* does not teach separate steps of "applying a gate photo resistant pattern" (step

[5f2]) and “applying a fourth photo resistant pattern” (step [5i2]).⁷ Petitioner proposes the same secondary reference combinations and alleged motivations to combine as presented in Ground 2 with respect to these limitations. Pet. 77-78. But the differences between *Hikita023* and *Hikita347* with respect to these limitations are inconsequential. EX2001 ¶207.

Beach teaches a “gate-simultaneous” process including the single step of applying photoresist 13, which Petitioner contends corresponds to both [5f2] and [5i2]. Pet. 84-86, 89-90; EX2001 ¶¶207-208. *Hikita023*, like *Hikita347*, discloses different materials for the gate contact (Pd) and ohmic electrodes (Ti layer and Al layer) just like *Hikita347*. EX1008 ¶¶[0054], [0056]; EX2001 ¶208. Furthermore, *Hikita023* describes a “gate-last” process, just like *Hikita347*. EX1008 ¶¶[0079]-[0080], FIGS. 6D, 6E; EX2001 ¶208.

Therefore, for at least the same reasons explained above with respect to VIII.A, *Hikita023* in view of *Beach* fails to disclose or suggest both of steps [5f2]

⁷ Although claim 5 states “applying a fourth photo resistant pattern” and claim 4 states “applying a metal photo resistant pattern,” both claims are describing the same process steps for patterning and etching ohmic contacts. EX2001 ¶207. Therefore, although different language is used, both limitations require the same step.

and [5i2], at least because *Beach* only describes a single process step resulting in both its gate and ohmic resist 13. Further, similar to Ground 2, Petitioner fails to articulate its proposed modified process and therefore fails to establish that these two distinct claim elements occurring at different stages of the claimed process are obvious over the single prior art step.

X. CONCLUSION

For the foregoing reasons, Petitioner's challenge is deficient and claims 1-5 should be found not unpatentable.

Dated: June 12, 2024

Respectfully submitted,

/s/ Walter D. Davis, Jr.

Walter D. Davis, Jr. (Reg. No. 45,137)

walter.davis@blankrome.com

Blank Rome LLP

1825 Eye St NW

Washington, DC 20006

Tel: 202-420-2200

Fax: 202-420-2201

Counsel for Patent Owner

CERTIFICATE OF WORD COUNT

The undersigned certifies that the foregoing PATENT OWNER's RESPONSE complies with the type-volume limitation in 37 C.F.R. § 42.24(b)(1). According to the word count tool in Microsoft Word, the brief contains 11,821 words, excluding the parts of the document that are exempted by 37 C.F.R. § 42.24(a).

Dated: June 12, 2024

Respectfully submitted,

/s/ Walter D. Davis, Jr.

Walter D. Davis, Jr. (Reg. No. 45,137)

Counsel for Patent Owner

CERTIFICATE OF SERVICE

The undersigned certifies that a true and correct copy of the foregoing **PATENT OWNER'S RESPONSE** is being served on counsel of record by filing this document through the Patent Review Processing System, with a copy served via electronic mail to the following email address, as authorized in the Petition:

Innoscence-EPC-IPRs@finnegan.com

Dated: June 12, 2024

Respectfully submitted,

/s/ Walter D. Davis, Jr.

Walter D. Davis, Jr. (Reg. No. 45,137)

Counsel for Patent Owner