

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INNOSCIENCE (ZHUHAI) TECHNOLOGY COMPANY AND
INNOSCIENCE AMERICA, INC.,
Petitioner,

v.

EFFICIENT POWER CONVERSION CORPORATION,
Patent Owner.

Case IPR2023-01383
Patent No. 8,404,508

PETITIONER'S REPLY TO PATENT OWNER'S RESPONSE

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I. Introduction

EPC cannot save its claims. In its Patent Owner's Response (Paper 17, "POR"), EPC advances an intrinsically unsupported construction, misinterprets the prior art, and misapplies Petitioner's combination.

II. Claim Construction

The claims **do not** require a "gate-first" process. POR 17-25. The Board properly rejected EPC's "gate-first" construction. Paper 11, 11-15.

A. Neither the Claim Language Nor the Specification Requires the Gate Structure to Be Formed First

The '508 patent claims do not recite an order for the gate structure steps ([1e1]-[1e5], [4f1]-[4f5], [5f1]-[5f5]) compared to the ohmic contact steps ([1g1]-[1g5], [4h1]-[4h5], [5i1]-[5i5]). These steps are separate and have no overlapping elements.

The specification specifies no sequence of forming the gate and ohmic contacts, nor any disclaimer. To the contrary, it repeatedly states that the invention is not limited to the described embodiments. Ex. 1001, 6:52-56 ("the embodiments of the invention are not considered being limited by the foregoing description and drawings," and "[m]odifications and substitutions to specific process conditions can be made"); 2:65-67 ("other embodiments may be employed and that various structural, logical, and electrical changes may be made."). Absent limiting

language, claims cannot be limited. *Hill-Rom Servs., Inc. v. Stryker Corp.*, 755 F.3d 1367, 1372-73 (Fed. Cir. 2014).

B. The Claims Do Not Require a Field Plate

EPC's only argument for "gate first" is the specification's description of a field plate in one embodiment, which EPC argues must be formed simultaneously with the source contact. POR 18-22. EPC's argument fails. First, the claims, specification, and prosecution history do not require a field plate. Second, forming a field plate does not require the gate structure to be formed first.

First, the claims do not recite a field plate, making them broader than the single field plate embodiment.

The field plate is a single embodiment, not the "invention." And it is an optional feature. Ex. 1001, Abstract ("The enhancement mode GaN transistor *may* also have a field plate made of Ohmic metal") (emphasis added). *Vehicle IP, LLC v. AT&T Mobility, LLC*, 594 Fed. Appx. 636, 643 (Fed. Cir. 2014) (Permissive language such as "may be" indicates that a certain feature is broader than the context in which it is described.). In contrast, the abstract describes a self-aligned gate as a required feature. Ex. 1001, Abstract ("the gate III-V compound and the gate metal *are* formed with a single photo mask process to be self-aligned") (emphasis added).

EPC argues the description of field plate in the paragraph where the “present invention” is described limits the invention. It does not. There, the “present invention” does not refer to a field plate. Ex. 1001, 3:1-4 (“The present invention is an enhancement mode GaN HEMT device with a gate metal material and a doped GaN or AlGaN material that are self-aligned ...”). Instead, the mention of field plate is optional. *Absolute Software, Inc. v. Stealth Signal, Inc.*, 659 F.3d 1121, 1137-38 (Fed. Cir. 2011) (not reading feature into claim where the patent refers to it as optional); *Hill-Rom Servs.*, 755 F.3d at 1372 (embodiments cannot limit the scope of the claims absent the patentee’s “words or expressions of manifest exclusion or restriction.”).

The prosecution history confirms a field plate is optional. The original claims included independent claims 1 and 23—identical except for a field plate.¹ Original claim 1 recited an enhancement-mode GaN transistor with various components **but not a field plate**, while claim 23 **adds the field plate**, demonstrating it is optional. *Compare* Ex. 1002, 19 (claim 1), *with id.*, 26 (claim 23). If the patent required a field plate, as EPC contends, it would be in the claim. *SRI Int’l v. Matsushita Elec. Corp.*, 775 F.2d 1107, 1122 (Fed. Cir. 1985)

¹ Original claims 1 and 23 were later cancelled by Applicant in response to a restriction requirement from the Patent Office.

(“It is settled law that when a patent claim does not contain a certain limitation and another claim does, that limitation cannot be read into the former claim in determining either validity or infringement.”).

Second, forming a field plate does not require the gate structure to be formed before the ohmic source and drain contacts, as Dr. Shealy explains. ShealySupp, ¶26. The gate structure can still be formed after the ohmic contacts. *Hikita-895*, [0056]-[0057] (gate is formed after the ohmic contacts, and field plate is formed thereafter); *Saito*, 2, Fig. 1 (same); *Kumar*, 1, Fig. 1 (ohmic contacts are formed first).

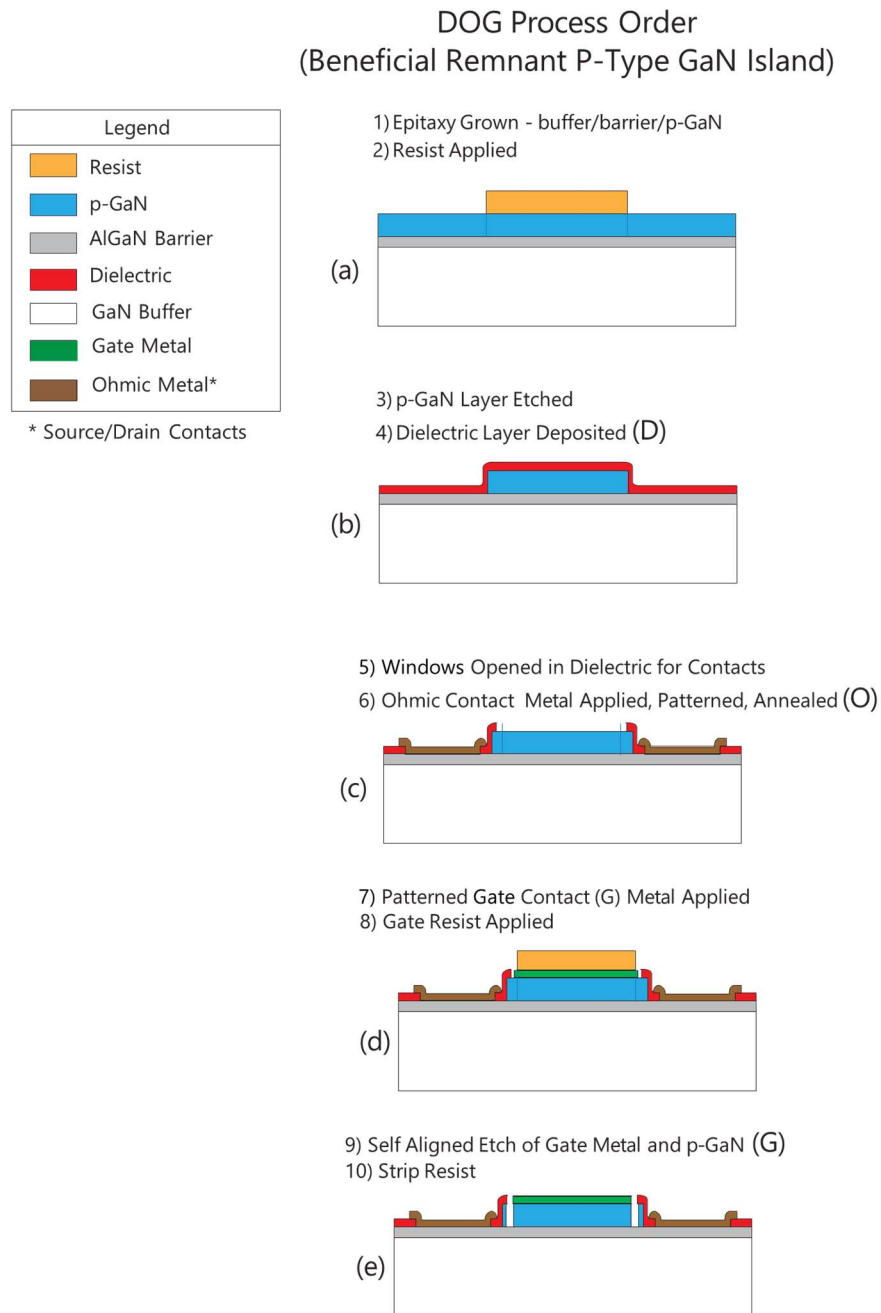
C. The Claims Cover Non-Gate-First Processes

Dr. Schubert argues that the non-gate-first processes would be non-functional. Dr. Schubert’s arguments lack support and merits. Dr. Schubert does not have any practical experience with a GaN transistor. Dr. Schubert’s experience with GaN semiconductor devices is limited to light-emitting diode (LED) devices, not with any GaN transistor of the type in the patent. The Board should give little weight to Dr. Schubert’s testimony.

Dr. Shealy provides two examples of non-gate-first processes covered by the claims.

1. First Example: “D (dielectric), O (ohmic contact), G (gate)” process

As Dr. Shealy explains, the claims cover a “D (dielectric), O (ohmic contact), G (gate)” process shown below.



ShealySupp (Ex. 1041), ¶28; Ex. 1040, 2.

Dr. Schubert wrongly argues that the remnant islands of the p-type semiconductor would render the device nonfunctional. The remnant p-type island has no detrimental effect on performance. ShealySupp, ¶33. To the contrary, the remnant p-type island could improve performance. *Id.* The remnant p-type GaN island over the channel between the gate and drain can partially deplete some of the channel charge, which reduces the longitudinal electric field strength and in turn increases the device's breakdown voltage. *Id.*; *Harvard*, 1-2, 4. The remnant p-type GaN island over the channel between the source and gate can lower the channel charge in this region, which is known to reduce the non-linear component of the device's source resistance, important for high frequency operation. ShealySupp, ¶33.

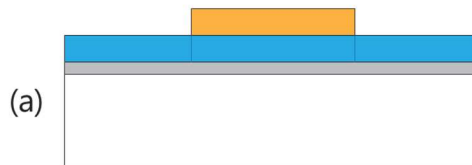
Dr. Schubert overstates remnant island dimension in the D-O-G process. ShealySupp, ¶34. The dimension of the remnant p-type GaN island is determined by the photoresist applied to etch the dielectric layer in Figure (c) of the D-O-G process diagram above, which determines the alignment of dielectric layer to the p-type GaN's edge. *Id.* A POSITA would have understood that, if desired, no remnant p-type GaN island could be left by applying photoresist, as shown below.

DOG Process Order (No Remnant P-Type GaN Island)

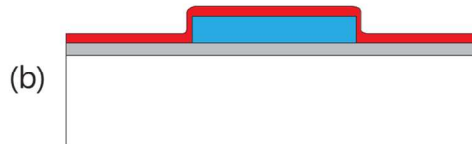
Legend	
	Resist
	p-GaN
	AlGaN Barrier
	Dielectric
	GaN Buffer
	Gate Metal
	Ohmic Metal*

* Source/Drain Contacts

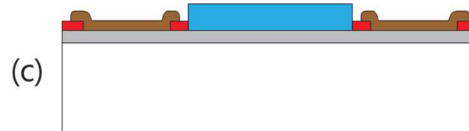
- 1) Epitaxy Grown - buffer/barrier/p-GaN
- 2) Resist Applied



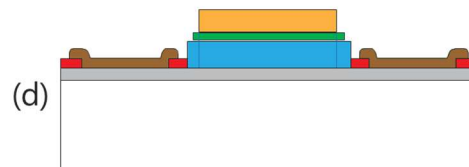
- 3) p-GaN Layer Etched
- 4) Dielectric Layer Deposited (D)



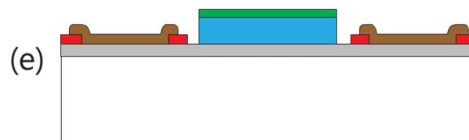
- 5) Windows Opened in Dielectric for Contacts
- 6) Ohmic Contact Metal Applied, Patterned, Annealed (O)



- 7) Patterned Gate Contact (G) Metal Applied
- 8) Gate Resist Applied



- 9) Self Aligned Etch of Gate Metal and p-GaN (G)
- 10) Strip Resist



ShealySupp, ¶34.

Dr. Shealy's group at Cornell used a D-O-G process to form GaN transistors long before the '508 patent. ShealySupp, ¶30; *Thompson*, 1 (describing a D-O-G process for GaN transistor device fabrication). The D-O-G process was commonly used to form GaN transistors that worked for the intended purpose. ShealySupp, ¶30. The D-O-G process also provides the advantage of protecting the gate region from contamination during subsequent processing steps. *Id.*; Ex. 2002, 86:15-20.

A POSITA would have understood that the above D (dielectric), O (ohmic contact), G (gate) process produces an operational GaN transistor. ShealySupp, ¶30.

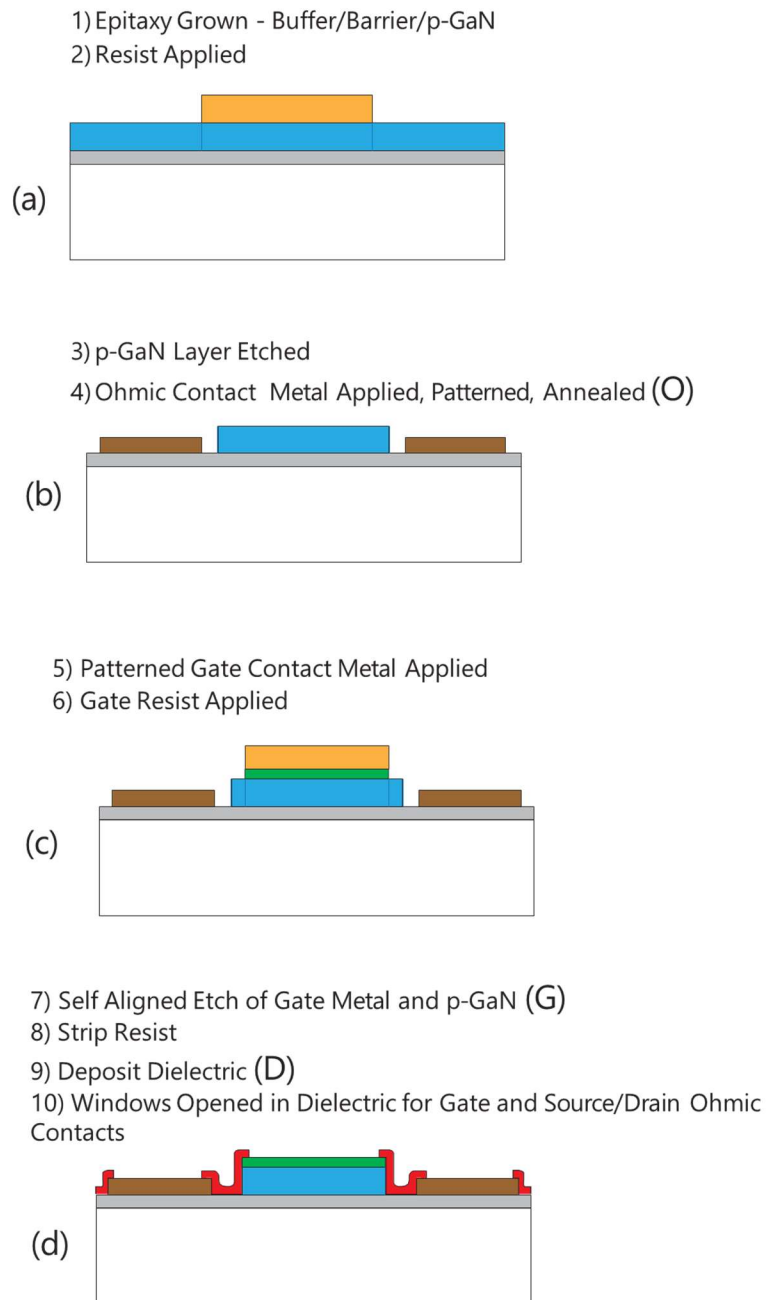
2. Second Example: “O (ohmic contact), G (gate), D (dielectric)” process

Dr. Shealy explains that the claims also cover an “O (ohmic contact), G (gate), D (dielectric)” process shown below.

OGD Process Order

Legend	
	Resist
	p-type GaN
	AlGaN Barrier
	Dielectric
	GaN Buffer
	Gate Metal
	Ohmic Metal*

* Source/Drain Contacts



ShealySupp, ¶35; Ex. 1040, 4.

Dr. Schubert wrongly argues the gate etching would remove the ohmic contacts entirely. Dr. Shealy explains the gate metal and source and drain contacts

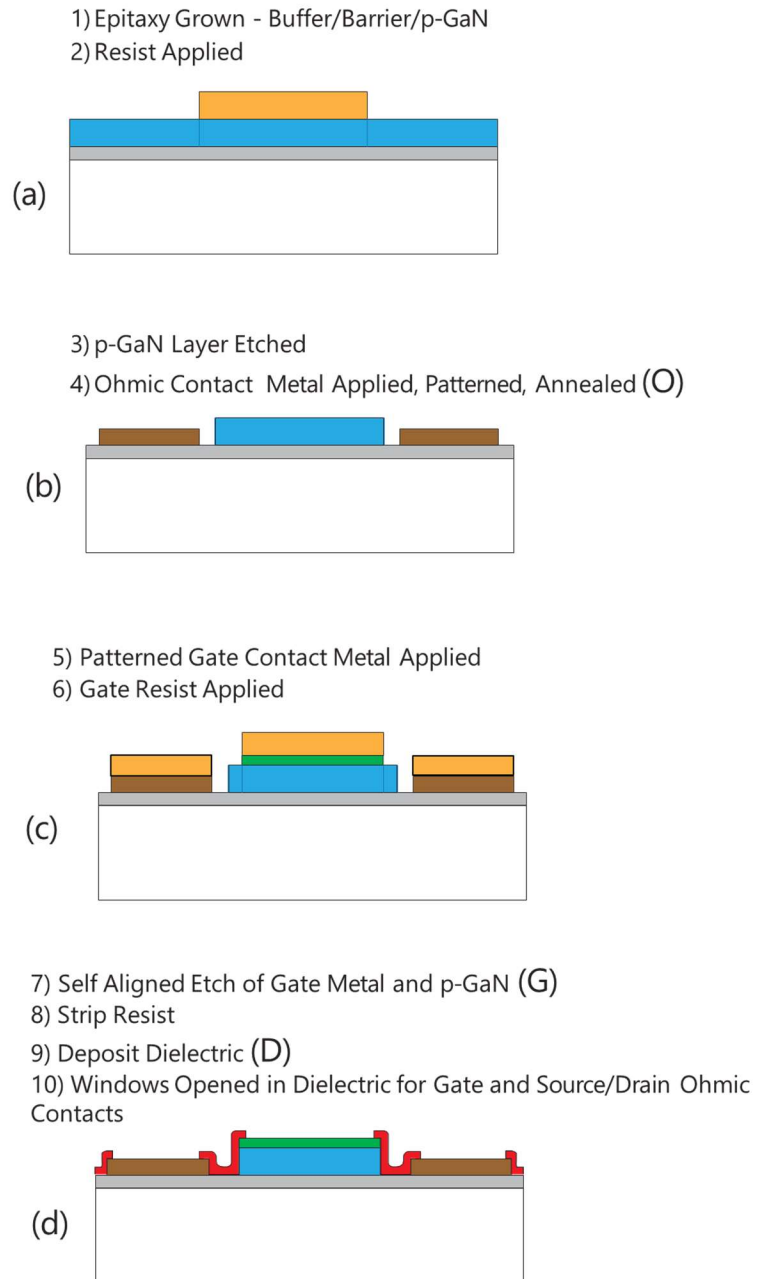
are typically made of different metal materials, and with proper selection of the etching chemical, the etching of gate metal would have no effect on the source and drain ohmic contacts. ShealySupp, ¶39; *Hikita-347*, [0060]-[0061] (describing a gate electrode formed of Pd, and source and drain contacts formed of a Ti layer and an Al layer); *Hikita-023*, [0054], [0056] (same); *Yoshida*, [0022], [0023] (using metal Al for source and drain electrodes and Au for gate electrode); *Harvard*, 1 (using different etching chemistries for forming ohmic contacts and gate contacts); *Walker* (different etching chemistry for different metals).

Dr. Shealy explains that applying a photoresist layer on the ohmic contacts during the gate etching provides a solution to protect the ohmic contacts, shown below in Figure (c).

OGD Process Order
(Photoresist Applied on Ohmic Contacts)

Legend	
	Resist
	p-type GaN
	AlGaN Barrier
	Dielectric
	GaN Buffer
	Gate Metal
	Ohmic Metal*

* Source/Drain Contacts



ShealySupp, ¶40.

Dr. Schubert wrongly argues that gate etching would partially remove the barrier layer. ShealySupp, ¶39. The barrier layer is not composed of metal, and the

chemistry used to etch the gate metal would have no effect on the barrier layer. *Id.*; *Hikita-347*, [0033] (teaching undoped AlGa_N barrier layer); *Yoshida*, [0014] (teaching n-type AlGa_N barrier layer). Regardless, partial removal of the barrier layer would not make the device nonfunctional, and the patent teaches partial removal. ShealySupp, ¶39; Ex. 1001, 3:52-54 (“The gate layer 15 can also be over-etched, removing about 0 to about 3 nm of the barrier layer 14 outside of the gate region”).

Dr. Shealy’s group at Cornell used an O-G-D process to form enhancement mode GaN transistors long before the ’508 patent. ShealySupp, ¶36; *Kim*, 1 (an O-G-D process for GaN transistor device fabrication); *Green*, 1 (same); *Kaper*, 1 (same). The O-G-D process was commonly used to form GaN transistors that worked for the intended purpose. ShealySupp, ¶36; *Wang*, 1-2 (using an O-G-D process to produce “[h]igh-performance AlGa_N-GaN HEMTs”); *Suh*, Fig. 18, [0072]-[0080] (using an O-G-D process to produce an enhancement mode GaN transistor with a self-aligned gate).

The O (ohmic contact), G (gate), D (dielectric) process produces an operational GaN transistor and provides certain benefits, such as protecting the gate from the anneal process of ohmic contacts. ShealySupp, ¶36.

III. *Yoshida-Beach-Sheppard* (Ground 1) Render Obvious Claims 1-3

A. A POSITA Would Have Been Motivated to Combine the References

1. The Petition sufficiently explains the combination of *Yoshida* and *Beach*

EPC wrongly argues that “Petitioner failed to particularly explain the combination.” POR 34-36. The Petition explains that a POSITA would have been motivated to combine *Yoshida*’s process with *Sheppard*’s multiple transition layers and with *Beach*’s self-aligned gate process and ohmic etching process, and expected success in doing so. Pet. 18-24.

Yoshida teaches a D (dielectric), O (ohmic contact), G (gate) process, and a POSITA would have modified *Yoshida*’s D-O-G process to incorporate *Beach*’s self-aligned gate, following the D-O-G process above. ShealySupp, ¶32; §II.C.1. *Yoshida* teaches the sequence of etching the p-GaN layer, depositing a dielectric layer, and forming ohmic contacts (Figures (a)-(c), D-O-G diagram above). ShealySupp, ¶32; *Yoshida*, [0022]-[0023] (using a D-O-G process). To incorporate *Beach*’s self-aligned gate and protect the gate region from contamination during subsequent processing steps, a POSITA would have modified *Yoshida*’s process to implement Figures (d) and (e) of the D-O-G process, before forming the gate structure. ShealySupp, ¶32. It would have been obvious to modify *Yoshida*’s process to implement a self-aligned gate structure, as shown below.

DOG Process Order
(*Yoshida-Beach*)

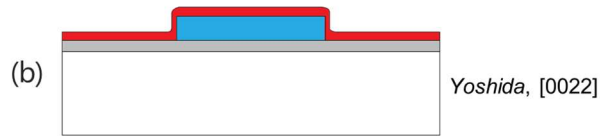
Legend	
	Resist
	p-GaN
	AlGaIn Barrier
	Dielectric
	GaN Buffer
	Gate Metal
	Ohmic Metal*

* Source/Drain Contacts

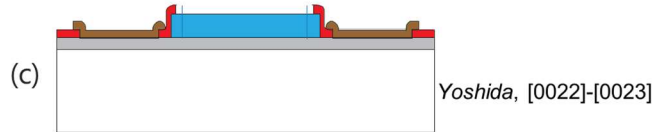
- 1) Epitaxy Grown - buffer/barrier/p-GaN
- 2) Resist Applied



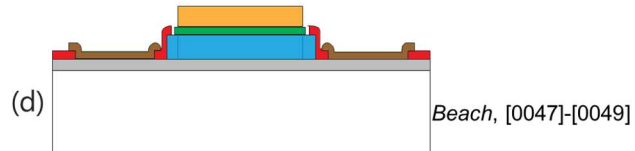
- 3) p-GaN Layer Etched
- 4) Dielectric Layer Deposited (D)



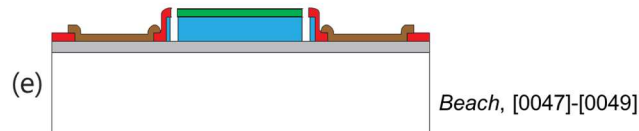
- 5) Windows Opened in Dielectric for Contacts
- 6) Ohmic Contact Metal Applied, Patterned, Annealed (O)



- 7) Patterned Gate Contact (G) Metal Applied
- 8) Gate Resist Applied



- 9) Self Aligned Etch of Gate Metal and p-GaN (G)
- 10) Strip Resist



ShealySupp, ¶32 (Modified *Yoshida* process).

Sheppard's multiple transition layers and *Beach's* self-aligned gate process and source and drain etching process were conventional techniques used in semiconductor fabrication before the patent. Shealy (Ex. 1003), ¶¶105, 127.

A POSITA would have incorporated these conventional techniques into *Yoshida*.

Id., ¶¶105, 129. Nothing more is required for a reasonable expectation of success.

Pfizer, Inc. v. Apotex, Inc., 480 F.3d 1348, 1364 (Fed. Cir. 2007) (“the expectation of success need only be reasonable, not absolute.”).

2. EPC does not properly address the Petition’s combination

EPC does not address the Petition’s combination—incorporating *Beach*’s self-aligned gate process and etching process to form an ohmic contact—into *Yoshida*’s process of forming a GaN transistor. Pet. 21-24. Instead, EPC argues bodily incorporation of *Beach*’s “gate-simultaneous” formation. POR 36-41.

EPC’s arguments requiring bodily incorporation of *Beach*’s “gate-simultaneous” process should be rejected. Bodily incorporating *Beach*’s process into *Yoshida* is not the law. *In re Mouttet*, 686 F.3d 1322, 1332 (Fed. Cir. 2012) (“It is well-established that a determination of obviousness ... does not require an actual, physical substitution of elements.”); *In re Keller*, 642 F.2d 413, 425 (CCPA 1981) (“The test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference ... [but] what the combined teachings of [those] references would have suggested”).

3. The claims do not require a “gate-first” process

EPC wrongly argues the proposed combination is not a “gate-first” process. POR 37, 41. The claims do not require an order between forming a gate and ohmic contacts. §II. EPC’s argument should be rejected for not addressing any claim elements required by the patent. *Intelligent Bio-Sys., Inc v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1367 (Fed. Cir. 2016) (the correct inquiry is whether a POSA would have “ha[d] a motivation to combine accompanied by a reasonable expectation of achieving *what is claimed in the patent-at-issue*.”) (emphasis added).

4. A “gate-first” process would have been obvious

Regardless, a “gate-first” process would have been obvious. ShealySupp, ¶41. Dr. Shealy explains that a “gate-first” process is one of only six sequencing permutations available—all of which are suitable options. ShealySupp, ¶43; *PAR Pharm., Inc. v. TWI Pharms., Inc.*, 773 F.3d 1186, 1197-98 (Fed. Cir. 2014) (obviousness “does not require that the motivation be the best option, only that it be a suitable option from which the prior art did not teach away.”). A POSITA would have been motivated to select a gate-first G-D-O process to self-align the ohmic source and drain contacts to the gate contact to reduce the minimum source-to-gate distance and reduce the source and drain access resistance. ShealySupp, ¶42. At minimum, a POSITA would have found it

obvious to try a “gate-first” G-D-O process and expected success to do so.

ShealySupp, ¶43; *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 421 (2007).

B. Petitioner’s Combination Is Not Based on Impermissible Hindsight

EPC wrongly argues Petitioner’s combination of *Yoshida* and *Beach* for elements [1e] and [1g] is based on hindsight. POR 41-42. Petitioner’s combination is based on the teaching of references and knowledge of a POSITA, not hindsight. The Petition explains how a POSITA would have been motivated and expected success in the combination of *Yoshida* and *Beach*. Pet. 21-24. Dr. Shealy further explains how a POSITA would have modified *Yoshida*’s process in view of *Beach*. Ex. 2002, 92:10-93:8, 94:8-95:23, 102:22-103:8; ShealySupp, ¶32; *In re McLaughlin*, 443 F.2d 1392, 1395 (CCPA 1971) (“so long as [obviousness] takes into account only knowledge which was within the level of ordinary skill in the art at the time the claimed invention was made and does not include knowledge gleaned only from applicant’s disclosure, such a reconstruction is proper.”).

EPC repeatedly argues that the combination of *Yoshida* and *Beach* presents an ordering different from the embodiments of the patent, contradicting that Petitioner uses the patent as a guide in the combination.

C. A POSITA Would Have Been Motivated to Combine *Yoshida*'s Process with *Beach*'s Ohmic Formation Process

EPC wrongly argues that *Yoshida* discloses a lift-off process of ohmic formation and that a POSITA would not replace it with *Beach*'s etching process. POR 43-47. *Yoshida* is silent on its ohmic formation process. Regardless, a POSITA would have been motivated to combine *Yoshida*'s process with *Beach*'s ohmic formation process.

1. *Yoshida* does not describe a lift-off process

Yoshida is silent about its process to use for ohmic formation. *Yoshida* simply says "metal Al deposited on the exposed n-type InGaN layer 4 to load source electrode S and drain electrode D." *Yoshida*, [0022]. *Yoshida*'s figures show no lift-off process for ohmic formation. EPC argues *Yoshida*'s Figure 1 "has ohmic contacts having vertical linear sidewalls entirely aligned with the etched dielectric material indicative of a self-aligned lift-off process." POR 44. *Yoshida*'s Figure 1, however, does not show dielectric material. ShealySupp, ¶48.

Dr. Schubert wrongly argues that a lift-off process produces ohmic contacts with sidewalls aligned with the edges of the dielectric layer, which he alleges cannot be achieved by etching. As Dr. Shealy explains, whether the vertical sidewalls of ohmic contacts are aligned with the dielectric material does not indicate either a lift-off or an etching process. ShealySupp, ¶49. But metal etching

is more precise than the lift-off process and can be used to produce aligned sidewalls. *Id.*

To minimize the undesired residual metal in the lift-off process, a negative (non-vertical) profile of photoresist is typically used for lift-off, shown in the left side of *Gorowitz*, Figure 1 (Dr. Shealy annotated). ShealySupp, ¶50; *Collins*, 2 (lift-off structure in which “the top of the resist line larger than the bottom”), Fig. 1 (lift-off structure having a non-vertical profile). The negative profile of photoresist results in a sloped sidewall of the remaining metal, different from the vertical sidewalls of the ohmic contacts in *Yoshida*. ShealySupp, ¶50.

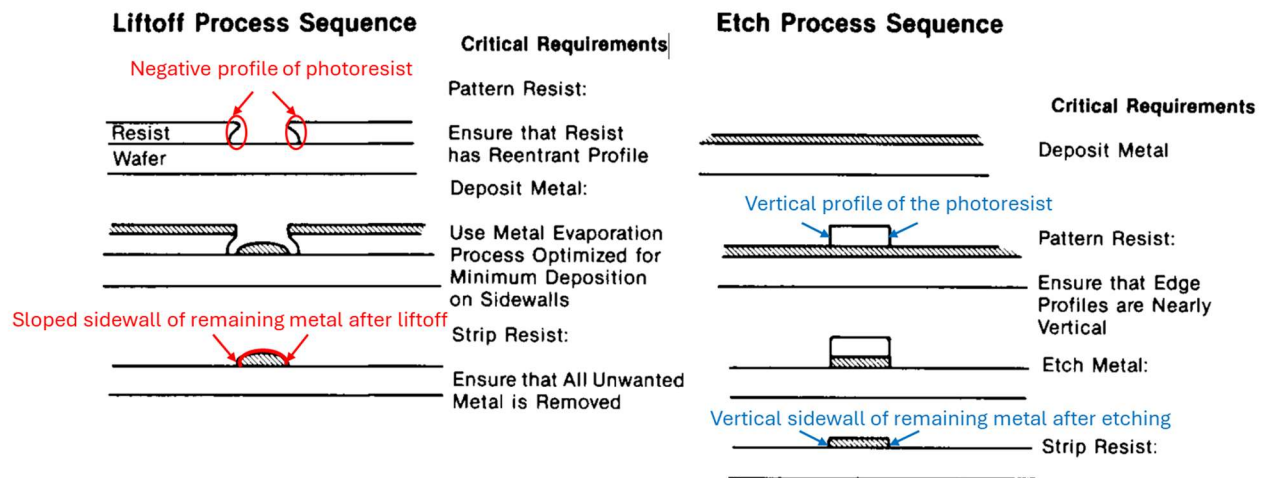
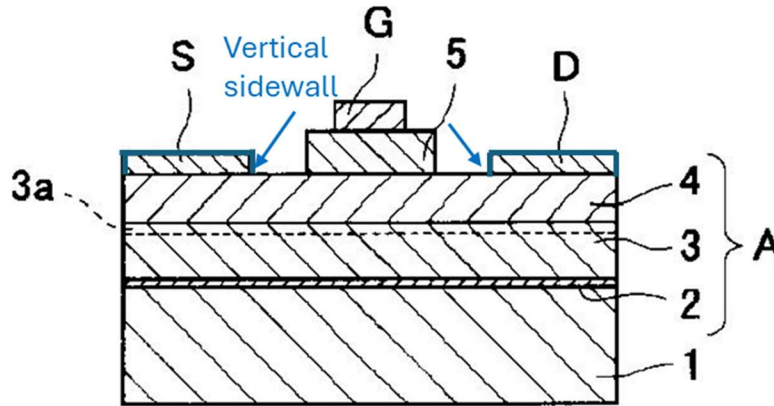


Fig. 1. Comparison of additive (liftoff) and subtractive (etch) metallization patterning processes.

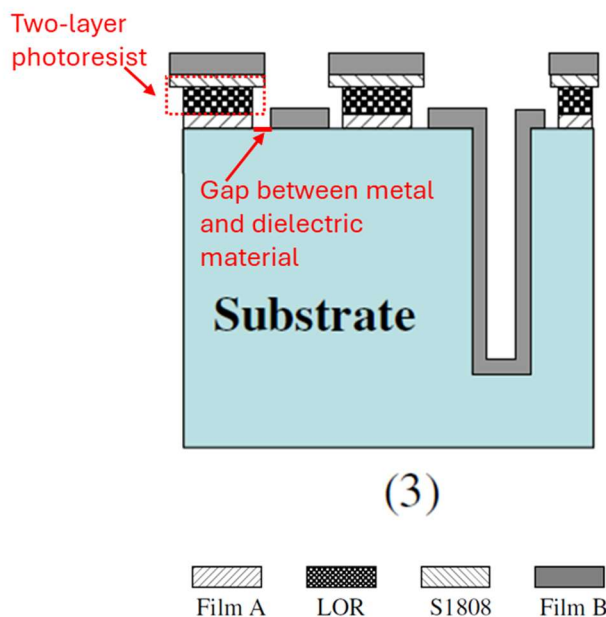
Gorowitz, Fig. 1.



Yoshida, Fig. 1.

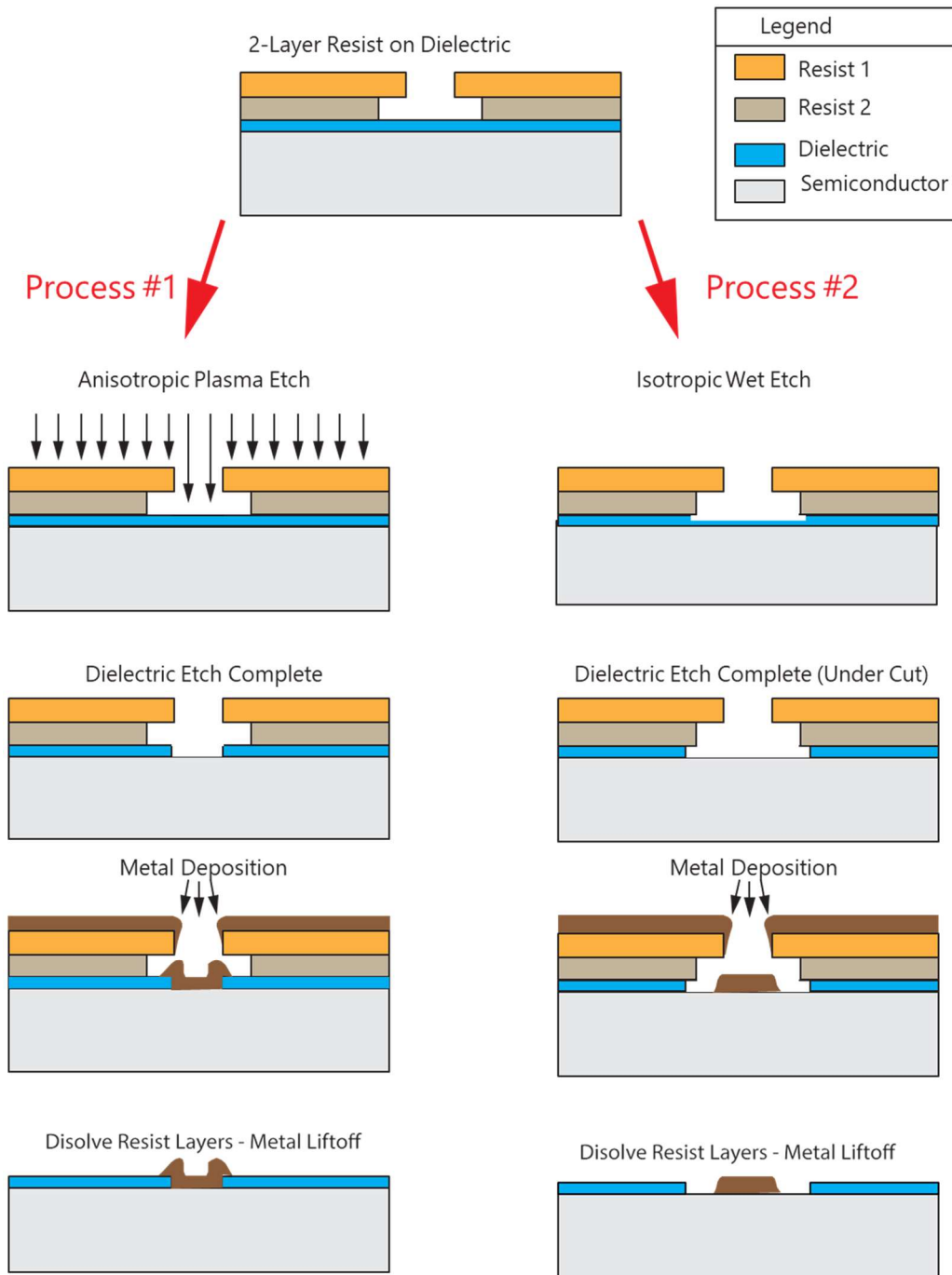
The right side of *Gorowitz*, Figure 1, shows an etching process. And as shown, a vertical photoresist profile is used for the etching process, resulting in vertical sidewalls of the metal material after the etching process, like the vertical sidewalls of ohmic contacts in *Yoshida*. ShealySupp, ¶51.

Another commonly used photoresist in lift-off process is the multi-layer photoresist, consisting of a top layer of wider photoresist and a lower layer of narrower photoresist. ShealySupp, ¶52. The multi-layer photoresist used in the lift-off process creates a gap between the metal and the dielectric layer (film A), as shown in *Liang*, Figure 1-(3) (Dr. Shealy annotated).



Liang, Fig. 1-(3).

The multi-layer photoresist in lift-off process produces non-aligned metal and dielectric layer, shown in the schematic representations Dr. Shealy provides below. ShealySupp, ¶54. The dielectric layer can be removed by either plasma etching (left process) or wet etching (right process). In either, the sidewall of the metal is not aligned with the edge of the dielectric layer, unlike *Yoshida's* structure.



ShealySupp, ¶54.

Contrary to Dr. Schubert, aligning the sidewalls of ohmic contacts with the edge of dielectric layer **is more difficult** using lift-off than metal etching.

ShealySupp, ¶55; Gorowitz, 23 (“The most accurate and controllable methods of

replicating the dimensions of the resist pattern involve the use of anisotropic plasma etching”). *Yoshida*’s ohmic contacts having vertical sidewalls are more likely achieved by etching, as taught by *Beach*. ShealySupp, ¶55.

2. A POSITA would have been motivated to form *Yoshida*’s ohmic contacts using *Beach*’s etching process

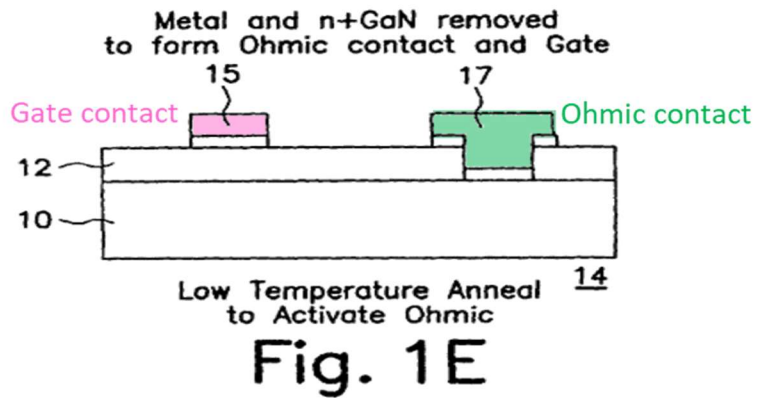
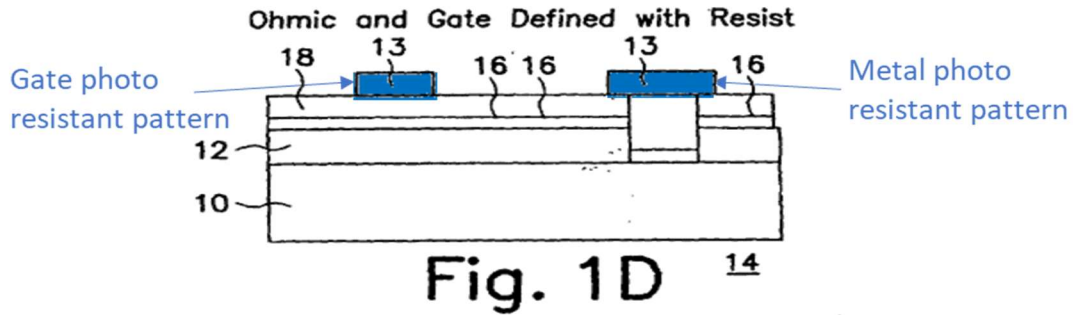
Regardless, a POSITA would have found it obvious to use an etching process to form the ohmic contacts. A POSITA would have understood that etching and lift-off are the only two prevalent techniques. ShealySupp, ¶56; *Gorowitz*, 4 (describing that “[w]hen resist patterns are used to define metal layers, the process can be either additive [lift-off] or subtractive [etching]).” *Yoshida* does not suggest that performing an etching process or lift-off was critical to its method to form a GaN transistor, and variations were a matter of design choice. ShealySupp, ¶56. When only two equally viable approaches are available, either would seem to be obvious. *ACCO Brands Corp. v. Fellowes, Inc.*, 813 F.3d 1361, 1367 (Fed. Cir. 2016) (finding motivation where there are only two ways to combine prior art elements); *KSR*, 550 U.S. at 421.

Obviousness “does not require that a particular combination must be the preferred, or the most desirable, combination described in the prior art in order to provide motivation for the current invention.” *Novartis Pharms. Corp. v. West-Ward Pharms. Int’l Ltd.*, 923 F.3d 1051, 1059 (Fed. Cir. 2019) (quoting *In re Fulton*, 391 F.3d 1195, 1200 (Fed. Cir. 2004)). *Beach*’s etching technique provides

performance benefits over lift-off, e.g., more accurate and controllable to pattern the metal. Pet. 23-24; Ex. 2002, 105:19-106:15 (“lift-off is avoided in a manufacturing environment at almost all costs”); *Gorowitz*, 4 (“Subtractive (etching) processes are more typically used”), 23 (“The most accurate and controllable methods of replicating the dimensions of the resist pattern involve the use of anisotropic plasma etching”); *ShealySupp*, ¶56. That *Beach*’s etching process provides certain performance benefits provides sufficient motivation to adopt it to form *Yoshida*’s ohmic contacts.

D. *Yoshida* and *Beach* Render Obvious “a Gate Photo Resistant Pattern” and “a Metal Photo Resistant Pattern”

EPC wrongly argues “*Beach* does not disclose or suggest separate steps (as claimed) of applying a gate photo resistant pattern and a metal photo resistant pattern.” POR 48-53. The Board correctly found that the claims **do not** require applying patterns at different times. Paper 11 (Institution Decision), 27. Although *Beach* labels both the “gate photo resistant pattern” and “metal photo resistant pattern” with the same number (13), they are different patterns placed at different locations, meeting the claim. Pet. 32, 36-37.



Beach, Figs. 1D, 1E.

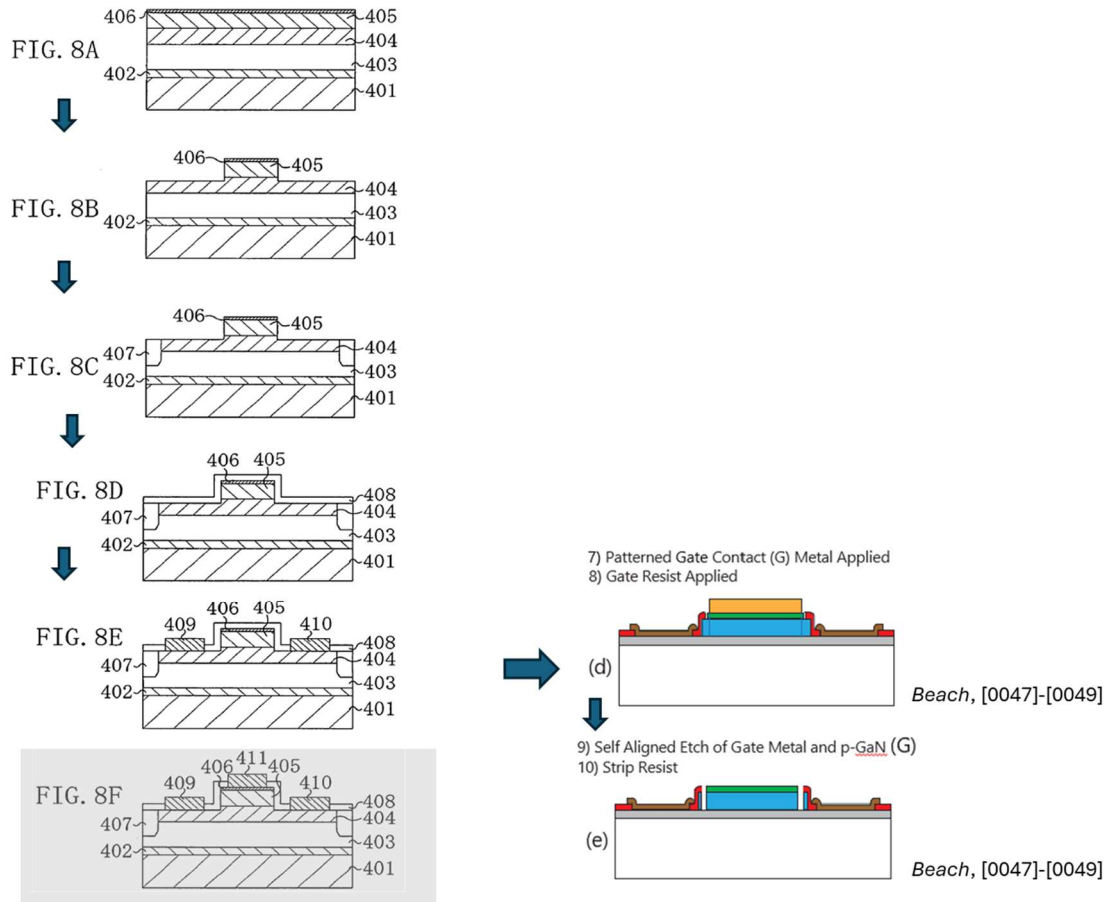
Regardless, as the Petition explains, *Yoshida* forms its gate structure and ohmic contacts in separate steps. Pet. 30-31, 35; *Yoshida*, [0022]-[0023]. The Petition explains that *Beach* renders obvious applying gate photo resistant and metal photo resistant patterns to form *Yoshida*'s gate structure and ohmic contacts, respectively. Pet. 31-33, 36-39. Thus, the **combination** of *Yoshida-Beach* renders obvious **separate** steps of applying a gate photo resistant and metal photo resistant patterns at different times.

IV. *Hikita-347-Beach-Sheppard* (Ground 2) Renders Obvious Claims 1-4

A. The Petition Sufficiently Explains the Combination of *Hikita-347* and *Beach*

Like in the *Yoshida* ground, EPC argues that the Petition does not particularly describe the combination. POR 54. EPC's argument fails for the same reason as explained for the *Yoshida* ground.

The petition explains that a POSITA would have been motivated to and expected success in combining *Hikita-347*'s process with *Sheppard*'s multiple transition layers and *Beach*'s self-aligned gate process and source and drain etching process. Pet. 47-51. *Hikita-347* describes a "D (dielectric), O (ohmic contact), G (gate)" process to form the enhancement-mode GaN transistor. *Hikita-347*, [0059]-[0061], Figs. 8A-8F; ShealySupp, ¶31. As Dr. Shealy explained, a POSITA would have combined *Hikita-347*'s D-O-G process with *Beach*'s self-aligned gate process and expected success. ShealySupp, ¶31; Ex. 2003, 2; Ex. 2002, 92:10-93:8, 94:8-95:23, 102:22-103:8. To incorporate *Beach*'s self-aligned gate, a POSITA would have modified *Hikita-347*'s Figure 8F to implement Figures (d) and (e) of the D-O-G process (below).



ShealySupp, ¶31 (Modified *Hikita-347* process).

B. A POSITA Would Have Been Motivated to Combine *Hikita-347*'s Process with *Beach*'s Self-Aligned Gate Process

Like for the *Yoshida* ground, EPC wrongly argues a POSITA would not be motivated to replace *Hikita-347*'s “gate-last” process with *Beach*'s “gate-simultaneous” process. POR 54-55. Again, EPC's argument is irrelevant to Petitioner's combination—incorporating *Beach*'s self-aligned gate process and etching process—not *Beach*'s “gate-simultaneous” process—into *Hikita-347*.

§III.A.2.

C. A POSITA Would Have Been Motivated to Combine *Hikita-347*'s Process with *Beach*'s Ohmic Formation Process

Like for the *Yoshida* ground, EPC wrongly argues that *Hikita-347* discloses a lift-off process. POR 56-58. *Hikita-347* is silent on its ohmic formation process. Regardless, a POSITA would have been motivated to combine *Hikita-347*'s process with *Beach*'s etching process.

1. *Hikita-347* does not describe a lift-off process

Hikita-347 simply says, “[e]ach of a source electrode 490 and a drain electrode 410 is formed of a Ti layer and an Al layer in an associated one of the openings”—it does not describe a lift-off process. *Hikita-347*, [0060].

Hikita-347's figures do not show lift-off. As explained for *Yoshida*, the precise alignment between the sidewalls of the ohmic contact and dielectric material is better achieved by an etching process. ShealySupp, ¶60; §III.C.1. *Hikita-347* likely uses an etching process, as taught by *Beach*. ShealySupp, ¶60.

2. A POSITA would have been motivated to form *Hikita-347*'s ohmic contacts using *Beach*'s etching process

Regardless, a POSITA would have found it obvious to use an etching process to form *Hikita-347*'s ohmic contacts, as explained in the *Yoshida* ground. ShealySupp, ¶61; §III.C.2.

D. Whether Beach Discloses an Enhancement Mode or Depletion Mode Device Is Irrelevant

EPC argues that *Hikita-347*'s enhancement mode devices and *Beach*'s depletion mode devices are not combinable. POR 58-59. Petitioner's combination, however, incorporates *Beach*'s self-aligned gate process and etching process—not its wholesale transistor-forming process—into *Hikita-347*.

Dr. Shealy explained that the ohmic contacts and gate processes are the same in enhancement mode and depletion mode devices, and a POSITA would have understood that *Beach*'s self-aligned gate process and ohmic etching process are applicable to both enhancement mode and depletion mode devices. Ex. 2002, 104:8-105:11.

Moreover, *Beach* discloses that an enhancement mode (normally off) device is desirable, and Dr. Schubert acknowledged this before the ITC. *Beach*, [0004] (describing that a nominally off device is desirable), [0012] (same); Ex. 1053, 1025:12-1026:24.

E. Whether Beach's Gate Contact and Ohmic Contacts Are Formed of the Same Material Is Irrelevant

EPC wrongly argues that, because *Hikita-347*'s gate contact and ohmic contacts are formed of different materials and *Beach* teaches the same electrode metal for its gate and ohmic contacts, a POSITA would not have been motivated to combine them. POR 59-60. Petitioner's combination incorporates *Beach*'s

self-aligned gate process and etching process—not *Beach*’s entire process. EPC’s argument improperly calls for bodily incorporation. *In re Etter*, 756 F.2d 852, 859 (Fed. Cir. 1985) (noting that whether one prior art reference can be incorporated into another is “basically irrelevant.”).

F. The Claims Do Not Require a “Gate-First” Process

EPC repeats its flawed argument that none of *Hikita-347*, *Beach*, or *Sheppard* teaches a “gate-first” process. POR 60-61. The claims do not require a “gate-first” process. §II. Regardless, a “gate-first” process would have been obvious. §III.A.4.

G. *Hikita-347* and *Beach* Render Obvious “a Gate Photo Resistant Pattern” and “a Metal Photo Resistant Pattern”

Like for the *Yoshida* ground, EPC wrongly argues that the combination of *Hikita-347* and *Beach* does not teach both “a gate photo resistant pattern” and “a metal photo resistant pattern.” POR 61-63. The claims do not require applying the patterns at different times. §III.D. The Petition explains that *Hikita-347* forms a gate structure and ohmic contacts in separate steps. Pet. 56-57, 60-61; *Hikita-347*, [0060]-[0061]. The Petition explains that *Beach* renders obvious applying a gate photo resistant pattern and a metal photo resistant pattern to form *Hikita-347*’s gate structure and ohmic contacts, respectively. Pet. 57-58, 61. The **combination** of *Hikita-347* and *Beach* renders obvious separate steps of applying a gate photo resistant pattern and a metal photo resistant pattern at different times.

V. *Hikita-023-Beach-Sheppard* (Ground 3) Renders Obvious Claim 5

A. A POSITA Would Have Been Motivated to Combine *Hikita-023*'s Process with *Beach*'s Self-Aligned Gate Process

Like for the *Yoshida* ground, EPC argues that a POSITA would not be motivated to replace *Hikita-023*'s "gate-last" process with *Beach*'s "gate-simultaneous" process. POR 63-64. EPC's argument is irrelevant to Petitioner's combination—incorporating *Beach*'s self-aligned gate process and etching process for ohmic contact formation—not *Beach*'s "gate-simultaneous" process—to *Hikita-023*'s process. EPC's argument fails for the reasons explained in the *Yoshida* ground. ShealySupp, ¶38; §III.A.2.

B. A POSITA Would Have Been Motivated to Combine *Hikita-023*'s Process with *Beach*'s Ohmic Formation Process

EPC wrongly argues that *Hikita-023* discloses a lift-off process and that a POSITA would not replace it with *Beach*'s etching process. POR 64-65. *Hikita-023*'s lift-off process is not critical to its method to form a GaN transistor, and variations of such was a matter of design choice. *Hikita-023*, [0079]; ShealySupp, ¶63. For the reasons explained above, a POSITA would have found it obvious to use the etching process taught by *Beach* to form the ohmic contacts. *Id.*; §III.C.2.

C. Whether Beach Discloses an Enhancement Mode or Depletion Mode Device Is Irrelevant

Like for the *Hikita-347* ground, EPC wrongly argues that because *Hikita-023* describes enhancement mode devices and *Beach* describes depletion mode devices, a POSITA would not have been motivated to combine them. POR 65. EPC’s argument fails for the reasons explained for the *Hikita-347* ground. §IV.D.

D. Whether Beach’s Gate Contact and Ohmic Contacts Are Formed of the Same Material Is Irrelevant

Like for the *Hikita-347* ground, EPC argues that because *Hikita-023*’s gate contact and ohmic contacts are formed of different materials and *Beach* teaches the same material for both contacts, a POSITA would not have been motivated to combine the teachings of *Hikita-023* with *Beach*. POR 65-66. EPC’s argument fails for the reasons explained for the *Hikita-347* ground. §IV.E.

E. The Claims Do Not Require a “Gate-First” Process

EPC repeats its argument that none of *Hikita-023*, *Beach*, or *Sheppard* teaches a “gate-first” process. POR 66-67. The claims do not require a “gate-first” process, and a “gate-first” process would have been obvious, as explained above. ShealySupp, ¶43; §§II, III.A.4.

F. *Hikita-023* and *Beach* Render Obvious “a Gate Photo Resistant Pattern” and “a Fourth Photo Resistant Pattern”

Like for the *Yoshida* ground, EPC wrongly argues that the combination of *Hikita-023* and *Beach* does not teach both “a gate photo resistant pattern” and “a fourth photo resistant pattern.” POR 67-69. The claims do not require applying the patterns at different times. §III.D. The Petition explains that *Hikita-023* forms a gate structure and ohmic contacts in separate steps. Pet. 85, 89; *Hikita-023*, [0079]-[0080]. The Petition explains that *Beach* renders obvious applying a gate photo resistant pattern and a fourth photo resistant pattern to form *Hikita-023*’s gate structure and ohmic contacts, respectively. Pet. 85-86, 89-90. Thus, the **combination** of *Hikita-023* and *Beach* renders obvious separate steps of applying a gate photo resistant pattern and a fourth photo resistant pattern at different times.

VI. The Board Should Give Dr. Schubert’s Declaration Little Weight

The Board should give little weight to the testimony of Dr. Schubert because he has no practical experience with GaN transistors. Dr. Schubert’s experience with GaN semiconductor devices is limited to light-emitting diode (LED) devices, not with any GaN transistor of the type in the ’508 patent. The publications listed in paragraph 13 of Schubert’s declaration are related to **GaAs** transistors, not **GaN** transistors. While some publications are related to GaN material, they are not in the context of forming a GaN **transistor** of the type in the ’508 patent. Ex. 2001, ¶13. Dr. Schubert has no personal experience of building a GaN transistor. Dr. Schubert

does not meet EPC's definition of a POSITA because he does not have "three years of professional work experience in the epitaxial growth" of semiconductor devices. POR 17; Ex. 2001, Appx. A.

Unlike Dr. Schubert, Dr. Shealy is one of the pioneer scientists in the field of GaN transistors. Ex. 2002, 87:15-88:17. His research was focused on GaN transistors during his tenure at Cornell. Ex. 1003, ¶¶15-18; Ex. 2002, 87:15-88:17. He led a research group at Cornell focusing on technologies to develop GaN transistors and had significant experience building GaN transistors. Ex. 1003, ¶¶15-18; Ex. 2002, 87:15-88:17. His research lab at Cornell built the first GaN HEMT device on silicon in 1999. Ex. 2002, 87:19-23. Dr. Shealy has published over 50 peer-reviewed articles on GaN transistors. Ex. 1003, Appx. A. Dr. Shealy's testimony should be given more weight than Dr. Schubert's testimony.

VII. Conclusion

For these reasons and those in the Petition, the challenged claims should be canceled.

Dated: September 4, 2024

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CERTIFICATION OF WORD COUNT

Pursuant to 37 C.F.R. §42.24, Petitioner certifies that the word count of Petitioner's Reply (exclusive of any table of contents, table of authorities, mandatory notices under §42.8, certificates of service and word count, and list of exhibits or claim listing) as measured by Microsoft Word is 5,587.

Dated: September 4, 2024

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CERTIFICATE OF SERVICE

The undersigned certifies that a copy of the foregoing **Petitioner's Reply to Patent Owner's Response** was served electronically on September 4, 2024, via email directed to counsel of record for the Patent Owner at:

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