

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INNOSCIENCE (ZHUHAI) TECHNOLOGY COMPANY, LTD.,
AND
INNOSCIENCE AMERICA, INC.,

Petitioner,

v.

EFFICIENT POWER CONVERSION CORPORATION,

Patent Owner.

Case No. IPR2023-01383
U.S. Patent No. 8,404,508

SECOND DECLARATION OF JAMES RICHARD SHEALY, PH.D.

TABLE OF CONTENTS

I.	INTRODUCTION	4
II.	QUALIFICATIONS	5
III.	MATERIALS CONSIDERED	5
IV.	LEGAL STANDARDS	7
V.	LEVEL OF ORDINARY SKILL IN THE ART	8
VI.	RESPONSE TO EPC’S CLAIM CONSTRUCTION of “gate-first” process	8
A.	Neither the Claim Language nor the Specification Requires a Gate-First Process.....	8
B.	The Claims Do Not Require a Field Plate.....	10
C.	The Claims Cover Non-Gate-First Processes	12
1.	First Example: D (dielectric), O (ohmic contact), G (gate) process.....	13
2.	Second Example: O (ohmic contact), G (gate), D (dielectric) process	21
D.	A POSITA Would Have Found a Gate-First Process Obvious	28
VII.	RESPONSE TO EPC’S ARGUMENTS REGARDING OHMIC FORMATION.....	30
A.	<i>Yoshida</i> Does Not Describe a Lift-off Process and a POSITA Would Have Been Motivated to Form <i>Yoshida</i> ’s Ohmic Contacts Using <i>Beach</i> ’s Etching Process.....	31
B.	<i>Hikita-347</i> Does Not Describe a Lift-off Process and a POSITA Would Have Been Motivated to Form <i>Hikita-347</i> ’s Ohmic Contacts Using <i>Beach</i> ’s Etching Process.....	39
C.	A POSITA Would Have Been Motivated to Form <i>Hikita-023</i> ’s Ohmic Contacts Using <i>Beach</i> ’s Etching Process.....	40

VIII. CONCLUSION.....	41
-----------------------	----

I. INTRODUCTION

1. I have been retained by Innoscience (Zhuhai) Technology Company, Ltd., and Innoscience America, Inc. (collectively “Innoscience”), as an independent expert for the above-identified *inter partes* review proceeding involving U.S. Patent No. 8,404,508 (“the ’508 patent”).

2. I am over 21 years of age and, if I am called upon to do so, I would be competent to testify as to the matters set forth herein.

3. My compensation is in no way contingent on the nature of my findings, the presentation of my findings in testimony, or the outcome of any proceeding.

4. I previously provided a declaration in this proceeding as Ex. 1003. My CV was previously submitted as Appendix A to Ex. 1003.

5. I have been asked to provide this supplemental declaration to analyze certain technical arguments in Patent Owner’s Response (POR) relating to the claimed gate formation and ohmic formation process, and related opinions stated in the declaration of Dr. E. Fred Schubert in support thereof.

6. While I disagree with many other positions expressed by Dr. Schubert in his declaration, I have not been asked to opine on those disagreements here.

7. Based on my experience, my knowledge of the art at the relevant time, my analysis of prior art, the understanding a person of ordinary skill in the art

(POSITA) would have had regarding the claim terms in light of the specification, and my analysis technical arguments of Efficient Power Conversion Corporation (“Patent Owner” or “EPC”), it remains my opinion that each of claims 1–5 of the ’508 patent is unpatentable for at least the reasons I discuss below.

8. Throughout this declaration, I refer to specific pages, figures, and/or line numbers of various exhibits. These citations are illustrative and are not intended to suggest that they are the only support for the propositions for which they are cited.

II. QUALIFICATIONS

9. My qualifications have been provided in my prior declaration. Ex. 1003, ¶¶8-21.

III. MATERIALS CONSIDERED

10. In forming my opinions, I have reviewed my prior declaration, the following additional documents, and any other document cited in this declaration or my previous declaration:

Exhibit	Description
Ex. 1042	H. Kim et al., “Effects of SiN Passivation and High-Electric Field on AlGa _N –Ga _N HFET Degradation,” IEEE Electron Device Letters, vol. 24, no. 7, July 2003, pp. 421-423 (“ <i>Kim</i> ”)
Ex. 1043	B. Green et al., “The Effect of Surface Passivation on the Microwave Characteristics of Undoped AlGa _N /Ga _N HEMT’s,” IEEE Electron Device Letters, vol. 21, no. 6, June 2000, pp. 268-270 (“ <i>Green</i> ”)

Exhibit	Description
Ex. 1044	V. Kaper et al., “High-Power Monolithic AlGaIn/GaN HEMT Oscillator,” IEEE Journal of Solid-State Circuits, vol. 38, no. 9, September 2003, pp. 1457-1461 (“ <i>Kaper</i> ”)
Ex. 1045	W. Wang et al., “Performance Enhancement by Using the n ⁺ -GaIn Cap Layer and Gate Recess Technology on the AlGaIn–GaIn HEMT Fabrication,” IEEE Electron Device Letters, vol. 26, no. 1, January 2005, pp. 5-7 (“ <i>Wang</i> ”)
Ex. 1046	U.S. Patent Application Publication No. 2008/0296618 to Suh et al., published December 4, 2008 (“ <i>Suh</i> ”)
Ex. 1047	R. Thompson et al., “Improved Fabrication Process for Obtaining High Power Density AlGaIn/GaN HEMTs,” IEEE GaAs Digest, November 2003, pp. 298-300 (“ <i>Thompson</i> ”)
Ex. 1048	Gorowitz et al., “Methods of Metal Patterning and Etching,” 1987 (“ <i>Gorowitz</i> ”)
Ex. 1049	George G. Collins et al., “Process Control of the Chlorobenzene Single-Step Liftoff Process with a Diazo-Type Resist,” IBM Journal of Research and Development, vol. 26, no. 5, September 1982, pp. 596-604 (“ <i>Collins</i> ”)
Ex. 1050	J. Liang et al., “Improved Bi-Layer Lift-off Process for MEMS Applications,” Microelectronic Engineering, vol. 26, issues 5-6, May 2008 (“ <i>Liang</i> ”)
Ex. 1051	Walker et al., “Handbook of Metal Etchants,” 1991 (“ <i>Walker</i> ”)
Ex. 1052	E. Harvard et al., “Performance of AlGaIn/GaN High-Electron Mobility Transistors With AlSiN Passivation,” IEEE Transactions on Electron Devices, vol. 58, No. 1, January 2011 (“ <i>Harvard</i> ”)
Ex. 2001	Declaration of Dr. E. Fred Schubert
Ex. 2004	U.S. Patent 6,478,871, filed Oct. 2, 2000
Ex. 2005	U.S. Patent 9,991,360, filed Mar. 5, 2012

Exhibit	Description
Ex. 2007	U.S. Patent D715,107, filed Jul. 26, 2013

11. I have also relied on my education, experience, research, training, and knowledge in the relevant art, and my understanding of any applicable legal principles described in this declaration.

12. All of the opinions contained in this declaration are based on the documents I reviewed and my knowledge and professional judgment. My opinions have also been guided by my understanding of how a person of ordinary skill in the art would have understood the claims of the '508 patent at the time of the alleged invention. For purposes of this declaration, I have been asked to assume that the date of the alleged invention is the earliest claimed priority date: April 8, 2009.

13. I reserve the right to supplement and amend any of my opinions in this declaration based on documents, testimony, and other information that becomes available to me after the date of this declaration.

IV. LEGAL STANDARDS

14. My understanding of the relevant legal standards is set forth in my previous declaration. Ex. 1003, ¶¶24-47.

V. LEVEL OF ORDINARY SKILL IN THE ART

15. My understanding of the level of ordinary skill in the art is set forth in my previous declaration. Ex. 1003, ¶¶68-69. I have applied the same level of ordinary skill in considering my opinions in this declaration.

16. I understand that Dr. Schubert provided a different definition in his declaration. *See* Ex. 2001, ¶80. My opinions in my previous declaration (Ex. 1003) and in this declaration do not change if I apply Dr. Schubert’s proposed definition of a POSITA.

VI. RESPONSE TO EPC’S CLAIM CONSTRUCTION OF “GATE-FIRST” PROCESS

17. In my Initial Declaration, I applied the plain and ordinary meaning of claim terms as understood by a POSITA in light of the specification and the prosecution history. I have reviewed the evidence and proposed construction of a “gate-first” process EPC provided in its POR. I disagree with EPC’s construction.

A. Neither the Claim Language nor the Specification Requires a Gate-First Process

18. On pages 17-25 of its POR, EPC argues that the claims of the ’508 patent are limited to a gate-first process, i.e., the gate structure is formed before the ohmic contacts. I disagree. The claim language does not recite an order in terms of whether the gate or the ohmic contacts should be formed first. The claimed gate structure steps include five steps: (1) depositing a gate contact layer; (2) applying a gate photo resistant pattern; (3) etching away the gate contact layer; (4) etching

away the doped GaN layer; (5) removing the gate photo resistant pattern. The claimed ohmic contact steps separately include five additional steps: (1) depositing an ohmic contact metal; (2) applying a metal photo resistant pattern; (3) etching the ohmic contact metal; (4) removing the metal photo resistant pattern; (5) performing rapid thermal annealing. The gate structure steps and ohmic contact steps are independent and self-contained. The gate structure and ohmic contacts are separate components of the transistor with separate functions, and logically the gate structure could be formed before, after, or simultaneously with the ohmic source and drain contacts.

19. Nor does the '508 patent emphasize an order between the formation of the gate or the ohmic contacts. The purported invention of the '508 patent has nothing to do with the ohmic contacts or the sequence of forming the gate structure compared to the ohmic contacts. For example, the '508 patent describes "[t]he present invention is an enhancement mode GaN HEMT device with a gate metal material and a doped GaN or AlGa_N material that are self-aligned, and a method for making such a device." Ex. 1001, 3:1-4. Therefore, the '508 patent describes the invention as providing a self-aligned gate structure, not the sequence of forming the gate structure compared to the ohmic contacts.

B. The Claims Do Not Require a Field Plate

20. On pages 18 through 22 of its POR, EPC argues that the '508 patent claims require a field plate formed simultaneously with the source contact. EPC argues that formation of the field plate is only achievable if the gate structure is formed before the ohmic metal is deposited. I disagree that the '508 patent claims require a field plate.

21. The claims of the '508 patent do not recite any field plate, much less a simultaneous formation of the field plate and source contact. The claims require “depositing an Ohmic contact metal,” “applying a metal photo resistant pattern,” “etching the Ohmic contact metal,” “removing the metal photo resistant pattern,” and “performing rapid thermal annealing” to form a source contact. Ex. 1001, 7:10-15. None of these steps require forming a field plate, a separate semiconductor feature from the source contact.

22. I understand that the original claims of the '508 patent include two independent claims 1 and 23, the only difference of which is the feature of field plate. Original claim 1 recites an enhancement-mode GaN transistor with various components but not a field plate, while claim 23 adds the field plate feature to the components included in claim 1, demonstrating that the field plate feature is an optional embodiment of the '508 patent. *Compare* Ex. 1002, 19 (claim 1), *with id.*, 26 (claim 23).

23. The '508 patent also describes the field plate as an optional embodiment. For example, the abstract states that: “The enhancement mode GaN transistor *may* also have a field plate made of Ohmic metal, where a drain Ohmic metal, a source Ohmic metal.” Ex. 1001, abstract (emphasis added). In contrast, the abstract states “the gate III-V compound and the gate metal *are* formed with a single photo mask process to be self-aligned and the bottom of the gate metal and the top of the gate compound have the same dimension.” Ex. 1001, abstract (emphasis added).

24. EPC points to the description of field plate appearing in the paragraph where the “present invention” is described as limiting the invention. There, the “present invention” does not refer to a field plate. Ex. 1001, 3:1-4 (“The present invention is an enhancement mode GaN HEMT device with a gate metal material and a doped GaN or AlGa_N material that are self-aligned, and a method for making such a device.”). Instead, the description of field plate is an add-on, non-limiting feature.

25. In my opinion, in view of the patent specification, language of the claims, and prosecution history of the '508 patent, a POSITA would have understood that the '508 patent claims cover devices without a field plate.

26. I also disagree with EPC that formation of a field plate requires a gate-first process. It was well known that a separate process can be carried out for

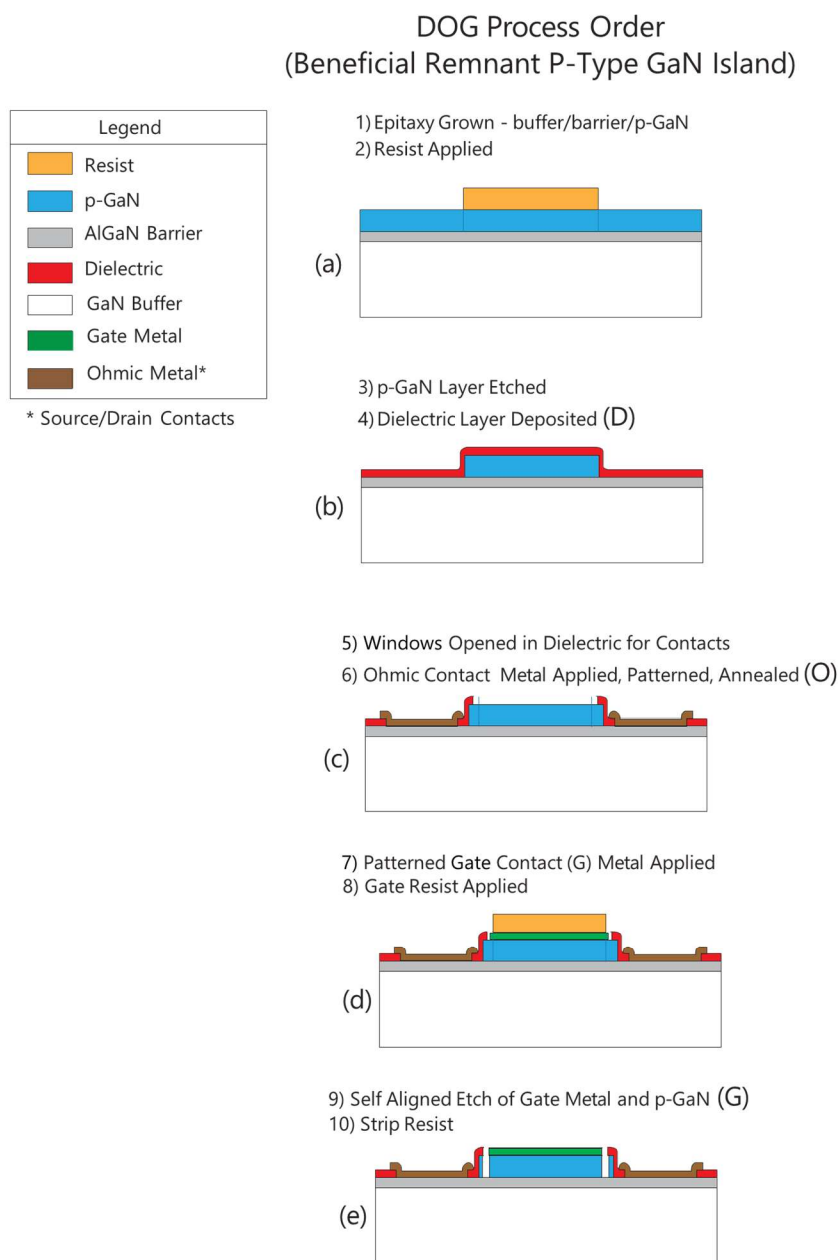
the field plate formation after the formation of ohmic contacts and gate contact. The formation of a field plate does not dictate the sequence between forming the gate and ohmic contacts. For example, *Hikita-895* (Ex. 1037) describes a process in which the gate is formed after the ohmic source and drain contacts, and a field plate is formed thereafter. *See Hikita-895*, [0056]-[0057]; *see also Saito*, 2, Fig. 1 (describing forming a device in a sequence of source and drain contacts, gate, and field plate). It was also well known that a field plate can be formed simultaneously with a gate contact, which can occur after forming the ohmic contacts. For example, *Kumar* (Ex. 1035) describes a process in which the ohmic contacts are formed first, and then the field plate is formed simultaneously with the gate contact, where the same metal is used to form both the gate contact and field plate. *See Kumar*, 1, Fig. 1.

C. The Claims Cover Non-Gate-First Processes

27. A POSITA would have understood that the '508 patent claims cover a process in which the gate structure is formed after the ohmic structure. As I explained in my deposition, the claims also cover a “D (dielectric), O (ohmic contact), G (gate)” process and “O (ohmic contact), G (gate), D (dielectric)” process, in which a self-aligned gate structure is formed after forming ohmic contact. I provide two examples below.

1. First Example: D (dielectric), O (ohmic contact), G (gate) process

28. As I explained in my deposition, the '508 patent claims cover a “D (dielectric), O (ohmic contact), G (gate)” process shown in the diagram below.



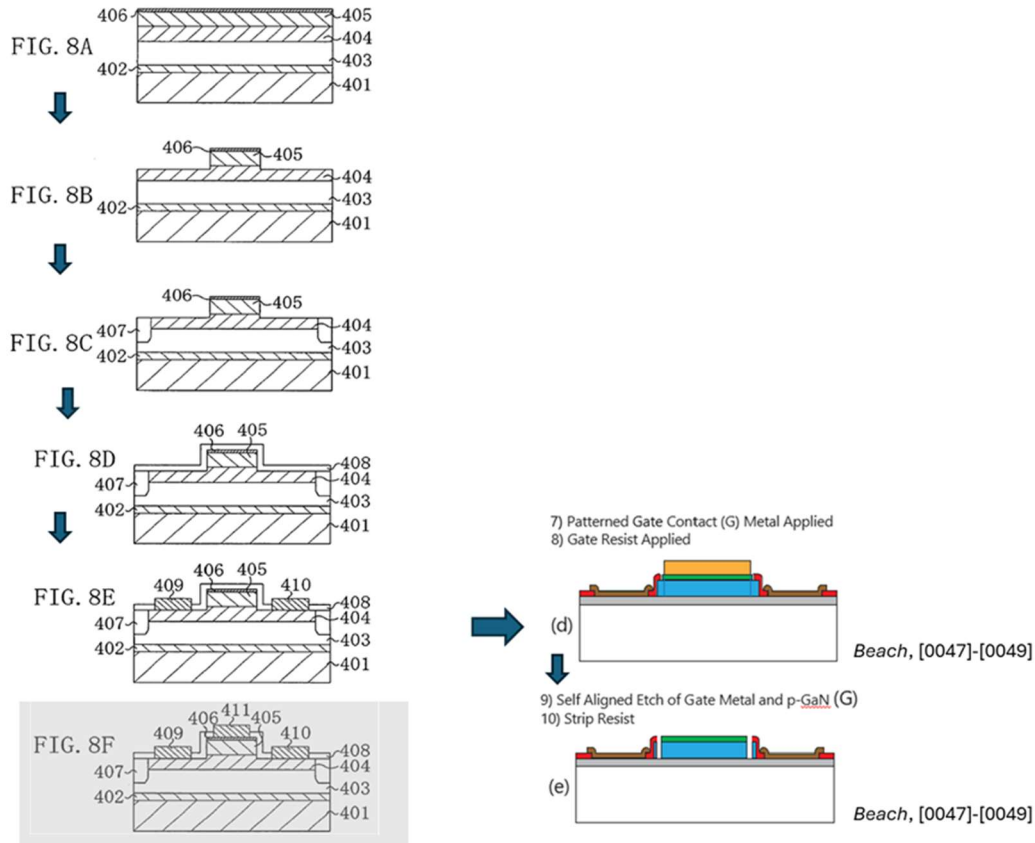
D (dielectric), O (ohmic contact), G (gate) process
(Beneficial Remnant P-Type GaN Island)

29. First, epitaxial layers and p-GaN layer are grown on the substrate, and a photoresist is applied over the p-GaN layer, shown in Figure (a) of the diagram above. Next, the p-GaN layer is etched, and a dielectric layer is deposited on the surface, shown in Figure (b). Then, windows are opened in the dielectric layer for ohmic contacts and gate contact, and ohmic contacts are formed in the openings on the barrier layer, shown in Figure (c). Then, patterned gate contact metal is applied in the opening on the p-GaN, and a photoresist is applied on the gate metal, shown in Figure (d). Finally, a self-aligned gate is formed using the photoresist, and the photoresist is removed, shown in Figure (e).

30. As I stated in my deposition, my research group at Cornell used a D (dielectric), O (ohmic contact), G (gate) process to form GaN transistors in early 2000 when we built HEMT devices at Cornell. *See Thompson*, 1 (describing a D, O, G process for GaN transistor device fabrication). The D (dielectric), O (ohmic contact), G (gate) process was commonly used to form GaN transistors that worked for the intended purpose. The devices produced from the DOG process at Cornell were state of art for milliwave and microwave transistors. A POSITA would have understood that the above D (dielectric), O (ohmic contact), G (gate) process produces an operational GaN transistor. The D (dielectric), O (ohmic contact), G (gate) process also provides a distinct advantage of protecting the gate region from contamination during subsequent processing steps, as I explained in my deposition.

A POSITA would have understood that the above D (dielectric), O (ohmic contact), G (gate) process produces an operational GaN transistor.

31. *Hikita-347* and *Yoshida* both teach such a D, O, G process. For example, *Hikita-347* teaches the step sequence of etching the p-GaN layer, depositing a dielectric layer, and forming ohmic contacts, as in Figures (a)-(c) of the diagram I provided above, as shown in Figures 8A-8E. *See Hikita-347*, Figs. 8A-8E, [0058]-[0061] (using an D, O, G process to produce a GaN transistor that “allows a sufficient large current density”). To incorporate a self-aligned gate as taught in *Beach*, a POSITA would have modified Figure 8F of *Hikita-347* to implement Figures (d) and (e) of the D-O-G process diagram I provided above. The modified process of *Hikita-347* is illustrated below. As I explained in my initial declaration, a POSITA would have been motivated and expected success in such modifications.



Modified *Hikita-347* process

32. *Yoshida* teaches a D, O, G process similar to *Hikita-347*. *Yoshida* teaches the step sequence of etching the p-GaN layer, depositing a dielectric layer, and forming ohmic contacts, as in Figures (a)-(c) of the D-O-G diagram I provided above. *Yoshida*, [0022]-[0023] (using a D, O, G process to produce a GaN transistor). To incorporate a self-aligned gate as taught in *Beach*, a POSITA would have modified *Yoshida*'s process to implement Figures (d) and (e) of the D-O-G process diagram I provided above, prior to formation of the gate structure. The modified process of *Yoshida* is illustrated below. As I explained in my initial declaration, a POSITA would have found it obvious to modify *Yoshida*'s process

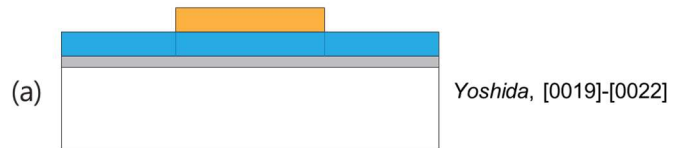
to implement a self-aligned gate structure, as shown below in the diagram for D-O-G process.



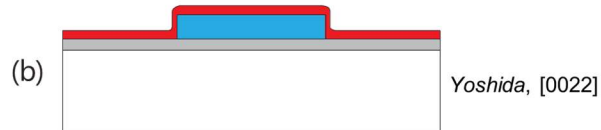
* Source/Drain Contacts

DOG Process Order (Yoshida-Beach)

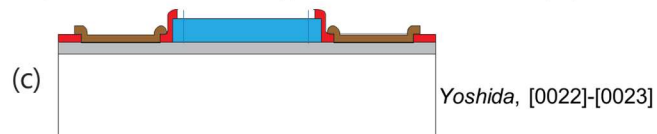
- 1) Epitaxy Grown - buffer/barrier/p-GaN
- 2) Resist Applied



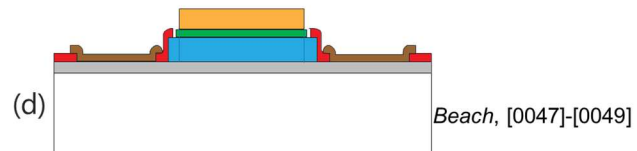
- 3) p-GaN Layer Etched
- 4) Dielectric Layer Deposited (D)



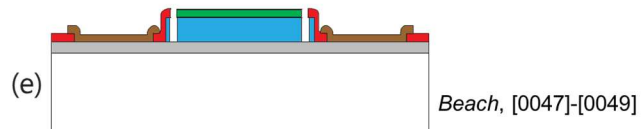
- 5) Windows Opened in Dielectric for Contacts
- 6) Ohmic Contact Metal Applied, Patterned, Annealed (O)



- 7) Patterned Gate Contact (G) Metal Applied
- 8) Gate Resist Applied



- 9) Self Aligned Etch of Gate Metal and p-GaN (G)
- 10) Strip Resist



Modified Yoshida process

33. Dr. Schubert argues that the D, O, G process is non-functional. Ex. 2001, ¶¶ 89-90. I disagree. Dr. Schubert argues that the remnant islands of the p-type semiconductor would render the device nonfunctional because the remnant islands of p-type GaN deteriorate the conductivity of the transistor's access regions and increase in the ON resistance. Ex. 2001, ¶ 91. This is not true. The remnant p-type island would have no detrimental effect to the performance of the device. To the contrary, the remnant p-type island could improve the performance of the device. The remnant p-type GaN island over the channel between the gate and drain can partially deplete some of the channel charge, which reduces the longitudinal electric field strength and in turn increases the device's breakdown voltage. The remnant p-type GaN island over the channel between the source and gate can lower the channel charge in this region, which is known to reduce the non-linear component of the device's source resistance, important for high frequency operation. *See Harvard*, 1-2, 4, 7 (describing that using an AlSiN passivation layer, which increases the resistance and reduces the channel charge in the region between the source contact and gate, increases the breakdown voltage and improves performance of the device).

34. Dr. Schubert's diagram also overstates the dimension of the remnant island of the p-type GaN material in the D, O, G process. The dimension of the remnant p-type GaN island is determined by the photoresist applied to etch the

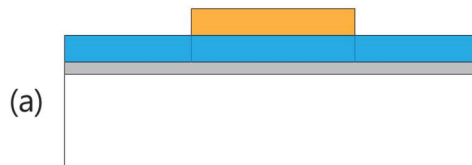
dielectric layer in Figure (c) of the D, O, G process diagram illustrated above, which determines the alignment of dielectric layer to the p-type GaN's edge. A POSITA would have understood that, if desired, no remnant p-type GaN island would have been left by applying appropriate photoresist, as shown in the diagram below.

DOG Process Order (No Remnant P-Type GaN Island)

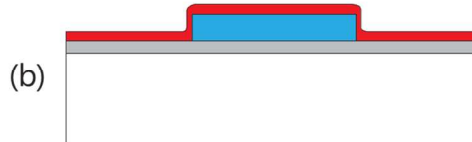
Legend	
	Resist
	p-GaN
	AlGaN Barrier
	Dielectric
	GaN Buffer
	Gate Metal
	Ohmic Metal*

* Source/Drain Contacts

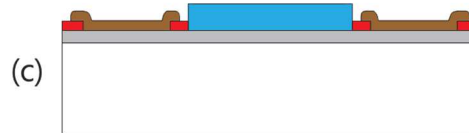
- 1) Epitaxy Grown - buffer/barrier/p-GaN
- 2) Resist Applied



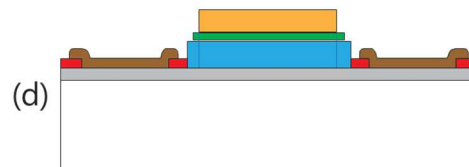
- 3) p-GaN Layer Etched
- 4) Dielectric Layer Deposited (D)



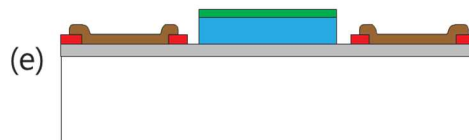
- 5) Windows Opened in Dielectric for Contacts
- 6) Ohmic Contact Metal Applied, Patterned, Annealed (O)



- 7) Patterned Gate Contact (G) Metal Applied
- 8) Gate Resist Applied



- 9) Self Aligned Etch of Gate Metal and p-GaN (G)
- 10) Strip Resist



D (dielectric), O (ohmic contact), G (gate) process (no remnant p-type GaN Island)

2. Second Example: O (ohmic contact), G (gate), D (dielectric) process

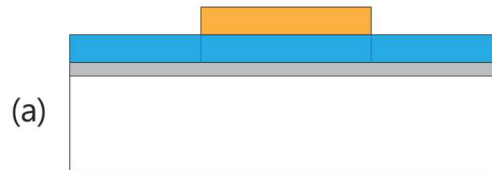
35. As I explained in my deposition, the '508 patent claims cover an “O (ohmic contact), G (gate), D (dielectric)” process shown in the diagram below. First, epitaxial layers and p-GaN layer are grown on the substrate, and a photoresist is applied over the p-GaN layer, shown in Figure (a) of the diagram below. Next, the p-GaN layer is etched, and ohmic contacts are formed on the barrier layer, shown in Figure (b). Then, patterned gate contact metal is applied on the p-GaN, and a photoresist is applied on the gate metal, shown in Figure (c). Finally, a self-aligned gate is formed using the photoresist, the photoresist is removed, a dielectric layer is deposited, and windows are opened in the dielectric layer for gate and ohmic contacts, shown in Figure (d).

OGD Process Order

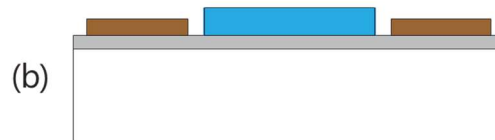
Legend	
	Resist
	p-type GaN
	AlGaN Barrier
	Dielectric
	GaN Buffer
	Gate Metal
	Ohmic Metal*

* Source/Drain Contacts

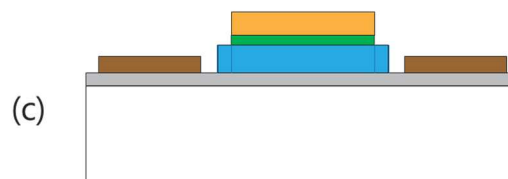
- 1) Epitaxy Grown - Buffer/Barrier/p-GaN
- 2) Resist Applied



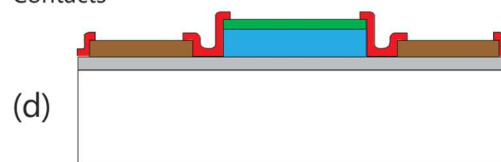
- 3) p-GaN Layer Etched
- 4) Ohmic Contact Metal Applied, Patterned, Annealed (O)



- 5) Patterned Gate Contact Metal Applied
- 6) Gate Resist Applied



- 7) Self Aligned Etch of Gate Metal and p-GaN (G)
- 8) Strip Resist
- 9) Deposit Dielectric (D)
- 10) Windows Opened in Dielectric for Gate and Source/Drain Ohmic Contacts



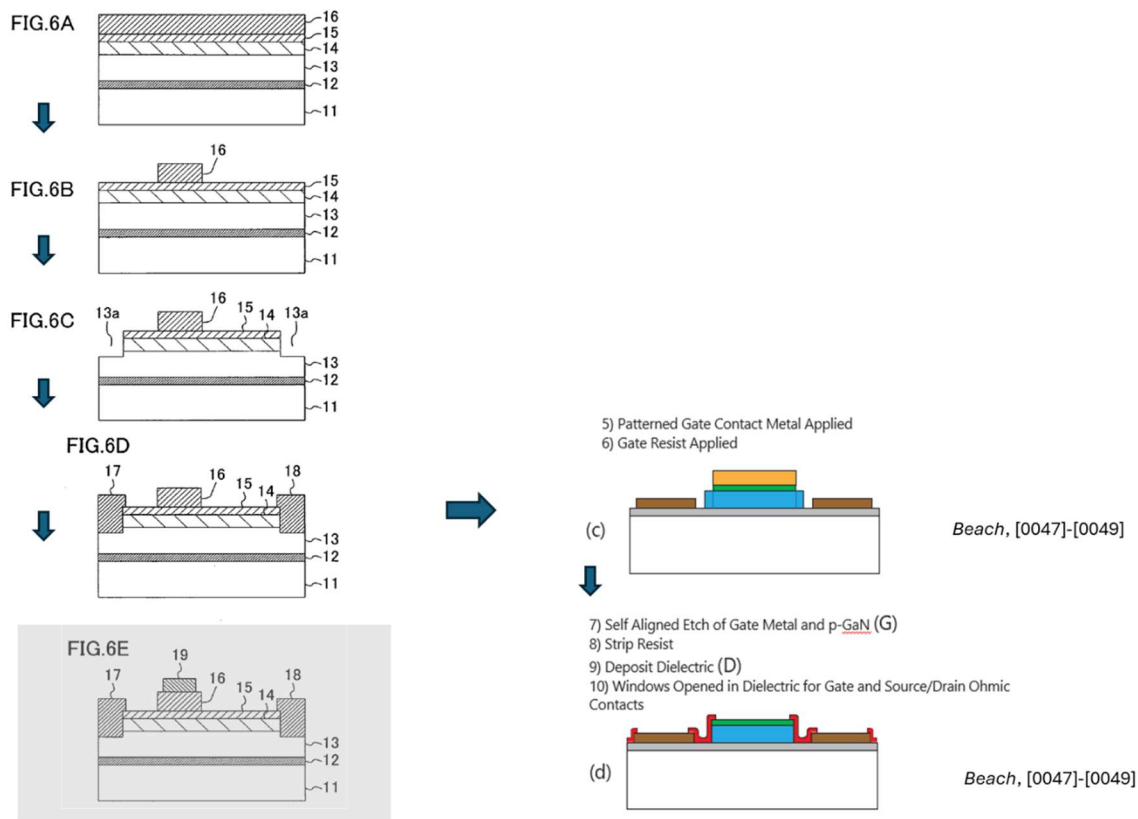
O (ohmic contact), G (gate), D (dielectric) process

36. My research group at Cornell used an O (ohmic contact), G (gate), D (dielectric) process to form GaN transistors in early 2000 when I led the GaN

research at Cornell. *See Kim*, 1 (describing an O, G, D process for GaN transistor device fabrication); *Green*, 1 (same); *Kaper*, 1 (same). The O (ohmic contact), G (gate), D (dielectric) process was commonly used to form GaN transistors that worked for the intended purpose. The OGD process we used at Cornell produced state of art GaN HEMT devices. *See Wang*, 1-2 (using an O, G, D process to produce “[h]igh-performance AlGaIn-GaN HEMTs”); *Suh*, Fig. 18, [0072]-[0080] (using an O, G, D process to produce an enhancement mode GaN transistor with a self-aligned gate structure). A POSITA would have understood that the above O (ohmic contact), G (gate), D (dielectric) process produces an operational GaN transistor and provides certain benefits, such as protecting the gate from the anneal process, as I explained in my deposition.

37. I understand that the Board found in the Institution Decision that the steps of forming the dielectric layer must be performed before the ohmic contact formation. As I explained above, the dielectric formation steps may occur after the ohmic contact formation, where the source and drain contact area is opened in Figure (d) after the formation of source and drain contacts in Figure (b). And during my tenure at Cornell, my research group built many state-of-art GaN transistors using an “O (ohmic contact), G (gate), D (dielectric)” process, where the dielectric layer is formed after the formation of ohmic contacts.

38. *Hikita-023* teaches such an O, G, D process. For example, *Hikita-023* teaches the step sequence of etching the p-GaN layer, forming a gate, forming ohmic contacts, and depositing a dielectric layer. See *Hikita-023*, Figs. 6A-6E, [0076]-[0080], [0089] (using an O, G, D process to produce a GaN transistor). To incorporate a self-aligned gate as taught in *Beach*, a POSITA would have modified Figure 6E of *Hikita-023* to implement steps (c) and (d) of the O, G, D process diagram I provided above. As I explained in my initial declaration, a POSITA would have been motivated and expected success in such modifications.



Modified *Hikita-023* Process

39. I understand that Dr. Schubert argues that the O, G, D process is non-functional. Ex. 2001, ¶ 96. I disagree. There are many examples of functional OGD process in the literature I referred to above. *See Kim*, 1 (describing an O, G, D process for GaN transistor device fabrication); *Green*, 1 (same); *Kaper*, 1 (same). As I explained above, the O, G, D process was commonly used to produce an enhancement mode GaN transistor. Further, Dr. Schubert's arguments are technically incorrect for several reasons. Dr. Schubert argues that the gate metal etch according to the photoresist pattern will remove the source and drain contact. But it was well known that the gate metal and ohmic contacts are typically made by different metal materials, and with proper selection of the etching chemistry, the etching of gate metal would not harm the source and drain ohmic contacts. For example, *Hikita-347* describes a gate electrode formed of Pd, and source and drain contacts formed of a Ti layer and an Al layer. *Hikita-347*, [0060]-[0061]. *Yoshida* describes using metal Al for source and drain electrodes and Au for gate electrode. *Yoshida*, [0022]. By selecting proper chemistry, the etching of the gate would not have an impact on the ohmic contacts previously formed on the barrier layer. *See Harvard*, 1 (using different etching chemistries for forming ohmic source and drain contacts and gate contact); *see generally Walker* (describing different etching chemistry for different metals, e.g., Aluminum (Al), Gold (Au), Palladium (Pd), Titanium (Ti), etc.). Moreover, the etching of gate metal would not partially

remove the barrier layer. The barrier layer is not composed of metal material, and the chemistry used to etch the gate metal will have no effect on the barrier layer. *See Hikita-347*, [0033] (teaching an undoped AlGa_N barrier layer); *Yoshida*, [0014] (teaching an n-type AlGa_N barrier layer). Further, the partial removal of the barrier layer would not make the device nonfunctional. In fact, the '508 patent itself teaches removing part of the barrier layer during the gate formation process. Ex. 1001, 3:52-54 ("The gate layer 15 can also be over-etched, removing about 0 to about 3 nm of the barrier layer 14 outside of the gate region").

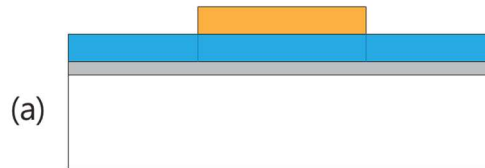
40. In any event, if there is a concern of damaging the ohmic contacts during the gate etching, a photoresist layer could be placed on the ohmic contacts during the gate etching to protect the ohmic contacts beneath the photoresist, as shown in the diagram below. The step can be performed in step (c) of the O-G-D process while the photoresist is placed on the gate metal. The photoresist can be placed on the ohmic contacts at the same time when the photoresist on the gate metal is placed and protects the ohmic contacts from the etching of the gate metal. The photoresist on the ohmic contacts would be removed in step (d) of the O-G-D process, along with the removal of the gate photoresist. Applying a photoresist layer on the ohmic contacts would be a trivial step for a POSITA to add in this O-G-D process.

OGD Process Order (Photoresist Applied on Ohmic Contacts)

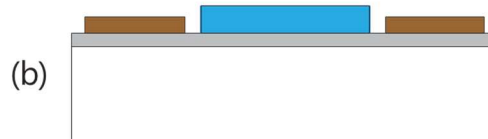
Legend	
	Resist
	p-type GaN
	AlGaN Barrier
	Dielectric
	GaN Buffer
	Gate Metal
	Ohmic Metal*

* Source/Drain Contacts

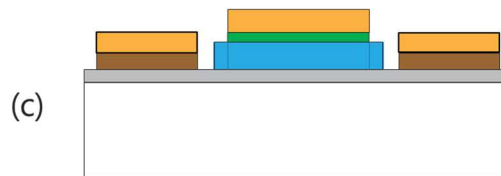
- 1) Epitaxy Grown - Buffer/Barrier/p-GaN
- 2) Resist Applied



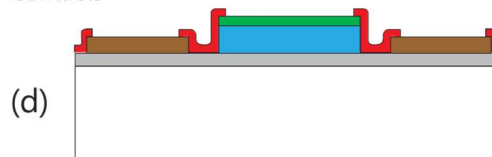
- 3) p-GaN Layer Etched
- 4) Ohmic Contact Metal Applied, Patterned, Annealed (O)



- 5) Patterned Gate Contact Metal Applied
- 6) Gate Resist Applied



- 7) Self Aligned Etch of Gate Metal and p-GaN (G)
- 8) Strip Resist
- 9) Deposit Dielectric (D)
- 10) Windows Opened in Dielectric for Gate and Source/Drain Ohmic Contacts



O (ohmic contact), G (gate), D (dielectric) process (applying ohmic photoresist)

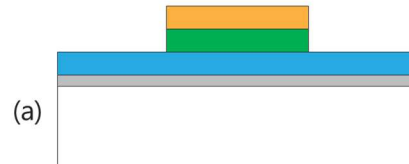
D. A POSITA Would Have Found a Gate-First Process Obvious

41. Even though the '508 patent claims do not require a gate-first process, such a process would be obvious to a POSITA. As I explained in my deposition, the G (gate), D (dielectric), O (ohmic contact) process includes the following steps. First, epitaxial layers and p-GaN layer are grown on the substrate, gate metal is deposited on the p-GaN layer, a photoresist is applied on the gate metal, and gate metal is etched, as shown in Figure (a) of the diagram below. Next, the p-GaN layer is etched, and the photoresist is removed, shown in Figure (b). Then, a dielectric layer is deposited on the surface, shown in Figure (c). Then, windows are opened in the dielectric layer for ohmic contacts, and ohmic contacts are formed in the openings, shown in Figure (d). Finally, windows are opened in the dielectric layer, exposing the gate contact.

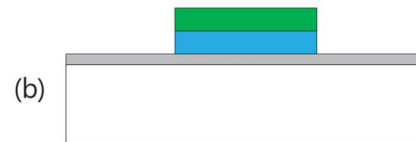
GDO Process Order



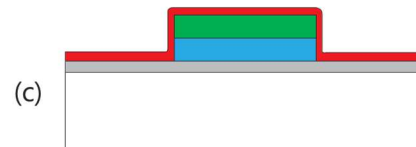
- 1) Epitaxy (E) Grown - Buffer / Barrier / p-GaN
- 2) Deposit Gate Metal
- 3) Deposit Photo Resist
- 4) Pattern Resist - Etch Gate Metal



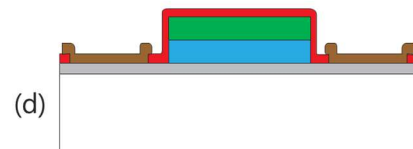
- 5) Continue Etching p-GaN Layer - Self aligned Gate Stack (G)
- 6) Remove Resist



- 7) Deposit Dielectric (D)



- 8) Windows Opened in Dielectric for Ohmic Contacts
- 9) Ohmic Contact Metal Applied, Patterned, Annealed (O)



- 10) Windows Opened in Dielectric Exposing Gate Contact (not shown)

G (gate), D (dielectric), O (ohmic contact) process

42. As I explained in my deposition, each of the D-O-G, O-G-D, and G-D-O process has its advantages and disadvantages. A POSITA would have selected a gate-first G-D-O process based on the design needs of the specific application. For example, a POSITA would have been motivated to use a gate-first G-D-O process to self-align the ohmic source and drain contacts to the gate contact, so as to reduce the minimum source-to-gate distance and reduce the source and drain access resistance.

43. As I explained in my deposition, there are only six permutations of ordering in forming a gate contact, ohmic contacts, and dielectric layer, all of which are suitable options. Each of the permutations would have been obvious to a POSITA. And a POSITA would have found it obvious to try a gate-first G-D-O process and expected success to do so.

VII. RESPONSE TO EPC'S ARGUMENTS REGARDING OHMIC FORMATION

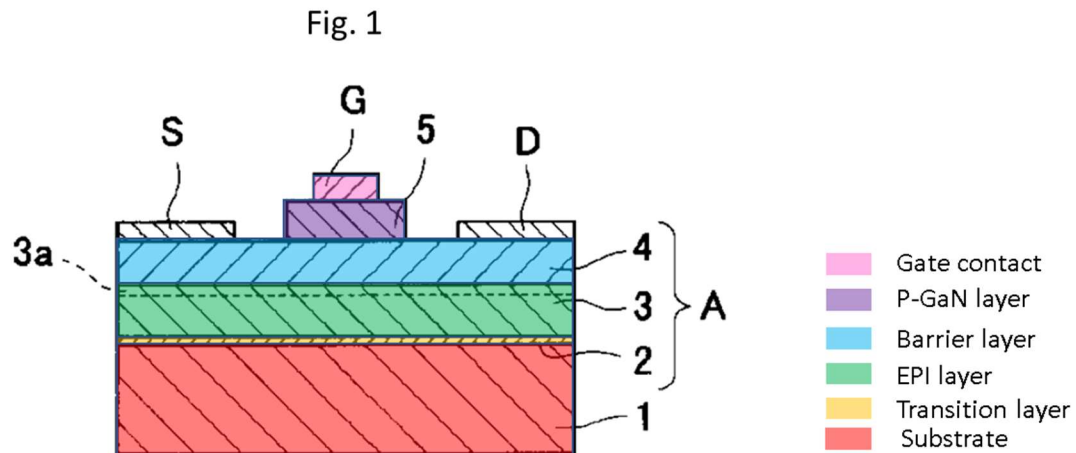
44. EPC argues in its POR that *Yoshida*, *Hikita-347*, and *Hikita-023* each disclose a lift-off process to form the ohmic contacts and that a POSITA would not have been motivated to replace the lift-off process with the etching process. I disagree.

A. *Yoshida* Does Not Describe a Lift-off Process and a POSITA Would Have Been Motivated to Form *Yoshida*'s Ohmic Contacts Using *Beach*'s Etching Process

45. On pages 43-47 of its POR, EPC alleges that *Yoshida* describes a lift-off process to form the ohmic contacts and that a POSITA would not have been motivated to replace the lift-off process with the etching process. I disagree.

46. *Yoshida* is silent as to which process to use for ohmic formation. *See Yoshida*, [0022] (“metal Al deposited on the exposed n-type InGaN layer 4 to load source electrode S and drain electrode D”). A POSITA would have understood that *Yoshida*'s ohmic contacts may be formed by an etching process similar to *Beach* and would have been motivated to use *Beach*'s etching process to form *Yoshida*'s ohmic contacts.

47. Dr. Schubert argues that *Yoshida* describes a lift-off process for ohmic formation because Figure 1 of *Yoshida* shows “ohmic contacts having vertical sidewalls entirely aligned with the etched dielectric material.” Ex. 2001, ¶¶ 157-160.



48. Figure 1 of *Yoshida* does not show any dielectric layer. It is unclear how Dr. Schubert concludes that the ohmic contacts of *Yoshida* have vertical sidewalls entirely aligned with the etched dielectric material based on illustration of Figure 1.

49. Dr. Schubert argues that a lift-off process produces ohmic contacts with sidewalls aligned with the edges of the dielectric layer, but not a metal etching process. This is incorrect. Whether the vertical sidewalls of ohmic contacts are aligned with the dielectric material does not indicate a lift-off or an etching process. In fact, metal etching is more precise than the lift-off process and can be used to produce aligned sidewalls.

50. To minimize the undesired residual metal in the lift-off process, a negative (non-vertical) profile of photoresist is typically used for lift-off, as shown in the left side of *Gorowitz*, Figure 1 below. See also *Collins*, 2 (describing an

overhang lift-off structure in which “the top of the resist line larger than the bottom”), Fig. 1 (showing a lift-off structure having a non-vertical profile). The negative profile of photoresist results in a sloped side wall of the remaining metal, which is different from the vertical sidewalls of the ohmic contacts in *Yoshida*.

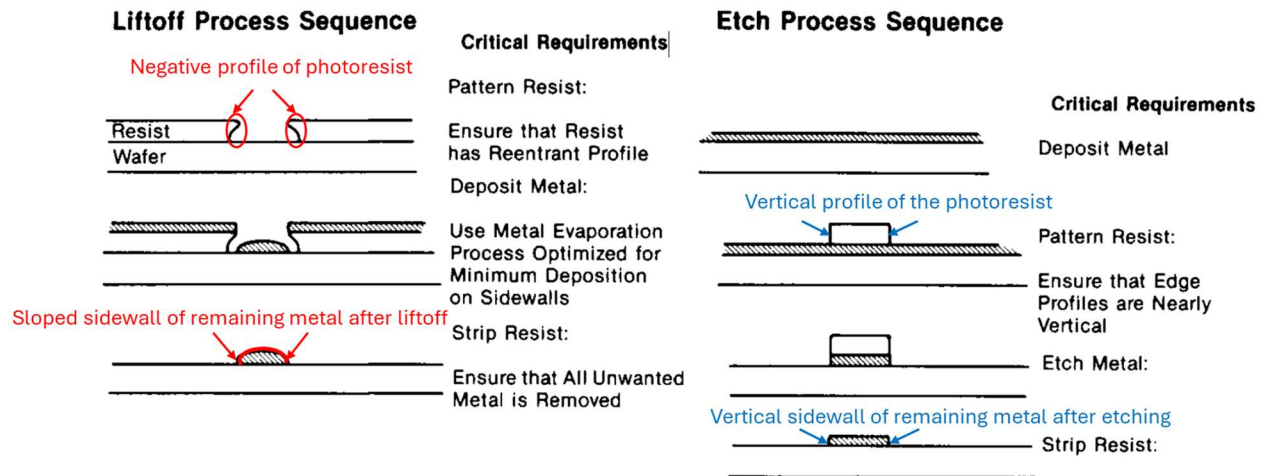
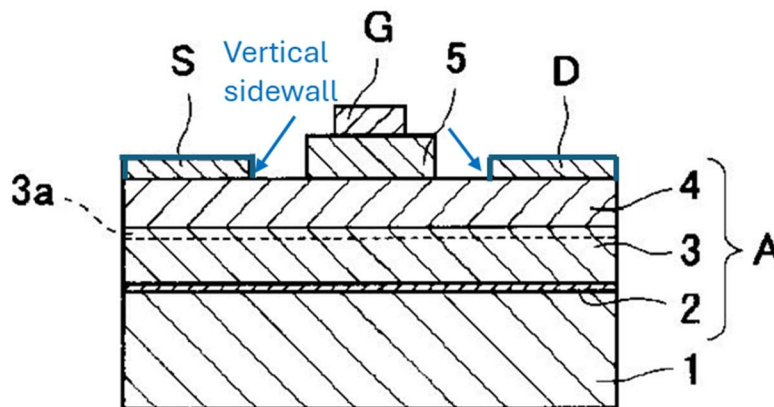


Fig. 1. Comparison of additive (liftoff) and subtractive (etch) metallization patterning processes.

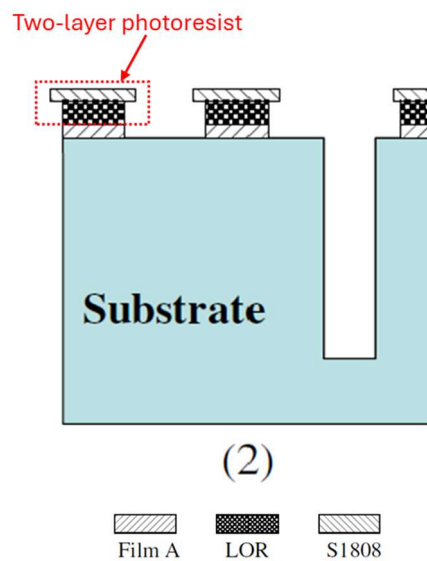
Gorowitz, Fig. 1 (annotated)



Yoshida, Fig. 1 (annotated)

51. The right side of *Gorowitz*, Figure 1 shows an etching process. And as shown, a vertical photoresist profile is used for the etching process, resulting in vertical sidewalls of the metal material after the etching process. The etching process produces vertical sidewalls of metal material, like the vertical sidewalls of ohmic contacts in *Yoshida*.

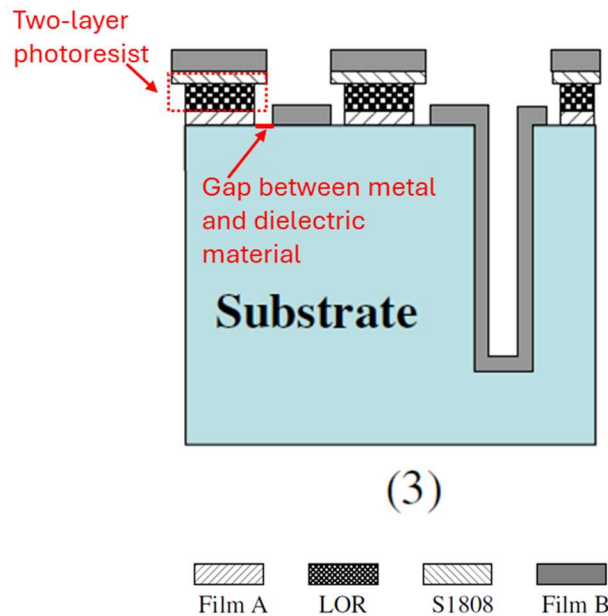
52. Another type of photoresist commonly used in lift-off process is the multi-layer photoresist, consisting of a top layer of wider photoresist and a lower layer of narrower photoresist, as shown in Figure 1-(2) of *Liang* below.



Liang, Fig. 1-(2) (annotated)

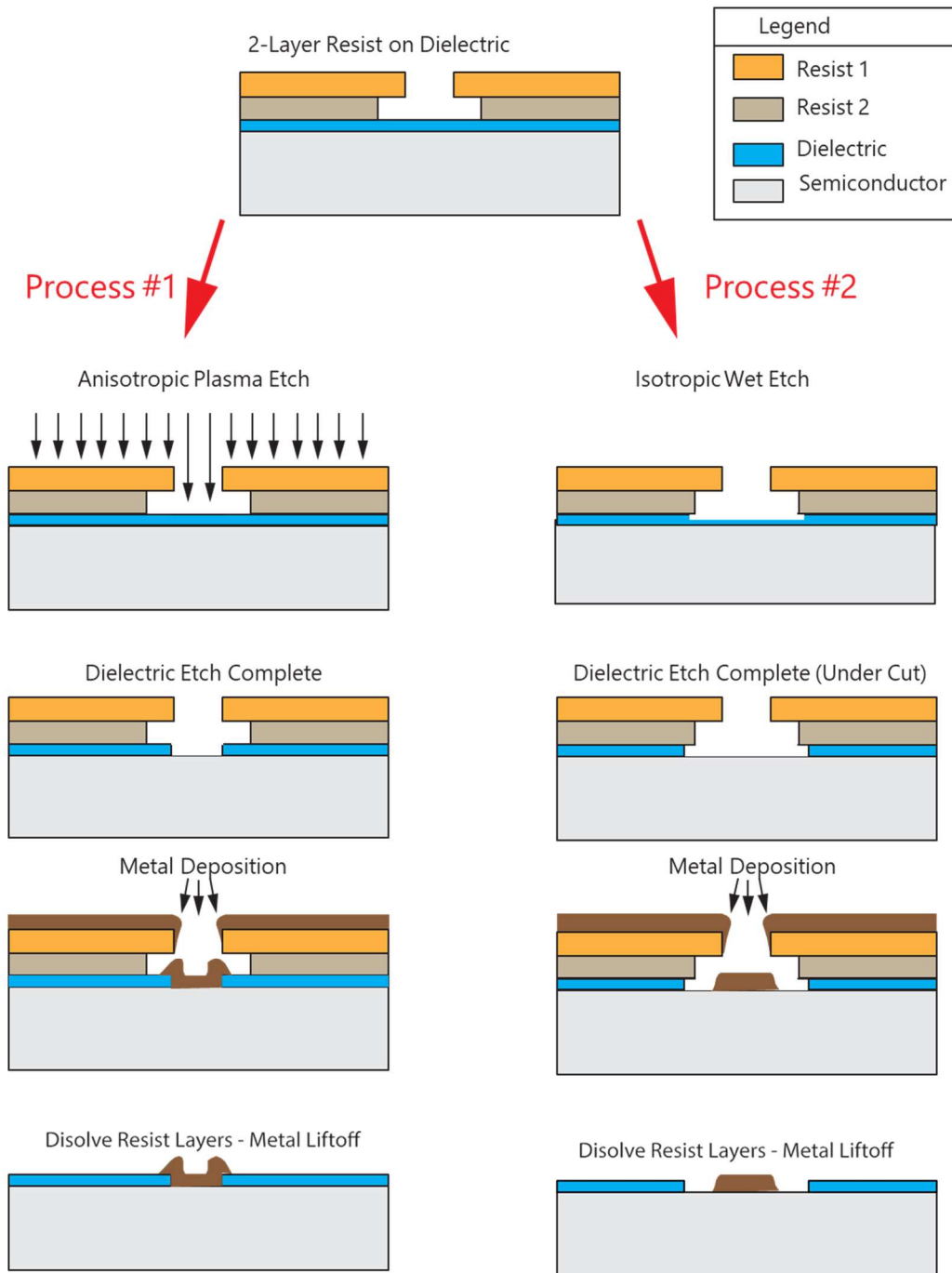
See also *Liang*, 2 (describing a layer of lift-off resist LOR is put underneath of a layer of photoresist S1808).

53. The multi-layer photoresist used in the lift-off process results in a gap between the metal and the dielectric layer (film A), as shown in Figure 1-(3) of *Liang*.



Liang, Fig. 1-(3) (annotated)

54. The multi-layer photoresist used in the lift-off process produces non-aligned metal and dielectric layer, as shown in the schematic representations I provide below. When the dielectric layer is etched by plasma etching, an overlapping between the metal and dielectric layer would occur, shown in the left side of the diagram. When the dielectric layer is etched by wet etching, a gap between the metal and dielectric layer would occur, shown in the right side of the diagram. In either case, the sidewall of the metal is not aligned with the edge of the dielectric layer, unlike the structure shown in *Yoshida*.



Metal Lift-off Using a Double Layer Photo Resist

55. Thus, it is more difficult to align the sidewalls of ohmic contacts with the edge of dielectric layer using the lift-off process compared to the metal etching because the metal edge is never aligned with any feature in the lift-off process. *See*

Gorowitz, 23 (“The most accurate and controllable methods of replicating the dimensions of the resist pattern involve the use of anisotropic plasma etching”). A POSITA would have understood that *Yoshida*’s ohmic contacts having vertical sidewalls are more likely achieved by an etching process as taught by *Beach*.

56. Dr. Schubert also argues that the lift-off process is preferable to the etching process. I disagree. As I explained in my previous declaration and in my deposition, the lift-off process leaves unwanted metal layer remaining and does not provide the same level of precision as the metal etching process. *See Gorowitz*, 4 (“Subtractive (etching) processes are more typically used”), 23 (“The most accurate and controllable methods of replicating the dimensions of the resist pattern involve the use of anisotropic plasma etching”). The lift-off process is expensive because it requires precise processing of a photoresist to achieve a negative profile. The lift-off process is generally avoided in manufacturing because the complex processing of the photoresist may result in more variations in the metal dimensions. Further, as I explained in my previous declaration, lift-off and metal etching are the only two prevalent techniques for metal patterning. *Yoshida* does not suggest that performing an etching process or lift-off was critical to its method to form a GaN transistor. *Beach*’s etching technique provides performance benefits over lift-off, e.g., more accurate and controllable to pattern the metal. Using a metal etching process to form the ohmic contacts, as taught by *Beach*,

would be an obvious design choice to form the ohmic contacts of *Yoshida*. See *Gorowitz*, 4 (“When resist patterns are used to define metal layers, the process can be either additive [lift-off] or subtractive [etching].”).

57. EPC argues on page 47 of its POR that I used lift-off process for gate formation in my patents. But these patents are not concerned with comparing metal lift-off with metal etching, and the lift-off process is used as an example of forming metal structures. U.S. Patent No. 6,478,871 describes using lift-off to form an AlGaN nucleation layer 14. See Ex. 2004, 3:16-24, 4:7-15, Fig. 2. The lift-off described in the '871 patent does not relate to metal etching at all.

58. U.S. Patent No. 9,991,360 describes using lift-off to form ohmic contacts, gate, and ohmic contact pads. See Ex. 2005, 7:64-67, 11:27-41, Figs. 5K, 5L, 5N, 5P. The '360 patent confirms my explanations above regarding a multi-layer photoresist used for a lift-off process and similarly shows sidewalls of metal structure not aligned with the edges of dielectric layer after the lift-off process. For example, the '360 patent describes a double layer photoresist consisting of an underlayer 515 and an overlayer 516 to form ohmic contacts in a lift-off process, where the underlayer 515 has a non-vertical profile. Ex. 2005, 11:10-14. The '360 patent also describes a double layer photoresist consisting of an underlayer 519 and an overlayer 520 to form gate metal 521 in a lift-off process, where the underlayer 519 has a non-vertical profile. Ex. 2005, 11:22-26. Figure 5O of the '360 patent

shows gate metal 521 having non-vertical side walls and overlapping with dielectric layer 507 after a lift-off process. Ex. 2005, Fig. 5O. The '360 patent further describes forming source and drain contact pads 522 using a lift-off process and shows source and drain contact pads 522 having non-vertical side walls and overlapping with dielectric layer 507 after the lift-off process. Ex. 2005, 11:34-39, Fig. 5P.

B. *Hikita-347* Does Not Describe a Lift-off Process and a POSITA Would Have Been Motivated to Form *Hikita-347*'s Ohmic Contacts Using *Beach*'s Etching Process

59. At pages 56 through 58 of its POR, EPC similarly argues that *Hikita-347* discloses a lift-off process to form the ohmic contacts and that a POSITA would not have been motivated to replace the lift-off process with the etching process. I disagree.

60. Like *Yoshida*, *Hikita-347* is silent as to which process to use for ohmic formation. *See Hikita-347*, [0060] ("Each of a source electrode 490 and a drain electrode 410 is formed of a Ti layer and an Al layer in an associated one of the openings, and then heat treatment is performed thereto in an N₂ atmosphere at 650° C."). Nor does the drawing of *Hikita-347* show any lift-off process for ohmic formation. As I explained above, the precise alignment between the sidewalls of the ohmic contact and dielectric material is better achieved by an etching process compared to a lift-off process. A POSITA would have understood

that *Hikita-347*'s ohmic contacts having vertical sidewalls are likely achieved by an etching process as taught by *Beach*.

61. As I explained above, the metal etching process, as described in *Beach*, is a preferable process for providing alignment between the ohmic contact sidewalls with the edges of the dielectric layer. The lift-off process can be expensive and is generally avoided in manufacturing. Regardless of whether *Hikita-347* teaches a lift-off technique, a POSITA would have been motivated to use *Beach*'s etching process to form *Hikita-347*'s ohmic contacts instead of lift-off.

C. A POSITA Would Have Been Motivated to Form *Hikita-023*'s Ohmic Contacts Using *Beach*'s Etching Process

62. At pages 64 through 65 of its POR, EPC similarly argues that *Hikita-023* discloses a lift-off process to form the ohmic contacts and that a POSITA would not have been motivated to replace the lift-off process with the etching process. I disagree.

63. As I explained above, the metal etching process, as taught in *Beach*, is a preferable process to lift-off in manufacturing. Metal etching also provides better controllability and precision to align the ohmic contact sidewalls with the edges of the dielectric layer. *Hikita-023* does not suggest that performing a lift-off was critical to its method to form a GaN transistor, and variations of such was a matter of design choice. *Hikita-023*, [0079]. For the reasons I explained above and in my

initial declaration, a POSITA would have been motivated to use *Beach*'s etching process to form *Hikita-023*'s ohmic contacts and expected success in doing so.

VIII. CONCLUSION

64. In signing this declaration, I understand that the declaration will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I acknowledge that I may be subject to cross-examination in this case and that cross-examination will take place within the United States. If cross-examination is required of me, I will appear for cross-examination within the United States during the time allotted for cross-examination.

65. I declare that all statements made herein of my knowledge are true, and that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Date: September 2, 2024


James Richard Shealy, Ph.D.