

Improved Fabrication Process for Obtaining High Power Density AlGaIn/GaN HEMTs

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Abstract

An improved process for fabricating high power density AlGaIn/GaN HEMTs is now presented. Previously, a silicon nitride passivation layer has been shown to improve the power performance of AlGaIn/GaN HEMTs by minimizing surface related dispersion effects. Typically, this passivation layer has been deposited during the final stages of the fabrication process, with the device active area exposed to various potentially harmful plasmas and chemical treatments. In the new process, a high quality silicon nitride layer is deposited early in the fabrication process, serving to both protect the AlGaIn surface from damage and to minimize dispersion related phenomena. In addition, the silicon nitride layer provides an opportunity for forming well defined field-plated gate structures. 0.6 μm x 150 μm gate devices built with this process have demonstrated state-of-the-art CW output power and power added efficiency of >15.6 W/mm and 44% respectively at 10 GHz, when operated at 60 V drain voltage.

INTRODUCTION

A primary limiting factor to obtaining high power densities in AlGaIn/GaN High Electron Mobility Transistors (HEMTs) has been current slump and current collapse phenomena, typically attributed to dislocations and surface states [1-3]. Both phenomena can severely impact the device performance, reducing the output power densities that can be achieved. The use of a silicon nitride passivation layer has previously been shown to reduce these dispersion effects, sometimes dramatically improving the device power performance to reach state-of-the-art levels of 11.7 W/mm or more at 10 GHz for small gate periphery devices [4-6]. Typically, this silicon nitride layer is applied after ohmic and Schottky gate contacts have been formed, with the exposed AlGaIn surface having been subjected to various potentially damaging plasma and chemical treatments before being passivated. Such damage to the surface can be avoided by depositing a silicon nitride passivation layer earlier during device fabrication, while still obtaining the improvement in device power performance. In [7], a MISFET process for AlGaIn/GaN on Sapphire was presented in which silicon nitride was deposited after mesa isolation, and prior to any contact formation or annealing steps, resulting in devices with excellent performance and uniformity. We now present a modified version of this

process designed to fabricate HEMTs, in which the gate is a metal-semiconductor contact, rather than MISFETs. The resulting 0.6 μm x 150 μm gate devices are able to operate at 60 V drain voltage, with a state-of-the-art CW output power density and power added efficiency of >15.6 W/mm and 44 % respectively at 10 GHz, as shown in Figure 1.

PROCESS DESCRIPTION

Similar to the MISFET process described in [6], device fabrication primarily consists of depositing a high quality silicon nitride film very early in the process, and then etching windows through the passivation layer before depositing metals. First, a mesa isolation is formed by using a Cl_2 -based ECR etch. Next, a high quality silicon nitride layer is deposited to protect the surface, optimized to withstand ohmic metal annealing temperatures in addition to minimizing the surface related dispersion. Photo-lithography is then used to define the regions where Ti/Al/Ti/Au ohmic contacts will be formed. Just prior to ohmic metal evaporation, a CF_4 -based RIE etch is used to open a window through the silicon nitride layer, followed by a 30 sec. wet chemical buffered oxide etch. The CF_4 plasma can etch the AlGaIn barrier layer in addition to the silicon nitride, leaving a damaged surface that can aid in improving ohmic contact formation. For the Schottky gate contact, electron-beam lithography is used to define the footprint for the gate structure, with a CF_4 -based RIE etch used to define a window through the silicon nitride. Once this gate window has been opened, a 45 sec. 850° C rapid thermal anneal is used to form ohmic contacts and to anneal surface damage in the opened gate windows. Photolithography or electron-beam lithography can then be used to define the region for Ni/Au Schottky gate metallization. The use of etch windows for defining the gate also provides an opportunity for metallizing T-shaped gates with precisely defined gate lengths and stem heights, as well as source-to-gate spacing 0.7 μm or smaller due to improved contact edges. By extending the length of the drain side gate overhang, a field-plated gate structure can be formed to improve the device breakdown characteristics [8].

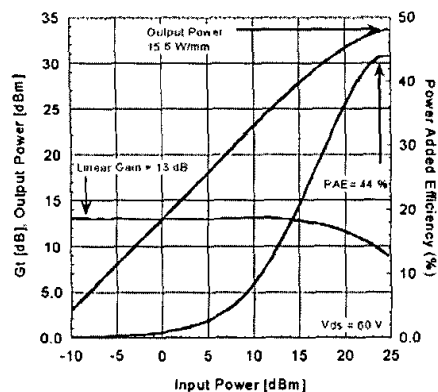


Figure 1. Power sweep of 0.6 μm x 150 μm gate HEMT showing state-of-the-art CW power performance when operated at 60 V drain-source voltage.

DEVICE FABRICATION

By utilizing this process, small periphery 0.6 μm x 150 μm gate devices have been produced on a GaN-capped Al-GaN/AlN/GaN HEMT structure. The un-doped HEMT structure was grown on a SiC substrate with organometallic vapor phase epitaxy. Following a thin AlGaN nucleation layer, a 300 nm AlN sub-buffer was grown [6], and then a 1 μm GaN buffer. A composite barrier was then deposited, consisting of a 1.5 nm AlN interlayer, an 11 nm Al_{0.35}Ga_{0.65}N barrier, and finally a 2 nm GaN cap. The AlN interlayer serves to improve electron mobility at the hetero-interface by reducing alloy related scattering, and to enhance the sheet charge density [9]. The GaN cap is used to reduce gate leakage by raising the barrier height [10], in addition to partially depleting electrons from the channel. From C-V measurements the sheet charge density at +0.4 V gate bias was found to be $1.7 \times 10^{13} / \text{cm}^2$ [11]. The passivation thickness used was 40 nm. When fabricated, the devices had a source-to-gate and source-to-drain spacing of 0.69 μm and 2.31 μm respectively. From TLM measurements, the ohmic contacts had a transfer resistance of 0.6 Ω-mm, with a sheet resistance of 280 Ω/sqr. The gate structure, shown in Figure 2, had a relatively small 0.12 μm metal overhang on the drain side, 40 nm away from the surface due to the silicon nitride passivation layer thickness. Although the gate structure forms a field-plated gate, it has not been optimized to improve the breakdown voltage of the devices.

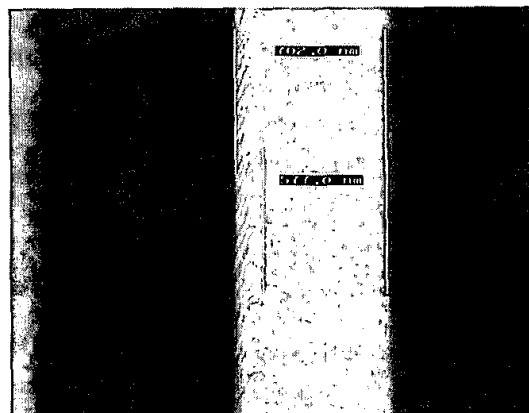


Figure 2. SEM of 0.6 μm x 150 μm gate HEMT showing gate length and overhang length of 0.58 μm and 0.12 μm respectively.

MEASUREMENTS

Once the device fabrication was complete, the devices were then characterized on-wafer using coplanar wave guide probes. Measurements included DC, small signal, and CW 10 GHz load-pull using a Maury™ system. The substrate was in physical contact with a room temperature copper chuck during the measurements, without the use of any backside metal.

The typical device has maximum transconductance of 300 mS/mm and a pinch-off voltage of -2.1 V. The maximum drain current was 1.3 A/mm with +4 V on the gate, when the gate had 1 mA/mm of forward current. The gate leakage current at pinch-off condition was less than 20 μA/mm at 15 V drain voltage. From small signal measurements at the peak g_m point, the f_T and f_{max} were found to be 19.2 GHz and 42.2 GHz respectively.

For large signal testing at 10 GHz, the devices were impedance matched for peak power at 40 V drain bias, and operated in class AB regime. Power sweeps were then performed at varying drain bias from 15 to 60 V in steps of 5 V without changing the matching conditions or gate bias. The output power and PAE at 4 dB gain compression is plotted as a function of drain voltage, shown in Fig 3. At 60 V drain bias, the devices demonstrated a CW output power density of 15.6 W/mm and power added efficiency of 44 %, at 4 dB gain compression. This represents a state-of-the-art power density for an AlGaN/GaN HEMT with a 0.6 μm gate length. The linear transducer gain was 13 dB.

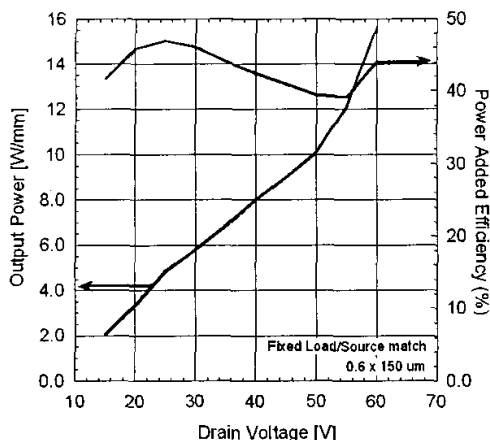


Figure 3. Output power and PAE at 4 dB gain compression at varying drain voltage. Load and Source were matched for maximum output power at 40 V.

CONCLUSION

This report presented an improved fabrication process for obtaining AlGaIn/GaN HEMTs that can operate at 60 volts drain bias and demonstrate state-of-the-art power performance. This new process takes advantage of the passivation and performance enhancing properties of high quality silicon nitride films when deposited on the AlGaIn/GaN HEMT surface. By passivating the surface after mesa isolation, and prior to any metal evaporation steps, the surface of the device active area remains protected throughout the fabrication process. In addition, by controlling the thickness of the silicon nitride film and the metal overhang length on the drain side of the gate structure, a field-plated gate can be formed to increase the breakdown voltage of the device. Using this process, small periphery $0.6 \mu\text{m} \times 150 \mu\text{m}$ gate devices have been produced which can operate at 60 V drain voltage and demonstrate state-of-the-art CW output power densities of $>15.6 \text{ W/mm}$ with a PAE of 44 %.

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