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VLSI Metallization

Volume Editors
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Chapter 4

Methods of Metal Patterning and Etching

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I. INTRODUCTION

In virtually all methods for forming metal interconnect or gate patterns, the starting point is the exposure of a resist material and its subsequent

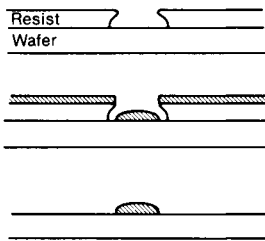
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development to form the patterns to be replicated. The most widespread exposure method involves optical or photolithography, which will be the subject of a major portion of this chapter. Electron beam lithography [1–5], which is largely used for mask fabrication, can also be employed for microcircuit patterning. X-ray lithography is a promising technology that is under development in a number of laboratories [6–10].

When resist patterns are used to define metal layers, the process can be either additive or subtractive. In an additive process (commonly called *liftoff*), a photoresist pattern protects portions of the wafer surface during evaporative deposition of a metal layer. The areas without photoresist allow metal adhesion to the wafer surface. When the photoresist pattern is stripped away using a solvent, the metal adhering to the resist is lifted off leaving behind the completed metallization layer [11]. This is schematically shown in Fig. 1.

Subtractive (etching) processes are more typically used. These consist of the deposition of metal across the entire wafer surface and subsequent patterning of photoresist coated over the metal. The metal layer is then etched away in the unprotected areas forming the metal interconnect pattern. Finally, the photoresist is stripped off the remaining metal pattern. Plasma or reactive ion etching, which will be discussed in detail in Section II, are the primary methods of performing this step when geometries suitable for VLSI applications are involved.

Liftoff Process Sequence



Critical Requirements

Pattern Resist:

Ensure that Resist has Reentrant Profile

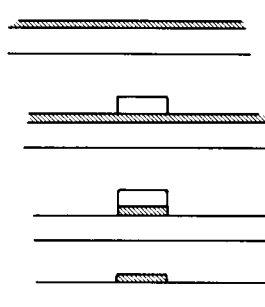
Deposit Metal:

Use Metal Evaporation Process Optimized for Minimum Deposition on Sidewalls

Strip Resist:

Ensure that All Unwanted Metal is Removed

Etch Process Sequence



Critical Requirements

Deposit Metal

Pattern Resist:

Ensure that Edge Profiles are Nearly Vertical

Etch Metal:

Strip Resist:

Fig. 1. Comparison of additive (liftoff) and subtractive (etch) metallization patterning processes.

II. LITHOGRAPHY

A. General Principles

Although the fundamentals of microlithography are discussed elsewhere [12–14], it is instructive to consider those elements that affect the results of the metal patterning process.

The requirements of a photoresist process are (1) a defect free resist pattern, (2) sufficient resist thickness to withstand the subsequent etching process, (3) resist wall profiles of the proper angle for the etch process, (4) linewidth control within a specified tolerance (e.g., $\pm 5\%$ of the mask dimension), and (5) registration to the underlying layer within tolerance (e.g., 0.2 to 0.3 μm).

Table I summarizes the total sequence for forming a resist pattern. In the exposure step, a photomask pattern is placed in precise optical registration with the wafer. The photoresist is exposed by passing UV radiation through the mask, rendering the exposed resist either soluble (positive resist) or insoluble (negative resist) to the developer solution. Some positive resists have the capability of being processed in an image reversal mode, making them functionally equivalent to negative resists [15]. Figure 2 is a comparison of the process sequences required. After development, the photoresist image is thermally cured to improve its adhesion and etch resistance.

B. Defects in Resist Patterns

Inspection of resist images often reveals unwanted pattern defects. These are typically due to missing resist, excess resist, or contamination by

TABLE I
Sequence for Photoresist Pattern Formation

Step	Condition
(1) Prime coat wafer surface with adhesion promoter	Vacuum vapor prime or spin coat hexamethyl disilazane (HMDS) or equivalent
(2) Spin coat photoresist	Thickness range from 0.5 to 2.5 μm
(3) Bake photoresist film	Temperature range from 75 to 130°C
(4) Expose photoresist film	30–350 mJ/cm ²
(5) Develop photoresist	Batch immersion or spray process
(6) Hard-bake photoresist images	Temperature range from 90 to 200°C

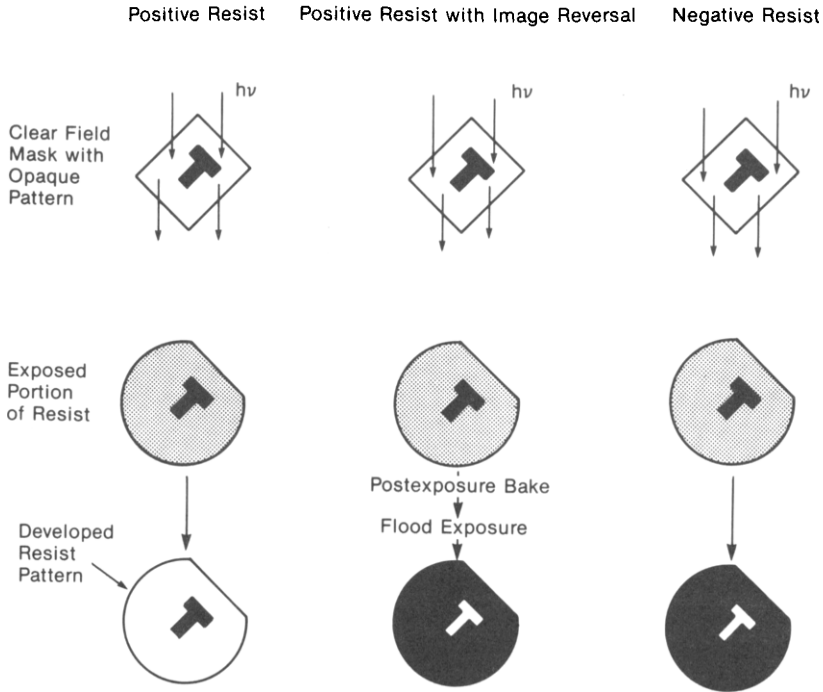


Fig. 2. Comparison of photoresist processing sequences to produce positive and negative tone patterns. With image reversal photoresists standard development results in a positive tone. Postexposure bake followed by a flood exposure prior to development results in a negative tone.

particulates. Missing resist can be caused by poor dehydration of the wafer surfaces, leading to adhesion problems. In the case of severe lack of adhesion, the resist patterns can become detached during development, sometimes coming to rest across adjacent pattern areas. Incomplete wetting of the wafer surface by the resist due to contamination of the wafer or of the resist, can result in pinholes in the resist.

Bridging across resist lines by incompletely exposed and developed photoresist can be a serious problem. This can result from standing waves associated with reflection from metal surfaces, which will be discussed later. Incomplete development of exposed portions of the resist, due to poor wetting by the developer, will also leave resist residues.

One source of contamination is the resist itself. The brittle positive resist film, when subjected to impacts or abrasion, will often flake, sometimes redepositing on the circuit areas. Wafer handling equipment, especially prealign systems that apply pressure to wafer edges, can enhance this

problem. Significant yield losses can be avoided if the resist is removed from the edge of the wafer. This is done with resist processing equipment by directing a stream of solvent to the back of the wafer. When the proper wafer spin speed is used, the solvent wraps around the edge removing the photoresist in a band a few millimeters wide around the periphery of the wafer.

Photoresist solutions have a limited shelf life and can precipitate particles as they age, especially if storage conditions are less than optimum. Particulates that form in solution can be minimized by using only fresh resist materials and properly designed coating equipment. The coating track equipment, especially the resist pump, can be a significant source of contamination. A good design is one that completely displaces the photoresist with each activation. Pumps that allow some of the resist to remain and age should be avoided. Point-of-use filtration systems can also reduce this problem, but attention must be paid to the filter housing since it can retain resist allowing it to age. For consistently low particle count resist coatings, frequent purging and cleaning of all resist handling equipment is required. Particle counts should be monitored regularly on coated test wafers.

C. Alignment Tools

The alignment tools typically employed for VLSI patterning use one of two methods to transfer the mask image to the photoresist. The most predominant method uses a 1X mask pattern that is transferred by reflective optics. Systems using reflective optics are built using the scanning approach. They employ a mask containing an array of die patterns that are transferred to the wafer in one pass after a single global alignment. These systems do not suffer from chromatic aberration and thus are able to use a wide range of illumination wavelengths (250–450 nm). The most commonly used system has a working resolution as low as $\sim 2\ \mu\text{m}$. However, there is a great deal of interest in using upgraded systems in the shorter wavelength range for increased resolution and process latitude [10].

Another alignment tool is the 1X stepper. This system exposes each die, which is a replica of the mask, serially on the wafer, stepping to each die pattern, aligning and exposing it. This reduces the wafer throughput but improves the overall registration by allowing the system to accommodate nonlinear changes in die placement caused by thermal processing of the wafer. A range of exposure wavelengths are used to minimize standing wave reflection problems [16]. These machines have a resolution limit in the 1- to $1.5\text{-}\mu\text{m}$ range. Step and repeat systems generally use only a single

mask pattern rather than an array of patterns. Any particulate contamination that blocks the exposing light will result in a repeating defect on the wafer. In this regard the 1X mask pattern has an advantage since it is easier to clean its smaller area. However, a $1\text{-}\mu\text{m}$ particle on the mask may result in a defect close to that size on the wafer. The mask surfaces are maintained in a clean state by the use of a pellicle [17], which is a shield of transparent film stretched across a frame that is affixed to each face of the mask. Within a range of sizes, particles falling on the pellicle will not be resolved in the resist.

The step-and-repeat method can also be used in the reduction mode. A magnified mask, called a *reticle*, is generally either 5 or 10 times larger than the desired resist pattern. The step-and-repeat aligner uses refractive optics and monochromatic illumination, and is capable of resolving pattern elements as small as $0.5\text{ }\mu\text{m}$. These systems also generally employ pellicles. The primary advantage of the reduction stepper is its greater suitability for high-resolution applications. It has traditionally been used for resolving patterns between 1 and $2\text{ }\mu\text{m}$, meeting pattern registration tolerances of $0.3\text{ }\mu\text{m}$. Recent improvements in optical performance now make it possible to use these systems in the submicron range.

D. Reflectivity

Reflective surfaces are undesirable when imaging VLSI circuit patterns. As light is reflected off the substrate surface, destructive interference causes sinusoidal variations in the intensity within the thickness of the photoresist and consequently similar variations on the edges of the developed patterns

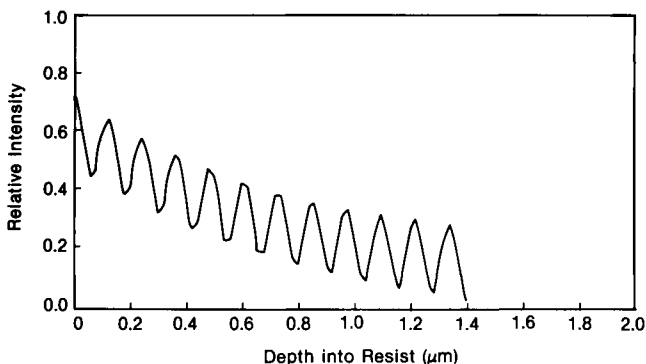


Fig. 3. Simulation of relative intensity versus depth into the photoresist. The sinusoidal variation is caused by standing waves (image formed by projection printing at a wavelength of 405 nm).

[11]. Figure 3 is a simulation of this effect. At the start of exposure, the gradual fall-off in intensity is due to absorption in the photoresist. Standing waves cause the development rate to vary. This is indicated by the staircase pattern superimposed on the curves of thickness versus development time, shown in Fig. 4. It is obvious from the photo in Fig. 5, that standing waves reduce resolution and influence image profiles. In severe cases, the standing wave foot becomes pronounced and causes bridging across nearby pattern elements.

One method of minimizing the standing wave problem is to employ a postexposure bake. This thermal treatment is thought to allow the exposed photoactive compound (PAC) to diffuse slightly, thus providing a more uniform exposure throughout the photoresist thickness (see Fig. 6) [18–20]. The temperature of the postexposure bake process is critical, since heating below the softbake temperature will do little to reduce standing waves, and too high a temperature will cause image profiles to degrade. Generally, postexposure bake processes require a higher initial exposure to maintain an equivalent linewidth.

The occurrence of standing waves can be prevented by the use of a layer of absorbing material under the photoresist. The most commonly used material is a dyed polyimide layer that absorbs well in the 400–450-nm range. This material is soluble in an aqueous base and is removed when the positive photoresist is developed [21–24]. This process requires careful characterization and control of the rate of removal of the antireflective coating since it is undesirable to undercut the photoresist. An alternative method is to bake the antireflective layer at a higher temperature, thus making it insoluble in developer. Once the resist is developed, an oxygen

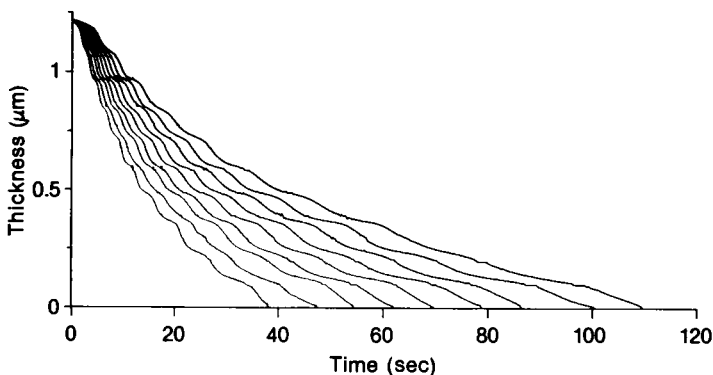


Fig. 4. Change in resist thickness as a function of development time for a series of exposures of decreasing dose. Oscillations in each curve are due to effects of standing waves on exposure. Data were obtained with a Perkin–Elmer development rate monitor.

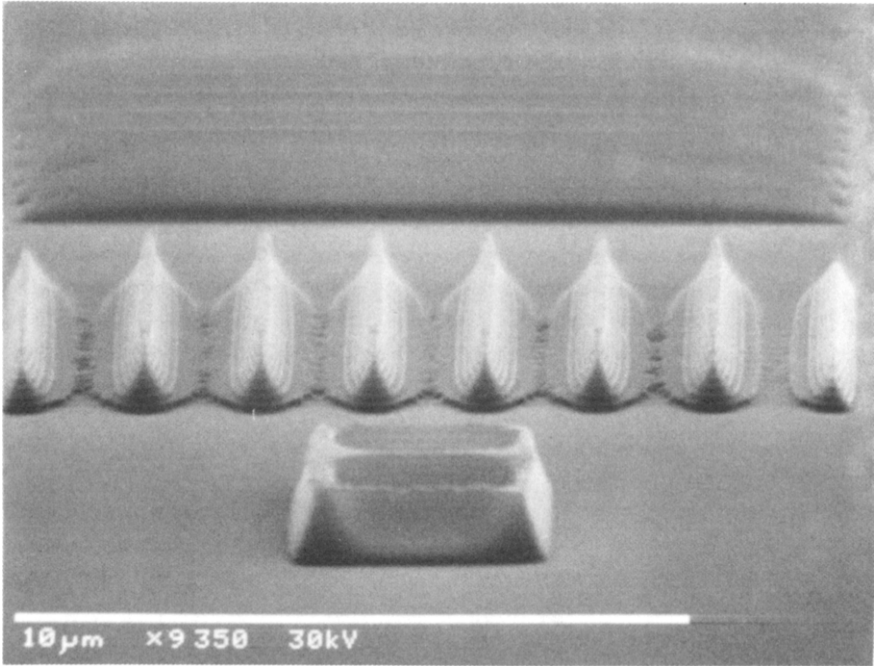


Fig. 5. SEM photo of resist images with 0.8- μm lines and spaces. The standing wave foot has completely bridged across the patterns causing a loss in resolution. (Courtesy of J. Norton.)

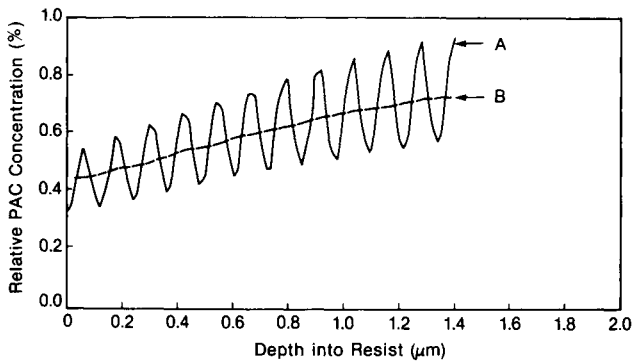


Fig. 6. Simulation of the effective exposure (percent PAC) as a function of depth into the resist film on a bare silicon substrate: curve A shows before postexposure bake and curve B after postexposure bake.

plasma is used to remove the remaining antireflective layer [25]. Other antireflective layers that have been investigated include sputtered silicon, titanium–tungsten alloy, vanadium, silicon dioxide, and silicon nitride [26]. These materials are deposited in a separate operation, often involving complex vacuum equipment, and they require precise thickness control. Such control may be difficult to obtain over topography on the wafer.

Reflective notching of a photoresist image is caused by light that is reflected off the edges of underlying topography. This problem can result in the degradation of resist images by exposure in unwanted areas. The addition of a nonbleaching dye to photoresist helps to absorb the reflected light. Calculations have shown that this absorption is independent of the exposure dose and, therefore, the addition of a nonbleaching dye can actually reduce reflective notching [27]. Generally speaking, a dyed resist should be expected to lower contrast and produce a sloped resist profile [28]. However, the presence of a dye appears to cause a surface development inhibition effect that actually improves the resist profile.

E. Resist Edge Profiles

The edge profiles of the resist must be carefully controlled for both liftoff and dry etch processes. In the case of liftoff, it is important to obtain either vertical or overhanging resist profiles to ensure a discontinuity in the metal coverage between the resist and wafer surfaces (see Fig. 7). If this discontinuity does not exist, it is impossible to lift off the undersired metal successfully. In dry etching, the ratio of the metal to resist etch rate (selectivity) may be as low as 1 : 1. If the resist has a sloped edge profile, the erosion of the resist will be replicated in the metal causing loss in linewidth. This will be discussed in detail later. Vertical resist profiles not only preserve linewidth in anisotropic etch processes, but they also improve linewidth measurement precision, since a vertical edge is easier to detect and use as a fiducial point. Resist edge profiles are related to the aerial image used to expose the resist. Although the transmittance across a photomask grating pattern is originally characterized as a square wave, the light is diffracted into an infinite number of orders. Since, only the zero and first orders can be collected by the optics, the resulting aerial image is reconstructed as a sine wave [8]. As the spatial frequency of the grating pattern is increased, the amplitude (contrast) of the aerial image is reduced. Figure 8 is a schematic of this problem. The photoresist process has the task of returning this sine-wave aerial image to a square-wave resist profile. Figure 9 shows this sequence for a typical resist process. If the slope of the characteristic curve (fraction of percent of thickness remaining versus log expo-

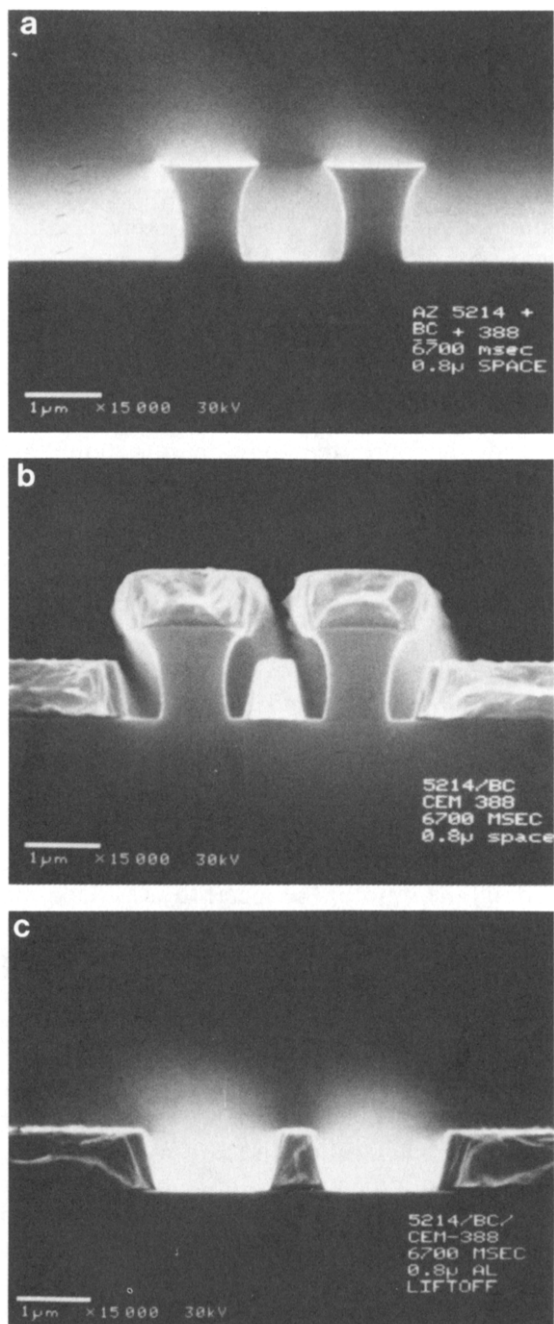


Fig. 7. SEM photos showing liftoff process for 1 μm of Al deposited on AZ-5214 resist. The high aspect ratio of the resist combined with reentrant profiles prevents deposition of the metal on the sidewalls, thus ensuring a successful liftoff process: (a) resist profile, (b) after deposition of 1.0 μm of Al, and (c) after liftoff. (Courtesy of J. Norton.)

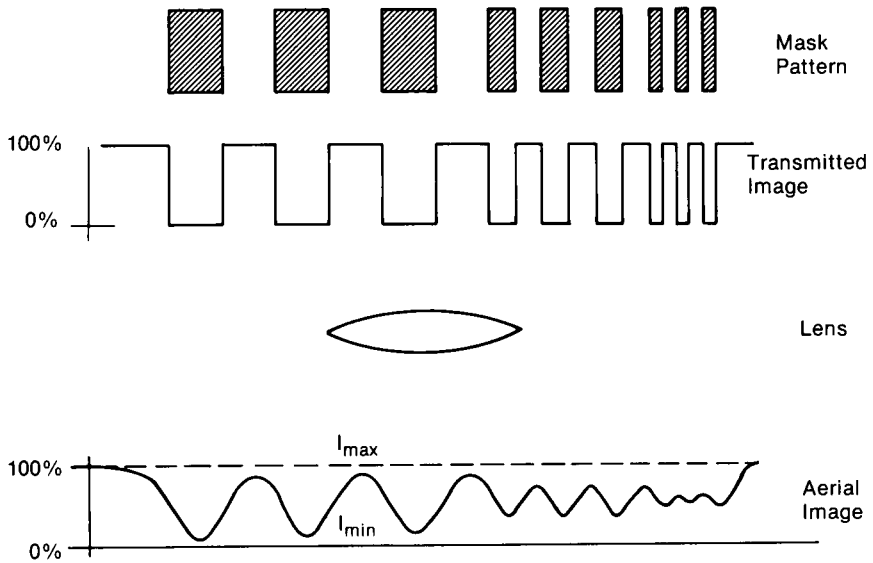


Fig. 8. Schematic of contrast loss with decreasing linewidth. Contrast of the aerial image is defined as $(I_{\max} - I_{\min}) / (I_{\max} + I_{\min})$ and varies between 0 and 1.0. High contrast is required to achieve good resist imaging performance. Notice that the higher frequency patterns exhibit less contrast.

sure) is increased, the resulting resist profiles become more vertical. The photoresist and developer combination must distinguish between those regions with sufficient exposure to allow development and those without sufficient exposure. The characteristic curve of a resist process allows comparison of different processes and their performance. The slope of this curve, also referred to as *gamma*, is an indicator of developer selectivity [29,30]. A practical means of determining gamma is to measure the development rate for a number of different exposures using a laser interferometer or a tool such as the Perkin-Elmer development rate monitor (DRM). A typical set of curves is shown in Fig. 10.

The traditional methods of improving the gamma of a resist process are usually aimed at optimizing the resist bake cycle and the developer formulation, while newer methods include modification of the aerial image by the addition of a contrast enhancement layer [31–35].

This material, which is spun onto the surface of the photoresist, contains a photobleachable dye. Figure 11 demonstrates graphically the effects of a contrast enhancement layer. The portions of the aerial image with higher irradiance bleach clear, allowing exposure of the underlying photoresist, while the low-irradiance areas never totally bleach through. This acts to sharpen the aerial image profiles. By the use of a contrast enhancement

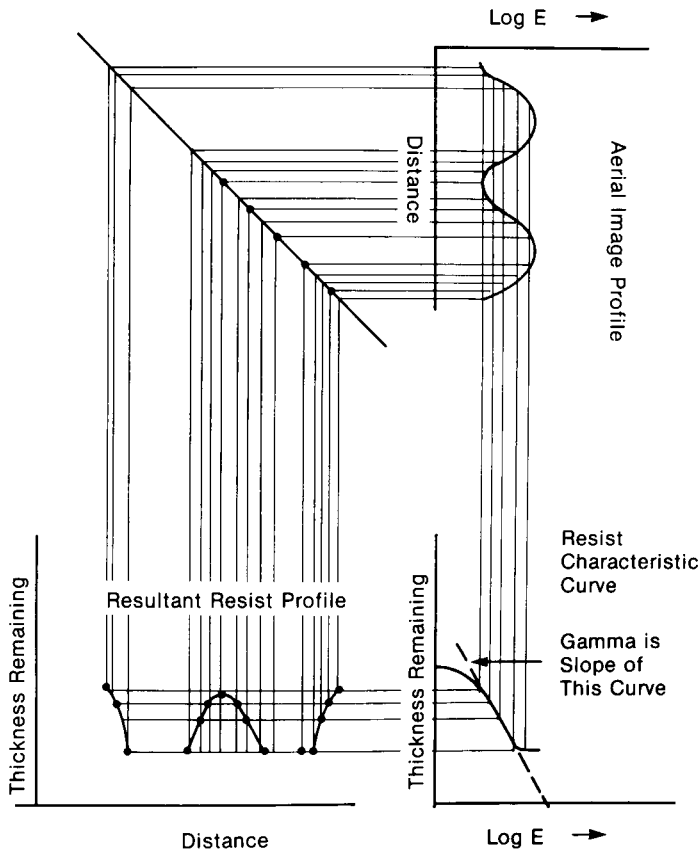


Fig. 9. Graphical representation of the modification of the aerial image profile, as converted to a resist profile, by the development process. As processing conditions are changed, the "gamma" or slope of the development curve becomes more steep. This causes the resultant resist profile to approach a square wave.

process, resist image profiles can be made nearly vertical without changing the gamma of the resist process. The improvement in image profiles can be seen by comparing Fig. 12 to Fig. 13. Contrast enhancement can not only improve the resolution of the photolithographic process, but it can, at the same time, improve the exposure latitude. An added benefit is the ability to obtain improved resolution with greater than normal photoresist thickness. This reduces the burden on dry etch processes, which can erode resist materials at greater than desirable rates.

The importance of achieving the desired image profiles has been discussed. However, it can be difficult to determine the effect of small process changes on profiles without a great deal of tedious work involving scanning

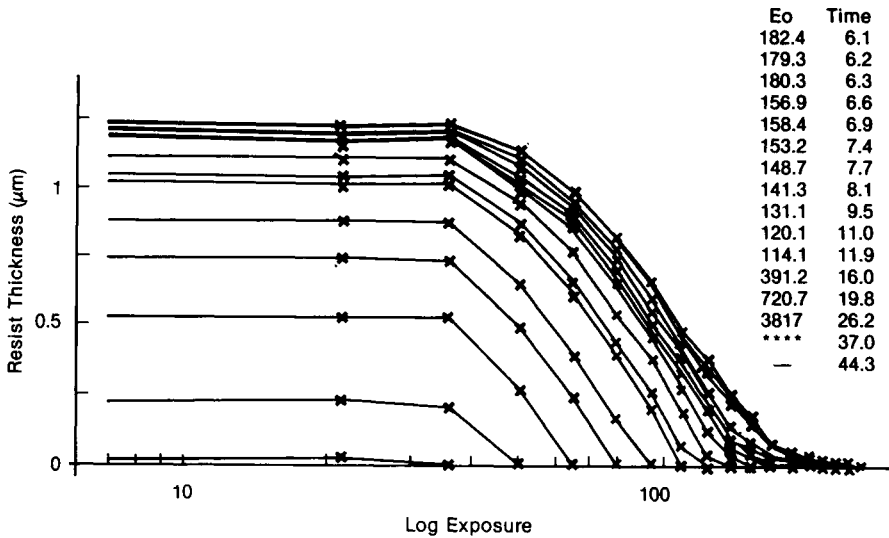


Fig. 10. Development rate monitor output showing resist thickness as a function of exposure dose for a series of development times.

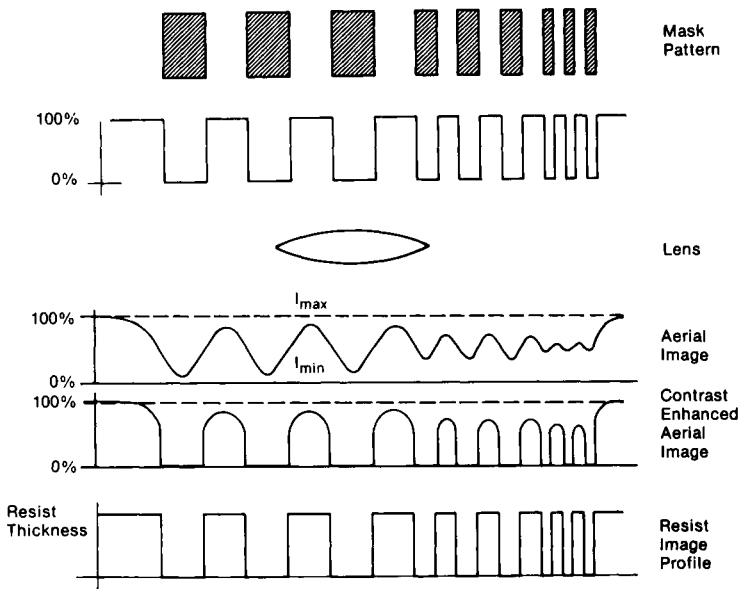


Fig. 11. Graphical representation of the effects of a contrast enhancement layer (CEL) on the aerial image of a photomask. The high-contrast mask image is degraded by the optical system into a low contrast, sine-wave aerial image. CEL consisting of a photobleachable dye initially absorbs strongly then becomes transparent when a threshold dose has been received. The nonlinear bleaching characteristics of the CEL act to transmit light in the high-intensity areas while completely blocking it in the low-intensity areas. This modification of the aerial image results in photoresist profiles that are vertical, improved system resolution and retention of the original resist thickness.

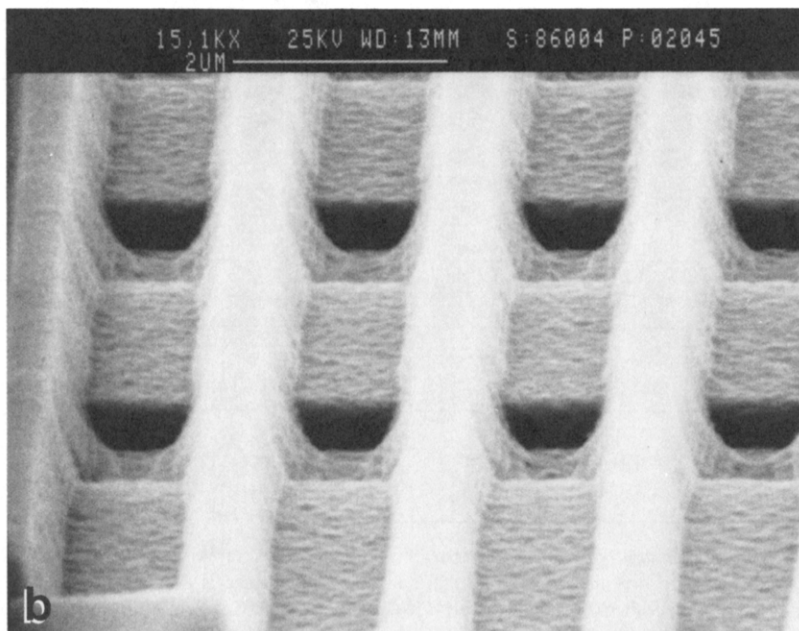
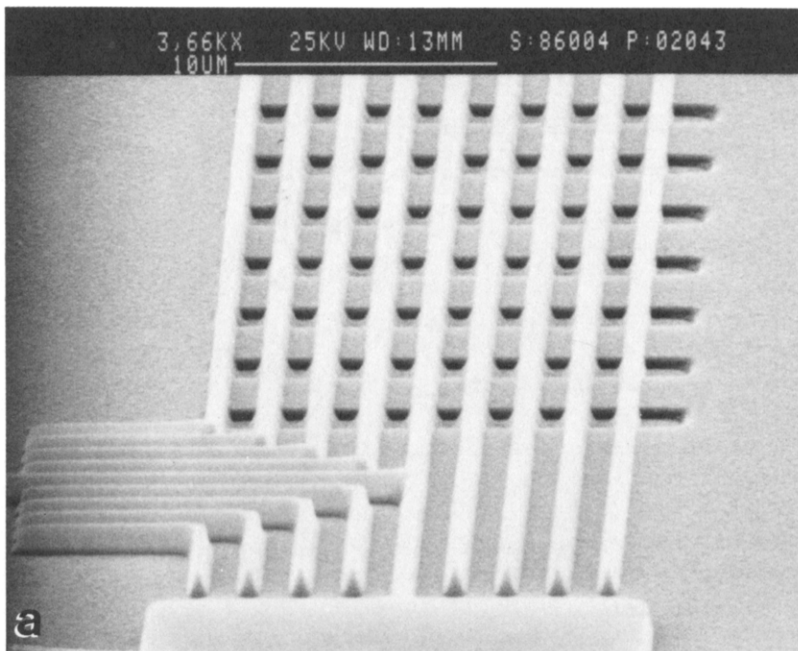


Fig. 12. SEM photos showing conventional resist profiles of 1- μm lines and spaces crossing 0.5- μm deep trenches. Note poor line profiles, standing waves, and bridging between lines. (Courtesy of J. Norton.)

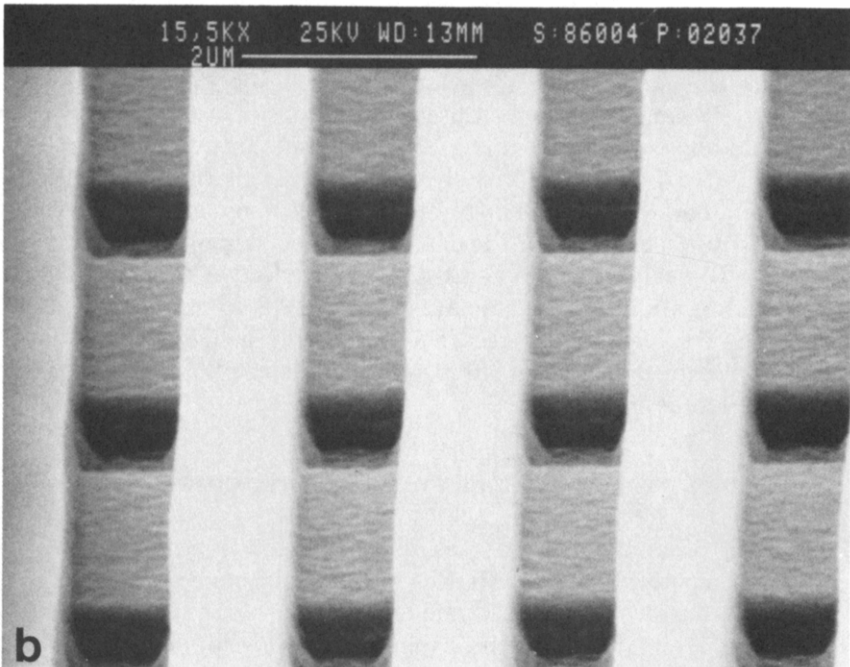
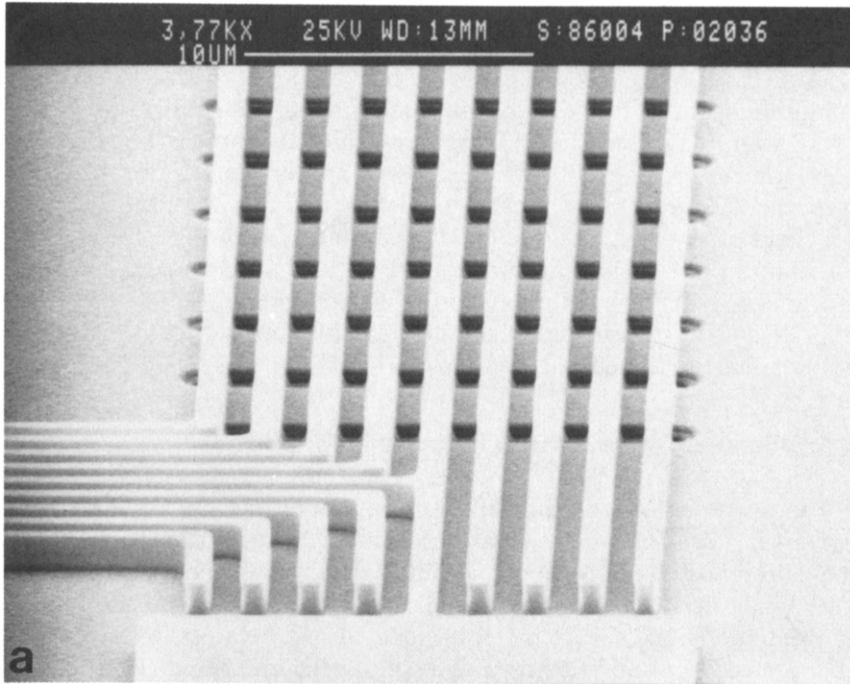


Fig. 13. SEM photos showing effects of contrast-enhancement process on photoresist profiles of 1.0- μ m lines and spaces. Note sharper profile, absence of standing waves, and improved linewidth control over steps. (Courtesy of J. Norton.)

electron microscope (SEM) cross sections. The impact of changing process conditions can be modeled by the use of simulation programs such as SAMPLE [36] or PROLITH [37]. These require the input of bleaching and development parameters. Such parameters are time consuming to remeasure whenever the process is changed slightly, and they are strongly process dependent. New methods such as the combination of the Perkin–Elmer DRM and PROSIM [38] software are able to accurately predict the resultant image profiles by simply exposing and developing a test wafer. This improved ease of use makes profile modeling an indispensable part of lithographic process development.

F. Alignment of Patterns to Underlying Patterns

The alignment of the metallization pattern to the underlying contact pattern is a critical process step. The autoalignment system employed in step-and-repeat systems must transmit light through the photoresist and reflect light from the deposited metal surface to detect the precise location of the underlying contact pattern. Next, the wafer must be moved into near-perfect registration before the resist pattern is exposed. Typical VLSI tolerances require alignment within $\pm 0.25 \mu\text{m}$. The surface roughness of metal films can reduce the signal-to-noise ratio of the reflected signal, making the alignment more difficult. If antireflective layers are employed, the alignment system must somehow deal with very low image signals when the exposing wavelength is used. Some systems use a helium–neon laser to aid alignment since most photoresists and antireflective materials transmit well in the red portion of the spectrum. An alternative approach is the use of a dark-field alignment system. In this approach, the change in photoresist surface topography is detected, thus making the system insensitive to the opacity of the photoresist and antireflective layers. One possible method of improving alignment performance is to remove the photoresist from the alignment target, thus providing a high-contrast target image. A system that performs this task using laser photoablation of the resist has been described [39].

G. Electrical Probe Method for Process Characterization

The determination of process latitude is of vital importance in VLSI patterning. A number of the variables that must be controlled in order to achieve a stable process are: substrate reflectivity; resist thickness; softbake time and temperature; and focus, exposure, and development conditions. If each of the process variables is characterized, a large quantity of line-

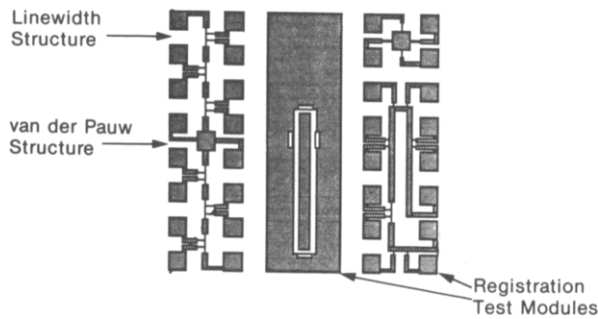


Fig. 14. Test structure for measuring registration and linewidth using the Prometrix Lithomap system.

width data must be obtained. Automated data collection by electrical measurement provides an ideal tool for both process development and process control. Commercial systems such as the Prometrix Lithomap system are able to probe and plot the linewidth and registration data, facilitating process development. The test structures consist of resistor bars and van der Pauw patterns, which are used to calculate the true linewidth, correcting for the local sheet resistance (see Fig. 14). The graphical data output formats include histograms, contour maps, focus-exposure curves, three-dimensional graphs, and registration vector maps (see Figs. 15 – 19).

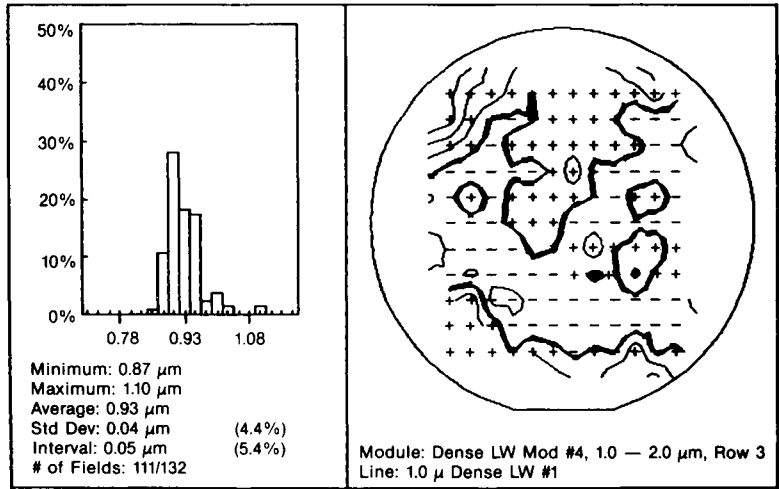


Fig. 15. Contour map of linewidth variation across wafer, measured with Prometrix Lithomap system. Since patterns are delineated by etching, nonuniformities in both lithography and etching are measured.

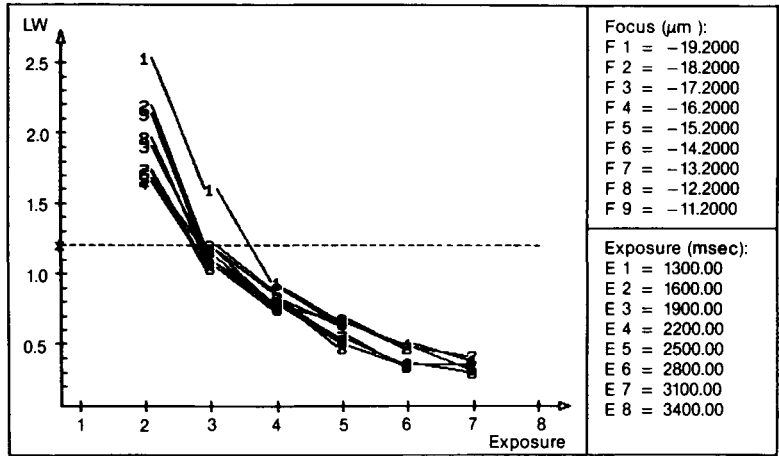


Fig. 16. Linewidth as a function of exposure for etched metal patterns generated by Prometrix Lithomap system. Each data point represents a different focus-exposure combination, which can be used to determine the conditions required to obtain the desired linewidth.

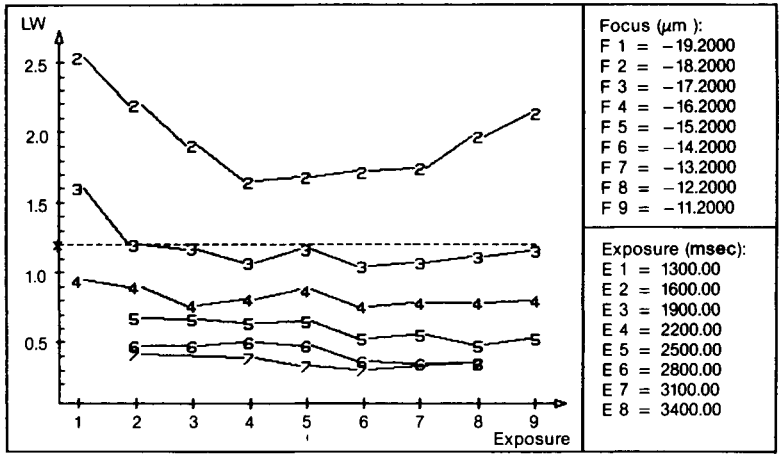


Fig. 17. Linewidth as a function of focus for etched metal patterns, each line represents the linewidth achieved over a range of focus values with a constant exposure. This shows the effective focus latitude clearly.

H. Reducing Resist Etch Rate

The etch rate of photoresist in plasma and reactive ion etch systems depends on the composition of the photoresist as well as on a large number of etching parameters, which will be discussed in detail later. The etch rate

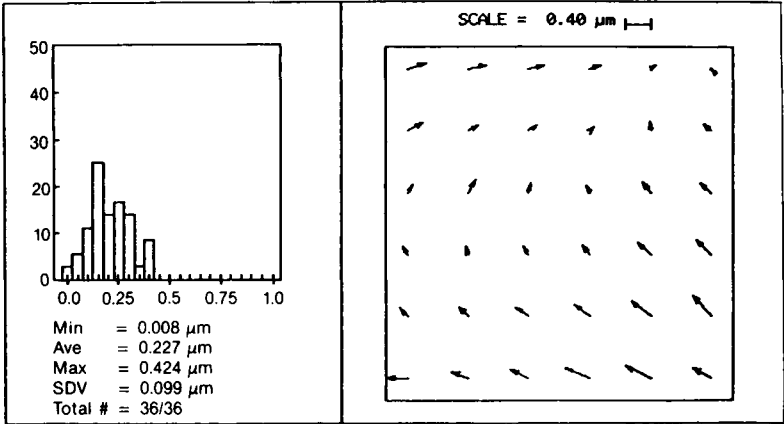


Fig. 18. Intrafield registration error vector map generated by Prometric Lithomap system. Each vector indicates the location, direction, and magnitude of the measured registration error within a single-exposure field. In this case a second step and repeat system was used to align to a pattern initially produced on a reference system. This data illustrates the possible registration differences that occur when step-and-repeat systems are not matched for overlay.

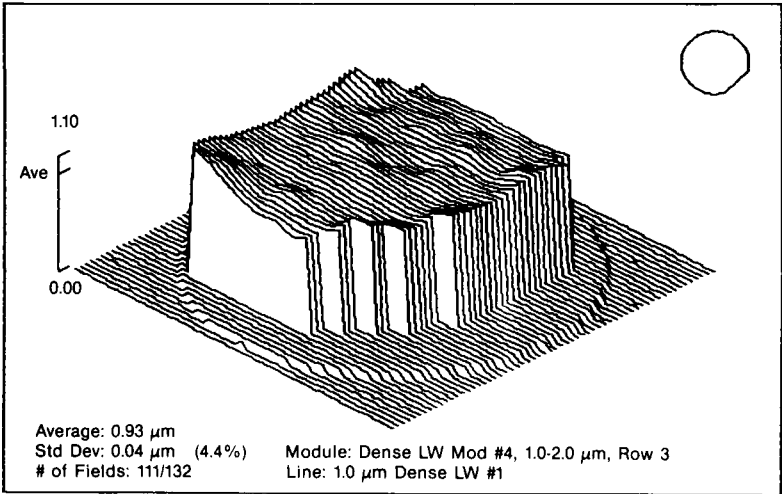


Fig. 19. Three-dimensional map of linewidth variations across a 4-in. wafer. Effects are due to lithography and etching of the metal pattern. Vertical axis represents measurement linewidth (data obtained with Prometrix Lithomap system).

of resist can be reduced somewhat by high-temperature baking processes, but these often result in unwanted distortion or flowing of the resist profiles. Deep UV hardening treatments act to cross-link the photoresist, reducing the etch rate [40].

TABLE II
Effect of Liquid “Hardening” on Photoresist Etch Rate

RIE process		Etch rate normal resist	Etch rate treated resist
Al	$\text{BCl}_3/\text{CCl}_4/\text{O}_2$	1400 Å/min	1075 Å/min
Mo	$\text{SF}_6/\text{Cl}_2/\text{O}_2$	2000 Å/min	1100 Å/min
Polysilicon	$\text{CBrF}_3/\text{Cl}_2$	500 Å/min	440 Å/min
SiO_2	CHF_3/Ar	80 Å/min	60 Å/min

Another technique involves the use of a topcoat of material that is spun over the developed photoresist image prior to a high-temperature hardbake [41]. This diffuses into the resist surface causing a hardened skin to form, thus minimizing the possibility of thermoplastic flow. Table II shows some comparative data for Kodak 820 resist with and without this treatment.

I. Multilayer Resists

The need for obtaining high-resolution, undistorted patterns, and vertical-wall profiles over complex and reflective topographies with a single layer of photoresist thick enough to withstand dry etching, is a challenge sometimes avoided by the use of multiple layers of materials that constitute the resist. In such processes, the lower layer is a thick, planarizing coating of an organic material such as conventional photoresist or polyimide; the intermediate transfer layer is a sputtered, evaporated, or chemical vapor deposited (plasma enhanced) film or spin-on “glass;” and the upper layer is a coating of photoresist for patterning [42]. The base layer not only performs a planarizing function and may have antireflecting properties due to the presence of a dye, but it is sufficiently thick so that it has adequate etch resistance. The inorganic transfer layer may also add antireflective characteristics, and it can be chosen so that it augments the etch resistance of the lower layer. The burden on the upper layer of photoresist is thus reduced since it need only be thin enough to pattern and etch the relatively thin and planar transfer layer.

Since highly anisotropic dry etch processes are used to pattern the intermediate and lower layers, standing wave and development problems are eliminated and high-resolution, vertical profiles can be assured. However, the low-reflectivity inherent in multilayer systems can cause alignment problems for reasons already discussed. The extra complexity of the multilayer process may be a deterrent to high-volume production, but its value has been demonstrated in a number of descriptions of processes for the

fabrication of submicron structures. Contrast enhancement layers, with or without antireflective coatings applied beneath the photoresist, represent a more simple form of multilayer resist structure, with less process complexity, but the final selection must rest on the nature of the application and on the processing resources available.

III. METAL ETCHING

A. General Principles

The most accurate and controllable methods of replicating the dimensions of the resist pattern involve the use of anisotropic plasma etching, in which the vertical etch rate of the metal is much greater than the lateral rate (e.g., $> 10:1$). Liquid etch processes, which are typically isotropic, are incapable of etching metals without causing undercutting beneath the resist and loss of control of critical dimensions. Furthermore, the adhesion of the resist, as well as its dimensional and chemical integrity, can be reduced by the strong acids, which are the ingredients of many wet etches.

As will be shown in Section III.F, all plasma etch processes are not necessarily anisotropic, and many of those that are, can be altered by changes in chemistry so that they are isotropic. In fact, “barrel” etching, the earliest form of plasma-induced etching, makes use of long-lived radicals that etch isotropically. The various types dry etch systems suitable for anisotropic etching have been discussed in detail in a number of reviews [43–46]. With the exception of reactive ion beam etching [46], the etch chambers of such systems house a pair of electrodes, with one of the electrodes coupled to a high-frequency source and the other electrode connected to ground, as is the chamber itself. In the reactive ion etch (RIE) mode, the wafers are placed on the powered electrode, while in the planar plasma mode, the wafers are on the grounded electrode.

Other differences, such as chamber pressure during etching, electrode spacing, and rf frequency, distinguish the two major methods of etching. Changes in these conditions can result in hybrid mechanisms, frequently referred to as quasi-RIE, which operate somewhere between the RIE and planar plasma modes. An outline of a typical batch RIE system with a parallel-plate electrode structure is shown in Fig. 20. An alternate electrode structure capable of handling more wafers in a single load is shown in Fig. 21. High etch rate, single-wafer etch systems, typically operate in the planar or quasi-RIE mode.

The goal in all types of plasma etching used in VLSI patterning applica-

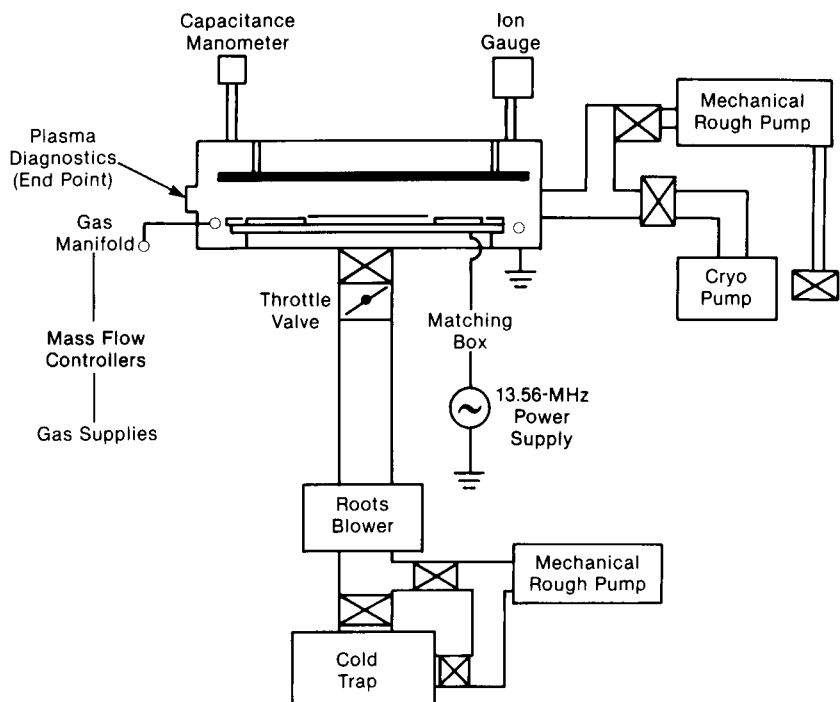


Fig. 20. Outline of typical batch RIE system with planar electrodes.

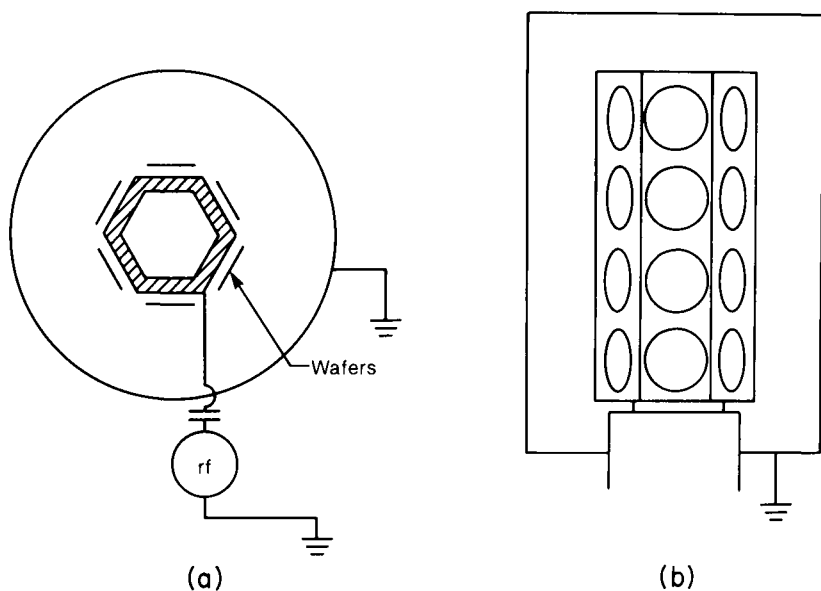


Fig. 21. Outline of hexode RIE system: (a) top view and (b) side view.

tions is to provide (1) reactive chemical species, primarily in the form of radicals and ions, which will combine with substrate atoms not masked by the resist to form volatile species and (2) to produce sufficient ion bombardment of the surface of the wafers to result in anisotropic or vertical removal of the film species. The mechanisms by which both of these steps occur are not well understood. Some of the proposed mechanisms are described by Flamm [44] and Smith [45].

Table III lists the general criteria for an effective metal etch process suitable for VLSI patterning applications. The importance of selectivity in etching is demonstrated in Fig. 22a and b, which show SAMPLE simulations of changes in the profiles and thickness of photoresist and metal during anisotropic RIE for a typical resist profile with metal-to-resist etch rate ratios of 3:1 and 1:1, respectively. Figures 23a and b demonstrate the effects of selectivity when a resist with vertical profile is used. The metal linewidth loss with vertical resist is negligible, while that for a tapered resist profile with 1:1 etch selectivity may be unacceptable for certain VLSI applications. However, if the photoresist profile is vertical and etches laterally, at a rate which is, for example, 50% that of the vertical etch rate of the metal, the metal linewidth loss due to tapering may also be excessive, as is shown in Fig. 24. Isotropic etching of the metal, which can take place without significant lateral or vertical attack of the resist, can produce even greater loss of metal linewidth (see Fig. 25) and demonstrates clearly the benefits of anisotropic processes.

High selectivity is important when etching metals over dielectrics because thinning of such substrates may result in the loss of adequate electrical isolation. Theoretically, the ability to detect the end of etch should permit the etch process to be stopped before excessive loss. However, the need to overetch in order to clear metal from portions of the underlying topography can result in loss of substrate. Nonuniformities in film thick-

TABLE III
General Criteria for Dry Etching Processes for Metals

-
- | | |
|-----|---|
| (1) | Anisotropic or vertical etching of the metal and of the resist. |
| (2) | High etch rate ratio (Err) of metal as compared to resist and substrate (e.g.) Err of metal:resist > 3; Err of metal:substrate > 10 |
| (3) | Vertical etch rate variation of < 5% across the surface of the wafer and from wafer to wafer |
| (4) | Ability to produce volatile etch products which will leave no residues on the wafer |
| (5) | Minimal radiational or sputter induced damage to the substrate |
| (6) | Ability to detect the completion of etch accurately and reproducibly |
| (7) | Metal etch rate that results is a commercially acceptable wafer throughput (e.g., 500 Å/min in a batch reactor or 2–3000 Å/min in a single-wafer reactor) |
-

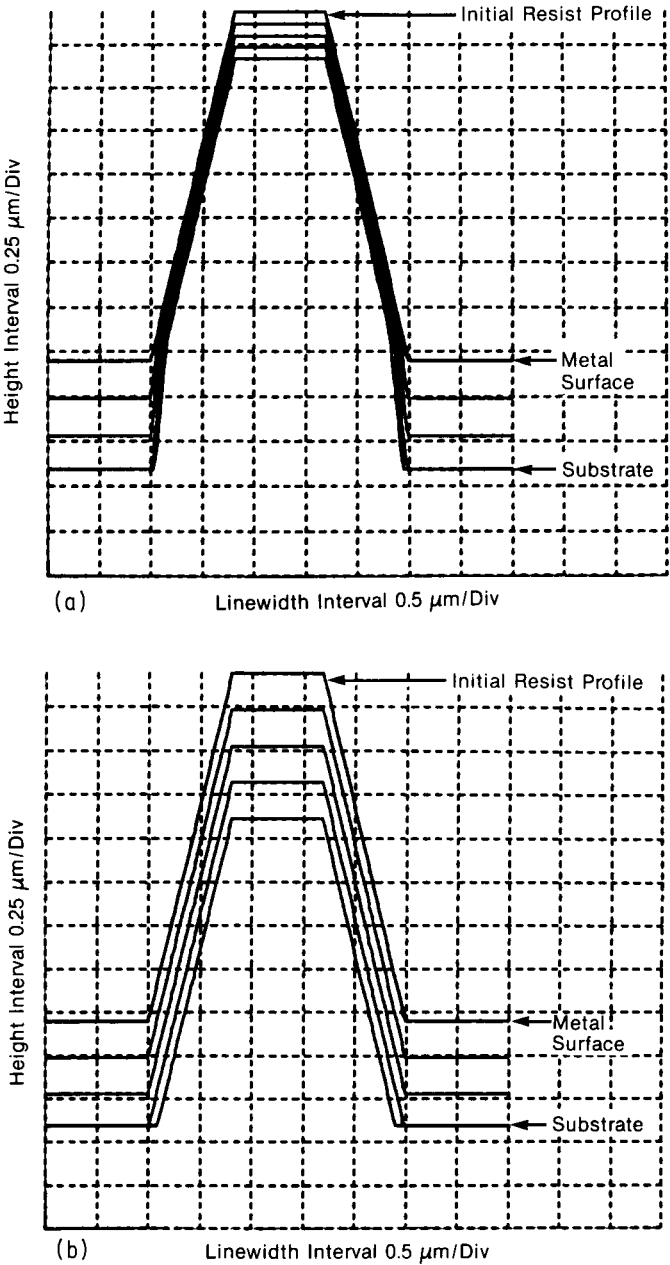


Fig. 22. SAMPLE simulation of anisotropic etching with tapered resist profile: (a) metal-to-resist etch rate ratio of 3 and (b) metal-to-resist etch rate ratio of 1. Note tapered metal profile and loss of linewidth in (b).

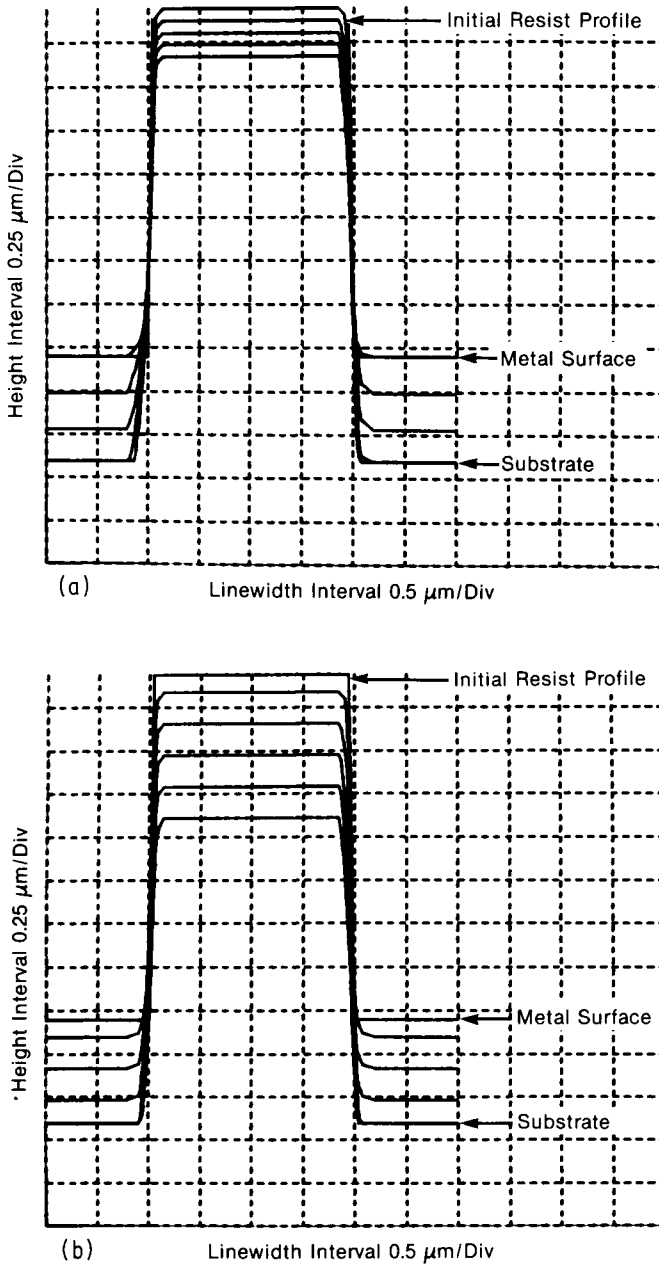


Fig. 23. SAMPLE simulation of anisotropic etching with vertical resist profile: (a) metal-to-resist etch rate ratio of 3 and (b) metal-to-resist etch rate ratio of 1. Note vertical profile and absence of linewidth loss in both cases.

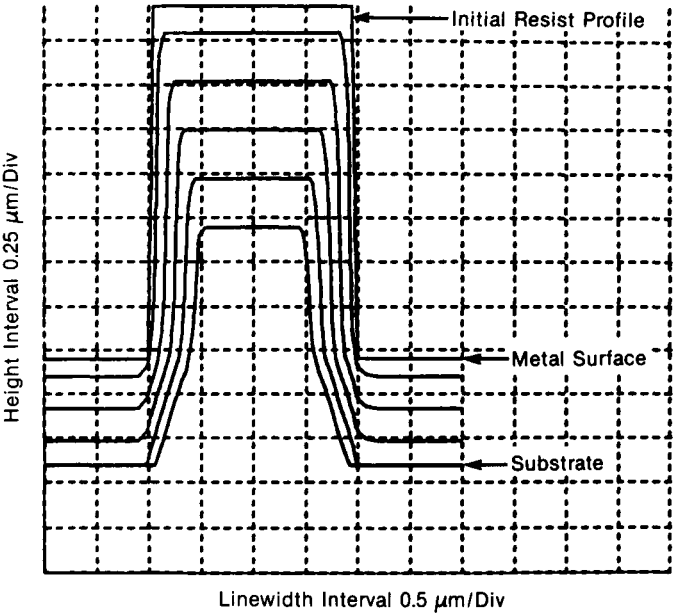


Fig. 24. SAMPLE simulation of isotropic etching of vertical resist profile with anisotropic etching of metal. Note tapered metal profile and loss of metal linewidth.

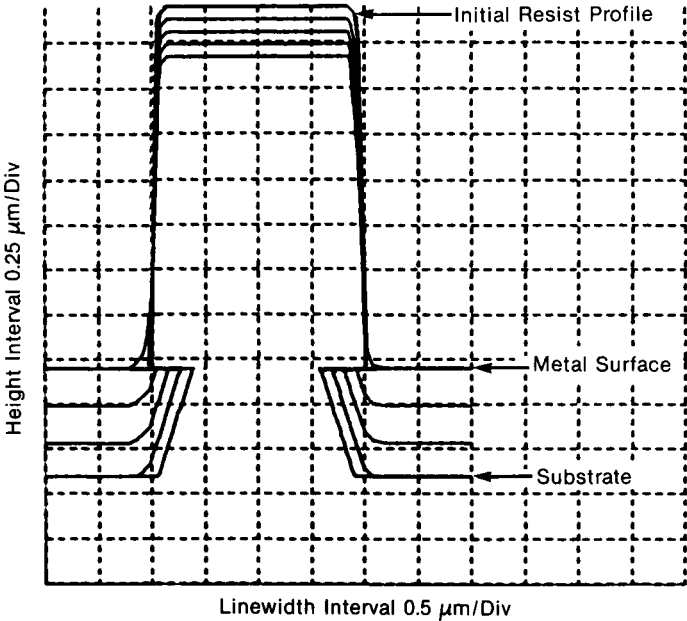


Fig. 25. SAMPLE simulation of isotropic etching of metal with anisotropic etching of vertical resist profile. Note undercutting and loss of metal linewidth.

ness or in across-the-wafer etch rate may also require additional etching that will attack, first, areas of substrate underneath the portions of the metal that are thinner or have been etched first. The most critical need for high metal–substrate selectivity is encountered while etching metal gates over thin (e.g., 150–250 Å) gate oxides.

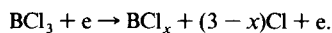
B. Etching of Aluminum and Aluminum Alloys

There is some irony to the fact that aluminum, and aluminum alloys, the metals most commonly used as interconnects in integrated circuit fabrication, present the greatest challenges in dry etching. Difficulties associated with etching these materials include: (1) erratic etch initiation times, (2) photoresist degradation, (3) incomplete etching of additives such as Si, Cu, and Ti, and (4) postetch corrosion. With all of these issues to contend with, the advantages of using Al as an interconnect material in a field of few competing materials, still outweigh, in most cases, the relatively complicated etching procedures that are required.

1. Removal of Native Oxide

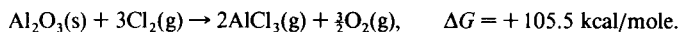
The thin native oxide (Al_2O_3) that forms on the surface of Al, hinders the etch process, resulting in a delay between the start of the discharge and the onset of Al etching. This “induction period” or “initiation time” is also influenced by the residual partial pressure of water vapor in the etch chamber, which if not scavenged can cause the surface of Al to reoxidize [47]. The slow and nonuniform removal of an Al_2O_3 film, which itself can be nonuniform in thickness, can cause severe Al etch uniformity problems both across the wafer and from wafer to wafer. It can also cause varying amounts of residue to be left on the underlying substrate if long overetch periods are not used.

Boron trichloride (BCl_3) is added to many etching gas mixtures because it acts as an efficient scavenger of oxygen and water vapor [48]. It also dissociates in the plasma to form species (BCl_x) that are strong reducing agents for Al_2O_3 [49,50]:

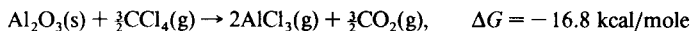


Silicon tetrachloride (SiCl_4) and carbon tetrachloride (CCl_4) are also used because of their ability to reduce Al_2O_3 in a discharge [48–50]. The species formed from the dissociation of these gases, however, are generally not as effective as BCl_x . Although chlorine (Cl_2) is able to etch aluminum, it cannot penetrate the Al_2O_3 layer. This may be explained by the high

positive value of the Gibbs free energy of reaction (ΔG), which is required for the reaction to proceed [51]:



With CCl_4 , the reaction is more thermodynamically favorable:



The negative ΔG value indicates that this reaction will proceed as written when provided with sufficient activation from the plasma.

Higher rf power is sometimes used at the start of the etch process in order to accelerate the removal of aluminum oxide films by increasing the rate of formation of active reducing species [52]. Pre-etch plasmas, such as H_2 [53], CF_4 [54], and Ar, which do not etch aluminum, have also been used to remove Al_2O_3 by sputtering.

Since aluminum chloride (AlCl_3), the main reaction product of aluminum etching, is hygroscopic, it can absorb water vapor in the atmosphere to which an open reactor is exposed. Although some plasmas are capable of scavenging oxygen or water vapor, other procedures can be followed in order to reduce the possibility of moisture accumulation in the chamber. These include (1) purging the chamber with inert gases or (2) using nitrogen-flushed load locks [55,56], (3) heating the chamber walls and electrodes during nonetching periods [57,58], and (4) using a liquid nitrogen

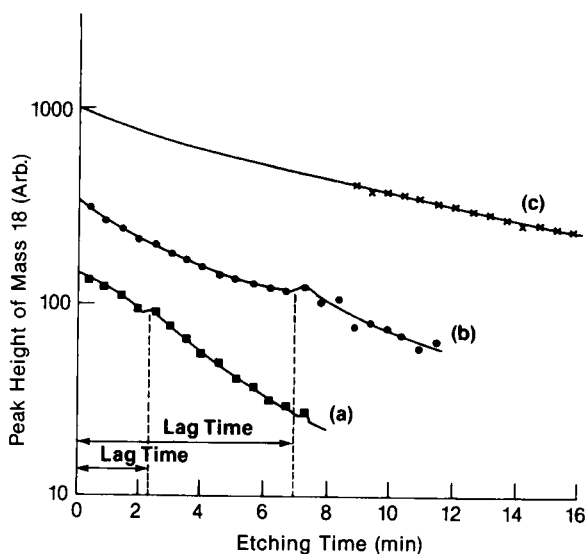
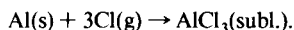


Fig. 26. Peak height of water vapor ($M/e = 18$) using mass spectroscopy versus etching time of Al: (a) pumping with a diffusion pump and a cold trap, (b) pumping with a cold trap and a mechanical pump, and (c) pumping with a mechanical pump only, Al does not etch. (From Tsukada *et al.* [59].)

trap or a cryopump to obtain low background pressure [55]. The influence of cold traps and pumping systems on the etching of Al using CCl_4 is shown in Fig. 26 [59]. Water (18 amu) was monitored using mass spectroscopy during etching. Aluminum etching started only after the H_2O partial pressure dropped below a critical level (0.5 Pa). From this, it is obvious that if the induction period cannot be controlled, reproducible and accurate aluminum etching will be difficult to achieve.

2. Etch Gas Mixtures

Since aluminum fluoride is nonvolatile, etching of aluminum is generally performed with chlorinated gases, and occasionally, with brominated gases. A simplified equation for the reaction is

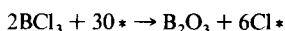


For the reasons already mentioned, effective Al etching is rarely accomplished with the use of a single gas. The major components of most gas mixtures are CCl_4 , BCl_3 , and SiCl_4 . Other halogens such as Cl_2 [60–62], HCl , Br_2 , or HBr [60], which cannot be used alone because of difficulty in removing aluminum oxide, can be added to increase etch rates by providing a greater population of reactant species.

CCl_4 is usually mixed with inert gases such as Ar [63], He [64], or N_2 [65], or with Cl_2 [66] to reduce polymer formation. BCl_3 has been shown to be a relatively poor source of atomic Cl as compared to CCl_4 [67]. Etch rates of Al using BCl_3 alone are therefore in the range of only 400–500 Å/min. A typical method of increasing the Al etch rate is to add Cl_2 to BCl_3 [68]. The composition of these gases however, is critical, particularly in batch systems, since sufficient Cl_2 is needed for reasonable etch rates, for all wafers, but excessive amounts may result in isotropic etching and poor dimensional control. The use of a BCl_3/Cl_2 -based gas mixture was successfully demonstrated in the RIE mode, using a two-stage process in which the Cl_2 flow and dc-bias voltage were reduced at the endpoint to prevent undercutting [69].

The addition of Cl_2 to BCl_3 has also been shown to lower the ability of the latter to reduce Al_2O_3 . Emission spectroscopy studies have indicated that when Cl_2 is present, the relative intensities of BCl [67] and B signals [70] decrease (see Figs. 27 and 28). This suggests that the dissociation of BCl_3 is being suppressed, and indicates further that B or BCl_x species are involved in the reaction with Al_2O_3 .

Another method of increasing Al etch rates while using BCl_3 is to add O_2 or CF_4 to enhance the generation of active Cl species as shown by [68]



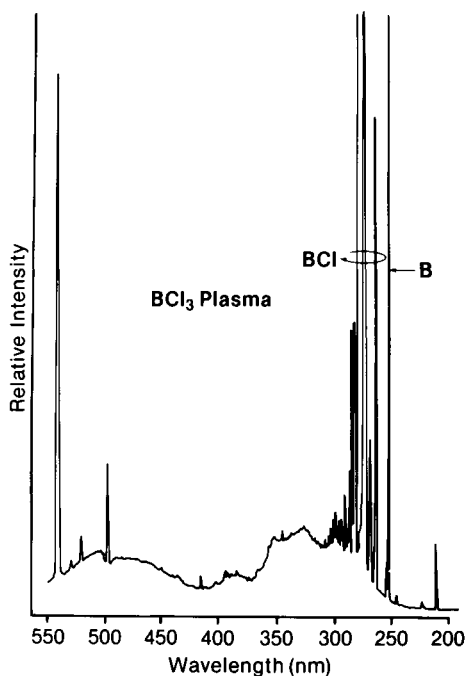


Fig. 27. Optical emission spectrum of a BCl_3 plasma in a reactive ion etcher. Etching parameters are flow, 30 sccm; pressure, 70 mTorr; and power, 300 W (0.25 W/cm^2).

Small amounts of oxygen, usually under 5%, can increase Al etch rates by as much as a factor of six. However, higher percentages (e.g., 10% or more), can cause boron oxide formation, which results in particulates.

Anisotropic reactive ion etching has been reported using $\text{BCl}_3/\text{CF}_4/\text{O}_2$ [71] and $\text{BCl}_3/\text{CCl}_4/\text{O}_2$ [70]. In the latter work, a two-step procedure was developed, with the $\text{BCl}_3/\text{CCl}_4/\text{O}_2$ mixture first used to anisotropically etch the bulk of the film to an endpoint. The CCl_4 flow was then terminated in order to more effectively remove metal over steep steps due to the slightly isotropic etch of the BCl_3/O_2 mixture during the overetch period (See Fig. 29 and 30). The availability of an effective means of overetch while still preserving linewidth dimensions can become especially important when bias sputtering of Al is used [72]. With this deposition technique, the Al may actually be planarized and, therefore, become more difficult to remove over topography. Other gases used for aluminum etching are listed in Table IV.

3. Aluminum Alloys

When aluminum is alloyed with small percentages of silicon to prevent penetration into junctions, and with copper or titanium to increase elec-

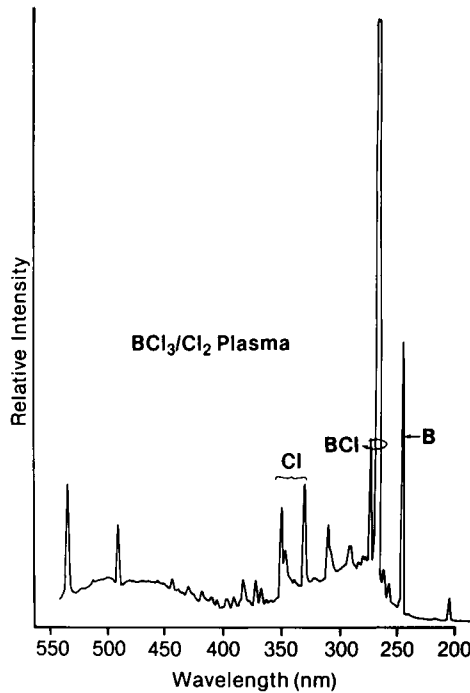


Fig. 28. Optical emission spectrum of a 10% Cl_2 in BCl_3 plasma in a reactive ion etcher. Etching parameters are flow, 33 sccm; pressure, 70 mTorr; and power, 300 W (0.25 W/cm^2).

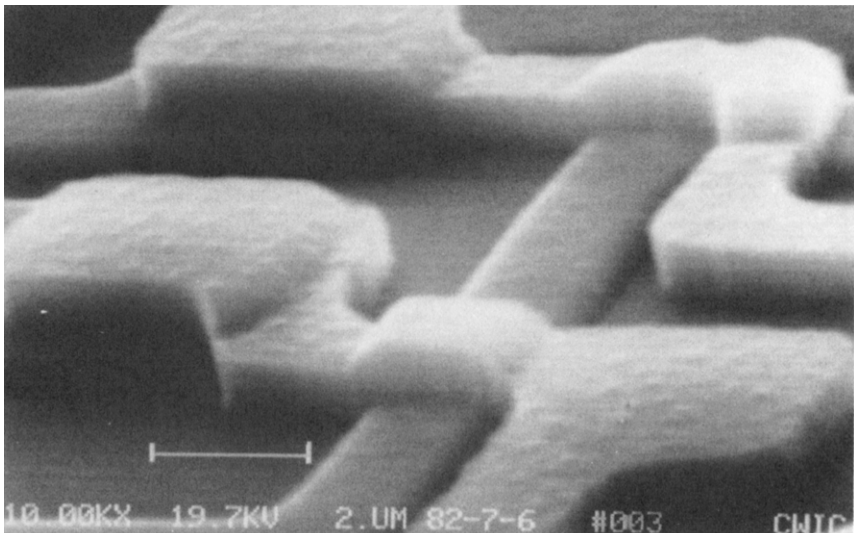


Fig. 29. SEM photo of Al/1% Si (over steps of oxide covered polysilicon) with hillocks removed by etching with $\text{BCl}_3/\text{CCl}_4/\text{O}_2$ for the etch period and BCl_3/O_2 for a 40% overetch. (Courtesy of J. Norton.)

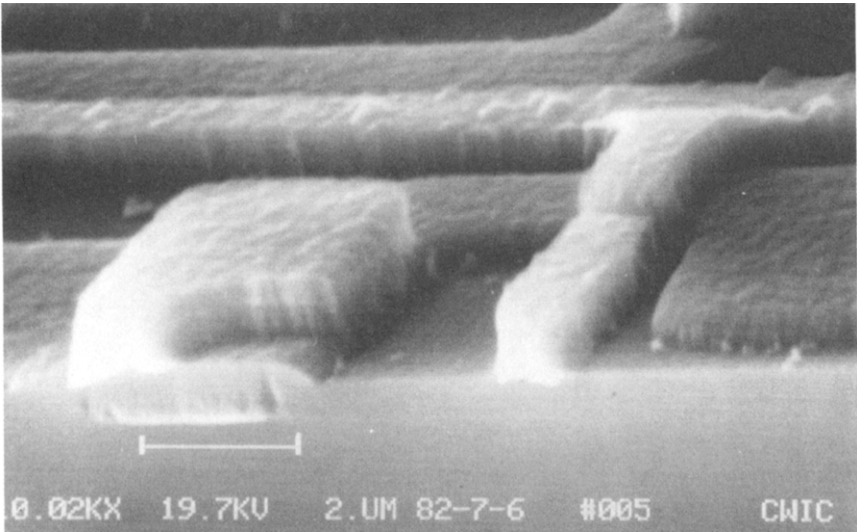


Fig. 30. SEM photo of Al/1% Si (over steps of oxide covered polysilicon) with hillocks that did not completely etch, using BCl₃/CCl₄/O₂ for the etch and 40% overetch period. (Courtesy of J. Norton.)

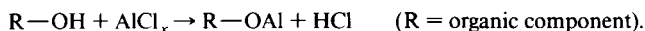
TABLE IV
Gases Used for Aluminum Etching

Gas	Reference(s)
CCl ₄ /He	[64,79]
CCl ₄ /Ar	[63]
CCl ₄ /N ₂	[65]
CCl ₄ /Cl ₂	[66]
BCl ₃ /Cl ₂	[68,80]
BCl ₃ /Cl ₂ /SiF ₄ /He	[69]
BCl ₃ /CCl ₄ /O ₂	[70]
BCl ₃ /CF ₄ /O ₂	[71]
BCl ₃ /Cl ₂ /CF ₄ /O ₂	[73]
BCl ₃ /Cl ₂ /C ₃ H ₆	[74]
BCl ₃ /Cl ₂ /CHCl ₃ /He	[78]
BCl ₃ /PCl ₃	[75]
HBr/Ar	[63]
Br/Ar	[63]
BBr ₃	[75,77]
SiCl ₄ /BCl ₃ /Cl ₂ /He	[76]

tromigration resistance, the etch process can become more complex. The same gases that etch pure aluminum can usually be used to etch alloys containing silicon or titanium since SiCl_4 and TiCl_4 are volatile species. A higher dc-bias voltage may be needed, however [80]. If during the sputter deposition of the alloy film, there is a pileup of Si or Ti at the substrate interface, longer overetching or the addition of a postetch step to remove these materials must be instituted.

Aluminum/copper films, on the other hand, are more difficult to etch, since copper chlorides are not very volatile. The most favorable results have been obtained in RIE systems operating at low pressures (e.g., 20 mTorr) while maintaining the wafer surface at relatively high temperatures [81]. Exposure of Cu to Cl_2 at 30°C was shown to produce a chloride surface layer whose thickness increased linearly with time [82]. Mass spectroscopy data then showed that desorption of Cu_3Cl_3 began at about 150°C .

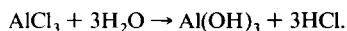
Etching at higher temperatures may preclude the use of typical photoresist materials, and inorganic etch masks may be required. Even under normal aluminum etching conditions, aluminum etch products have been shown to enhance the degradation of positive photoresist [83]. Pattern distortion due to resist flow or reticulation can occur, at least in part due to the heat generated by the exothermic etching reaction. Also the phenolic groups present in positive photoresists are likely sites of attack by AlCl_x species, as shown in the following reaction [51]:



Special photoresist “hardening” techniques such as PRIST (plasma resist image stabilization technique) [79,84] and UV hardening [85] are sometimes used in combination with high-temperature bakes to make the photoresist more resistant during the aluminum etch. The mechanisms for obtaining the improved properties are not completely understood, but they are believed to be related to the thermal decomposition of the photoactive component (a naphthoquinone diazide) in the resist system, and the removal of residual solvent (typically, cellosolve acetate).

4. Postetch Corrosion and Passivation

The chlorine containing residues of aluminum etching, which remain on plasma-exposed surfaces, can cause postetch corrosion. Upon exposure to moisture in the atmosphere, they can hydrolyze, producing hydrochloric acid in the following reaction:



Chlorine ions (Cl^-) penetrate the aluminum oxide passivating layer and

react with Al to produce additional AlCl_3 , sustaining this reaction. Since only a catalytic amount of chloride ions is required, small amounts of residue can cause severe corrosion.

A variety of steps have been used to prevent postetch corrosion. Deionized water rinses or soaks [86,87] are sometimes used, but often corrosion occurs so rapidly that it has already taken place before the wafers can be immersed. Rinsing is also often unsuccessful in preventing long-term corrosion [88].

Another means of corrosion prevention is to expose the wafers to a postetch plasma-containing fluorinated gases. Chlorine ions that are adsorbed on the wafer surface are replaced by fluorine ions (e.g., AlCl_3 can be converted to AlF_3). Gases that have been used for this purpose include CF_4 [89–91], CHF_3 [89,90], NF_3 [89], and SF_6 [89]. Other postetch plasmas, such as N_2 [92], H_2 [93], or O_2 are sometimes used to remove polymeric materials and to form a layer of protective native aluminum oxide. Since the photoresist is capable of retaining AlCl_3 and absorbing water, it is either completely removed from the wafers before they are taken out of the etcher or is removed shortly after the Al etch.

Thermal oxidation treatments, at 300–350°C in O_2 at atmospheric pressure [94], have been shown to provide corrosion resistance superior to that which can be obtained with an oxygen plasma alone.

When etching aluminum/copper films, the problem of postetch corrosion is significantly increased. Electrochemically dissimilar metals, such as Al and Cu, can form a galvanic cell that causes electrochemical corrosion to occur in the presence of moisture. In the case where TiW is used as a barrier layer or etch stop for Al etching, enhanced corrosion can occur for similar reasons. Furthermore, it has been shown that chloride ions adhere more strongly to titanium and tungsten, making them even more difficult to remove [90]. In the application where TiW is needed as an etch stop to protect silicon, care must be taken not to etch through this layer during any postetch plasma treatment that makes use of fluorinated gases. Plasmas containing CHF_3 may be best suited for this purpose because of their higher selectivities to TiW [90].

5. Endpoint Detection

Laser interferometry and optical emission spectroscopy can be used for endpoint detection while etching aluminum and aluminum alloys [95]. Figure 31 shows an optical emission scan of a $\text{BCl}_3/\text{CCl}_4/\text{O}_2$ plasma before and during the aluminum etch process [70]. Increases in the emission intensities of etch product species, such as Al(396 and 308 nm) and AlCl (261 nm), are observed. At the same time, there is a decrease in the intensity of the chlorine reactant species (256 and 305 nm). Theoretically, any of these changes can be used for endpoint detection, but the most

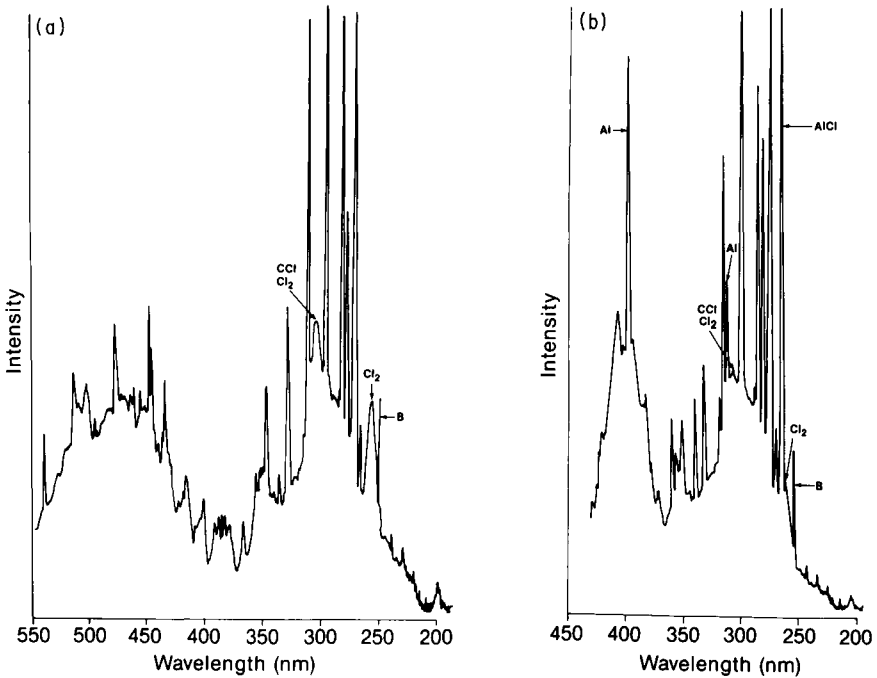


Fig. 31. Optical emission spectrum of a 75% BCl_3 , 20% CCl_4 , and 5% O_2 plasma in a reactive ion etcher: (a) before and (b) during the Al etch process.

reliable results are usually obtained with the 396-nm Al emission line, since its intensity is high and it is typically isolated from other interfering peaks in the spectrum. A representative trace while monitoring the 396 nm line is shown in Fig. 32. After the (typical) 45-sec induction period, related to the removal of aluminum oxide, there is a sharp increase in the emission intensity, followed by a decrease as the Al clears from the surface of the wafer. The double peak is indicative of a two-pass sputtering process with, possibly, a thin film of aluminum oxide at the interface.

C. Refractory Metal Etching

Due mainly to their low resistivity and high-temperature stability, refractory metals are being extensively investigated for use as gates or as interconnects [96–102]. Molybdenum and tungsten are prime candidates for gate materials because of their stability over gate dielectrics [103] and their resistivities, which are up to two orders of magnitude lower than that of doped polysilicon. As interconnect materials, most refractory metals can remain stable during subsequent high-temperature processing steps, such as dielectric depositions and metal anneals. They can also make contact to

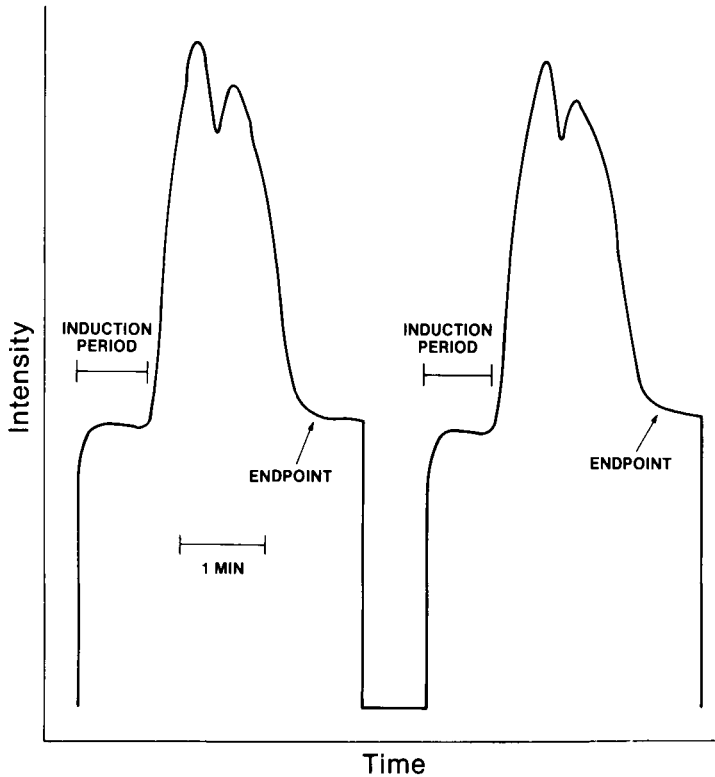


Fig. 32. Intensity versus time characteristic of the 396-nm (Al) optical emission line, while etching patterned wafers in successive runs.

silicon without spiking and can be processed free of the corrosion problems that have occasionally been observed with aluminum and its alloys. The fact that their resistivities are two to three times higher than that of aluminum does not appear to be too great a disadvantage in their use as first-level metal interconnects, since the runs are typically short in VLSI applications.

1. Etch Chemistry

The etching of refractory metals, such as Mo, W, Ti, Ta, Nb, and V, has been accomplished primarily with fluorine-containing gases. Early work was done in barrel etchers using CF_4 [104–106] and CF_4/O_2 [107–110]. Oxygen was added to CF_4 in order to enhance the formation of active fluorine species [111]. The subsequent demand for more rigorous dimensional control and the availability of new equipment have led to the development of planar plasma (PPE) and reactive ion etching (RIE) processes. Pertinent references are listed in Table V.

TABLE V
Gases Used to Etch Refractory Metals

Metal	Gas	Reference(s)	Metal	Gas	Reference(s)	
Mo	CF ₄ /O ₂	[112]	W	SF ₆ /N ₂	[124]	
	CF ₄ /O ₂ ^a	[98]		SF ₆ /O ₂	[112,126]	
	NF ₃ ^a	[113,114]		CBrF ₃ /O ₂	[127]	
	NF ₃ /Ar ^a	[113,114]		CBrF ₃	[128]	
	NF ₃ /He ^a	[114]		XeF ₂	[129]	
	SF ₆	[115]	Ti	CF ₄	[125]	
	SF ₆ /Cl ₂	[116]		C ₂ F ₆	[130]	
	SF ₆ /Cl ₂ /O ₂	[116]		CBrF ₃ /O ₂ /He ^a	[131]	
	CF ₄ /Cl ₂	[117]	Ti:W	CCl ₂ F ₂ /O ₂	[116]	
	CBrF ₃	[118]		SF ₆ /Cl ₂	[116]	
	CCl ₂ F ₂ /O ₂	[116]		SF ₆ /Cl ₂ /O ₂	[116]	
	CCl ₄ /O ₂	[119–121]		CCl ₄ /O ₂	[132]	
	Cl ₂ /O ₂	[122]	Ta	SF ₆ /O ₂	[112]	
W	CF ₄	[123,124]		Nb	CF ₄	[105]
	CF ₄ /O ₂	[112]		V	C ₂ F ₆	[130,133]
	CF ₄ /N ₂	[124]				
	CHF ₃	[125]				

^a Planar plasma etching. All others reactive ion etching.

Some of the results of Mo etching experiments using Cl₂F₂/O₂ in an RIE system are shown in Fig. 33 [116]. The etch rate of Mo increases as oxygen is added to CCl₂F₂. Molybdenum can form volatile fluorinated species (MoFn), oxyfluorides (MoOF_n), and oxychlorides (MoOCl_n). Anisotropic etching can be obtained with this mixture if the pressure is kept below 100 mTorr [116].

Anisotropic molybdenum etching can also be accomplished by using a mixture of SF₆ and Cl₂ (Fig. 34). The addition of 10–15% Cl₂ in SF₆/Cl₂ was found to increase the etch rate of Mo and reduce linewidth losses. These results are similar to those that were observed during polysilicon etching [134]. The etch rate of Mo and the selectivity of Mo to photoresist were found to increase by almost a factor of two by adding oxygen to SF₆/Cl₂ (Fig. 35). Emission spectroscopy showed that the relative intensity of the F atom signal and the etch rate of Mo, first increase with O₂ additions and then decrease. Both atomic fluorine and oxygen contribute to the degradation of organic photoresist materials. In the range of 10–30% oxygen added, the etch rate of photoresist seems to depend primarily on the relative fluorine atom levels. At higher percentages of oxygen added, the photoresist etch rate is dominated by the relative oxygen atom levels. These gas mixtures have been used to etch Mo/TiW bilayer metallization systems [116]. An SEM photo showing anisotropic etching of a Mo/TiW line is shown in Fig. 36.

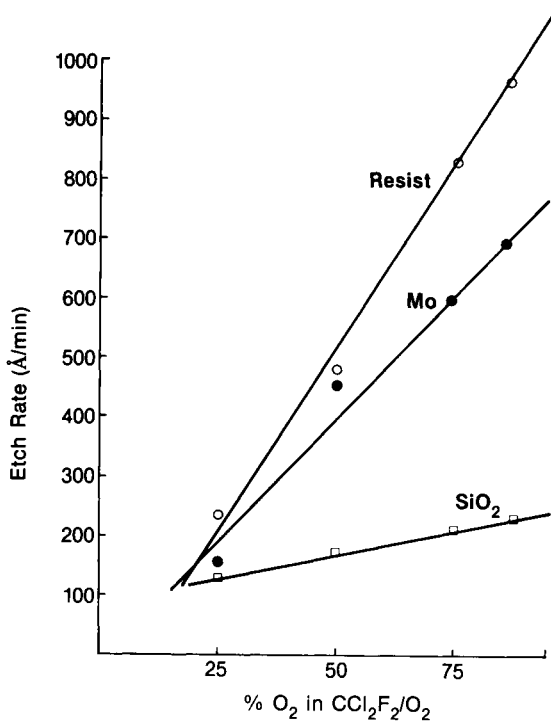


Fig. 33. The etch rates of Mo, photoresist, and silicon dioxide versus percent O₂ in CCl₂F₂/O₂. Etching parameters are flow, 60 sccm; pressure, 100 mTorr; and power, 300 W (0.25 W/cm²); and a carbon cathode cover in a reactive ion etcher.

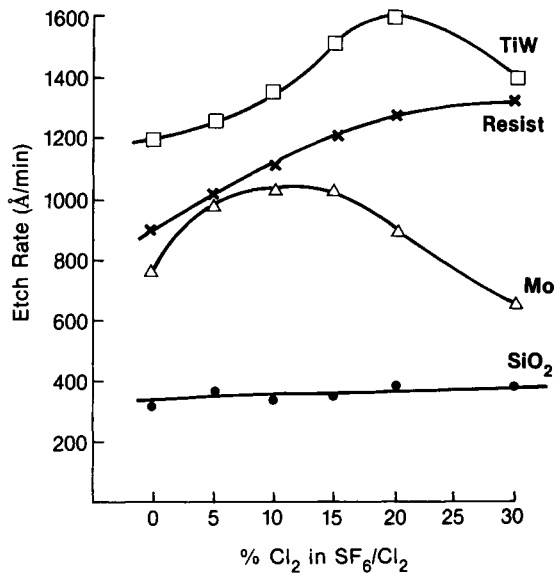


Fig. 34. The etch rates of Mo, TiW, photoresist, and silicon dioxide versus percent Cl₂ in SF₆/Cl₂. Etching parameters are flow, 30 sccm; pressure, 65 mTorr; and power, 250 W (0.21 W/cm²); and a quartz cathode cover in a reactive ion etcher.

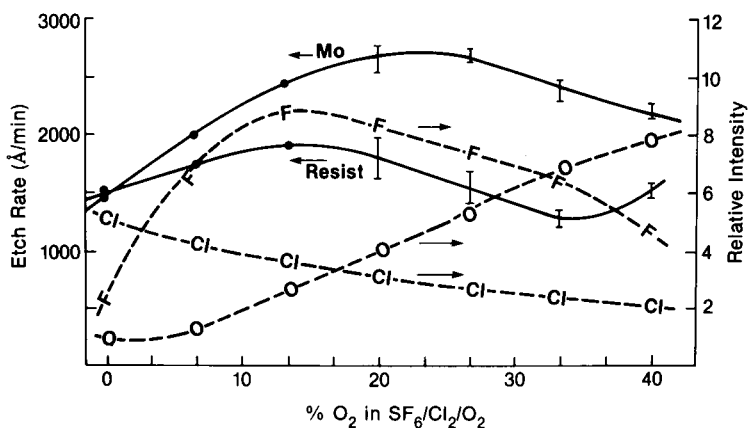


Fig. 35. Etch rates of Mo and photoresist, and relative emission signals of F (704 nm), Cl₂ (256 nm), and O (77 nm) versus percent O₂ in SF₆/Cl₂/O₂. Etching parameters are flow, 60 sccm, ratio of Cl:SF₆ of 0.17; pressure, 65 mTorr; and power 200 W (0.16 W/cm²); and quartz cathode cover in a reactive ion etcher.

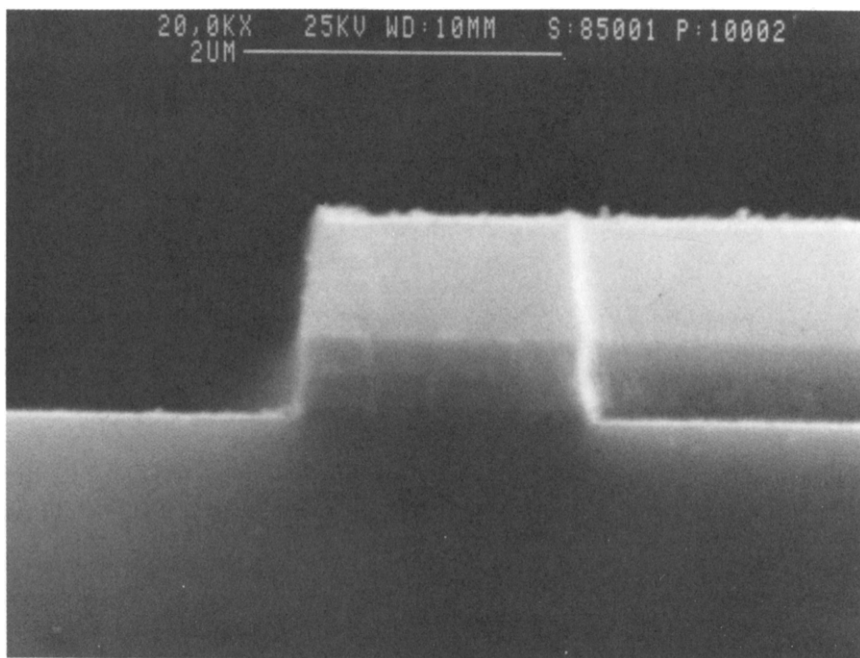
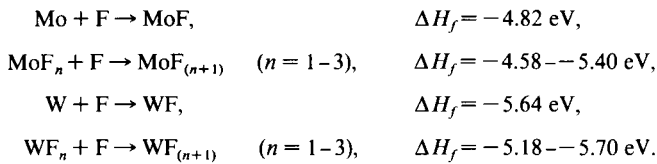


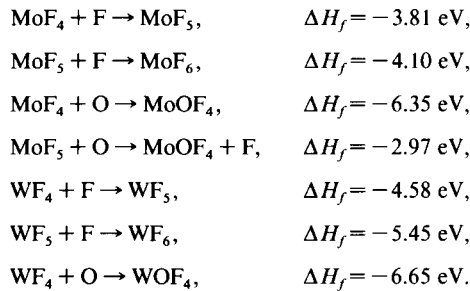
Fig. 36. SEM photo of a Mo/TiW line. Photoresist has not been removed. Etching parameters are flow, 60 sccm; 63% SF₆/11% Cl₂/26% O₂; pressure, 65 mTorr; and power 200 W (0.16 W/cm²); quartz cathode cover in a reactive ion etcher. (Courtesy of J. Norton.)

In another study, the etch rates of W, Mo, and Ta were determined as a function of SF_6/O_2 mixture composition in a reactive ion etcher [112] (see Fig. 37). Mass spectrometry during the etch process has shown that at low fractions of oxygen, WF_n , MoF_n , and TaF_n species were predominant. At high oxygen fractions WOF_n and MoOF_n were detected, but there was no indication of TaOF_n . The mechanisms proposed for etching Mo and W are similar and are described in the following [112]:

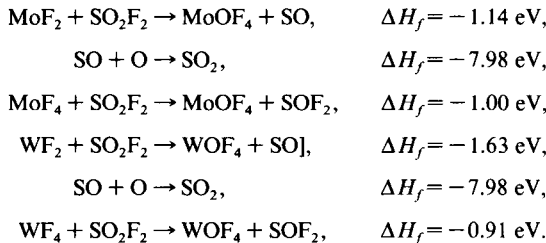
(1) Formation of fluorides:



(2) Surface fluorination or oxidation:



(3) Gas-phase or surface reactions with secondary products:



Molybdenum gate etching has also been reported in chlorine-based plasmas such as CCl_4 [119–121] or Cl_2 [122] mixed with high percentages of oxygen. The main products of etching with these gases are molybdenum oxychlorides. The etch rate of Mo in CCl_4/O_2 increases with pressure (Fig. 38), while those of silicon dioxide, silicon (24), and photoresist decrease. Selectivities of Mo to SiO_2 can be as high as 100:1, while still maintaining anisotropic etching.

The amount of oxygen in a Mo film has been shown to affect its etch rate

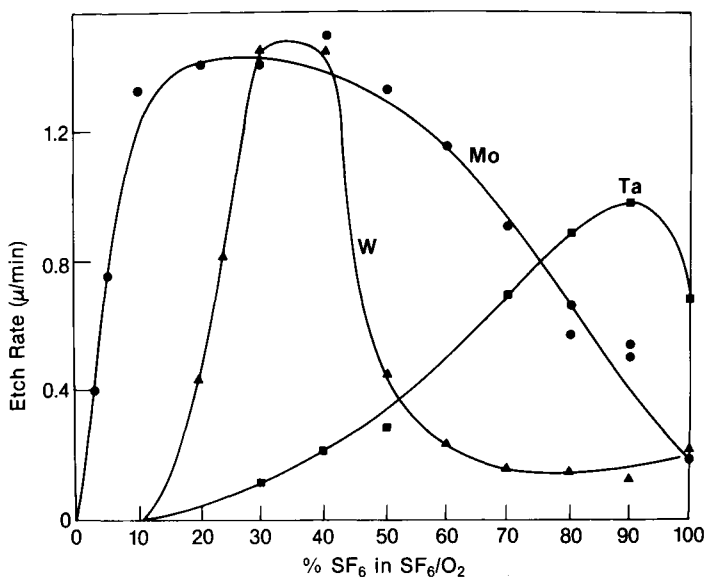


Fig. 37. Etch rates of W, Mo, and Ta, for RIE mode in a SF_6/O_2 plasma; electrode area is 12 cm^2 ; pressure, 0.2 Torr; power, 50 W; and flow, 40 sccm. (From Picard and Turban [112].)

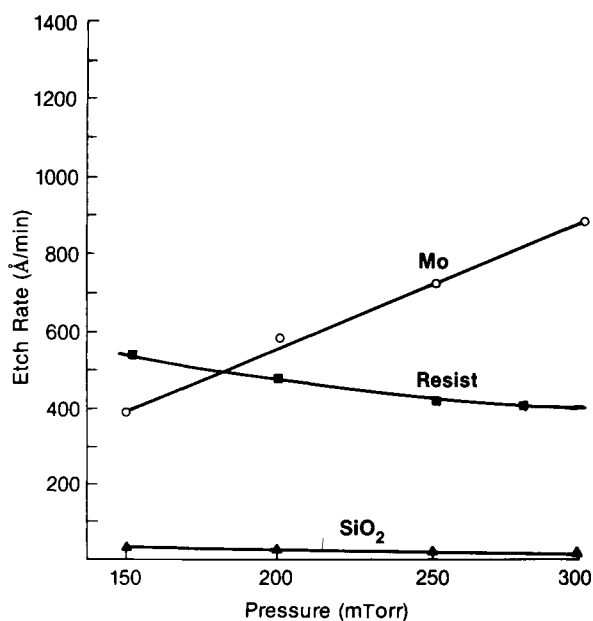


Fig. 38. Etch rates of Mo, photoresist, and silicon dioxide versus pressure in CCl_4/O_2 . Etching parameters are flow 100 sccm; 75% O_2 in CCl_4/O_2 ; and power, 300 W ($0.25 \text{ W}/\text{cm}^2$); and a quartz cathode cover in a reactive ion etcher.

in a plasma [119–121]. It is believed that when oxygen is incorporated, it aids in the formation of volatile molybdenum oxychlorides, resulting in an enhanced etch rate. Dry etching techniques for forming tapered profiles have been developed based on the isotropic etching of Mo films heavily doped with oxygen [135].

2. Endpoint Detection

Endpoint detection for refractory metal etching can usually be achieved by monitoring the optical emission lines of reactant species such as Cl_2 (256 nm) or F (704 nm). Product species of some refractory materials are not readily observable by emission spectroscopy in the range of 200 to 800 nm. Sharp endpoints, however, can also be obtained by using laser interferometry.

D. Refractory Metal Silicide Etching

Refractory metal silicides are sometimes preferred over the refractory metals as gate materials because they are generally more thermally stable. They are sometimes used alone, but are more frequently deposited or formed over polysilicon to fabricate gates. The refractory metal silicide/polysilicon structure (polycide) offers the advantages of the well-understood and reliable polysilicon/ SiO_2 interface and low resistivity.

The rapid development of the silicide technology is demonstrated by the large number of published descriptions of etching studies (see Table VI) and by extensive reviews [136,137].

The etching of a polycide structure must be done under conditions that etch both layers anisotropically. If the lower polysilicon layer etches in the lateral direction at a faster rate than the silicide layer, an overhang structure will result, and subsequent deposited layers will have poor step coverage. Without such undercutting, any discontinuous profile can also result in a local area of stress. The etching must also be selective to thin underlying gate dielectrics.

1. Etch Chemistry

Gas composition ratios have been the most critical factors in obtaining smoothly etched sidewall profiles. This was observed while etching TaSi_2 /polysilicon using SF_6/Cl_2 [138] and BCl_3/Cl_2 mixtures [139]. With BCl_3/Cl_2 the profile was reported to be a function of gas ratio, dc self-bias voltage, and even the number of wafers etched in a batch. These effects, which are shown in Fig. 39 (from Light [139]) were also observed while

TABLE VI
Gases Used for Refractory Metal Silicide Etching

	Gas	Reference(s)		Gas	Reference(s)
MoSi ₂	CF ₄ /O ₂	[143]	TaSi ₂	CF ₄ /O ₂ ^a	[154]
	CF ₄ /C ₂ F ₆	[145]		CF ₄ /O ₂	[155]
	CF ₄ /C ₂ F ₆ /O ₂	[145]		SF ₆ /Cl ₂	[138,155]
	SF ₆ /He	[146]		SF ₆ /C ₂ ClF ₅	[141]
	SF ₆ /O ₂	[147]		SiF ₄ /Cl ₂	[147,156]
	SF ₆ /CCl ₄	[148]		BCl ₃ /Cl ₂	[139]
	SF ₆ /HCl	[148]	TiSi ₂	CCl ₄ /Ar/N ₂ /H ₂ ^a	[157]
	NF ₃ /CCl ₄	[148]		Cl ₂ /H ₂ ^a	[157]
	NF ₃ /HCl	[148]		CCl ₂ F ₂ /O ₂ ^a	[158]
	NF ₃ ^a	[149,150]		C ₂ ClF ₅	[159]
WSi ₂	NF ₃ /Ar,He ^a	[149]	NbSi ₂	CCl ₂ F ₂ /H ₂	[160]
	CCl ₄ /O ₂	[121]		SF ₆ /CCl ₄	[148]
	CF ₄ /O ₂ ^a	[151]		SF ₆ /HCl	[148]
	CF ₄ /O ₂	[142,152]		NF ₃ /CCl ₄	[148]
	SF ₆ /He	[146]		NF ₃ /HCl	[148]
	SF ₆ /O ₂ ^a	[153]			
	SF ₆ /C ₂ ClF ₅	[141]			
	BCl ₃ /Cl ₂	[140]			

^a Planar plasma etching. All others reactive ion etching.

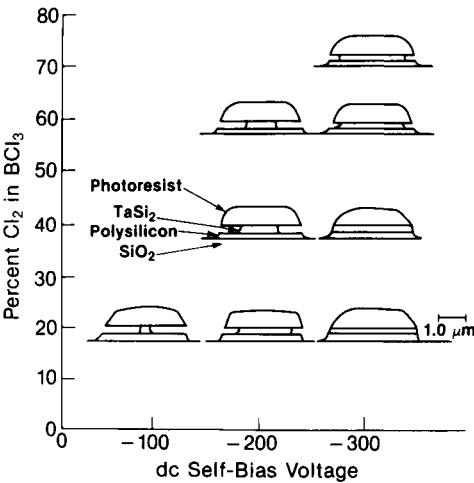


Fig. 39. The effect of percentage Cl₂ in BCl₃ and dc self-bias voltage on the profiles of polycide line. (From Light and Bell [139].)

etching WSi_2 /polysilicon with the same gases [140]. Lateral etching was more prevalent in the silicide layer than in the polysilicon.

The dependence of line profile on BCl_3/Cl_2 composition and on the number of wafers etched in a load (loading effect), was explained by a sidewall passivation model in which boron species limit the lateral etching reaction by recombining with the Cl etching species in the absence of ion bombardment. The concentration of boron-type recombinants increases with decreasing percentages of Cl_2 , or when Cl_2 in the plasma is depleted by the etching of a large number of wafers at a time [139]. The same reasoning has been applied to undercutting of Al using the same gas mixture.

Optimum sidewall profiles have been obtained using 25–50% SF_6 in a mixture of SF_6 and $\text{C}_2\text{F}_5\text{Cl}$ [141]. Some lateral etching of both WSi_2 and polysilicon was observed, but this occurred at equal rates in both layers.

While etching WSi_2 /polysilicon using CF_4/O_2 [142], a vertical profile and a 1:1 WSi_2 :polysilicon etch rate ratio were obtained with mixtures containing 30–35% O_2 in CF_4/O_2 . At higher percentages of oxygen, tapered profiles were obtained, but at the expense of a small amount of polysilicon undercutting.

The etch rate of MoSi_2 increases with increasing pressure in a mixture of

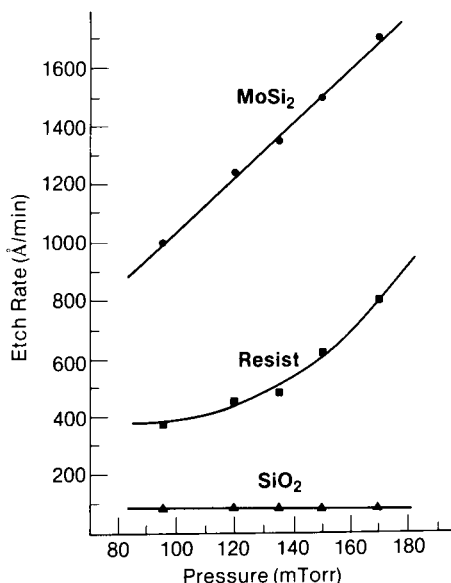


Fig. 40. Etch rates of MoSi_2 , resist, and SiO_2 versus pressure in a CCl_4/O_2 plasma. Etching parameters are flow, 100 sccm; 50% O_2 in CCl_4/O_2 ; and power, 300 W (0.25 W/cm^2); and a quartz cathode cover in a reactive ion etcher.

50% O_2 in CCl_4/O_2 , as shown in Fig. 40 [121]. A $MoSi_2$ line can be etched anisotropically at 135 mTorr, but polysilicon etches isotropically above 80 mTorr. Anisotropic etching of the polycide stack can be accomplished at 65 mTorr.

2. Endpoint Detection

Endpoint detection of refractory metals and polycide structures can be accomplished using emission spectroscopy by monitoring reactant species such as Cl (256 nm) or F (704 nm), or by laser interferometry, as shown in Fig. 41 (from Clark *et al.* [141]). Laser interferometry can distinguish the two layers in the polycide structure.

E. Etching of Bilayer Metals

As has been already pointed out in Chapter 3 by Skelly *et al.*, all of the desired properties of a metallization system suitable for VLSI applications are difficult to obtain with just one metal layer. Often, multiple layers are used in order to improve conductivity, spiking, electromigration, contact resistance, or adhesion. A second metal may also be added to serve as an etch stop material. An example of this will be demonstrated in a subsequent section describing a pillar formation process.

Bilayer metallization systems can place special requirements on the etch process. For many of the before mentioned applications, it would be desirable, for simplicity, to be able to etch the entire metallization in a single step, as is frequently done in the case of polycides. However, combinations of Al/TiW or Mo/Al are difficult to etch in one step since chlorinated gases are required for Al, and fluorinated gases are better suited for the refractory metals. Whether the etching is with one or with multiple steps,

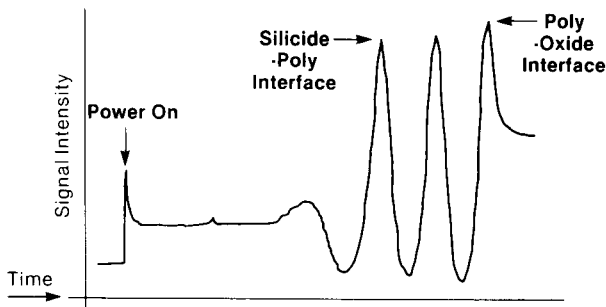
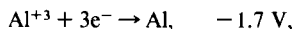


Fig. 41. Example of laser interferometer endpoint trace during the etch of tungsten polycide. The film interfaces are indicated. (From Clark *et al.* [141].)

the proper parameters must be chosen in order to provide the desired continuous edge profiles.

Platinum silicides [161,162] or TiW [163] barriers are used in combination with aluminum in order to eliminate spiking. The use of thin (300–800 Å) metal layers, such as Cr, Al [164–166], Ti [167,168], or TiW [169], inserted under Mo have been shown to improve either the ohmic contact to silicon or adhesion of Mo to silicon dioxide. Because the lower layer of metal is thin, smooth edge profiles are easier to obtain than in the case of polycide etching. Another concern however, is postetch corrosion. Such corrosion of an electrochemical nature is more likely with bilayer systems because of a self-bias driving force that can exist between layers to form a galvanic cell.

Table VII is an electromotive force (emf) series of metals [170]. Potentials between metals are determined by taking the absolute difference between their standard emf potentials. The higher the value, the greater the tendency for galvanic corrosion to occur. For example, there is a potential of 1.5 V between Mo and Al:



In this galvanic combination, since molybdenum is higher in the series, it becomes cathodic and the aluminum becomes anodic. A two step etch is needed to effectively etch a bilayer metal consisting of 5000 Å Mo over 400 Å Al [166]. The Mo can be etched, using a fluorinated gas such as SF₆ or NF₃, down to the thin Al layer. A chlorinated gas is then needed in a

TABLE VII
Standard Electromotive Force (emf) Series of Metals

	Metal–metal ion equilibrium (unit activity)	Electrode potential versus normal H electrode at 25°C (V)
↑	Au–Au ⁺	1.498
	Pt–Pt ²⁺	1.118
Noble or cathodic	Pd–Pd ²⁺	0.951
	Cu–Cu ²⁺	0.342
	Mo–Mo ³⁺	–0.200
	Cr–Cr ³⁺	–0.744
Active or Anodic	Nb–Nb ³⁺	–1.099
	Ti–Ti ²⁺	–1.630
↓	Al–Al ³⁺	–1.662

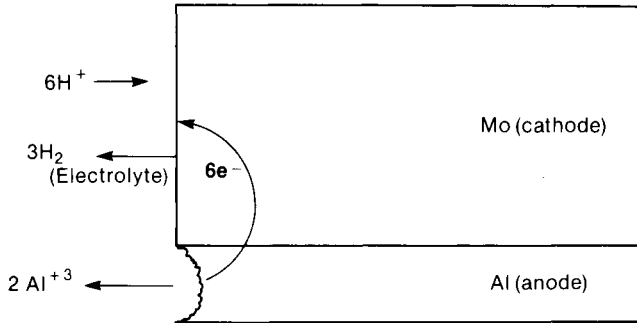
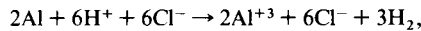


Fig. 42. Electrochemical corrosion reactions enhanced by the Mo-Al couple.

second step to etch the thin Al. The hygroscopic aluminum trichloride etch product from this step can absorb water from the room environment to form hydrochloric acid in aqueous solution (an electrolyte). The aluminum then corrodes according to the following reaction:



which is illustrated in Fig. 42. Two means of preventing this type of corrosion are to prevent the formation of the electrolyte or to passivate the Al surface. The former is the more reliable alternative for reasons already discussed in Section III.B on etching aluminum and aluminum alloys.

Electrochemical corrosion of this nature has also been observed in systems such as aluminum/copper [171], molybdenum/gold [172], tungsten/gold [173], and aluminum/titanium : tungsten.

F. Etching of Special Structures

1. Tapered Line Profiles

Most of the etching process described thus far have been designed to provide sidewall profiles that are essentially vertical. This is often necessary in order to obtain adequate linewidth control, especially with submicron dimensions. However, vertical profiles can present difficulties with respect to the uniformity of coverage by the overlying dielectric. In structures where tapered line profiles can be tolerated, step coverage can be significantly improved. The tapering of metal lines can generally be accomplished either by erosion of the mask material or by isotropic metal etching.

In one method, the photoresist profile is tapered as a result of a postexposure bake. If the metal etch conditions are chosen so that the resist and

the metal etch anisotropically, but at similar etch rates, the taper of the resist profile will be replicated in the metal. A molybdenum line tapered using this resist erosion process is shown in Fig. 43.

Under certain plasma etch conditions or resist compositions, the resist sidewall may be etched laterally at the same time that the metal is being etch anisotropically. The result is also a tapered metal line profile. This process was demonstrated with silicon dioxide using a poly(methyl methacrylate) (PMMA) photoresist mask [174] and with Mo using a PMMA mask.

Isotropic etching of the metal with undercutting of the mask material, is another method of producing tapered metal sidewalls (see Fig. 44). Care must be taken so that the profile obtained is not reentrant, but generally this is the easiest, if not the most controllable method of producing a taper.

When it is important for the etched metal sidewalls to be vertical, and step coverage of subsequent layers must be improved, most advanced processes use some form of planarization of a relatively thick layer of dielectric deposited over the metal.

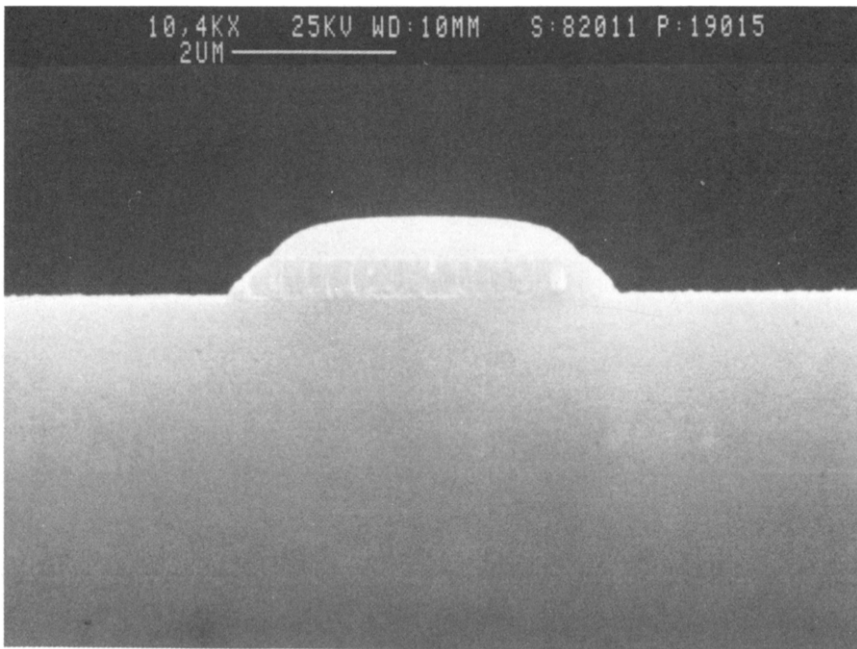


Fig. 43. SEM cross-sectional photo of a Mo line that has been tapered by etching a pretapered photoresist mask and Mo at the same rate. The photoresist has not been removed. (Courtesy of J. Norton.)

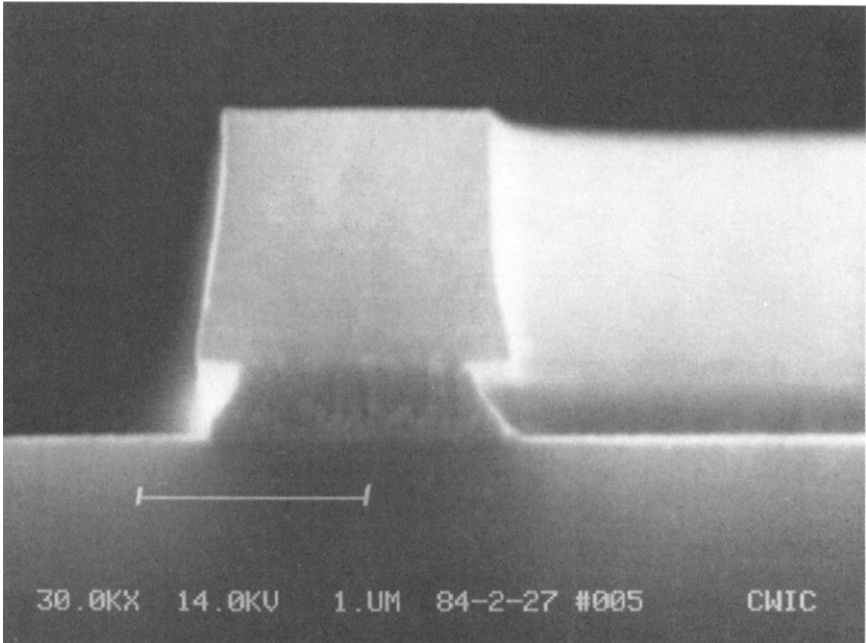


Fig. 44. SEM cross-section photo of a Mo line that has been tapered by undercutting a photoresist mask. The photoresist has not been removed. (Courtesy of J. Norton.)

2. Refractory Metal Plugs

As dimensions in VLSI circuits shrink, contact and via diameters must also be reduced. The ability to provide adequate coverage of metals into small holes, using standard sputtering techniques, can be a serious problem and even a limiting factor in the circuit design. Metals such as molybdenum or tungsten can be deposited using chemical vapor deposition (CVD), which provides nearly conformal step coverage, even in small diameter deep vias [175]. In some cases, the step coverage of these metals, using standard sputtering techniques is often much better than that which can be obtained with aluminum alloys. A drawback in using refractory metals for upper layer interconnects, however, is the fact that their higher resistivities require thicker layers and place greater burdens on etching and on step coverage by dielectrics. One solution to the problem is to use refractory metals only to fill or partially fill the vias, and to deposit an aluminum alloy film over them, followed by patterning and etching of the interconnect lines. This can be accomplished using a metal planarization scheme as outlined in Fig. 45. Nearly 100% step coverage by the overlying aluminum

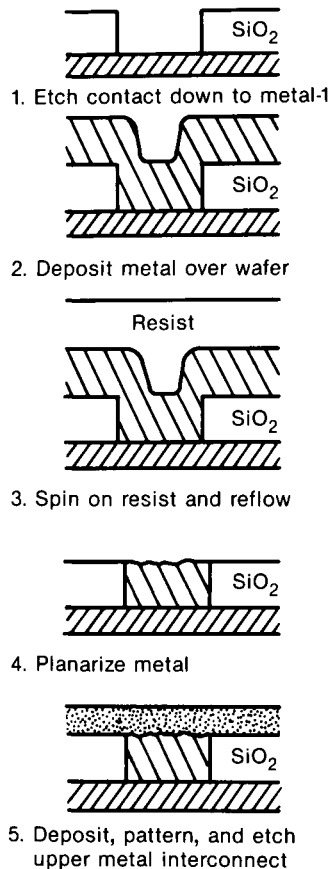


Fig. 45. Method of forming metal plugs, using a blanket metal deposition, resist planarization, and plasma etchback.

film can be obtained. The planarization is similar to the more frequently used silicon dioxide planarization in that it is performed under conditions that etch the metal and the resist at the same rate. An example of this using tungsten etched in an RIE system with $\text{CCl}_2\text{F}_2/\text{O}_2$ is shown in Fig. 46.

An even more attractive process is to use selective CVD W to fill vias [176–178]. If the vias being filled are of the same depth, and they are not overfilled, etching at this step is not necessary. Many VLSI process sequences, however, include a silicon dioxide planarization step. In this case, vias on the same wafer may vary in depth by as much as $1\text{ }\mu\text{m}$. In order to fill the deep vias, the shallow vias must be overfilled, creating a “nail-head”-type structure (see Fig. 47). The “nailheads” can also be removed by a photoresist planarization technique. An SEM photo of a selective CVD W plug after planarization etchback is shown in Fig. 48.

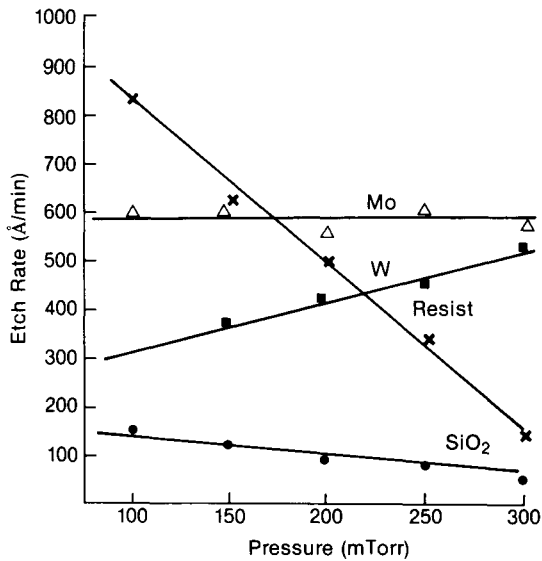


Fig. 46. Etch conditions used for W plug formation using photoresist planarization. Etch parameters are flow, 60 sccm; 75% O₂ in CCl₂F₂/O₂; and power, 300 W (0.25 W cm²); and a carbon cathode cover in a reactive ion etcher.

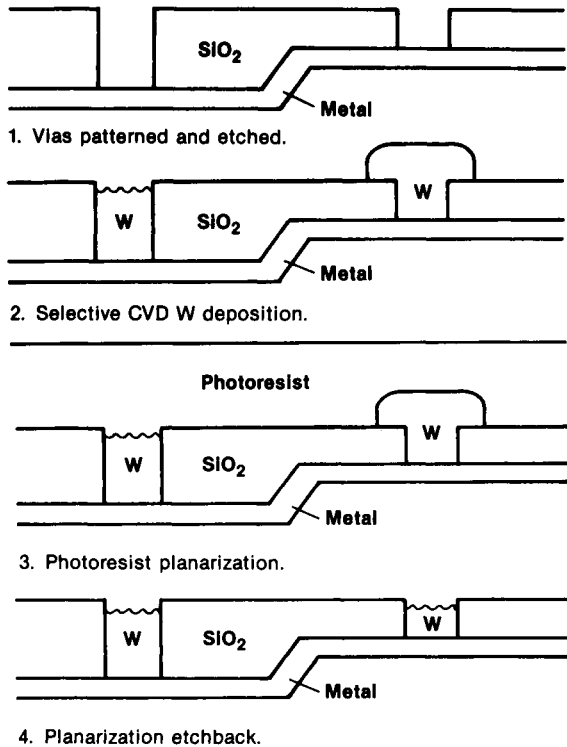


Fig. 47. Methods of forming metal plugs, using selective CVD W deposition, resist planarization, and plasma etchback.

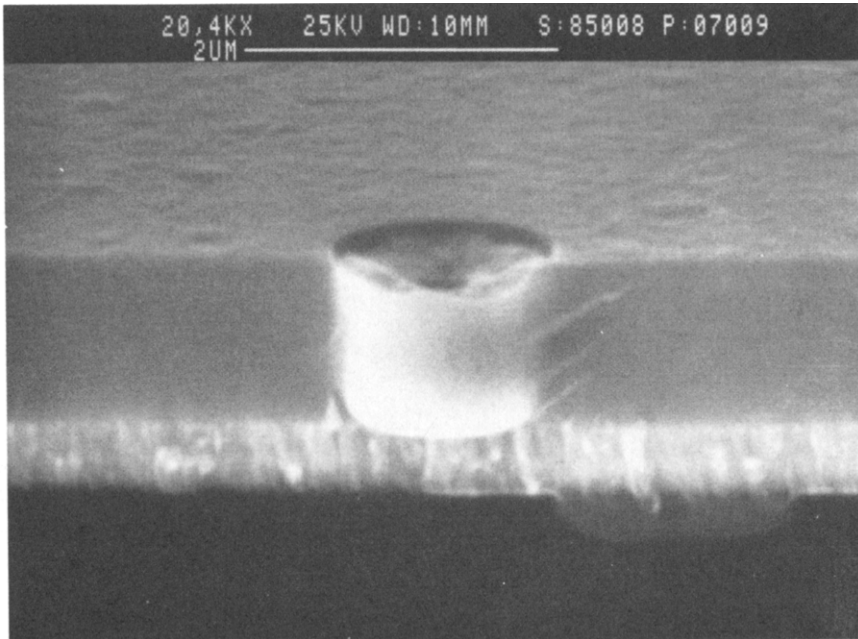


Fig. 48. SEM photo of a selective CVD W plug after planarization etchback to remove the “nailhead.” (Courtesy of J. Norton.)

3. Metal Pillars

Another method of improving the effective interconnect metal step coverage, without using valuable space on the chip, is to etch metal pillars. The scheme, which is shown in Fig. 49, eliminates via hole etching and provides a solid interlevel metal contact. This process can work well in designs, in which the distance between the upper and lower layers of metal does not vary greatly across the chip. If the pillars extend above the top of the planarized oxide layer (step 4 in Fig. 49) by excessive amounts, step coverage over them may not be adequate. Standard anisotropic metal etching techniques can be used. However, sufficient etching selectivity of the pillar material to the underlying metal or metal etch stop material is critical. The SEM photo in Fig. 50 shows an example of a Mo/Cr pillar over a Mo interconnect. Here, a thin layer of Cr, deposited under the Mo pillar serves as an etch stop. The Mo pillar can be etched selectively over Cr using $\text{SF}_6/\text{Cl}_2/\text{O}_2$. The thin (300 Å) Cr layer can then be removed in Cl_2/O_2 , or by wet etching.

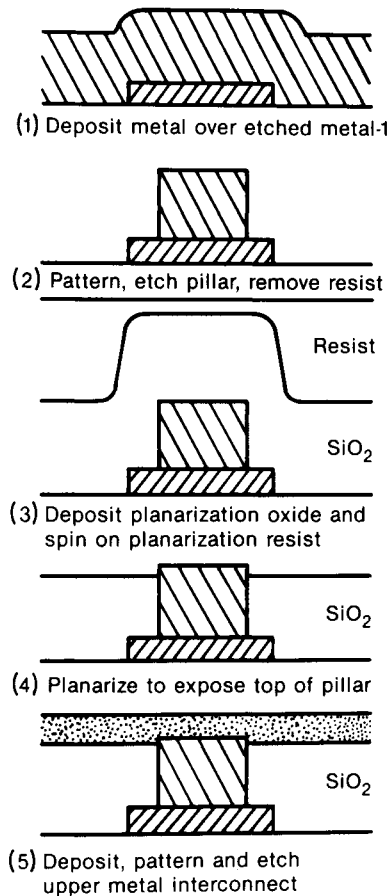


Fig. 49. Sequence used to produce metal pillars.

Another combination of metals used in a pillar process consists of Al/Cr deposited over Al interconnects [179]. In this case, the entire Al/Cr/Al stack was etched together, then cross patterned with photoresist to define the pillars. The upper layer of Al was then etched down to the Cr etch stop (see Fig. 51). With this method, alignment of the pillar to the underlying metal is not as critical, but etching of the relatively tall stack with adequate dimensional control can present difficulties.

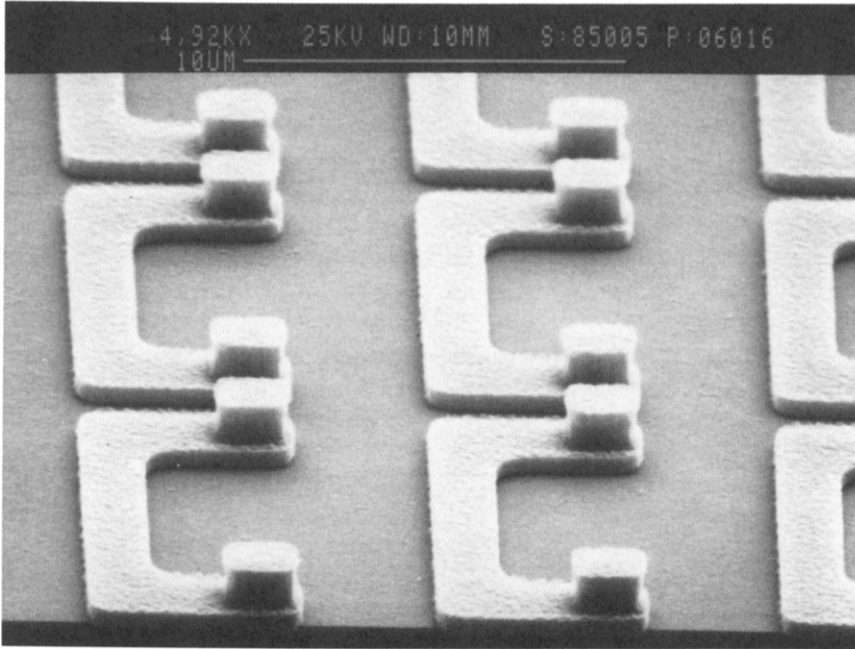


Fig. 50. SEM photo of 1- μ m-tall Mo/Cr pillars etched on top of Mo lines. (Courtesy of J. Norton.)

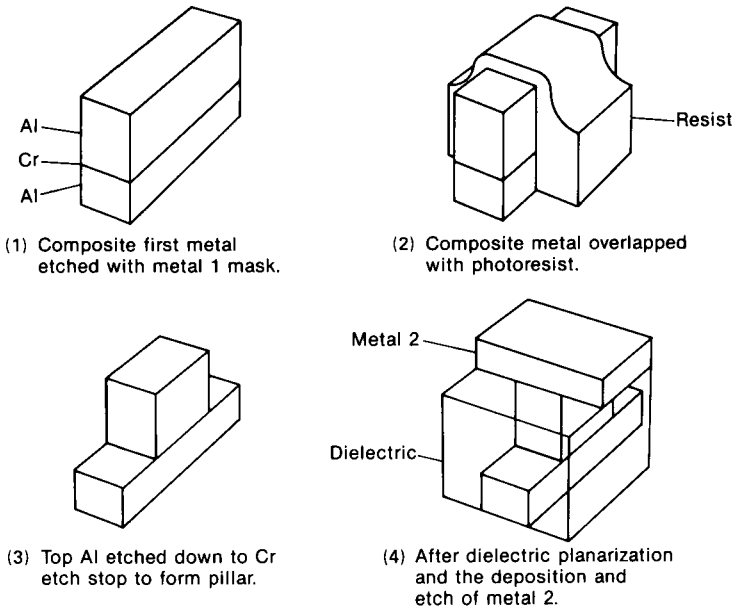


Fig. 51. Sequence used to produce Al/Cr/Al pillars using a photoresist overlap method. (Adapted from Oakley *et al.* [179].)

IV. SUMMARY

Photolithography equipment and processes are currently available for use in the patterning of metallizations suitable for VLSI applications where the critical dimensions are in excess of about $1.0\text{ }\mu\text{m}$. Improvements in equipment, photoresist materials, and the use of multiple layers and contrast enhancement materials may push the lower limits of optical lithography to the $0.5\text{ }\mu\text{m}$ or lower. At the same time, electron beam and x-ray lithography are being improved with the goal of implementing submicron processes on a manufacturing scale. Although the resolution which is sought will probably be attained, the problem of accurate alignment to underlying topography will perhaps be a greater challenge.

Dry etch techniques for pattern replication also have demonstrated capabilities in the $1.0\text{-}\mu\text{m}$ range, and there appear to be no fundamental reasons why features $0.5\text{ }\mu\text{m}$ or lower cannot be fabricated, given an appropriate resist structure. Decreasing geometries and increasing wafer sizes, however, represent a combination that will most likely require the abandonment of batch etch systems in favor of single-wafer systems. Etch rate improvements, as well as more accurate and more responsive endpoint detection and control, and greater selectivity to both resist and substrate will become more important factors in etch equipment and process development.

ACKNOWLEDGMENTS

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