

Improved bi-layer lift-off process for MEMS applications

Jinxing Liang^{a,b,*}, Fusao Kohsaka^a, Takahiro Matsuo^{a,b}, Xuefeng Li^a, Toshitsugu Ueda^a

^a *IPS, Waseda University, Kitakyushu 808-0135, Japan*

^b *Sakamoto Electric MFG. Co. Ltd., Fukuoka 811-0202, Japan*

Received 7 October 2007; received in revised form 7 January 2008; accepted 13 January 2008

Available online 21 February 2008

Abstract

Conventional lift-off process is designed for defining very fine pattern or removing metals hard to etch and the process is limited to surface microfabrication due to the requirement on directional deposition. We improved the process for the step coverage requirement in 3-D MEMS. A novel bi-layer (top image resist Shipley S1808 and bottom lift-off resist Microchem LOR) lift-off process was built up for patterning 3-D devices. Resists were coated and patterned with an overhang profile on a substrate before the substrate was etched. The key feature of the new lift-off process is to create a resist undercut profile, which is deep enough to reduce step coverage and durable to aggressive substrate etchant. The two-step development method was effective for patterning 3-D microdevices with high aspect ratio trench or through-holes. The development time of the resist profile was optimized. Fine pattern of 2 μm /5 μm (line/space) was achieved on quartz microstructure with high aspect ratio (2.7) trench.

© 2008 Elsevier B.V. All rights reserved.

Keywords: Lift-off; 3-D patterning; Two-step development method; Undercut; MEMS

1. Introduction

In traditional photolithograph process, resist needs to be coated on the sidewalls of a high aspect ratio trench or a through-hole to define a 3-D microstructure pattern. However, it is difficult to coat resist on the vertical sidewalls of high aspect ratio microstructures. Spray coating system has been reported for deep structures [1], but successful resist coating on the sidewall of a through-hole at high aspect ratio has not been found. Electroplated photoresist such as Shipley ED2100 has been recently introduced [2]. In the case of bulk etched MEMS capacitive device, however, sensitive comb electrodes in this system may stick to each other in liquid solution and hinder the photoresist plating [3]. We have built up a simple process that does not need resist coating after substrate etching.

Lift-off is a patterning technique that is widely used for defining very fine structure or removing hard-etched metals

such as platinum [4–6]. This technique needs directional deposition so it is limited to surface microfabrication. When the step coverage is required in 3-D MEMS, the lift-off process needs to be improved. A bi-layer lift-off process for new applications on 3-D patterning has been set up in our research group.

The process flow of the new bi-layer lift-off process is shown in Fig. 1. First, substrate etching pattern is defined using traditional photolithograph technique. A lift-off pattern for surface wire is then created. After the substrate and mask film A are etched, metal film B is deposited. The last step is to perform the lift-off and remove mask film A which is protected by lift-off pattern. In our previous report [7], we successfully fabricated capacitive tilt sensor using lift-off resist LOL2000. However, LOL is a thin resist, which is designed for lifting-off thin metal. For clean lift-off processing, the lift-off resist layer should be thicker than the deposited metal thickness, typically 1.2–1.3 times the thickness of the metal film for introducing lift-off solution (Fig. 2). In this 3-D patterning application, multi-layer LOL resist should be coated for increasing the lift-off resist thickness. Multi-layer coating will result in bad uniformity.

* Corresponding author. Address: IPS, Waseda University, Kitakyushu 808-0135, Japan.

E-mail address: liang@kyushu.rise.waseda.ac.jp (J. Liang).

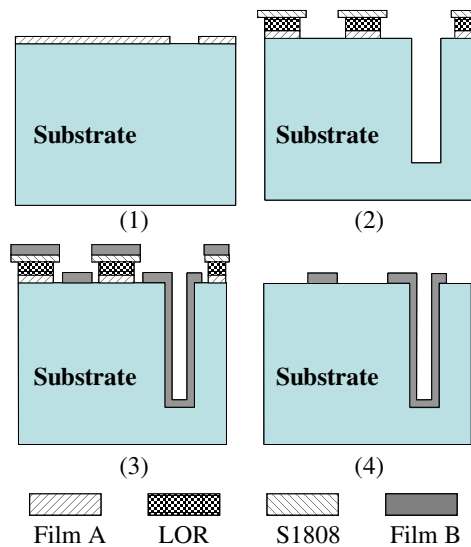


Fig. 1. Schematic diagram of 3-D patterning process: (1) patterning basic structure; (2) creating lift-off pattern and etching substrate and film A; (3) depositing film B; (4) lifting-off and etching film A.

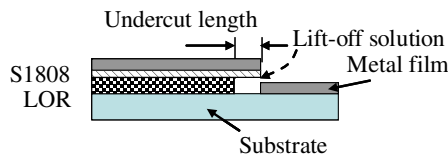


Fig. 2. Schematic diagram of undercut profile.

This research investigated the thick lift-off resist LOR for 3-D patterning and confirmed fine pattern fabrication on quartz substrate.

2. Experimental

The bi-layer process is a two-layer procedure. A layer of the lift-off resist Microchem LOR15A, which is not sensitive to UV light, is put underneath a layer of photoresist Shipley S1808. There are several variables that can be used to give the desired undercut, such as exposure, soft-bake temperature and time, developer type. In this research, we adjusted the resist development time to control and optimize the process.

2.1. Creating undercut profile

Undercut profile was created using a two-step development method. The detailed experimental flow is described as the following: (1) Z cut alpha-quartz wafer substrate was washed and sputtered with Cr/Au films; (2) lift-off resist LOR15A was spun on the quartz substrate at 4000 rpm for 30 s and then pre-baked in an oven at 150 °C for 30 min; (3) photoresist Shipley S1808 was spun at 4000 rpm for 20 s and then pre-baked in an oven at 90 °C for 15 min; (4) the substrate was exposed to UV light; (5) to investigate the undercut length, exposed substrates

were developed for 30 s, 45 s, and 60 s for the first step development; (6) the substrate was hard-baked in an oven at 150 °C for 30 min; (7) the second step development was performed for 80 s, 100 s and 120 s, respectively. All development treatments were performed in Shipley developer CD-26 solution at room temperature.

2.2. Defining 3-D pattern

High aspect ratio microstructure was fabricated by anisotropic etching Z cut quartz wafer at polar angle 45°. The fabrication of high aspect ratio microstructure on quartz was referred to our previous publication [8]. Saturated ammonium bifluoride solution at 87 °C, which is commonly used for etching quartz with an etching rate of 110 $\mu\text{m}/\text{h}$ at Z direction, was used as quartz etchant. The surface pattern was defined as 5 $\mu\text{m}/5 \mu\text{m}$, 2 $\mu\text{m}/10 \mu\text{m}$ and 2 $\mu\text{m}/5 \mu\text{m}$ at line/space, respectively. And the opening space for etching substrate was 5 μm . Corresponding to the process flow in Fig. 1, sputtered Cr/Au films were used as Film A, and Cr/Au/Cr films were used as Film B. Lift-off was performed in the Microchem remover PG solution at 60 °C for 1 h.

3. Results and discussions

3.1. Optimization of undercut

Fig. 3 shows the first step development results upon the development time from 30 s to 60 s. The ideal profile of this step is thoroughly etching the photoresist and LOR but no overhang (undercut length) because resist residue will affect the second step development. If overhang happens, the

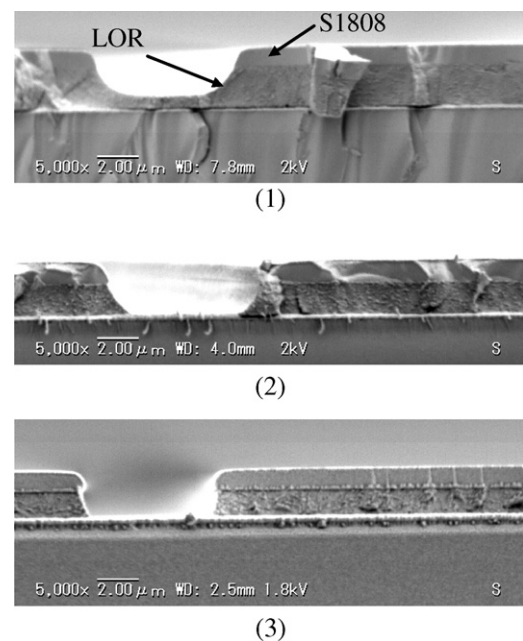


Fig. 3. SEM pictures of the cross section view after first step development. (1) 30 s; (2) 45 s; (3) 60 s.

photoresist may fall or deform during the post-development hard-bake treatment, hindering the second step development [7]. According to the results (Fig. 3), we selected 60 s as the first step development time followed by 30 min hard-bake at 150 °C in an oven. The second step development was performed from 80 s to 120 s. Fig. 4 shows the

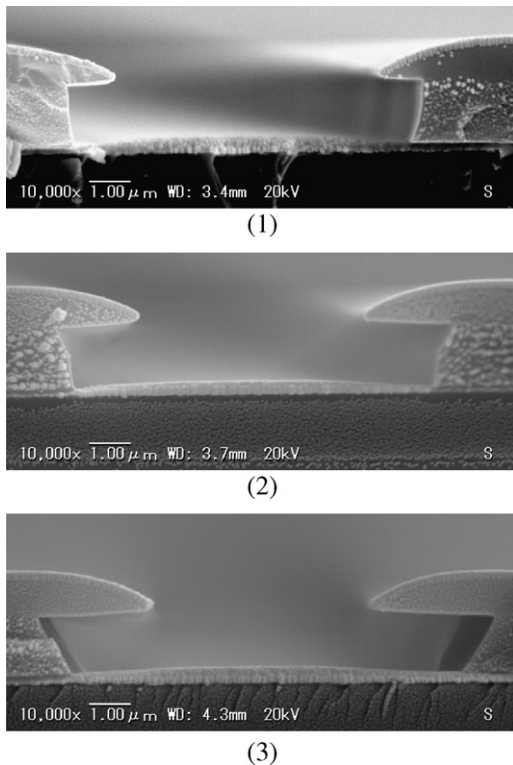


Fig. 4. SEM pictures of undercut profile after the second step development: (1) 80 s; (2) 100 s; (3) 120 s.

development results. High aspect ratio undercut ($AR = \text{undercut length} : \text{lift-off resist thickness}$) was achieved in this step. No dropping off was observed even large overhang as 1.8 μm at 120 s development. This result should be contributed by the hard-baking treatment. Generally, the larger overhang, the easier lift-off because a high aspect ratio undercut can avoid continuous metal film on and under the resist. Further the hard-baking treatment also contributes to enhance the resist performance to aggressive substrate etchant. This is the reason why we develop this two-step development method. Our previous research has demonstrated that no deep undercut can be achieved due to the dropping off by the conventional one-step development method. And the hard-baking treatment following development will destroy the overhang profile [7]. Selection of development time (undercut length) should also depend on the aspect ratio of the substrate microstructure to be coated.

3.2. Patterning 3-D microstructure

Fig. 5a shows the cross section of the 60 min etched structure with a 5 μm line and 5 μm space pattern. The aspect ratio (depth:width) of the trench was 2.7. The result demonstrated that optimized overhang structure withstood the corrosion of aggressive substrate etchant. In this experiment, the second step development was performed at 100 s. Au/Cr metal films, which were used as the substrate etching mask, were etched because these films will affect the next metal deposition on the sidewall of the trench. Fig. 5b shows the cross section of 2 μm line and 10 μm space pattern after Cr/Au/Cr metal films deposition. Lift-off removed the Cr/Au/Cr films on the resist, followed by etching the Au/Cr films underneath the lift-off resist. Desired

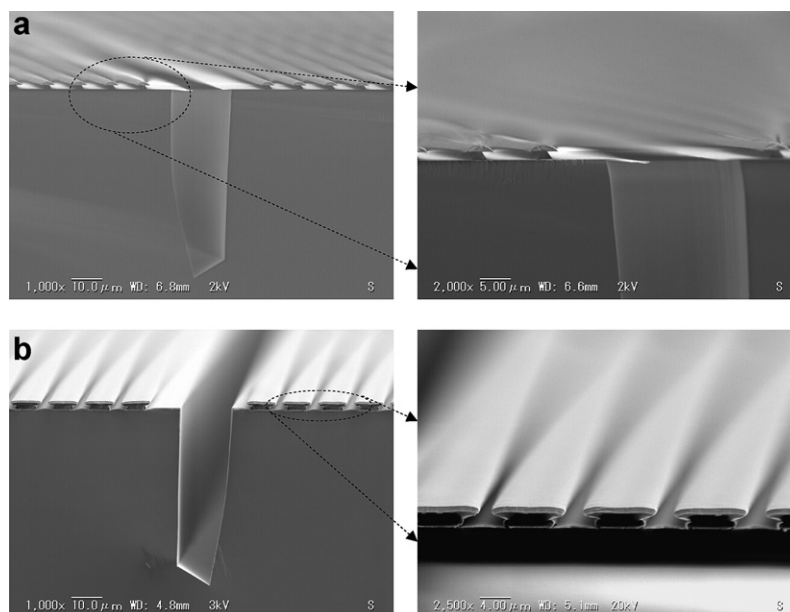


Fig. 5. Lift-off pattern on 3-D microstructure: (a) following etching quartz; (b) following sputtering metal films.

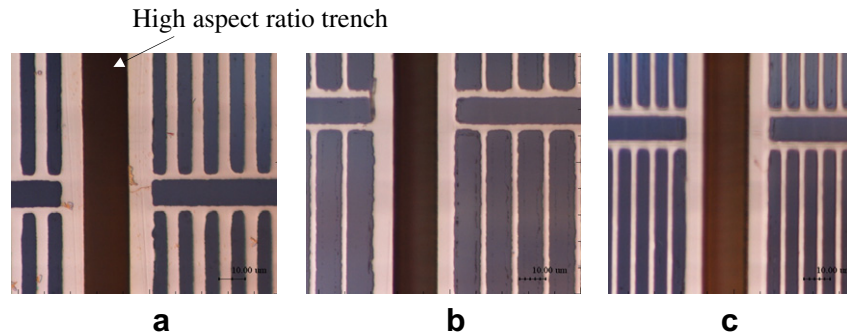


Fig. 6. Fabricated fine line/space pattern on high aspect ratio microstructure: (a) $L/S = 5\ \mu\text{m}/5\ \mu\text{m}$; (b) $L/S = 2\ \mu\text{m}/10\ \mu\text{m}$; (c) $L/S = 2\ \mu\text{m}/5\ \mu\text{m}$.

Cr/Au films were left on the surface and sidewall of the trench. Fig. 6 gives the results of successfully fabricated three kinds of patterns and the lines and spaces are $5\ \mu\text{m}/5\ \mu\text{m}$ in Fig. 6a, $2\ \mu\text{m}/10\ \mu\text{m}$ in Fig. 6b and $2\ \mu\text{m}/5\ \mu\text{m}$ in Fig. 6c, respectively. Two μm line and $5\ \mu\text{m}$ space is considered to be the finest pattern which can be achieved in this process because the hard-baking treatment would reduce the pattern resolution and minimum $2\text{--}3\ \mu\text{m}$ wide LOR resist is needed to support the upper photoresist.

3.3. Prospective applications

Improved lift-off process was used for fabricating quartz-based capacitive tilt sensor. The basic principle has been introduced in our previous publication [3]. In the case of MEMS device fabrications, which are not compatible with the post-resist coating process, such as spring beam or thin film-based microelectronic device, proposed lift-off process should be simple and effective. Appropriate LOR resist should be chosen depending on the aspect ratio of the microstructures in the device and the thickness of metal films. LORs are available in film thickness from $30\ \text{nm}$ to $4\ \mu\text{m}$. However, thicker LOR means worse pattern resolution because high aspect ratio undercut is needed for reducing step coverage. Limited by our sputtering system, we used Cr/Au films as metal A and Cr/Au/Cr films as metal B. Completely different metal A and metal B are preferable.

4. Conclusions

Lift-off process was improved for patterning 3-D microdevices. The resist pattern for lift-off is created before etching substrate, and the resist pattern should be hard enough to withstand the aggressive substrate etchant.

And the undercut should be deep enough to reduce the step coverage which is required by the 3-D microdevice. We developed a two-step development method for creating a high aspect ratio undercut and resistive overhang. The overhang was optimized and controlled by the development time. Based on this idea, fine patterns as line/space at $5\ \mu\text{m}/5\ \mu\text{m}$, $2\ \mu\text{m}/10\ \mu\text{m}$ and $2\ \mu\text{m}/5\ \mu\text{m}$ on the surface with metal films on the sidewall of high aspect ratio trench ($AR = 2.7$) were achieved on quartz wafer. A quartz MEMS-based capacitive tilt sensor was successfully fabricated using the developed process. Developed process might be used in other 3-D microdevice fabrication.

Acknowledgements

This research was supported by ‘2006–2007’ Consortium R&D Projects for Regional Revitalization’ of Ministry of Economy, Trade and Industry.

References

- [1] V.K. Singh, M. Sasaki, K. Hane, M. Esashi, *Jpn. J. Appl. Phys.* 43 (2004) 2387.
- [2] J. O’Brien, P.J. Hughes, M. Brunet, B. O’Neill, J. Alderman, B. Lane, A. O’Riordan, C. O’Driscoll, *J. Micromech. Microeng.* 11 (2001) 353.
- [3] F. Kohsaka, J. Liang, T. Matsuo, T. Ueda, *IEEJ Trans. SM* 127 (2007) 431.
- [4] R.M. Halverson, M.W. MacIntyre, W.T. Motsiff, *IBM J. Res. Develop.* 26 (1982) 590.
- [5] G.G. Collins, C.W. Halsted, *IBM J. Res. Develop.* 26 (1982) 596.
- [6] Y. Chen, K. Peng, Z. Cui, *Microelectron. Eng.* 73–74 (2004) 278.
- [7] J. Liang, F. Kohsaka, T. Matsuo, T. Ueda, in: *The 5th IEEE Conference on Sensors, EXCO*, Daegu, Korea, October 22–25, 2006, p. 394.
- [8] J. Liang, F. Kohsaka, T. Matuo, T. Ueda, *IEEJ Trans. SM* 127 (2007) 337.