

Performance of AlGaIn/GaN High-Electron Mobility Transistors With AlSiN Passivation

Ekaterina Harvard, Richard Brown, and James R. Shealy

Abstract—The performance of AlGaIn/GaN high-electron mobility transistors that were passivated with AlSiN and SiN and fabricated side by side has been studied. It is found that the AlSiN passivation produced state-of-the-art devices, improving both small- and large-signal performance over the SiN passivation, particularly at higher drain bias. With large-signal excitation at 10 GHz, the effects of second-harmonic termination on the load pull were also studied. Significant improvements in the power-added efficiency were demonstrated.

Index Terms—GaN, microwave power FETs, MODFETs, passivation.

I. INTRODUCTION

THE AlGaIn/GaN high-electron mobility transistor (HEMT) has been studied for its high-power handling capability and applications in microwave sources and power amplifiers, as well as monolithic microwave integrated circuits MMICs [1]–[4]. State-of-the-art devices have delivered more than 30 W/mm of output power at 8 GHz [5], 16 W/mm at 10 GHz [6], and 10 W/mm at 40 GHz [7]. Devices with short gate lengths (30 nm) have shown cutoff frequencies (f_T) of 180 GHz [8]. Furthermore, high-efficiency amplifiers have been produced with power-added efficiency (PAE) exceeding 75% [9].

Surface passivation has been shown to play a key role in reducing surface trapping and dispersion in the channel [10]. However, this layer increases the gate-source capacitance (a key parasitic) and creates a resistive shunt in both the gate-source and gate-drain circuits. Thus, a dielectric that adequately passivates the surface without creating large parasitic resistances and capacitances would be ideal. This paper presents a comparison between two passivation materials, SiN and AlSiN, on side-by-side fabricated devices. Each dielectric was deposited by a high-temperature low-pressure chemical vapor deposition (LPCVD) process to a thickness of roughly 30 nm, producing low-defect, hydrogen-free (relative to more common methods) films. AlSiN was used due to its larger bandgap and its expected lower permittivity at microwave frequencies. Comparisons of both small- and large-signal performance were carried out. For small-signal measurements, the device model and element extraction method described by Shealy *et al.* [11] was used

for extracting the device parameters. These parameters and the model were also used to predict the effects of various parasitic elements on the small-signal performance of the device, particularly the cutoff frequencies f_T and f_{max} .

A significant second-harmonic component at the output when the device was biased near pinchoff allowed for the study of the effects of harmonic loading. The theory of harmonic loading [12] has been studied in computer simulation [13] and demonstrated in many experiments. The effects of the higher order harmonics produced by the device have been documented both at the input [14] and output [15]–[20].

Theoretical analysis states that the PAE can be improved by 5%–10% by terminating the second harmonic in a short, which reflects the in-phase second-harmonic power back to the device in the opposite phase, allowing it to contribute to the fundamental power [12]. Experiments on recent devices reflect this range, where improvements of PAE of 4.1% [15] to as much as 10% [19] have been reported.

II. FABRICATION

AlSiN and SiN films were deposited in a modified LPCVD system onto etched mesa-isolated AlGaIn/GaN HEMT structures with 25-nm $\text{Al}_{0.25}\text{Ga}_{0.75}\text{N}$ barriers grown on semi-insulating SiC. Dielectric deposition was performed at 750 °C at a pressure of 2 torr, with trimethylaluminum, dichlorosilane, and ammonia as precursors. The conditions for the deposition of the SiN films were adjusted to produce low-stress slightly Si-rich films. The aluminum fraction (controlled by the trimethylaluminum flux) of the AlSiN dielectrics was measured to be ~6 at. by x-ray photoelectron spectroscopy. At a wavelength of 1 μm , the refractive index was measured to be 2.008 for AlSiN and 2.014 for SiN. A side-by-side capacitance–voltage (CV) comparison measurement provided a 2-D electron gas (2DEG) concentration of $7.5 \times 10^{12} \text{ cm}^{-2}$ in an unpassivated sample, $8.9 \times 10^{12} \text{ cm}^{-2}$ in a SiN-passivated sample, and $7.1 \times 10^{12} \text{ cm}^{-2}$ in an AlSiN-passivated sample. SiN-passivated structures had a corresponding sheet resistance of ~450 Ω/square . Ta/Ti/Al/Mo/Au source/drain and Ni/Au gate contacts were placed in windows etched using CF_4 and $\text{SF}_6/\text{BCl}_3/\text{Ar}$ reactive ion etching (RIE) chemistries, respectively, defined by electron beam lithography. A cross-sectional diagram of the HEMT structure is shown in Fig. 1.

III. MEASUREMENTS

After fabrication, the 100-, 250-, and 400- μm total gate periphery, dual-gate U-layout devices were characterized on

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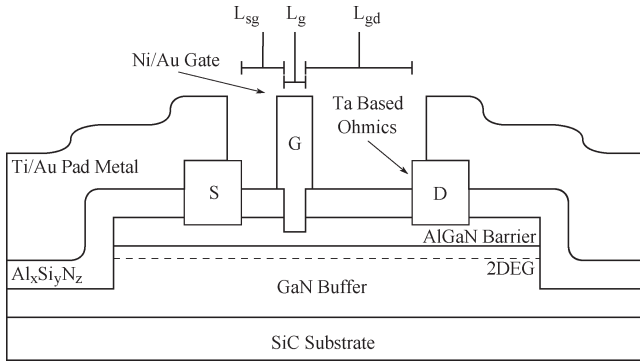


Fig. 1. Cross-sectional schematic of the HEMT structure, showing design parameters.

wafer using coplanar waveguide probes contacting Ti/Au probe pads. DC and small-signal measurements were taken, as well as large-signal measurements on a 10-GHz continuous-wave (CW) harmonic load-pull system.

The small-signal device parameter extraction measurements were taken using an HP 8510C 50-GHz network analyzer, with the DC bias supplied by an Agilent 4144B connected to the network analyzer bias tees. The combination of probes, cables, and connectors was calibrated from 500 MHz to 42 GHz using a coplanar impedance standard substrate [21].

After small-signal characterization, power measurements were performed. A schematic of the large-signal measurement system is given in Fig. 2. The 10-GHz signal was generated by an Agilent 83650 CW generator and then amplified by a 10-W amplifier. Bias was provided by an Agilent 4142B source measure unit (SMU) through bias tees at the input of the input tuner and the output of the fundamental output tuner. Maury MT982 mechanical tuners were used as the input and fundamental output tuners, and one MT983 tuner was used for the second-harmonic output. The fundamental- and second-harmonic outputs signals were separated by a diplexer with a measured insertion loss of 0.21 dB. The fundamental output signal was attenuated by a 30-dB attenuator after the output tuner. The input and reflected signals were measured with an Agilent E4417A dual-channel power meter. A second Agilent E4417 was used to measure the fundamental and second-harmonic output powers. The bench was calibrated using an HP 8510C 50-GHz network analyzer. Each section of the setup, starting with each path in the directional coupler, was separately calibrated by measuring the S-parameters. This approach would allow us to later transform the signal to the device plane.

The first step of the matching process was setting the source impedance. The goal was to create a conjugate match to allow maximum power transfer from the source to the device. Therefore, the reflected power should be minimized. The matching was done by first scanning the input tuner slide over the range of a wavelength to find the point where the reflected power was at a minimum. Then, the slide was scanned, and again, the point of minimum reflected power was taken. To verify a conjugate match, the connection was broken between the output of the input tuner and the input probes. Keeping all other connections, the one-port S-parameters were measured for the input into the device using the input probes, with the

output of the input tuner looking backward toward the source. These two sets of S_{11} -measurements were transformed to the device plane and mapped on a Smith chart (see Fig. 3). A conjugate match at the output was measured in a similar fashion by breaking the connection at the output probe and measuring the S_{11} -parameters looking into the output side of the device and the input side of output branch (see Figs. 4 and 5). The effectiveness of the match is demonstrated by a power sweep (see Fig. 6). Because the matching was done at a fixed drive (fixed P_{in}), we should expect that the match at that particular drive is at its best. This condition is observed in the figure as a notable drop in reflected power at the tuning drive.

The load impedance is usually set by the application, because the optimum tuning points for power, PAE, or gain may be different for the same device. In this case, the devices were tuned for the maximum PAE. The output tuner was scanned in the same manner as in the input tuner, except that the point of peak efficiency was used instead of the reflected power. Last, the load impedance of the second harmonic was set by scanning and optimizing the second-harmonic tuner for the maximum PAE. The device and second-harmonic branch S_{11} -parameter are shown in Fig. 5. Note that, at the device plane, the second-harmonic branch does not appear as a short, because although the tuner calibration at that point shows a short, when transformed through the intervening components (i.e., diplexer, cables, and probes), the whole branch is not.

IV. RESULTS

A. Small-Signal and DC Results

The pinchoff voltages of the SiN- and AlSiN-passivated devices were approximately -2.5 and -1.5 V, respectively, whereas the as-grown pinchoff was -4 V. This result indicates that the barrier layers were recessed by the gate window etch by differing amounts. Fig. 7 shows the pinchoff voltages measured for both types of passivation as a function of gate length. The quiescent voltage was chosen as the point of maximum transconductance for all devices. The DC-IV output curves for two devices with $250\text{-}\mu\text{m}$ -periphery and $0.15\text{-}\mu\text{m}$ gate length are shown in Fig. 8. With the gate forward biased at 2 V, the AlSiN-passivated device had a knee voltage of 3.4 V, whereas the SiN-passivated device had a knee voltage of 2.8 V. The maximum drain current at $V_g = 2$ V and $V_d = 10$ V was 209 mA for the AlSiN-passivated device and 218 mA for the SiN-passivated device. The inverse of the drain current with respect to the drain current is shown in Fig. 9. The upturn at the low drain bias visible for the AlSiN-passivated device corresponds to the measured increase in access resistance, which will be discussed later.

1) *Parameter Extraction:* The parameter values were obtained using the small-signal model extraction method as described by Shealy *et al.* [11] based on the Tasker and Hughes model [22]. The parasitic elements were extracted by biasing the devices at two operational extremes, approximating either a short or open circuit, which allows for the extraction of capacitive and inductive elements. The extraction was carried out over a range of biases, and the values in the bias-independent regions were used.

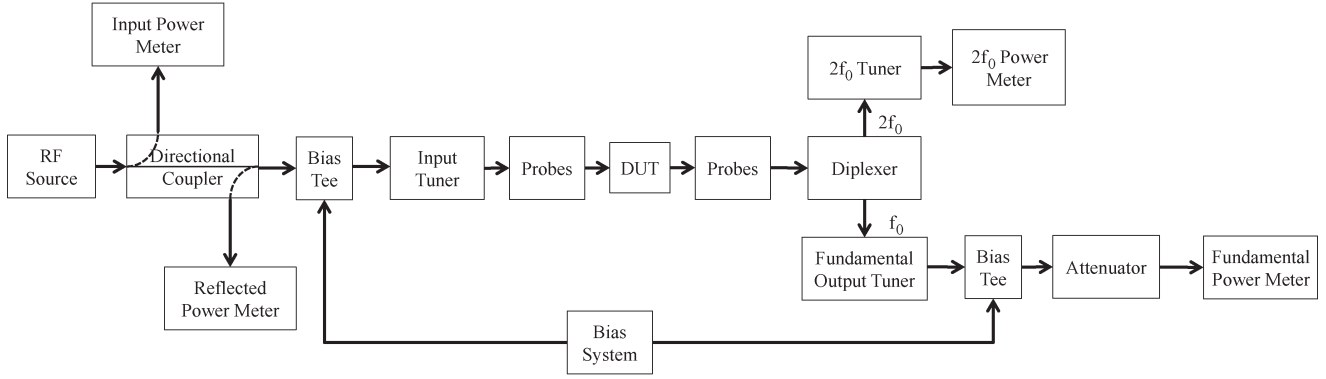


Fig. 2. Schematic of the large-signal power bench featuring a low-loss diplexer to separate the 10- and 20-GHz components of the output signal.

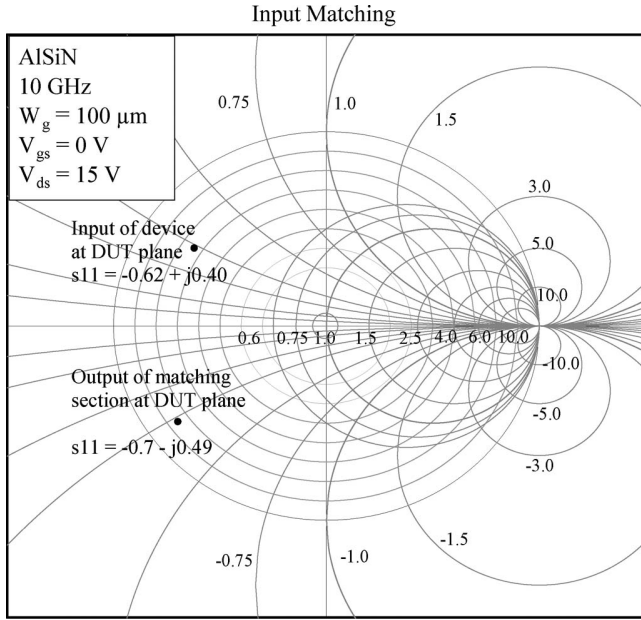


Fig. 3. S_{11} parameter looking into the device input and looking back into the input tuning network with a device with a 100- μm gate periphery and a 0.25- μm gate length.

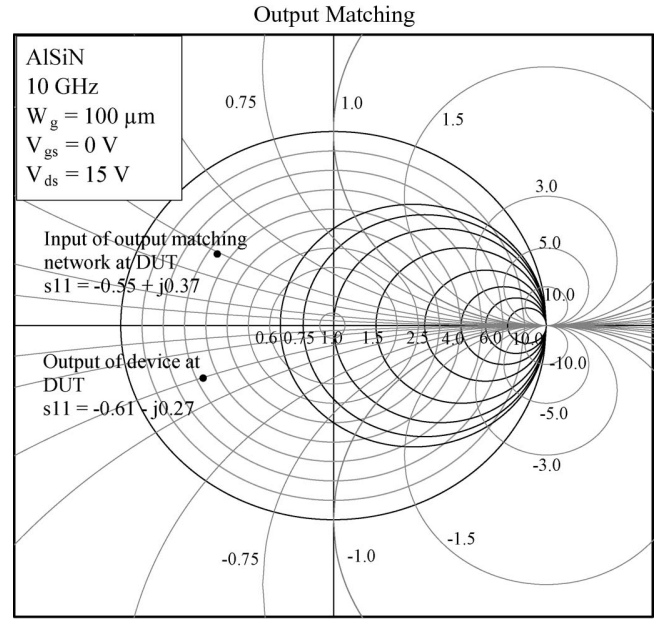


Fig. 4. S_{11} parameter looking into the device output and into the output tuning network with a device with a 100- μm gate periphery and a 0.25- μm gate length.

Devices with both types of passivation showed trends similar to previous work [11]. For both passivation schemes, small-periphery devices exhibited lower parasitic capacitances but higher series parasitic resistances. Gate resistance scaled inversely with gate length.

2) *Performance of Dielectrics*: Several significant differences in the small-signal performance of the two dielectrics were observed. In particular, lower values for several key parasitics were observed for the AlSiN-passivated devices.

The access (source and drain) resistances were found to be comparable for both AlSiN- and SiN-passivated devices under standard extraction conditions. To observe the changes in access resistance with the drain current, the gate voltage was swept from pinchoff into forward bias, and the resistance values were extracted at each point. For both SiN and AlSiN, the drain resistance was bias independent. However, the source resistance was found to nonlinearly increase with the drain current in the SiN-passivated devices. This effect is attributed to large longitudinal electric fields in the source-gate region [23]. As

shown in Fig. 10, the AlSiN-passivated devices did not exhibit this behavior, because both the source and drain resistances remained more or less bias independent.

Another set of key parasitics that showed significant differences between the two passivation materials was the pad capacitance. Fig. 11 shows the gate-drain pad capacitance for various periphery devices. The increase in periphery is due to the physically larger structure of the metal pads.

The AlSiN-passivated devices had consistently lower values across all peripheries. As will further be discussed, the gate-drain and gate-source pad capacitances affect or limit the f_T and f_{max} of the device.

3) *Figures of Merit*: The maximum value of the extrinsic f_T recorded was 87 GHz, and the maximum value of the extrinsic f_{max} was 150 GHz. The f_T was optimized at a gate length of 75 nm, and f_{max} was optimized at a gate length of 200 nm. The AlSiN-coated devices consistently had roughly 10% higher values of these device bandwidth metrics for the same gate dimensions. This condition is attributed to the reduction of key parasitics. Figs. 12 and 13 show the trends of the extracted

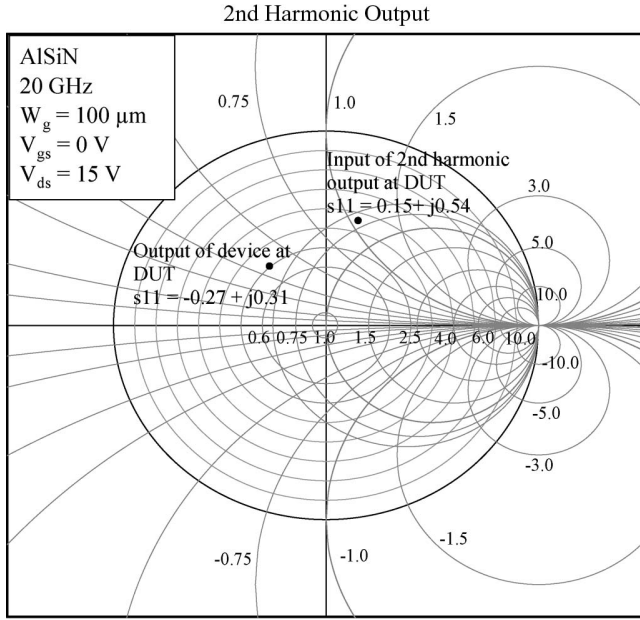


Fig. 5. S_{11} parameter looking into the output of the device and into the second harmonic tuning network with a device with a 100- μm gate periphery and a 0.25- μm gate length.

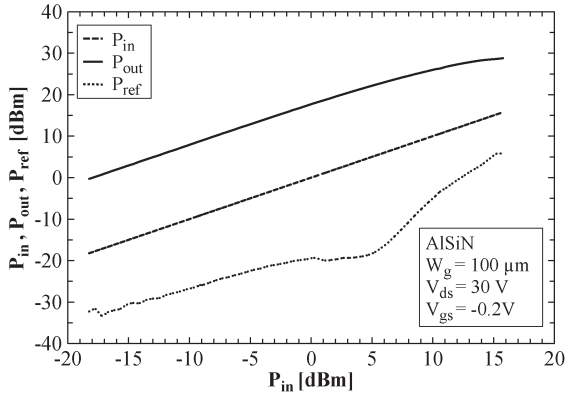


Fig. 6. Input, output, and reflected power with drive.

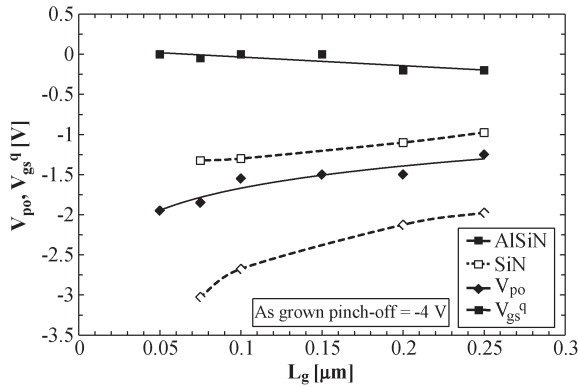


Fig. 7. Pinchoff and quiescent voltages of AISiN- and SiN-passivated devices.

intrinsic f_T and f_{max} with gate dimensions for AISiN-passivated devices. The intrinsic f_{max} maximized at the same gate length of 200 nm was 202 GHz for a 100- μm gate periphery. However, intrinsic f_T maximizes at gate lengths of 100 or 150 nm.

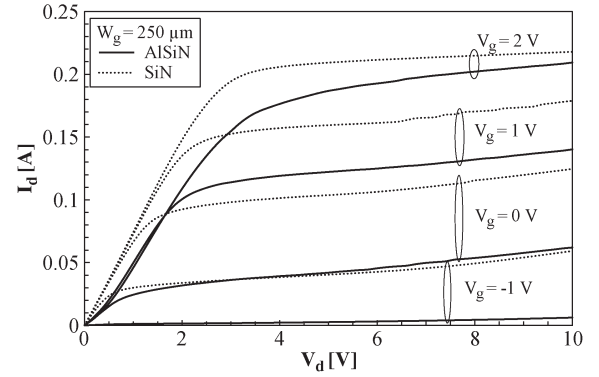


Fig. 8. DC drain current for two devices with a 0.15- μm gate length and a 250- μm periphery.

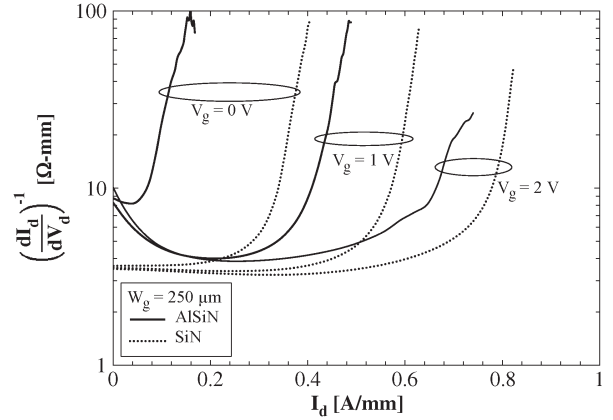


Fig. 9. Inverse of the derivative of the drain current with respect to drain current for two devices with a 0.15- μm gate length and a 250- μm periphery.

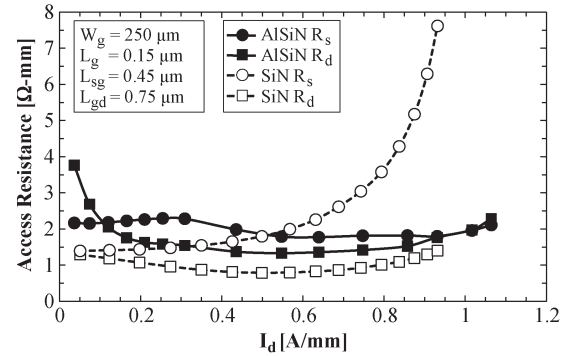


Fig. 10. Behavior of extracted access resistance as a function of the drain current for devices of both passivation schemes. The SiN-passivated devices exhibit significant nonlinearity at high drain currents.

Furthermore, there is a clear trend of increasing f_{max} with decreasing periphery, which can be attributed to decreasing parasitic capacitances and, more notably, the output conductance. The equation for f_{max} [22] may be reduced to the following simple form:

$$f_{\text{max}} \sim \frac{1}{\sqrt{4G_{\text{ds}}R_{\text{in}}}}$$

where $R_{\text{in}} = R_{\text{s}} + R_{\text{g}} + R_{\text{gs}}$. Based on the extracted values of these elements, we observed that G_{ds} dominates the term, because it strongly scales with periphery, dominating R_{in} , which

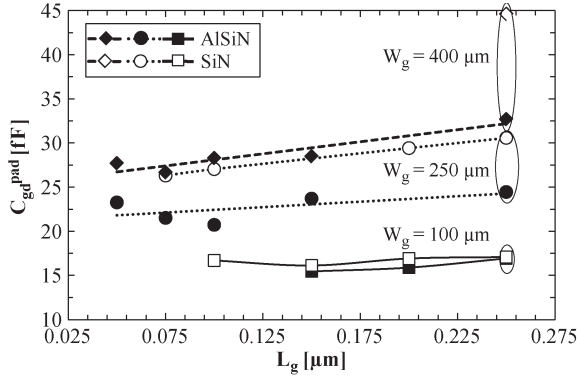


Fig. 11. Extracted gate-drain pad capacitance plotted against gate length and periphery.

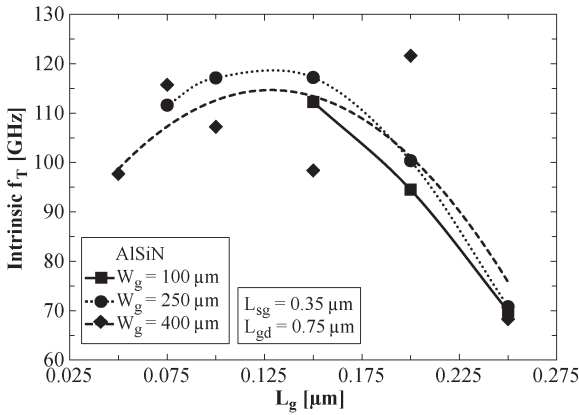


Fig. 12. Intrinsic f_T extracted against device gate length. As the gate length decreases, the cutoff frequency increases to an optimum at a length of around 100 or 150 nm, beyond which the performance of the device begins to deteriorate.

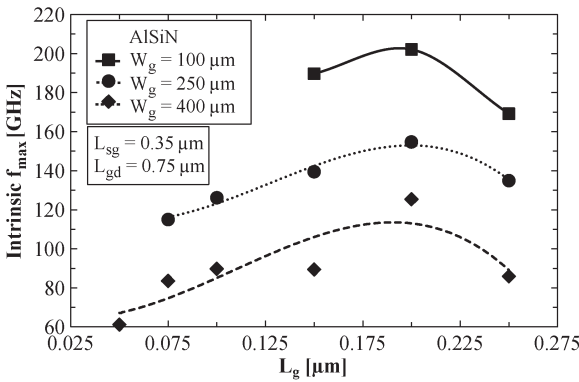


Fig. 13. Intrinsic $f_{\max}$ extracted against device gate length. As the gate length decreases, the frequency increases to an optimum at a length of 200 nm.

only slightly scales. For a gate width of 50 μm , we predict an intrinsic $f_{\max}$ of approximately 260 GHz (see Fig. 14).

To simulate the relative effects of individual parasitic elements, the value of the element was swept from zero to its extracted value, and the intrinsic device simulation was run at each step. It was found that the gate-drain pad capacitance has a significant effect on both the f_T and $f_{\max}$. The f_T is also strongly affected by the gate-source pad capacitance and source resistance, although as periphery increases, the gate-source

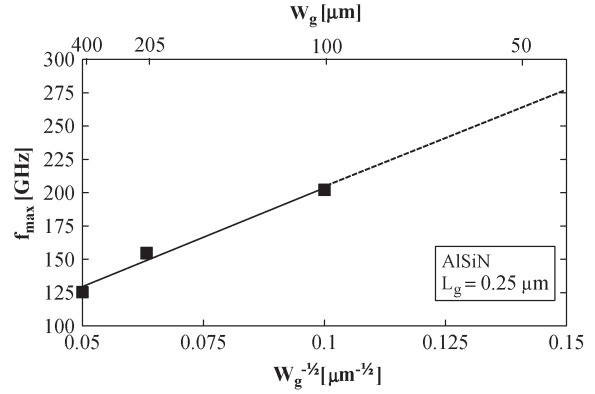


Fig. 14. Intrinsic $f_{\max}$ plotted versus inverse gate periphery.

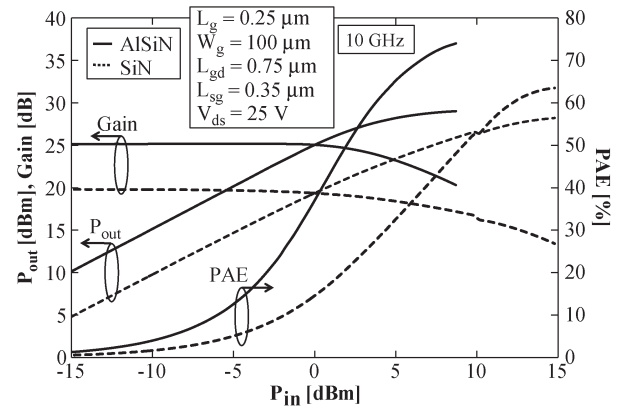


Fig. 15. Gain, output power, and power-added efficiency as functions of input power for devices with a 100- μm gate periphery and a 0.25- μm gate length for both passivation schemes.

capacitance has an increasingly dominant effect. For example, an f_T of 66 GHz was extracted for an AlSiN-passivated device with a gate length of 0.15 μm and a periphery of 100 μm . The f_T was simulated to increase to 83 GHz by zeroing the gate-drain pad capacitance alone and increase to 91 GHz by zeroing the gate-source pad capacitance alone. Zeroing the source resistance alone increased the f_T to 74.5 GHz. For a device with a 0.15- μm gate length and a 250- μm periphery, the f_T increased from 69 GHz to 102 GHz with the removal of the gate-drain pad capacitance alone and 136 GHz with the removal of the gate-source pad capacitance alone. Zeroing the source resistance alone increased the f_T to 93 GHz. The $f_{\max}$ is affected by the output conductance, and for smaller peripheries, the gate-drain pad capacitance dominates the decrease in $f_{\max}$, but the effects of the gate resistance and output conductance increase with increasing gate periphery. For a device with a 0.25- μm gate length and a 100- μm periphery, the extracted $f_{\max}$ of 125 GHz increased to 262 GHz with the elimination of the gate-drain pad capacitance, but just 136 GHz with the elimination of the gate resistance, and no change was observed with the elimination of the output conductance. However, a device with a 250- μm periphery saw an increase in $f_{\max}$ from 66 GHz to 87 GHz without the gate-drain pad capacitance, 80 GHz without the gate resistance, and 86.6 GHz without the output conductance.

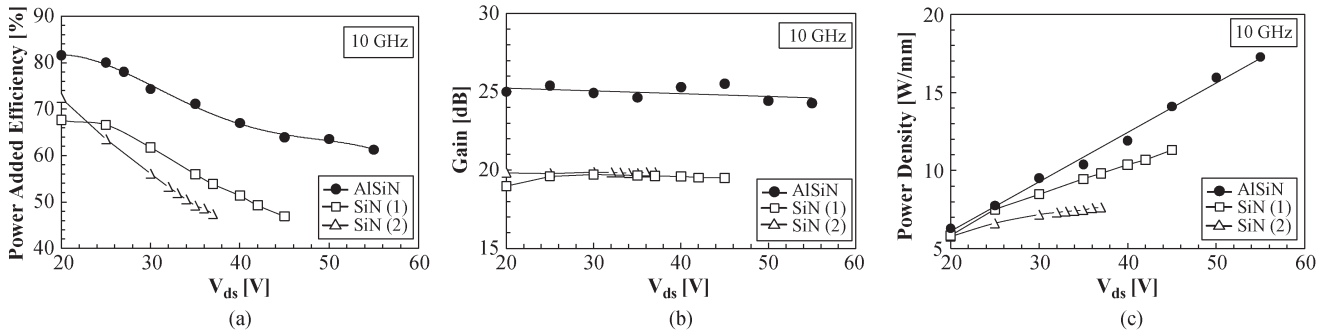


Fig. 16. Comparison of (a) peak PAE, (b) gain, and (c) output power for AlSiN- and SiN-passivated devices. SiN(1) refers to an earlier stand-alone sample fabricated by the same process as the SiN(2) and AlSiN samples, which were fabricated side by side.

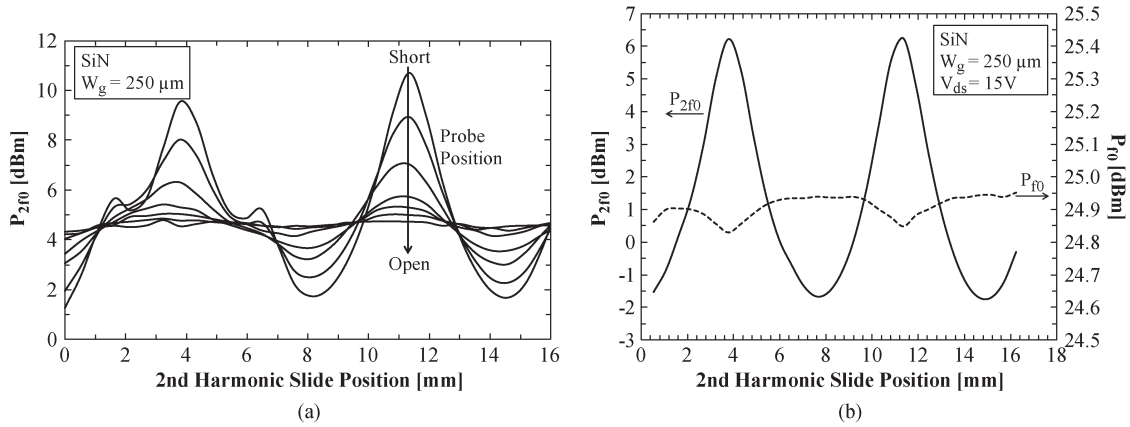


Fig. 17. (a) Second-harmonic output power as a function of the second-harmonic tuner slide and probe. The probe position ranged from 2.222 mm to 0.3175 mm out. The device was biased at $V_{ds}^q = 15$ V, $V_{gs}^q = -2.2$ V, and $I_d^q = 62.27$ mA. (b) Second-harmonic output power and fundamental power as a function of the second-harmonic tuner slide. The second-harmonic probe was fixed at 0.9525 mm out, and the device was biased at $V_{ds}^q = 15$ V, $V_{gs}^q = -2.2$ V, and $I_d^q = 62.27$ mA and was driven at 11.54 dBm of input power.

B. Large-Signal Results

Large-signal measurements were performed at 10 GHz on a number of 100- and 250- μ m gate periphery devices. The input RF signal was swept to the highest power possible before the gate was driven into forward bias. In our measurements, the AlSiN-passivated devices consistently outperformed SiN-passivated devices of identical dimensions. Fig. 15 shows a typical power sweep for identical devices with different passivations. Not only did the AlSiN devices produce more gain and higher efficiencies, but the efficiencies also dropped off less sharply with increasing drain bias. This condition is the principal difference of the performance of devices using the two passivation technologies.

A series of power sweeps were performed, with the drain bias increasing in steps of 1 V or 5 V, until the device failed. The results are summarized in Fig. 16.

The drain bias range reflects the difference between the drain bias tolerance of the two passivations. The AlSiN-passivated devices consistently performed at higher drain biases, as high as 55 V, whereas the SiN-passivated devices often broke down above 45 V.

Overall, the AlSiN-passivated devices consistently outperformed the SiN-passivated devices. A maximum PAE of 82% was measured at 15 V on an AlSiN-passivated device with a 100- μ m gate periphery, with 24 dB of gain. The maximum

output power measured was 17.5 W/mm at 55 V on the drain. For the SiN-passivated devices, the maximum PAE was 72.5% at 15 V, with 20 dB of gain, and the maximum output power was 7.5 W/mm at 37 V on the drain. The decrease in dispersion in the case of the AlSiN passivation is reflected by the significantly higher PAE of those devices at high drain bias. At low bias, the efficiencies of both AlSiN- and SiN-passivated devices are similar, but as the drain bias increases, the SiN-passivated devices drop off in efficiency much faster than the AlSiN-passivated devices.

The impact on efficiency has been of particular interest. In this setup, the termination of the second harmonic was achieved using a second tuner, which was adjusted to achieve the maximum PAE. To study the effect of the second-harmonic loading, a series of power sweeps were carried out at various tuner settings. First, it was confirmed that terminating the second harmonic in a short would maximize the output power and efficiency. When the tuner is “shorted,” the probe is all the way down or 0 mm “out.” The distance out increases as the probe is pulled out to approximate an open. Fig. 17(a) shows the second-harmonic power as a function of the tuner slide position with varying probe positions. When the probe is brought close to the transmission line—approximating a short—the second-harmonic power is observed to have its largest swing in value over the range of the slide. Furthermore, it is observed

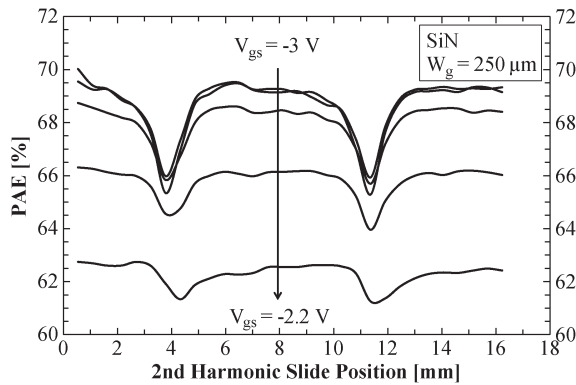


Fig. 18. Power-added efficiency as a function of gate bias and second-harmonic tuner slide position. The second-harmonic probe was fixed at 0.635 mm out, and the device was biased at $V_{ds}^q = 15$ V, $V_{gs}^q = -2.2$ V, and $I_d^q = 62.27$ mA and was driven at 11.54 dBm of input power.

[see Fig. 17(b)] that, when the second-harmonic power is at a maximum, the first-harmonic power is at a minimum.

Next, the gate-source bias was swept from the quiescent voltage (the peak of transconductance) to close to pinchoff (see Fig. 18). For a SiN-passivated device with 250- μ m periphery, the PAE increased from 63% at $V_{gs} = -2.2$ V to 70% at $V_{gs} = -3$ V.

V. CONCLUSION

High-efficiency HEMTs that were passivated using AlSiN have been demonstrated. An output power of 17.5 W/mm with a corresponding PAE of 61% at 10 GHz has been shown at a drain bias of 55 V. These devices also maintained state-of-the-art small-signal performance, with close to 90-GHz extrinsic f_T and 150-GHz extrinsic f_{max} . The AlSiN-passivated devices consistently outperformed their SiN counterparts in both small- and large-signal measurements.

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