

Petitioner's Demonstratives

**Innoscence (Zhuhai) Technology Company and Innoscence
America, Inc.,**

v.

Efficient Power Conversion Corporation

IPR2023-01383

December 18, 2024

INNOSCIENCE EXHIBIT 1056

INNOSCIENCE v. EPC

IPR2023-01383

U.S. Patent No. 8,404,508

U.S. Patent No. 8,404,508

"Enhancement mode GaN HEMT device and method for fabricating the same"

Inventors: Alexander Lidow, Robert Beach, Alana Nakata, Jianjun Cao, Guang Yuan Zhao



8,404,508 B2
Mar. 26, 2013

(54) ENHANCEMENT MODE GAN HEMT DEVICE AND METHOD FOR FABRICATING THE SAME (56) References Cited

(75) Inventors: Alexander Lidow, Marina Del Ray, CA (US); Robert Beach, La Crescenta, CA (US); Alana Nakata, Redondo Beach, CA (US); Jianjun Cao, Torrance, CA (US); Guang Yuan Zhao, Torrance, CA (US)

(73) Assignee: Efficient Power Conversion Corporation, El Segundo, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 495 days.

(21) Appl. No.: 12/756,960

(22) Filed: Apr. 8, 2010

(65) Prior Publication Data
US 2010/0258843 A1 Oct. 14, 2010

Related U.S. Application Data
(60) Provisional application No. 61/167,777, filed on Apr. 8, 2009.

(51) Int. Cl. H01L 21/00 (2006.01)

(52) U.S. Cl. 438/46; 438/172; 438/285; 257/E21.409; 257/E29.091; 257/E29.194; 257/E29.252; 257/E29.315

(58) Field of Classification Search 438/46-52, 438/172-177, 285-299, 481; 257/E21.409, 257/E29.074, 89, 91, 194, 242, 246, 252, 257/315

See application file for complete search history.

OTHER PUBLICATIONS
Hu, et al., "Enhancement Mode AlGaIn/GaN HEMT With Selectively Grown pn Junction Gate", *Electronics Letters*, vol. 35, No. 8, pp. 753-754, Apr. 13, 2000.

(Continued)

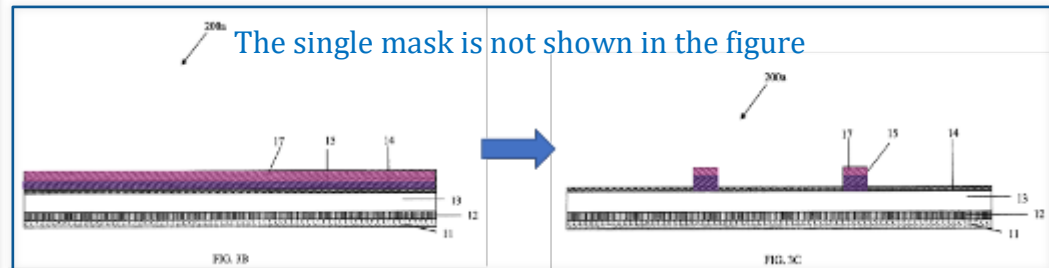
Primary Examiner—Michael Lebertritt
(74) Attorney, Agent, or Firm—Dickstein Shapiro LLP

(57) ABSTRACT
An enhancement-mode GaN transistor and a method of forming it. The enhancement-mode GaN transistor includes a substrate, transition layers, a buffer layer comprised of a III Nitride material, a barrier layer comprised of a III Nitride material, drain and source contacts, a gate III-V compound containing acceptor type dopant elements, and a gate metal, where the gate III-V compound and the gate metal are formed with a single photo mask process to be self-aligned at the bottom of the gate metal and the top of the transition layers. The enhancement-mode GaN transistor may also have a field plate made of Ohmic metal, a drain Ohmic metal, a source Ohmic metal, and a gate Ohmic metal, which are formed by a single photo mask process.

5 Claims, 25 Drawing Sheets

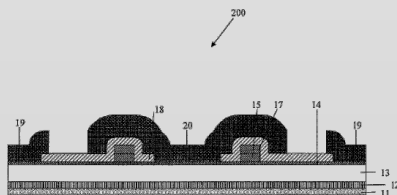
The present invention is an enhancement mode GaN HEMT device with a gate metal material and a doped GaN or AlGaIn material that are self-aligned, and a method for making such a device. The materials are patterned and etched using a single photo mask, which reduces manufacturing costs. Furthermore, a field plate at source potential is pat-

Ex. 1001, 3:1-6



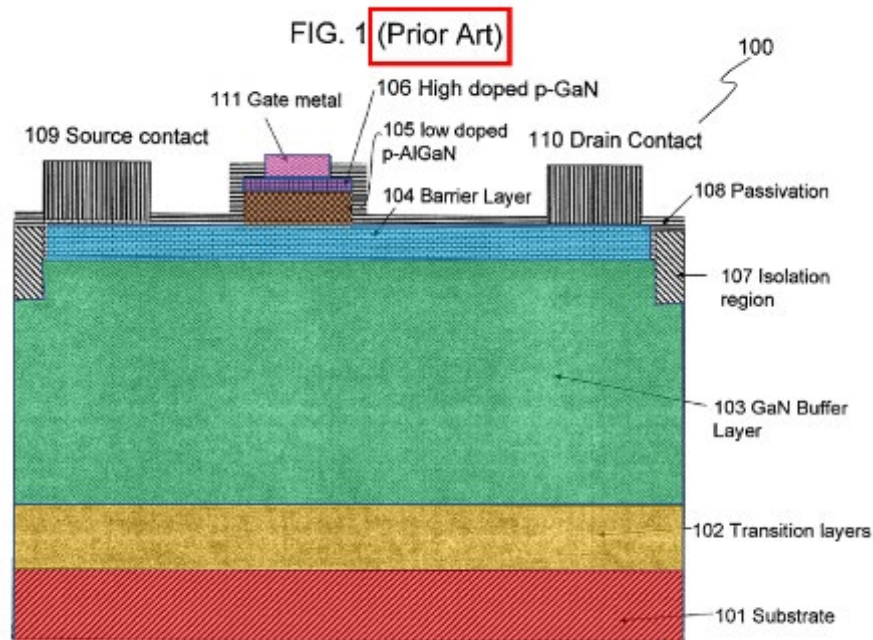
Ex. 1001, Figs. 3B, 3C

Alleged Point of Novelty: creating gate metal and GaN layer that are self-aligned by etching with a single photomask
Other elements are admitted prior art



The '508 Patent Distinguishes from Prior Art Based on Using a Single Mask Process to Form a Gate

The two-mask is not shown in the figure



Ex. 1001, Fig. 1

Figure 1 Shows the **Admitted Prior Art**
Two-Mask Gate Formation Process

As shown in FIG. 1, the gate metal, p-type GaN, or p-type AlGaIn material are defined by **two separate photo masks**. The first mask is used to form the p-type GaN or p-type AlGaIn, either by patterning a hard mask and selectively growing the p-type GaN or by patterning and etching the p-type GaN. The second mask is used to form the gate metal either by patterning and lifting off the gate metal or by patterning and etching the gate metal. **The two mask process leads to wider gate length than photo/etch minimum CD. This causes high gate charge, wider cell pitch, and higher Rdson ("on resistance"). The conventional method of fabrication also increases manufacturing costs.** Another disadvantage is that the highest electric field is located at the p-type GaN material or p-type AlGaIn material gate corner toward the drain ohmic contact metal. This high electric field leads to high gate leakage current and a gate reliability risk.

Ex. 1001, 1:65-2:18

- **No discussion** of ordering of gate formation to distinguish prior art

Instituted Grounds

- All claims of the '508 patent are challenged
- Claims in dispute: independent claims 1, 4, 5

Claim(s) Challenged	35 U.S.C. § ¹	Reference(s)/Basis
1–3	103	Yoshida, ² Beach, ³ Sheppard ⁴
1–4	103	Hikita-347, ⁵ Beach, Sheppard
5	103	Hikita-023 ⁶ , Beach, Sheppard

Claim 1 of the '508 Patent

**Epitaxial
layers
formation**

**Gate
formation
(alleged
novelty)**

**Dielectric
layer
formation**

**Ohmic
formation**

Claim 1	Claim Limitation
1pre	A method of forming an enhancement mode GaN transistor, the method comprising:
1a	nucleating and growing transition layers on a substrate;
1b	growing an III Nitride EPI layer over the transistor layers;
1c	growing an III Nitride barrier layer over the EPI layer;
1d	growing a GaN layer with acceptor type dopants over the barrier layer;
1e1	depositing a gate contact layer on the doped GaN layer;
1e2	applying a gate photo resistant pattern;
1e3	etching away the gate contact layer outside the gate region;
1e4	etching away the doped GaN layer, except a portion of the doped GaN layer beneath the gate contact;
1e5	removing the gate photo resistant pattern;
1f1	depositing a dielectric layer;
1f2	applying a contact photo resistant pattern;
1f3	etching the dielectric layer to open the drain and source contact area;
1f4	removing the contact photo resistant pattern;
1g1	depositing an Ohmic contact metal;
1g2	applying a metal photo resistant pattern;
1g3	etching the Ohmic contact metal;
1g4	removing the metal photo resistant pattern; and
1g5	performing rapid thermal annealing to form Ohmic drain and source contacts.

**No dispute that the prior art discloses
each of the claim limitations**

Ex. 1001, 6:59-7:15; Pet. 6-10

Claim 4 of the '508 Patent

Claim 4		Claim Limitation
Epitaxial layers formation	4pre	A method of forming an enhancement mode GaN transistor, the method comprising:
	4a	nucleating and growing transition layers on a substrate;
	4b	growing an InAlGaN EPI layer over the transistor layers;
	4c	growing an InAlGaN barrier layer over the InAlGaN EPI layer;
	4d	growing an InAlGaN layer with acceptor type dopants over the InAlGaN barrier layer;
Gate formation (alleged novelty)	4e	growing a GaN layer with acceptor type dopants over the doped InAlGaN layer
	4f1	depositing a gate contact layer on the doped GaN layer;
	4f2	applying a gate photo resistant pattern;
	4f3	etching away the gate contact layer outside the gate region;
	4f4	etching away the doped GaN layer and the doped InAlGaN layer, except for portions of the doped GaN layer and the doped InAlGaN layer beneath gate contact;
Dielectric layer formation	4f5	removing the gate photo resistant pattern;
	4g1	depositing a dielectric layer;
	4g2	applying a contact photo resistant pattern;
	4g3	etching the dielectric layer to open the drain and source contact area;
Ohmic formation	4g4	removing the contact photo resistant pattern;
	4h1	depositing an Ohmic contact metal;
	4h2	applying a metal photo resistant pattern;
	4h3	etching the Ohmic contact metal;
	4h4	removing the metal photo resistant pattern; and
	4h5	performing rapid thermal annealing to form Ohmic drain and source contacts.

No dispute that the prior art discloses each of the claim limitations

Claim 5 of the '508 Patent

**Epitaxial
layers
formation**

**Gate
formation
(alleged
novelty)**

**Dielectric
layer
formation**

**Ohmic
formation**

Claim 5	Claim Limitation
5pre	A method of forming an enhancement mode GaN
5a	nucleating and growing transition layers on a sub
5b	growing an InAlGaN EPI layer over the transistor layers;
5c	growing an AlGaN barrier layer over the InAlGaN EPI layer;
5d	growing an AlGaN layer with acceptor type dopants over the AlGaN barrier layer;
5e	growing a GaN layer with acceptor type dopants over the doped AlGaN layer
5f1	depositing a gate contact layer on the doped GaN layer;
5f2	applying a gate photo resistant pattern;
5f3	etching away the gate contact layer outside the gate region;
5f4	etching away the doped GaN layer, except for portions of the doped GaN layer and the doped AlGaN layer beneath gate contact;
5f5	removing the gate photo resistant pattern;
5g1	applying another photo resistant pattern;
5g2	etching the doped AlGaN layer such that the doped AlGaN extends outside the gate region towards the drain;
5g3	depositing an Ohmic contact metal;
5h1	applying a fourth photo resistant pattern;
5h2	etching the Ohmic contact metal
5h3	removing the fourth photo resistant pattern; and
5h4	performing rapid thermal annealing to form Ohmic drain and source contacts.

No dispute that the prior art discloses each of the claim limitations

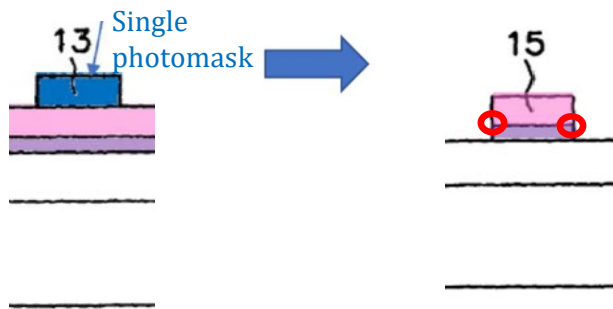
The Alleged Point of Novelty Was Previously Disclosed by Inventor Beach

(72) Inventor; and
(75) Inventor/Applicant (for US only): **BEACH, Robert**
[US/US]; 2945 Casitas Avenue, Altadena, CA 91001 (US).

Inventor Beach disclosed the alleged invention in a prior patent

Beach

Gate contact layer
Doped GaN layer



Beach, Figs. 1D, 1E

Beach discloses creating gate metal and GaN layer that are self-aligned by etching with a single photomask

'508 Patent

The single mask is not shown in the figure

Gate contact layer
Doped GaN layer



Ex. 1001, Figs. 3B, 3C

Undisputed Claim Elements

Epitaxial layers formation	Gate formation (alleged novelty)	Dielectric layer formation	Ohmic formation
Claim elements taught by prior art	Claim elements taught by prior art	Claim elements taught by prior art	Claim elements taught by prior art
Undisputed	Undisputed	Undisputed	Undisputed

See generally POR

Disputed Issues

Gate formation	Ohmic formation	Separate “gate photo resistant pattern” and “metal photo resistant pattern”
Motivation to combine: (1) whether the gate process must be performed first; (2) motivation to combine Yoshida/Hikita-347/Hikita-023 with Beach’s gate formation process Disputed	Motivation to combine Yoshida/ Hikita-347/Hikita-023 with Beach’s ohmic formation process Disputed	Whether the combination teaches separate “gate photo resistant pattern” and “metal photo resistant pattern” Disputed

See generally POR

Claim Construction Gate-First Is Not Required

Claim 1 of the '508 Patent

Claim 1	Claim Limitation
1pre	A method of forming an enhancement mode GaN transistor, the method comprising:
	nucleating and growing transition layers on a substrate;
	growing an III Nitride EPI layer over the transistor layers;
	growing an III Nitride barrier layer over the EPI layer;
	growing a GaN layer with acceptor type dopants over the barrier layer;
1e1	depositing a gate contact layer on the doped GaN layer;
1e2	applying a gate photo resistant pattern;
1e3	etching away the gate contact layer outside the gate region;
1e4	etching away the doped GaN layer, except a portion of the doped GaN layer beneath the gate contact;
1e5	removing the gate photo resistant pattern;
1f1	depositing a dielectric layer;
1f2	applying a contact photo resistant pattern;
1f3	etching the dielectric layer to open the drain and source contact area;
1f4	removing the contact photo resistant pattern;
1g1	depositing an Ohmic contact metal;
1g2	applying a metal photo resistant pattern;
1g3	etching the Ohmic contact metal;
1g4	removing the metal photo resistant pattern; and
1g5	performing rapid thermal annealing to form Ohmic drain and source contacts.

**EPC wrongly
argues the process
must be sequenced
as G-D-O**

**Gate
formation
(G)**

**Dielectric
layer
formation
(D)**

**Ohmic
Formation
(O)**

POR 17-25

The Board Correctly Found that No Gate-First Process Is Required

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INNOSCIENCE (ZHUHAI) TECHNOLOGY COMPANY, LTD.,
AND
INNOSCIENCE AMERICA, INC.
Petitioner,

v.

EFFICIENT POWER CONVERSION CORPORATION,
Patent Owner.

IPR2023-01383
Patent 8,404,508 B2

Before JON B. TORNQUIST, JEFFREY W. ABRAHAM, and
KIMBERLY McGRAW, *Administrative Patent Judges*.

McGRAW, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

At this stage of the proceeding, based on the present record, we determine that the claims require that the dielectric layer steps of [1f] must occur before the ohmic contact steps of [1g] but that the claims do not require that the gate structure be formed before the source and drain contacts.

Paper No. 11, 12

The Claims Do Not Require a G-D-O Process

- The claims do not recite any terms requiring a G-D-O order
- The specification specifies no sequence of forming the gate and ohmic contacts

The present invention is an enhancement mode GaN HEMT device with a gate metal material and a doped GaN or AlGaN material that are self-aligned, and a method for making such a device. The materials are patterned and etched using a single photo mask, which reduces manufacturing costs. Furthermore, a field plate at source potential is pat-

Ex. 1001, 3:1-6

The above description and drawings are only to be considered illustrative of specific embodiments, which achieve the features and advantages described herein. Modifications and substitutions to specific process conditions can be made. Accordingly, the embodiments of the invention are not considered as being limited by the foregoing description and drawings.

Ex. 1001, 6:50-56

**No G-D-O process
is required**



“Unless the steps of a method [claim] actually recite an order, the steps are not ordinarily construed to require one.”

Interactive Gift Exp., Inc. v. Compuserve Inc., 256 F.3d 1323, 1342 (Fed. Cir. 2001).

Reply 1-2

The Claims Do Not Require a Field Plate

- EPC wrongly argues that the claims require a field plate formed simultaneously with the ohmic contact, necessitating a G-D-O process
- The claims do not recite any field plate
- The patent describes a field plate as an optional unclaimed embodiment

The present invention is an enhancement mode GaN HEMT device with a gate metal material and a doped GaN or AlGaIn material that are self-aligned, and a method for making such a device. The materials are patterned and etched using a single photo mask, which reduces manufacturing costs. Furthermore, a field plate at source potential is pat-

Ex. 1001, 3:1-6

**No field plate
is required**

where the gate III-V compound and the gate metal are formed with a single photo mask process to be self-aligned and the bottom of the gate metal and the top of the gate compound have the same dimension. The enhancement mode GaN transistor may also have a field plate made of Ohmic metal, where a drain Ohmic metal, a source Ohmic metal, and the field plate are formed by a single photo mask process.

Ex. 1001, abstract

**Field plate is
optional**

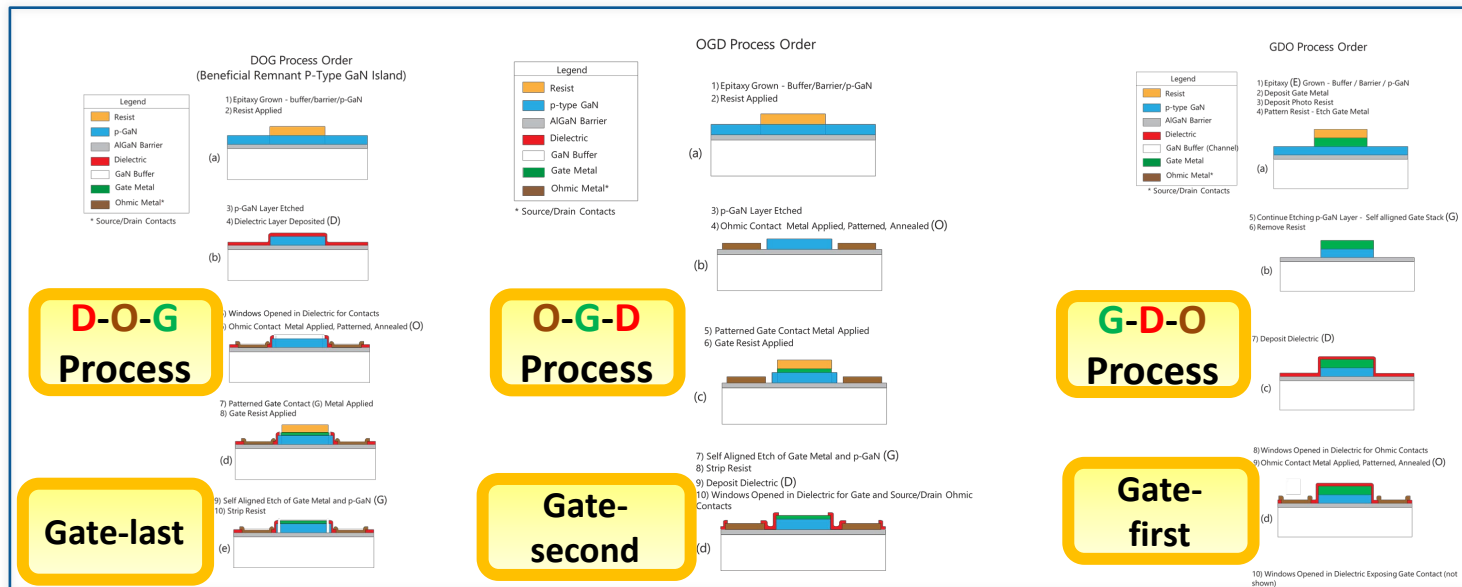
Reply 2-4

The Claims Cover Non-Gate-First Processes

- The claims cover six permutations of orders forming the **gate (G)**, **dielectric layer (D)**, and **Ohmic contacts (O)**

So anyway, those -- and by the way, there's a total of six variations of this and what we've just shown is three of them. There's three others you could draw.

Shealy Tr. (Ex. 2002), 101:9-12



Reply 4-12; Ex. 1040, 1-4

The Non-Gate-First Processes Provide Technical Advantages

- Forming the gate (G), dielectric layer (D), and Ohmic contacts (O) in different orders provide distinct advantages

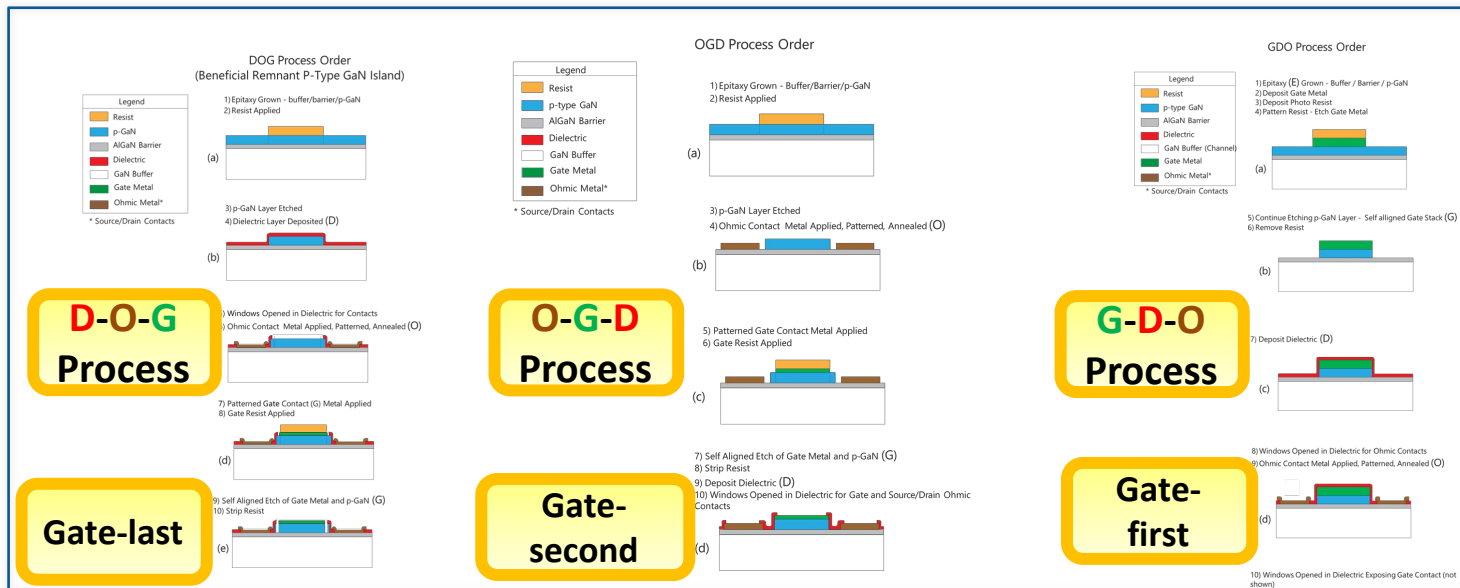
All are suitable design options

Process Order	Benefits
D-O-G	Protect the gate region from contamination during subsequent processing steps
O-G-D	Prevent the device surface from contamination
G-D-O	- Reduce the minimum source-to-gate distance - Reduce the source and drain access resistance

Conclusion: No Gate-First Is Required

- The Claims do not require a gate-first process

The claims are not limited to a gate-first **G-D-O** process



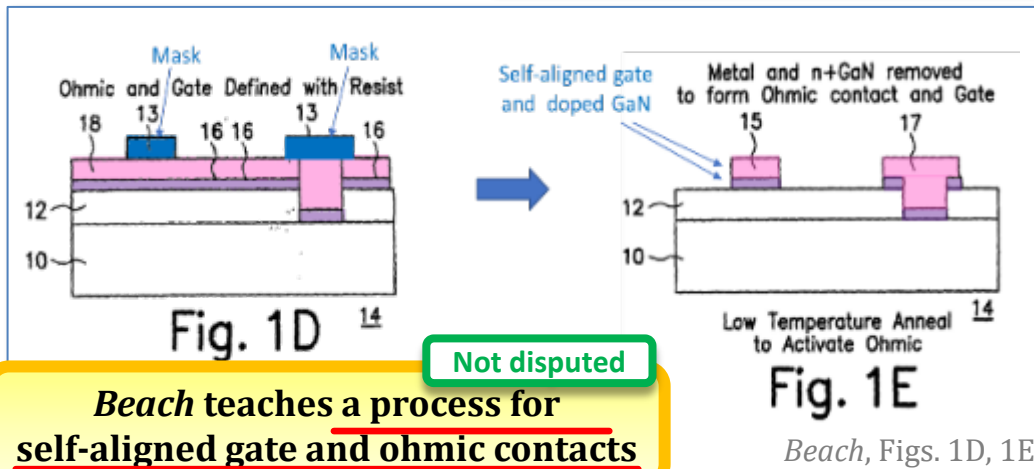
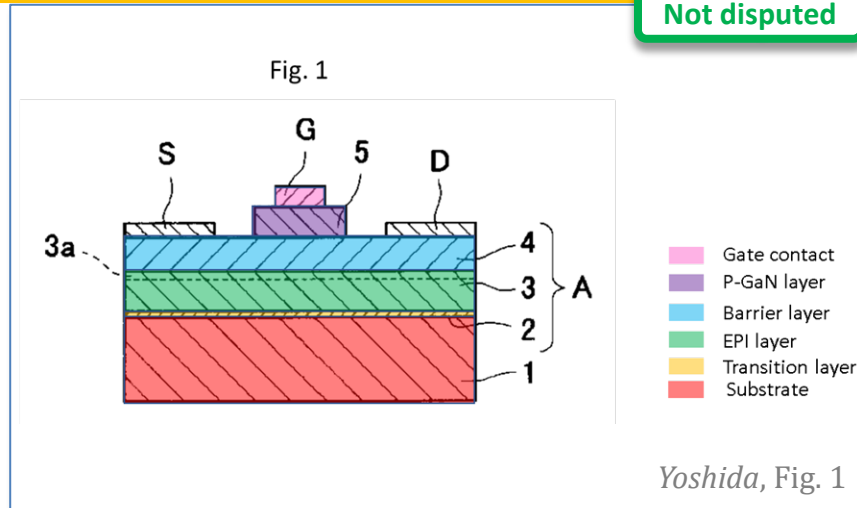
Any of the six permutations are suitable options

Ground 1: *Yoshida, Beach, and Sheppard*

Overview of Prior Art

***Yoshida* teaches the claimed process except a process for self-aligned gate and ohmic contacts, and growing multiple transition layers**

Not disputed



Optional buffer, nucleation and/or transition layers (not shown) may be provided on the substrate 10. For example, an AlN buffer layer may be provided to provide an appropriate crystal structure transition between the silicon carbide substrate and the remainder of the device. Additionally, strain balancing transition layer(s) may also be provided as described, for example, in commonly assigned U.S. Patent

Sheppard, 6:58-64

***Sheppard* teaches growing multiple transition layers**

Not disputed

Pet. 13-18

Yoshida-Beach-Sheppard Renders Obvious Claim 1

The only disputed issues are
motivation to combine

Claim Limitation

Method of forming an enhancement mode GaN transistor, the method comprising:

**Epitaxial
layers
formation**

- 1a nucleating and growing transition layers on a substrate;
- 1b growing an III Nitride EPI layer over the transistor layers;
- 1c growing an III Nitride barrier layer over the EPI layer;
- 1d growing a GaN layer with acceptor type dopants over the barrier layer;

**Gate
formation
(alleged
novelty)**

- 1e1 depositing a gate contact layer on the doped GaN layer;
- 1e2 applying a **gate photo resistant pattern**;
- 1e3 etching away the gate contact layer outside the gate region;

**Disputed Issue #1:
motivation to combine
Yoshida with Beach**

**Disputed Issue #3: teaching of
separate gate and metal
photo resistant pattern**

**Dielectric
layer
formation**

- 1f1 depositing a dielectric layer;
- 1f2 applying a contact photo resistant pattern;
- 1f3 etching the dielectric layer to open the drain and source contact area;
- 1f4 removing the contact photo resistant pattern;

**Ohmic
formation**

- 1g1 depositing an Ohmic contact metal;
- 1g2 applying a **metal photo resistant pattern**;
- 1g3 etching the Ohmic contact metal;

**Disputed Issue #2:
motivation to combine
Yoshida with Beach**

removing the metal photo resistant pattern; and
performing rapid thermal annealing to form Ohmic drain and source contacts.

Disputed Claim Elements (Claim 1)

Disputed Issue 1	Disputed Issue 2	Disputed Issue 3
EPC argues 1) a gate first construction, and 2) lack of motivation to combine <i>Yoshida</i> with <i>Beach</i> 's gate formation	EPC argues lack of motivation to combine <i>Yoshida</i> with <i>Beach</i> 's ohmic formation	EPC argues the combination does not teach separate "gate photo resistant pattern" and "metal photo resistant pattern"

Disputed Issue 1: Motivation to Combine for the Gate Formation Steps

Claim 1	Claim Limitation
1e1	depositing a gate contact layer on the doped GaN layer;
1e2	applying a gate photo resistant pattern;
1e3	etching away the gate contact layer outside the gate region;
1e4	etching away the doped GaN layer, except a portion of the doped GaN layer beneath the gate contact;
1e5	removing the gate photo resistant pattern;

Motivation to combine:

Why would a POSITA incorporate *Beach's* self-aligned single mask gate formation process into *Yoshida*?

Motivation to Combine *Yoshida* with *Beach* for the Gate Formation Steps

1. Analogous art: Both describe GaN HEMTs
2. KSR's use of known technique to improve similar devices in the same way.
3. KSR's some teaching, suggestion, motivation (TSM) in the prior art to modify or combine.
4. Reasonable expectation of success: POSITA had reasonable expectation that *Beach*'s technique would further *Yoshida*'s goals of gate alignment
5. EPC's counter arguments are incorrect

Motivation to Combine *Yoshida* with *Beach* for the Gate Formation Steps

1. Analogous

2. Known technique

3. TSM

4. Expectation

5. Rebuttal to EPC

Yoshida and *Beach* are analogous art, they both specifically describe techniques for forming GaN transistors

Yoshida [0009]

To achieve the above object, the present invention provides a high mobility transistor in which a stacked structure, comprised by stacking an i-type semiconductor layer and an n-type semiconductor layer in that order, is formed on a semi-insulating substrate; each semiconductor layer comprises a GaN-based compound semiconductor; a gate electrode is formed on the n-type semiconductor layer via a p-type semiconductor layer comprising GaN-based compound semiconductor.

Beach [0002], [0004]

The present invention relates generally to formation of a III-nitride material system device.

The devices fabricated for these types of applications are based on general device structures that exhibit high electron mobility and are referred to variously as heterojunction field effect transistors (HFETs), high electron mobility transistors (HEMTs) or modulation doped field effect transistors (MODFETs).

Using *Beach's* Known Technique to Improve *Yoshida's* Similar Device

1. Analogous

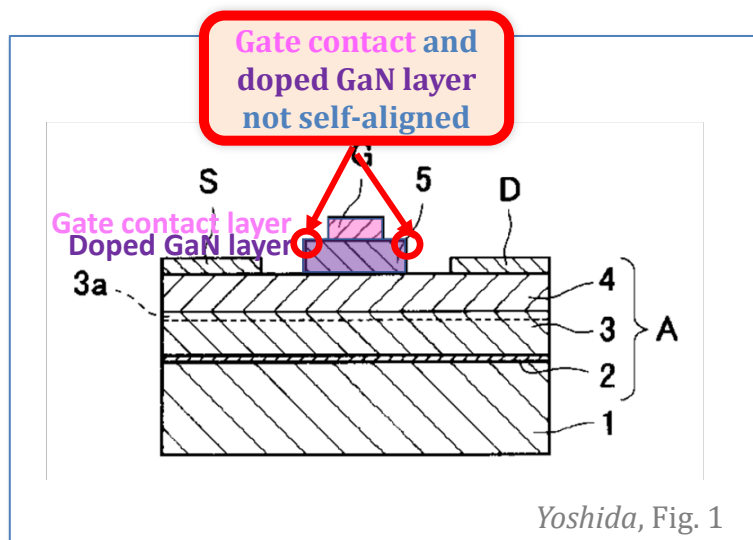
2. Known technique

3. TSM

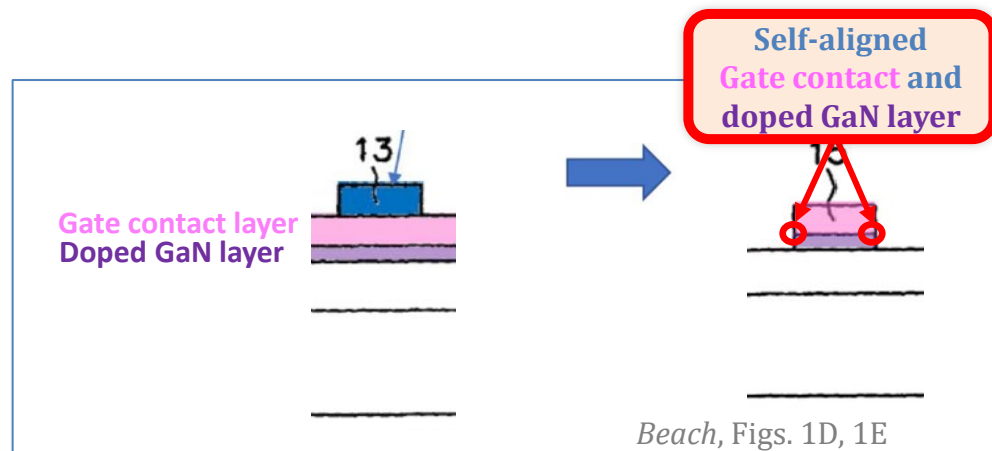
4. Expectation

5. Rebuttal to EPC

Yoshida-Beach is using a known technique (*Beach's* self-aligned single mask gate process) to improve similar devices (*Yoshida's* transistor) in the same way (using a single mask to etch the gate contact and doped GaN layers)



***Yoshida's* similar GaN transistor**



***Beach's* known technique improves gate alignment and saves cost of applying a second mask**

Some TSM to use *Beach's* gate process in *Yoshida*

1. Analogous

2. Known technique

3. TSM

4. Expectation

5. Rebuttal to EPC

Yoshida expressly states to “etch away the p-type GaN layer except where the gate electrode was to be loaded,” which is achieved by *Beach*

Yoshida [0022]

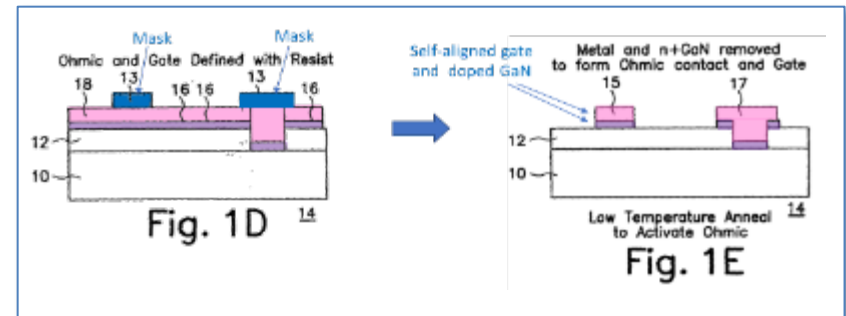
Dry etching was then performed using a plasma-converted mixture of hydrogen, argon, and methane as an etchant to etch away the p-type GaN layer except where the gate electrode was to be loaded and exposing the n-type InGaN layer 4.

Yoshida suggests self-alignment is desirable because it aims to remove all the p-type GaN layer except underneath the gate

Beach achieves *Yoshida's* objective: etching the doped GaN layer except the area under gate contact

Beach [0047]

After the deposition of photoresist layer 13, material 18 is removed, as by etching, except where protected by photoresist 13. The removal, or etching process, also eliminates protective layer 16 under patterned photoresist 13.



Beach, Figs. 1D, 1E

A POSITA Would Have Reasonable Expectation of Success

1. Analogous 2. Known technique 3. TSM 4. Expectation 5. Rebuttal to EPC

A POSITA would have expected success in implementing *Beach's* gate process in *Yoshida* because etching multiple layers of materials using the same mask was well understood and implemented decades before the '508 patent

129. Using *Beach's* single mask process to etch the gate contact and doped GaN layer in *Yoshida's* device would have required only conventional techniques in their ordinary and expected manner, because using the same mask to etch different layers of materials was routine, conventional, and well understood in the art. Thus, a POSITA would have reasonably expected to succeed in using *Beach's* single mask process to form *Yoshida's* GaN device.

Shealy, ¶129

A POSITA Would Have Reasonable Expectation of Success

1. Analogous

2. Known technique

3. TSM

4. Expectation

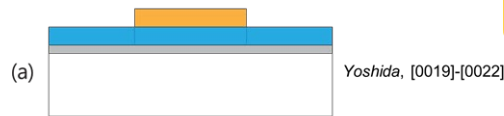
5. Rebuttal to EPC



**Yoshida's
D-O-G Process**

DOG Process Order (Yoshida-Beach)

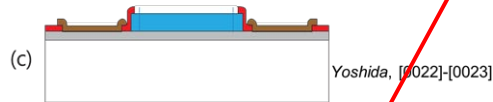
- 1) Epitaxy Grown - buffer/barrier/p-GaN
- 2) Resist Applied



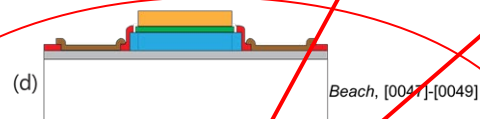
- 3) p-GaN Layer Etched
- 4) Dielectric Layer Deposited (D)



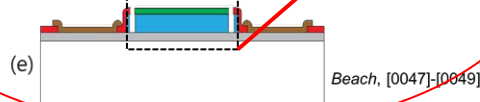
- 5) Windows Opened in Dielectric for Contacts
- 6) Ohmic Contact Metal Applied, Patterned, Annealed (O)



- 7) Patterned Gate Contact (G) Metal Applied
- 8) Gate Resist Applied



- 9) Self Aligned Etch of Gate Metal and p-GaN (G)
- 10) Strip Resist



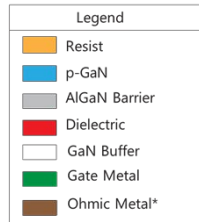
Incorporating *Beach's* gate process in *Yoshida* requires only a simple modification

**Self-aligned
Gate contact and
doped GaN layer**

**The gate
etching step of
Yoshida is
modified**

The Petition Explains a POSITA Would have Expected Success in Applying *Beach's* Single Mask Gate Process in *Yoshida*

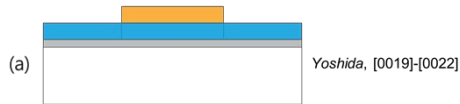
Not a new argument



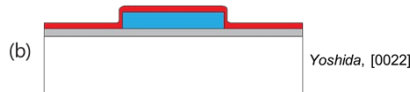
* Source/Drain Contacts

DOG Process Order (*Yoshida-Beach*)

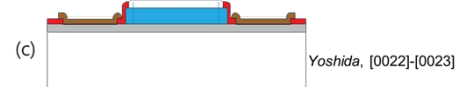
- 1) Epitaxy Grown - buffer/barrier/p-GaN
- 2) Resist Applied



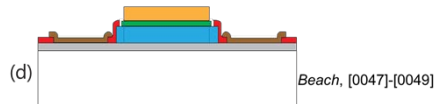
- 3) p-GaN Layer Etched
- 4) Dielectric Layer Deposited (D)



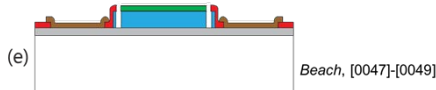
- 5) Windows Opened in Dielectric for Contacts
- 6) Ohmic Contact Metal Applied, Patterned, Annealed (O)



- 7) Patterned Gate Contact (G) Metal Applied
- 8) Gate Resist Applied



- 9) Self Aligned Etch of Gate Metal and p-GaN (G)
- 10) Strip Resist



A POSITA would have expected success because applying a single mask to

form the gate contact and doped GaN layer was a well-known and conventional

technique. Shealy, ¶127. The '508 patent states that the etching of the gate contact

and p-GaN layer using the same mask is performed by "any known technique,"

because etching multiple layers of different materials using the same mask was

routine, conventional, and well understood in the art. Ex. 1001, 3:45-50; Shealy,

¶127. Indeed, using the same mask to etch different layers of materials in

semiconductor devices was known and implemented decades before the '508

Pet. 22

**Same combination,
same argument**

Reply 14, *ShealySupp*, ¶32

A POSITA Would Have Reasonable Expectation of Success

1. Analogous

2. Known technique

3. TSM

4. Expectation

5. Rebuttal to EPC

D-O-G Process
incorporating self-aligned gate process

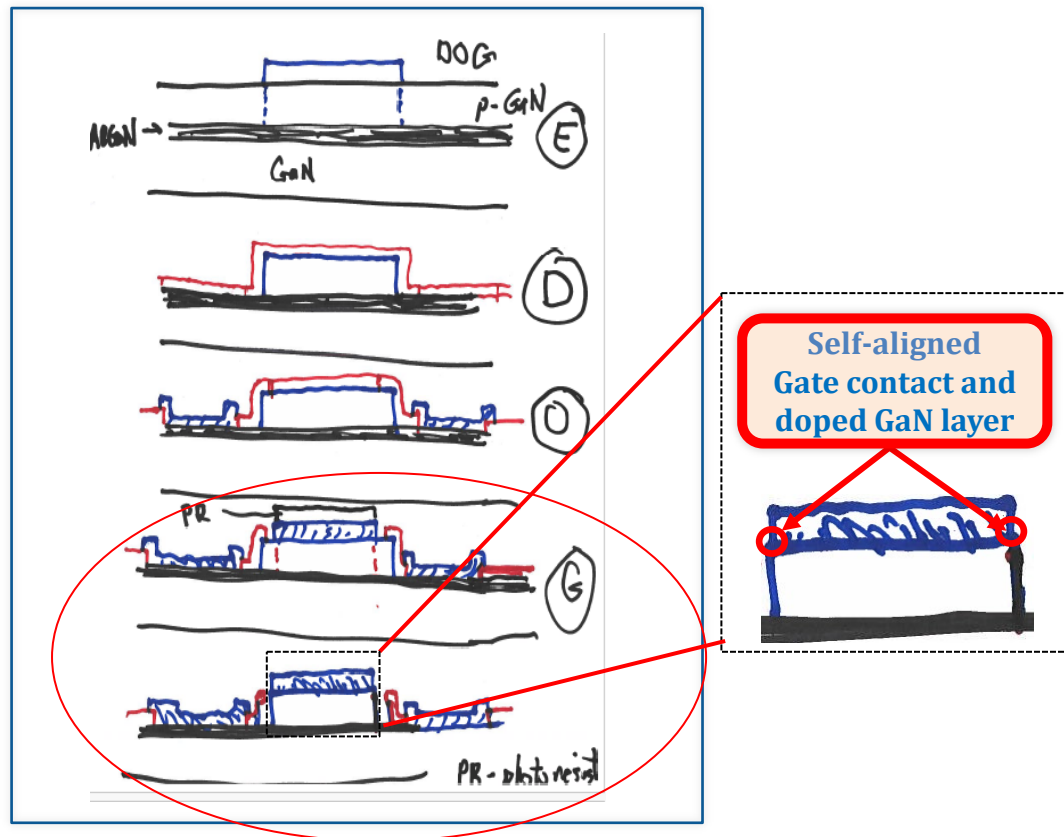


Exhibit prepared by Dr. Shealy at Depo.
(Exs. 1040, 2003), 2

Reply 13-14

Patent Owner Demands for Additional Explanation of the Combination

Not a new argument

EX2001 ¶135. Simply put, even if one were to have been motivated to combine the references identified by Petitioner, because Petitioner failed to particularly explain the combination, it is impossible to determine whether a POSA would have expected to successfully combine the references, and whether that unidentified process flow would yield an operable device.

POR 36

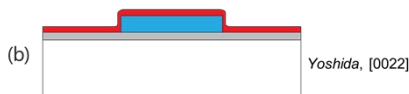


DOG Process Order (Yoshida-Beach)

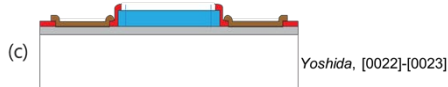
- 1) Epitaxy Grown - buffer/barrier/p-GaN
- 2) Resist Applied



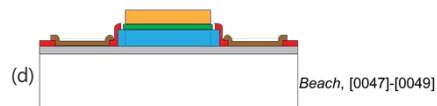
- 3) p-GaN Layer Etched
- 4) Dielectric Layer Deposited (D)



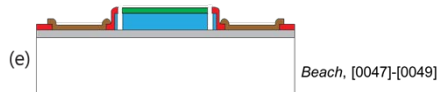
- 5) Windows Opened in Dielectric for Contacts
- 6) Ohmic Contact Metal Applied, Patterned, Annealed (O)



- 7) Patterned Gate Contact (G) Metal Applied
- 8) Gate Resist Applied



- 9) Self Aligned Etch of Gate Metal and p-GaN (G)
- 10) Strip Resist



Reply 14, *ShealySupp*, ¶32



“[T]he very nature of the reply and sur-reply briefs are to respond (whether to refute, rebut, explain, discredit, and so on) to prior raised arguments within the confines of 37 C.F.R. § 42.23(b).”

Rembrandt Diagnostics, LP v. Alere, Inc.,
76 F.4th 1376, 1384 (Fed. Cir. 2023)

The Diagram Illustrating the *Yoshida-Beach* Combination Is not a New Argument

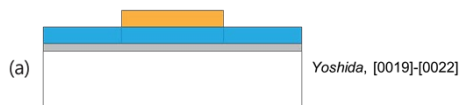
Not a new argument



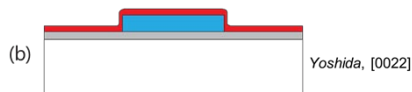
* Source/Drain Contacts

DOG Process Order (*Yoshida-Beach*)

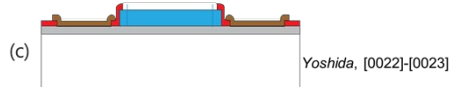
- 1) Epitaxy Grown - buffer/barrier/p-GaN
- 2) Resist Applied



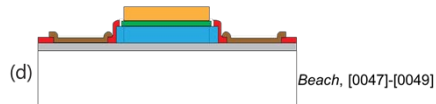
- 3) p-GaN Layer Etched
- 4) Dielectric Layer Deposited (D)



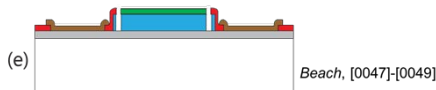
- 5) Windows Opened in Dielectric for Contacts
- 6) Ohmic Contact Metal Applied, Patterned, Annealed (O)



- 7) Patterned Gate Contact (G) Metal Applied
- 8) Gate Resist Applied



- 9) Self Aligned Etch of Gate Metal and p-GaN (G)
- 10) Strip Resist



- The Petition explains the expectation of success in the *Yoshida-Beach* combination
- Dr. Shealy further elaborates the step-by-step implementation of self-aligned D-O-G process in deposition
- The diagram is in response to EPC's demand for additional combination details in its Patent Owner's Response
- No change of references, no change of grounds

“Parties are not barred from elaborating on their arguments on issues previously raised.”

Chamberlain Grp., Inc. v. One World Techs., Inc.,
944 F.3d 919, 925 (Fed. Cir. 2019)



Reply 14, *ShealySupp*, ¶32

EPC's Incorrect Arguments

- 1. Analogous
- 2. Known technique
- 3. TSM
- 4. Expectation
- 5. Rebuttal to EPC

Issue	EPC's Incorrect Argument	Correct Resolution
Motivation to combine: Why would a POSITA incorporate <i>Beach</i> 's self-aligned single mask gate formation process into <i>Yoshida</i>	1. <i>Beach</i> and <i>Yoshida</i> are not gate-first, so the combination cannot be gate-first. 2. Bodily incorporating <i>Beach</i>'s gate simultaneous process in <i>Yoshida</i> would not work, and a POSITA would not be motivated to do so. 3. The <i>Yoshida-Beach</i> combination does not meet claim limitation [1e4].	A POSITA would have incorporated <i>Beach</i> 's self-aligned single mask gate formation process into <i>Yoshida</i> to improve gate's alignment

EPC's Incorrect Argument #1 of 3: No Motivation Because *Yoshida* and *Beach* Do Not Teach a Gate-First Process

1. Gate-first construction 2. Gate-simultaneous v. gate-last 3. Limitation [1e4]

EPC incorrectly argues no motivation to combine because *Beach* and *Yoshida* do not teach a gate-first process

- The Claims **do not** require a gate-first process
- A gate-first process would have been obvious

43. As I explained in my deposition, there are only six permutations of ordering in forming a gate contact, ohmic contacts, and dielectric layer, all of which are suitable options. Each of the permutations would have been obvious to a POSITA. And a POSITA would have found it obvious to try a gate-first G-D-O process and expected success to do so.

ShealySupp, ¶43

EPC's Incorrect Argument #2 of 3 : No Motivation Because *Beach* Is a Gate-Simultaneous Process

1. Gate-first construction

2. Gate-simultaneous v. gate-last

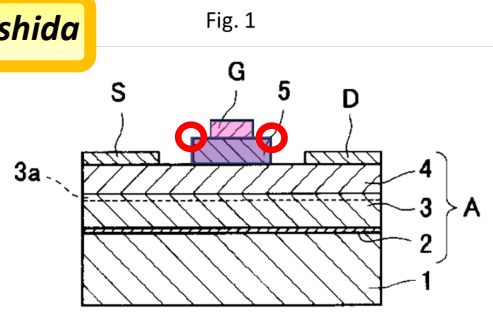
3. Limitation [1e4]

EPC incorrectly argues no motivation to combine because *Beach* is a gate-simultaneous process and *Yoshida* is a gate-last process

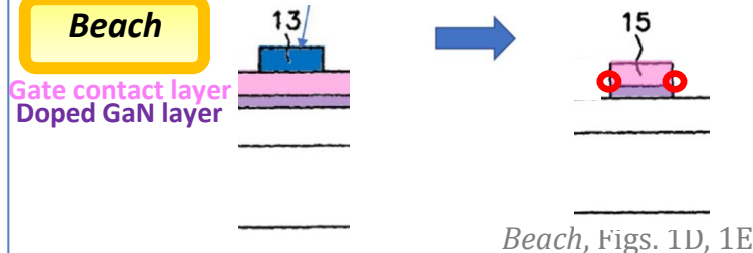
**Bodily
Incorporation**

Beach is a gate-simultaneous process and *Yoshida* is a gate-last process – does not matter

Yoshida



Beach



The combination maintains *Yoshida*'s process flow, but only substitutes *Beach*'s implementation details for the self-aligned gate formation

“It is well-established that a determination of obviousness ... **does not require an actual, physical substitution of elements.**”

In re Mouttet, 686 F.3d 1322, 1332 (Fed. Cir. 2012)

Reply 15

EPC's Incorrect Argument #3 of 3: the Modified *Yoshida* Process Does Not Meet [1e4]

1. Gate-first construction

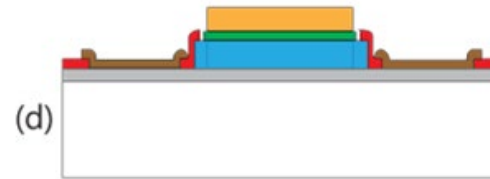
2. Gate-simultaneous v. gate-last

3. Limitation [1e4]

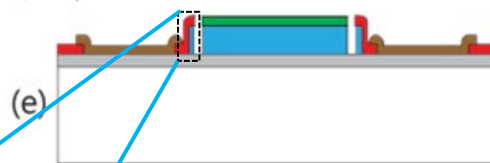
EPC in its sur-reply first raises the new argument that the *Yoshida-Beach* combination does not meet limitation [1e4] because it would result in remnant p-type GaN islands outside the gate area

Claim 1	Claim Limitation
1e1	depositing a gate contact layer on the doped GaN layer;
1e2	applying a gate photo resistant pattern;
1e3	etching away the gate contact layer outside the gate region;
1e4	etching away the doped GaN layer, except a portion of the doped GaN layer beneath the gate contact;
1e5	removing the gate photo resistant pattern;

7) Patterned Gate Contact (G) Metal Applied
8) Gate Resist Applied

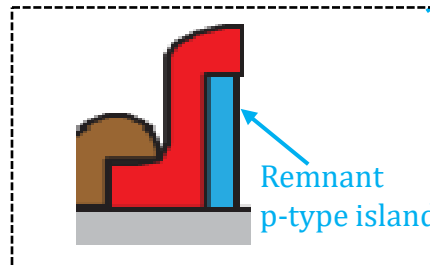


9) Self Aligned Etch of Gate Metal and p-GaN (G)
10) Strip Resist



* Source/Drain Contacts

Improper new argument by EPC



EPC improperly argues that the *Remnant p-type GaN Island* does not meet limitation [1e4]

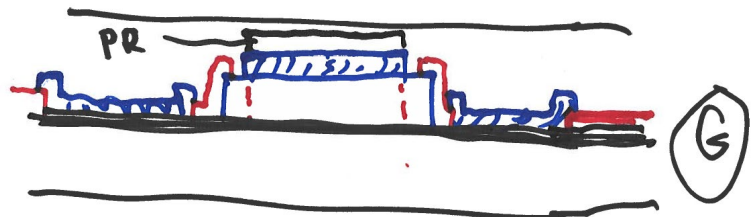
Sur-Reply 6, 16-18

EPC Improperly Argues that the Modified *Yoshida* Process Does Not Meet Claim Limitation [1e4]

1. Gate-first construction

2. Gate-simultaneous v. gate-last

3. Limitation [1e4]



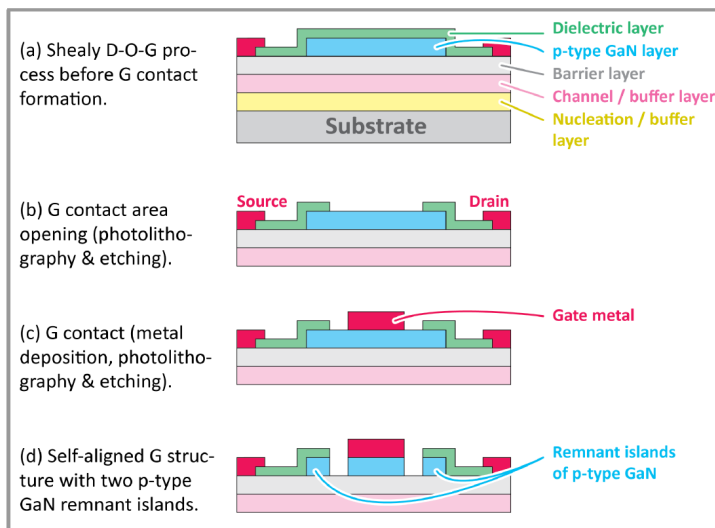
Remnant p-type GaN Islands Exhibit prepared by Dr. Shealy at Depo. (Ex. 1040), 2

Dr. Shealy's deposition testimony provided the D-O-G process with remnant p-GaN island

EPC argued in its POR regarding the functionality of the remnant p-type GaN islands, but never raised any argument against [1e4]

EPC's new argument should not be allowed

prior art. EX2001 ¶¶89-90. Importantly, the gate electrode process as described by Dr. Shealy would not work because it would leave remnant islands of the p-type semiconductor, for example, p-type GaN in the context of the '508 patent, between the source and gate as well as between the gate and drain. Such remnant islands (shown below) are detrimental to the function of an enhancement mode HEMT and a POSA would not proceed in such a manner. *Id.* at ¶90.



EX2001 ¶90

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Modified *Yoshida* Process Meets Claim Limitation [1e4]

1. Gate-first construction

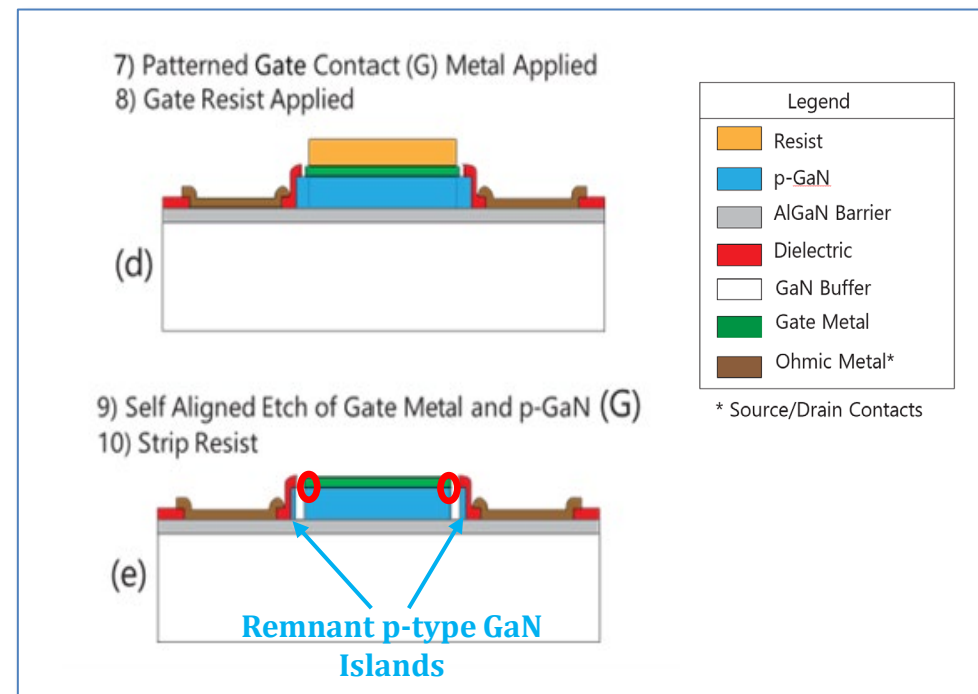
2. Gate-simultaneous v. gate-last

3. Limitation [1e4]

Claim 1	Claim Limitation
1e1	depositing a gate contact layer on the doped GaN layer;
1e2	applying a gate photo resistant pattern;
1e3	etching away the gate contact layer outside the gate region;
1e4	etching away the doped GaN layer, except a portion of the doped GaN layer beneath the gate contact;
1e5	removing the gate photo resistant pattern;

Modified *Yoshida* process with **remnant p-type GaN Islands** meet [1e4]:

- the **p-type GaN** outside of the **gate region** is etched
- the **p-type GaN** outside the **photoresistant pattern** is etched
- the **gate metal** and **p-type GaN** are self-aligned after etching



Modified *Yoshida* Process Meets [1e4]

1. Gate-first construction

2. Gate-simultaneous v. gate-last

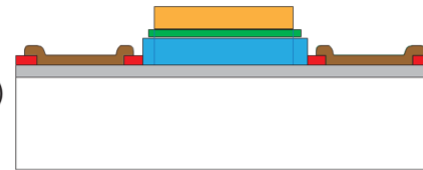
3. Limitation [1e4]

Dr. Shealy explains that the remnant p-type GaN islands can be eliminated by applying appropriate photoresist, indisputably meeting limitation [1e4]

Claim 1	Claim Limitation
1e1	depositing a gate contact layer on the doped GaN layer;
1e2	applying a gate photo resistant pattern;
1e3	etching away the gate contact layer outside the gate region;
1e4	etching away the doped GaN layer, except a portion of the doped GaN layer beneath the gate contact;
1e5	removing the gate photo resistant pattern;

7) Patterned Gate Contact (G) Metal Applied
8) Gate Resist Applied

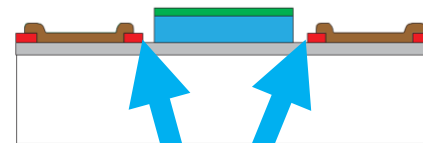
(d)



* Source/Drain Contacts

9) Self Aligned Etch of Gate Metal and p-GaN (G)
10) Strip Resist

(e)



Unrebutted in EPC's Sur-Reply

**No Remnant
p-type GaN Islands**

Motivation to Combine *Yoshida* with *Beach* for the Gate Formation Steps

1. Analogous art: Both describe GaN HEMTs
Same transistors → Obvious to combine
2. KSR's use of known technique to improve similar devices in the same way.
Known technique, known device → Obvious to combine
3. KSR's some teaching, suggestion, motivation (TSM) in the prior art to modify or combine.
Yoshida/Beach TSM → Obvious to combine
4. Reasonable expectation of success: POSITA had reasonable expectation that *Beach*'s technique would further *Yoshida*'s goals of gate alignment
Expectation to improve gate alignment → Obvious to combine
5. EPC's counter arguments are incorrect
Remnant p-type islands still meet claims and can be eliminated → Obvious to combine

Disputed Issue 2: Motivation to Combine for the Ohmic Formation Steps

Claim 1	Claim Limitation
1g1	depositing an Ohmic contact metal;
1g2	applying a metal photo resistant pattern;
1g3	etching the Ohmic contact metal;
1g4	removing the metal photo resistant pattern; and
1g5	performing rapid thermal annealing to form Ohmic drain and source contacts.

Motivation to combine:

Why would a POSITA incorporate *Beach's* ohmic formation process into *Yoshida*?

Motivation to Combine *Yoshida* with *Beach* for the Ohmic Formation Steps

1. Analogous art: Both describe GaN HEMTs
2. KSR's use of known technique to improve similar devices in the same way.
3. KSR's some teaching, suggestion, motivation (TSM) in the prior art to modify or combine.
4. Reasonable expectation of success: POSITA had reasonable expectation that *Beach*'s technique would further *Yoshida*'s goal of ohmic formation
5. EPC's counter arguments are incorrect

Motivation to Combine *Yoshida* with *Beach* for the Ohmic Formation Steps

1. Analogous

2. Known technique

3. TSM

4. Expectation

5. Rebuttal to EPC

Yoshida and *Beach* are analogous art, they both specifically describe techniques for forming GaN transistors

Yoshida [0009]

To achieve the above object, the present invention provides a high mobility transistor in which a stacked structure, comprised by stacking an i-type semiconductor layer and an n-type semiconductor layer in that order, is formed on a semi-insulating substrate; each semiconductor layer comprises a GaN-based compound semiconductor; a gate electrode is formed on the n-type semiconductor layer via a p-type semiconductor layer comprising GaN-based compound semiconductor.

Beach [0002], [0004]

The present invention relates generally to formation of a III-nitride material system device.

The devices fabricated for these types of applications are based on general device structures that exhibit high electron mobility and are referred to variously as heterojunction field effect transistors (HFETs), high electron mobility transistors (HEMTs) or modulation doped field effect transistors (MODFETs).

Using *Beach's* Known Technique to Improve *Yoshida's* Similar Device

1. Analogous

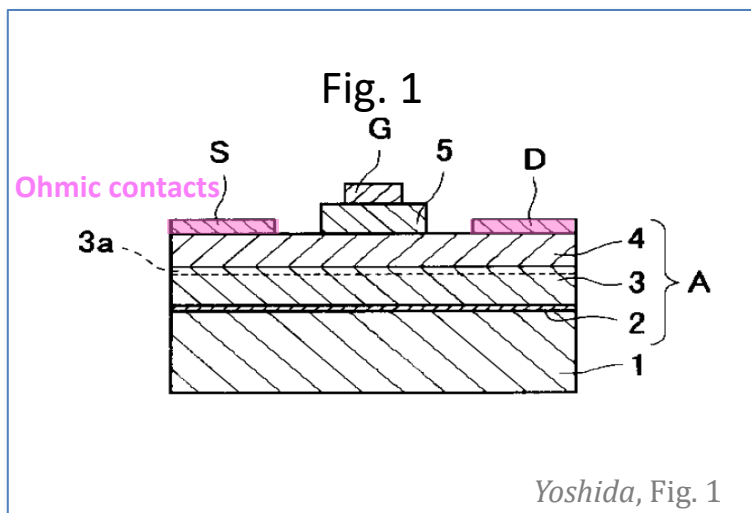
2. Known technique

3. TSM

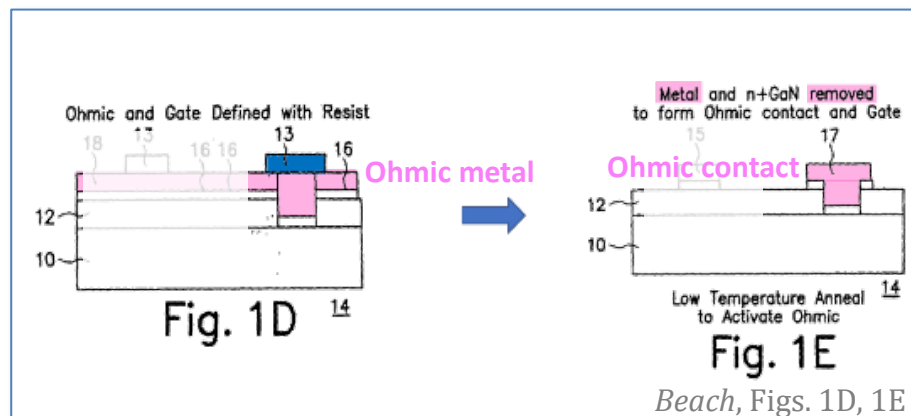
4. Expectation

5. Rebuttal to EPC

Yoshida-Beach is using a known technique (*Beach's* masking and etching process) to improve similar devices (*Yoshida's* transistor) in the same way (using masking and etching to form ohmic contacts)



Yoshida's similar GaN transistor



Beach's known technique to form ohmic contact is simpler than the alternative lift-off process and saves manufacturing cost

Some TSM to use *Beach's* ohmic process in *Yoshida*

1. Analogous

2. Known technique

3. TSM

4. Expectation

5. Rebuttal to EPC

Yoshida expressly states to form ohmic contacts, but does not explain the implementation details which *Beach* provides

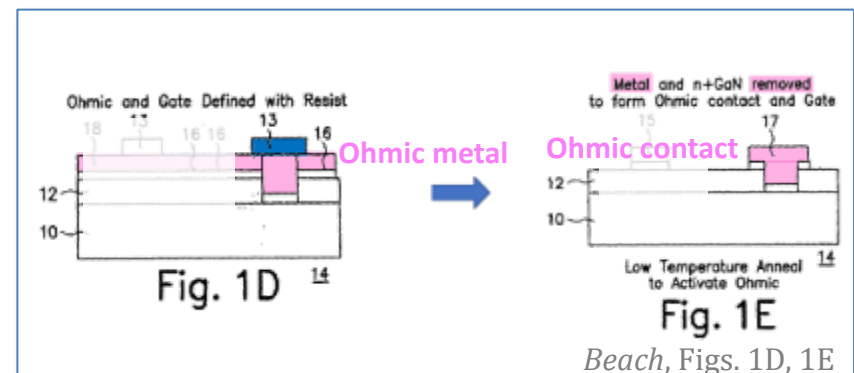
Yoshida [0022]

after patterning with photoresist, the area including the part where the gate electrode was to be loaded was masked, [leaving] the portion where source and drain electrodes were to be loaded open, and metal Al deposited on the exposed n-type InGaN layer 4 to load source electrode S and drain electrode D.

Beach achieves *Yoshida's* objective: forming ohmic contacts

Beach [0047]

Referring now to Figure 1D, resist material 13 is deposited in a pattern to permit the formation of a gate 15 and ohmic contact 17. ... After the deposition of photoresist layer 13, material 18 is removed, as by etching, except where protected by photoresist 13.



A POSITA Would Have Reasonable Expectation of Success

1. Analogous 2. Known technique 3. TSM 4. Expectation 5. Rebuttal to EPC

A POSITA would have expected success in implementing *Beach's* ohmic process in *Yoshida* because *Beach's* process of using a mask to pattern and etch ohmic metal was well-known and conventional

Beach, according to the known, routine process of masking and etching. Using *Beach's* masking process to etch the Ohmic contact metal in *Yoshida's* device would have required only conventional techniques in their ordinary and expected manner, because using a mask to etch an Ohmic contact metal was routine, conventional, and well understood in the art. Thus, a POSITA would have reasonably expected to succeed in using *Beach's* masking process to form *Yoshida's* Ohmic source and drain contacts.

Shealy, ¶147

EPC's Incorrect Argument: No Motivation Because *Yoshida* Teaches a Lift-Off Process

1. Analogous

2. Known technique

3. TSM

4. Expectation

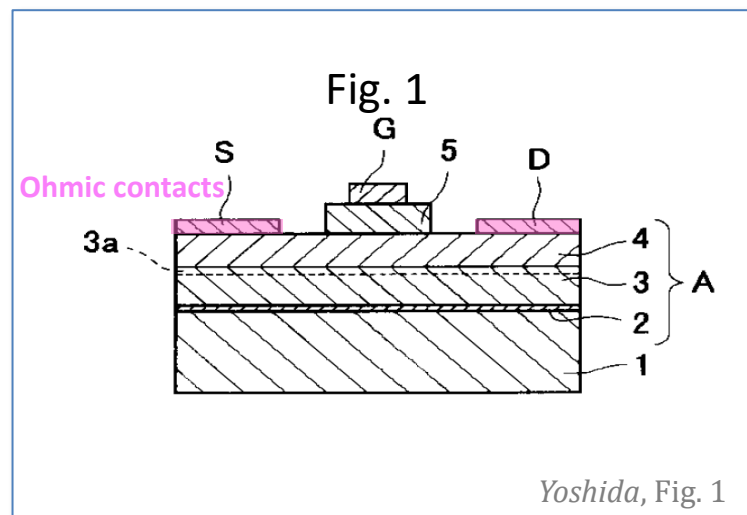
5. Rebuttal to EPC

EPC incorrectly argues no motivation to combine because *Yoshida* discloses using a lift-off technique to form ohmic contacts

Yoshida [0022]

after patterning with photoresist, the area including the part where the gate electrode was to be loaded was masked, [leaving] the portion where source and drain electrodes were to be loaded open, and metal Al deposited on the exposed n-type InGaN layer 4 to load source electrode S and drain electrode D.

***Yoshida* is silent as to any lift-off technique to form ohmic contacts**



Metal etching is more precise than lift-off and can produce vertical sidewalls

EPC's Incorrect Argument: No Motivation Because *Yoshida* Teaches a Lift-Off Process

1. Analogous

2. Known technique

3. TSM

4. Expectation

5. Rebuttal to EPC

Metal Etching Produces Vertical Sidewalls like in *Yoshida*

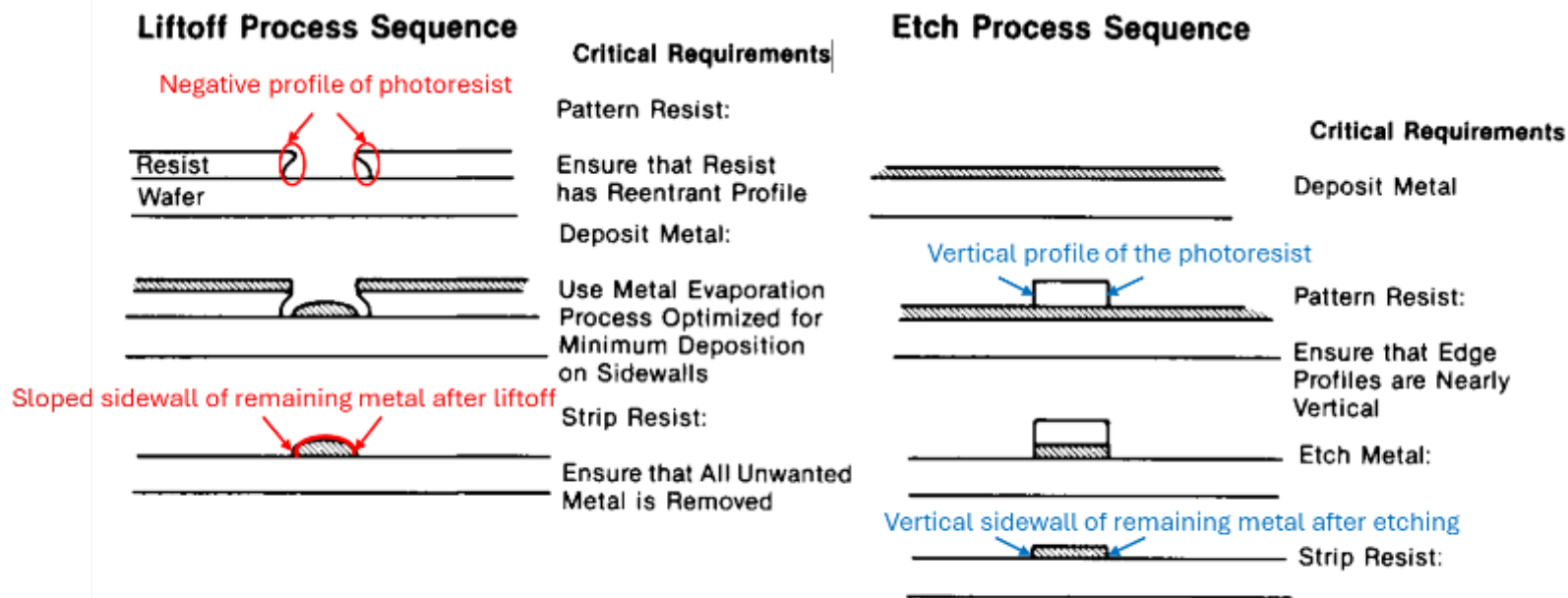


Fig. 1. Comparison of additive (lift-off) and subtractive (etch) metallization patterning processes.

Gorowitz, Fig. 1

EPC's Incorrect Argument: No Motivation Because *Yoshida* Teaches a Lift-Off Process

1. Analogous

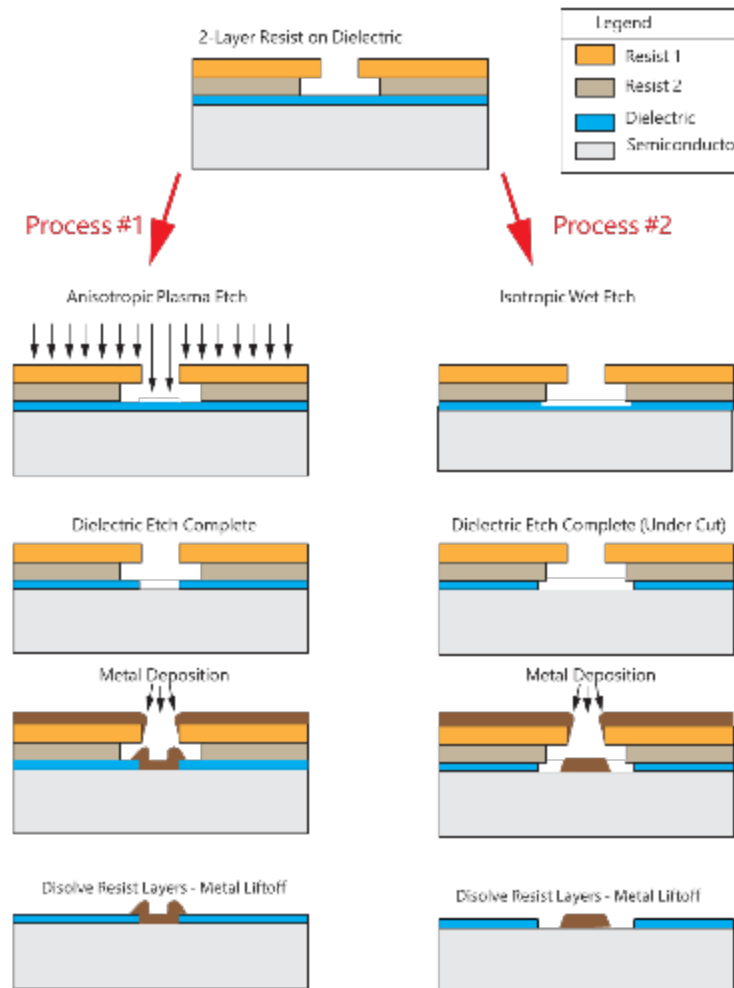
2. Known technique

3. TSM

4. Expectation

5. Rebuttal to EPC

**Lift-off Does Not
Produce Vertical
Sidewalls like in
*Yoshida***



ShealySupp, ¶54

Reply 22

Beach's Metal Etching Process Is an Obvious Design Choice

1. Analogous

2. Known technique

3. TSM

4. Expectation

5. Rebuttal to EPC

Only **two** prevalent alternatives, lift-off or metal etching. *Beach's* metal etching process provides benefits over lift-off and is an **obvious design choice**

metal dimensions. Further, as I explained in my previous declaration, lift-off and metal etching are the only two prevalent techniques for metal patterning. *Yoshida* does not suggest that performing an etching process or lift-off was critical to its method to form a GaN transistor. *Beach's* etching technique provides performance benefits over lift-off, e.g., more accurate and controllable to pattern the metal. Using a metal etching process to form the ohmic contacts, as taught by *Beach*, would be an obvious design choice to form the ohmic contacts of *Yoshida*. See *Gorowitz*, 4 (“When resist patterns are used to define metal layers, the process can be either additive [lift-off] or subtractive [etching].”).

ShealySupp, ¶56

Motivation to Combine *Yoshida* with *Beach* for the Ohmic Formation Steps

1. Analogous art: Both describe GaN HEMTs
Same transistors → Obvious to combine
2. KSR's use of known technique to improve similar devices in the same way.
Known technique, known device
→ Obvious to combine
3. KSR's some teaching, suggestion, motivation (TSM) in the prior art to modify or combine.
Yoshida/Beach TSM → Obvious to combine
4. Reasonable expectation of success: POSITA had reasonable expectation that *Beach*'s technique would further *Yoshida*'s goals of ohmic formation
Expectation to form ohmic contacts → Obvious to combine
5. EPC's counter arguments are incorrect
Beach's metal etching more precise than lift-off
→ Obvious to combine

Disputed Issue 3: Separate “Gate Photo Resistant Pattern” and “Metal photo Resistant Pattern”

Claim 1	Claim Limitation
1e1	depositing a gate contact layer on the doped GaN layer;
1e2	applying a gate photo resistant pattern ;
1e3	etching away the gate contact layer outside the gate region;
1e4	etching away the doped GaN layer, except a portion of the doped GaN layer beneath the gate contact;
1e5	removing the gate photo resistant pattern;

Claim 1	Claim Limitation
1g1	depositing an Ohmic contact metal;
1g2	applying a metal photo resistant pattern ;
1g3	etching the Ohmic contact metal;
1g4	removing the metal photo resistant pattern; and
1g5	performing rapid thermal annealing to form Ohmic drain and source contacts.

Issue	EPC’s Argument	Correct Resolution
The combination teaches separate “gate photo resistant pattern” and “metal photo resistant pattern”	<i>Beach</i> teaches a single pattern for forming the gate structure and ohmic contacts.	<i>Beach</i> teaches separate “gate photo resistant pattern” and “metal photo resistant pattern”; <i>Yoshida</i> teaches forming the gate structure and ohmic structure in separate steps

The Board Correctly Found that *Beach* teaches different patterns

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INNOSCIENCE (ZHUHAI) TECHNOLOGY COMPANY, LTD.,
AND
INNOSCIENCE AMERICA, INC.
Petitioner,

v.

EFFICIENT POWER CONVERSION CORPORATION,
Patent Owner.

IPR2023-01383
Patent 8,404,508 B2

Before JON B. TORNQUIST, JEFFREY W. ABRAHAM, and
KIMBERLY McGRAW, *Administrative Patent Judges*.

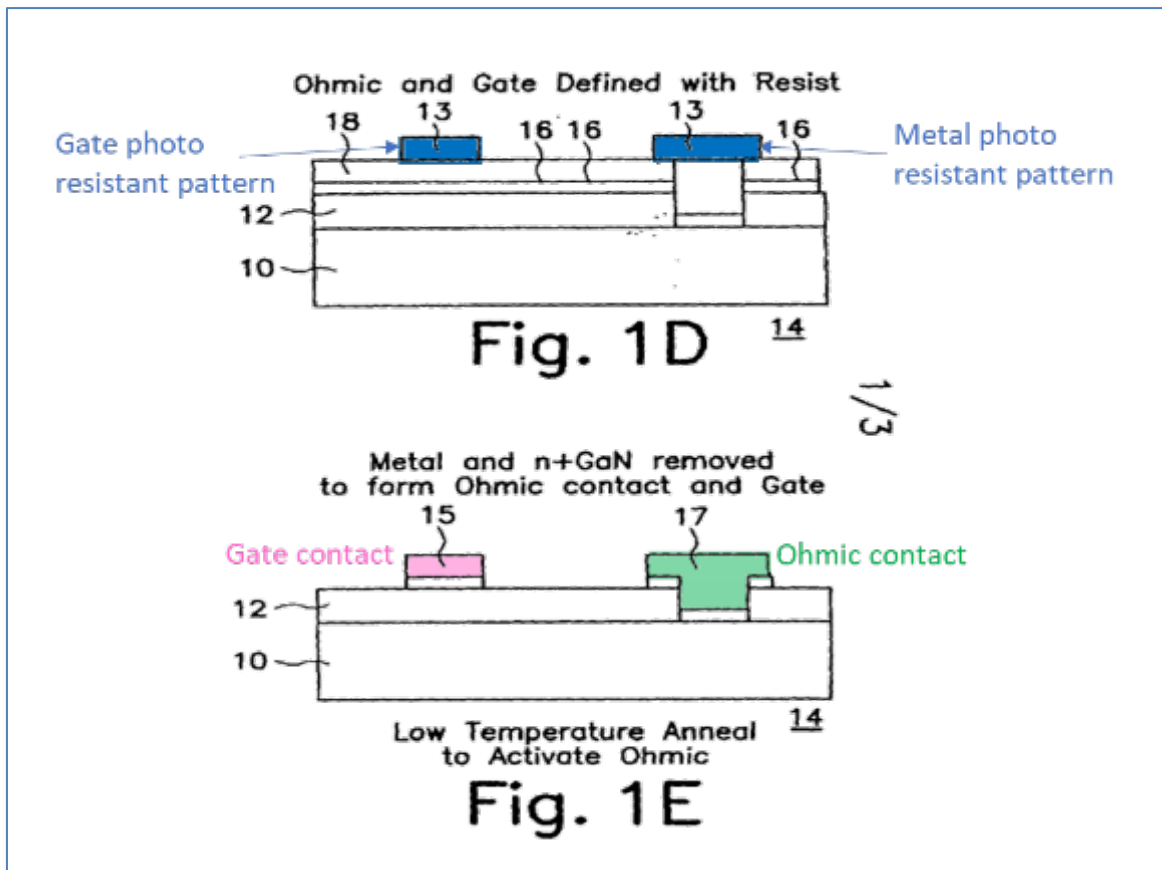
McGRAW, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

Although Beach deposits resist 13 in a single step, the resist is applied in different locations with varying types of layers underneath. Thus, depending on where resist layer 13 is applied, resist layer 13 appears to function as a different type of pattern, (i.e., as either as a gate photo resistant pattern or a metal photo resistant pattern). Again, as noted above, based on the present record, claim 1 does not require that the gate photo resistant pattern and the metal photo resistant pattern be applied at different times.

Paper No. 11, 28

***Beach* Teaches Separate “Gate Photo Resistant Pattern” and “Metal Photo Resistant Pattern”**



Beach, Figs. 1D, 1E

Yoshida-Beach Renders Obvious Forming Gate Structure and Ohmic Contacts in Separate Steps

- Even if separate steps are required, *Yoshida* forms its gate structure and ohmic contacts in separate steps

Ohmic Formation

was to be loaded and exposing the n-type InGaN layer 4. An SiO₂ film was then deposited by plasma CVD to cover the entire surface, and after patterning with photoresist, the area including the part where the gate electrode was to be loaded was masked, [leaving] the portion where source and drain electrodes were to be loaded open, and metal Al deposited on the exposed n-type InGaN layer 4 to load source electrode S and drain electrode D.

Yoshida, [0022]

Gate Formation

Lastly, after etching away the masking and opening the SiO₂ film beneath it, the source electrode S and drain electrode G locations were masked with SiO₂ film, Au was deposited in the opening portions, and gate electrodes G were loaded above the p-type GaN layer 5 to fabricate the HEMT shown in Fig. 1. With this HEMT, a drain current (*I_{ds}*) of 60 mA under an applied gate

Yoshida, [0023]

Yoshida-Beach Renders Obvious Separate Patterns for Gate and Metal Photo Resistant Patterns

- The Petition explains *Yoshida* forms its gate structure and ohmic contacts in separate steps, rendering obvious applying gate and metal photo resistant patterns at separate steps

Yoshida discloses how to form this GaN HEMT:

1. grow layers 2-5 over the **substrate 1** in this order;
2. etch away the **p-GaN layer** except where the **gate** is to be loaded;
3. deposit a dielectric layer to cover the entire surface;
4. apply a mask, open the source and drain contact area in the dielectric layer;
5. deposit the source and drain electrodes on the “exposed” **n-type AlGaN layer**;⁴
6. remove the mask and form the **gate contact** above the **p-GaN layer** to produce an enhancement mode GaN transistor.

Pet. 14-15

Yoshida-Beach Renders Obvious Separate Patterns for Gate and Metal Photo Resistant Patterns

- The Petition explains *Yoshida* forms its gate structure and ohmic contacts in separate steps

Yoshida in view of *Beach* renders obvious [1e]. Shealy, ¶115. *Yoshida*

Yoshida discloses forming a gate electrode G (gate contact) over the p-GaN

layer 5, as shown below. *Yoshida*, [0009], [0016], [0023].

Yoshida discloses that, to form the p-GaN layer and gate contact, the p-GaN layer was etched away “except where the gate electrode was to be loaded.”

Yoshida, [0022]. Then the gate electrode is loaded above the p-GaN layer. *Yoshida*, [0023]. Although Figure 1 shows that the p-GaN layer 5 extends beyond the gate

Pet. 30-31

Yoshida in view of *Beach* renders obvious [1g]. Shealy, ¶135. *Yoshida*

discloses depositing metal Al (ohmic contact metal) on the n-type semiconductor

layer 4 to load source electrode S and drain electrode D (ohmic source and drain

contacts). *Yoshida*, [0022], [0010]; Shealy, ¶135.

Pet. 35

Disputed Issue 3: Separate “Gate Photo Resistant Pattern” and “Metal photo Resistant Pattern”

Issue	EPC’s Argument	Correct Resolution
The combination teaches separate “gate photo resistant pattern” and “metal photo resistant pattern”	<i>Beach</i> teaches a single pattern for forming the gate structure and ohmic contacts.	<i>Beach</i> teaches separate “gate photo resistant pattern” and “metal photo resistant pattern”; <i>Yoshida</i> teaches forming the gate structure and ohmic structure in separate steps

Although not required by the claims, the *Yoshida-Beach* combination teaches applying separate patterns in separate steps

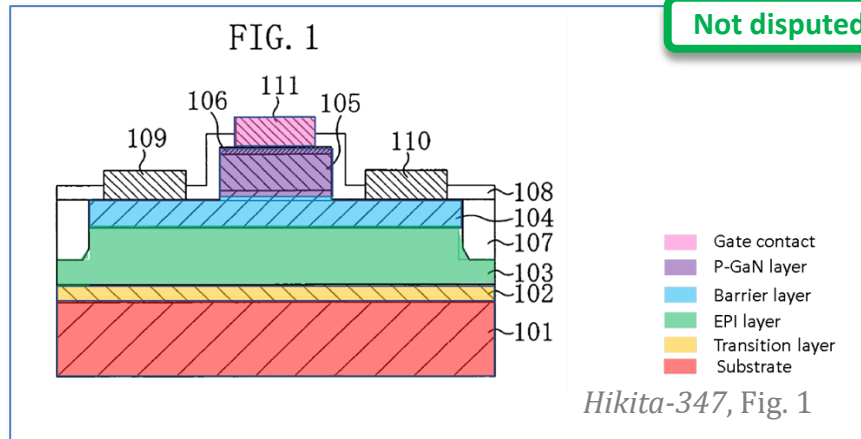
Yoshida-Beach-Sheppard Renders Obvious Claim 1

Claim 1	Claim Limitation	
1pre	A method of forming an enhancement mode GaN transistor, the method comprising:	✓
1a	nucleating and growing transition layers on a substrate;	✓
1b	growing an III Nitride EPI layer over the transistor layers;	✓
1c	growing an III Nitride barrier layer over the EPI layer;	✓
1d	growing a GaN layer with acceptor type dopants over the barrier layer;	✓
1e1	depositing a gate contact layer on the doped GaN layer;	✓
1e2	applying a gate photo resistant pattern;	✓
1e3	etching away the gate contact layer outside the gate region;	✓
1e4	etching away the doped GaN layer, except a portion of the doped GaN layer beneath the gate contact;	✓
1e5	removing the gate photo resistant pattern;	✓
1f1	depositing a dielectric layer;	✓
1f2	applying a contact photo resistant pattern;	✓
1f3	etching the dielectric layer to open the drain and source contact area;	✓
1f4	removing the contact photo resistant pattern;	✓
1g1	depositing an Ohmic contact metal;	✓
1g2	applying a metal photo resistant pattern;	✓
1g3	etching the Ohmic contact metal;	✓
1g4	removing the metal photo resistant pattern; and	✓
1g5	performing rapid thermal annealing to form Ohmic drain and source contacts.	✓

Ground 2: *Hikita-347, Beach, and Sheppard*

Overview of Prior Art

Hikita-347 teaches the claimed process except a process for self-aligned gate and ohmic contacts, using a mask to open source and drain contact area, and growing multiple transition layers

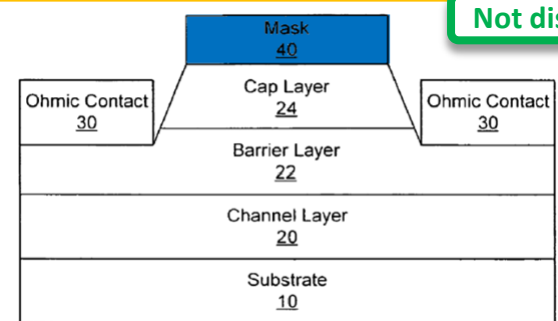
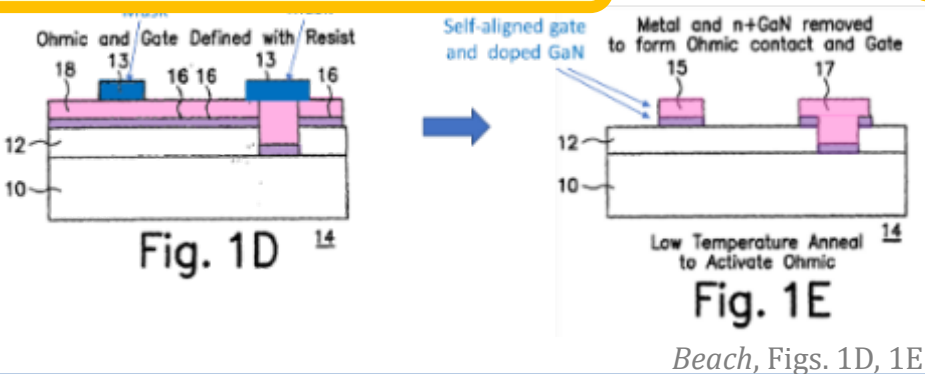


Beach teaches a process for self-aligned gate and ohmic contacts

Not disputed

Sheppard teaches using a mask to open source and drain contact area and growing multiple transition layers

Not disputed



Hikita-347-Beach-Sheppard Renders Obvious Claim 1

Like in *Yoshida* ground, the only disputed issues are motivation to combine

Claim Limitation

forming an enhancement mode GaN transistor, the method comprising:

Hikita-347 & Sheppard	Epitaxial layers formation	1a	nucleating and growing transition layers on a substrate;
		1b	growing an III Nitride EPI layer over the transistor layers;
		1c	growing an III Nitride barrier layer over the EPI layer;
		1d	growing a GaN layer with acceptor type dopants over the barrier layer;
Hikita-347 & Beach	Gate formation (alleged novelty)	1e1	depositing a gate contact layer on the doped GaN layer;
		1e2	applying a gate photo resistant pattern;
		1e3	etching away the gate contact layer outside the gate region;
		Disputed Issue #1: motivation to combine Hikita-347 with Beach	
Hikita-347 & Sheppard	Dielectric layer formation		lay the doped GaN layer, except a portion of the gate photo resistant pattern;
		1f1	depositing a dielectric layer;
		1f2	applying a contact photo resistant pattern;
		1f3	etching the dielectric layer to open the drain and source contact area;
Hikita-347 & Beach	Ohmic formation	1f4	removing the contact photo resistant pattern;
		1g1	depositing an Ohmic contact metal;
		1g2	applying a metal photo resistant pattern;
		1g3	etching the Ohmic contact metal;
		Disputed Issue #2: motivation to combine Hikita-347 with Beach	
		g the metal photo resistant pattern; and	
		ing rapid thermal annealing to form Ohmic drain and source contacts.	

Disputed Issue #3: teaching of separate gate and metal photo resistant pattern

Pet. 42-61: POR 53-63

Disputed Issue #1:
motivation to combine
Hikita-347 with Beach

Disputed Issue #3: teaching of
separate gate and metal
photo resistant pattern

Disputed Issue #2:
motivation to combine
Hikita-347 with Beach

Disputed Claim Elements (Claim 1)

Disputed Issue 1	Disputed Issue 2	Disputed Issue 3
EPC argues 1) a gate first construction, and 2) lack of motivation to combine <i>Hikita-347</i> with <i>Beach</i> 's gate formation	EPC argues lack of motivation to combine <i>Hikita-347</i> with <i>Beach</i> 's ohmic formation	EPC argues the combination does not teach separate "gate photo resistant pattern" and "metal photo resistant pattern"

Similar issues as in *Yoshida* ground

Disputed Issue 1: Motivation to Combine for the Gate Formation Steps

Claim 1	Claim Limitation
1e1	depositing a gate contact layer on the doped GaN layer;
1e2	applying a gate photo resistant pattern;
1e3	etching away the gate contact layer outside the gate region;
1e4	etching away the doped GaN layer, except a portion of the doped GaN layer beneath the gate contact;
1e5	removing the gate photo resistant pattern;

Motivation to combine:

Why would a POSITA incorporate *Beach's* self-aligned single mask gate formation process into *Hikita-347*?

Motivation to Combine *Hikita-347* with *Beach* for the Gate Formation Steps

1. Analogous art: Both describe GaN transistors
2. KSR's use of known technique to improve similar devices in the same way.
3. KSR's some teaching, suggestion, motivation (TSM) in the prior art to modify or combine.
4. Reasonable expectation of success: POSITA had reasonable expectation that *Beach*'s technique would further *Hikita-347*'s goals of gate alignment
5. EPC's counter arguments are incorrect

Motivation to Combine *Hikita-347* with *Beach* for the Gate Formation Steps

1. Analogous

2. Known technique

3. TSM

4. Expectation

5. Rebuttal to EPC

Hikita-347 and *Beach* are analogous art, they both specifically describe techniques for forming GaN transistors

Hikita-347 [0002]

The present invention relates to a field-effect transistor using nitride semiconductor, which is applicable to a power transistor for use in a power supply circuit of a consumer-electronics product such as a TV set and a method for fabricating the field-effect transistor.

Beach [0002], [0004]

The present invention relates generally to formation of a III-nitride material system device.

The devices fabricated for these types of applications are based on general device structures that exhibit high electron mobility and are referred to variously as heterojunction field effect transistors (HFETs), high electron mobility transistors (HEMTs) or modulation doped field effect transistors (MODFETs).

Using *Beach's* Known Technique to Improve *Hikita-347's* Similar Device

1. Analogous

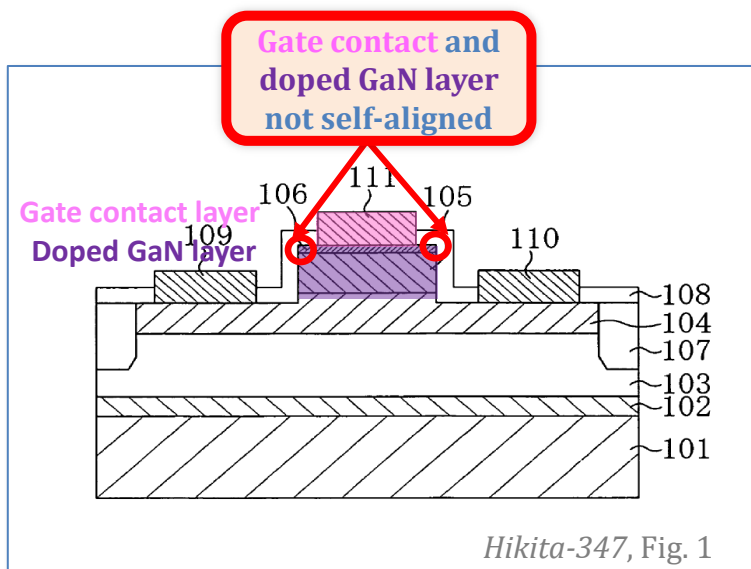
2. Known technique

3. TSM

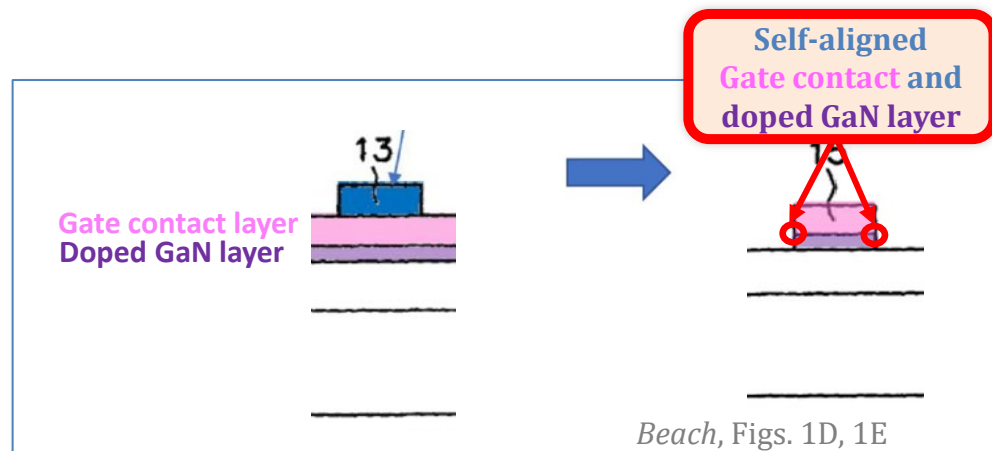
4. Expectation

5. Rebuttal to EPC

Hikita-347-Beach is using a known technique (*Beach's* self-aligned single mask gate process) to improve similar devices (*Hikita-347's* transistor) in the same way (using a single mask to etch the gate contact and doped GaN layers)



Hikita-347's similar
GaN transistor



Beach's known technique improves gate alignment and saves cost of applying a second mask

Some TSM to use *Beach's* gate process in *Hikita-347*

1. Analogous

2. Known technique

3. TSM

4. Expectation

5. Rebuttal to EPC

Hikita-347 expressly states to etch away the p-type GaN layer “located in other part than the gate region,” which is achieved by *Beach*

Hikita-347 [0035]

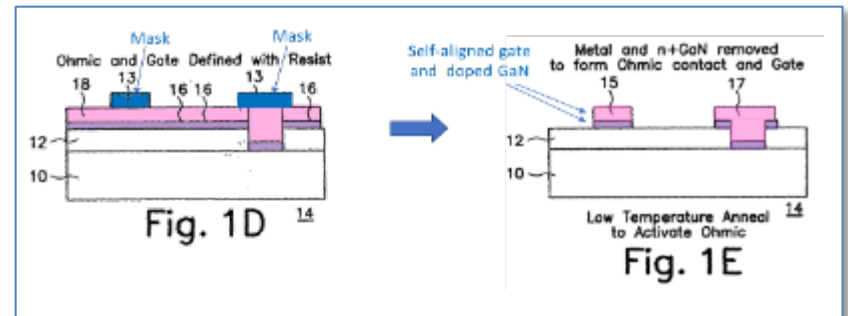
Parts of the heavily doped p-type GaN layer 106 and the p-type GaN layer 105 located in other part than a gate region is removed by selective etching.

Hikita-347 suggests self-alignment is desirable because it aims to remove all the p-type GaN layer except underneath the gate

Beach achieves *Hikita-347's* objective: etching the doped GaN layer except the area under gate contact

Beach [0047]

After the deposition of photoresist layer 13, material 18 is removed, as by etching, except where protected by photoresist 13. The removal, or etching process, also eliminates protective layer 16 under patterned photoresist 13.



Beach, Figs. 1D, 1E

Pet. 48-49, 21-22

A POSITA Would Have Reasonable Expectation of Success

1. Analogous 2. Known technique 3. TSM 4. Expectation 5. Rebuttal to EPC

A POSITA would have expected success in implementing *Beach's* self-aligned single mask gate process in *Hikita-347* because etching multiple layers of materials using the same mask was well understood and implemented decades before the '508 patent

Hikita-347's device. *Hikita-347's* technique described by *Beach*, ac

According to Dr. Shealy, Incorporating *Beach's* self-aligned gate process in *Hikita-347* requires only a simple modification

and etching. Using *Beach's* single mask process to etch the gate contact and doped

GaN layer in *Hikita-347's* device would have required only conventional

techniques in their ordinary and expected manner, because using the same mask to

etch different layers of materials was routine, conventional, and well understood in

the art. Thus, a POSITA would have reasonably expected to succeed in using

Beach's single mask process to form *Hikita-347's* GaN device.

Shealy, ¶184

Pet. 48-49, 21-22

A POSITA Would Have Reasonable Expectation of Success

1. Analogous

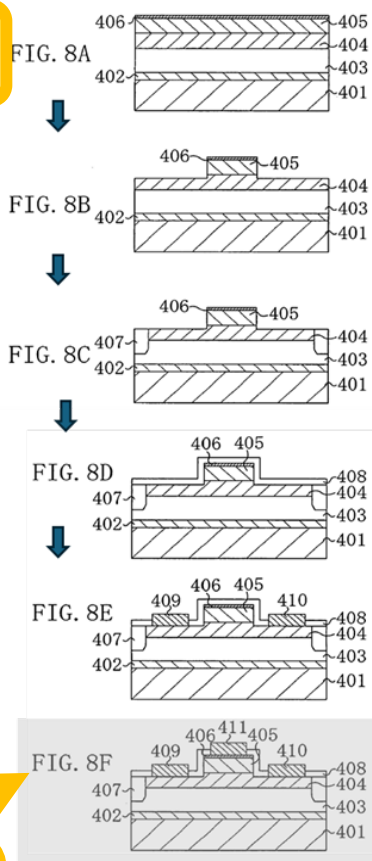
2. Known technique

3. TSM

4. Expectation

5. Rebuttal to EPC

**Hikita-347's
D-O-G Process**

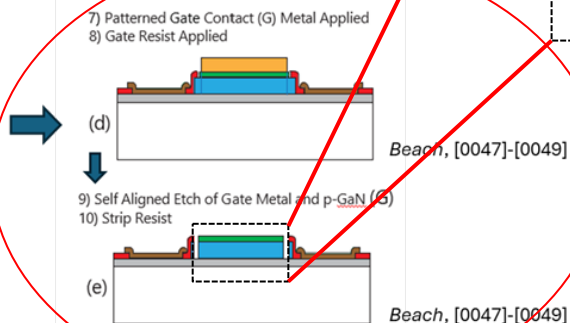


Hikita-347, Figs. 8A-8F

Incorporating Beach's self-aligned gate process in Hikita-347 requires only a simple modification



* Source/Drain Contacts



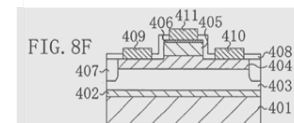
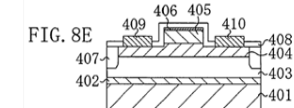
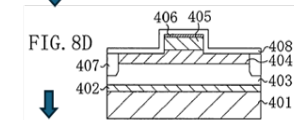
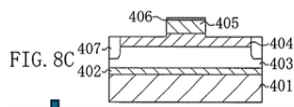
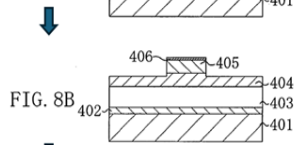
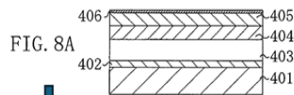
**Self-aligned
Gate contact and
doped GaN layer**



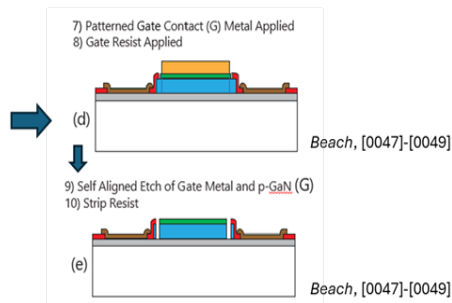
**The gate etching
step of Hikita-347
is modified**

The Petition Explains a POSITA Would have Expected Success in Applying Beach's Single Mask Gate Process in *Hikita-347*

Not a new argument



Hikita-347, Figs. 8A-8F



region. *Hikita-347*, [0057]. A POSITA would have been motivated to use *Beach*'s single mask process to form the gate contact and p-type GaN layer(s) in *Hikita-347*'s device and expected success for the same reasons explained in Ground 1. Shealy, ¶¶179, 229; §VIII.A.1.d.ii.

Pet. 49

A POSITA would have expected success because applying a single mask to form the gate contact and doped GaN layer was a well-known and conventional technique. Shealy, ¶127. The '508 patent states that the etching of the gate contact and p-GaN layer using the same mask is performed by "any known technique," because etching multiple layers of different materials using the same mask was routine, conventional, and well understood in the art. Ex. 1001, 3:45-50; Shealy, ¶127. Indeed, using the same mask to etch different layers of materials in semiconductor devices was known and implemented decades before the '508

Pet. 22

Reply 27, *ShealySupp*, ¶31

A POSITA Would Have Reasonable Expectation of Success

1. Analogous 2. Known technique 3. TSM 4. Expectation 5. Rebuttal to EPC

D-O-G Process
incorporating self-aligned gate process

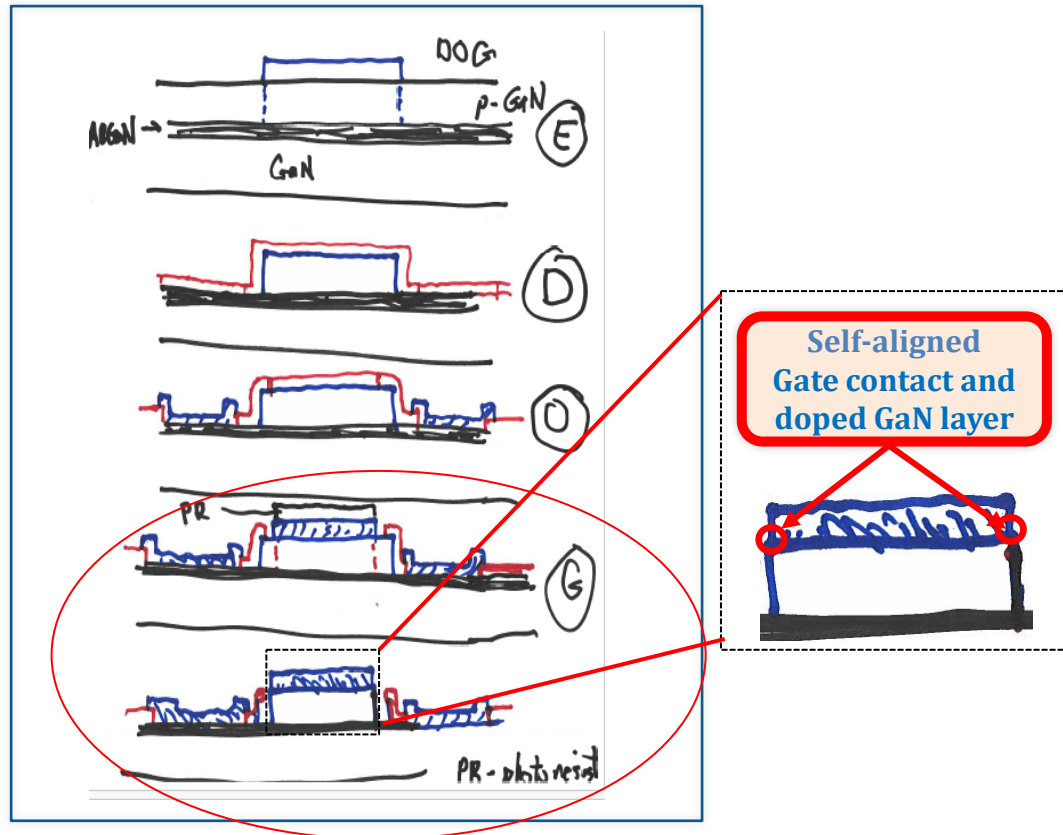
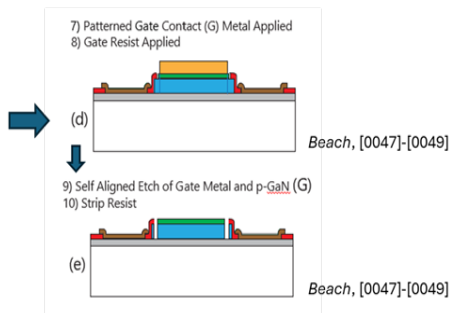
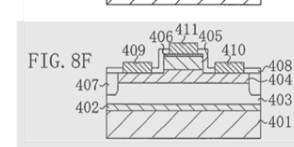
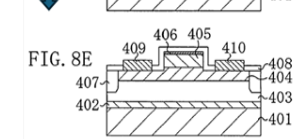
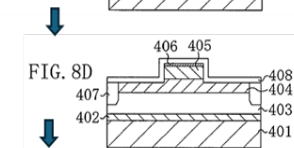
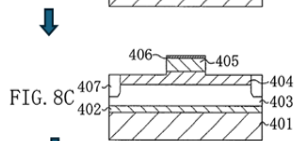
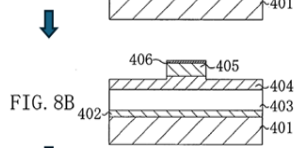
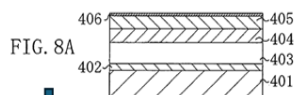


Exhibit prepared by Dr. Shealy at Depo.
(Exs. 1040, 2003), 2

Patent Owner Demands for Additional Explanation of the Combination

Not a new argument



As in Ground 1, Petitioner fails to particularly describe its proposed combination sufficient to permit any analysis as to how the “jigsaw puzzle” is assembled. See §VII.A. Generally, Petitioner proposes the same modifications to *Hikita347* as it proposed to *Yoshida* with respect to gate formation and ohmic contact formation and identified the same motivations to combine.

POR 54



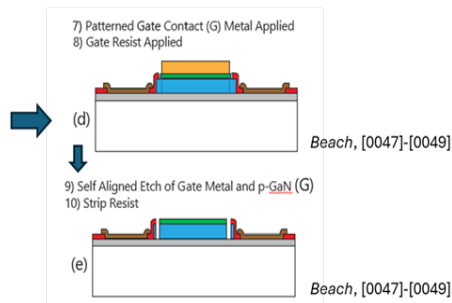
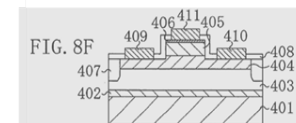
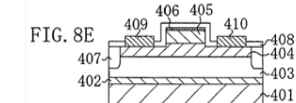
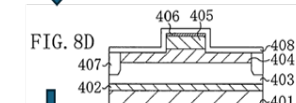
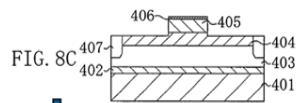
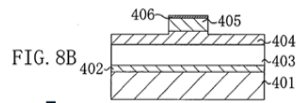
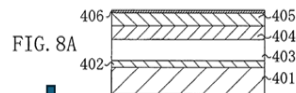
“[T]he very nature of the reply and sur-reply briefs are to respond (whether to refute, rebut, explain, discredit, and so on) to prior raised arguments within the confines of 37 C.F.R. § 42.23(b).”

Rembrandt Diagnostics, LP v. Alere, Inc., 76 F.4th 1376, 1384 (Fed. Cir. 2023)

Reply 27, *ShealySupp*, ¶31

The Diagram Illustrating the *Hikita-347-Beach* Combination Is not a New Argument

Not a new argument



- The Petition explains the expectation of success in the *Hikita-347-Beach* combination
- Dr. Shealy further elaborates the step-by-step implementation of self-aligned D-O-G process in deposition
- The diagram is in response to EPC's demand for additional combination details in its Patent Owner's Response
- No change of references, no change of grounds

Hikita-347, Figs. 8A-8F

Reply 27



“Parties are not barred from elaborating on their arguments on issues previously raised.”

Chamberlain Grp., Inc. v. One World Techs., Inc., 944 F.3d 919, 925 (Fed. Cir. 2019)

EPC's Incorrect Arguments

- 1. Analogous
- 2. Known technique
- 3. TSM
- 4. Expectation
- 5. Rebuttal to EPC

Issue	EPC's Incorrect Argument	Correct Resolution
Motivation to combine: Why would a POSITA incorporate <i>Beach</i> 's self-aligned single mask gate formation process into <i>Hikita-347</i>	1. <i>Beach</i> and <i>Hikita-347</i> are not gate-first, so the combination cannot be gate-first. 2. Bodily incorporating <i>Beach</i>'s gate simultaneous process in <i>Hikita-347</i> would not work, and a POSITA would not be motivated to do so. 3. Bodily incorporating <i>Beach</i>'s depletion mode device with <i>Hikita-347</i>'s enhancement mode device would not work, and a POSITA would not be motivated to do so. 4. Bodily incorporating <i>Beach</i>'s gate and ohmic contact formed with the same material in <i>Hikita-347</i>'s device would not work, and a POSITA would not be motivated to do so. 5. The <i>Hikita-347-Beach</i> combination does not meet claim limitation [1e4].	A POSITA would have incorporated <i>Beach</i> 's self-aligned single mask gate formation process into <i>Hikita-347</i> to improve gate's alignment

Reply 26-27, 29-30

EPC's Incorrect Argument #1 of 5: No Motivation Because *Hikita-347* and *Beach* Do Not Teach a Gate-First Process

1. Gate-first 2. Gate-simultaneous 3. Depletion mode 4. Ohmic material 5. Limitation [1e4]

EPC incorrectly argues no motivation to combine because *Beach* and *Hikita-347* do not teach a gate-first process

- The Claims **do not** require a gate-first process
- A gate-first process would have been obvious

43. As I explained in my deposition, there are only six permutations of ordering in forming a gate contact, ohmic contacts, and dielectric layer, all of which are suitable options. Each of the permutations would have been obvious to a POSITA. And a POSITA would have found it obvious to try a gate-first G-D-O process and expected success to do so.

ShealySupp, ¶43

EPC's Incorrect Argument #2 of 5 : No Motivation Because *Beach* Is a Gate-Simultaneous Process

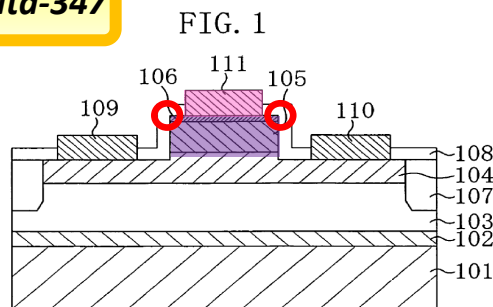
1. Gate-first 2. Gate-simultaneous 3. Depletion mode 4. Ohmic material 5. Limitation [1e4]

EPC incorrectly argues no motivation to combine because *Beach* is a gate-simultaneous process and *Hikita-347* is a gate-last process

**Bodily
Incorporation**

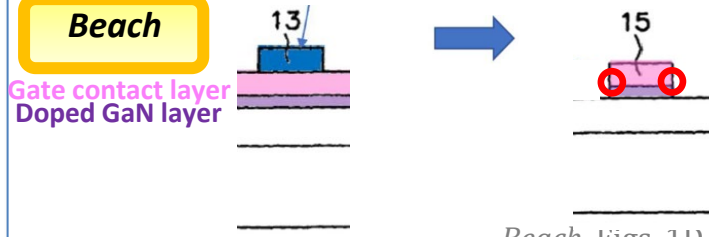
Beach is a gate-simultaneous process and *Hikita-347* is a gate-last process – does not matter

Hikita-347



Hikita-347, Fig. 1

Beach



Beach, Figs. 1D, 1E

The combination maintains *Hikita-347*'s process flow, but only substitutes *Beach*'s implementation details for the self-aligned gate formation

“It is well-established that a determination of obviousness ... **does not require an actual, physical substitution of elements.**”

In re Mouttet, 686 F.3d 1322, 1332 (Fed. Cir. 2012)

Reply 27, 15



EPC's Incorrect Argument #3 of 5 : No Motivation Because *Beach* Is a Depletion Mode Device

1. Gate-first 2. Gate-simultaneous 3. Depletion mode 4. Ohmic material 5. Limitation [1e4]

EPC incorrectly argues no motivation to combine because *Hikita-347*'s enhancement mode devices and *Beach*'s depletion mode devices are not combinable

**Bodily
Incorporation**

Petitioner's combination:
Incorporate *Beach*'s **self-aligned gate process**
into *Hikita-347*

The self-aligned gate process and ohmic process are **the same** for enhancement mode and depletion mode devices

Q. Would *Beach*'s self-aligned etching process be performed the same regardless of what mode the device was?

A. Yes.

A. The only difference in this technique to achieve an enhancement mode device is the presence of one additional p-type layer above the barrier; everything else about the structure is the same, and of course, one skilled in the art very likely works on both including I believe *Beach* has papers in both.

But in any case, one skilled in the art is familiar with both devices and they process the same as far as the ohmic and gate contacts.

EPC's Incorrect Argument #3 of 5 : No Motivation Because *Beach* Is a Depletion Mode Device

1. Gate-first 2. Gate-simultaneous 3. Depletion mode 4. Ohmic material 5. Limitation [1e4]

***Beach* Teaches an Enhancement Mode Device**

... controlled by a nominally on device. Accordingly, it would be desirable to create a III-nitride heterojunction device that is nominally off to avoid current conduction problems during start-up and other modes. *Beach*, [0004]

[0012] A number of types of power devices can potentially benefit from a nominally off device with low on resistance. For example, it would desirable to obtain a power switch, power rectifier, synchronous rectifier, current control device or other power devices that are nominally off when no power is applied. Current control devices can *Beach*, [0012]

12 Q. If "nominally on" means depletion mode, then
13 "nominally off" would mean enhancement mode, right?
14 A. Generally, "normally on" refers to a depletion
15 mode transistor and "normally off" refers to an enhancement
16 mode transistor.

Schubert Tr. (Ex. 1053), 1025:12-16

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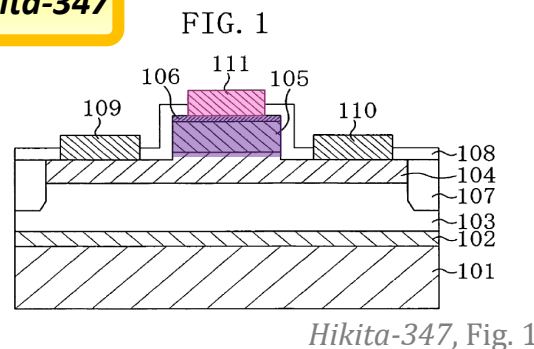
EPC's Incorrect Argument #4 of 5 : No Motivation Because *Beach*'s Gate Contact and Ohmic Contacts Are Formed of the Same Material

1. Gate-first 2. Gate-simultaneous 3. Depletion mode 4. Ohmic material 5. Limitation [1e4]

EPC incorrectly argues no motivation to combine because *Beach* teaches the same electrode metal for its gate and ohmic contacts and *Hikita-347* teaches different materials

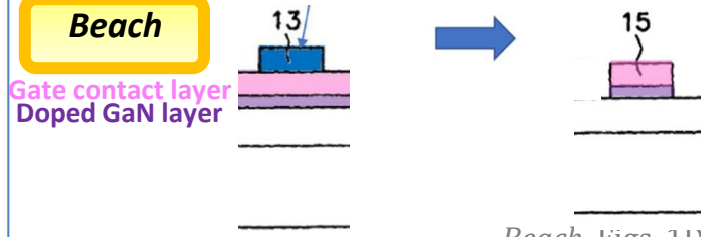
Beach uses the same metal for gate and ohmic contact – does not matter

Hikita-347



Hikita-347, Fig. 1

Beach



Beach, Figs. 1D, 1E

Bodily Incorporation

The combination maintains *Hikita-347*'s process flow, but only substitutes *Beach*'s implementation details for the self-aligned gate formation

“It is well-established that a determination of obviousness ... **does not require an actual, physical substitution of elements.**”

In re Mouttet, 686 F.3d 1322, 1332 (Fed. Cir. 2012)
Reply 29-30; POR 59-60



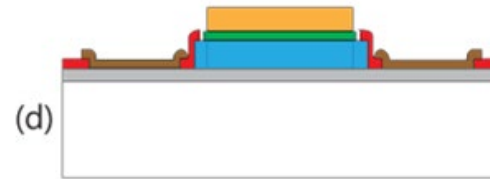
EPC's Incorrect Argument #5 of 5 : the Modified *Hikita-347* Process Does Not Meet [1e4]

1. Gate-first 2. Gate-simultaneous 3. Depletion mode 4. Ohmic material 5. Limitation [1e4]

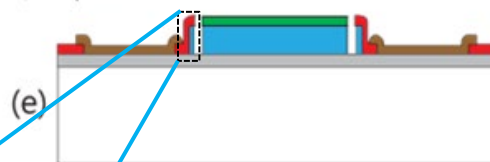
EPC in its sur-reply first raises the new argument that the *Hikita-347-Beach* combination does not meet limitation [1e4] because it would result in remnant p-type GaN islands outside the gate area

Claim 1	Claim Limitation
1e1	depositing a gate contact layer on the doped GaN layer;
1e2	applying a gate photo resistant pattern;
1e3	etching away the gate contact layer outside the gate region;
1e4	etching away the doped GaN layer, except a portion of the doped GaN layer beneath the gate contact;
1e5	removing the gate photo resistant pattern;

7) Patterned Gate Contact (G) Metal Applied
8) Gate Resist Applied

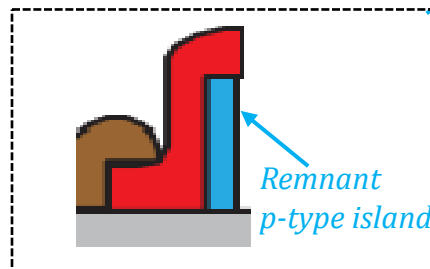


9) Self Aligned Etch of Gate Metal and p-GaN (G)
10) Strip Resist



* Source/Drain Contacts

Improper new argument by EPC

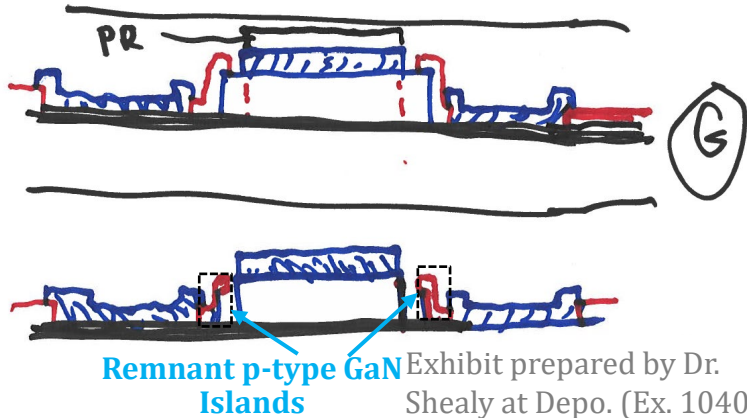


EPC improperly argues that the *Remnant p-type GaN Island* does not meet limitation [1e4]

Sur-Reply 28-29

EPC Improperly Argues that the Modified *Hikita-347* Process Does Not Meet Claim Limitation [1e4]

1. Gate-first
2. Gate-simultaneous
3. Depletion mode
4. Ohmic material
5. Limitation [1e4]

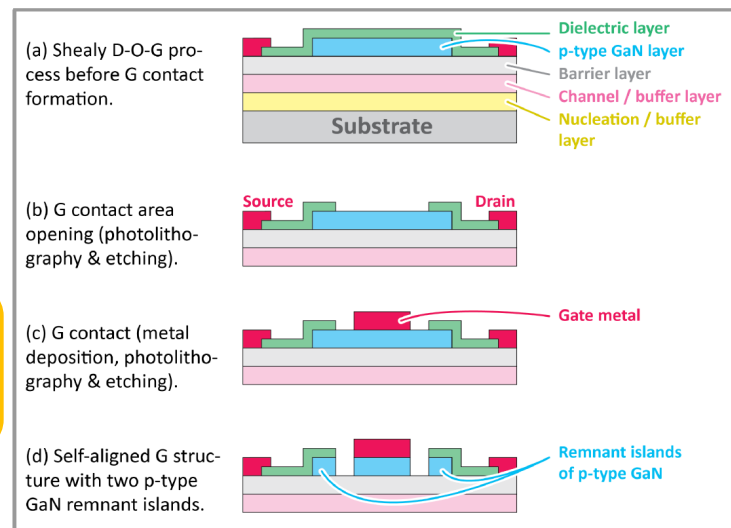


Dr. Shealy's deposition testimony provided the DOG process with remnant p-GaN island

EPC argued in its POR regarding the functionality of the remnant p-type GaN islands, but never raised any argument against [1e4]

EPC's new argument should not be allowed

prior art. EX2001 ¶¶89-90. Importantly, the gate electrode process as described by Dr. Shealy would not work because it would leave remnant islands of the p-type semiconductor, for example, p-type GaN in the context of the '508 patent, between the source and gate as well as between the gate and drain. Such remnant islands (shown below) are detrimental to the function of an enhancement mode HEMT and a POSA would not proceed in such a manner. *Id.* at ¶90.



EX2001 ¶90

POR 23

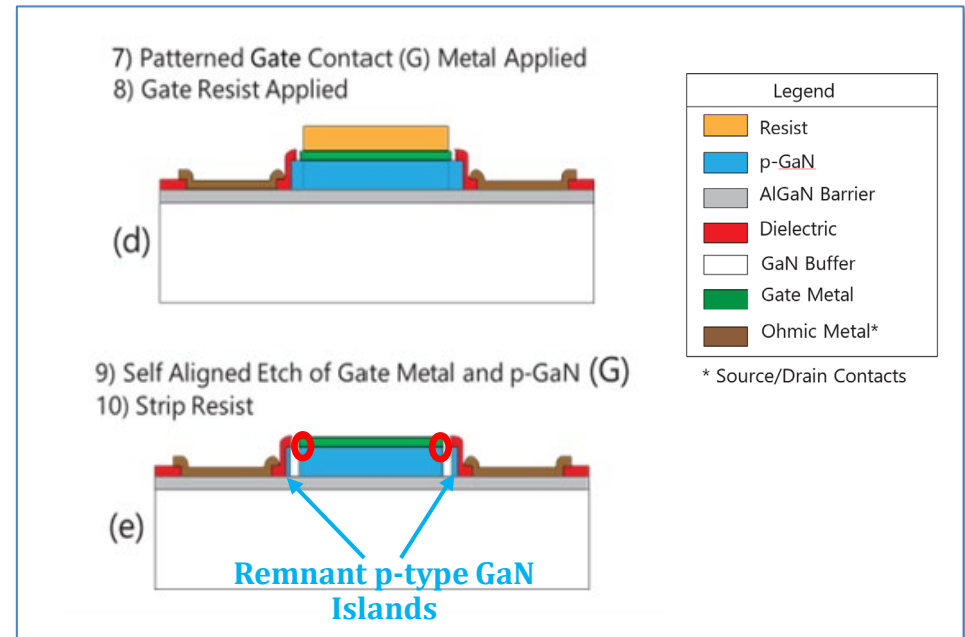
Modified *Hikita-347* Process Meets Claim Limitation [1e4]

1. Gate-first
2. Gate-simultaneous
3. Depletion mode
4. Ohmic material
5. Limitation [1e4]

Claim 1	Claim Limitation
1e1	depositing a gate contact layer on the doped GaN layer;
1e2	applying a gate photo resistant pattern;
1e3	etching away the gate contact layer outside the gate region;
1e4	etching away the doped GaN layer, except a portion of the doped GaN layer beneath the gate contact;
1e5	removing the gate photo resistant pattern;

Modified *Hikita-347* process with **remnant p-type GaN Islands** meet [1e4]:

1. the **p-type GaN** outside of the **gate region** is etched
2. the **p-type GaN** outside the **photoresistant pattern** is etched
3. the **gate metal** and **p-type GaN** are self-aligned

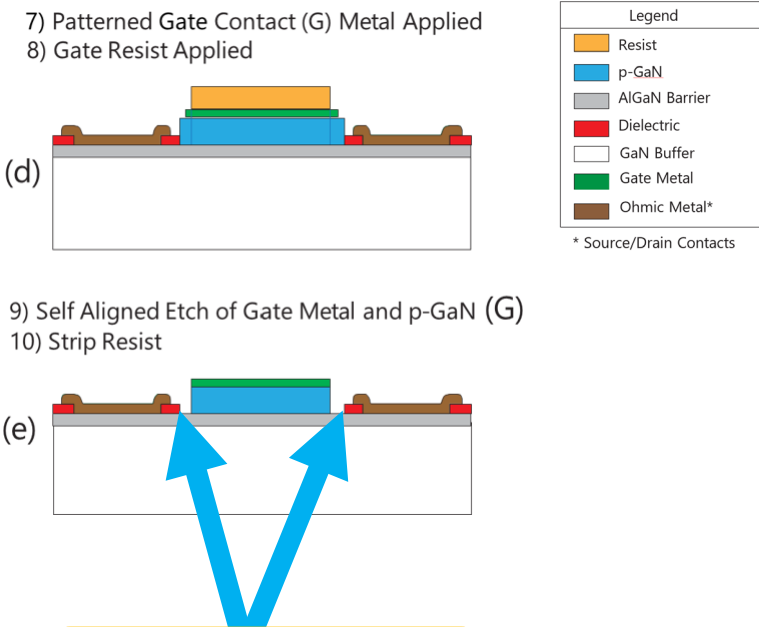


Modified *Hikita-347* Process Meets Claim Limitation [1e4]

1. Gate-first
2. Gate-simultaneous
3. Depletion mode
4. Ohmic material
5. Limitation [1e4]

Dr. Shealy explains that the remnant p-type GaN islands can be eliminated by applying appropriate photoresist, indisputably meeting limitation [1e4]

Claim 1	Claim Limitation
1e1	depositing a gate contact layer on the doped GaN layer;
1e2	applying a gate photo resistant pattern;
1e3	etching away the gate contact layer outside the gate region;
1e4	etching away the doped GaN layer, except a portion of the doped GaN layer beneath the gate contact;
1e5	removing the gate photo resistant pattern;



Unrebutted in EPC's Sur-Reply

No Remnant
p-type GaN Islands

Motivation to Combine *Hikita-347* with *Beach* for the Gate Formation Steps

1. Analogous art: Both describe GaN transistors
Same transistors → Obvious to combine
2. KSR's use of known technique to improve similar devices in the same way.
Known technique, known device → Obvious to combine
3. KSR's some teaching, suggestion, motivation (TSM) in the prior art to modify or combine.
***Hikita-347/Beach* TSM → Obvious to combine**
4. Reasonable expectation of success: POSITA had reasonable expectation that *Beach*'s technique would further *Hikita-347*'s goals of gate alignment
Expectation to improve gate alignment → Obvious to combine
5. EPC's counter arguments are incorrect
Bodily incorporation is irrelevant → Obvious to combine

Disputed Issue 2: Motivation to Combine for the Ohmic Formation Steps

Claim 1	Claim Limitation
1g1	depositing an Ohmic contact metal;
1g2	applying a metal photo resistant pattern;
1g3	etching the Ohmic contact metal;
1g4	removing the metal photo resistant pattern; and
1g5	performing rapid thermal annealing to form Ohmic drain and source contacts.

Motivation to combine:

Why would a POSITA incorporate *Beach's* ohmic formation process into *Hikita-347*

Motivation to Combine *Hikita-347* with *Beach* for the Ohmic Formation Steps

1. Analogous art: Both describe GaN transistors
2. KSR's use of known technique to improve similar devices in the same way.
3. KSR's some teaching, suggestion, motivation (TSM) in the prior art to modify or combine.
4. Reasonable expectation of success: POSITA had reasonable expectation that *Beach*'s technique would further *Hikita-347*'s goal of ohmic formation
5. EPC's counter arguments are incorrect

Motivation to Combine *Hikita-347* with *Beach* for the Gate Formation Steps

1. Analogous

2. Known technique

3. TSM

4. Expectation

5. Rebuttal to EPC

Hikita-347 and *Beach* are analogous art, they both specifically describe techniques for forming GaN transistors

Hikita-347 [0002]

The present invention relates to a field-effect transistor using nitride semiconductor, which is applicable to a power transistor for use in a power supply circuit of a consumer-electronics product such as a TV set and a method for fabricating the field-effect transistor.

Beach [0002], [0004]

The present invention relates generally to formation of a III-nitride material system device.

The devices fabricated for these types of applications are based on general device structures that exhibit high electron mobility and are referred to variously as heterojunction field effect transistors (HFETs), high electron mobility transistors (HEMTs) or modulation doped field effect transistors (MODFETs).

Using *Beach's* Known Technique to Improve *Hikita-347's* Similar Device

1. Analogous

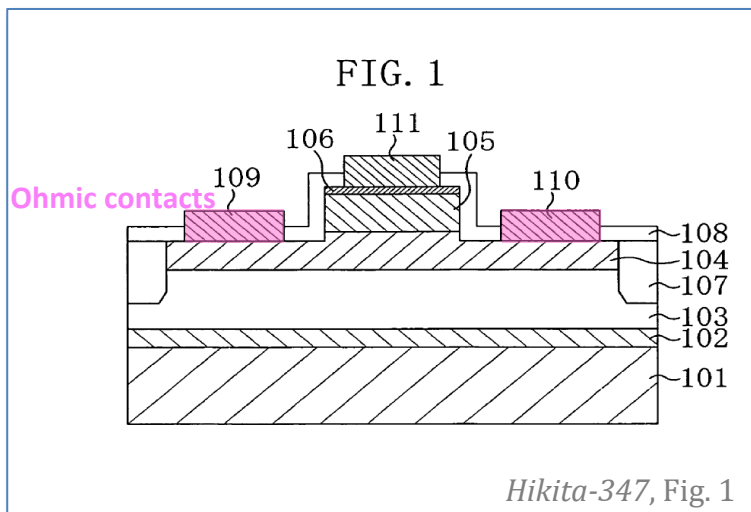
2. Known technique

3. TSM

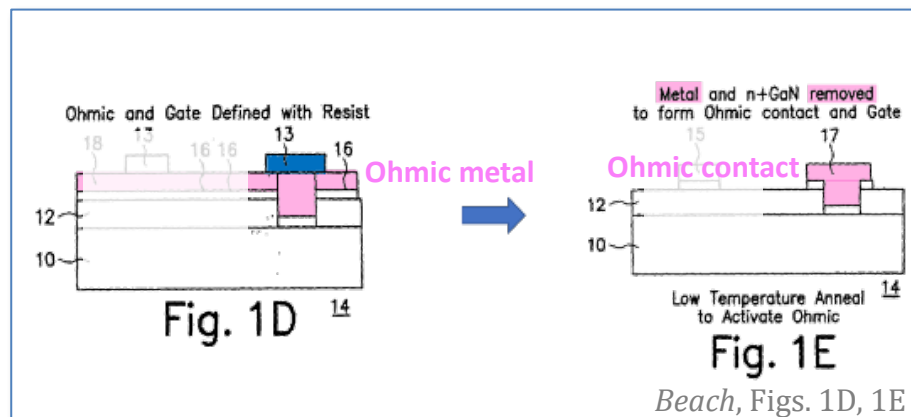
4. Expectation

5. Rebuttal to EPC

Hikita-347-Beach is using a known technique (*Beach's* masking and etching process) to improve similar devices (*Hikita-347's* transistor) in the same way (using masking and etching to form ohmic contacts)



***Hikita-347's* similar GaN transistor**



***Beach's* known technique to form ohmic contact is simpler than the alternative lift-off process and saves manufacturing cost**

Some TSM to use *Beach's* ohmic process in *Hikita-347*

1. Analogous 2. Known technique 3. TSM 4. Expectation 5. Rebuttal to EPC

***Hikita-347* expressly states to form ohmic contacts, but does not explain the implementation details which *Beach* provides**

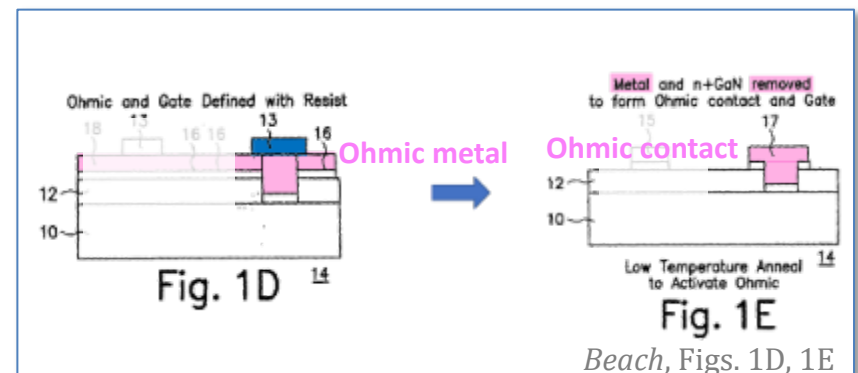
***Hikita-347* [0060]**

Next, as shown in FIG. 8E, openings are formed in a SiN film, for example, by ICP dry etching or the like. Each of a source electrode 490 and a drain electrode 410 is formed of a Ti layer and an Al layer in an associated one of the openings, and then heat treatment is performed thereto in an N₂ atmosphere at 650° C.

***Beach* achieves *Hikita-347's* objective: forming ohmic contacts**

***Beach* [0047]**

Referring now to Figure 1D, resist material 13 is deposited in a pattern to permit the formation of a gate 15 and ohmic contact 17. ... After the deposition of photoresist layer 13, material 18 is removed, as by etching, except where protected by photoresist 13.



A POSITA Would Have Reasonable Expectation of Success

1. Analogous 2. Known technique 3. TSM 4. Expectation 5. Rebuttal to EPC

A POSITA would have expected success in implementing *Beach's* ohmic process in *Hikita-347* because *Beach's* process of using a mask to pattern and etch ohmic metal was well-known and conventional

drain contacts. *Hikita-347's* Ohmic source and drain contacts could be formed using the masking process described by *Beach*, according to the known, routine process of masking and etching. Using *Beach's* masking process to etch the Ohmic contact metal in *Hikita-347's* device would have required only conventional techniques in their ordinary and expected manner, because using a mask to etch an Ohmic contact metal was routine, conventional, and well understood in the art.

Shealy, ¶205

EPC's Argument that No Motivation Because *Hikita-347* Teaches a Lift-Off Process Is Incorrect

1. Analogous

2. Known technique

3. TSM

4. Expectation

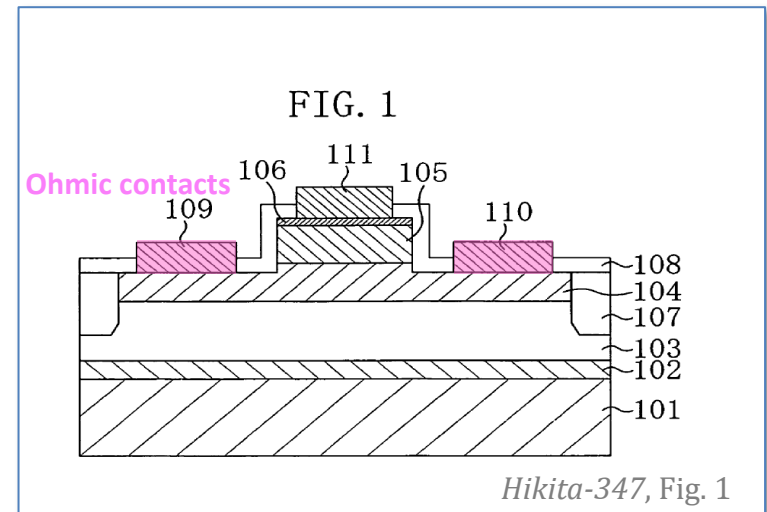
5. Rebuttal to EPC

EPC incorrectly argues no motivation to combine because *Hikita-347* discloses using a lift-off technique to form ohmic contacts

Hikita-347 [0060]

Next, as shown in FIG. 8E, openings are formed in a SiN film, for example, by ICP dry etching or the like. Each of a source electrode 490 and a drain electrode 410 is formed of a Ti layer and an Al layer in an associated one of the openings, and then heat treatment is performed thereto in an N₂ atmosphere at 650° C.

***Hikita-347* is silent as to any lift-off technique to form ohmic contacts**



Metal etching is more precise than lift-off and can produce vertical sidewalls

EPC's Incorrect Argument: No Motivation Because *Hikita-347* Teaches a Lift-Off Process

1. Analogous

2. Known technique

3. TSM

4. Expectation

5. Rebuttal to EPC

Metal Etching Produces Vertical Sidewalls like in *Hikita-347*

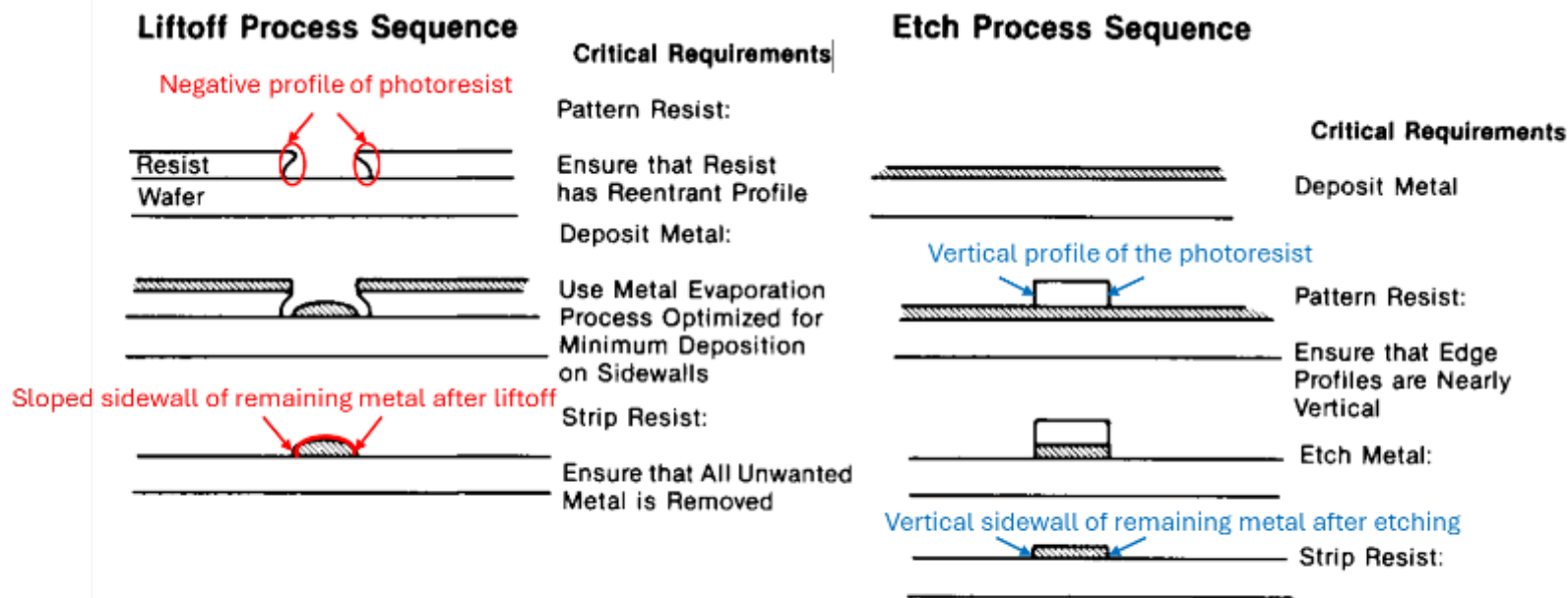


Fig. 1. Comparison of additive (lift-off) and subtractive (etch) metallization patterning processes.

Gorowitz, Fig. 1

EPC's Incorrect Argument: No Motivation Because *Hikita-347* Teaches a Lift-Off Process

1. Analogous

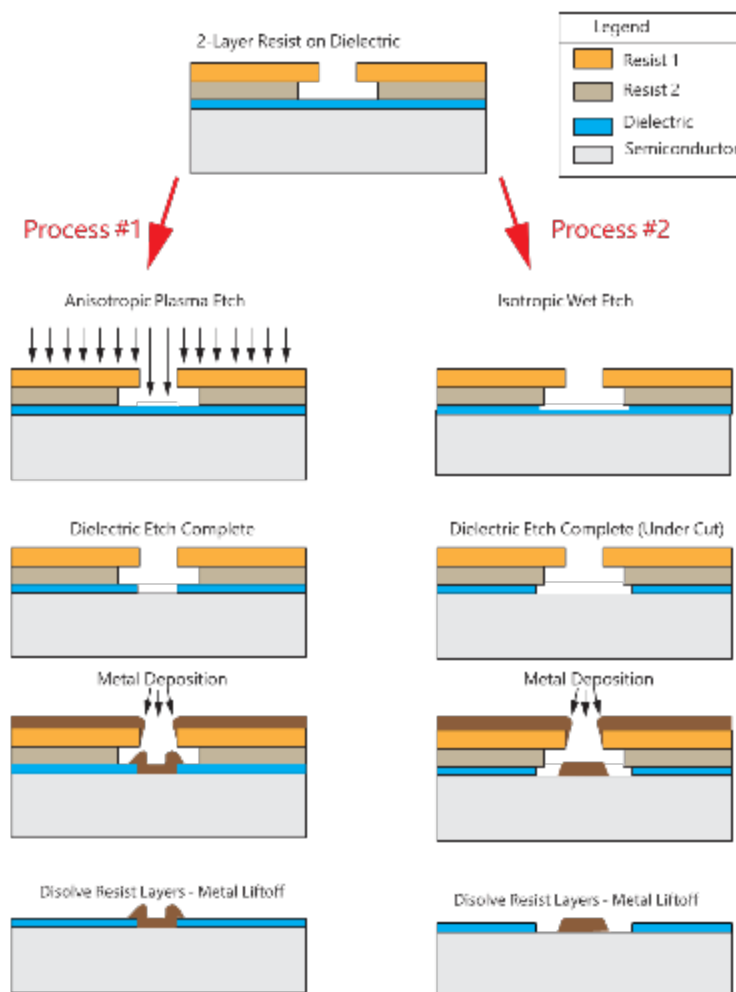
2. Known technique

3. TSM

4. Expectation

5. Rebuttal to EPC

Lift-off Does Not Produce Vertical Sidewalls like in *Hikita-347*



ShealySupp, ¶54

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Beach's Metal Etching Process Is an Obvious Design Choice

1. Analogous

2. Known technique

3. TSM

4. Expectation

5. Rebuttal to EPC

Only **two** prevalent alternatives, lift-off or metal etching. *Beach's* metal etching process provides benefits over lift-off and is an **obvious design choice**

metal dimensions. Further, as I explained in my previous declaration, lift-off and metal etching are the only two prevalent techniques for metal patterning. *Yoshida* does not suggest that performing an etching process or lift-off was critical to its method to form a GaN transistor. *Beach's* etching technique provides performance benefits over lift-off, e.g., more accurate and controllable to pattern the metal. Using a metal etching process to form the ohmic contacts, as taught by *Beach*, would be an obvious design choice to form the ohmic contacts of *Yoshida*. See *Gorowitz*, 4 (“When resist patterns are used to define metal layers, the process can be either additive [lift-off] or subtractive [etching].”).

ShealySupp, ¶56

Motivation to Combine *Hikita-347* with *Beach* for the Ohmic Formation Steps

1. Analogous art: Both describe GaN transistors
Same transistors → Obvious to combine
2. KSR's use of known technique to improve similar devices in the same way.
Known technique, known device
→ Obvious to combine
3. KSR's some teaching, suggestion, motivation (TSM) in the prior art to modify or combine.
Hikita-347/Beach TSM → Obvious to combine
4. Reasonable expectation of success: POSITA had reasonable expectation that *Beach*'s technique would further *Hikita-347*'s goals of ohmic formation
Expectation to form ohmic contacts → Obvious to combine
5. EPC's counter arguments are incorrect
Beach's metal etching more precise than lift-off
→ Obvious to combine

Disputed Issue 3: Separate “Gate Photo Resistant Pattern” and “Metal photo Resistant Pattern”

Claim 1	Claim Limitation
1e1	depositing a gate contact layer on the doped GaN layer;
1e2	applying a gate photo resistant pattern ;
1e3	etching away the gate contact layer outside the gate region;
1e4	etching away the doped GaN layer, except a portion of the doped GaN layer beneath the gate contact;
1e5	removing the gate photo resistant pattern;

Claim 1	Claim Limitation
1g1	depositing an Ohmic contact metal;
1g2	applying a metal photo resistant pattern ;
1g3	etching the Ohmic contact metal;
1g4	removing the metal photo resistant pattern; and
1g5	performing rapid thermal annealing to form Ohmic drain and source contacts.

Issue	EPC’s Argument	Correct Resolution
The combination teaches separate “gate photo resistant pattern” and “metal photo resistant pattern”	<i>Beach</i> teaches a single pattern for forming the gate structure and ohmic contacts.	<i>Beach</i> teaches separate “gate photo resistant pattern” and “metal photo resistant pattern”; <i>Hikita-347</i> teaches forming the gate structure and ohmic structure in separate steps

The Board Correctly Found that *Beach* teaches different patterns

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INNOSCIENCE (ZHUHAI) TECHNOLOGY COMPANY, LTD.,
AND
INNOSCIENCE AMERICA, INC.
Petitioner,

v.

EFFICIENT POWER CONVERSION CORPORATION,
Patent Owner.

IPR2023-01383
Patent 8,404,508 B2

Before JON B. TORNQUIST, JEFFREY W. ABRAHAM, and
KIMBERLY MCGRAW, *Administrative Patent Judges*.

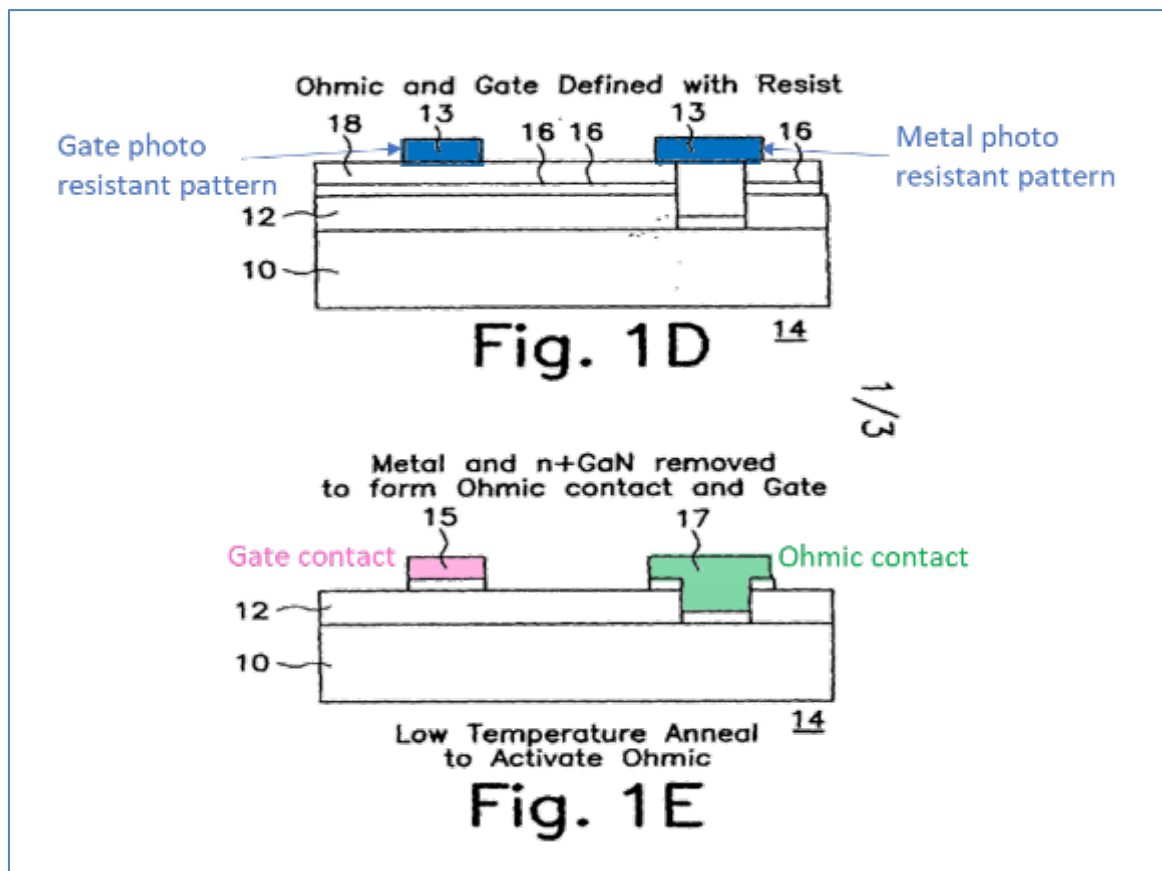
MCGRAW, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

Although Beach deposits resist 13 in a single step, the resist is applied in different locations with varying types of layers underneath. Thus, depending on where resist layer 13 is applied, resist layer 13 appears to function as a different type of pattern, (i.e., as either as a gate photo resistant pattern or a metal photo resistant pattern). Again, as noted above, based on the present record, claim 1 does not require that the gate photo resistant pattern and the metal photo resistant pattern be applied at different times.

Paper No. 11, 28

Beach Teaches Separate “Gate Photo Resistant Pattern” and “Metal Photo Resistant Pattern”



Beach, Figs. 1D, 1E

Hikita-347-Beach Renders Obvious Forming Gate Structure and Ohmic Contacts in Separate Steps

- Even if separate steps are required, *Hikita-347* forms its gate structure and ohmic contacts in separate steps

Ohmic Formation

[0060] Next, as shown in **FIG. 8E**, openings are formed in a SiN film, for example, by ICP dry etching or the like. Each of a source electrode 490 and a drain electrode 410 is formed of a Ti layer and an Al layer in an associated one of the openings, and then heat treatment is performed thereto in an N₂ atmosphere at 650° C.

Hikita-347, [0060]

Gate Formation

[0061] Next, as shown in **FIG. 8F**, part of the SiN film 408 provided on the heavily doped p-type GaN layer 406 is removed, for example, by ICP dry etching or the like. Subsequently, a gate electrode 411 of Pd is formed in an associated one of the openings in the SiN film 408. The

Hikita-347, [0061]

Hikita-347-Beach Renders Obvious Separate Patterns for Gate and Metal Photo Resistant Patterns

- The Petition explains *Hikita-347* forms its gate structure and ohmic contacts in separate steps, rendering obvious applying gate and metal photo resistant patterns at separate steps

Hikita-347 discloses forming a gate electrode 111 (gate contact) over the p-type GaN layer 105, as shown below. *Hikita-347*, [0013], [0034], [0061].

Pet. 56

Hikita-347 in view of *Beach* renders obvious [1g]. Shealy, ¶196.

Hikita-347 discloses depositing a Ti layer and an Al layer (ohmic contact metal) on the n-undoped AlGaIn layer 104 to form a source electrode 109 and a drain electrode 110 (ohmic source and drain contacts). *Hikita-347*, [0034], [0060];

Pet. 60-61

Disputed Issue 3: Separate “Gate Photo Resistant Pattern” and “Metal photo Resistant Pattern”

Issue	EPC’s Argument	Correct Resolution
The combination teaches separate “gate photo resistant pattern” and “metal photo resistant pattern”	<i>Beach</i> teaches a single pattern for forming the gate structure and ohmic contacts.	<i>Beach</i> teaches separate “gate photo resistant pattern” and “metal photo resistant pattern”; <i>Yoshida</i> teaches forming the gate structure and ohmic structure in separate steps

Although not required by the claims, the *Hikita-347-Beach* combination teaches applying separate patterns in separate steps

Hikita-347-Beach-Sheppard Renders Obvious Claim 1

Claim 1	Claim Limitation	
1pre	A method of forming an enhancement mode GaN transistor, the method comprising:	✓
1a	nucleating and growing transition layers on a substrate;	✓
1b	growing an III Nitride EPI layer over the transistor layers;	✓
1c	growing an III Nitride barrier layer over the EPI layer;	✓
1d	growing a GaN layer with acceptor type dopants over the barrier layer;	✓
1e1	depositing a gate contact layer on the doped GaN layer;	✓
1e2	applying a gate photo resistant pattern;	✓
1e3	etching away the gate contact layer outside the gate region;	✓
1e4	etching away the doped GaN layer, except a portion of the doped GaN layer beneath the gate contact;	✓
1e5	removing the gate photo resistant pattern;	✓
1f1	depositing a dielectric layer;	✓
1f2	applying a contact photo resistant pattern;	✓
1f3	etching the dielectric layer to open the drain and source contact area;	✓
1f4	removing the contact photo resistant pattern;	✓
1g1	depositing an Ohmic contact metal;	✓
1g2	applying a metal photo resistant pattern;	✓
1g3	etching the Ohmic contact metal;	✓
1g4	removing the metal photo resistant pattern; and	✓
1g5	performing rapid thermal annealing to form Ohmic drain and source contacts.	✓

Hikita-347-Beach-Sheppard Renders Obvious Claim 4

Claim Limitation	
Same disputed issues as in claim 1	
Epitaxial layers formation	4a nucleating and growing transition layers on a substrate;
	4b growing an InAlGaN EPI layer over the transistor layers;
	4c growing an InAlGaN barrier layer over the InAlGaN EPI layer;
	4d growing an InAlGaN layer with acceptor type dopants over the InAlGaN barrier layer;
Gate formation (alleged novelty)	4e growing a GaN layer with acceptor type dopants over the doped InAlGaN layer
	4f1 growing a gate contact layer on the doped GaN layer;
	4f2 applying a gate photo resistant pattern;
	4f3 etching away the gate contact layer outside the gate region;
	4f4 etching away the doped GaN layer and the doped InAlGaN layer, except the doped GaN layer and the doped InAlGaN layer beneath gate contact;
Dielectric layer formation	4f5 removing the gate photo resistant pattern;
	4g1 depositing a dielectric layer;
	4g2 applying a contact photo resistant pattern;
	4g3 etching the dielectric layer to open the drain and source contact area;
Ohmic formation	4g4 removing the contact photo resistant pattern;
	4h1 depositing an Ohmic contact metal;
	4h2 applying a metal photo resistant pattern;
Disputed Issue #2: motivation to combine Hikita-347 with Beach	4h3 etching the Ohmic contact metal;
	4i1 etching the metal photo resistant pattern; and
4j rapid thermal annealing to form Ohmic drain and source contacts.	

Disputed Issue #1:
motivation to combine
Hikita-347 with Beach

Disputed Issue #3: teaching of
separate gate and metal
photo resistant pattern

EPC argues claim 4 and claim 1 together
in its papers; claim 4 is obvious for the
same reasons

Hikita-347-Beach-Sheppard Renders Obvious Claim 4

Claim 4	Claim Limitation	
4pre	A method of forming an enhancement mode GaN transistor, the method comprising:	✓
4a	nucleating and growing transition layers on a substrate;	✓
4b	growing an InAlGaN EPI layer over the transistor layers;	✓
4c	growing an InAlGaN barrier layer over the InAlGaN EPI layer;	✓
4d	growing an InAlGaN layer with acceptor type dopants over the InAlGaN barrier layer;	✓
4e	growing a GaN layer with acceptor type dopants over the doped InAlGaN layer	✓
4f1	depositing a gate contact layer on the doped GaN layer;	✓
4f2	applying a gate photo resistant pattern;	✓
4f3	etching away the gate contact layer outside the gate region;	✓
4f4	etching away the doped GaN layer and the doped InAlGaN layer, except for portions of the doped GaN layer and the doped InAlGaN layer beneath gate contact;	✓
4f5	removing the gate photo resistant pattern;	✓
4g1	depositing a dielectric layer;	✓
4g2	applying a contact photo resistant pattern;	✓
4g3	etching the dielectric layer to open the drain and source contact area;	✓
4g4	removing the contact photo resistant pattern;	✓
4h1	depositing an Ohmic contact metal;	✓
4h2	applying a metal photo resistant pattern;	✓
4h3	etching the Ohmic contact metal;	✓
4h4	removing the metal photo resistant pattern; and	✓
4h5	performing rapid thermal annealing to form Ohmic drain and source contacts.	✓

Ground 3: *Hikita-023, Beach, and Sheppard*

Claim 5 of the '508 Patent

**Epitaxial
layers
formation**

**Gate
formation
(alleged
novelty)**

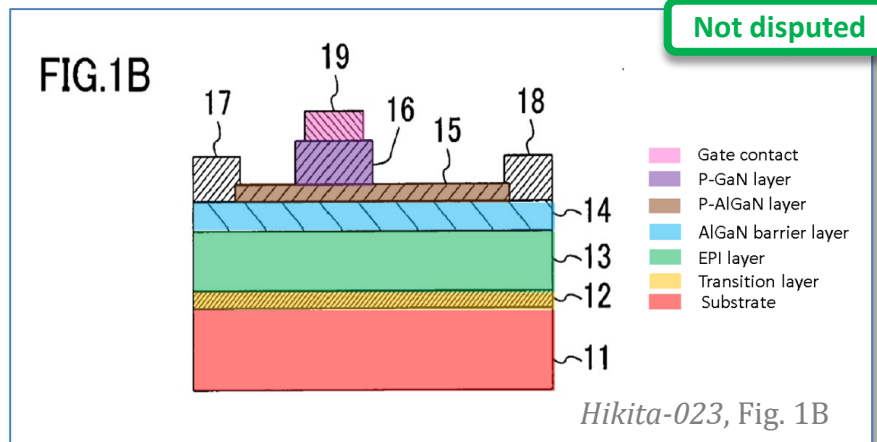
**Dielectric
layer
formation**

**Ohmic
formation**

Claim 5	Claim Limitation	
5pre	A method of forming an enhancement mode GaN transistor, the method comprising:	
5a	nucleating and growing transition layers on a substrate;	
5b	growing an InAlGaN EPI layer over the transistor layers;	
5c	growing an AlGaN barrier layer over the InAlGaN EPI layer;	
5d	growing an AlGaN layer with acceptor type dopants over the AlGaN barrier layer;	
5e	growing a GaN layer with acceptor type dopants over the doped AlGaN layer;	
5f1	depositing a gate contact layer on the doped GaN layer;	No dispute that the prior art discloses each of the claim limitations
5f2	applying a gate photo resistant pattern;	
5f3	etching away the gate contact layer outside the gate region;	
5f4	etching away the doped GaN layer, except for portions of the doped GaN layer and the doped AlGaN layer beneath gate contact;	
5f5	removing the gate photo resistant pattern;	
5g1	applying another photo resistant pattern;	
5g2	etching the doped AlGaN layer such that the doped AlGaN extends outside the gate region towards the drain:	
5g3	5i1	depositing an Ohmic contact metal;
5h1	5i2	applying a fourth photo resistant pattern;
5h2	5i3	etching the Ohmic contact metal
5h3	5i4	removing the fourth photo resistant pattern; and
5h4	5i5	performing rapid thermal annealing to form Ohmic drain and source contacts.
	removing the contact photo resistant pattern;	

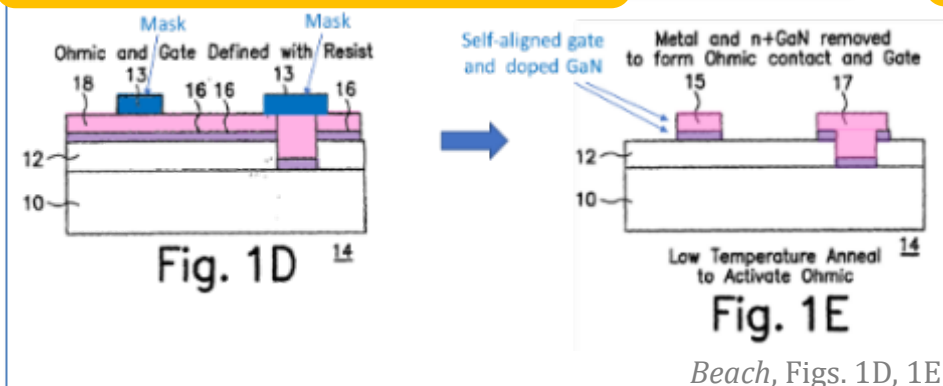
Overview of Prior Art

Hikita-023 teaches the claimed process except a process for self-aligned gate and ohmic contacts, using a mask to open source and drain contact area, and growing multiple transition layers



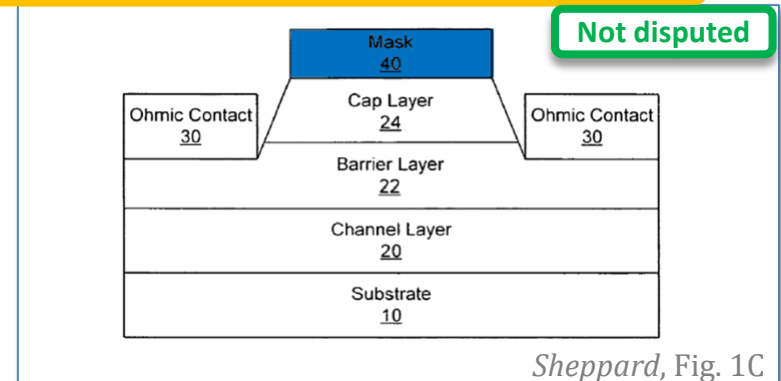
Beach teaches a process for self-aligned gate and ohmic contacts

Not disputed



Sheppard teaches using a mask to open source and drain contact area and growing multiple transition layers

Not disputed



Hikita-023-Beach-Sheppard Renders Obvious Claim 5

EPC makes similar incorrect arguments in the *Hikita-023* ground as the *Hikita-347* ground

Claim Line

For similar reasons as in *Hikita-347*, EPC's arguments fail

Epitaxial layers formation

Disputed Issue #1: motivation to combine *Hikita-023* with *Beach*

Gate formation (alleged novelty)

Dielectric layer formation

Ohmic formation

Disputed Issue #2: motivation to combine *Hikita-023* with *Beach*

Disputed Issue #3: teaching of separate gate and fourth photo resistant pattern

5a	nucleating and growing transition layers on a substrate;		
5b	growing an InAlGaN EPI layer over the transistor layers;		Not disputed
5c	growing an AlGaN barrier layer over the InAlGaN EPI layer;		
5d	growing an AlGaN layer with acceptor type dopants over the AlGaN barrier layer;		
5e	growing a GaN layer with acceptor type dopants over the doped AlGaN layer		
5f1	depositing a gate contact layer on the doped GaN layer;		
5f2	applying a gate photo resistant pattern;		
5f3	etching away the gate contact layer outside the gate region;		
5f4	etching away the doped GaN layer, except for portions of the doped GaN layer and the doped AlGaN layer beneath gate contact;		
5f5	removing the gate photo resistant pattern;		
5g1	applying another photo resistant pattern;		
5g2	etching the doped AlGaN layer such that the doped AlGaN extends outside the gate region towards the drain;		Not disputed
5g3	depositing an Ohmic contact metal;	5i1	depositing an Ohmic contact metal;
5h1	applying a fourth photo resistant pattern;	5i2	applying a fourth photo resistant pattern;
5h2	depositing a fourth Ohmic contact metal	5i3	depositing a fourth Ohmic contact metal
5h3	removing the fourth photo resistant pattern; and		
5h4	rapid thermal annealing to form Ohmic drain and source contacts.		

Hikita-023-Beach-Sheppard Renders Obvious Claim 5

Claim 5	Claim Limitation	
5pre	A method of forming an enhancement mode GaN transistor, the method comprising:	✓
5a	nucleating and growing transition layers on a substrate;	✓
5b	growing an InAlGa _N EPI layer over the transistor layers;	✓
5c	growing an AlGa _N barrier layer over the InAlGa _N EPI layer;	✓
5d	growing an AlGa _N layer with acceptor type dopants over the AlGa _N barrier layer;	✓
5e	growing a Ga _N layer with acceptor type dopants over the doped AlGa _N layer	✓
5f1	depositing a gate contact layer on the doped Ga _N layer;	✓
5f2	applying a gate photo resistant pattern;	✓
5f3	etching away the gate contact layer outside the gate region;	✓
5f4	etching away the doped Ga _N layer, except for portions of the doped Ga _N layer and the doped AlGa _N layer beneath gate contact;	✓
5f5	removing the gate photo resistant pattern;	✓
5g1	applying another photo resistant pattern;	✓
5i1	depositing an Ohmic contact metal;	✓
5i2	applying a fourth photo resistant pattern;	✓
5i3	etching the Ohmic contact metal	✓
5i4	removing the fourth photo resistant pattern; and	✓
5i5	performing rapid thermal annealing to form Ohmic drain and source contacts.	✓
5h3	etching the dielectric layer to open the drain and source contact area;	✓
5h4	removing the contact photo resistant pattern;	✓

Conclusion on Petition

Motivation to Combine for Gate formation	Motivation to Combine for Ohmic formation	Separate “gate photo resistant pattern” and “metal photo resistant pattern”
Yes	Yes	Taught by combination
(1) The gate process need not be performed first; (2) A POSITA would have been motivated to combine <i>Yoshida/Hikita-347/Hikita-023</i> with <i>Beach’s</i> gate formation process	A POSITA would have been motivated to combine <i>Yoshida/ Hikita-347/Hikita-023</i> with <i>Beach’s</i> ohmic formation process	The combination teaches separate “gate photo resistant pattern” and “metal photo resistant pattern”

All claims are obvious

Expert Credential

The Board Should Give Dr. Schubert's Declaration Little Weight

- Dr. Schubert has no practical experience with GaN transistors
 - No personal experience of building a GaN transistor

- First demonstration of crystallographic etching of GaN (with graduate student D. A. Stocker, 1998). The discovery, crystallographic etching, can be implemented by wet chemical etching, including photo-enhanced electrochemical (PEC) wet etching. The discovery is widely used in the LED industry to strongly enhance light extraction from LED chips and is found in LED light bulbs.
- Experimental demonstration of a ten-fold enhancement of p-type doping activation in $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ doped superlattices as compared to bulk GaN and $\text{Al}_x\text{Ga}_{1-x}\text{N}$ (with graduate students D. A. Stocker and I. D. Goepfert, 1999)
- Invention and demonstration of the photon-recycling semiconductor light-emitting diode (PRS-LED) which emits *white* light and many other colors with very high luminous performance of $> 300 \text{ lm/W}$ (with graduate students X. Guo and J. W. Graff, 1999). Invention of the monolithically integrated GaInN/GaN PRS-LED (with graduate students X. Guo and J. W. Graff, 2000)
- Invention and demonstration of polarization-enhanced ohmic contacts in p-type and n-type GaN (with graduate students Y.-L. Li and J. W. Graff 2000)
- Developed efficiency-droop reducing GaInN / GaInN and GaInN / AlGaInN LED active regions grown by MOCVD and ALE that were demonstrated to reduce the efficiency droop by as much as 40% (with Jong Kyu Kim, Martin F. Schubert, Di Zhu, Jiuru Xu, Mary Crawford, and Dan Koleske, starting in 2007)

Ex. 2001, Appx. A., 2-3

**No experience on
GaN Transistors**

- Dr. Schubert does not meet EPC's definition of a POSITA
 - Lacking “three years of professional work experience in the epitaxial growth” of semiconductor devices.

The Board Should Give Dr. Shealy's Declaration More Weight

- Dr. Shealy is a pioneer scientist in the field of GaN transistors
 - Built the first operational GaN HEMT on silicon substrate
 - First to build an insulating gate device in GaN
 - Developed the Cornell nucleation process for GaN materials around the world
 - Built the benchmark high power microwave transistors

Now before I make the drawings, I wanted to comment on the dielectric first approach. The dielectric first approach is the approach that was taken in my lab from 1995 to 2005 when we built HEMT devices at Cornell. We built the first operational HEMT on silicon which is kind of the backbone of this whole power converter industry that's emerged from that. We were the first to do it.

We were the first to build an insulating gate device on a HEMT structure in gallium nitride.

We developed what's called the Cornell nucleation process, there's two nucleation processes used for gallium nitride materials around the world; one came from Cornell, my lab; one came from Nakamura who is a little bit better known than I am. He came from Nichia in Japan.

Shealy Tr. (Ex. 2002), 87:15-88:7

Reply, 33-34