



Patent Owner's Demonstratives

Innoscience (Zhuhai) Technology Co., Ltd. and
Innoscience America, Inc.
v.

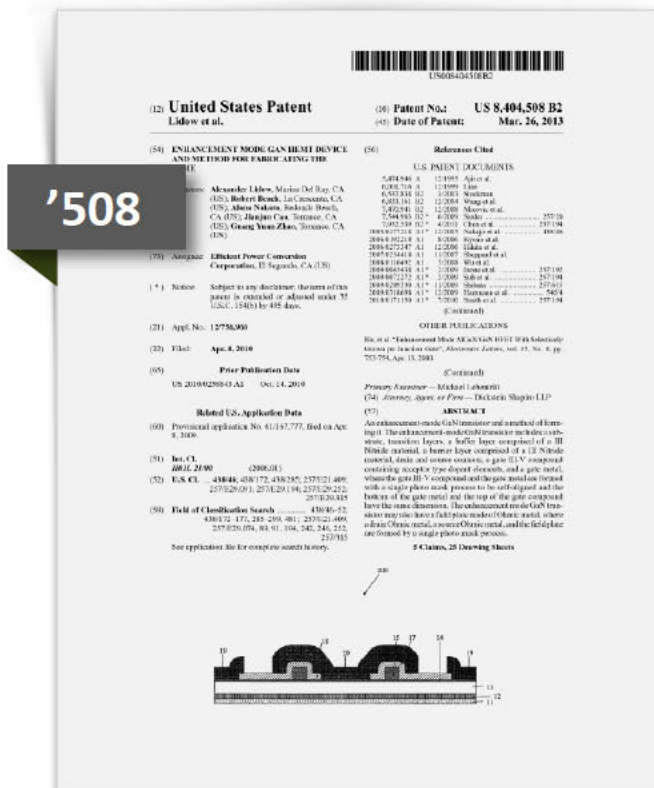
Efficient Power Conversion Corporation

Case: IPR2023-01383

Patent No.: 8,404,508

December 18, 2024

The '508 Patent

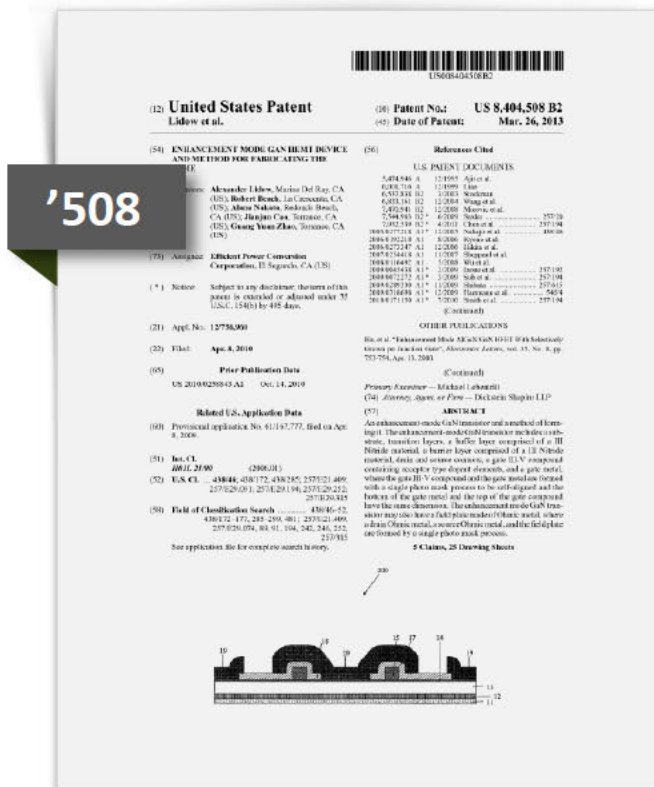


- The '508 Patent Technology
- Claim Construction
- Ground 1 (Claims 1-3): Yoshida, Beach, Sheppard
- Ground 2 (Claims 1-4): Hikita347, Beach, Sheppard
- Ground 3 (Claims 1-5): Hikita023, Beach, Sheppard

(54) **ENHANCEMENT MODE GAN HEMT DEVICE AND METHOD FOR FABRICATING THE SAME**

The '508 Patent's Technology

The '508 Patent



- Method for Fabricating an Enhancement Mode HEMT Device
- Claimed steps include epitaxial layer deposition and structure fabrication
- Fabrication steps at issue:
 - Gate formation
 - Dielectric formation
 - Ohmic contact (source & drain contacts) formation

(54) **ENHANCEMENT MODE GAN HEMT DEVICE AND METHOD FOR FABRICATING THE SAME**

Present Invention: One Process – Two Features

US 8,404,508 B2

The present invention is an enhancement mode GaN HEMT device with a gate metal material and a doped GaN or AlGaIn material that are self-aligned, and a method for making such a device. The materials are patterned and etched using a single photo mask, which reduces manufacturing costs. Furthermore, a field plate at source potential is patterned and etched together with drain and source ohmic contact metal. The field plate reduces the electric field at the gate corner of this enhancement mode GaN HEMT device.

Referring to FIGS. 2 and 3A-3E, a first embodiment is now described for forming an enhancement mode GaN HEMT device with a self-aligned gate, wherein like reference numerals are used consistently for like features throughout the drawings. FIG. 2 illustrates an enhancement mode GaN HEMT device 200 formed by the method described below with respect to FIGS. 3A-3E, which has a gate metal 17 and a p-type GaN material 15 that are self-aligned. Device 200 includes a silicon substrate 11, transition layers 12, un-doped GaN buffer material 13, un-doped AlGaIn barrier material 14, p-type GaN gate layer 15, gate metal 17, dielectric material 18, drain ohmic contact 19 and source ohmic contact 20. The source metal 20 also serves as a field plate that extends over the gate and toward the drain contact. Layers 13, 14, and 15 are made of a III-Nitride material. A III-Nitride material can be composed of $In_xAl_{1-x}Ga_{1-y}N_z$, where $x \leq 1$, $y \leq 1$, and $z \leq 1$.

FIG. 3A illustrates the EPI structure of GaN HEMT device 200a, including, from bottom up, silicon substrate 11, transition layers 12, un-doped GaN buffer material 13, un-doped AlGaIn barrier layer 14, and p-type GaN gate layer 15. The un-doped GaN buffer material 13 preferably has a thickness of about 0.5 to about 5 μm . The un-doped AlGaIn barrier layer 14 preferably has a thickness of about 50 Å to about 300 Å. The un-doped AlGaIn barrier layer 14 includes Al from about 12 to 100 percent of the metallic content of the AlGaIn material. The p-type GaN gate layer 15 may have a thickness of about 100 Å to about 2000 Å. Additionally, the p-type GaN gate layer may have a doping concentration between about 10^{18} to about 10^{20} atoms per cm^3 .

As shown in FIG. 3B, a gate metal 17 is deposited on the EPI structure shown in FIG. 3A. The gate metal 17, alternatively, can be grown at the end of EPI growth. Gate metal 17 can be made of a refractory metal or its compound, e.g., tungsten (W), tantalum nitride (Ta₂N₅), titanium nitride (TiN), palladium (Pd), tungsten (W), tungsten silicide (WSi₂).

Subsequently, a single photo mask is used to pattern and etch the gate metal 17 and the p-type GaN gate layer 15, resulting in the structure shown in FIG. 3C. The gate metal 17 and the p-type GaN gate layer 15 are etched by any known technique, e.g., plasma etching, followed by a photoresist strip. The p-type GaN gate layer 15 can be under-etched, leaving about 0 to about 10 nm of the gate material outside of the gate region. The gate layer 15 can also be over-etched, removing about 0 to about 1 nm of the barrier layer 14 outside of the gate region. In the over-etching case, the barrier layer 14 is about 0 to about 3 nm thinner outside of the gate region than that in the gate region.

Referring now to FIG. 3D, a dielectric material 18, such as silicon nitride (Si₃N₄), is deposited. After deposition of the dielectric material 18, a contact photo mask is used to pattern and etch the dielectric material 18, followed by a photoresist strip, resulting in the structure shown in FIG. 3D.

Referring now to FIG. 3E, ohmic contact metal is deposited. Ohmic contact metal can be made of titanium (Ti), aluminum (Al), and a capping metal stack. After ohmic metal deposition, a metal mask is used to pattern and etch the ohmic contact metal, resulting in the drain ohmic contact 19 and the source ohmic contact 20, as shown in FIG. 3E. Rapid thermal

3

The present invention is an enhancement mode GaN HEMT device with a gate metal material and a doped GaN or AlGaIn material that are self-aligned, and a method for making such a device. The materials are patterned and etched using a single photo mask, which reduces manufacturing costs. Furthermore, a field plate at source potential is patterned and etched together with drain and source ohmic contact metal. The field plate reduces the electric field at the gate corner of this enhancement mode GaN HEMT device.

(Paper 17 at 17-21; Ex. 1001 at 3:1-9)

Identified “present invention”:

- Method of forming self-aligned gate structure; and
- Patterning and etching field plate at source potential together with ohmic contacts

'508 Patent - Independent Claims

1. A method of forming an enhancement mode GaN transistor, the method comprising:
nucleating and growing transition layers on a substrate;
growing an III Nitride EPI layer over the transistor layers;
growing an III Nitride barrier layer over the EPI layer;
growing a GaN layer with acceptor type dopants over the barrier layer;
depositing a gate contact layer on the doped GaN layer;
applying a gate photo resistant pattern;
etching away the gate contact layer outside the gate region;
etching away the doped GaN layer, except a portion of the doped GaN layer beneath the gate contact;
removing the gate photo resistant pattern;
depositing a dielectric layer;
applying a contact photo resistant pattern;
etching the dielectric layer to open the drain and source contact area;
removing the contact photo resistant pattern;
depositing an Ohmic contact metal;
applying a metal photo resistant pattern;
etching the Ohmic contact metal;
removing the metal photo resistant pattern; and
performing rapid thermal annealing to form Ohmic drain and source contacts.

4. A method of forming an enhancement mode GaN transistor, the method comprising:
nucleating and growing transition layers on a substrate;
growing an InAlGaEPI layer over the transistor layers;
growing an InAlGaEPI barrier layer over the InAlGaEPI layer;
growing an InAlGaEPI layer with acceptor type dopants over the InAlGaEPI barrier layer;
growing a GaN layer with acceptor type dopants over the doped InAlGaEPI layer;
depositing a gate contact layer on the doped GaN layer;
applying a gate photo resistant pattern;
etching away the gate contact layer outside the gate region;
etching away the doped GaN layer and the doped InAlGaEPI layer, except for portions of the doped GaN layer and the doped InAlGaEPI layer beneath gate contact;
removing the gate photo resistant pattern;
depositing a dielectric layer;
applying a contact photo resistant pattern;
etching the dielectric layer to open the drain and source contact area;
removing the contact photo resistant pattern;
depositing an Ohmic contact metal;
applying a metal photo resistant pattern;
etching the Ohmic contact metal;
removing the metal photo resistant pattern; and
performing rapid thermal annealing to form Ohmic drain and source contacts.

5. A method of forming an enhancement mode GaN transistor, the method comprising:
nucleating and growing transition layers on a substrate;
growing an InAlGaEPI layer over the transistor layers;
growing an AlGaEPI barrier layer over the InAlGaEPI layer;
growing an AlGaEPI layer with acceptor type dopants over the AlGaEPI barrier layer;
growing a GaN layer with acceptor type dopants over the doped AlGaEPI layer;
depositing a gate contact layer on the doped GaN layer;
applying a gate photo resistant pattern;
etching away the gate contact layer outside the gate region;
etching away the doped GaN layer, except for portions of the doped GaN layer and the doped AlGaEPI layer beneath gate contact;
removing the gate photo resistant pattern;
applying another photo resistant pattern;
etching the doped AlGaEPI layer such that the doped AlGaEPI extends outside the gate region towards the drain;
removing the photo resistant pattern;
depositing a dielectric layer;
applying a contact photo resistant pattern;
etching the dielectric layer to open the drain and source contact area;
removing the contact photo resistant pattern;
depositing an Ohmic contact metal;
applying a fourth photo resistant pattern;
etching the Ohmic contact metal;
removing the fourth photo resistant pattern; and
performing rapid thermal annealing to form Ohmic drain and source contacts.

Claim Steps Terminology – Representative Claim 1

1. A method of forming an enhancement mode GaN transistor, the method comprising:

nucleating and growing transition layers on a substrate;
growing an III Nitride EPI layer over the transistor layers;
growing an III Nitride barrier layer over the EPI layer;
growing a GaN layer with acceptor type dopants over the barrier layer;

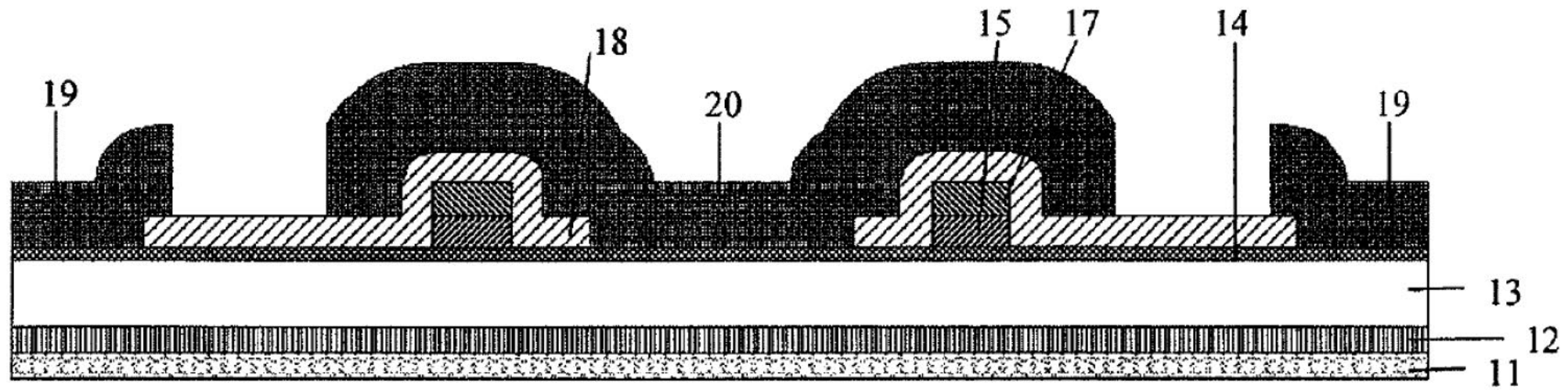
depositing a gate contact layer on the doped GaN layer;
applying a gate photo resistant pattern;
etching away the gate contact layer outside the gate region;
etching away the doped GaN layer, except a portion of the doped GaN layer beneath the gate contact;
removing the gate photo resistant pattern;

depositing a dielectric layer;
applying a contact photo resistant pattern;
etching the dielectric layer to open the drain and source contact area;

removing the contact photo resistant pattern;
depositing an Ohmic contact metal;
applying a metal photo resistant pattern;
etching the Ohmic contact metal;
removing the metal photo resistant pattern; and
performing rapid thermal annealing to form Ohmic drain and source contacts.

- Gate formation – “G”
- Dielectric Layer Formation – “D”
- Ohmic Contact Formation – “O”

Enhancement Mode GaN HEMT



(Ex. 1001 at FIG. 2)

Self-Aligned Gate Formation

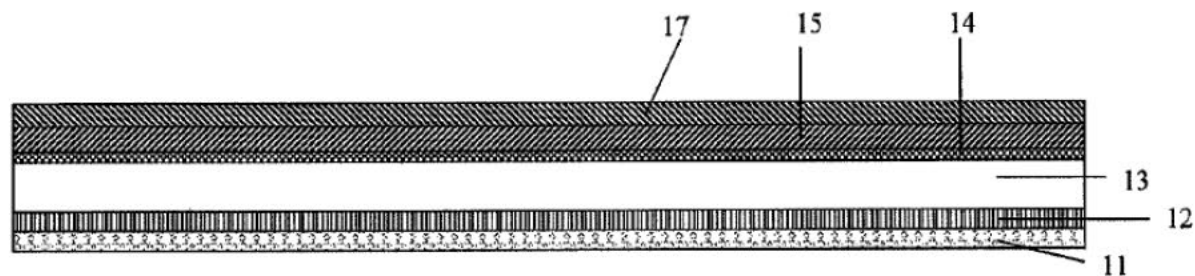


FIG. 3B

(Ex. 1001)

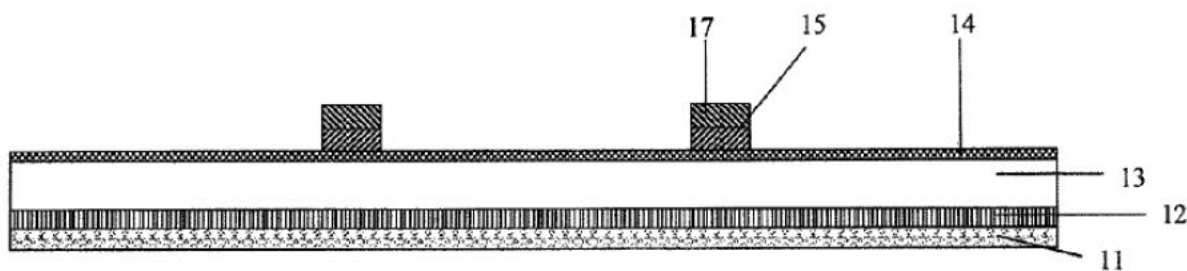


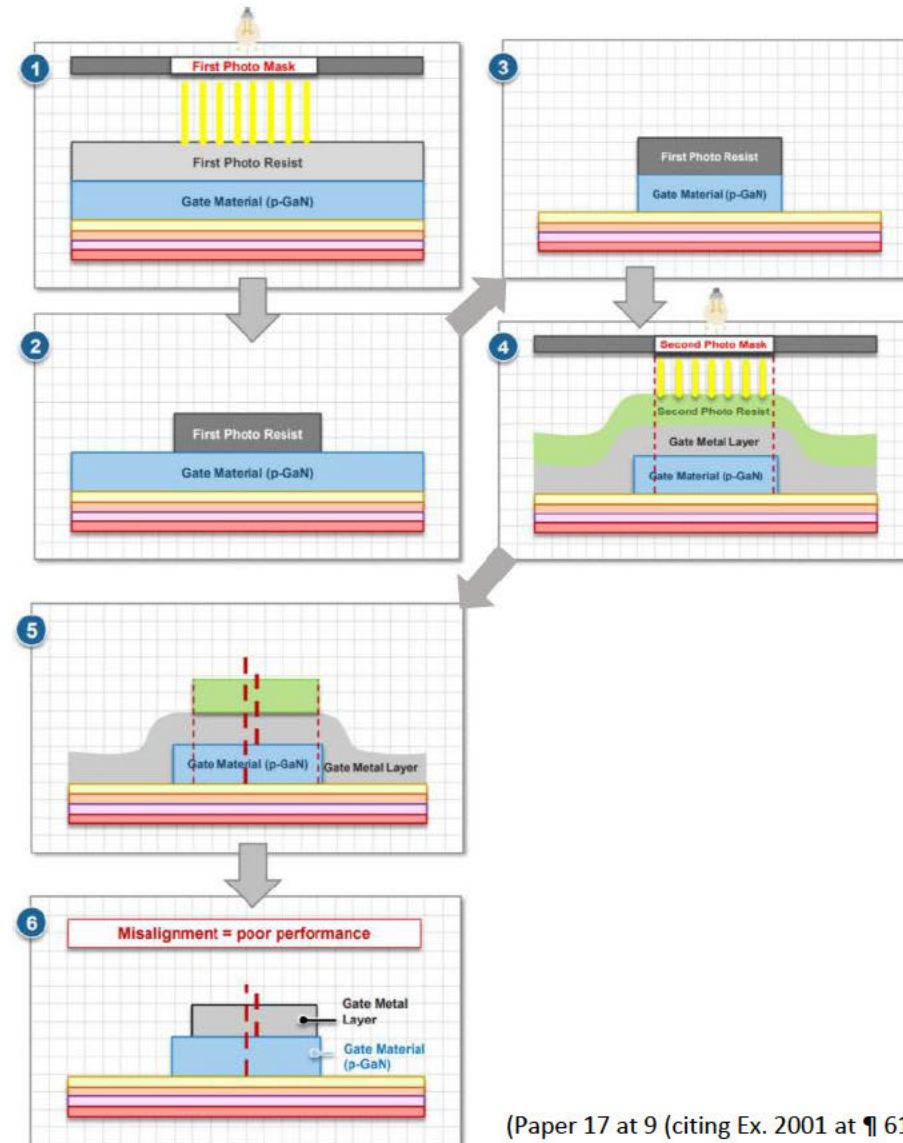
FIG. 3C

(Ex. 1001)

depositing a gate contact layer on the doped GaN layer;
applying a gate photo resistant pattern;
etching away the gate contact layer outside the gate region;
etching away the doped GaN layer, except a portion of the
doped GaN layer beneath the gate contact;
removing the gate photo resistant pattern;

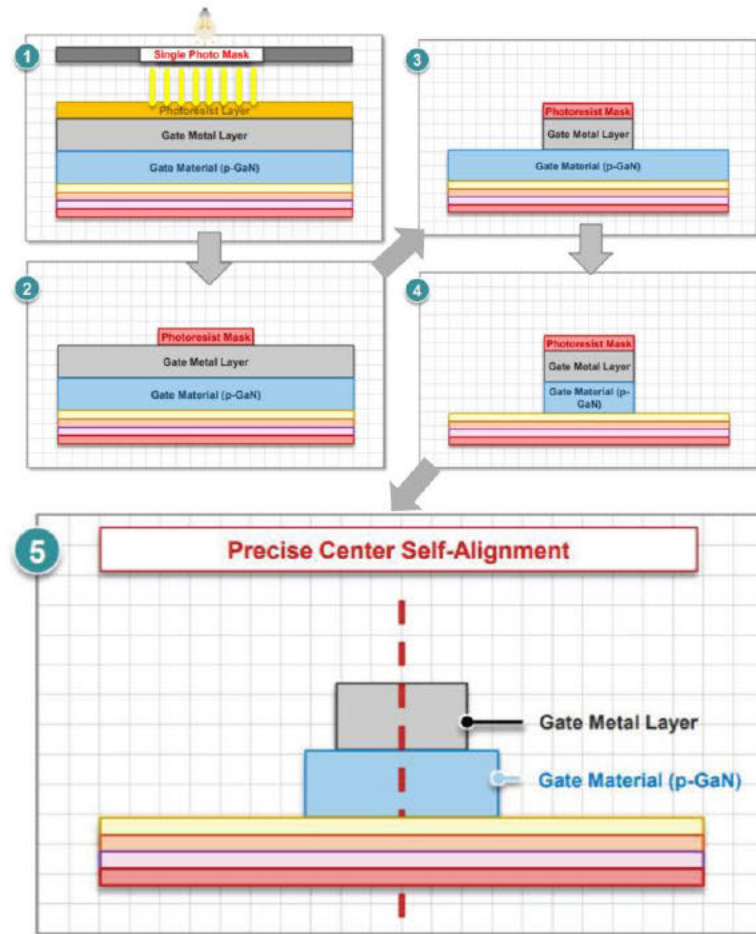
(Ex. 1001 at Claim 1)

Prior Art - Misalignment



(Paper 17 at 9 (citing Ex. 2001 at ¶ 61))

'508 Patent – Self-Aligned Gate Process – Precise Center Self-Alignment



(Paper 17 at 10 (citing Ex. 2001 at ¶ 62))

depositing a gate contact layer on the doped GaN layer;
applying a gate photo resistant pattern;
etching away the gate contact layer outside the gate region;
etching away the doped GaN layer, except a portion of the
doped GaN layer beneath the gate contact;
removing the gate photo resistant pattern;

(Ex. 1001 at Claim 1)

Dielectric Formation

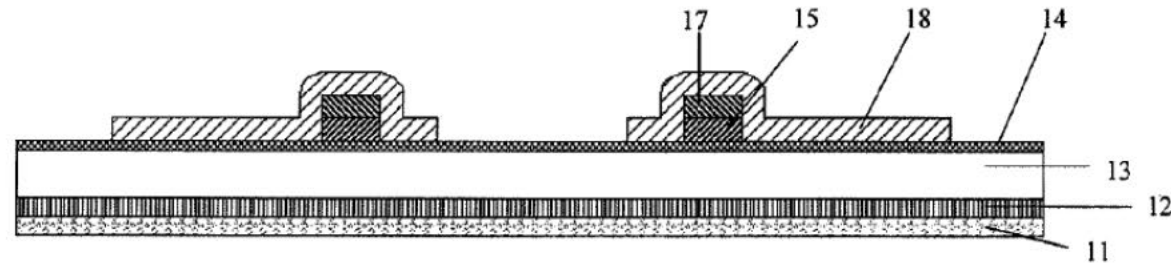


FIG. 3D

(Ex. 1001)

Ohmic Contact Formation – Field Plate at Source Potential

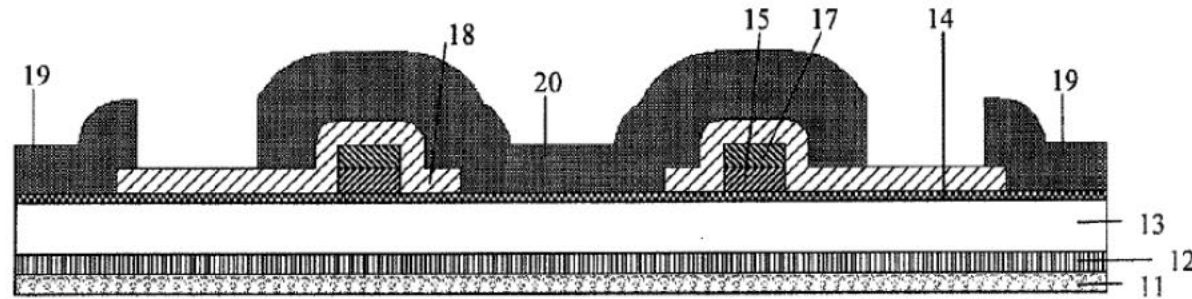


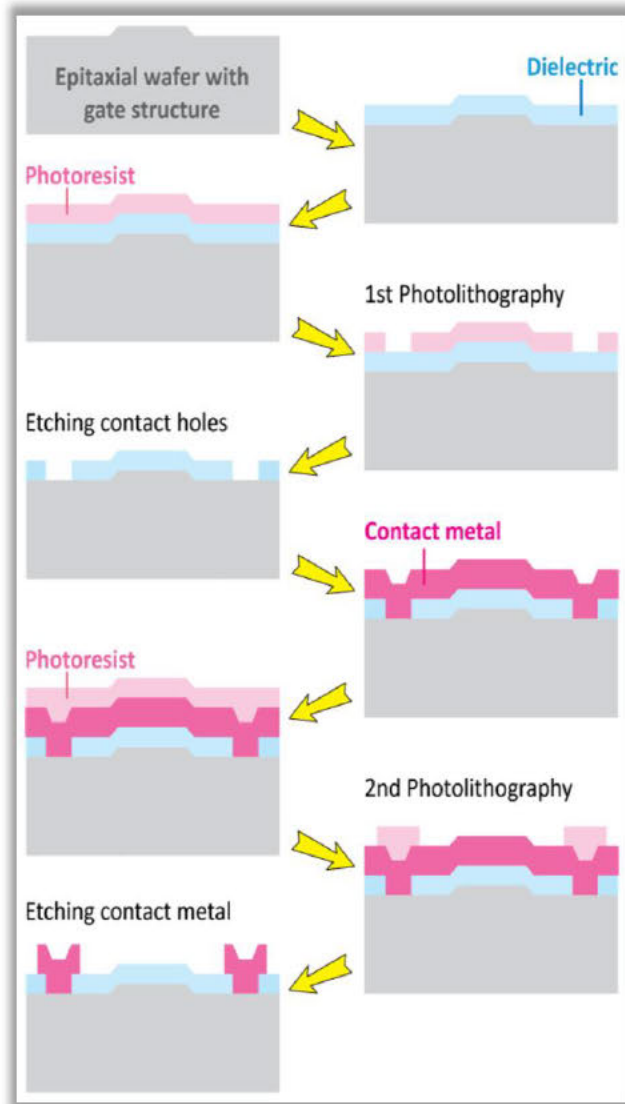
FIG. 3E

(Ex. 1001)

depositing an Ohmic contact metal;
applying a metal photo resistant pattern;
etching the Ohmic contact metal;
removing the metal photo resistant pattern; and
performing rapid thermal annealing to form Ohmic drain
and source contacts.

(Ex. 1001 at Claim 1)

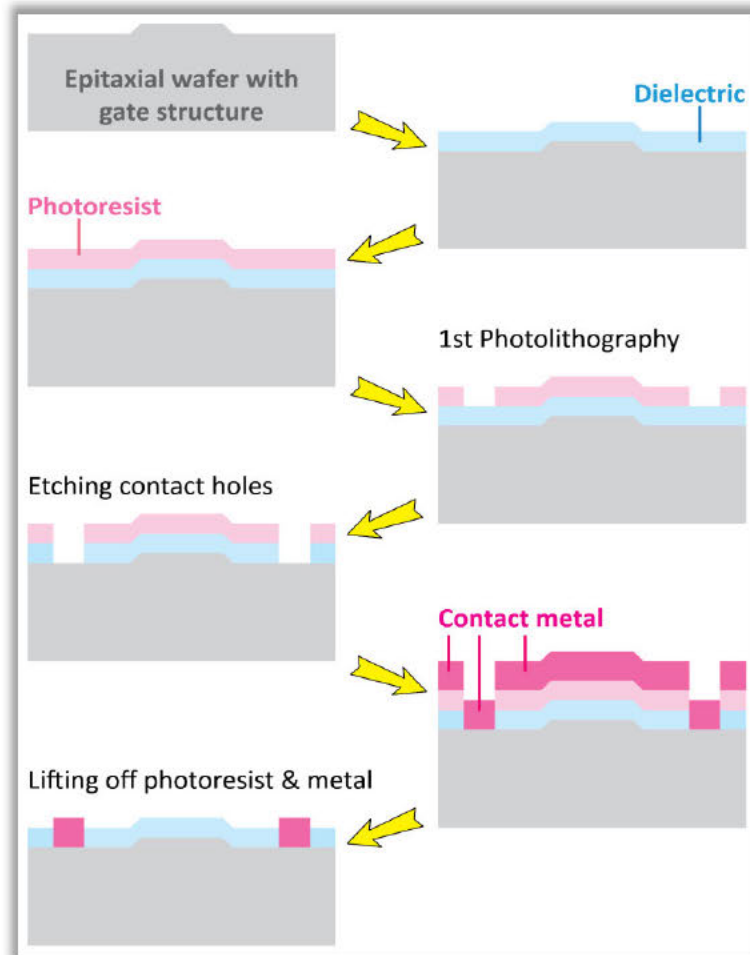
Two-Etch Process: Simultaneous Ohmic Contact and Field Plate Formation



(Paper 17 at 12 (citing Ex. 2001 at ¶¶ 71-72))

- Process:
 - Deposit photoresist material on dielectric
 - 1st Photolithography process to open source and drain contact locations (create holes in dielectric material)
 - Remove photoresist
 - Deposit ohmic contact metal
 - 2nd Photolithography process to pattern source, drain, field plate
- Results:
 - No vertical alignment of contacts and dielectric material due to natural misalignment
 - Option to simultaneously form field plate over gate structure
 - Multiple photolithography processes

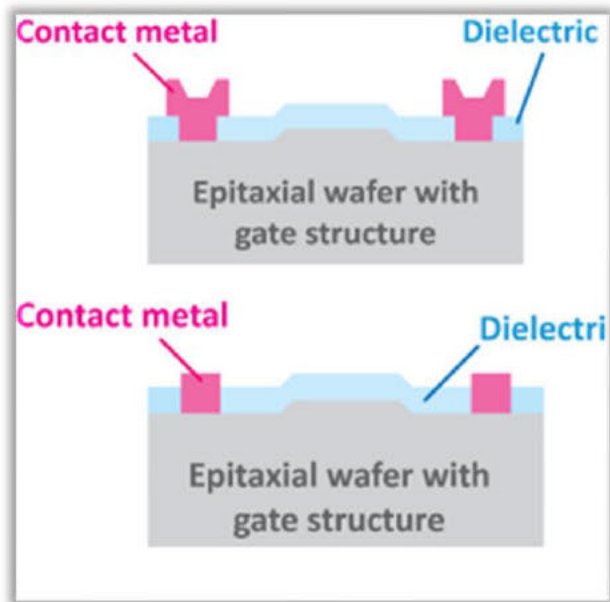
One-Etch Ohmic Contact Process (Not Covered) – e.g., Lift Off



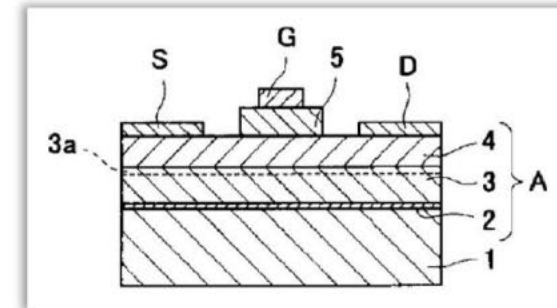
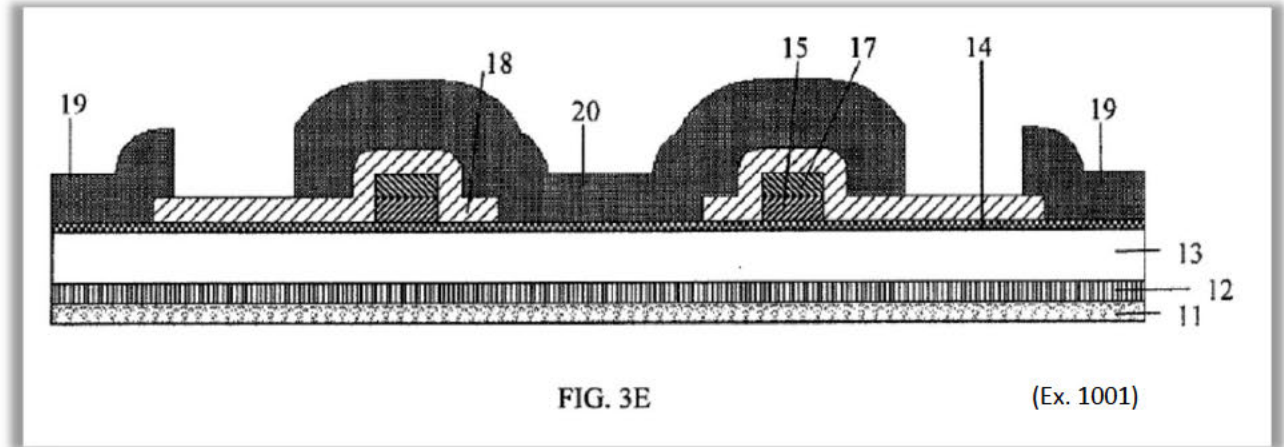
(Paper 17 at 15 (citing Ex. 2001 at ¶¶ 71-72))

- **Process:**
 - Deposit photoresist material on dielectric
 - 1st Photolithography: Patterning and etching process to open source and drain contact locations (create holes in dielectric)
 - Deposit ohmic contact metal
 - Lift-off: remove photoresist and contact metal above photoresist
- **Results:**
 - Vertical alignment of contacts and dielectric material
 - No option to simultaneously form field plate over gate structure at source potential
 - Single photolithography process to pattern ohmic contacts

One Etch v. Two Etch Process Results: Differences



(Paper 17 at 45 (citing Ex. 2001 at ¶ 160))



(Paper 17 at 45; Ex. 1004)

Claim Construction

Sequence of Fabrication Process Steps

Claim 1

1. A method of forming an enhancement mode GaN transistor, the method comprising:

nucleating and growing transition layers on a substrate;
growing an III Nitride EPI layer over the transistor layers;
growing an III Nitride barrier layer over the EPI layer;
growing a GaN layer with acceptor type dopants over the barrier layer;

[1e] depositing a gate contact layer on the doped GaN layer;
applying a gate photo resistant pattern;
etching away the gate contact layer outside the gate region;
etching away the doped GaN layer, except a portion of the doped GaN layer beneath the gate contact;
removing the gate photo resistant pattern;

[1f] depositing a dielectric layer;
applying a contact photo resistant pattern;
etching the dielectric layer to open the drain and source contact area;
removing the contact photo resistant pattern;

[1g] depositing an Ohmic contact metal;
applying a metal photo resistant pattern;
etching the Ohmic contact metal;
removing the metal photo resistant pattern; and
performing rapid thermal annealing to form Ohmic drain and source contacts.

Claim Construction Positions

Patent Owner	Petitioner	Board
<u>Gate “G” first:</u> Gate structure formation before ohmic contact formation [1e] (G), [1f] (D) → 1[g] (O) (Paper 17 at 17-18; Paper 20 at 2-3)	No needed construction (Paper 1 at 10) No order for gate structure steps [1e] compared to ohmic contact steps [1g] (Paper 18 at 1)	“the claims require that the dielectric layer steps of [1f] must occur before the ohmic contact steps of [1g]” (Paper 11 at 12)

“Present Invention”

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The **present invention** is an enhancement mode GaN HEMT device with a gate metal material and a doped GaN or AlGaN material that are self-aligned, and a method for making such a device. The materials are patterned and etched using a single photo mask, which reduces manufacturing costs. Furthermore, a field plate at source potential is patterned and etched together with drain and source ohmic contact metal. The field plate reduces the electric field at the gate corner of this enhancement mode GaN HEMT device.

(Ex. 1001 at 3:1-9; Paper 17 at 18-22)

- Present invention disclosed by inventors in context of '508 patent is a **process** including two features:
 - “a method for making” a self-aligned gate structure “using a single photo mask”
 - a method of forming a field plate *at source potential* “patterned and etched **together with** drain and source ohmic contacts”
- “Furthermore” usage demonstrates field plate formation is also part of the “present invention”
- Inventors identify both structure and process as “present invention”

Claims Recite all Required Steps to Achieve “present invention”

1. A method of forming an enhancement mode GaN transistor, the method comprising:

nucleating and growing transition layers on a substrate;
growing an III Nitride EPI layer over the transistor layers;
growing an III Nitride barrier layer over the EPI layer;
growing a GaN layer with acceptor type dopants over the barrier layer;
depositing a gate contact layer on the doped GaN layer;
applying a gate photo resistant pattern;

etching away the gate contact layer outside the gate region;
etching away the doped GaN layer, except a portion of the doped GaN layer beneath the gate contact;
removing the gate photo resistant pattern;
depositing a dielectric layer;
applying a contact photo resistant pattern;
etching the dielectric layer to open the drain and source contact area;

removing the contact photo resistant pattern;

depositing an Ohmic contact metal;

applying a metal photo resistant pattern;

etching the Ohmic contact metal;

removing the metal photo resistant pattern; and

performing rapid thermal annealing to form Ohmic drain and source contacts.

[1g]

- All independent claims recite all steps for forming a field plate:
 - [1g]; [4h]; [5i]
 - Patterning ohmic metal forms source contact & field plate
- Process capable of forming a field plate together with ohmic contacts is “present invention”

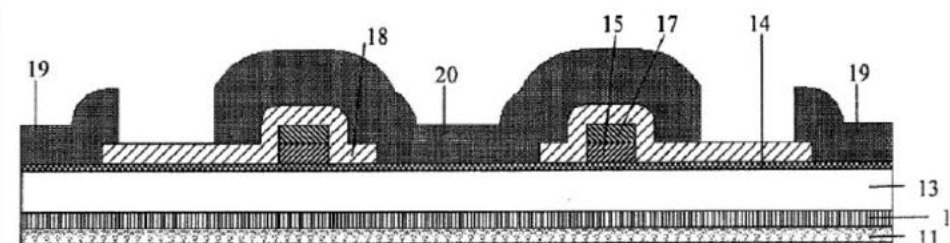


FIG. 3E

(Ex. 1001)

Specification Supports Simultaneous Field Plate Formation is “present invention”

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The **present invention** is an enhancement mode GaN HEMT device with a gate metal material and a doped GaN or AlGaN material that are self-aligned, and a method for making such a device. The materials are patterned and etched using a single photo mask, which reduces manufacturing costs. Furthermore, a field plate at source potential is patterned and etched together with drain and source ohmic contact metal. The field plate reduces the electric field at the gate corner of this enhancement mode GaN HEMT device.

(Ex. 1001 at 3:1-9)

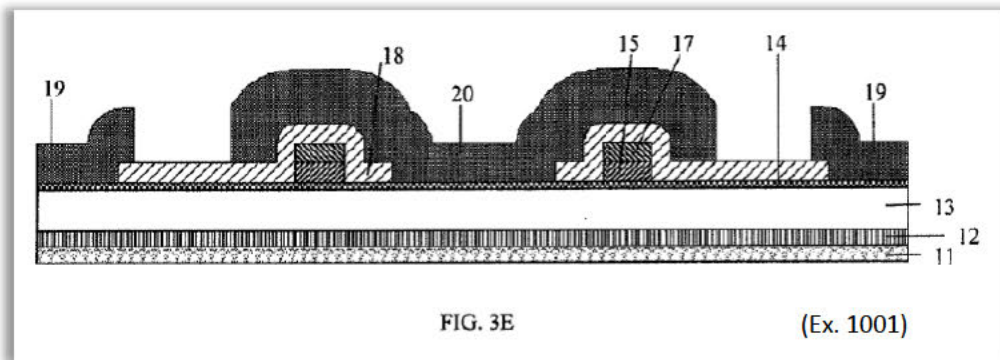


FIG. 3E

(Ex. 1001)

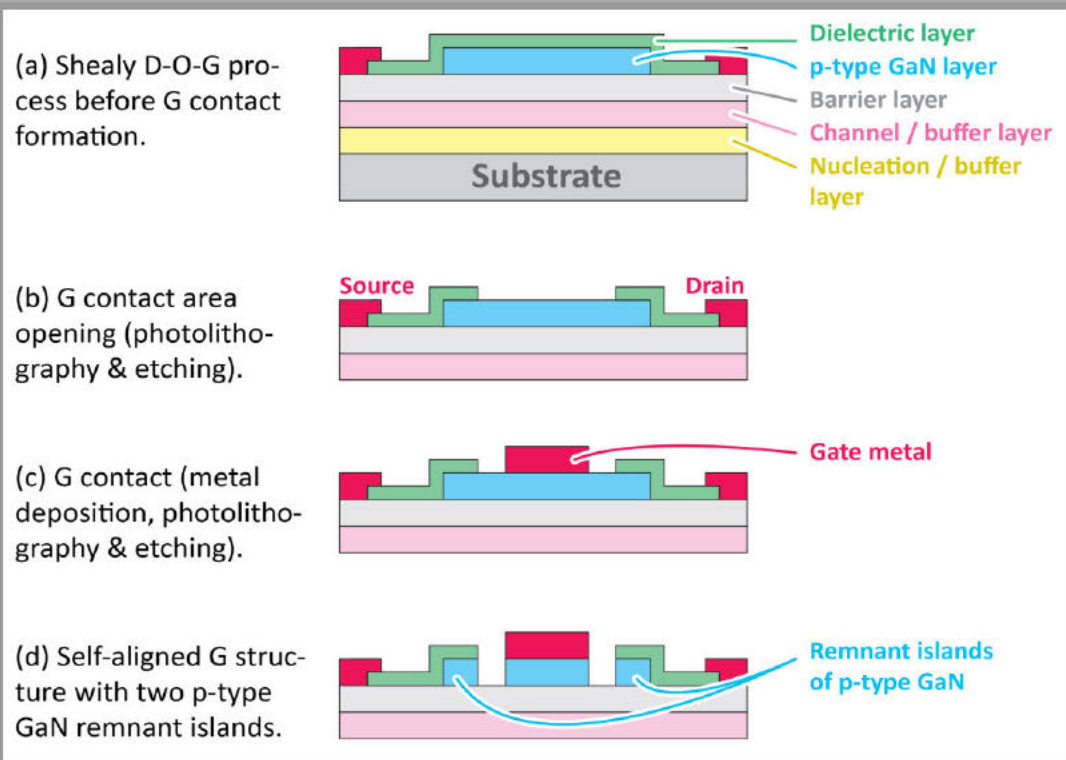
18, drain ohmic contact 19, and source ohmic contact 20. The source metal 20 also serves as a field plate that extends over the gate and toward the drain contact. Layers 13, 14, and 15

(Paper 17 at 19 (citing Ex. 1001 at 3:21-23))

- “Present invention” paragraph uses “Furthermore” to set off both aspects of inventive process
 - Forming field plate “together with” ohmic contacts at source potential (Paper 20 at 3-4)
- Specification consistently describes forming field plate together with contacts, including showing all figures with field plate (Ex. 2002 at 28:24-32:9; Paper 17 at 17-22; Paper 20 at 5)
- Only a “Gate-First” Achieves BOTH “present invention[s]”
- Only process capable of simultaneous “pattern[ing] and etch[ing]” field plate at source potential with source and drain ohmic contact
 - Field plate located **over** gate structure
 - Field plate included in all embodiments
 - Field plate cannot be deposited over gate structure without presence of formed gate structure (Paper 17 at 19 (citing Ex. 2001 ¶¶ 58, 74-75, 83))

Non-G-D-O Processes Cannot Achieve “Present Invention” and Align with Claims

Dr. Shealy's First **D-O-G** Process



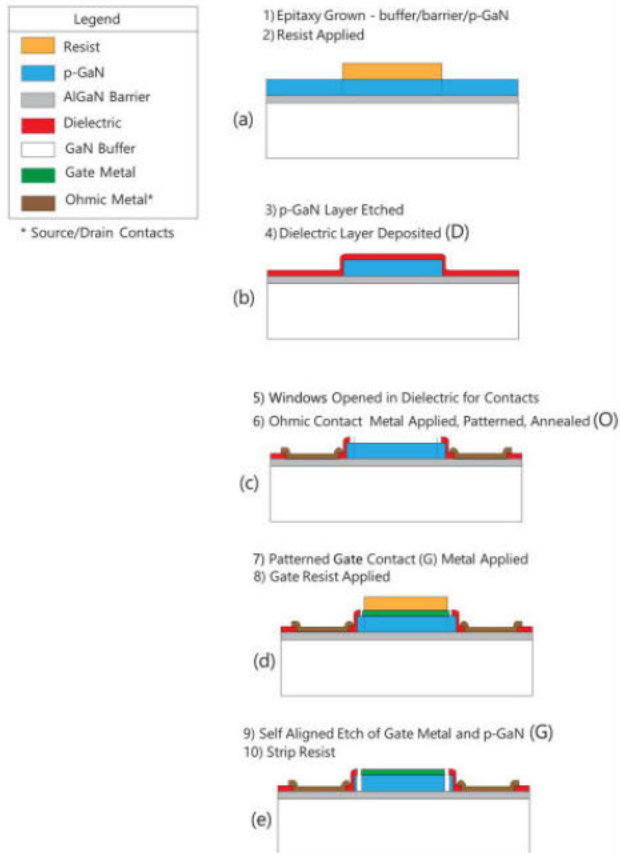
(Paper 17 at 23 (citing Ex. 2001 ¶ 90))

- Gate-last (Dielectric, Ohmic, Gate) are inoperable
 - **D-O-G** processes result in remnant islands
 - Transistors including remnant islands would not function as intended enhancement-mode devices (POR, 23 (citing Ex. 2001 ¶ 90))
- Since ohmic material deposited before gate, cannot achieve:
 - Field plate over the gate structure field; or
 - Simultaneous patterning and etching of source contact and field plate

Revised D-O-G Processes Non-Operable and Does not Align with Claim Language

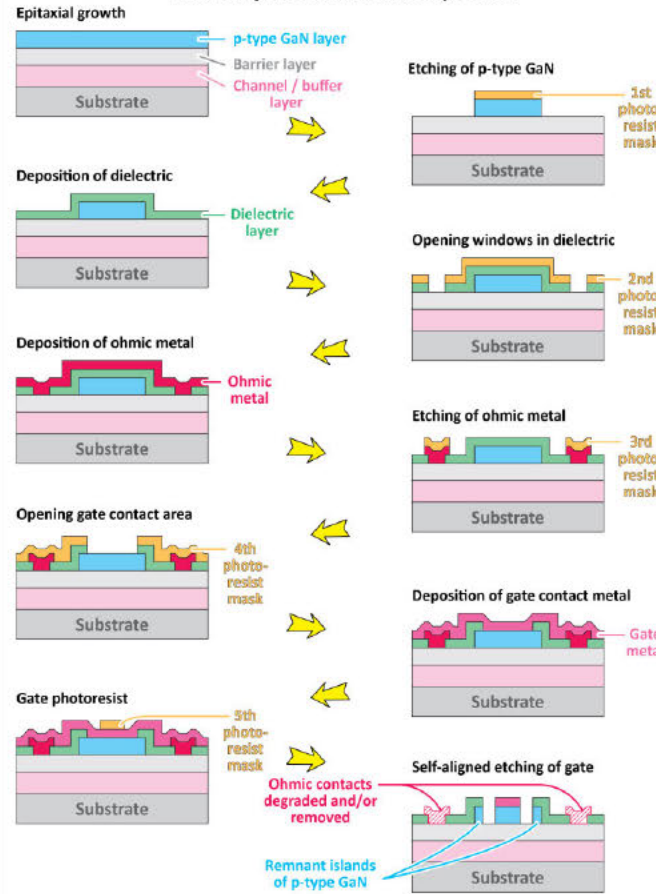
Dr. Shealy's Revised D-O-G Process

DOG Process Order (Beneficial Remnant P-Type GaN Island)



(Paper 18 at 5)

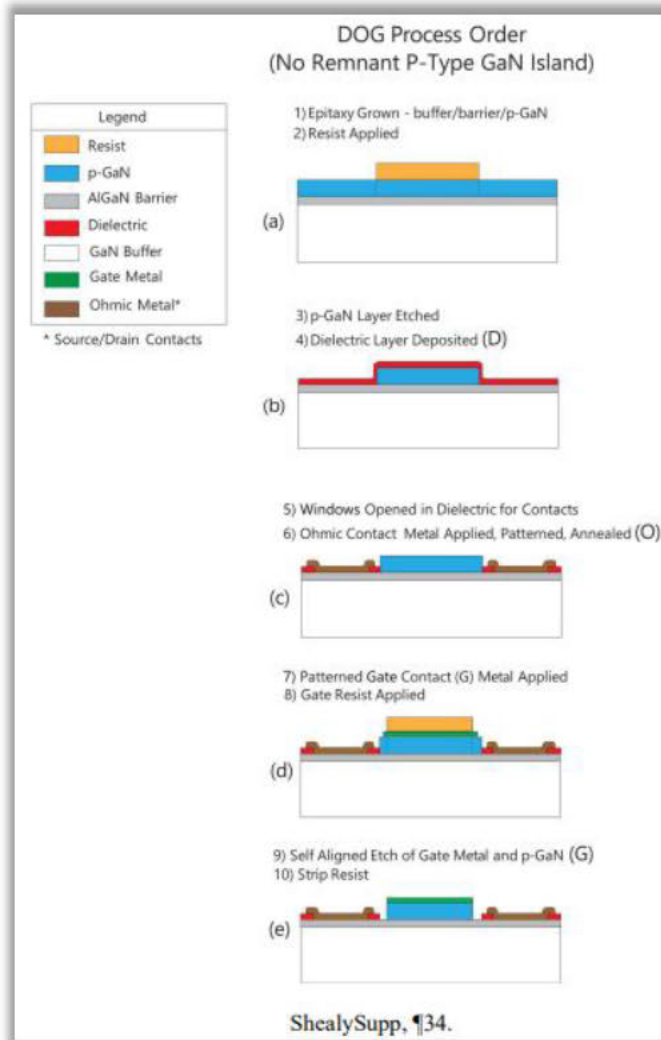
Dr. Shealy's DOG fabrication process



(Paper 20 at 7)

- Hypothetical **D-O-G** processes are not relevant
 - No claim language or specification analysis
- Revised **D-O-G** processes do not meet claim language
 - No analysis how remnant islands meets limitation [1e4] "etching away the doped GaN layer, except a portion of the doped GaN layer beneath the gate contact"
- Results in remnant p-GaN islands
 - Operability of remnant islands in enhancement mode devices is based on incomplete speculation
 - No evidence remnant island containing devices with self-aligned gate structures and/or field plates formed together with contacts would be operable
- No analysis that hypothetical process to remove remnant islands can meet claim language – omits steps

Petitioner's Proposed D-O-G Process without Remnant Islands is Incomplete

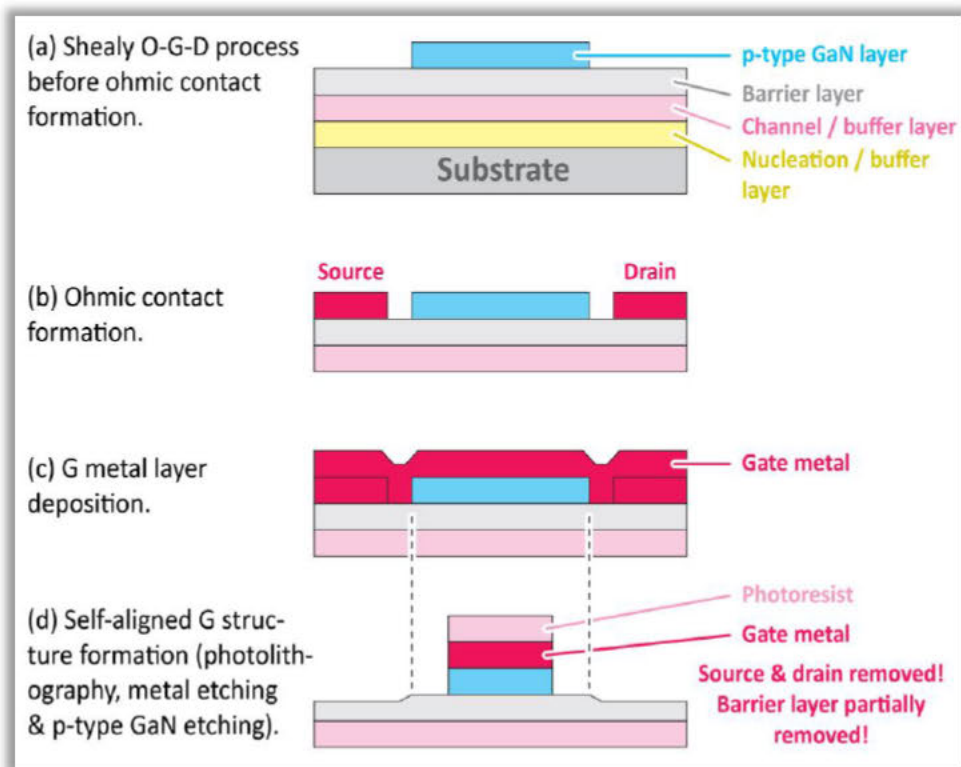


(Paper 18 at 7)

- Incomplete process without all steps shown
 - E.g., no steps showing formation of gate contact – step (d)
- Failure to demonstrate this process meets claim limitations
- Conclusory opinion
- No capability of process to form field plate together with ohmic contacts

Non-G-D-O Processes Cannot Achieve “Present Invention” and Align with Claims

Dr. Shealy's Described **O-G-D** Process



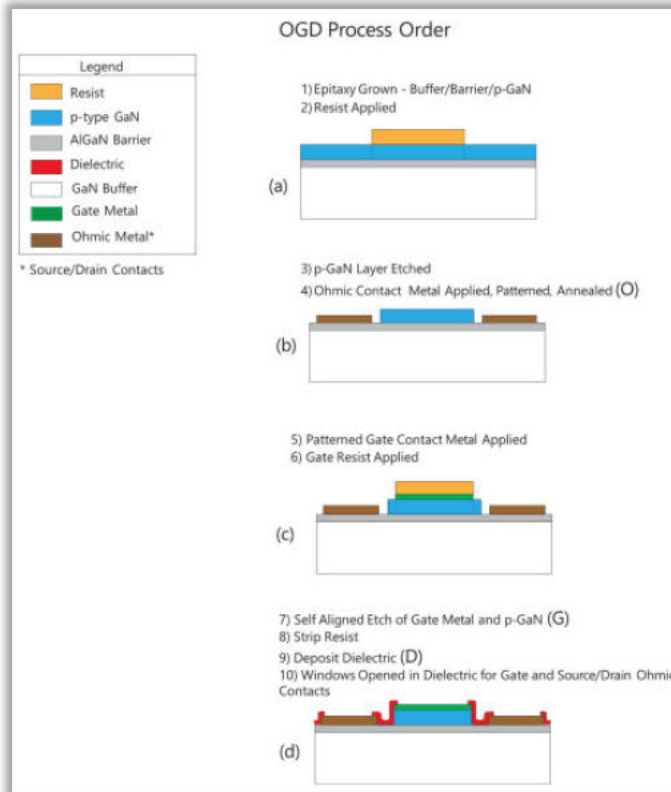
(Paper 17 at 25 (citing Ex. 2001 ¶ 96))

- **O-G-D** Process is materially different than process described and claimed in '508 patent
 - No analysis of claim language and specification supporting process
 - Numerous inefficiencies:
 - Multiple etchings of gate material
 - Self-alignment etching step will etch exposed barrier layer (POR 24-25 (citing Ex. 2001 ¶ 96))
 - Gate metal etching will remove portions of source and drain contacts since unprotected
- Since ohmic material deposited before gate, cannot achieve:
 - Field plate over the gate structure field; or
 - Simultaneous patterning and etching of source contact and field plate

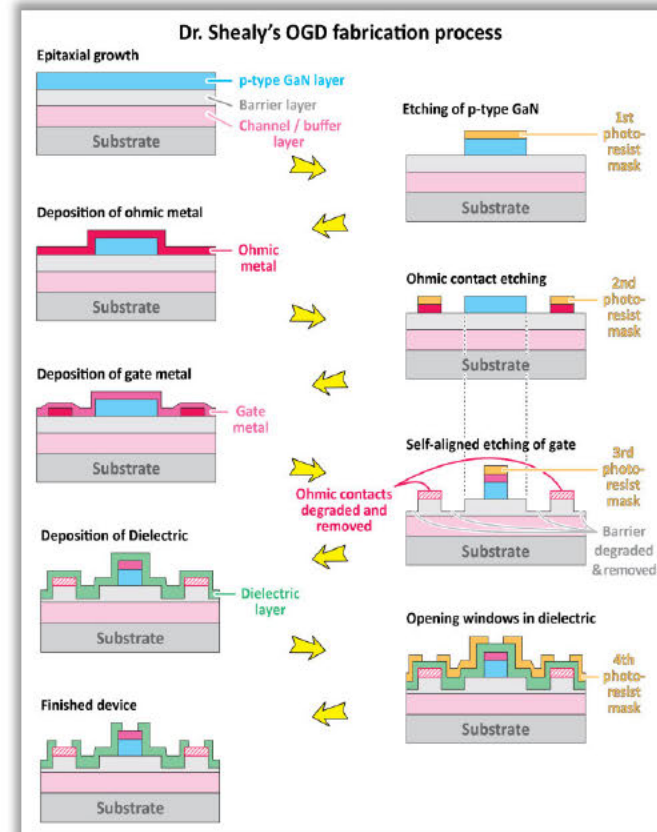
No (Con't)

O Processes Cannot Achieve “Present Invention” and Align with Claims

Dr. Shealy's Revised O-G-D Process



(Paper 18 at 9)



(Paper 20 at 10)

- No evidence Dr. Shealy's proposed **O-D-G** process even meets claim language
 - No analysis how [1f3] “etching the dielectric layer to open the drain and source contact area” is met in context of '508 patent
 - Ohmic formed before dielectric
 - Contrary to Board's Interpretation
 - Contrary is language of claims
 - Contrary to specification
- Results in non-operable embodiment from degradation and removal of ohmic metal during subsequent etch

Only G-D-O Construction Can be Correct Construction

1. A method of forming an enhancement mode GaN transistor, the method comprising:

nucleating and growing transition layers on a substrate;
growing an III Nitride EPI layer over the transistor layers;
growing an III Nitride barrier layer over the EPI layer;
growing a GaN layer with acceptor type dopants over the
barrier layer;

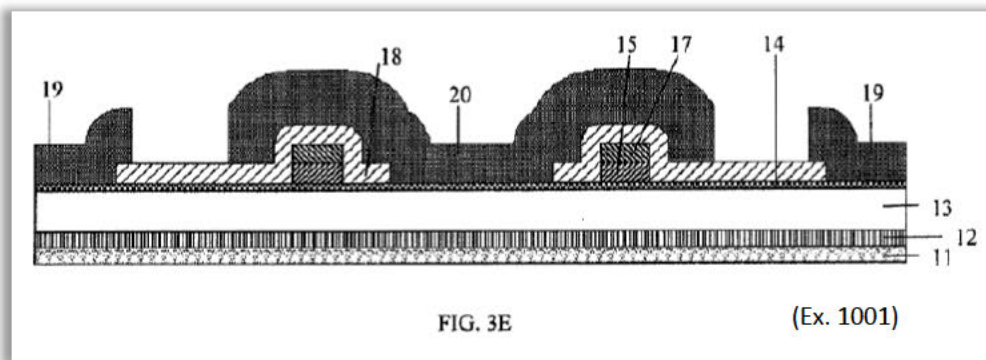
depositing a gate contact layer on the doped GaN layer;
applying a gate photo resistant pattern;
etching away the gate contact layer outside the gate region;
etching away the doped GaN layer, except a portion of the
doped GaN layer beneath the gate contact;
removing the gate photo resistant pattern;

- depositing a dielectric layer;
- applying a contact photo resistant pattern;
- etching the dielectric layer to open the drain and source contact area;

removing the contact photo resistant pattern;
depositing an Ohmic contact metal;

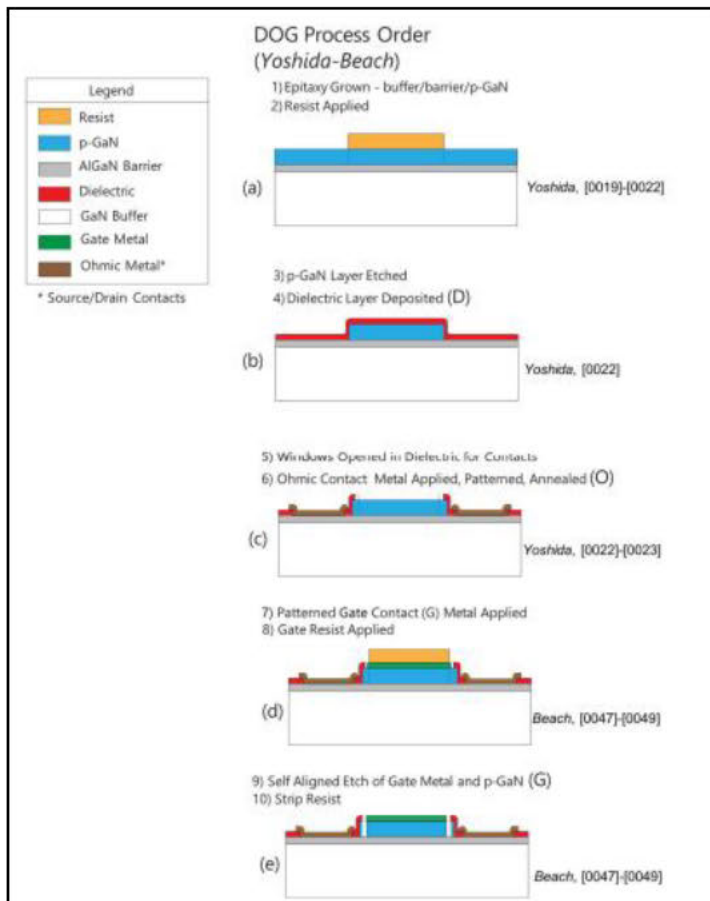
applying a metal photo resistant pattern;
etching the Ohmic contact metal;
removing the metal photo resistant pattern; and
performing rapid thermal annealing to form Ohmic drain
and source contacts.

- Only **G-D-O** Process:
 - Performs “present invention”
 - Claims dictate construction
 - Specification dictates construction
 - Complies with all embodiments of specification
 - Forms an operable enhancement mode HEMT transistor

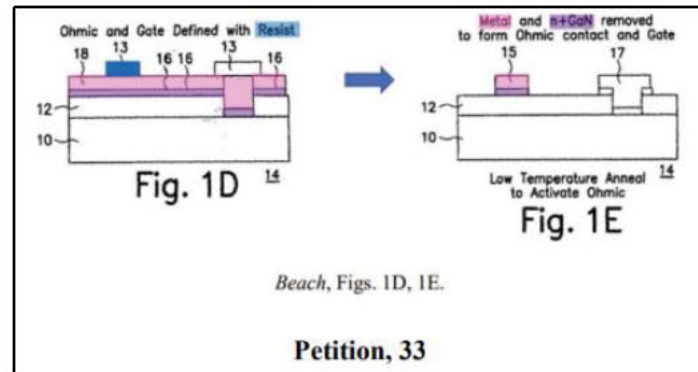


Improper Reply Evidence

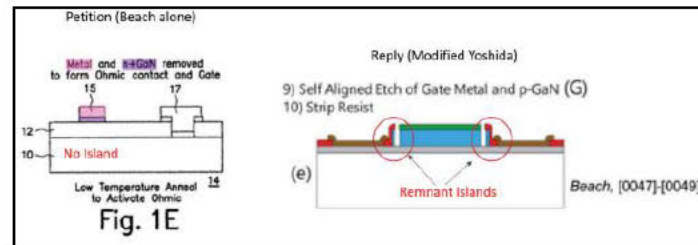
Reply Disclosed New Sequences and Motivations to Combine Too Late



(Paper 18 at 14)



(Paper 20 at 17)



(Paper 20 at 18)

- New theory of invalidity based on combination of process steps instead of individual steps
 - E.g., abandoning limitation-by-limitation analysis relying on individual reference per limitation
- New analysis could have been presented earlier
 - Not responsive to arguments
 - Gap-fills:
 - Includes new expert testimony that could have been included in Petition
 - Attempts to show analysis pertaining to invention as a whole

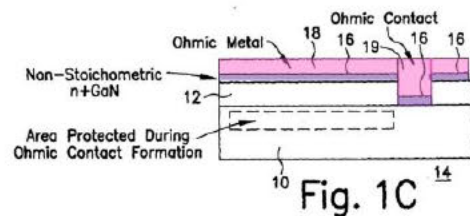
if necessary to respond to petitioner's reply. Petitioner may not submit new evidence or argument in reply that it could have presented earlier, e.g. to make out a prima facie case of unpatentability. A party also may submit rebuttal evidence in support of its reply. See

(TPG at 73; Paper 20 at 11)

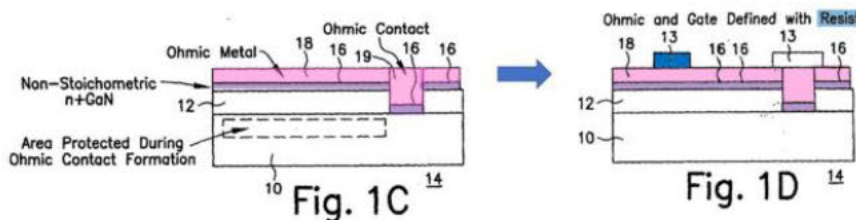
Reply Sequences and Motivations to Combine are Patently New

Petition analyzed only isolated individual limitations
by reference

“Beach discloses element [1e1]”

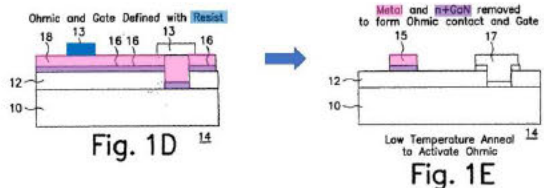


“Second, Beach discloses step [1e2]”



Beach, Figs. 1C, 1D.

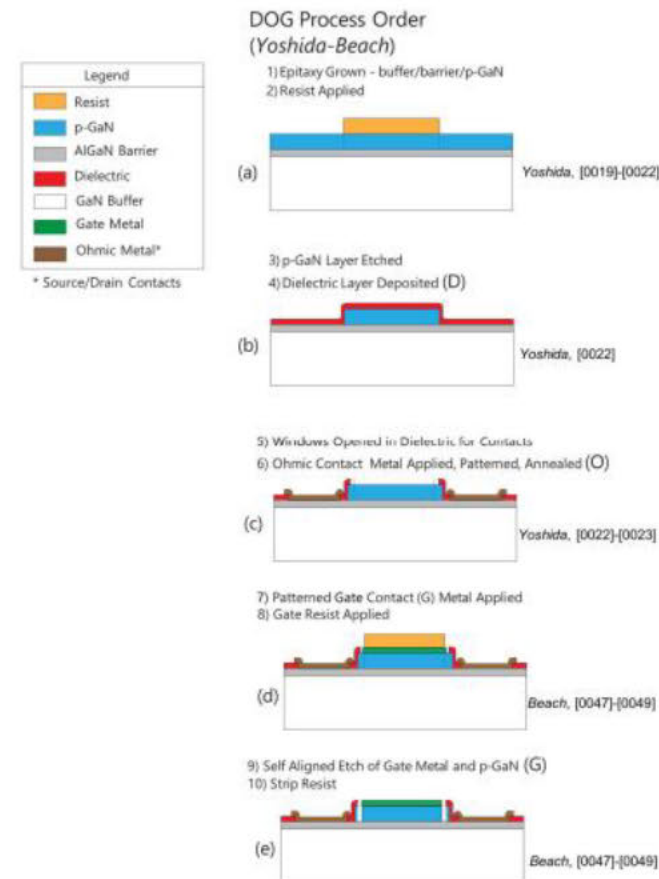
“Third, Beach discloses
step [1e3]...and [1e4]”



Beach, Figs. 1D, 1E.

(Paper 1 at 31-33)

Reply analyzed process as whole by combined references



(Paper 18 at 14)

Petition's Invalidity Theory Never Addressed Invention as a Whole
Petition Never Explained How to Combine Prior Art Processes

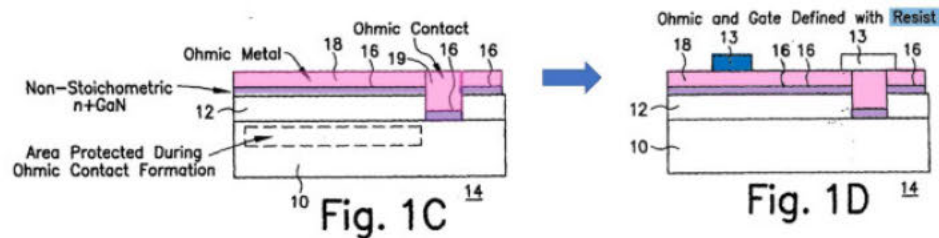
DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Reply's Changing Invalidity Theory

Reply: “combination of *Yoshida-Beach* renders obvious separate steps of applying a gate photo resistant and metal photo resistant patterns at different times” (Paper 18 at 25, 30, 33)

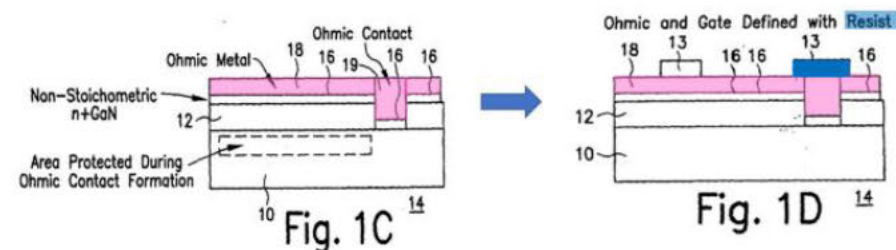
Petition:

Second, *Beach* discloses step [1e2], i.e., applying a **gate photo resistant pattern 13** (mask) to the structure, as shown below. *Beach*, [0047] (“resist material 13 is deposited in a pattern to permit the formation of a gate 15 and ohmic contact 17”).



(Paper 1 at 32)

Second, *Beach* discloses that a **metal photo resistant pattern 13** (mask) is applied over the **ohmic contact metal 18**. *Beach*, [0047] (“resist material 13 is deposited in a pattern to permit the formation of a gate 15 and ohmic contact 17.”).



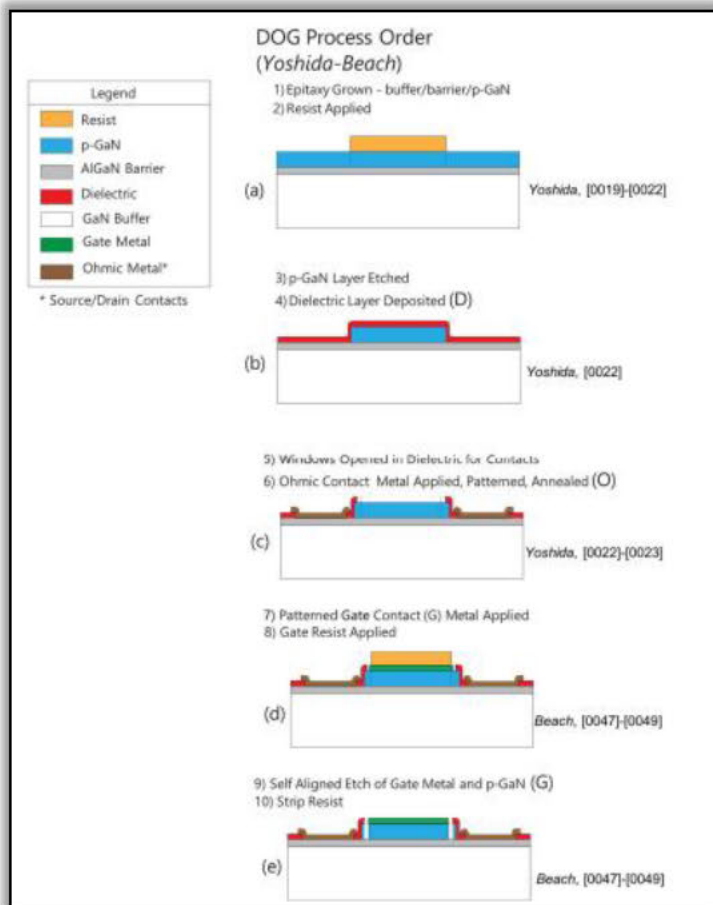
Beach, Figs. 1C, 1D.

(Paper 1 at 35-36)

- Petition included no assertion of separate steps of two photo resistant patterns
 - Same step identified
 - No identified motivation to modify single step of Beach into two steps

(Paper 20 at 13)

Reply's New Motivations to Combine

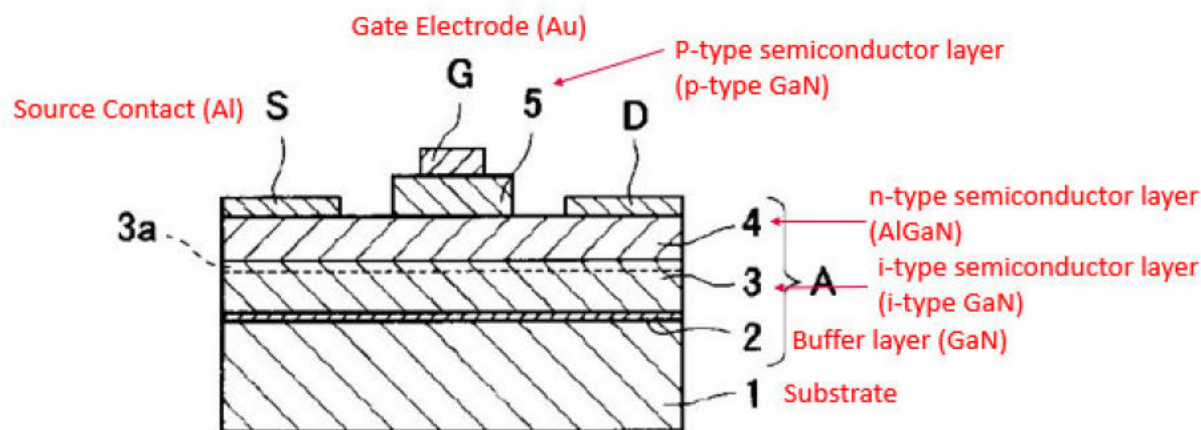


(Paper 18 at 14)

- Reply's new sequences rely on new testimony from expert including new motivations to combine (Paper 20 at 14)
 - E.g., "protect[ing] the gate region from contamination during subsequent processing steps" – justifies figures (d) and (e)
 - New motivation to combine based on conventional nature of self-aligned gate structures
- Never proposed sequence as whole – no analysis of individual steps interacting with each other
- New sequences and motivations to combine are not responsive to arguments but instead supporting newly identified invalidity theory

Ground 1 (Claims 1-3): Yoshida, Sheppard, and Beach

Cited Prior Art: Yoshida – “Gate-Last”



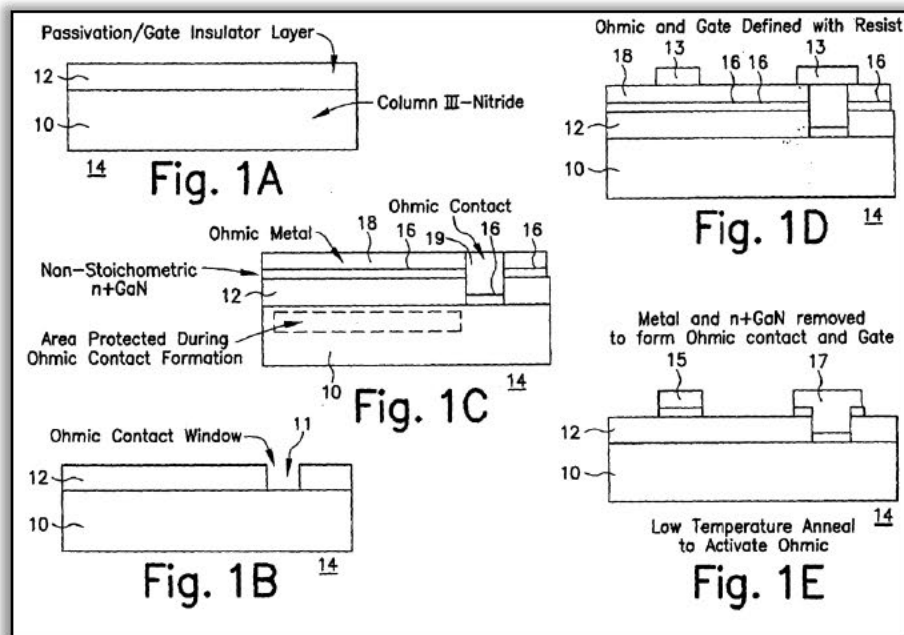
(Paper 17 at 45 (citing Ex. 2001 at ¶ 85))

- Yoshida's "Gate-Last" Process

- Grow layers 2-5 over substrate 1
- "[E]tch away the p-type GaN layer except where the gate electrode was to be loaded"
(Ex. 1004 at [0022])
- Deposit a dielectric layer to cover exposed surface
- Apply photo resist/mask, opening spaces in dielectric layer for source (S) and drain (D) electrodes
- Deposit Al in openings and form S and D electrodes
- Remove photo mask and open dielectric film over p-type GaN gate material leaving electrodes masked
- Deposit Au in opening to form gate electrode and then form gate contact above p-type GaN

(Paper 7 at 8-9)

Cited Prior Art: Beach – “Gate-Simultaneous”



(Paper 17 at 45 (citing Ex. 2001 at ¶ 85))

- Gate-simultaneous process to form depletion mode transistor
 - Form ohmic contact window 11
 - Deposit n-type protective material 16
 - Deposit ohmic metal 18
 - Simultaneously pattern and etch gate and ohmic contact
 - Results in remnant islands (ohmic contact 17)

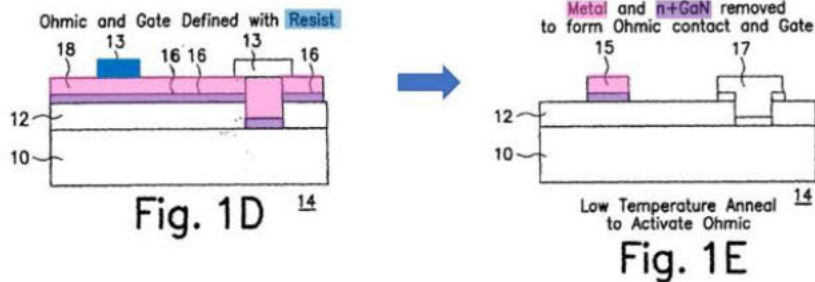
[0047] Referring now to Figure 1D, resist material 13 is deposited in a pattern to permit the formation of a gate 15 and ohmic contact 17. After the deposition of photoresist layer 13, material 18 is removed, as by etching, except where protected by photoresist 13. The removal, or etching process, also eliminates protective layer 16 under patterned photoresist 13.

(Ex. 1005 at ¶ [0047])

Petitioner Fails to Identify Motivation to Combine Yoshida and Beach

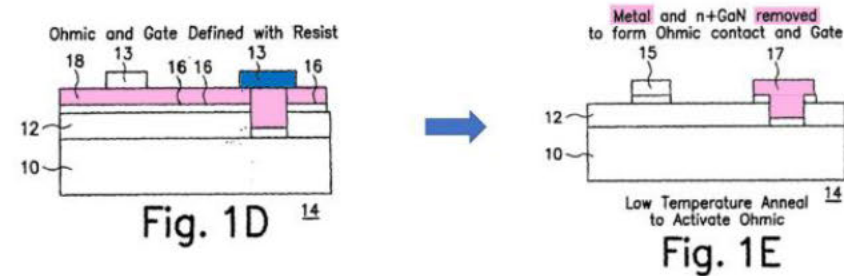


- Petitioner's invalidity analysis is hindsight based as it relies exclusively on picking and choosing discrete elements of prior art without analysis of combination or invention as a whole
 - InTouch Tech., Inc. v. VGO Commc'ns., Inc.*
751 F.3d 1327 (Fed. Cir. 2014)
- No analysis on how Yoshida and Beach hypothetical process combination interacts in Petition
- No expectation of success because no analysis of combination



Beach, Figs. 1D, 1E.

(Paper 1 at 33)

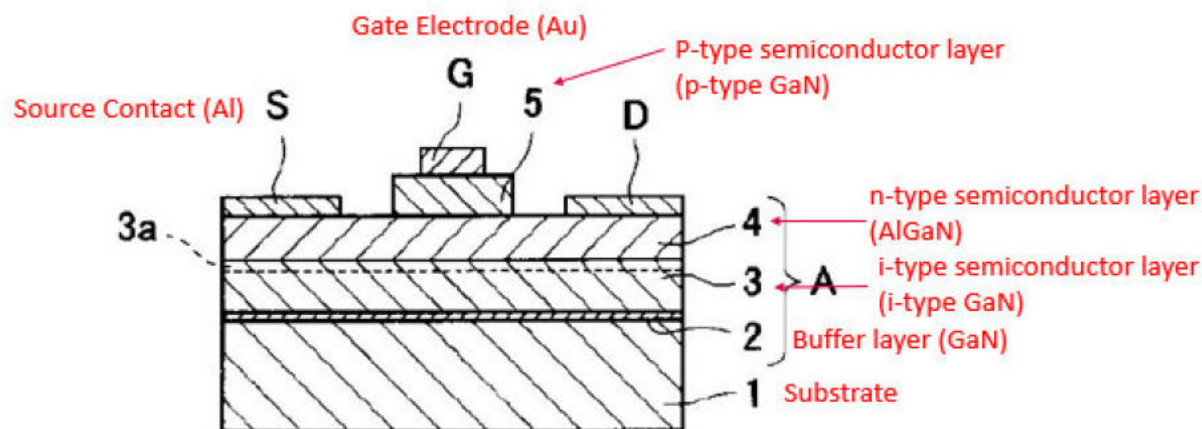


Beach, Figs. 1D, 1E.

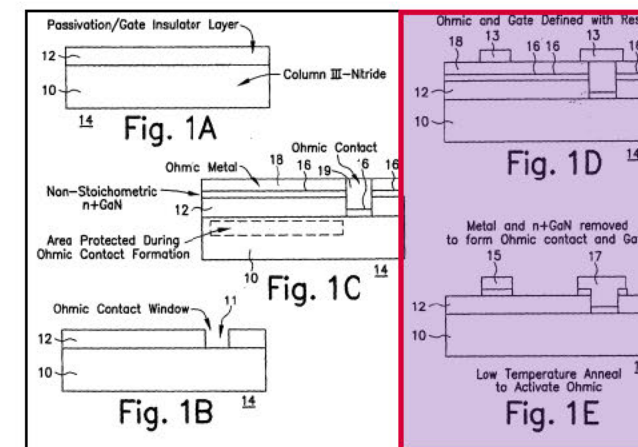
(Paper 1 at 37)

Petitioner Fails to Identify Motivation to Combine Yoshida and Beach (Cont'd)

Gate-Last

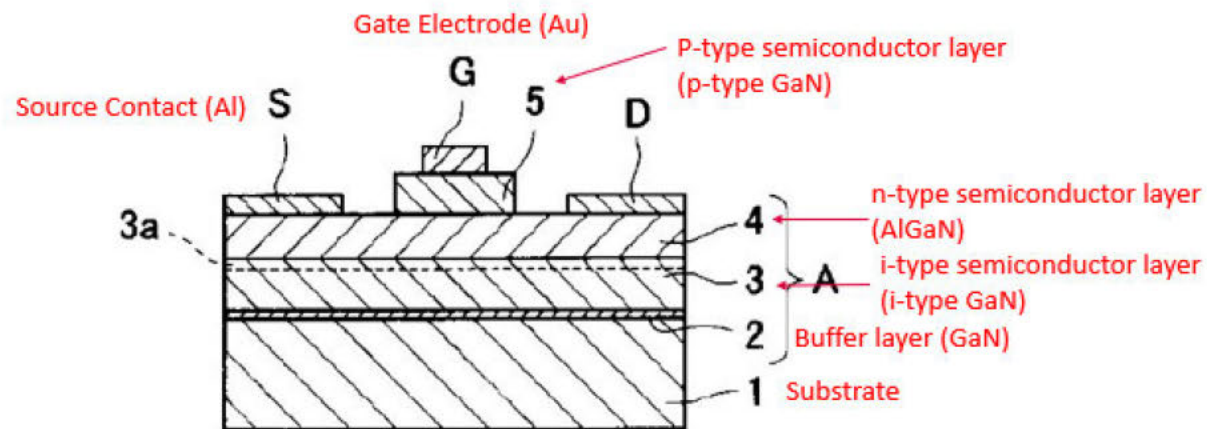


Gate-Simultaneous

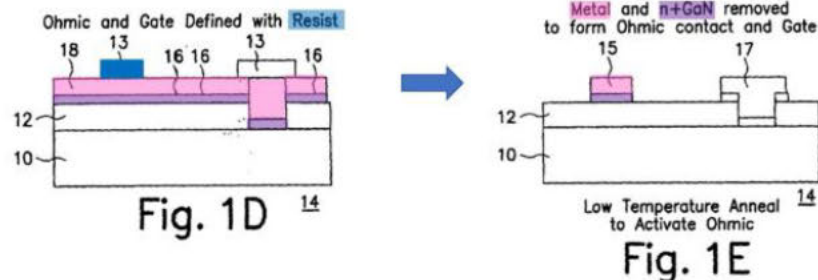


- Petition identifies no specific modification to combine *Yoshida* with *Beach* to achieve claimed invention
- No proposed modification to achieve a “gate-first” process
 - Petitioner’s expert agrees: “good reasons not to necessarily choose that path” (Ex. 2002 at 85:19-86:8, 95:11-23)
- Petitioner’s identified motivations to combine are inconsistent and contrary to proposed gate formation
 - “where the gate electrode was to be loaded” – Not motivation because based on requirements of non-self-aligned process
 - No reduction in overall number of etching steps because a self-aligned process achieving Yoshida would involve more steps
 - Differences in processes and process steps dissuades a POSA from incorporating teaching from gate-simultaneous to gate-last process
 - Gate-Simultaneous is distinct: No indication what portions or how to incorporate
 - Gate-Simultaneous involves same metal for ohmic contact and gate material
- Combination of Gate-Last and Gate-Simultaneous would result in inoperable device – ohmic contacts formed on p-GaN material

Petition's Combination is Premised on Hindsight

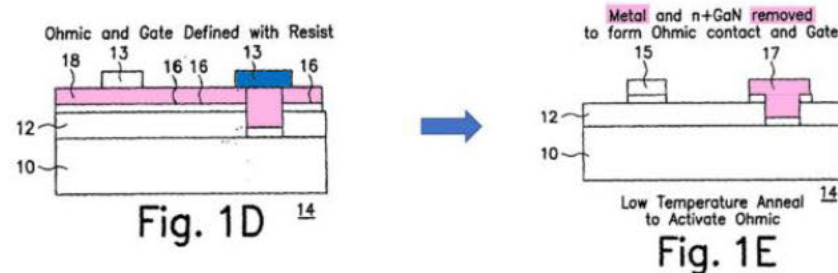


- The Petition's "mix and match" approach solely identifies elements allegedly disclosed by prior art but fails to describe a proposed combination and cannot therefore establish an expectation of success
- No analysis of modifying Yoshida to achieve invention as a whole
- Absent hindsight – no reason to combine elements of Yoshida and Beach with expectation of success



Beach, Figs. 1D, 1E.

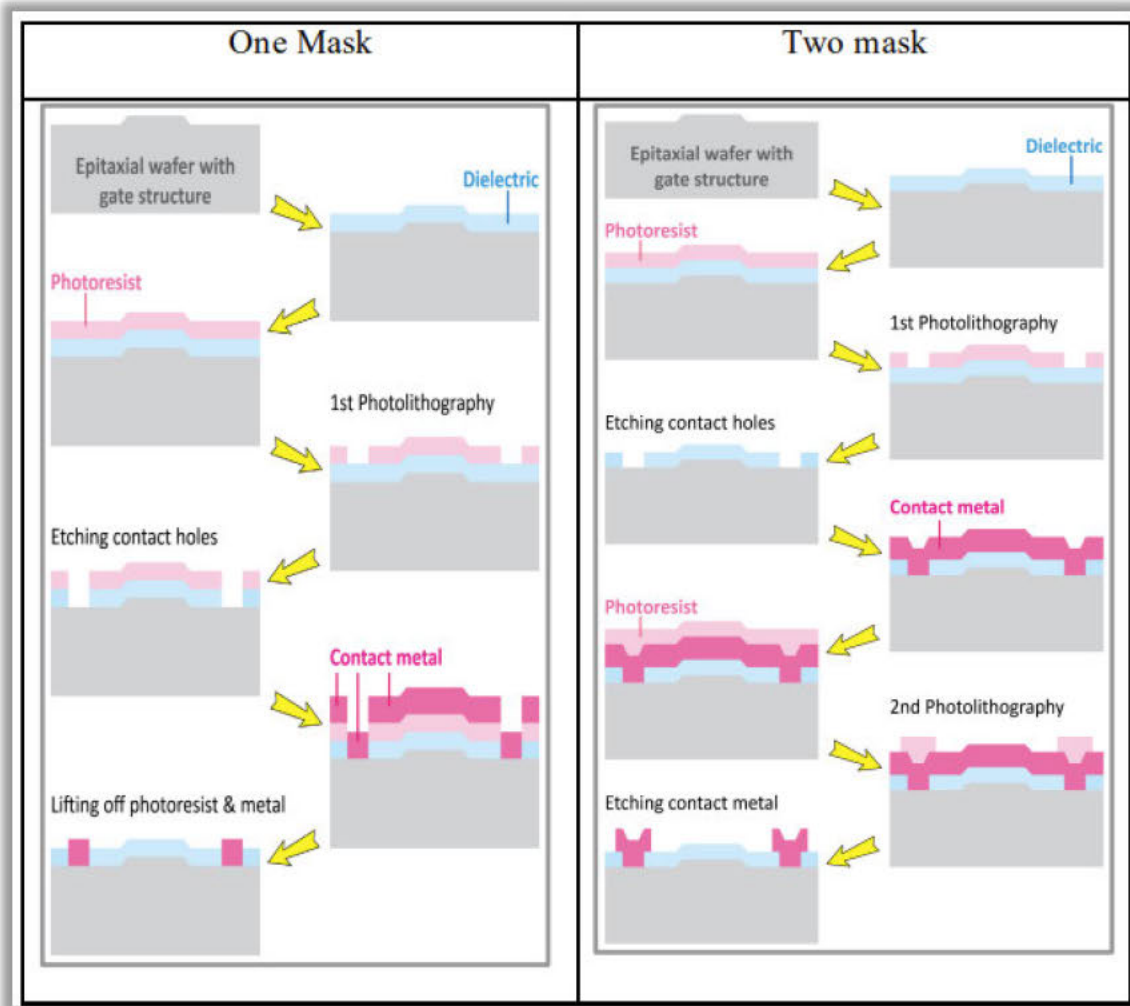
(Paper 1 at 33)



Beach, Figs. 1D, 1E.

(Paper 1 at 37)

No Motivation to Replace Yoshida's Ohmic Formation With Beach's Two-Etch Process



(Paper 17 at 43)

- Yoshida does not disclose a two-etch ohmic process
 - Yoshida's description and figure indicates lift-off
- Beach's gate formation is two etchings
- Depiction in Yoshida's figure different than two-etching process in Beach
- No reason to modify Yoshida to incorporate two-etching process – no expectation of success
 - Two-Mask of Beach more complicated (cost, time)
 - Lift/off or one mask of Yoshida simpler
 - Two-Mask results in residual material below contact (not depicted in Yoshida)
- Permit formation of field plate – hindsight
- Motivation contradicts self-alignment motivation

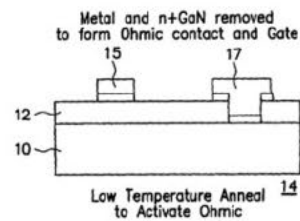
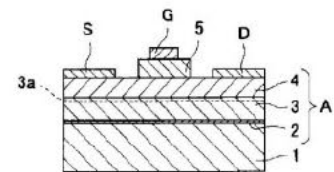


Fig. 1E
EX1005 FIG. 1E



EX1004

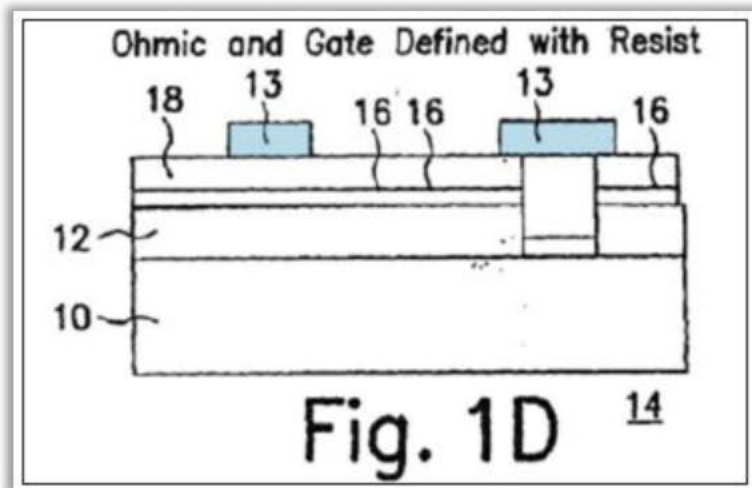
(Paper 17 at 45)

A POSA Would Not Replace Yoshida's Ohmic Formation Process With More Complicated Process

- Petitioner relies upon generalities of transistor fabrication processes instead of Yoshida's disclosure
 - No evidence Liang or Gorowitz are applicable to Yoshida/Beach process
 - References are general and do not rebut Dr. Schubert's opinion based on Yoshida
 - Petitioner's alleged motivation to combine Yoshida and Beach because lift-off and etching are only two formation processes is overly generic
 - References of record show numerous processes and structures within lift-off
 - The '508 Patent demonstrates even with photo masking there are different types of processes
 - Inconsistent with Petitioner's motivation to select self-alignment for simpler process because proposed combination is more complicated for ohmic formation than taught by either reference
 - Petitioner's new combination includes more photomasking steps than the prior art

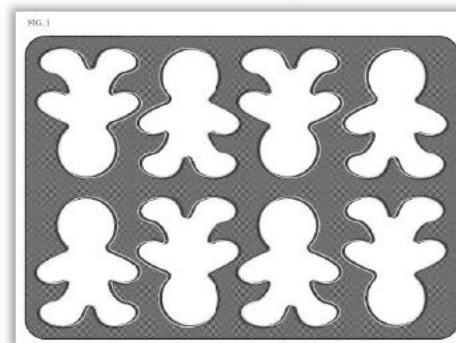
(Paper 20 at 23-26)

Prior Art Fails to Disclose Separate “*applying*” Gate Pattern and Metal Pattern

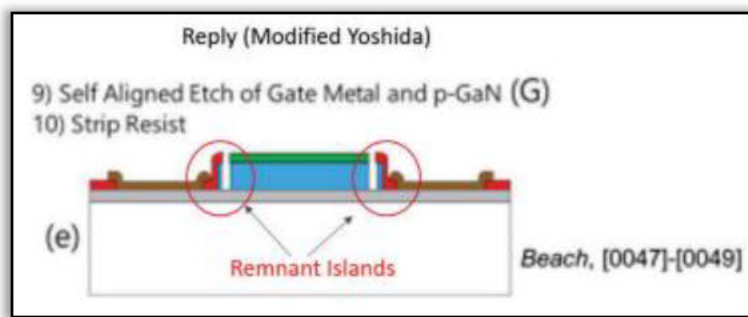


[0047] Referring now to Figure 1D, resist material 13 is deposited in a pattern to permit the formation of a gate 15 and ohmic contact 17. After the deposition of photoresist layer 13, material 18 is removed, as by etching, except where protected by photoresist 13. The removal, or etching process, also eliminates protective layer 16 under patterned photoresist 13.

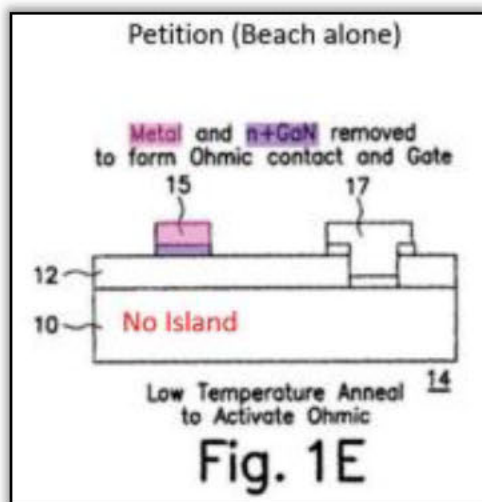
- Petition relies on Beach for both:
 - [1e2] applying a gate photo resistant pattern; and
 - [1g2] applying a metal photo resistant pattern
- Petition never sets forth proposed modification of Yoshida to achieve claimed step
- Beach discloses *and* teaches a single step of depositing resist material 13
 - Single step cannot teach two discrete steps: *Becton, Dickenson & Co. v. Tyco Healthcare Grp., LP*, 616 F.3d 1249 (Fed. Cir. 2010)
 - Single step – not two steps performed simultaneously
- No motivation to apply resist 13 in separate process steps
 - Hindsight only – no motivation to select; more mask steps
- Combination fails to disclose gate-first process



Petitioner's New Sequence Shows Ground 1 Does Not Teach [1e4]



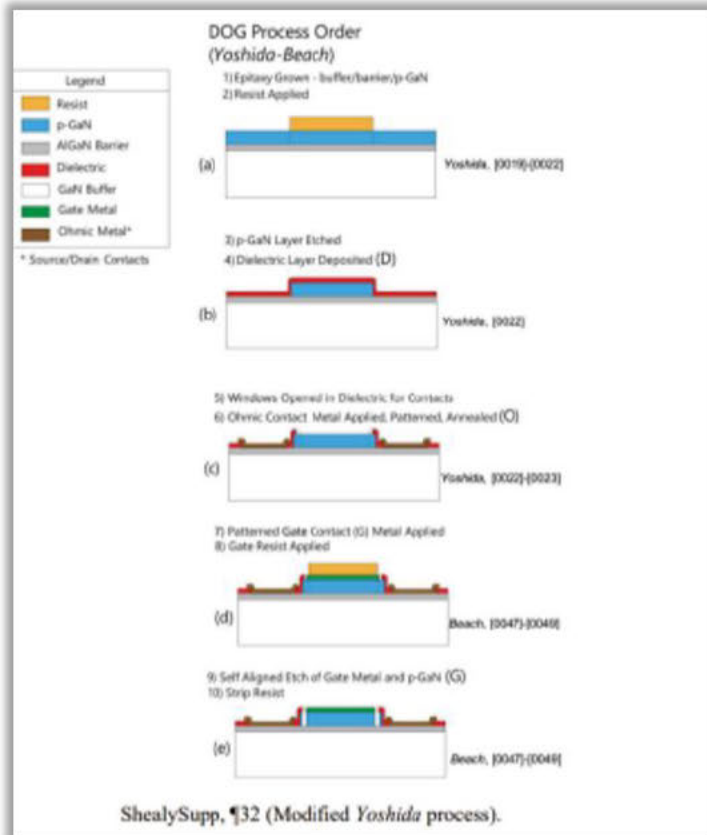
(Paper 20 at 18)



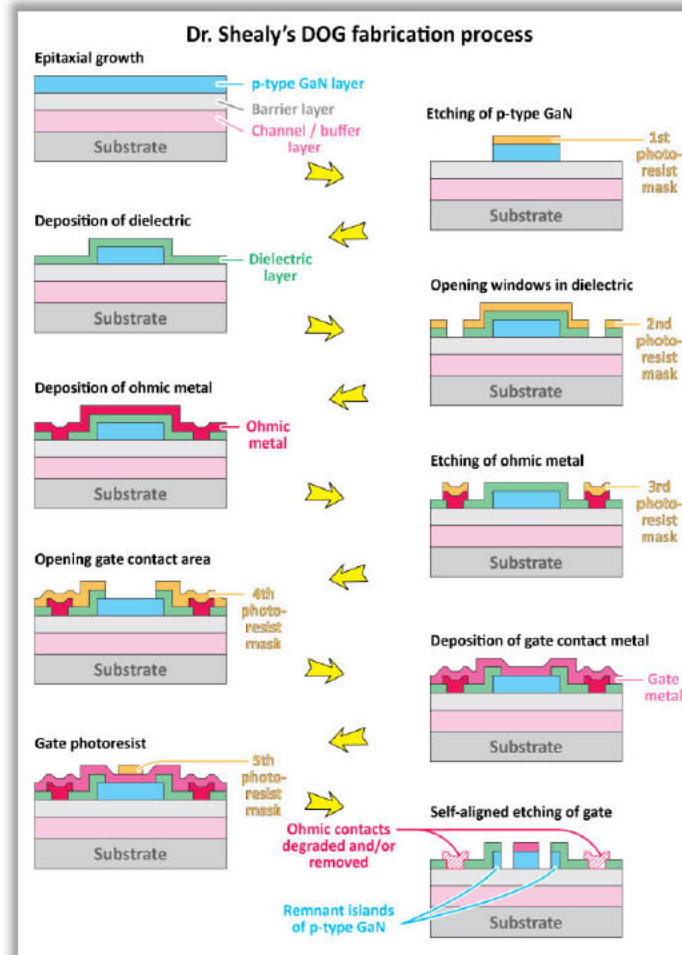
(Paper 20 at 18)

- Reply process sequence shows prior art does not teach “etching away the doped GaN layer, except a portion of the doped GaN layer beneath the gate contact” (Paper 20 at 16-18)
 - Remnant islands not addressed by Petitioner
 - Petition identified left side of FIG. 1E that did not include remnant islands
 - “Beach discloses...step [1e4], i.e., etching away the doped GaN layer, except a portion of the doped GaN layer beneath the gate contact...”
- Theory of invalidity changed from Beach FIG. 1E left side without remnant islands to new sequence including remnant islands
 - Either improper change in theory that Beach alone teaches [1e4] to sequence combination teaches [1e4]; or
 - The Petition failed to explain how a process including remnant islands meets [1e4]
- Bodily incorporation is not relevant because Petitioner identified the particular elements and did not identify specific combinations

No Motivation to Combine Ground 1 to Arrive at New Sequence



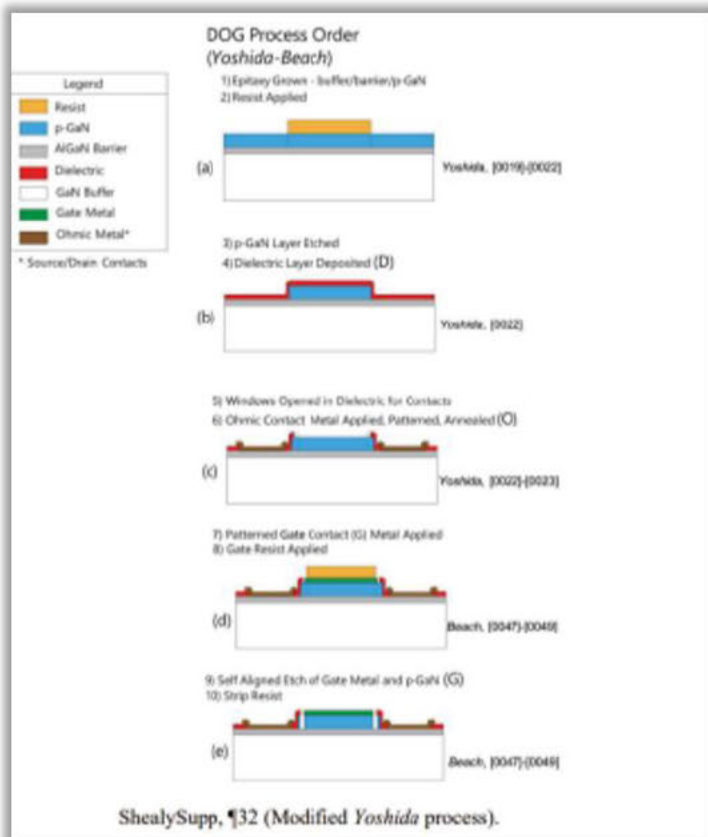
(Paper 18 at 14)



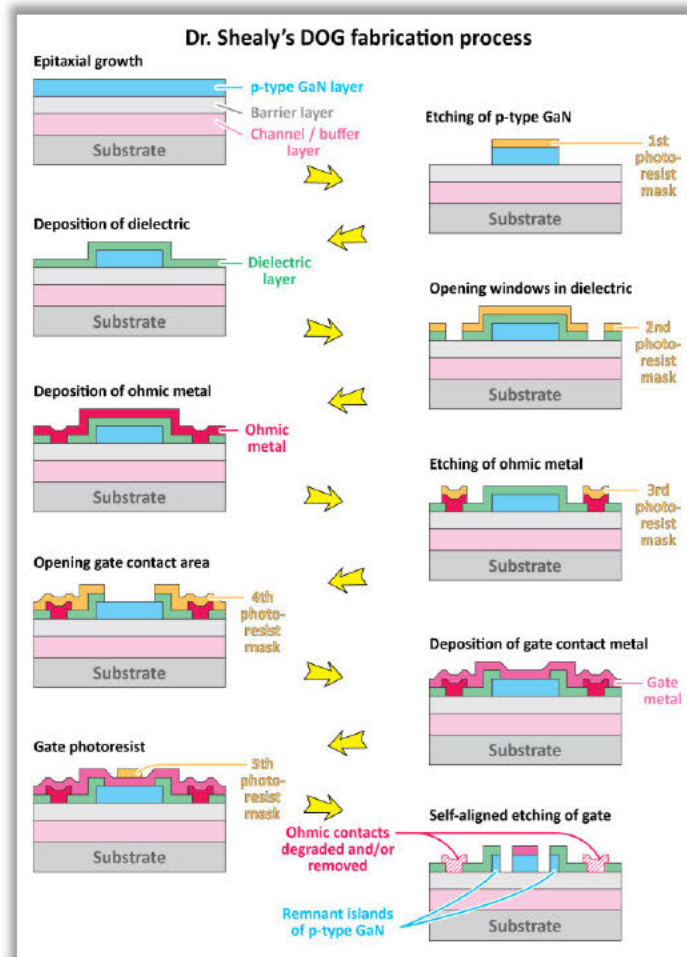
(Paper 20 at 7)

- The Petition's identified Motivations to Combine do not Apply to Reply Sequence (Paper 20 at 21)
 - More complicated: Multiple additional photomasks (>4)
 - Requires two-etching steps of p-type material
 - Inconsistent with etching p-type GaN except where gate electrode to be loaded

Hindsight is Only Basis for Petitioner's Proposed Sequence



(Paper 18 at 14)



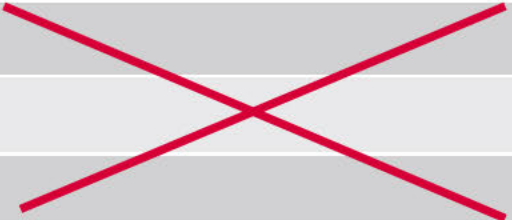
(Paper 20 at 7, 24)

- Petition did not include proposed sequence
 - Difference in prior art process order, structural arrangement, method of operation, and materials would have dissuaded a POSA from the combination
- Analysis concerning proposed sequence further evidences it is based on '508 patent
- Dr. Shealy's **D-O-G** analysis generalizes transistor formation sequence to avoid steps
 - D, O, G** formation processes were known; difference is in the process as a whole
 - Petitioner does not tie the combined sequences to the claim elements

(Paper 20 at 22-24)

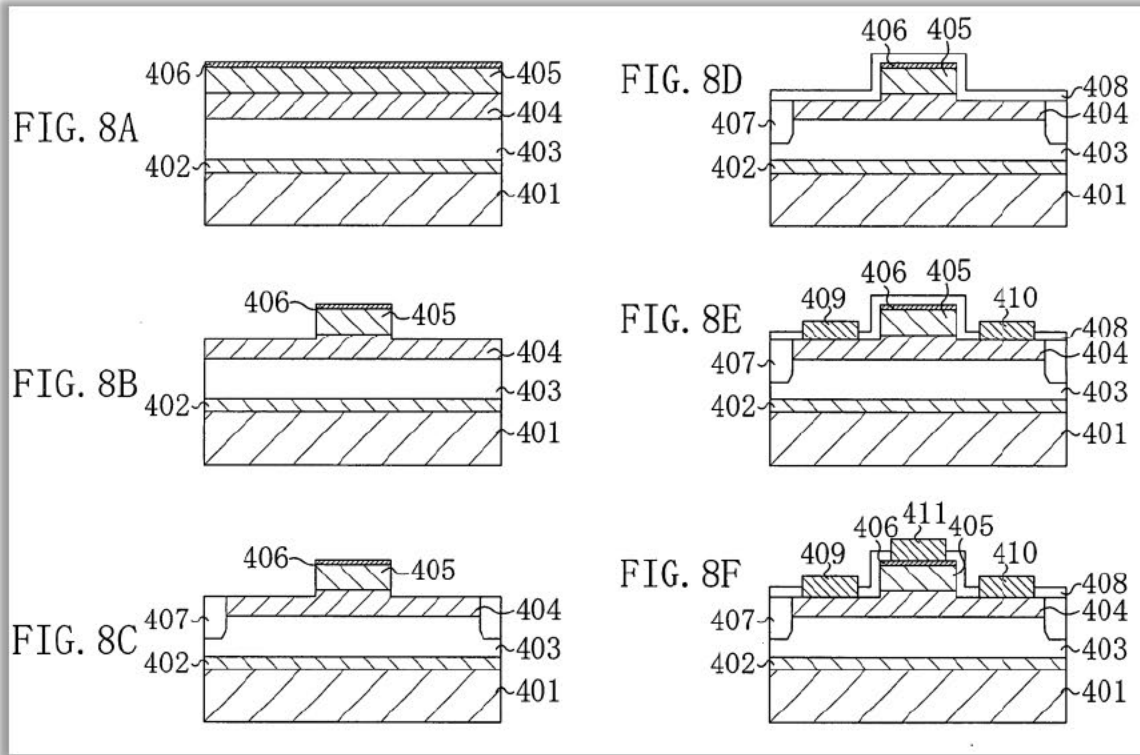
No Motivation to Combine to Arrive at Gate-First Process

- The Petition never proposed Yoshida, Beach, Sheppard combination resulting in gate-first process (Paper 20 at 20)
 - Petitioner's allegation that a "gate-first" process would be obvious as one of only six sequencing permutations does not address differences between prior art and a gate-first process (*Id.*)
 - No motivation to change from gate-last and gate-simultaneous to arrive at gate-first (*Id.*)
 - Differences between prior art to modify each process element is too complicated and not explained
 - Petitioner's assertion is too general – significant number of variables would result in lack of expectation of success

Gate-First	Gate-Simultaneous	Gate-Last
		Yoshida
	Beach	
		Sheppard



Ground 2 (Claims 1-4): Hikita347, Sheppard, and Beach

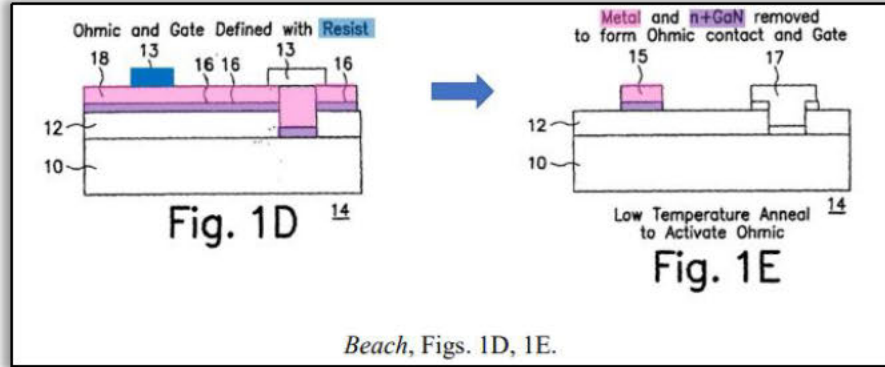


(Ex. 1007)

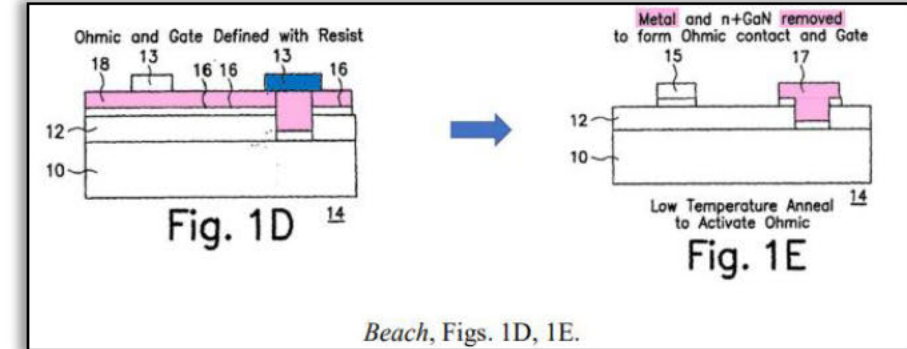
- “Gate-Last” enhancement mode GaN transistor
 - Source & drain formed before gate electrode
- Single photo-mask ohmic formation process

Petitioner’s Proposed combination of Hikita347, Sheppard, and Beach is materially the same as Ground 1

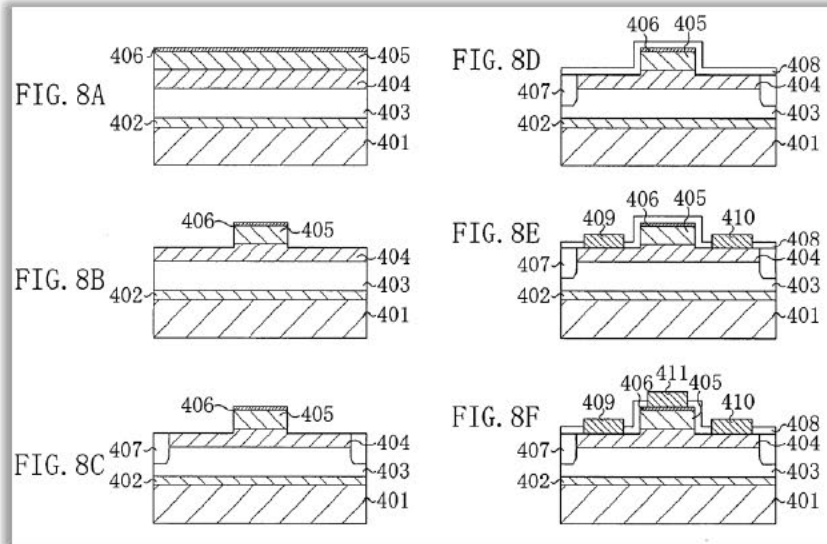
The Petition Failed to Identify with Particularity a Proposed Combination



(Paper 1 at 33)



(Paper 1 at 37)



(Ex. 1007)

- No showing how “jigsaw puzzle” assembled
- No explanation of “Gate-Last” combination with “Gate-Simultaneous”
- No showing invention obvious as a whole

No Motivation to Combine Gate-Last Process with Gate-Simultaneous Process

- Hikita347 is indisputably gate last; Beach is indisputably a gate-simultaneous
 - Petition basis motivation to combine references on same motivation as Yoshida/Beach
 - Motivation is lacking and inconsistent for same reasons as Yoshida/Beach
 - Motivation to combine with expectation of success is similarly deficient because Petition similarly did not explain proposed combination of “gate-simultaneous” and “gate-last” positions
- The Petition’s motivation to combine includes a misunderstanding of the disclosure
 - Hikita347 never discloses gate formation before or simultaneous to ohmic formation

No Motivation to Apply Beach's Two-Etching Process to Hikita347

- Petitioner's identified motivation to combine is deficient for same reasons as Ground 1
- Hikita347 similarly does not disclose a two-etch ohmic formation process
- Proposed combination premised on same hindsight to modify Hikita347 into a two-etch process
 - Combination of "gate-last" with "gate-simultaneous" processes for dielectric and ohmic formation
 - Substitutions "picked and chose" from hindsight
 - Hikita347 use of ohmic metal does not provide particularized motivation
 - Creates more steps
 - Hindsight evident by relying on '508 patent's disclosure of field plate as justification

[0060] Next, as shown in **FIG. 8E**, openings are formed in a SiN film, for example, by ICP dry etching or the like. Each of a source electrode **490** and a drain electrode **410** is formed of a Ti layer and an Al layer in an associated one of the openings, and then heat treatment is performed thereto in an N₂ atmosphere at 650° C. (Ex. 1007)

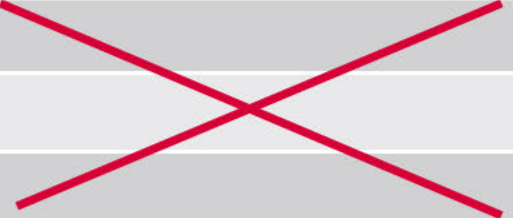
No Motivation to Combine Enhancement mode with Depletion Mode Prior Art

- Enhancement mode devices operate materially differently than depletion mode devices
 - Require different structures
 - Require different materials
 - Lead to different manufacturing techniques (epitaxial growth, fabrication processes)
- Hikita347 – Enhancement mode; Beach – Depletion mode
 - Due to different materials and purposes for materials – no expectation of success
 - Beach does not require gate materials below gate structure; instead has protective material
 - Layers serve different purposes

Hikita347's Fabrication Process Dissuades Inclusion of Beach

- Hikita347 gate metal and ohmic contacts are formed of different materials (Ni or Pd vs. Ti/Al)
- Beach electrodes are formed of same material – “gate-simultaneous”
- Incompatibility of materials and formation process
 - Further evidences difference in processes and materials between references
 - Further evidences Petitioner's hindsight bias in prior art combination

Undisputed: Hikita347, Beach, and Sheppard Combination does Not Teach “Gate - First”

Gate-First	Gate-Simultaneous	Gate-Last
		Hikita347
	Beach	
		Sheppard

Proposed combination does not teach “gate-first” process required by claims 1-4 of ’508 patent

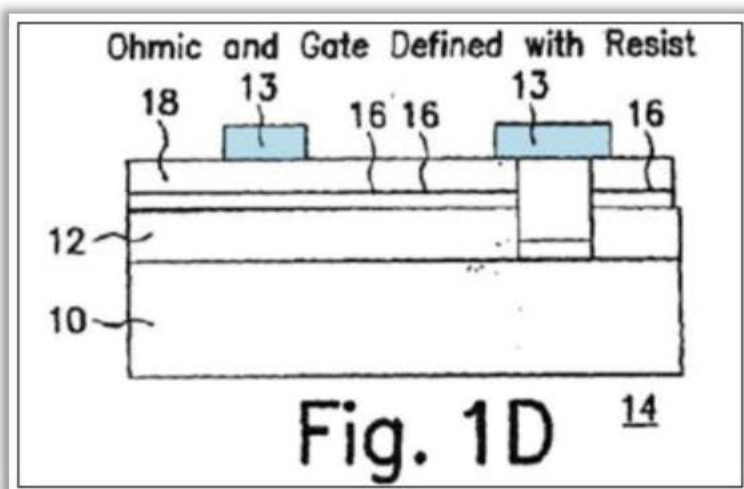
- No reference teaches patterning and etching a self-aligned gate structure before forming ohmic contacts
- Petitioner never proposes a method to modify the proposed combination to achieve a gate-first process
- Dr. Shealy opined against “gate-first” (Ex. 2002 at 85:19-86:8, 95:11-23)
- Dr. Schubert explained known detriments of proceeding in the manner of the ’508 patent (Ex. 2001 at ¶ 187)



DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

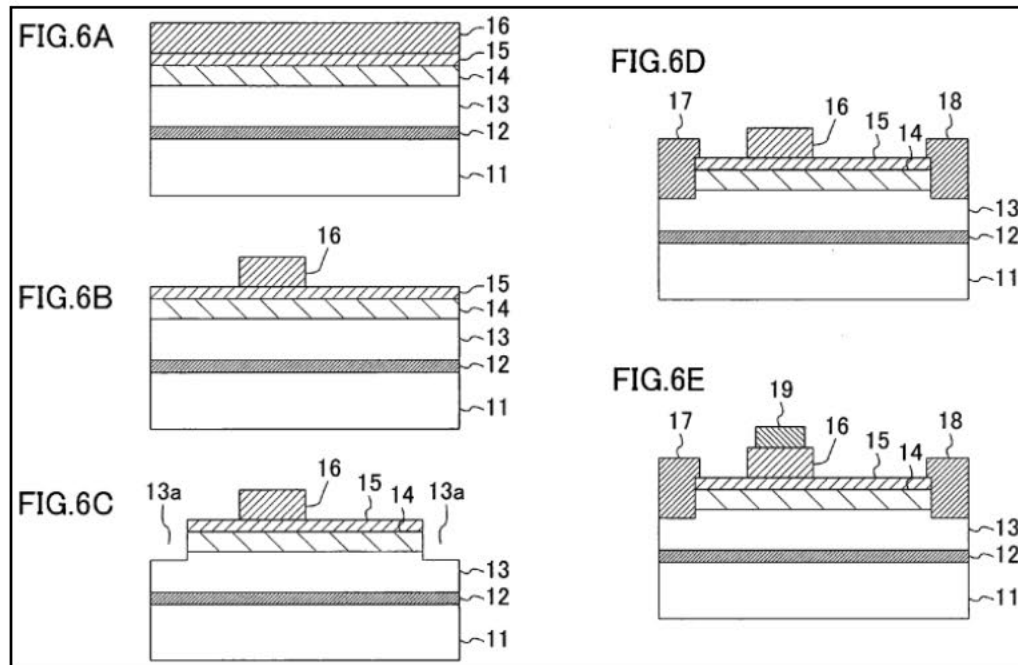
Prior Art Fails to Disclose Separate “*applying*” Gate Pattern and Metal Pattern

- Ground 2’s Hikita347, Beach, and Sheppard fail to disclose separate “applying” steps for the same reason as Ground 1
 - Petitioner concedes Hikita347 does not teach either [1e2], [4f2] (applying a gate photo resistant pattern) or [1g2], [4h2] (applying a metal photo resistant pattern) (Paper 1 at 56-58, 60-61)
 - Petitioner relies exclusively on Beach for teaching these steps (*Id.*)
- Beach describes a single applying step for a resist material.
- Deficient for Two Reasons:
 - Beach teaches a single process step – not two simultaneous process steps
 - Beach teaches depositing gate photo resist simultaneous – and not prior to – metal photo resist



[0047] Referring now to Figure 1D, resist material 13 is deposited in a pattern to permit the formation of a gate 15 and ohmic contact 17. After the deposition of photoresist layer 13, material 18 is removed, as by etching, except where protected by photoresist 13. The removal, or etching process, also eliminates protective layer 16 under patterned photoresist 13.

Ground 3 (Claim 5): Hikita023, Sheppard, and Beach



(Paper 17 at 34 (citing Ex. 1008))

Hikita023 Process

- “Gate-Last” enhancement mode GaN transistor
 - Source & Drain (17, 18) formed before gate electrode (19)
- Single photo-mask ohmic formation process (liftoff)

Hikita023 & Hikita347

- Hikita023 – Filed a year after Hikita347 (same inventors)
- Both enhancement mode devices (normally OFF)
- Only difference between references immaterial to issues in dispute

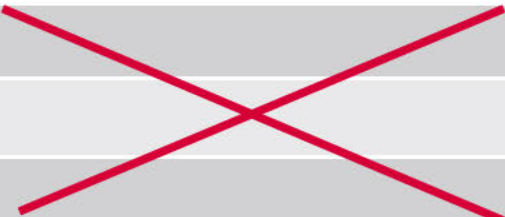
Petitioner’s Proposed combination of Hikita023, Sheppard, and Beach is materially the same as Grounds 1/2

Ground 3 is Similarly Deficient as Ground 2: No Motivation to Combine Gate-Last Process with Gate-Simultaneous Process

- No Motivation to Combine Gate-Last Process with Gate-Simultaneous Process
 - Petition inapplicably relies on motivations to combine relating to Yoshida and Beach – a different primary reference with a different process and different disclosures
 - Hikita023 is a “gate-last” process; no motivation to combine with expectation of success as Grounds 1 and 2
 - No motivation to combine Hikita023-Beach/Sheppard to achieve “gate-first” process
- No Motivation to Substitute Hikita023’s Ohmic formation process with Beach’s two-mask process
 - Hikita023 describes a one mask ohmic formation process, like Hikita047 and Yoshida
 - Same reasons a POSA would not combine Hikita347’s teachings with Beach’s teachings apply to Ground 3
- No Motivation to Combine Hikita023’s Enhancement Mode Device with Beach’s Depletion Mode Device
 - Hikita347 is enhancement mode; like Hikita023
 - Same reasons a POSA would not combine Hikita347’s teachings with Beach apply to Ground 3
- Hikita023’s Fabrication Process is Incompatible with Beach’s “Gate-Simultaneous” Process
 - Hikita023 describes different materials for gate electrodes and ohmic electrodes and are thus incompatible with Beach’s gate-simultaneous process – therefore a POSA would not seek to combine the references

Ground 3: Even if Combined – Fails to Render Obvious Claim 5

- Even if a POSA combined the teachings of Hikita023, Beach, and Sheppard – still not arrive at Claim 5 as a whole
 - A combination of Hikita023, Beach, and Sheppard fails to disclose or suggest “gate-first” process

Gate-First	Gate-Simultaneous	Gate-Last
		Hikita023
	Beach	
		Sheppard

- Hikita023, Beach, and Sheppard as proposed in the Petition fail to teach both [5f2] applying a gate photo resistant pattern and [5i2] applying a fourth photo resistant pattern
 - Petition only identifies Beach as disclosing both these elements
 - For same reasons as Grounds 1 and 2, Beach alone or in combination does not disclose or teach separate steps of applying resist material for gate and ohmic formation

Conclusion

- All we are left with are pieces of the puzzle -



Level of Ordinary Skill in Art

Patent Owner Proposal	Petitioner Proposal
Four-year degree in electrical engineering, physics, material science, or a closely related field, and three years professional work experience in the epitaxial growth, design, and fabrication of semiconductor electronic devices, including those of GaN (Paper 17 at 17)	Four-year degree in electrical engineering, chemical engineering, physics, or material science or a closely related field and at least two years of experience in semiconductor design or fabrication, including the processing of semiconductor materials, analysis of device operation, or the development of new device topologies (Paper 1 at 11)

Patent Owner's Expert Dr. Schubert: Differences in POSA's do not affect his opinion in this proceeding

(Paper 17 at 17 (citing Ex. 2001 at ¶ 81))

Dr. Schubert's Approval

In co-pending ITC trial, Petitioner did not object to Dr. Schubert being qualified as an expert for the subject matter of the 508 patent.

(Paper 20 at 32)

17 MR. PARADKAR: Your Honor, we offer
18 Dr. Schubert as a technical expert in the semiconductor
19 field and specifically in gallium nitride devices, their
20 methods of manufacture.

21 CHIEF JUDGE CHENEY: Is there any objection?

22 MR. LAVENUE: No objection.

23 MR. WINSTON: No objection, Your Honor.

24 CHIEF JUDGE CHENEY: Dr. Schubert will be
25 accepted as an expert in the semiconductor field and

1 specifically in gallium nitride devices and their methods
2 of manufacture.

(Ex. 2008 at 426:19-428:2)

Only a “Gate-First” Achieves BOTH “present invention[s]”

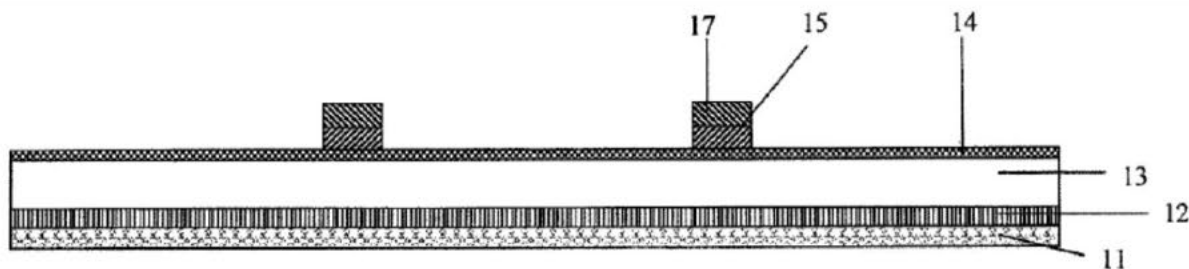


FIG. 3C

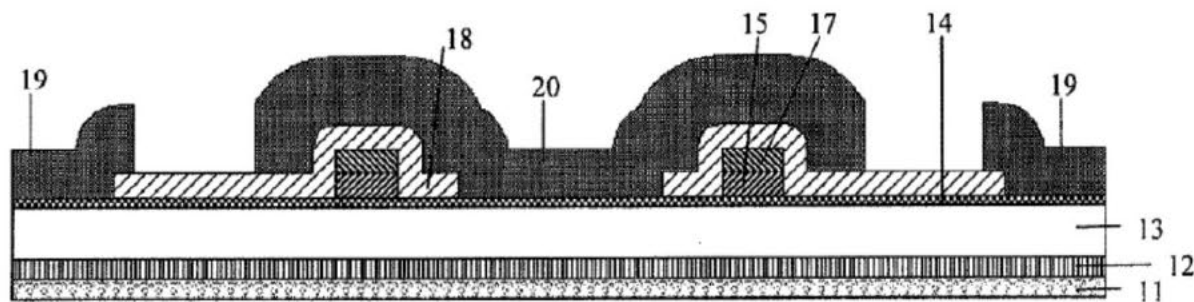


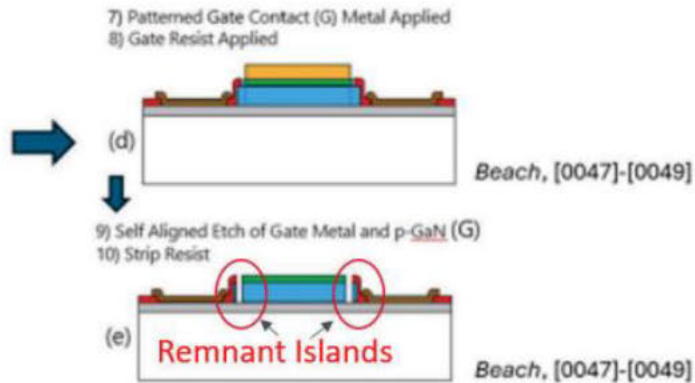
FIG. 3E

- Undisputed: Achieves self-aligned process
- Only process capable of simultaneous “pattern[ing] and etch[ing]” field plate at source potential with source and drain ohmic contact.
 - Field plate located **over** gate structure
 - Field plate included in all embodiments
 - Field plate cannot be deposited over gate structure without presence of formed gate structure (POR at 19 (citing Ex. 2001 58, 74-75, 83))
- Process improvement by forming field plate together with the source and drain contacts

18, drain ohmic contact 19, and source ohmic contact 20. The source metal 20 also serves as a field plate that extends over the gate and toward the drain contact. Layers 13, 14, and 15

(Paper 17 at 19 (citing Ex. 1001 at 3:21-23))

Hikita347/023, Beach, Sheppard New Sequences are Similarly Deficient



Reply, 27 (annotated)

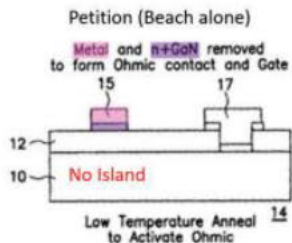
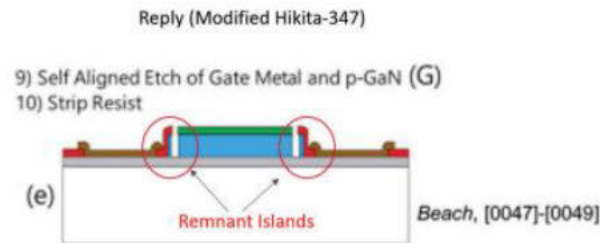


Fig. 1E



Limitation [1e4], [4f4] Comparison (annotated). Petition, 33⁸; Reply, 27

(Paper 20 at 29)

- New Sequences concerning Hikita347/023 are new and improper for same reasons as Ground 1
 - Like Ground 1 – No proof Grounds 2/3 teach limitations [1e4], [4f4], or [5f4] – “etching away the doped GaN layer, except a portion of the doped GaN layer beneath the gate contact”
 - POSA not motivated to modify Hikita347/023 based on Beach and Sheppard due to differences in references to arrive at newly described sequence (same reasons as Ground 1)
- Proposed ohmic contact formation is more complicated
- Motivations to Combine from Petition are not consistent with proposed combination (more complicated)
- Proposed combination solely based on hindsight combination of dissimilar references

Alleged Statement of Facts

- Confirms hindsight analysis by individually reciting claim limitations without evidentiary citations
- Board not required to admit into evidence. 37 CFR 42.23