

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INNOSCIENCE (ZHUHAI) TECHNOLOGY COMPANY, LTD.,
AND
INNOSCIENCE AMERICA, INC.,
Petitioner,

v.

EFFICIENT POWER CONVERSION CORPORATION,
Patent Owner.

Case IPR2023-01383
U.S. Patent 8,404,508

**PETITIONER'S BRIEF IN RESPONSE TO THE BOARD'S ORDER
REGARDING CONSTRUCTION OF CLAIM ELEMENT [1E4]**

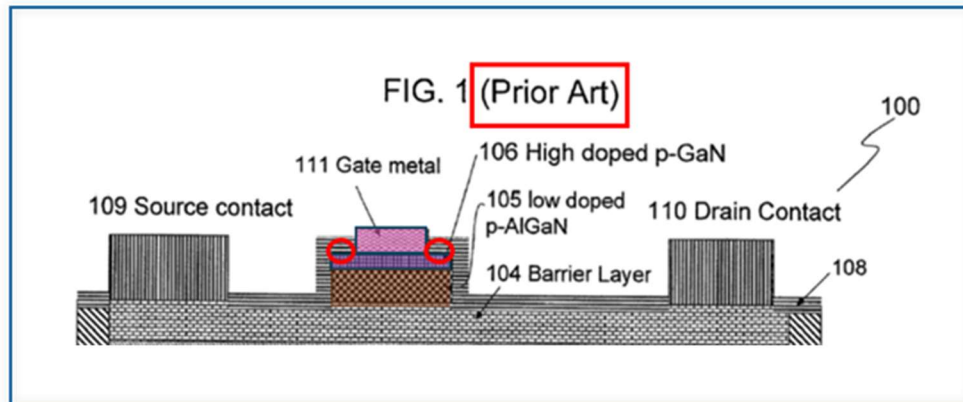
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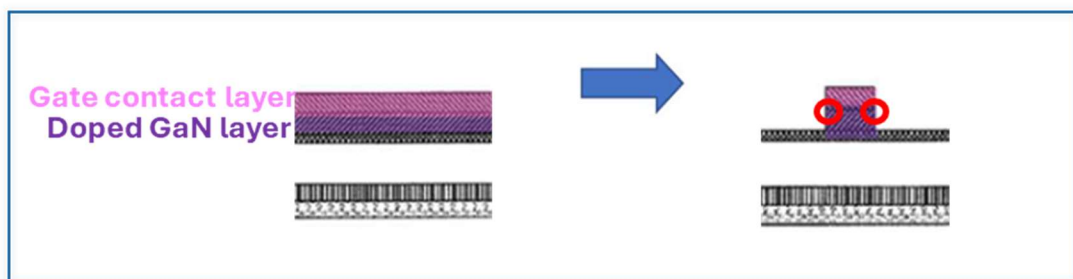
Pursuant to the Board's Order (Paper 34), Petitioner submits that, applying EPC's construction at the ITC litigation, of "etching away the doped GaN layer, except a portion of the doped GaN layer beneath the gate contact" (element [1e4]), the "remnant p-type GaN Islands" in the modified *Yoshida* process are fully consistent with a finding of unpatentability. A proper construction of element [1e4] requires etching the doped GaN layer and gate contact to form a self-aligned gate structure. The '508 patent never contemplates etching the doped GaN layer outside the region where the gate structure is formed, permitting "remnant p-type GaN Islands" outside the gate region (i.e., not connected to the gate).

I. Remnant P-Type GaN Islands Satisfy Element [1e4]

The alleged "present invention" of the '508 patent is the use of a single mask to etch both the doped GaN layer and the gate contact layer, such that the doped GaN layer and gate contact are "automatically self-aligned" to achieve a "[m]inimum gate length," avoiding the "wider gate length" of conventional processes. Ex. 1001, 2:5-16, 3:1-6, 4:6-11. Figure 1 of the '508 patent, admitted as prior art, shows that the doped GaN layer 106 (as well as the doped AlGaIn layer 105) under the gate contact layer are unetched in regions connected to and extending beyond the gate, resulting in the wider gate length. *Id.*, 1:53-2:6, Fig. 1.

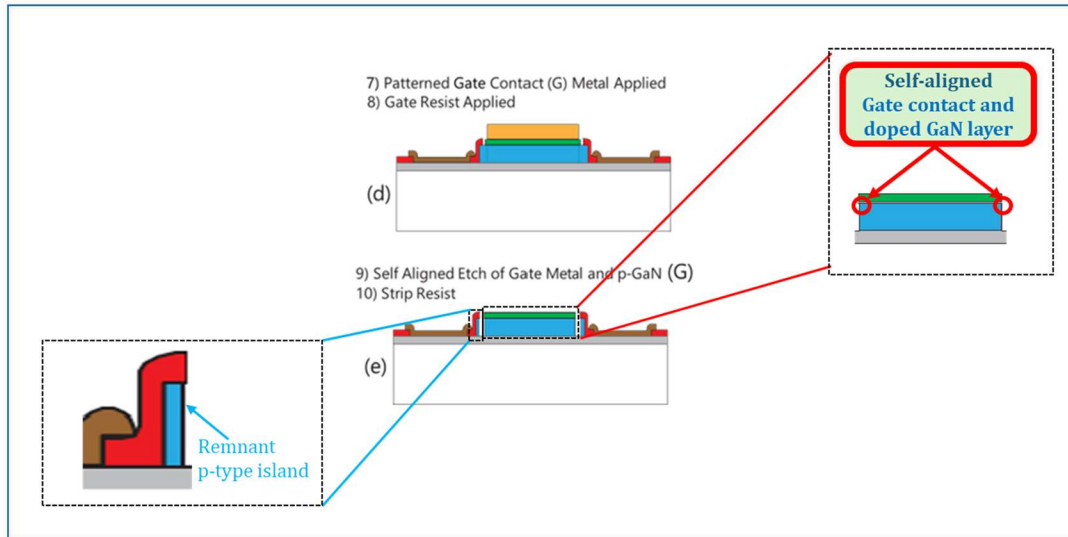


To minimize the gate length, the '508 patent's solution uses a single mask to etch both the gate contact and the doped GaN layer to produce a self-aligned gate and doped GaN structure, achieving a doped GaN layer precisely aligned to the gate contact layer, shown below. This self-alignment process is the alleged “present invention” and repeated in every embodiment of the '508 patent.



Ex. 1001, Figs. 3B, 3C (annotated); Ex. 1001, 3:1-6, 5:38-45, 5:52-58, 6:15-21, Figs. 2, 3C, 5C, 7C, 8, 11. *Techtronic Indus. Co. v. ITC*, 944 F.3d 901, 907 (Fed. Cir. 2019) (“[W]here ... specification describes ... invention as having [a] feature, that representation may disavow contrary embodiments.”) (quotation omitted).

The modified *Yoshida* process applies a single mask to etch the **gate contact layer** and the **doped GaN layer** under it, producing a self-aligned gate structure.



See Petitioner's Reply, 14. Thus, the modified *Yoshida* process, having remnant p-type GaN islands, satisfies any reasonable construction of claim element

[1e4]—etching for the doped GaN layer and gate contact to be self-aligned.

Element [1e4] requires using a self-aligned process to etch the gate contact and doped GaN layer—it does not require etching the doped GaN layer everywhere in the device, such as the p-type GaN islands separate from the gate region. The resultant remnant p-type GaN islands are separate from (and disjoint from) the gate region of the device, not affecting the gate length and self-alignment of the device.¹

¹ Additionally, and as explained in Petitioner's Reply, the modified *Yoshida* process could also be modified to have no remnant p-type GaN islands, by applying appropriate photoresist. See Reply, 6-7. EPC does not dispute that the remnant p-type GaN islands can be eliminated and that the modified *Yoshida* process without the remnant p-type GaN islands satisfies element [1e4]. Therefore,

II. Remnant P-Type GaN Islands of Modified *Yoshida* Process Meet EPC’s Construction at the ITC

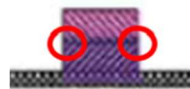
EPC argued in the ITC litigation, that the term “etching away the doped GaN layer, except a portion of the doped GaN layer beneath the gate contact,” means “etching away the doped GaN layer without etching beneath the gate contact”—and “[a]ll that is required is that the area under the gate contact not be etched.” Ex. 1039, 16-17. Applying EPC’s construction of the term here in this IPR, the modified *Yoshida* process, having the “remnant p-type GaN Islands,” meets element [1e4], because, as shown above, the p-type GaN layer is etched to align with the gate contact, and the portion of p-type GaN layer beneath the gate contact is not etched (with any remnant p-type GaN islands not under the gate contact being irrelevant).

In its Sur-reply, EPC appears to change its position and argue that element [1e4] requires all of p-type GaN layer outside the gate contact be etched, which is a change from EPC’s position at the ITC. Sur-reply, 16-17. EPC’s nose-of-wax construction should be rejected. *Amazon.com, Inc. v. Barnesandnoble.com, Inc.*, 239 F.3d 1343, 1351 (Fed. Cir. 2001) (“A patent may not, like a ‘nose of wax,’ be twisted one way to avoid anticipation and another to find infringement.”).

regardless of the dispute on the remnant p-type GaN islands, this alternative implementation of modified *Yoshida* process indisputably satisfies element [1e4].

III. A Proper Construction of Element [1e4] Requires a Self-Aligned Gate Contact and Doped GaN Layer, Which Is Also Consistent with Construction of the Limitation by Petitioner at the ITC

A proper construction of element [1e4] of the '508 patent requires etching for the doped GaN layer and gate contact to be self-aligned, as follows:



Thus, while the '508 patent makes clear how etching occurs under the gate, the '508 patent is silent on etching the doped GaN layer in regions separate/disjoint from below where the gate structure is formed, and claim element [1e4] does not specify that. This understanding is consistent with Petitioner's construction at the ITC, of "etching away the doped GaN layer in all regions extending outside the gate contact," because the dispute at the ITC was whether the claim allows the doped GaN layer at the gate region to be wider than the gate contact, improperly capturing the non-self-aligned prior art process. There was no issue at the ITC, whether the claim allows the presence of any doped GaN layer separate from the region where the gate structure is to be formed, like the "remnant p-type GaN Islands." The "remnant p-type GaN Islands" issue was not before the ITC.

Respectfully submitted,

Dated: January 13, 2025

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CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6(e), I certify that on January 13, 2025, a copy of **Petitioner's Brief in Response to the Board's Order Regarding Construction of Claim Element [1e4]** was served upon the below-listed counsel by electronic mail:

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