

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INNOSCIENCE (ZHUHAI) TECHNOLOGY COMPANY, LTD.,
AND
INNOSCIENCE AMERICA, INC.,
Petitioner,

v.

EFFICIENT POWER CONVERSION CORPORATION,
Patent Owner.

Case IPR2023-01383
U.S. Patent 8,404,508

PETITIONER'S NOTICE OF APPEAL

Pursuant to 35 U.S.C. §§ 141(c), 142, and 319 and 37 C.F.R. § 90.2(a), Petitioner Innoscience (Zhuhai) Technology Company, Ltd. and Innoscience America, Inc. (“Innoscience”) hereby provides notice of appeal to the United States Court of Appeals for the Federal Circuit from the Final Written Decision of the Patent Trial and Appeal Board (“Board”) entered on March 18, 2025 (Paper No. 39) (“Final Written Decision”) and from all underlying orders, decisions, rulings, and opinions relating to the *inter partes* review of U.S. Patent No. 8,404,508 (“’508 patent”) in Case No. IPR2023-01383. This Notice is timely under 37 C.F.R. § 90.3(a)(1), having been filed no later than sixty-three (63) days after issuance of the Final Written Decision.

In accordance with 37 C.F.R. § 90.2(a)(3)(ii), Petitioner states that the issues on appeal include, but are not limited to:

- the Board’s determination that claims 1-3 of the ’508 patent were not shown to be unpatentable under 35 U.S.C. § 103 as obvious over the combination of Yoshida, Beach, Sheppard;
- the Board’s determination that that claims 1-4 of the ’508 patent were not shown to be unpatentable under 35 U.S.C. § 103 as obvious over the combination of Hikita-347, Beach, Sheppard;

- the Board's determination that that claim 5 of the '508 patent was not shown to be unpatentable under 35 U.S.C. § 103 as obvious over the combination of Hikita-023, Beach, Sheppard;
- the Board's factual findings, conclusions of law, or other determinations supporting or relating to the foregoing issues; and
- all other issues decided adversely to Petitioner in any orders, decisions, rulings, or opinions underlying or supporting the Final Written Decision.

A copy of the Final Written Decision is attached to this Notice.

Pursuant to 35 U.S.C. § 142 and 37 C.F.R. § 90.2(a)(1), this Notice is being filed with the Director of the United States Patent and Trademark Office, and a copy of this Notice is being concurrently filed with the Patent Trial and Appeal Board. In addition, a copy of this Notice and the required docketing fees are being filed with the Clerk's Office for the United States Court of Appeals for the Federal Circuit via CM/ECF in accordance with 37 C.F.R. § 90.2(a)(2), Federal Rule of Appellate Procedure 15, and Federal Circuit Rule 15.

Date: May 20, 2025

Respectfully submitted,

By: /Lionel M. Lavenue/
Lionel M. Lavenue, Reg. No. 46,859
Lead Counsel

CERTIFICATE OF SERVICE AND FILING

I hereby certify that on May 20, 2025, in addition to being filed and served electronically through the Patent Trial and Appeal Board's P-TACTS System, this **PETITIONER'S NOTICE OF APPEAL** was filed with and served on the Director of the United States Patent and Trademark Office via e-mail at the following:

Office of the General Counsel
U.S. Patent and Trademark Office
efileSO@uspto.gov

I also hereby certify that on May 20, 2025, this **PETITIONER'S NOTICE OF APPEAL** and the requisite docketing fees were filed with the Clerk's Office of the United States Court of Appeals for the Federal Circuit via CM/ECF.

I further hereby certify that on May 20, 2025, this **PETITIONER'S NOTICE OF APPEAL** was served by electronic mail on the following counsel for Patent Owner:

Walter D. Davis, Jr.
walter.davis@blankrome.com

Dipu Doshi
dipu.doshi@blankrome.com

Mark Mashack
mark.mashack@blankrome.com

Stephen Soffen
stephen.soffen@blankrome.com

Cory R. Edwards
cory.edwards@blankrome.com

Ameya V. Paradkar
arun.paradkar@blankrome.com

Jonathan England
jonathan.england@blankrome.com

EPCC-Inno-IPRS@blankrome.com

Dated: May 20, 2025

By: /Daniel E. Doku/
Daniel E. Doku
Senior Litigation Legal Assistant
FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, LLP

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INNOSCIENCE (ZHUHAI) TECHNOLOGY COMPANY, LTD.,
AND
INNOSCIENCE AMERICA, INC.,
Petitioner,

v.

EFFICIENT POWER CONVERSION CORPORATION,
Patent Owner.

IPR2023-01383
Patent 8,404,508 B2

Before JON B. TORNQUIST, JEFFREY W. ABRAHAM, and
KIMBERLY McGRAW, *Administrative Patent Judges*.

McGRAW, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining No Challenged Claims Unpatentable
35 U.S.C. § 318(a)
Dismissing as Moot Petitioner's Motion to Exclude Evidence
37 C.F.R. § 42.64

I. INTRODUCTION

We instituted this *inter partes* review pursuant to 35 U.S.C. § 314 to review claims 1–5 of U.S. Patent No. 8,404,508 B2 (Ex. 1004, “the ’508 Patent”) owned by Efficient Power Conversion Corporation (“Patent Owner” or “EPC”). We have jurisdiction under 35 U.S.C. § 6. This Final Written Decision is entered pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73. For the reasons discussed below, Innoscience (Zhuhai) Technology Company, Ltd. and Innoscience America, Inc., (collectively “Petitioner” or “Innoscience”) have not shown by a preponderance of the evidence that claims 1–5 are unpatentable.

A. Procedural History

Petitioner filed a petition for an *inter partes* review (Paper 1 (“Pet.”)) challenging claims 1–5 of U.S. Patent No. 8,404,508 B2 (Ex. 1001 (“the ’508 Patent”)). Efficient Power Conversion Corporation (“Patent Owner”) filed a Preliminary Response. Paper 7 (“Prelim. Resp.”). We instituted this *inter partes* review of all challenged claims based on all grounds asserted in the Petition. Paper 11 (“Inst. Dec.”).

Patent Owner then filed a Patent Owner Response (Paper 17, “Resp.”), to which Petitioner filed a Reply (Paper 18, “Pet. Reply”), and Patent Owner filed a Sur-reply. Paper 20 (“PO Sur-reply”).

An oral hearing was held on December 18, 2024. After the hearing, the Board requested additional briefing regarding the parties’ construction of the term “etching away the doped GaN layer, except a portion of the doped GaN layer beneath the gate contact” as recited in claim 1, including whether there can be “a region of the doped GaN layer outside the gate contact that is entirely unetched.” Paper 34 (“Order”). In response, Petitioner and Patent

Owner each filed an opening brief (Paper 35 (Petitioner's opening brief; Paper 36 (Patent Owner's opening brief)) and a responsive brief (Paper 38 (Petitioner's responsive brief); Paper 37 (Patent Owner's responsive brief)).

Additionally, Petitioner filed a Motion to Exclude Exhibit 2008 (Paper 25, "Pet. Mot. Excl."), to which Patent Owner filed an Opposition (Paper 27, "PO Opp."), and Petitioner filed a Reply (Paper 31, "Pet. Reply Mot. Excl.").

B. Related Proceedings

The parties identify two matters involving the '508 patent: *Efficient Power Conversion Corporation v. Innoscience (Zhuhai) Technology Co., Ltd.*, 2:23-cv-04026-AB-AS (C.D. Cal. May 24, 2023) and *Certain Semiconductor Devices, and Methods of Manufacturing Same and Products Containing the Same*, Inv. No. 337-TA-1366 (USITC May 26, 2023). Pet. 92; Paper 5 (Patent Owner's Mandatory Notices), 2.

C. Real Parties-In-Interest

Petition identifies the real parties-in-interest as Innoscience (Zhuhai) Technology Company, Ltd., Innoscience America, Inc., and InnoScience (Suzhou) Holding Technology Company, Ltd. Pet. 92; Paper 16.

Patent Owner identifies itself as the real party-in-interest. Paper 5, 1–2.

D. The '508 Patent

The '508 patent, titled "Enhancement Mode GaN HEMT Device and Method for Fabricating the Same," which issued March 26, 2013 and claims priority to a provisional application filed on April 8, 2009, relates to the field of enhancement mode gallium nitride (GaN) high electron mobility transistor (HEMT) devices and methods of forming such devices. *See*

Ex. 1001, codes (45), (54), (57), 2:14–18. The '508 patent explains that “GaN semiconductor devices are increasingly desirable because of their ability to switch at high frequency, to carry large current, and to support high voltages.” Ex. 1001, 1:22–24.

Figure 2 of the '508 patent, with color annotations and the labels on the right side provided by Petitioner, is reproduced below. Pet. 8; Ex. 1001, Fig. 2.

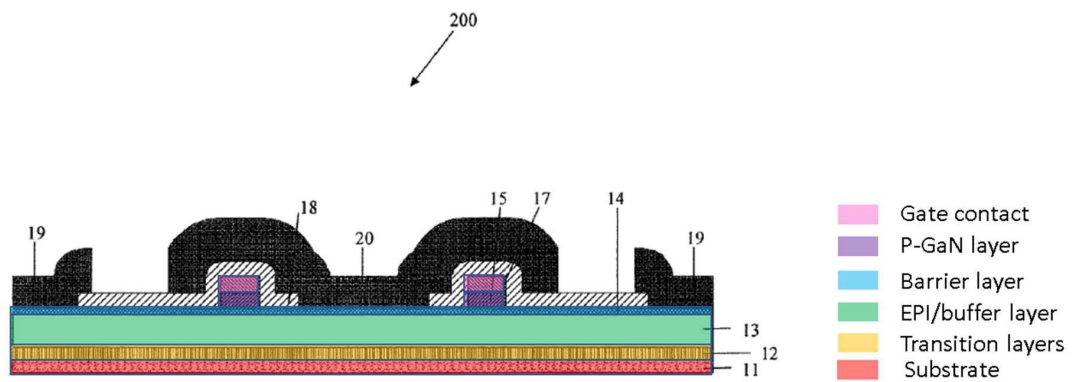


FIG. 2

Figure 2 above, with Petitioner’s color annotations added, illustrates a first embodiment of an enhancement mode GaN HEMT device having silicon substrate 11, transition layers 12, undoped GaN buffer material 13, AlGaN barrier material 14, p-type GaN gate layer 15 (purple), gate metal (pink), dielectric material 18, drain ohmic contact 19, and source ohmic contact 20. Ex. 1001, 2:25–27, 3:10–25.

The process for forming the device according to the first embodiment of the '508 patent is schematically illustrated in Figures 3B–3E, shown below, with Petitioner’s color annotations added to Figures 3B and 3C. Ex. 1001, 2:28–30; Pet. 9–10.

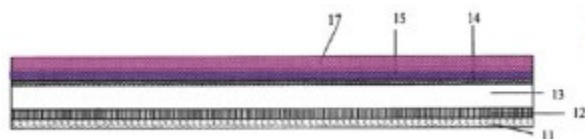


FIG. 3B

Figure 3B above shows gate metal 17 (pink) deposited on an EPI structure having p-type GaN gate layer 15 (purple). Ex. 1001, 3:26–29, 3:39–40.

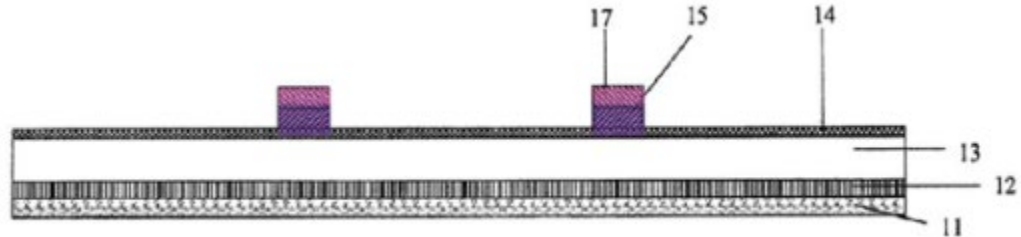


FIG. 3C

Figure 3C above shows the structure resulting from a single photo mask used to pattern and etch gate metal 17 (pink) and p-type GaN gate layer 15 (purple). Ex. 1001, 3:45–47.

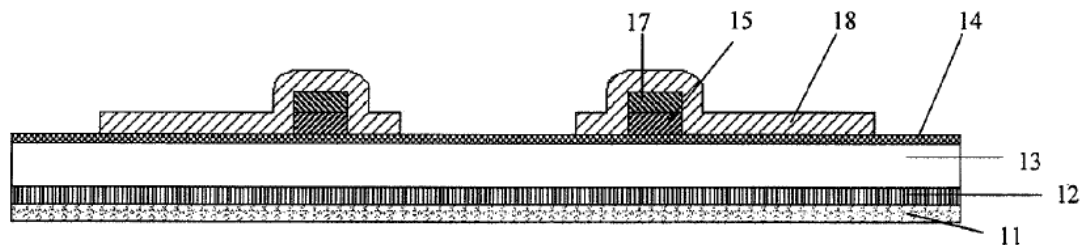


FIG. 3D

The '508 patent states that the structure shown in Figure 3D above is formed by depositing dielectric material 18 and then, after deposition of the material, a contact photo mask is used to pattern and etch the dielectric material 18, followed by a photoresist strip. Ex. 1001, 3:57–61.

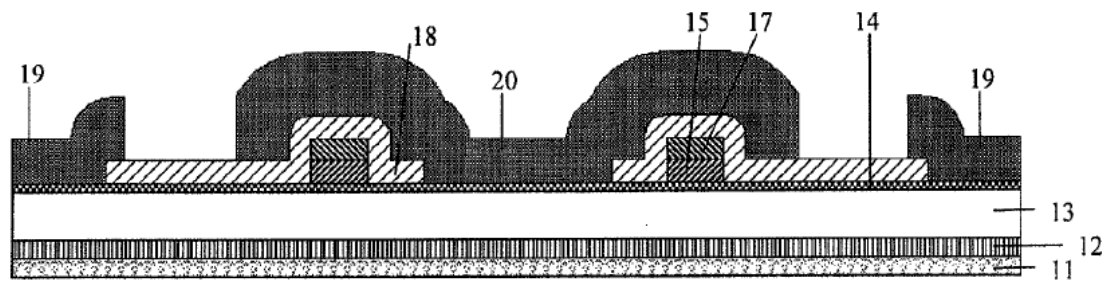


FIG. 3E

The '508 patent states, referring to Figure 3E above, ohmic contact metal is deposited, after which, a metal mask is used to pattern and etch the ohmic contact metal, resulting in drain ohmic contact 19 and source ohmic contact 20. Ex. 1001, 3:62–67. Rapid thermal anneal is performed to form ohmic contacts to AlGaIn/GaN 2DEG. *Id.* at 3:67–4:2.

E. Illustrative Claim

Claims 1, 4, and 5 are the challenged independent claims and are reproduced below with bracketed annotations corresponding to the annotations in the Petition. Pet., Claim Appendix.

Claim 1: [1pre] A method of forming an enhancement mode GaN transistor, the method comprising:

- [1a] nucleating and growing transition layers on a substrate;
- [1b] growing an III Nitride EPI layer over the transistor layers;
- [1c] growing an III Nitride barrier layer over the EPI layer;
- [1d] growing a GaN layer with acceptor type dopants over the barrier layer;
- [1e]:
 - [1e1] *depositing a gate contact layer on the doped GaN layer;*
 - [1e2] *applying a gate photo resistant pattern;*
 - [1e3] *etching away the gate contact layer outside the gate region;*

[1e4] *etching away the doped GaN layer, except a portion of the doped GaN layer beneath the gate contact;*

[1e5] removing the gate photo resistant pattern;

[1f]:

[1f1] depositing a dielectric layer;

[1f2] applying a contact photo resistant pattern;

[1f3] etching the dielectric layer to open the drain and source contact area;

[1f4] removing the contact photo resistant pattern;

[1g]:

[1g1] depositing an Ohmic contact metal;

[1g2] applying a metal photo resistant pattern;

[1g3] etching the Ohmic contact metal;

[1g4] removing the metal photo resistant pattern; and

[1g5] performing rapid thermal annealing to form Ohmic drain and source contacts.

Ex. 1001, 6:59–7:15 (labels and formatting added to correspond with Petitioner’s designation of claim limitations (*see, e.g.,* Pet. 25–35; Claim Appendix)) (emphasis added).

Claim 4: [4pre] A method of forming an enhancement mode GaN transistor, the method comprising:

[4a] nucleating and growing transition layers on a substrate;

[4b] growing an InAlGaNEPI layer over the transistor layers;

[4c] growing an InAlGaN barrier layer over the InAlGaNEPI layer;

[4d] growing an InAlGaN layer with acceptor type dopants over the InAlGaN barrier layer;

[4e] growing a GaN layer with acceptor type dopants over the doped InAlGaN layer;

[4f]:

- [4f1] *depositing a gate contact layer on the doped GaN layer*
- [4f2] *applying a gate photo resistant pattern;*
- [4f3] *etching away the gate contact layer outside the gate region;*
- [4f4] *etching away the doped GaN layer and the doped InAlGaN layer, except for portions of the doped GaN layer and the doped InAlGaN layer beneath gate contact;*
- [4f5] removing the gate photo resistant pattern;

[4g]:

- [4g1] depositing a dielectric layer;
- [4g2] applying a contact photo resistant pattern;
- [4g3] etching the dielectric layer to open the drain and source contact area;
- [4g4] removing the contact photo resistant pattern;

[4h]:

- [4h1] depositing an Ohmic contact metal;
- [4h2] *applying a metal photo resistant pattern;*
- [4h3] etching the Ohmic contact metal;
- [4h4] removing the metal photo resistant pattern; and
- [4h5] performing rapid thermal annealing to form Ohmic drain and source contacts.

Ex. 1001, 7:21–8:7 (labels and formatting added to correspond with Petitioner’s designation of claim limitations (*see, e.g.,* Pet. 66–74; Claim Appendix)) (emphasis added).

Claim 5: [5pre] A method of forming an enhancement mode GaN transistor, the method comprising:

- [5a] nucleating and growing transition layers on a substrate;
- [5b] growing an InAlGaNEPI layer over the transistor layers;
- [5c] growing an AlGaN barrier layer over the InAlGaNEPI layer;

- [5d] growing an AlGa_N layer with acceptor type dopants over the AlGa_N barrier layer;
- [5e] growing a Ga_N layer with acceptor type dopants over the doped AlGa_N layer;
- [5f]:
 - [5f1] *depositing a gate contact layer on the doped Ga_N layer*
 - [5f2] *applying a gate photo resistant pattern;*
 - [5f3] *etching away the gate contact layer outside the gate region;*
 - [5f4] *etching away the doped Ga_N layer, except for portions of the doped Ga_N layer and the doped AlGa_N layer beneath gate contact;*
 - [5f5] removing the gate photo resistant pattern;
- [5g]:
 - [5g1] applying another photo resistant pattern;
 - [5g2] etching the doped AlGa_N layer such that the doped AlGa_N extends outside the gate region towards the drain;
 - [5g3] removing the photo resistant pattern;
- [5h]:
 - [5h1] depositing a dielectric layer;
 - [5h2] applying a contact photo resistant pattern;
 - [5h3] etching the dielectric layer to open the drain and source contact area;
 - [5h4] removing the contact photo resistant pattern;
- [5i]:
 - [5i1] depositing an Ohmic contact metal;
 - [5i2] applying a fourth photo resistant pattern;
 - [5i3] etching the Ohmic contact metal
 - [5i4] removing the fourth photo resistant pattern; and
 - [5i5] performing rapid thermal annealing to form Ohmic drain and source contacts.

Ex. 1001, 8:8–39 (labels and formatting added to correspond with Petitioner’s designation of claim limitations (*see, e.g.*, Pet. 78–89; Claim Appendix)) (emphasis added).

F. The Asserted Grounds of Unpatentability

Petitioner contends claims 1–5 of the ’508 patent are unpatentable on the following grounds. Pet. 11.

Claim(s) Challenged	35 U.S.C. §¹	Reference(s)/Basis
1–3	103	Yoshida, ² Beach, ³ Sheppard ⁴
1–4	103	Hikita-347, ⁵ Beach, Sheppard
5	103	Hikita-023 ⁶ , Beach, Sheppard

In support of its unpatentability arguments, Petitioner relies on the declaration of James Richard Shealy, Ph.D. (Ex. 1003, “Shealy Dec.”) and a supplemental declaration (Ex. 1041, “Second Shealy Dec.”). Patent Owner relies on the declaration of E. Fred Schubert, Ph.D. (Ex. 2001, “Schubert Dec.”).

¹ The Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112–29, 125 Stat. 284 (Sept. 16, 2011), includes revisions to Section 103 that became effective on March 16, 2013. Because the challenged claims issued from an application filed before March 16, 2013, we apply the pre-AIA law to the challenges. *See* Ex. 1001, code (30).

² JP H11-261053, published Sept. 24, 1999 (Ex. 1004, pp. 8–11 (original language), pp. 1–7 (certified English translation), p. 12 (certification) “Yoshida”)). All references are to the English translation portion of Ex. 1004.

³ US 2007/0057624, published June 23, 2005 (Ex. 1005, “Beach”).

⁴ US 7,238,560, issued July 3, 2007 (Ex. 1006, “Sheppard”).

⁵ US Pub. App. No. 2006/0273347, published Dec. 7, 2006 (Ex. 1007, “Hikita-347”).

⁶ US Pub. App. No. 2008/0079023, published Apr. 3, 2008 (Ex. 1008, “Hikita-023”).

II. DISCUSSION

A. Principles of Law

To prevail in challenging Patent Owner's claims, Petitioner has the burden of demonstrating by a preponderance of the evidence that the claims are unpatentable. 35 U.S.C. § 316(e); 37 C.F.R. § 42.1(d). That burden never shifts to the Patent Owner. *Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015). The petition must identify with particularity the evidence that supports the grounds for the challenge to each claim. 35 U.S.C. § 312(a)(3).”)).

A claim is unpatentable as obvious under § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) when in evidence,⁷ objective indicia of non-obviousness (i.e., secondary considerations). *Graham*, 383 U.S. at 17–18. Additionally, a “patent composed of several elements is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art.” *See KSR*, 550 U.S. at 418. Rather, “it can be important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements in the way the

⁷ Patent Owner does not rely on any objective indicia of non-obviousness in its arguments.

claimed new invention does.” *Id.* “To satisfy its burden of proving obviousness, a petitioner cannot employ mere conclusory statements. The petitioner must instead articulate specific reasoning, based on evidence of record, to support the legal conclusion of obviousness.” *In re Magnum Oil Tools Int’l, Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016).

We analyze Petitioner’s challenges according to the above-stated principles.

B. Claim Construction

In an *inter partes* review, we interpret a claim “using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. [§] 282(b).” 37 C.F.R. § 42.100(b). Under this standard, we construe the claim “in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.” *Id.*

“[T]he ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention” and “after reading the entire patent” and its prosecution history. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313, 1321 (Fed. Cir. 2005) (en banc).

Prior to institution, neither party provided express claim constructions for any claim terms. *See* Pet. 10 (stating no claim construction required); Prelim. Resp. 7–8. As noted in our Decision on Institution, it was apparent that the parties disputed whether the proper construction of the challenged claims required that the gate structure be formed before the source and drain contacts. Inst. Dec. 12–15. We provided our preliminary construction and invited the parties to further address this issue at trial if they so choose. Inst.

Dec. 12, 15 (providing a preliminary construction that “the claims require that the dielectric layer steps of [1f] must occur before the ohmic contact steps of [1g] but that the claims do not require that the gate structure be formed before the source and drain contacts”).

After institution, Patent Owner disputes our construction and argues that the claims “require[] a ‘gate-first’ process to achieve the advantages of the ‘present invention,’ and therefore the gate *must* be formed before the ohmic contacts.” Resp. 17. Petitioner replies that neither the Specification nor the claims require any particular sequence for forming the gate and ohmic contacts and that, contrary to Patent Owner’s assertions, the claims “cover non-gate-first processes,” including a “‘D (dielectric), O (ohmic contact), G (gate)’ process” as well as “an ‘O (ohmic contact), G (gate), D (dielectric)’ process.” Pet. Reply, 4–12.

During the proceeding, the parties also dispute the proper construction of “etching away the doped GaN layer, except a portion of the doped GaN layer beneath the gate contact” as recited in step [1e4] and provided briefing on this issue. Papers 35, 36, 37, 38.

Because, as explained below, our determination rests upon Petitioner’s failure to show a sufficient reason to modify the asserted art, which is not dependent upon any particular claim construction, we need not, and do not, address these claim construction issues. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (citing *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)) (holding that only claim terms in controversy need to be construed, and only to the extent necessary to resolve the controversy).

C. Level of Ordinary Skill in the Art

We consider the grounds of unpatentability in view of the understanding of a person of ordinary skill in the art (sometimes abbreviated herein as “POSITA”). *Graham*, , 383 U.S. at 17–18. Petitioner argued that a person of ordinary skill in the art would have had a “at least a four-year degree in electrical engineering, chemical engineering, physics, or material science or a closely related field and at least two years of experience in semiconductor device design or fabrication, including the processing of semiconductor materials, analysis of device operation, or the development of new device topologies. Additional education could substitute for professional experience and vice versa.” Pet. 11 (citing Ex 1003 ¶ 69). Patent Owner did not dispute this proposed definition prior to institution. *See generally* Prelim. Resp. In our Decision on Institution, we adopted Petitioner’s proposal.

After institution, Patent Owner asserted a slightly different definition of a POSITA, namely someone who “would have possessed at least a four-year degree in electrical engineering, physics, material science, or a closely related field, and three years of professional work experience in the epitaxial growth, design, and fabrication of semiconductor electronic devices, including those of GaN.” Resp. 17. Relevant graduate education could substitute for the professional work experience. *Id.*

Upon review of the full record, we see no reason to modify, and we thus maintain, the definition of a POSITA applied in our Decision on Institution. We also determine that our decision would be the same under either of the parties’ proposed definitions.

Petitioner also asserts that Patent Owner's expert, Dr. Schubert, does not meet Patent Owner's own definition of a POSITA because he does not have three years of "professional work experience in the epitaxial growth of semiconductor devices." Reply 33–34 (citing Resp. 17; Ex. 2001, App'x. A).

We disagree. First, as noted above, we adopt Petitioner's, not Patent Owner's, proposed definition of a POSITA. Petitioner does not assert that Dr. Schubert fails to meet *Petitioner's* definition of a POSITA. Thus, for at least this reason, we disagree with Petitioner's argument that Dr. Schubert is not a POSITA.

Second, even if we were to apply Patent Owner's definition, Dr. Schubert still has at least the skill of one of ordinary skill in the art. Under Patent Owner's definition, relevant graduate education could substitute for the professional work experience. *Id.* Dr. Schubert has earned the U.S. equivalents of a bachelor's degree, a Master of Science degree, and a Ph.D. in Electrical Engineering from the University of Stuttgart, Germany. Ex. 2001 ¶¶ 6, 129. Petitioner does not make any argument that Dr. Schubert's graduate education is not a sufficient substitute for any alleged lack of "professional work experience in the epitaxial growth of semiconductor devices." See Reply 33–34 (asserting that Dr. Schubert lacks sufficient "professional work experience" but making no argument that his graduate education is not a sufficient substitute); Ex. 2001, App'x A. Thus, for at least this reason, we find Dr. Schubert qualifies as a POSITA under Patent Owner's definition.

Petitioner additionally argues that we should give Dr. Schubert's testimony little weight because he lacks "practical experience with a GaN

transistor.” *See* Reply 4 (stating Dr. Schubert’s argument that “the non-gate-first processes would be non-functional” should be given little weight because he “does not have any practical experience with a GaN transistor”); *see also* Reply 33 (stating the entirety of Dr. Schubert’s testimony should be given little weight because he has “no practical experience with GaN transistors” and Dr. Schubert’s publications “are not in the context of forming a GaN transistor of the type in the ’508 patent”).

We disagree with Petitioner’s argument because it fails to address Dr. Schubert’s academic and other experience with GaN transistors. Dr. Schubert is currently a tenured full professor in the Department of Electrical Computer, and Systems Engineering at Rensselaer Polytechnic Institute and was previously a tenured full professor in the Department of Electrical and Computer Engineering at Boston University. Ex. 2001, 129. Additionally, Dr. Schubert was the director of Boston University’s Semiconductor Devices Research Laboratory. Ex. 2001, 129. Dr. Schubert persuasively explains that his general expertise is in the field of electrical engineering and applied physics, including semiconductors, processing, and devices and his specific expertise is in the field of semiconductor materials (such as GaN), semiconductor devices, semiconductor integrated circuits, ohmic contacts, Schottky contacts, HEMTs, and optoelectronic devices such as light-emitting diodes (LEDs). Ex. 2001 ¶ 11, App’x A pp.129–137. His experience includes “the design, growth, fabrication, and testing of semiconductor devices as well as the employment of these devices in a variety of applications” and he is “familiar with both the design of such transistors [HEMTs] and the manufacturing processes used for FETs. Ex. 2001 ¶ 11, App’x A, pp. 129–137. He is an author or co-author of numerous

text books and articles, and co-inventor of numerous patents, including those dealing with HEMT transistors and GaN devices. Ex. 2001 ¶ 13, App’x A, pp. 129–137. Petitioner fails to present any persuasive argument or evidence that Dr. Schubert’s extensive education and experience regarding GaN transistors is insufficient or lacking such that his testimony should be given little weight.

Finally, we disagree with Petitioner’s additional argument that that its expert’s testimony (Dr. Shealy) should be given more weight than Patent Owner’s expert’s testimony (Dr. Schubert) because “[u]nlike Dr. Schubert, Dr. Shealy is one of the pioneer scientists in the field of GaN transistors.” Reply 34 (stating that Dr. Shealy’s research lab built the first GaN HEMT device on silicon in 1999 and citing Ex. 2002, 87:19–23⁸). Obviousness is determined through the lens of a “person of *ordinary skill* in the art,” not through the lens of a person with extraordinary skill or a pioneer in the field. Given Dr. Schubert’s extensive relevant education and experience, Petitioner does not persuasively explain why Dr. Shealy’s testimony on any specific topic, or his testimony in general, should be given more weight than Dr. Schubert’s.

D. Statement of Disputed Facts

Pursuant to 37 C.F.R. § 42.22(c) a petition “may include a statement of material facts.” “Each material fact preferably shall be set forth as a separately numbered sentence with specific citations to the portions of the record that support that fact.” *Id.*

⁸ Petitioner cites to the page numbers of the exhibit provided by the court reporter, not to the numbered pages of the exhibit on the lower most left side corner of the document. For consistency, the panel does the same.

Petitioner lists three statements regarding the “state of GaN transistor at the time of the ’508 patent.” Pet. 11–13. Fact number 3 appears to separately list each step recited in claim 1 as being known before the earliest possible priority date of the ’508 patent. Pet. 12–13. Petitioner does not, however, provide specific citations to the portions of the record that support these statements of facts. Pet. 12–13.

Patent Owner contends Petitioner’s statement of material facts “is materially deficient and should be ignored” because “Petitioner failed to include any citations to the record supporting any of its alleged facts.” PO Resp. 26.

Petitioner’s failure to provide citations supporting its statements of material fact is highly problematic. It essentially shifts the burden of proving the facts are incorrect to Patent Owner, without Petitioner having to provide citations to support its assertions. We need not determine whether such an omission requires ignoring the statements of material fact in this case, however, because the recited material facts are either clearly supported by the evidence of record or not necessary to render a decision in this case. We note that even if each step recited in statement of fact 3 were known, obviousness cannot be shown merely by showing that each individual step was known in the prior art. *See KSR*, 550 U.S. at 418.

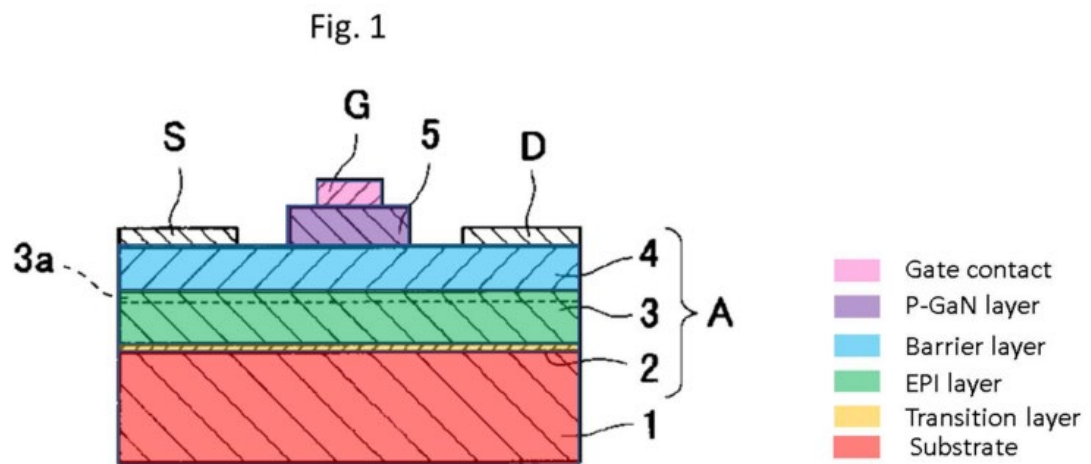
E. Overview of the Prior Art

1. Yoshida (Ex. 1004)

Yoshida is a Japanese Patent Publication titled “High Mobility Transistor” that published September 24, 1999. Ex. 1004, code (11), (43), (54). Yoshida states that its invention is directed to an HEMT comprising a GaN compound semiconductor that can operate under the application of

high voltages and at higher speeds. Ex. 1004 ¶¶ 1, 8. Both parties agree that the method disclosed in Yoshida forms the gate last, that is after the dielectric layer is deposited and the ohmic contacts are formed. *See* Resp. 42; Reply 14 (citing Ex. 1041 ¶ 32).

Yoshida depicts the basic structure of its claimed invention in Figure 1, reproduced below.



Yoshida, Fig. 1.

Figure 1 of Yoshida, with Petitioner’s color annotations added, shows a cross-sectional view of a transistor having a stacked structure comprising buffer layer 2, i-type semiconductor layer 3, and n-type semiconductor layer 4 formed on semi-insulating substrate 1. Ex. 1004 ¶ 10, 25. Figure 1 also shows gate electrode G on p-type semiconductor layer 5⁹, as well as source electrode S and drain electrode D, all formed on n-type semiconductor layer 4. Ex. 1004 ¶ 10, 25.

Yoshida discloses methods for fabricating the structure shown in Figure 1. Ex. 1004 ¶¶ 19–23. In particular, Yoshida discloses the deposition of GaN buffer layer 2 (yellow) on semi-insulating substrate 1

⁹ Yoshida’s identification of the p-type GaN layer as element “6” instead of element “5” in paragraphs 10 and 21 appears to be a typographical error. *Compare* Ex. 1004 ¶¶ 10, 21 with Ex. 1004 ¶ 25, Figure 1.

(red), followed by deposition of i-type GaN layer 3 (green), n-type AlGaIn layer 4 (blue), and p-type GaN layer 5 (purple). *Id.* ¶¶ 10, 20–21, 25.

A dry etching process is then used “to etch away p-type GaN layer except where the gate electrode [is] to be loaded, to expose the underlying layer 4.” *Id.* ¶ 22. After the GaN layer (purple) is etched away, a dielectric “SiO₂ film [is] then deposited by plasma CVD to cover the entire surface.” *Id.* Then “after patterning with photoresist, the area including the part where the gate electrode [is] to be loaded [is] masked,” leaving “the portion where [the] source and drain electrodes [are] to be loaded open.” *Id.* Metal Al is then deposited on exposed layer 4 to load source electrode S and drain electrode D. *Id.*

“Lastly, after etching away the masking and opening the SiO₂ film beneath it, the source electrode S and drain electrode G locations were masked with SiO₂ film, Au was deposited in the opening portions, and gate electrodes G were loaded above the p-type GaN layer 5 to fabricate the HEMT shown in Fig. 1.” *Id.* ¶ 23.

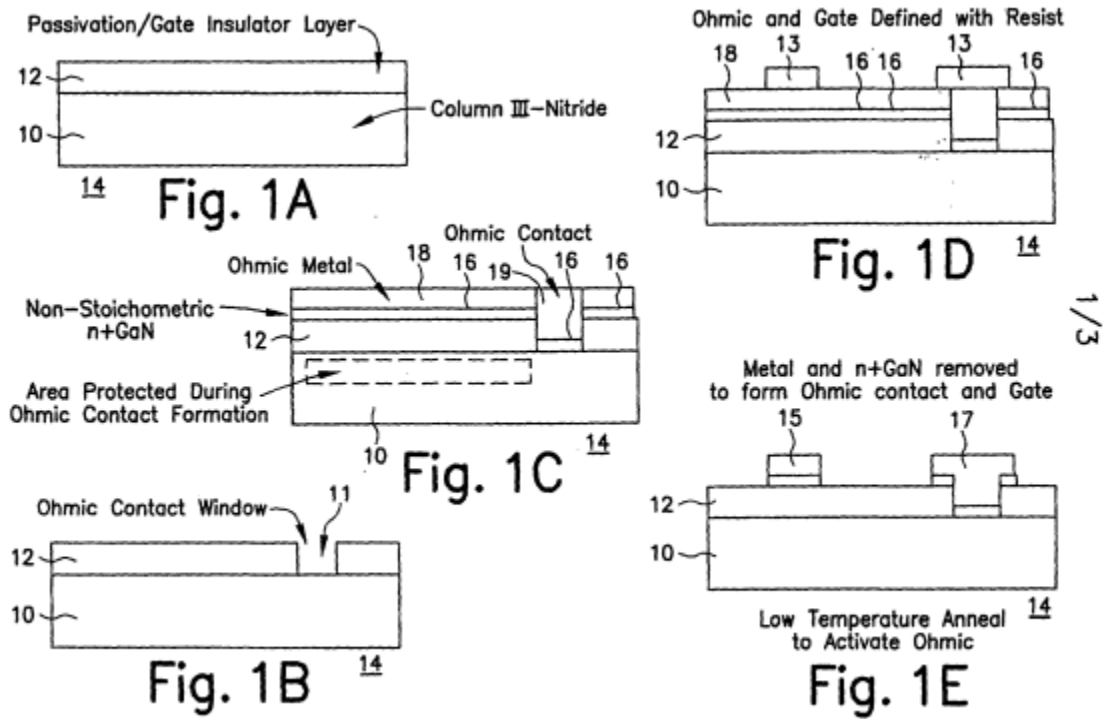
2. *Beach (Ex. 1005)*

Beach is a PCT Publication titled “III-Nitride Device Passivation and Method” that published June 23, 2005 and discloses methods of making a III-nitride semiconductor device that allow formation of device contacts without damaging the III-nitride material during the high temperature processing. Ex. 1005, code (12), (43), (54).

Although Beach itself does not use the term “self-aligned,” Petitioner states Beach discloses a “self-aligning” process to form the gate in which a single mask is used to etch both the gate metal and doped GaN materials to form “self-aligned gate contact 15 and doped GaN layer stack”.

Pet. 15 (citing Ex. 1005 ¶¶ 47–48); *see also, e.g.*, Pet. 6 (stating Beach uses a single mask to etch the gate and doped GaN materials (citing Ex. 1005 ¶ 47, Figs. 1D, 1E), 16 (“Beach discloses how to form the self-aligned gate and doped GaN stack” (citing Ex. 1005 ¶¶ 43–45, 47, 49)).

A process for making Beach’s semiconductor device is shown in Figures 1A–1E of Beach, reproduced below.



Figures 1A–1E depict a “series of steps in a process for forming a III-nitride device 14 with an ohmic contact and a gate electrode.” Ex. 1005 ¶ 40.

Figure 1A depicts device 14 having gate insulator layer 12 formed over layer 10, which is typically composed of a III-nitride, such as GaN. Ex. 1005 ¶¶ 40–41. In Figure 1B, ohmic contact window 11 is opened in layer 12 to provide access to layer 10 for the deposition of an ohmic contact. Ex. 1005 ¶ 42. In Figure 1C, prior to deposition of ohmic contact material, non-diffusive material 16 is formed over device 14. Ex. 1005 ¶ 43. After

layer 16 has been deposited over layer 12 and layer 10 within ohmic contact window 11, material for ohmic contact 19 is deposited over layer 16.

Ex. 1005 ¶ 45. An anneal step is performed to process ohmic material 18 to form ohmic contact 19 and the presence of protective layer 16 prevents damage to the surfaces of layers 10 and 12. *See* Ex. 1005 ¶ 46.

In Figure 1D, resist material 13 is deposited in a pattern to permit formation of both gate 15 as well as ohmic contact 17. Ex. 1005 ¶ 47. After deposition of photo resist layer 13, material 18 is removed by etching, except where protected by photoresist 13. Ex. 1005 ¶ 47. The removal, or etching process, also eliminates protective layer 16 under patterned photoresist 13. Ex. 1005 ¶ 47. Figure 1E shows that the resulting gate contact 15 and ohmic contact are connected to particular areas of device 14 through the remaining portions of protective layer 16. Ex. 1005 ¶ 48. After material 18 has been removed in regions not covered by photoresist 13, photo resist 13 is stripped off and the resultant structure is subjected to a low temperature anneal step. Ex. 1005 ¶ 49.

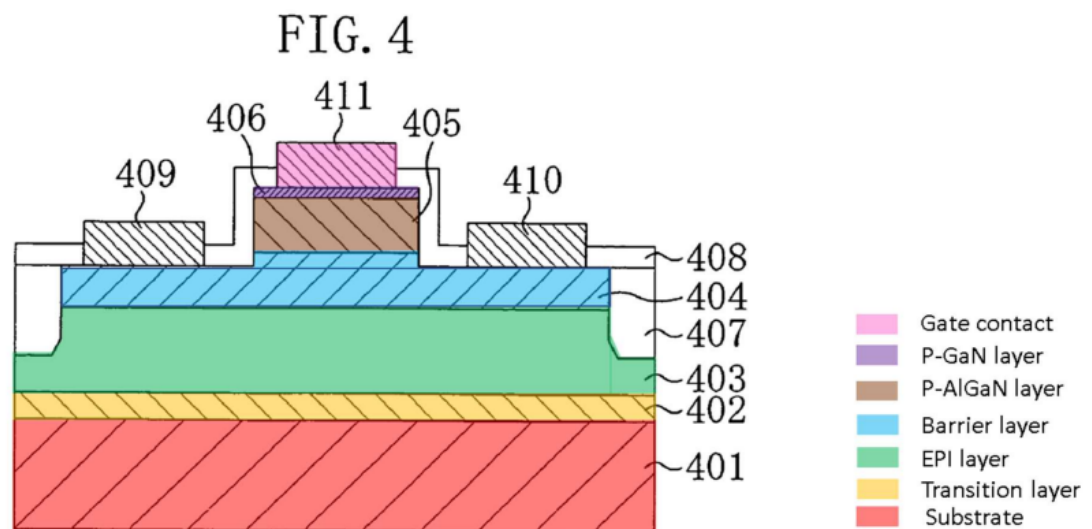
3. *Sheppard (Ex. 1006)*

Sheppard is a U.S. patent issued July 3, 2007 titled “Methods of Fabricating Nitride-based transistors with a Cap Layer and a Recessed Gate.” Ex. 1006, code (12), (45), (54). Sheppard states that its invention relates to, *inter alia*, methods of fabricating HEMTs, including forming a channel layer, forming a barrier layer on the channel layer, forming a cap layer on the barrier layer, and forming a gate recess in the cap layer that extends to the barrier layer. *Id.* at 2:30–35. Sheppard also states that the channel layer of Figure 1A may be deposited on the substrate using buffer

layers, transition layers, and/or nucleation layers. Ex. 1006, 7:25–28, Fig. 1A.

4. *Hikita-347 (Ex. 1007)*

Hikita-347 is a U.S. Patent Publication titled “Field-Effect Transistor and Method for Fabricating the Same” that published on December 7, 2006. Ex. 1007, code (12), (43), (54). Hikita-347 states that one object of the invention is “to provide a field-effect transistor of normally OFF type nitride semiconductor, which is applicable to a power transistor and allows a sufficient large current density, and a method for fabricating the field-effect transistor.” *Id.* ¶ 8.



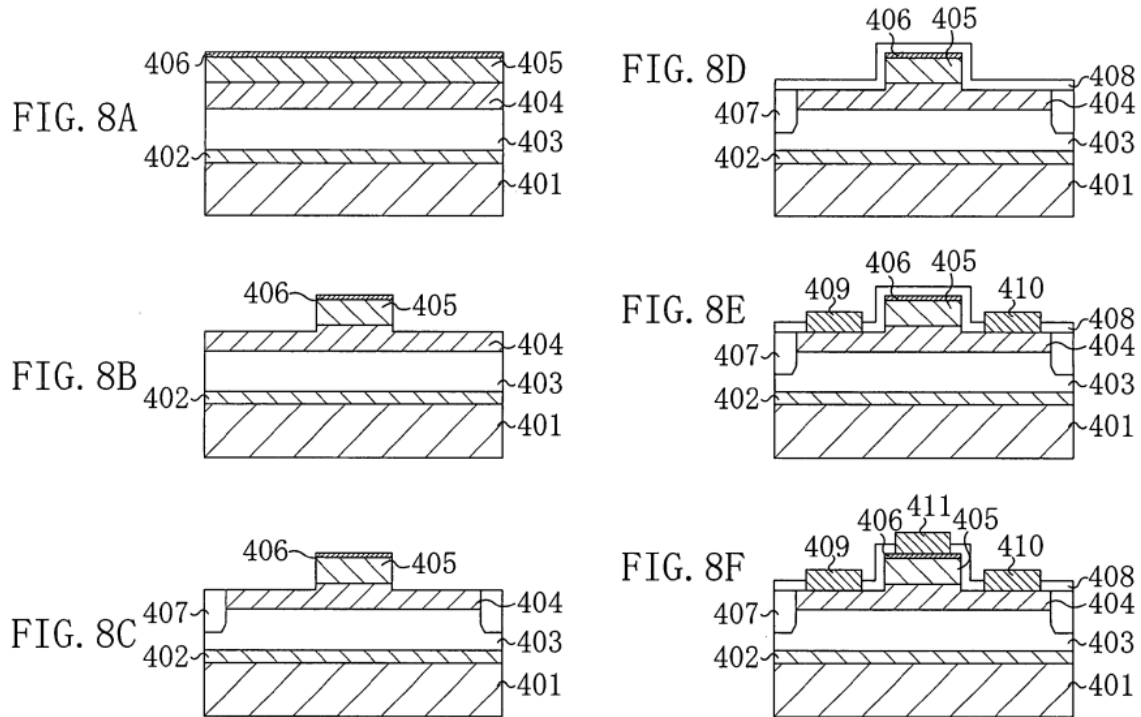
Hikita-347, Fig. 4.

Hikita-347 Figure 4, with Petitioner’s color annotations added, is a cross-sectional view of a field-effect transistor according to a second embodiment of the present invention. Ex. 1007 ¶ 47.

The transistor comprises sapphire substrate 401 (red), AlN buffer layer 402 (yellow), undoped GaN layer 403 (green), undoped AlGaN layer 404 (blue), p-type AlGaN layer 405 (brown), p-type GaN layer 406 (purple),

source electrode 409 (white), drain electrode 410 (white), and gate electrode/gate contact 411 (pink). Ex. 1007 ¶ 48.

Hikita-347 Figures 8A-8F, reproduced below, depict an exemplary method for making the transistor of Figure 4. Ex. 1007 ¶ 55.



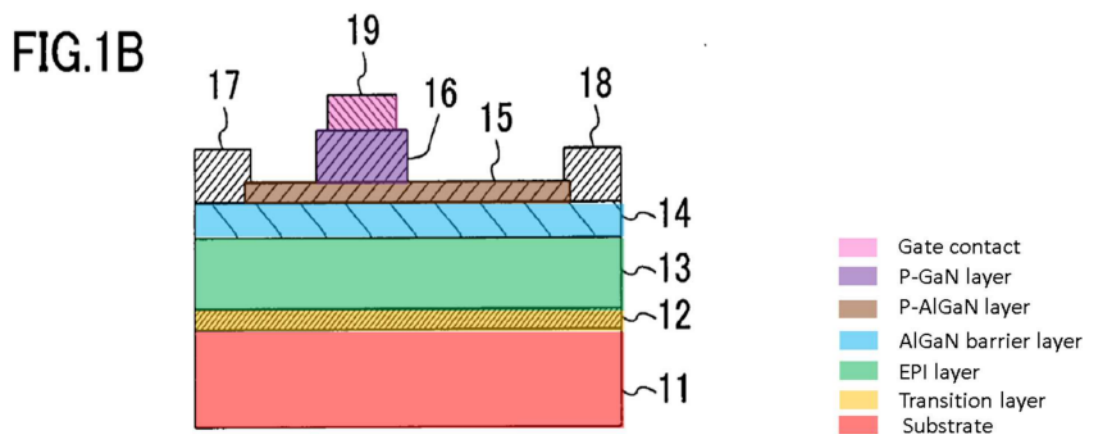
Figures 8A through 8F are cross sectional views illustrating respective steps for fabricating a field-effect transistor of Figure 4. Ex. 1007 ¶ 55.

In this process, AlN buffer layer 402, undoped GaN layer 403, undoped AlGaIn layer 404, p-type AlGaIn layer 405, and optional heavily doped p-type GaN layer 406 are formed on a sapphire substrate (Fig. 8A). See Ex. 1007 ¶ 56. Next, as shown in Figure 8B, parts of layer 406, layer 405, and an upper portion of layer 404 located in a part other than the gate region are selectively removed, such as by etching. Ex. 1007 ¶ 57. Next, with a device formation region covered with a photoresist, boron is ion-implanted and isolation region 407 is formed (Fig. 8C). Ex. 1007 ¶ 58. Subsequently, an SiN film is deposited (Fig. 8D). Ex. 1007 ¶ 59. Openings

in the SiN film are then opened, such as by etching, and source electrode 409 and drain electrode are formed in the openings and a heat treatment is performed (Fig. 8E). Ex. 1007 ¶ 60. Next, part of SiN film 408 on p-type GaN layer 406 is removed, such as by etching. Ex. 1007 ¶ 61. Then gate electrode 411 is formed in one of the openings in SiN film 408. Ex. 1007 ¶ 61.

5. *Hikita-023 (Ex. 1008)*

Hikita-023 is a U.S. Patent Publication titled “Nitride Semiconductor Device and Method for Fabricating the Same,” that published on April 3, 2008. Ex. 1008, code (12), (43), (54). Hikita-023 states that one object of the invention is to prevent the current collapse caused in normally-off type nitride semiconductor devices applicable to power transistors. Ex. 1008 ¶ 14.

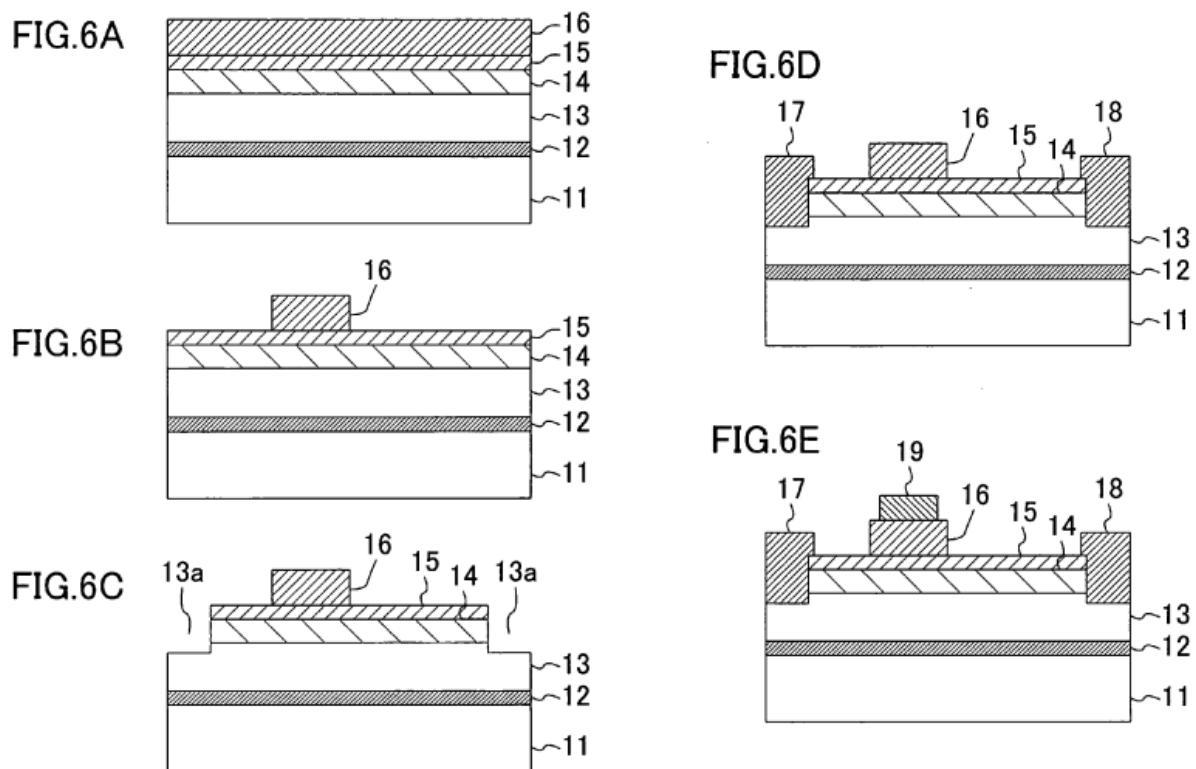


Hikita-023, Fig. 1B.

Hikita-023 Figure 1B is a sectional view of a nitride semiconductor device according to a first embodiment having substrate 11 (red), buffer layer 12 (yellow), undoped GaN layer 13 (green), undoped AlGaN 14 (blue), p-type AlGaN layer 15 (brown), p-type GaN layer 16 (purple), source

contact 17, drain 18 contacts (white), and gate contact 19 (pink). Ex. 1008 ¶¶ 38, 51–56.

Hikita-023 Figures 6A–6E, reproduced below, are cross sectional views showing successive process steps of the method for fabricating a nitride semiconductor device according to the first embodiment shown in Figure 1B. Ex. 1008 ¶ 43.



Hikita-23 Figures 6A–6E illustrate successive process steps to fabricate the semiconductor device according to the first embodiment. Ex. 1008 ¶¶ 75–80.

F. Alleged Obviousness of Claims 1–3 over Yoshida, Beach, and Sheppard

Independent claim 1, and claims 2 and 3 which depend therefrom, are directed to a multi-step process for fabricating an enhancement mode GaN

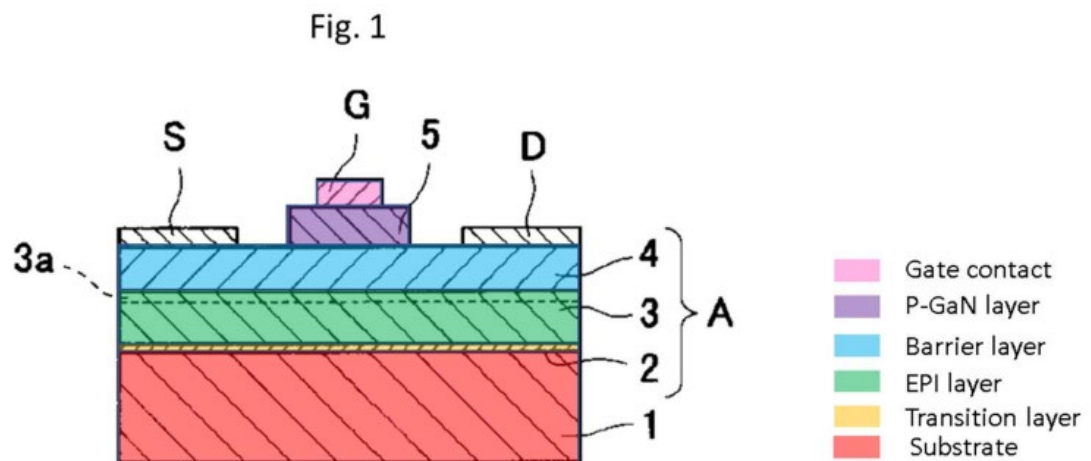
transistor. Ex. 1001, 6:59–7:15. Petitioner asserts that the combination of Yoshida, Sheppard, and Beach teaches each of the steps recited in these claims 1. Pet. 13–43; Reply 13–26. Patent Owner opposes.

Having considered the parties' contentions and supporting evidence, we determine that Petitioner fails to sufficiently show why a POSITA would have been motivated to modify Yoshida's process to incorporate Beach's single mask process to arrive at the method recited in claim 1. Accordingly, Petitioner has not shown by a preponderance of the evidence that claim 1, or claims 2 and 3 which depend therefrom, are unpatentable.

1. *Claim 1*

a) *The Parties' Arguments*

Relying, *inter alia*, on Yoshida's Figure 1, reproduced below, Petitioner asserts that the combination of Yoshida, Sheppard, and Beach teaches each of the steps recited in method claim 1.



Yoshida Figure 1, with Petitioner's color annotations added, depicts a HEMT having gate contact G (pink), p-doped GaN layer 5 (purple), source S and drain D (white), barrier layer 4

(blue), EPI layer (green), GaN buffer layer 2 (yellow), and substrate 1 (red). Ex. 1004, Fig. 1; Pet. 25–26.

Petitioner asserts that Yoshida discloses or suggest forming a GaN transistor, such as that shown in Figure 1 above, by growing the transition layers (yellow), EPI layer (green), barrier layer (blue), and p-doped GaN layer (purple) recited in steps [1a]–[1d]. Pet. 25–30 (citing Ex. 1004 ¶¶ 10–13, 15, 19–21, Fig. 1; Ex. 1003 ¶¶ 99, 101, 108–109, 112, 114). Petitioner also states that, to the extent Yoshida only discloses a single transition layer, not the multiple transition layers (yellow) recited in step [1a], Sheppard’s disclosure of a GaN transistor having multiple transition layers on a silicon substrate meets this limitation. Pet. 27 (citing Ex. 1006, 6:58–7:7, 7:25–32). Patent Owner does not dispute these assertions. *See generally* Resp.

Petitioner also asserts that Yoshida and/or Beach teach the remaining steps, namely the “the gate structure steps” recited in steps [1e1]–[1e5]¹⁰; the dielectric formation steps recited in steps [1f1]–[1f4]¹¹; and “the “ohmic contact steps” recited in steps [1g1]–[1g5].¹² Pet. 30–39.

With respect to gate structure steps [1e1]–[1e5], Petitioner asserts that, as shown in Yoshida Figure 1 above, Yoshida discloses forming gate electrode/gate contact G (pink) over the p-GaN layer 5 (purple), as required by claim step [1e1]. Pet. 30–31 (citing Ex. 1004 ¶¶ 9, 16, 22–23, Fig. 1). Petitioner also states that Yoshida discloses “that, to form the p-GaN layer

¹⁰ Petitioner refers to steps [1e1]–[1e5] as the “gate structure steps” and contends a “single mask” is used to etch both the gate contact layer and an underlying layer. Pet. Reply 2.

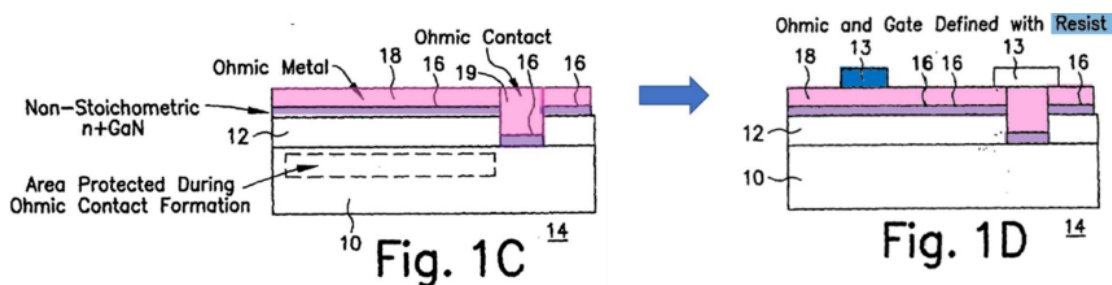
¹¹ Petitioner describes steps [1f1]–[1f4] as the dielectric formation steps. Pet. Reply 12.

¹² Petitioner refers to claim elements [1g1]–[1g5] as the “ohmic structure steps.” *See* Pet. Reply 2–3.

and gate contact, the pGaN layer was etched away ‘except where the gate electrode was to be loaded’” and that the gate electrode is then loaded above the p-GaN layer. Pet. 31 (citing Ex. 1004 ¶¶ 22–23; Ex. 1003 ¶ 117).

Petitioner admits that Yoshida does not explicitly disclose using a single mask (gate photo resistant pattern) to etch the p-GaN layer and gate contact layer or a p-GaN layer (purple) and gate contact layer (pink) of the same width. Petitioner asserts, however, that Beach’s method of forming a self-aligned gate and doped GaN layer renders this obvious. See Pet. 31 (citing Ex. 1003 ¶ 118). Relying on Beach’s Figure 1C, Petitioner asserts Beach discloses depositing gate contact layer (pink ohmic material 18) on doped GaN layer 16 (purple). Pet. 31–32 (citing Ex. 1005 ¶ 45, Fig. 1C).

Petitioner asserts that Beach’s teaching that “resist material 13 is deposited in a pattern to permit formation of gate 15 and ohmic contact 17” discloses “applying a gate photo resistant pattern” as required by step [1e2]. Pet. 32 (citing Ex. 1005 ¶ 47, Figs. 1C, 1D); *see also* Pet. 36–37 (stating the same teaching discloses applying a metal photo resistant pattern as required by step [1g2]).

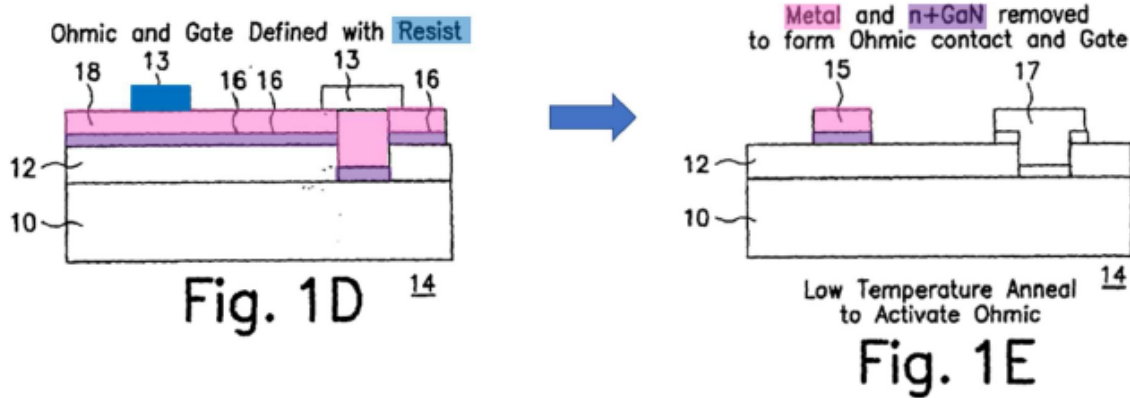


Beach, Figs. 1C, 1D.

Beach Figures 1C and 1D, with Petitioner’s color annotations added, depict certain steps for forming a III-nitride device. Ex. 1005 ¶ 40.

Petitioner also asserts that Beach discloses step [1e3] (etching away the gate contact layer [pink] outside the gate region) and step [1e4] (etching

away the doped GaN layer [purple] except a portion of the doped GaN layer beneath the gate contact) by teaching that after photoresist layer 13 (blue) is deposited, “material 18 [(pink)] is removed, as by etching, except where protected by photoresist 13. The removal, or etching process, also eliminates protective layer 16 under patterned photoresist 13.” Pet. 33 (citing Ex. 1005 ¶ 47, Figs. 1D, 1E (reproduced below)).



Beach, Figs. 1D, 1E.

Beach Figures 1D and 1E, with Petitioner’s color annotations added, depict certain steps for forming a III-nitride device. Ex. 1005 ¶ 40.

With respect to the reason to modify the asserted art to arrive at gate deposition steps [1e1]–[1e5], Petitioner asserts that a POSITA would have been motivated to apply Beach’s single mask process to form Yoshida’s device and expected success in doing so. Pet. 33 (citing Pet. § VII.A.1.d.ii [Pet. 21–22]). In particular, Petitioner contends that a POSITA would have been motivated to use Beach’s single mask process to form Yoshida’s gate contact and doped GaN layer for two reasons. Pet. 21–22.

First, Petitioner asserts that “Beach’s¹³ single mask processes effectively achieves Yoshida’s objective of etching away the doped GaN layer except the area where the gate contact is to be loaded.” Pet. 21 (citing Ex. 1003 ¶ 125; Ex. 1004 ¶ 22). Petitioner asserts that a POSITA would have recognized that Beach’s single mask process “automatically achieves self-alignment between the two layers, thus improving the gate’s alignment, which is desirable. Pet. 21 (citing Ex. 1003 ¶ 125; Ex. 1009¹⁴; Ex. 1033¹⁵).

Second, Petitioner asserts that Beach’s single mask process is simpler. Pet. 21 (citing Ex. 1003 ¶ 126). Petitioner asserts that Yoshida uses “separate masks for each etching step” while “Beach uses a single mask to etch the gate and doped GaN layer, removing the additional second mask steps.” Pet. 21 (citing Ex. 1003 ¶ 126, Ex. 1005 ¶ 47). Petitioner explains that a POSITA would have understood that applying masks is a substantial undertaking during manufacturing, and the removal of any additional mask application simplifies the manufacturing process, reducing cost. Pet. 21–22 (citing Ex. 1003 ¶ 126; Ex. 1033, 3:55–61).

Regarding the remaining steps of claim 1, Petitioner asserts Yoshida discloses steps [1f1–1f4] by, disclosing:

(1) depositing an SiO₂ film to “cover the entire surface” after etching away the p-type GaN layer (Pet. 34 (citing Ex. 1003 ¶ 131; Ex. 1004 ¶ 22)),

¹³ We omit the parties’ emphasis of reference names without specifying “emphasis omitted” throughout.

¹⁴ US Pub. 2007/0007547, pub. Jan. 11, 2007 (“Beach-547”) (describing self-aligned gates as advantageous).

¹⁵ US 6,897,514, pub. May 24, 2005 (“Kouznetsov”)(stating that self-alignment decreases die size and cost).

(2) patterning the SiO₂ film with photoresist such that the portion of the gate contact is “masked” and the portion to load the source and drain contacts are left open (Pet. 34 (citing Ex. 1004 ¶ 22)),

(3) etching the SiO₂ film to “leave open the drain and source contact area (Pet. 34 (citing Ex. 1004 ¶¶ 13, 21–22; Ex. 1003 ¶ 133)), and

(4) etching away the masking (Pet. 34 (citing Ex. 1004 ¶ 23; Ex. 1003 ¶ 134)).

Finally, Petitioner asserts Yoshida and Beach render obvious steps [1g1]–[1g5]. Pet. 35–39. In particular, Petitioner asserts Yoshida discloses depositing an ohmic contact metal (aluminum) onto layer 4 to load the ohmic source and drain contacts (S and D). Pet. 35 (citing Ex. 1004 ¶ 10, 22; Ex. 1003 ¶ 135). Petitioner admits that Yoshida does not explicitly disclose a process for forming the source and drain electrodes but asserts that “Beach renders obvious using the remaining steps in [1g] to form Yoshida’s ohmic source and drain contacts.” Pet. 36–39. Petitioner cites to Beach’s:

(1) deposition of ohmic contact metal 18 over layer 16 in ohmic contact window 11 (Pet. 36 (citing Ex. 1005 ¶ 45, Figs. 1B–1C)),

(2) application of metal photo resist pattern 13 over ohmic contact metal 18 (Pet. 36–37 (citing Ex. 1005 ¶ 47, Figs. 1C, 1D)),

(3) etching of ohmic contact metal 18 except the portion protected by the mask (Pet. 37 (citing Ex. 1004 ¶ 47, Figs. 1D, 1E)),

(4) removing mask 13 (Pet. 37 (citing Ex. 1005 ¶ 49)), and

(5) thermal annealing to form the source and drain contacts (Pet. 38 (citing Ex. 1005 ¶ 49, 54; Ex. 1003 ¶ 141)).

Patent Owner makes numerous arguments in response. For example, one of Patent Owner's main arguments is that none of the asserted references disclose or suggest a "gate-first" process that is required under a proper claim construction of the '508 patent. *See, e.g.*, Resp. 1–2, 6 (citing Ex. 2001 ¶¶ 58, 75), 17–22 (stating the '508 patent requires a "gate-first" process). Patent Owner asserts that combining Yoshida—which teaches a "gate-last" process—with Beach's "gate-simultaneous" process—which forms Beach's gate 15 and ohmic contacts 17 simultaneously—would not result in the gate-first process claimed by the '508 patent. Resp. 21, 27, 37–41.

Patent Owner also asserts that a POSITA would not have been motivated to combine Yoshida and Beach to arrive at the claimed invention. Resp. 34–48. Patent Owner contends Petitioner merely identifies disclosures from each reference but does not explain why or how these disclosures could be fit together to meet the steps recited in the claims. Resp. 36; *see also*, *e.g., id.* at 41–42 (stating Petitioner fails to identify what steps in Yoshida are modified to incorporate Beach, to explain the modified process itself, or show why a POSITA would have been motivated to perform the combined process). For example, Patent Owner states that even if a self-aligned gate etching process, such as in Beach, were well-known and conventional, Petitioner does not sufficiently explain why a POSITA would have modified the particular process disclosed in Yoshida, which deposits gate metal on an already etched p-type GaN layer. Resp. 40. Patent Owner explains that because Yoshida deposits gate metal on an already etched p-type GaN layer, using Beach's process would not reduce the overall number of etching steps or simplify the process. Resp. 40 (citing Ex. 2001 ¶ 153). Patent Owner

also states that Petition fails to explain how to modify Yoshida to perform a self-aligned process given Yoshida's teaching to deposit the intervening silicon dioxide materials and source and drain contact. Resp. 42 (citing Ex. 2001 ¶ 156).

Patent Owner also asserts that using a self-aligned process in Yoshida would require an extra step to remove Yoshida's dielectric layer to open an area for gate electrode deposition and self-alignment, which would further complicate, not simplify, the process.¹⁶ Resp. 40–41.

In its Reply, Petitioner asserts that the claims do not require that the recited steps be performed in any particular order and do not require a gate-first process. Pet. Reply 1–2. Petitioner states that the claims also cover non-gate-first processes, such as a “D (dielectric), O (ohmic contact), G (gate) process” (i.e., a D-O-G process) as well as an “O (ohmic contact), G (gate), D (dielectric) process” (i.e., an O-G-D process). Pet. Reply 4–12.

Petitioner also disputes Patent Owner's contention that the Petition fails to sufficiently explain the combination of Yoshida and Beach. Pet. Reply 13–17. Petitioner asserts the Petition explains a POSITA would have been motivated to combine, *inter alia*, Yoshida's process with Beach's self-aligned gate process and ohmic etching process with a reasonable expectation of success. *See* Pet. Reply 13. To support this argument, Petitioner states that Yoshida teaches a D-O-G process and a POSITA would have modified Yoshida's D-O-G process to incorporate Beach's self-aligned gate using the process set forth in the diagram below. Pet. Reply 13–14 (citing Shealy Supp. Dec ¶ 32; Reply § II.C.1).

¹⁶ We do not address Patent Owner's remaining arguments for patentability as they are not necessary to our Decision.



DOG Process Order (Yoshida-Beach)

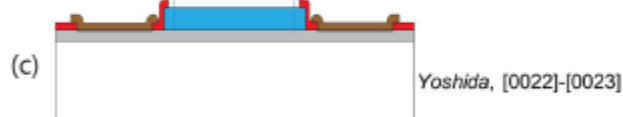
- 1) Epitaxy Grown - buffer/barrier/p-GaN
- 2) Resist Applied



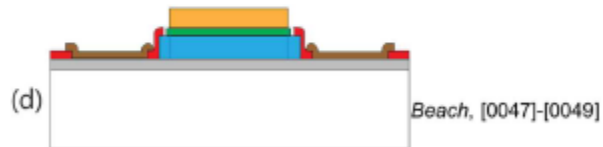
- 3) p-GaN Layer Etched
- 4) Dielectric Layer Deposited (D)



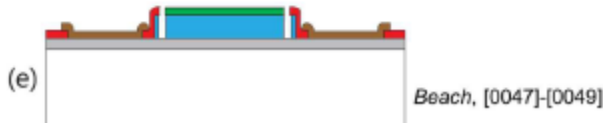
- 5) Windows Opened in Dielectric for Contacts
- 6) Ohmic Contact Metal Applied, Patterned, Annealed (O)



- 7) Patterned Gate Contact (G) Metal Applied
- 8) Gate Resist Applied



- 9) Self Aligned Etch of Gate Metal and p-GaN (G)
- 10) Strip Resist



ShealySupp. ¶32 (Modified *Yoshida* process).

The Modified Yoshida process diagram above contains five figures (a)–(e) that Petitioner asserts illustrates the sequence of a combined Yoshida and Beach process. Reply 13–14.

Petitioner states in its Reply that Beach's self-aligned gate process was a conventional technique used before the '508 patent and a POSITA would

have incorporated these conventional techniques into Yoshida's D-O-G with a reasonable expectation of success. Pet. Reply 13–14 (citing Ex. 1003 ¶¶ 105, 127, 129).

Petitioner also asserts that a “gate-first” process would have been obvious because a POSITA would have been motivated to select a gate-first G-D-O process to self-align the ohmic source and drain contacts to the gate contact to reduce the minimum source-to-gate distance and reduce the source and drain access resistance, and because a “‘gate-first’ process is one of only six sequencing permutations available.” Pet. Reply 16–17 (citing Ex. 1041 (Second Shealy Dec.) ¶¶ 41–43).

b) Analysis

We agree with Patent Owner that Petitioner fails sufficiently explain why or how a POSITA would have modified Yoshida's process to incorporate Beach's single mask, self-aligned gate process to form Yoshida's device using the method recited in claim 1. Resp. 34–36.

The Petition identifies two reasons that a POSITA “would have been motivated to apply Beach's single mask process to form Yoshida's device and expected success in doing so.” Pet. 33 (citing Pet. § VIII.A.1.d.ii [Pet. 21–22] for the reasons a POSITA would have been motivated to apply Beach's single mask process); *see also* Pet. 21–22 (setting forth two reasons a POSITA would have been motivated to use Beach's single mask process to form the gate contact and doped GaN layer to improve Yoshida's device); *see also* Pet. 31–32 (providing arguments as to how Yoshida in view of Beach teaches or suggests the gate structure steps). Neither of Petitioner's asserted reasons sufficiently show why a POSITA would have modified

Yoshida's process in view of Beach to form a device having a different p-GaN layer than that of either prior art reference.¹⁷

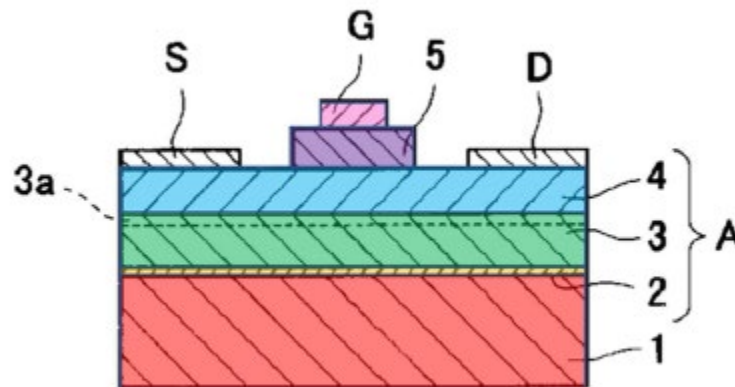
(1) Petitioner's First Asserted Reason to Modify Yoshida's Process

Petitioner first asserts that it would have been obvious to use Beach's single mask to "effectively achieve[] Yoshida's objective of etching away the doped GaN layer except the area where the gate contact is to be loaded" and that this process would desirably improve the gate's alignment. Pet. 21 (citing, *inter alia*, Ex. 1003 ¶ 125; Ex. 1004 ¶ 22). As explained in detail below, and as admitted by Petitioner in its Reply, the combined process etches away different areas of the doped GaN layer than what is etched away in either Yoshida or Beach and what is shown in the Petition, resulting in a device having "remnant islands" of p-GaN material. Pet. 31–33; Pet. Reply 13–15.

Specifically, the Petition identifies the area of the p-GaN layer etched away in Yoshida by pointing to Yoshida Figure 1 (shown below) and stating that although the figure shows that Ga-N layer 5 extends beyond the gate contact, Yoshida's description states that layer 5 is etched away except where the gate electrode was to be loaded. Pet. 31 (citing Ex. 1004 ¶ 22). No remnant islands are shown in Yoshida's Figure 1, however.

¹⁷ The parties also dispute whether the non-etched p-GaN layer that results in the remnant islands satisfy step [1e4], which requires "etching away the doped GaN layer, except a portion of the doped GaN layer beneath the gate contact." Because we determine Petitioner has not sufficiently shown a reason that a POSITA would have modified Yoshida's process in view of Beach to form Yoshida's device, we need not determine whether Yoshida's modified process also fails to teach or suggest step [1e4].

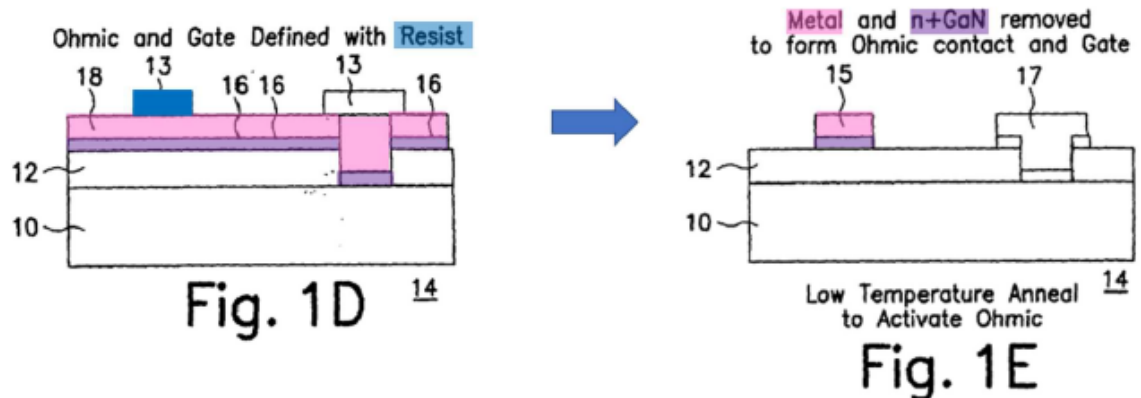
Fig. 1



Yoshida, Fig. 1.

Yoshida Figure 1, with Petitioner's color annotations added, depicts a HEMT having gate contact G (pink), p-doped GaN layer 5 (purple), source S and drain D (white). Ex. 1004, Fig. 1; Pet. 31.

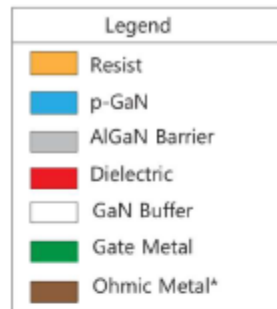
Petitioner also points to Beach Figure 1E to identify the area of the p-GaN layer etched away, stating Beach discloses “etching away the gate contact layer outside the gate region” and etching away the doped GaN layer, except a portion of the doped GaN layer beneath the gate contact” as shown below.” Pet. 33 (citing Ex. 1005 ¶ 47).



Beach, Figs. 1D, 1E.

Again, no remnant islands are shown in Beach's Figure 1E (or any other Beach figure).

In its Reply, Petitioner provides additional details on how to combine Yoshida and Beach and the resulting p-GaN layer and gate structure. Pet. Reply 13–14. The Reply states that Yoshida uses a D-O-G (i.e., a D (dielectric), O (ohmic contact), G (gate)) process to make its transistor and that a POSITA would have modified Yoshida's D-O-G process to incorporate Beach's self-aligned gate using the process set forth in the diagram below. Pet. Reply 13–14 (citing Second Shealy Dec ¶ 32; Reply § II.C.1).



* Source/Drain Contacts

DOG Process Order (Yoshida-Beach)

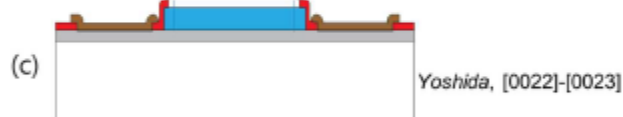
- 1) Epitaxy Grown - buffer/barrier/p-GaN
- 2) Resist Applied



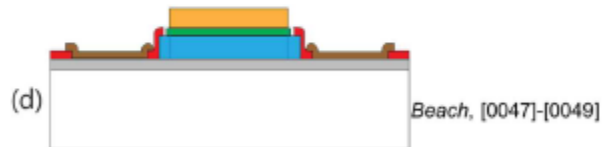
- 3) p-GaN Layer Etched
- 4) Dielectric Layer Deposited (D)



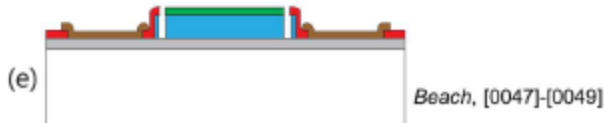
- 5) Windows Opened in Dielectric for Contacts
- 6) Ohmic Contact Metal Applied, Patterned, Annealed (O)



- 7) Patterned Gate Contact (G) Metal Applied
- 8) Gate Resist Applied



- 9) Self Aligned Etch of Gate Metal and p-GaN (G)
- 10) Strip Resist



ShealySupp. ¶32 (Modified *Yoshida* process).

The Modified Yoshida process diagram above contains five figures (a)–(e) that Petitioner asserts illustrates the sequence of a combined Yoshida and Beach process. Pet. Reply 13–14.

As shown in Figure (e) above of the Modified Yoshida process, the modified process results in “remnant islands,” which are the portions of the

p-GaN layer (blue) underneath the dielectric layer (red) on either side of the gate. Pet. Reply 5–6, 27; Ex. 1041 ¶ 31. The fact that the p-GaN area etched away in the Modified Yoshida process differs from the area of p-GaN etched away in either Yoshida or Beach as well as Petitioner’s description of how the p-GaN layer would be etched in the combined process belies Petitioner’s assertion that a POSITA would have been motivated to apply Beach’s single mask process “to form Yoshida’s device and expected success in doing so.” Pet. 33.

The existence of the remnant islands is not an insignificant difference. Although the parties disagree whether the remnant islands improve or impair Yoshida’s gate, the parties do not dispute that the p-GaN layer of the combined process functions differently than Yoshida’s p-GaN layer lacking such remnant islands. *See* Resp. 23 (asserting that a POSITA would not leave such remnant islands because they are detrimental to the function of the device and citing Ex. 2001 ¶ 90); Pet. Reply 6 (asserting that the remnant islands “could improve performance”). Indeed, Petitioner states that the remnant islands between the gate and drain can reduce “longitudinal electric field strength and in turn increase[] the device’s breakdown voltage.” Pet. Reply 6 (citing, *inter alia*, Ex. 1041 ¶ 33). Petitioner also asserts that the remnant islands between the source and gate can lower the channel charge in this region, which would “reduce the non-linear component of the device’s source resistance, important for high frequency operation.” Pet. Reply 6 (citing, *inter alia*, Ex. 1041 ¶ 33).

Thus, regardless of whether the remnant p-GaN islands created in the combined process result in a non-functional device or an “improved device,” it is undisputed that the combined method etches away the doped GaN layer

differently than that taught in either asserted prior art reference, resulting in remnant islands not found in Yoshida's device, and these remnant islands alter the functionality of Yoshida's p-GaN layer. Given the structural and functional differences between the pGaN layer resulting from the combined process and the p-GaN layer of Yoshida, we are not persuaded by Petitioner's argument that a POSITA would have been motivated to use Beach's single mask process to effectively etch away Yoshida's p-GaN layer.

We also recognize that in its Reply, Petitioner presents an alternative process that could be used if no remnant islands were desired. Pet. Reply 6–7. This alternative process, however, is discussed in a section of the Reply addressing claim scope, where Petitioner identifies different processes that it asserts could fall within the scope of claim 1. Reply 13–15. Significantly, however, neither the Petition nor the Reply make any argument that a POSITA would have been motivated to combine Yoshida and Beach using this alternative process. See Reply 13–15.

*(2) Petitioner's Second Asserted Reason to
Modify Yoshida's Process*

The second reason the Petition states that a POSITA would have used Beach's single-mask process with Yoshida is to simplify Yoshida's process. Pet. 21–22. Petitioner asserts that Beach's single mask process is simpler than Yoshida's two mask process, which uses "separate masks for each etching step," while "Beach uses a single mask to etch the gate and doped GaN layer, removing the additional second mask steps." Pet. 21 (citing Ex. 1003 ¶ 126, Ex. 1005 ¶ 47). Petitioner explains that a POSITA would have understood that applying masks is a substantial undertaking during manufacturing, and that the removal of any additional mask application

simplifies the manufacturing process, reducing cost. Pet. 21–22 (citing Ex. 1003 ¶ 126; Ex. 1033, 3:55–61 (describing that use of the same photoresist mask to form the layers decreases process cost and complexity)).

This argument is not persuasive because Petitioner does not sufficiently show that the combined process would decrease the total number of etching or masking steps or reduce costs.

Significantly, Petitioner admits that even in the combined process, a separate masking step and a separate etching step are still needed to etch the GaN layer. Pet. Reply 13–15. The first masking and etching steps are shown in figures (a) and (b) of Petitioner’s “Modified Yoshida’s process” and the second masking and etching step is shown in figures (d) and (e). Pet. Reply 14 (citing Ex. 1004 ¶¶ 19–22). As demonstrated in Petitioner’s proposed combination, GaN layer (blue) is masked and then etched with a resist pattern (yellow) two times. Thus, Petitioner’s contention that the combined process results in fewer masking and etching steps by masking and etching the GaN layer and the gate metal layer simultaneously is belied by the fact that, even in the combined process, the GaN layer must still be masked and etched separately as shown in figure (b) of Petitioner’s Modified Yoshida process. Pet. Reply 14; Ex. 1004 ¶¶ 19–22.

Thus, none of the reasons articulated in the Petition are sufficient to show that a POSITA would have been motivated to modify the procedure taught in Yoshida to incorporate Beach’s single mask process.

Petitioner also provides, in its Reply, new reasons that a POSITA would have been motivated to use Beach’s single mask process with Yoshida stating a POSITA would have used Beach’s process to protect the gate region from contamination. *See, e.g.*, Pet. Reply 13 (citing Ex. 1041

¶ 32). Petitioner’s contention presents a new theory of unpatentability based on new evidence that exceeds the proper scope of a reply brief under 37 C.F.R. § 42.23(b). *See Corephotonics, Ltd. v. Apple Inc.*, 84 F.4th 990, 1002 (Fed. Cir. 2023) (“the Board is not permitted to entertain ‘[s]hifting arguments’ but must, instead, reject any ‘entirely new theory of *prima facie* obviousness absent from the petition,’ if the petitioner attempts to inject such a theory into the proceeding post-petition”); *Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1369–70 (Fed. Cir. 2016) (holding that the Board did not err in refusing the reply brief as improper under 37 C.F.R. § 42.23(b) because petitioner relied on an entirely new rationale to explain why one of skill in the art would have combined the references at issue); For that reason, we will not consider it.

(3) *Petitioner’s “Gate-First Process”*

For completeness, we address one other argument relating to Petitioner’s assertion that claim 1 would have been obvious over Yoshida, Beach, and Sheppard. In its Response, Patent Owner also argues that claim 1 would not have been obvious over Yoshida, Beach, and Sheppard because the claims require a “gate-first” process, which the asserted art does not teach. Resp. 17–25, 35–41.

In its Reply, Petitioner asserts that the claims do not require a gate-first process, but that even if they did, a gate-first process would have been obvious. Pet. Reply 16–17. Petitioner makes a new argument that a gate-first process is one of only six sequencing permutations available, all of which are suitable options. Pet. Reply 16–17 (citing Ex. 1041 ¶ 41); *see also* Ex. 1041 ¶ 41 (setting forth a process to form a gate, dielectric, and ohmic contact in that order). Petitioner asserts that a POSITA would have

been motivated to select a gate-first process to align the ohmic source and drain contacts to the gate contact to “reduce the minimum source-to-gate distance and reduce the source and drain access resistance.” Pet. Reply 16 (citing Ex. 1041 ¶ 42).

To the extent that Petitioner is asserting that it would have been obvious to combine Yoshida, Beach, and Sheppard to arrive at a gate-first process, this argument is not persuasive. Petitioner fails to provide any argument or evidence as to how any of the asserted references relate to, let alone teach, a gate-first process. *See generally* Pet. Reply; *see also* Pet. Reply 16–17 (stating that a POSITA would have been motivated to use a G-D-O process but not sufficiently explaining how a POSITA, looking at Yoshida and Beach, would have modified the asserted art to select a gate-first process). Petitioner’s assertion that a gate-first process would have been obvious, untethered to any disclosure in the asserted art, or to any argument as to how a POSITA would have modified the asserted art to arrive at a G-D-O process, is not sufficient to show that claim 1 would have been obvious over Yoshida, Beach, and Sheppard. It is improper to use hindsight to pick and choose isolated disclosures in the prior art without sufficiently explaining why a POSITA would have been motivated to combine these disclosures to arrive at the claimed invention. *See In re Fine*, 837 F.2d 1071, 1075 (Fed. Cir. 1988) (“One cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention.”). Thus, to the extent Petitioner contends that it would have been obvious for a POSITA to modify Yoshida, Beach, and Sheppard to arrive at a “gate-first” process, any such argument is untimely, not clearly articulated, and not persuasive.

Accordingly, Petitioner has not shown by a preponderance of the evidence that claim 1 would have been obvious over Yoshida, Beach, and Sheppard.

2. *Claims 2–3*

Claims 2 and 3 depend from claim 1. Petitioner asserts that Yoshida discloses the limitations recited in these dependent claims. Pet. 39–50. Petitioner’s arguments do not cure the deficiencies set forth regarding claim 1. Accordingly, Petitioner has not shown by a preponderance of the evidence that claims 2 and 3 would have been obvious over Yoshida, Beach, and Sheppard.

G. Alleged Obviousness of Claims 1–4 over Hikita-347, Beach, and Sheppard (Ground 2)

Petitioner asserts that claims 1–4 would have been obvious over Hikita-347, Beach, and Sheppard. Pet. 42–74. With respect to independent claim 1, Petitioner states that “[l]ike the Yoshida combination, Hikita-347 and Beach disclose a GaN device where the doped GaN layer is etched away except the gate region.” Pet. 48. Petitioner states that a “POSITA would have been motivated to use Beach’s single mask process to form the gate contact and p-type GaN layer(s) in Hikita-347’s device and expected success for the same reason explained in Ground 1. Pet. 49 (citing Ex. 1003 ¶¶ 179, 229).

With respect to independent claim 4, Petitioner admits that Hikita-347 does not disclose using a single mask (gate photo resistant pattern) to etch away the two doped layers recited in [4f], but asserts that it would have been obvious to apply Beach’s single mask masking process to etch these layers for the same reasons set forth in Ground 1. *See* Pet. 73 (citing Pet. § VIII.A.1.d.ii [pp. 18–24]). In its Reply, Petitioner admits that the

“Modified Hikita-347 process” that uses Beach’s self-aligned, single mask process results in remnant islands. Pet. Reply 26–27; Ex. 1041 ¶ 31.

Petitioner’s argument for ground 2 is unpersuasive for the same reasons regarding ground 1 set forth above. Accordingly, Petitioner fails to show by a preponderance of the evidence that claims 1–4 would have been obvious over Hikita-347, Sheppard, and Beach.

H. Alleged Obviousness of Claim 5 over Hikita-023, Beach, and Sheppard (Ground 3)

Petitioner asserts that claim 5 is unpatentable over Hikita-023, Beach, and Sheppard. Pet. 74–90. Patent Owner opposes. Resp. 63–69.

Petitioner admits, *inter alia*, that Hikita-023 does not use a single mask to etch the gate material and p-type GaN layer as required by claim 5, but states “Beach does, as explained in Ground 1.” Pet. 76 (citing, *inter alia*, Pet. § VIII.A.2.f [Pet. 30–34]). Petitioner states that a “POSITA would have been motivated to use Beach’s single mask process to form the gate contact and doped GaN layer and expected success for the same reasons.” Pet. 77–78 (citing Ex. 1003 ¶ 270; Pet. § VIII.A.1.d.ii). For the same reasons set forth above with respect to ground 1, Petitioner fails to sufficiently show a reason a POSITA would have been motivated to modify Hikita-023 in view of Beach. Accordingly, Petitioner fails to show by a preponderance of the evidence that claim 5 would have been obvious over Hikita-023, Beach, and Sheppard.

III. PETITIONER’S MOTION TO EXCLUDE EXHIBIT 2008

Petitioner filed a Motion to Exclude (Paper 25, “Mot.”) Exhibit 2008, which is a hearing transcript from the parallel ITC investigation. Mot. 1. Because we do not rely upon Exhibit 2008 in our Decision, we dismiss Petitioner’s motion as moot.

IV. CONCLUSION

In summary:

Claims	35 U.S.C. §	Reference(s)	Claims Shown Unpatentable	Claims Not Shown Unpatentable
1–3	103	Yoshida, Beach, Sheppard		1–3
1–4	103	Hikita-347, Beach, Sheppard		1–4
5	103	Hikita-023, Beach, Sheppard		5
Overall Outcome				1–5

V. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that Petitioner has not shown by a preponderance of the evidence that claims 1–5 of the ’508 Patent are unpatentable;

FURTHER ORDERED that Petitioner’s Motion to Exclude is dismissed as moot; and

FURTHER ORDERED that because this Decision is final, a party to the proceeding seeking judicial review of the Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

FOR PETITIONER:

Lionel Lavenue
Kara Specht
Cory Bell
Forrest Jones
Chen Zang
Yi Yu
Luke MacDonald
Carlos Duarte-Guevara
FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER LLP
lionel.lavenue@finnegan.com
kara.specht@finnegan.com
cory.bell@finnegan.com
forrest.jones@finnegan.com
chen.zang@finnegan.com
yi.yu@finnegan.com
luke.macdonald@finnegan.com
carlos.duarte-guevara@finnegan.com

FOR PATENT OWNER:

Walter Davis
Dipu Doshi
Mark Thronson
Stephen Soffen
Ameya Paradkar
Jonathan England
BLANK ROME LLP
walter.davis@blankrome.com
dipu.doshi@blankrome.com
mthronson@blankrome.com
ssoffen@blankrome.com
aparadkar@blankrome.com
jwengland@blankrome.com