RAFAEL J. BETANCOURT

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SILICON ARCHITECT | AMS DESIGN & METHODOLOGY EXPERT

AMS Design Expert/Architect with 40+ tapeouts of analog/digital mixed-signal CMOS IC Design experience, directly responsible for the design and mass production of over a billion units. Experienced in complete product lifecycle, from initial conception through design, verification, fabrication & testing.

WORK HISTORY

2019-Present: ***Betasoft Consulting, Inc.***, Santa Clara, CA. Working Silicon – First Time, Every Time.
President, Silicon Architect - Specialized in AMS architecture, debug, modeling & verification. Expert in custom silicon ASIC development. CMOS VLSI Analog IP expert witness, deposition & litigation support.

Major clients include:

- 2022 – Present: ***Applied Materials Inc.***, *Santa Clara, CA* – R&D services for chiplet-based heterogeneous ICs.
- 2021 – Present: ***Palo Alto Electron, Inc.***, *Palo Alto, CA* – R&D services for chiplet-based heterogeneous ICs.
- 2020 – Present: ***Scientific Analog Inc.***, *Palo Alto, CA* – North American distributor for XMODEL CAD software, the most efficient tool available for fast and accurate analog mixed-signal modeling and verification in a purely digital environment using SystemVerilog.
- 2019 – 2022: ***Vidatronic, Inc.***, *Austin, TX* – Analog and mixed-signal design and verification services for power management IPs delivered to multiple clients, including AMD and Mojo Vision.
- 2019 – 2020: ***zGlue Inc.***, *Mountain View, CA* – Architecture, design, and debug of wearable and industrial IoT systems; management consulting services at the level of Sr. Director of Engineering including oversight of the Silicon engineering projects for mm Wave, design and management for Integrated Circuit R&D, technology development of 5G Smart Fabric analog and digital circuit IP including modification of Smart Fabric for customer needs.

2002-2018: ***Synaptics, Inc.***, *San Jose, CA* – a leading manufacturer of human interface sensing devices.

Director, Analog Mixed-signal Systems and Verification (last 4 years)
Hands-on role, responsible for a global team that performs AMS verification of complex capacitive Touch controllers, as well as integrated Touch and LCD Display Controllers (TDDI) for mobile and automotive applications.

- As technical lead for various Discrete/TDDI touch controller chips that have shipped hundreds of millions of units, managed the definition/specification for Touch sensing ASICs: silicon roadmap (MRD/PRD), technology scoping and feasibility studies.
- Established Analog Mixed-signal simulation flow in SYNA and created a "special forces" AMS elite team trained in AMS debug, verification, and modeling. Implemented best practices include Verilog-AMS modeling for functional verification, and the use of SystemVerilog extensions to model voltage/current & charge flow in analog behavioral models running in the digital event-driven simulator (NCSIM, VCS). Collaborated extensively with digital team to integrate SV-based AMS simulations in UVM self-checking environment. Implemented flow in 3 tapeouts and found functional bugs missed by digital DV in one ASIC pre-metal release.
- Worked with System Architects, Digital, Test, and Firmware teams to define complex interface specifications for analog touch and display control logic, and analog DFT.
- Worked closely with Apps, Firmware, and Test teams in NPI/MP of Touch and TDDI controllers. Provide technical support to field teams with RMA, and failure analysis investigations (DOE/DFMEA).

Principal Silicon Architect, Touch – Technical lead for Touchscreen CMOS controllers for mobile, tablet, and notebook PCs. Oversee silicon project definition and execution combining broad technical skills, technical lead skills and people skills to lead a talented interdisciplinary design team.
Sr. Analog Mixed-Signal Design Manager – Managed all ASIC Design (Digital, Analog & Mixed-signal), and grew the team up to 10 full-time IC designers. Assumed management for focused Analog Mixed-signal (AMS) team.

Petitioner Hisense USA Corporation
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Senior Analog IC Design Engineer – Technical lead for various Touch Controller ASICs, responsible for project management: supervised and mentored junior designers and layout/mask design contractors. Designed analog circuits for low-power, low-cost capacitive & resistive sensing ASICs.
Senior Analog IC Design Contractor – Designed analog circuits for low-power, low-cost capacitive and resistive sensing ASICs.

1998-2001: *Innovative Semiconductors, Inc.,* *Mountain View, CA.* – **Sr. Mixed-signal IC Design Engineer**

- **USB 2.0:** Designed 480Mb/s analog transceiver for USB 2.0 including cable driver, receiver, squelch detector, and clock recovery DLL in TSMC's 0.25um and 0.18um CMOS processes. Wrote specifications for 480MHz PLL clock synthesizer and interfaced with PLL design contractor for post-layout verification and performance characterization. Supervised two junior analog designers and layout/mask design contractor.
- **IEEE-1394:** Performed analog verification of 400Mb/s serial transceiver PHY using Mentor's Accusim simulator. Developed scripts in AMPLE to automate analog verification (PVT). Assisted with DRC and LVS of 1394 PHY chip in TSMC's 0.35um CMOS. Bench-tested, troubleshooted, and characterized 1394 PHY. Assisted with porting of IEEE-1394 PHY to UMC's 0.18um CMOS.

1987–1990: Member of the Technical Staff, MTS-I. *Hughes Aircraft Company**, El Segundo, Calif.*

- **Electro-Optical & Data Systems Group.** Performed digital GaAs ASIC design. Responsible for physical design and verification of a 5.2K-gates (41k transistors) 160MHz image processing chip (FIR filter) using Bell Labs' GaAs HEMT technology. This chip was, at the time, the largest and most complex ever to be fabricated in this technology. Contributed to the development of HCAD - a toolset for GaAs LSI and VLSI design. Wrote handbook on GaAs LSI design using HCAD. Contributed to the design effort of a 5k gates GaAs cell array. Performed modeling and simulation of a bipolar switching power supply IC using Analogy's Saber.
- **Industrial Electronics Group***, Torrance, Calif.* Developed millimeter-wave (Ku-Band) Traveling Wave Tube (TWT) amplifiers. Designed and developed tuning fixture for production testing of 94GHz TWT amplifiers. Performed high frequency microwave testing and troubleshooting of TWTs.
- **Radar Systems Group.** Performed technical support for the F-15 radar's APG-70 Transmitter Logic/Synchronizer module. Investigated and solved field problems with the transmitter power supply. Developed fault table for Receiver/Exciter Unit built-in test.

EDUCATION

2005 Engineers Degree in Electrical Engineering (D. Eng.), **Stanford University**, *Stanford, CA.*
- Specialized in VLSI, Analog Mixed-signal & low-power CMOS RF circuits, analog instrumentation, digital architecture. Courses in Engineering Management, Entrepreneurship, and Intellectual Property Law.
- Thesis: *Injection-locked ring oscillator frequency dividers*. Advisor: Thomas H. Lee

1989 MSEE, **University of Southern California**, *Los Angeles, CA*. – Specialized in analog and digital IC design.
1987 BSEE, University of Puerto Rico, *Mayagüez, Puerto Rico*. – Completed a 5-year program in 4 years. Graduated *magna cum laude* with a specialization in electronics.

SELECTED IP EXPERIENCE

Kilpatrick Townsend & Stockton*, Atlanta, GA* [1 case, expert witness]
- Analyzed technical patents and reviewed technical documents to elucidate and explain operation of complex circuits to legal staff.
- Worked closely with attorneys to prepare IPR Petition and supporting Expert Witness Declaration.

Unified Patents, *Chevy Chase, MD* [1 case, expert witness]
- Analyzed technical patents and reviewed technical documents to elucidate and explain operation of complex circuits to legal staff.

- Worked closely with attorneys to prepare an *ex parte* reexamination.

Duane Morris, *Washington D.C.* [1 case, expert witness]

- Analyzed technical patents for infringement and reviewed technical documents to elucidate and explain operation of complex circuits to legal staff.
- Worked closely with attorneys to prepare IPR Petition, wrote and submitted supporting Expert Witness Declaration. Case still pending.

Russ August & Kabat, *Los Angeles, CA*. [2 cases, expert witness]

- Analyzed technical patents for infringement and reviewed technical documents to elucidate and explain operation of complex ICs to legal staff.
- Worked closely with attorneys to prepare for litigation at ITC, wrote patent validity report, was deposed, and produced witness statement. Cases settled before testifying live in Court.
    - *2019 – ITC case number 337-TA-1162 "Certain Capacitive Touch-Controlled Mobile Devices, Computers, and Components Thereof;"*
    - *2020 – ITC case number 337-TA-1193 "Certain Capacitive Touch-Controlled Mobile Devices, Computers, and Components Thereof;"*

Synaptics Inc., *San Jose, CA*. ***Director, Analog Mixed-signal Systems and Verification*** [1 case, fact witness]

- Inventor/co-inventor of three (3) issued patents.
- Evaluated 1000s of Invention Disclosures (IDFs) over 14+ years as ASIC representative to the Corporate IP Committee at the number one Touch company in the world (SYNA).
- Helped defined the corporate IDF process/strategy and helped interview IP engineers, agents, & attorneys.
- *SYNA v. Goodix* – Participated in IP litigation as subject matter expert in a case regarding IP infringement. As technical lead for project using IP being infringed upon, I was deposed by opposing Counsel and testified at ITC Court in Washington D.C. in 2016. Had to review relevant IP (patents) and respond to interrogatory, prepare for deposition, and testified in Court. Case was settled (terms of the settlement are confidential).

Pennie & Edmonds LLP, *Palo Alto, CA*. *IC Design Consultant* [3 cases, expert witness]

- Analyzed technical patents for infringement and reviewed technical documents to elucidate and explain operation of complex digital ICs to legal staff.
- Worked closely with attorneys to prepare for patent application filing and infringement litigation.
- Specialized in all aspects of digital ASIC intellectual property.

SmartPad Inc., *San Francisco, CA*. *Hardware Design Consultant* [1 case, fact witness]

- Material fact witness on lawsuit against SmartPad, deposed by opposing Counsel years after leading the design of a portable battery-operated laptop computer for educational use.
- Found *prior art* in scientific literature that invalidated patent claims. Case settled.

PATENTS

- **"Calibrating Charge Mismatch in a Baseline Correction Circuit,"** US Patent 9,778,804, issued October 3, 2017.
- **"Multi-Step Incremental Switching Scheme,"** US Patent 9,740,351, issued August 22, 2017.
- **"System and method for measuring a capacitance and selectively activating an indicating transducer,"** US Patent 8,058,884, issued November 15, 2011.

SELECTED PUBLICATIONS

- **1-GHz and 2.8-GHz CMOS Injection-locked Ring Oscillator Prescalers,** *Symposium on VLSI Circuits, June 14-16, 2001, Kyoto, Japan.*
- **CMOS VCOs for Frequency Synthesis in Wireless Biotelemetry,** *International Symposium on Low Power Electronics and Design, August 10-12, 1998, Monterey, California.*
- **Low Phase Noise CMOS Ring Oscillator VCOs for Frequency Synthesis,** *2nd International Workshop on Design of Mixed-Mode Integrated Circuits, July 27-29, 1998, Guanajuato, Mexico.*

- **A Low Power Frequency Synthesizer for Wireless Biotelemetry**, *33rd. International Telemetering Conference, October 27-30, 1997, Las Vegas, Nevada.*
- **A 1.5mW, 200MHz CMOS VCO for Wireless Biotelemetry**, *First International Workshop on Design of Mixed-Mode Integrated Circuits and Applications, July 28-30, 1997, Cancun, Mexico.*
- **A High-speed GaAs Transversal Filter Circuit for Clutter Rejection Systems**, SPIE*'s Tech. Symp. Optical Eng. & Photonics in Aerospace Sensing, April 1990.*

SELECTED PROFESSIONAL DEVELOPMENT

- ***Python Programming for Beginners,*** *UC Santa Cruz* – Summer 2020
- ***System and Functional Verification Using UVM,*** *UC Santa Cruz* – Fall 2019
- ***Advanced Verification with SystemVerilog OOP Testbench,*** *UC Santa Cruz* – Summer 2019
- ***Developing the Nanometer ASIC: From Spec to Silicon***, *UC Santa Cruz* – Spring 2019
- ***SystemVerilog Essentials: Functional Verification and Simulation***, *UC Santa Cruz* – Spring 2019
- ***Kepner-Tregoe Decision Analysis Workshop*****,** Santa Clara, CA.
- ***RF IC Design for Wireless Communication Systems*****,** *MEAD Microelectronics*, San Francisco, CA.
- **Presenting Data and Information**, Edward R. Tufte, Palo Alto, CA.
- **Practical Aspects of Analog & Mixed-mode IC Design,** Oregon Center for Advanced Technology Education, Portland State University, Portland, OR.
- **Logic Synthesis 2 Workshop**, Synopsys, Inc., Mountain View, CA.
- **Saber Simulator Training**, Analogy, Inc., Newport Beach, CA.
- **IC Design: Place & Route**, Cadence Design Systems, San Jose, CA.

SELECTED CONSULTING EXPERIENCE

- **Eisenlohr Technologies, Inc.**, Davis, CA. **Hardware Design Consultant, X-Caliper Project** – Product development and design the hardware for X-Caliper, a portable battery-operated instrument used to perform precise measurements of dimensions and angles on X-ray films using MEMs inclinometers. Designed all digital, analog and power supply circuits for X-Caliper.
- **Jefferson Laboratories, Inc.**, Palo Alto, CA. **RF Engineer** – Designed experimental antennas for biotelemetry under a NASA contract for the Rodent Advanced Flight Habitat (RAHF). Fabricated prototypes, tested, and performed experimental research in antennas for biotelemetry under a NASA contract. Assisted in development of biotelemetry antennas for the Rodent Advanced Flight Habitat (RAHF) flown in the Space Shuttle in May 1998.
- **Celeritek, Inc.**, *Santa Clara, Calif.* **Mixed-signal Consultant** – Analyzed erratic behavior of PLL synthesizer and traced problem to noise injection from PIC microcontroller. Reversed engineered firmware to correct offending behavior.
- **SmartPad, Inc.**, *San Francisco, Calif.* **Hardware Design Consultant –** Designed a portable battery-operated laptop computer for educational use. Designed all digital, analog and power supply circuits for PowerPad product based on x86 processor using embedded MS-DOS and Datalight's ROM-DOS.

SELECTED INTERNSHIPS

- **Sun Microsystems Inc.**, Sunnyvale, CA. **Architecture Verification Engineer –** Verified the architecture of the UltraSPARC V.9 64-bit superscalar processor.
- **Silicon Graphics Inc.,** Mountain View, CA**. Digital Verification Engineer –** Verified functionality of a high-performance 80K-gates I/O-DMA controller for R4400 Onyx graphics workstation.
- **Intel Corp.**, Santa Clara, CA. **Micro-architecture Verification Engineer –** Verified the architecture of the Pentium processor using an FPGA Rapid Prototyping System that ran successfully Windows, UNIX and various graphics applications in a PC environment.

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AWARDS & SCHOLARSHIPS

- NASA-Ames Research Center ; Graduate Training Grant 1995-98
- National Consortium for Educational Access, Inc. Fellowship, 1994-97
- General Electric Foundation; Faculty for the Future Fellowship 1993-94
- Hughes Masters' Fellowship; 1987-89
- Tau Beta Pi Engineering Honor Society; 1987
- Phi Kappa Phi National Honor Society; 1986

PROFESSIONAL MEMBERSHIPS & AFFILIATIONS

- IEEE Senior Member
- IEEE Silicon Valley Chapter of the Technology and Engineering Management Society ("TEMS): 2020-21 Chair; 2018-19 Vice-Chair; 2022-23/2017 Secretary; Reviewer for 2019 TEMSCON.
- IEEE Santa Clara Valley Section: 2020 Vice-Chair.
- Member of IEEE Solid-State Circuits & Circuits & Systems societies (reviewer for ISCAS, TCAS-I/II Journals)
- Volunteer at IEEE Global Humanitarian Technology Conference 2018
- Volunteer Judge at International Science & Engineering Fair (ISEF), 7 times