

2/18/85

Row/bar
Backplate

LED
Tile

Hot
Bar
Soldered
Flex
Strip

Power
supply/
Control
PCB

ZIF
connector

ON PCB

Not
on

flex
strip

Power
supply/
Control
PCB

PCB
&
header
strip

Present
standard
connector

on harness/
jumper

White
Registered,
locking

Slim
Edge
Card
Connector

LED
Tile

Row/bar
Backplate

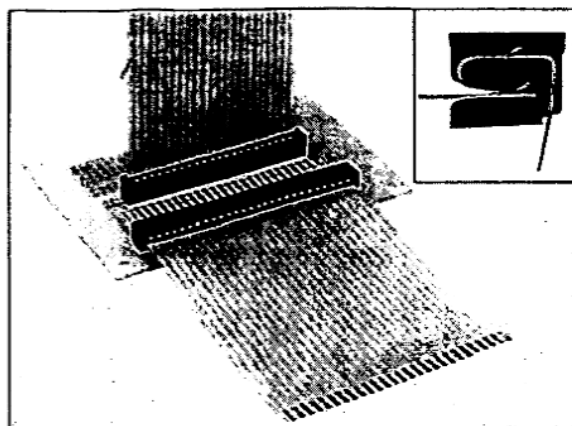
Standard
Pigtail
Wire
Jumper
harness

LEFT

John Kluge to
11/8/2005

2.54mm Pitch Miniature Connector for Flexible Board

FH1 Series



■Features

1. 2.54mm FPC and FFC Connector

The contact pitch is 2.54mm.

2. Contact Reliability

This connector assures high contact reliability for high voltage contact.

3. Eighteen Types of Contact Numbers

This connector consists of 18 kinds of 8, 9, 10, 11, 12, 13, 14, 15, 15, 17, 18, 19, 20, 21, 22, 27, and 29 contacts.

■Applications

HDD, facsimiles, printers, VTR, etc.

■Product Specifications

Rating	Rated Current: 1A Rated Voltage: 200V AC	Operating Temperature Range: -40~+85°C (Note 1) Operating Humidity Range: Relative humidity, 90% max. (Not dewed)	Storage Temperature Range: -10~+60°C (Note 2) Storage Humidity Range: Relative humidity, 90% max. (Not dewed)
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Applicable FPC	t=0.13~0.3 Tin plating
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Item	Specification	Condition
1. Insulation Resistance	5000MΩ min.	Measured at 500V DC
2. Withstand voltage	Neither short or breakdown should occur.	500V AC for 1 minute
3. Contact Resistance	20mΩ max. ※ FPC conductor resistance included	Measured at DC 1A
4. Mechanical operation	Contact resistance: 40mΩ max. No part should be broken, cracked or loosened	30 cycles
5. Vibration	No part should be broken, cracked or loosened	Frequency: 10~55Hz and full amplitude 1.50mm in 3 directions for 2 hours, respectively
6. Shock	No part should be broken, cracked or loosened	Acceleration: 490m/s ² , duration: 11ms, sine half-wave in 3 directions for 3 times, respectively
7. Moisture Resistance in Steady State	Insulation resistance: 500MΩ min.	Exposed to temperature 40°C and humidity 90~95% for 96 hours
8. Temperature Cycle	No part should be broken, cracked or loosened	5 cycles under conditions as follows: Temperature: -55°C→+5~+35~85~+5~+35°C Time: 30~10~15~30~10~15 minutes
9. Resistance to Soldering heat	Neither appearance should be deformed nor contact remarkably loosened.	Automatic soldering: 260°C±5 for 10 seconds

Note 1. Temperature rise included when energized

Note 2. This storage indicates a long-term storage state for the unused product before board mounted.

The operating temperature and humidity ranges are applied to the non-energized state after the connector has been installed in the board.

Note 3. The above standards represent this series. The individual formal agreement should be based on the "Specification".

■Material

Part	Material	Finish	Remarks
Insulator	PBT	Black	UL94V-0
Contact	Phosphor bronze	Tin plating	—

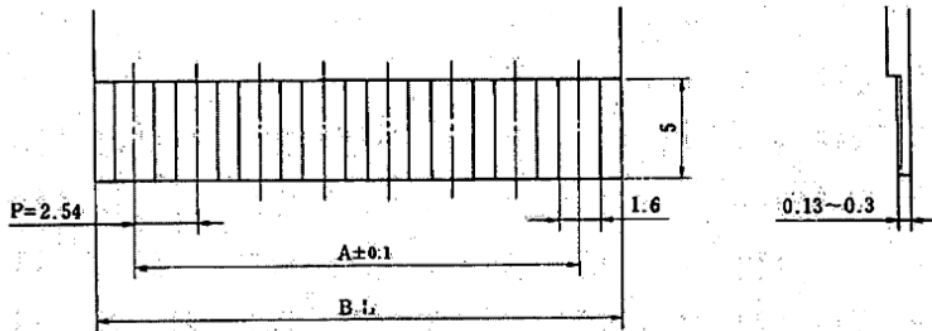
■Ordering Information

Please determine the specific product. If needed, please select and order the product from the product No. as listed on catalog page D4 and D5.

FH 1 - 17 S -2.54 DS
 q w e r t y

q Series Name : FH	r Contact alignment : Single
w Series No. : 1	t Contacts Pitch : 2.54mm
e Number of Contacts : 6, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 27, 29	y Contact Type : DS : Right angle type DSA : Straight type

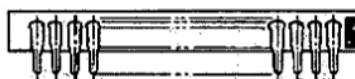
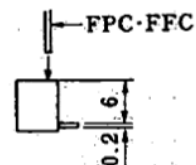
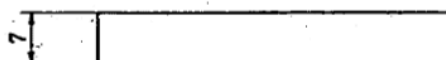
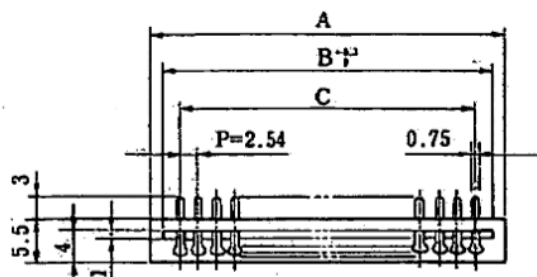
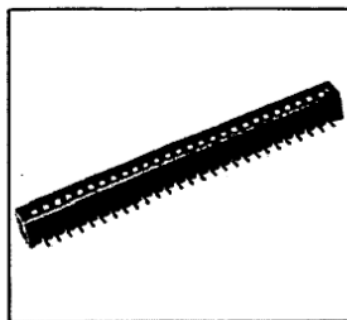
■FPC · FFC Dimensions



Unit: mm

Number of Contacts	5	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	27	29
Size																		
A	10.16	17.78	20.32	22.86	25.40	27.94	30.48	33.02	35.56	38.10	40.64	43.18	45.72	48.26	50.80	53.34	66.04	71.12
B	15.29	22.91	25.45	27.99	30.53	33.07	35.61	38.15	40.69	43.23	45.77	48.31	50.85	53.39	55.93	58.47	69.90	76.25

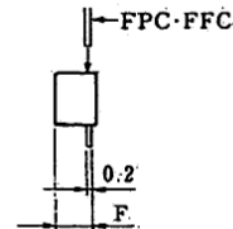
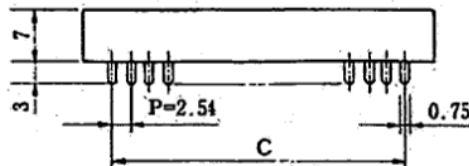
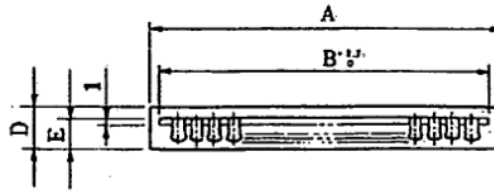
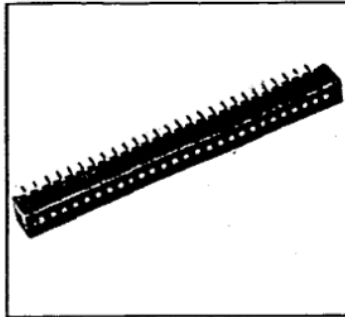
■Right Angle Type



Unit:mm

Product No.	HRS No.	Number of Contacts	A	B	C
FH1- 8S-2.54DS	CL586-0015-5	8	26.0	23.01	17.78
FH1- 9S-2.54DS	CL586-0016-8	9	28.5	25.55	20.32
FH1-10S-2.54DS	CL586-0017-0	10	31.0	28.09	22.86
FH1-11S-2.54DS	CL586-0018-3	11	33.6	30.63	25.40
FH1-12S-2.54DS	CL586-0019-6	12	36.1	33.17	27.94
FH1-13S-2.54DS	CL586-0020-5	13	38.7	35.71	30.48
FH1-14S-2.54DS	CL586-0027-4	14	41.3	38.25	33.02
FH1-15S-2.54DS	CL586-0028-7	15	43.8	40.79	35.56
FH1-16S-2.54DS	CL586-0029-0	16	46.3	43.33	38.10
FH1-17S-2.54DS	CL586-0001-0	17	48.8	45.87	40.64
FH1-18S-2.54DS	CL586-0002-3	18	51.4	48.41	43.18
FH1-19S-2.54DS	CL586-0003-6	19	53.9	50.95	45.72
FH1-20S-2.54DS	CL586-0004-9	20	56.4	53.49	48.26
FH1-21S-2.54DS	CL586-0005-1	21	59.0	56.03	50.80
FH1-22S-2.54DS	CL586-0006-4	22	61.5	58.57	53.34
FH1-27S-2.54DS	CL586-0007-7	27	73.0	70.00	66.04

■Straight Type



Unit: mm

Product No.	HRS No.	Number of Contacts	A	B	C	D	E	F
FH1-5S-2.54DSA	CL586-0036-5	5	18.3	15.39	10.16	5.5	4	4.5
FH1-8S-2.54DSA	CL586-0021-8	8	26.0	23.01	17.78	5.5	4	4.5
FH1-10S-2.54DSA	CL586-0023-3	10	31.0	28.09	22.86	5.5	4	4.5
FH1-11S-2.54DSA	CL586-0024-6	11	33.6	30.63	25.40	5.5	4	4.5
FH1-12S-2.54DSA	CL586-0025-9	12	36.1	33.17	27.94	5.5	4	4.5
FH1-13S-2.54DSA	CL586-0026-1	13	38.7	35.71	30.48	5.5	4	4.5
FH1-14S-2.54DSA	CL586-0030-9	14	41.3	38.25	33.02	5.5	4	4.5
FH1-15S-2.54DSA	CL586-0031-1	15	43.8	40.79	35.56	5.5	4	4.5
FH1-16S-2.54DSA	CL586-0032-4	16	46.3	43.33	38.10	5.5	4	4.5
FH1-17S-2.54DSA	CL586-0008-0	17	48.8	45.87	40.64	5.5	4	4.5
FH1-18S-2.54DSA	CL586-0009-2	18	51.4	48.41	43.18	5.5	4	4.5
FH1-19S-2.54DSA	CL586-0010-1	19	53.9	50.95	45.72	5.5	4	4.5
FH1-20S-2.54DSA	CL586-0011-4	20	56.4	53.49	48.26	5.5	4	4.5
FH1-21S-2.54DSA	CL586-0012-7	21	59.0	56.03	50.80	5.5	4	4.5
FH1-22S-2.54DSA	CL586-0013-0	22	61.5	58.57	53.34	5.5	4	4.5
FH1-27S-2.54DSA	CL586-0014-2	27	73.0	70.00	66.04	5.5	4	4.5
FH1-29S-2.54DSA	CL586-0037-8	29	79.3	76.35	71.12	6.0	4.5	5.0

an lateral caging/prop	Ultrasonic bath clean	Dry	Plasma Clean	F&K 4500 Multi-Dio Mount	WIP Buffer	Stigma Eutopic	Epoxy cure	Plasma Clean	Wirebond	Encap Dispense	Encap Cure	Auto Bt Inspect / Shunt Test	Bin
☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐

2W lateral caging/prop	Ultrasonic bath clean	Dry	Plasma Clean	F&K 4500 Multi-Dio Mount	WIP Buffer	Stigma Eutopic	Epoxy cure	Plasma Clean	Wirebond	Encap Dispense	Encap Cure	Auto Bt Inspect / Shunt Test	Bin
☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐

November 18, 2005

Control Logic Document for the 36 channel PWM supply:

A Microchip PIC18F8722 is used alone to generate 36 digital PWM waveforms (squarewaves). Duty cycle constants are stored in the micro's flash and explicitly represent on percentage times.

One main timing loop is used in the software control code. This loop monitors a main counter which is incremented by one each pass through the loop. The counter counts from 0 to 99 after which it rolls over to zero once again. When the counter is zero all of the PWM channels are set to logic '1'.

Each pass through the loop the counter is compared to individual duty cycle constants in succession, one after the other. If the count value equals the duty cycle constant the corresponding I/O is set to logic '0'.

Within the body of the loop a delay has been added such that the overall PWM period is 5 mS. Thus the PWM frequency is 200 Hz.

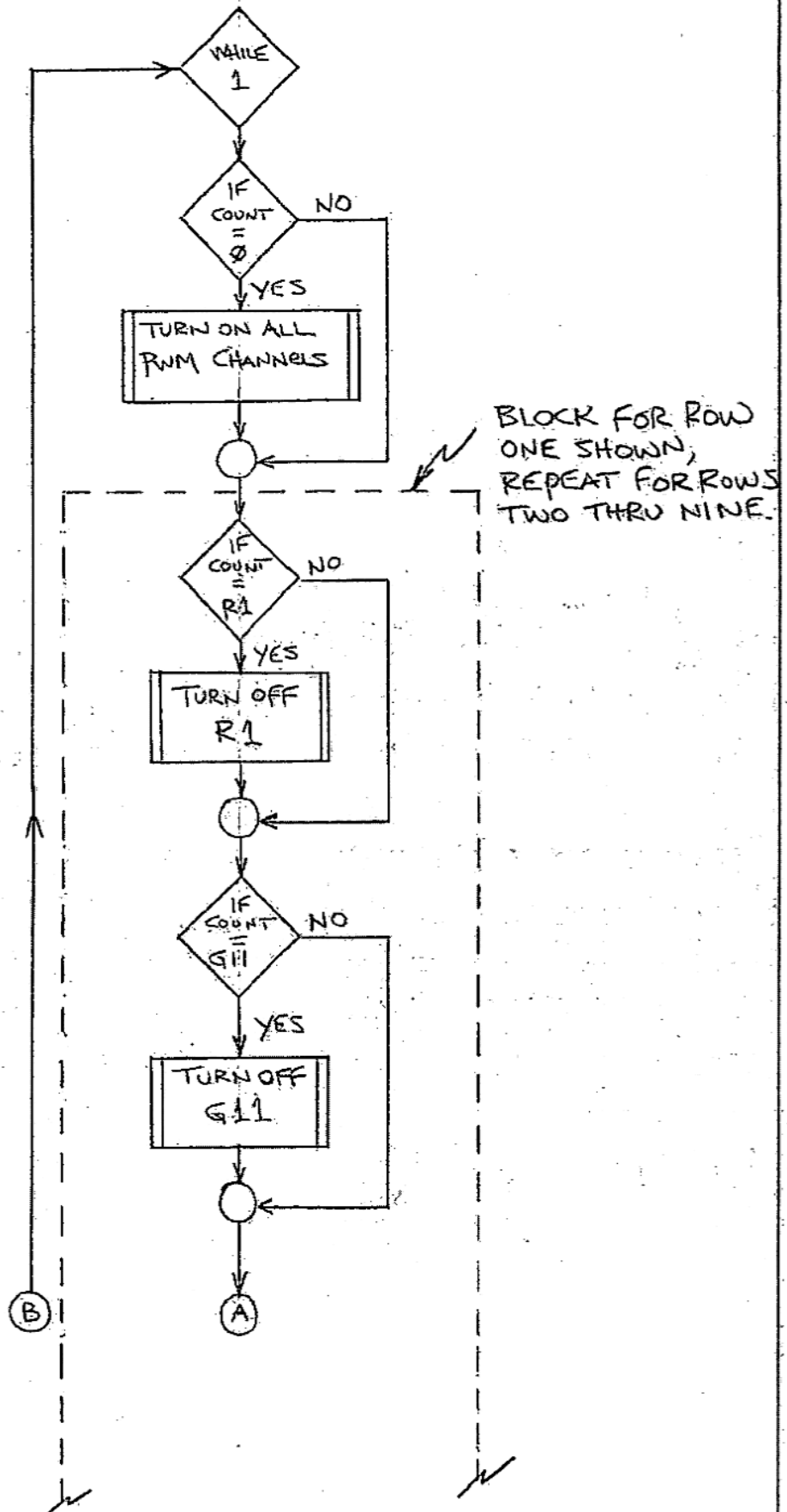
Incorporating the Agilent Color management chipset would be as follow:

The Agilent controller determines what it believes are optimal R, G, and B duty cycled waveforms. Irregardless of the format stored, bit depth, etc... these settings can be resolved as a number from 0 to 100, i.e. a duty cycle in terms of percent 'on'. Not only are these control waveforms generated for external drive purposes they are also retained in the Agilent controller's internal register set. These registers are accessible via I2C. The PIC18F8722 can be configured as an I2C master and by default the Agilent controller is an I2C slave. I am proposing that when the main counter in the 8722 is zero we read the R, G, and B registers from the Agilent controller. An alternative would be to read the analog voltages directly off the sensor head and thus bypass the Agilent controller altogether. After a register read has taken place the individual R, G, and B values can be added to the duty cycle count thresholds as an error term. Scaling of the error term can be applied as well as signing the register values such that this summing function represents an exact implementation of classical feedback control. The feedback element (R, G, and B from Agilent) can be scaled ("P") as mentioned previously. In addition the controller can be implemented such that the feedback elements can be scaled in and integrative ("I") or a derivative ("D") fashion and thus be implemented as a classical PID controller. Of course the feedback elements can be filtered digitally or subsampled, or both in unlimited combinations.

kjv

11/17/05

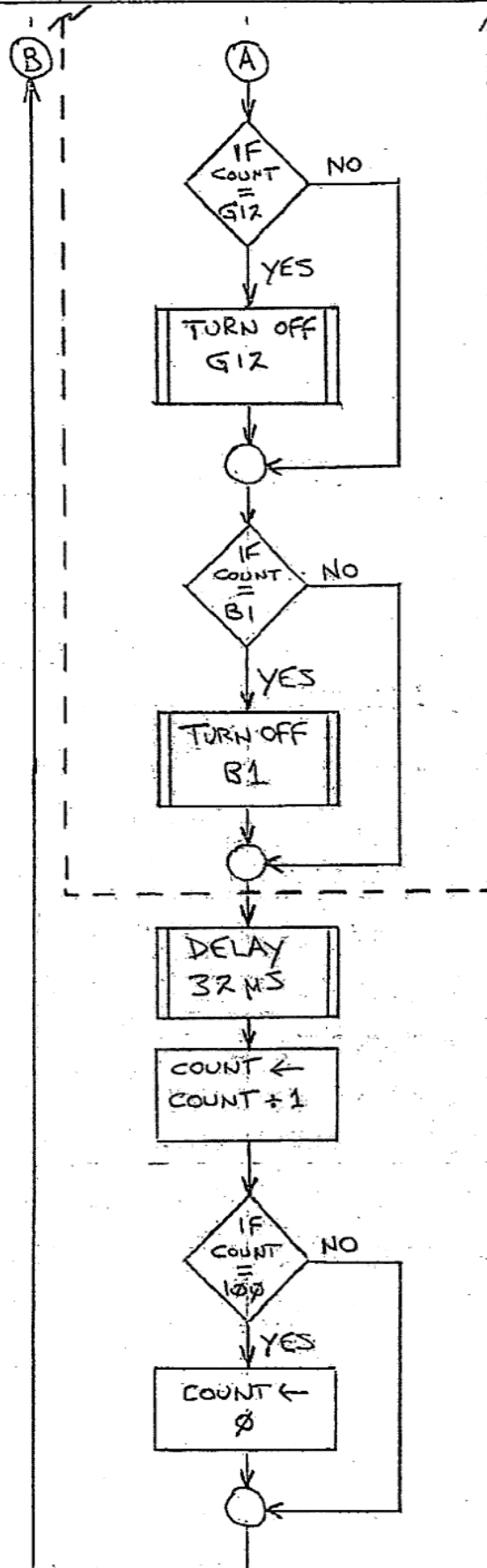
CREE



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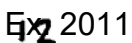
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STAEDTLER[®]
No. 937 811E
Engineer's Computation Pad



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Title		Cree	
Supply Block			
Size	Document Number	Rev	
A			
Date:	Friday November 18, 2005	Sheet	2 of 37
		2	



Cree Inc. - 36 channel PWM Supply

Revised: 11/18/2005 0:00

Bill Of Materials

Item	Board Qty	Ref	Part	PCB	Manf	Part #	Tol	Volt
1	72	C1(A-JJ),C5(A-JJ)	100pF	0805	AVX	08055A101JAT2A	5%	50
2	36	C2(A-JJ)	1uF	1812	AVX	18121C105KAT2A	10%	100
3	0	C3(A-JJ)	DNP	0805	ONP	1/10 Watt	1	
4	36	C4(A-JJ)	47000pF	0805	Panasonic	ECJ-2YB1H473K	10%	50
5	36	C5(A-JJ)	0.1uF	2225	Kemet	C2225C104KCRACU	10%	500V
6	36	C7(A-JJ)	1000pF	0805	AVX	08051A102JAT2A	5%	100
7	36	C8(A-JJ)	0.1uF	0805	AVX	08055C104KAT2A	10%	50
8	36	C9(A-JJ)	0.1uF	1206	AVX	12061C104KAT2A	10%	100
9	36	D1(A-JJ)	MURA130T3	SMA	ON-Semi	MURA130T3		300V
10	72	D2(A-JJ),D3(A-JJ)	1SMB5953BT3	SMB	ON-Semi	1SMB5953BT3		150V
11	18	J1,J2,J3,J4,J5,J6,J7,J8,J9,J10,J11,J12, J13,J14,J15,J16,J17,J18	HEADER 6	1H8PIN 100MIL	Motex	90136-1108		350V, 3A
12	36	L1(A-JJ)	330uH	DO3308	COILCRAFT	DO3308P-334		
13	36	Q1(A-JJ)	IRF3000	SO-8	International Rectifier	IRF3000		300
14	36	Q2(A-JJ)	MMBT2222A	SOT-23	VISHAY	MMBT2222A		40V
15	36	R1(A-JJ)	147K	0805	Panasonic	ERJ-6ENF1473V	1%	
16	36	R2(A-JJ)	10	0805	Rohm	MCR10EZHF10R0	1%	
17	108	R3(A-JJ),R6(A-JJ),R4(A-JJ)	10K	0805	Panasonic	ERJ-6ENF1002V	1%	
18	72	R5(A-JJ),R10(A-JJ)	1K	0805	Panasonic	ERJ-6ENF1001V	1%	
19	18	R7B,R7C,R7F,R7G,R7J,R7K,R7N,R7O, R7R,R7S,R7V,R7W,R7Z,R7AA,R7DD, R7EE,R7HH,R7II	RlimB, 33	1206	Yageo	9C12063A33R0FKHFT	1%	
20	36	R8(A-JJ)	100	0805	Panasonic	ERJ-6ENF1000V	1%	
21	36	R9(A-JJ)	301	0805	Panasonic	ERJ-6ENF3010V	1%	
22	36	R11(A-JJ)	21K	0805	Panasonic	ERJ-6ENF2102V	1%	
23	36	R12(A-JJ)	0.2-1W	2010	VISHAY	WSL2010R2000FEA18	1%	
24	36	U1(A-JJ)	LM5020-1	MSOP-10	National Semiconductor	LM5020-1		
25	9	R7A,R7H,R7L,R7P,R7T,R7X,R7BB,R7 FF,R7JJ	RlimB, 54.9	1206	Yageo	9C12063A54R9FKHFT	1%	
26	9	R7D,R7E,R7F,R7G,R7H,R7I,R7J,R7K, C,R7GG	RlimB, 30.9	1206	Yageo	9C12063A30R9FKHFT	1%	

990

1	PCB	PCB		PCB		
1	Tooling cost					
1	Assembly cost					

Notes:	
A,B,C,D,E,F,G,H,I,J,K,L, M,N,O,P,Q,R,S,T,U,V,W, X,Y,Z,AA,BB,CC,DD,EE, FF,GG,HH,II,JJ	
Component order:	
RlimB is 30.9 ohm for Red, 33 ohm for both Greens, and 54.9 ohm for Blue	
(A-JJ) indicates 36 components, in order listed above	

V-I Adaptive Colorwave Illumination Tile Disclosure

Each Colorwave tile comprises one or more multi-chip arrays of 2 or more LED chips connected in series mounted upon a substrate such as a ceramic tile, MCPCB or other substrate with good thermal conductivity, high temperature resistance, high thermal stability, resistance to change in humidity and other laudable characteristics needed for high performance, high efficiency, high reliability LED light engines. These substrates are typically fashioned into circuits from combinations of dielectric and conductive materials by additive or subtractive processes. Appropriate circuits on such substrates can be obtained from Berquist, BNI, Opulent, IRC and others to name a few. Suitable GaN-based LED chips can be obtained from Cree, Inc. and suitable AlInGaP/InGaAlP LED chips can be obtained from UEC, Epistar, Lumileds and Osram to name a few.

In a preferred Colorwave tile, there are 4 or 8 independent strings of LED chips, each consisting of 4 or 8 LED chips connected in series. For the present invention, it is best to first focus upon only 1 string of 4 LED chips in series. A significant challenge presented for commercial viability of tiles containing series combinations of 4 LED's in series relates to the variation in Voltage-Current characteristics exhibit by the population of LED chips available for making such tiles.

It is not uncommon for the Vf GaN based LEDs of a given variety to vary by as much as ± 0.75 volts from a nominal Vf at a standardized current such as 20 mA. If such LEDs are used to produce strings of 4 in series, the accumulated variance in Vf at the standardized current of 20 mA can add up to as much ± 3.0 volts across a population of modules. If the nominal Vf is typically 3.2 volts $\times$ 4 chips in series = 12.8 volts, then the ± 3.0 volts string Vf variance represents close to $\pm 25\%$ of the total string Vf. The power supply for the string must accommodate this variance in some way, to avoid large differences in current from one module to the next. Specifically, the power supply for each string must constitute an independent current-control circuit. In the absence of this, the Vf variance will result in current variance from tile to tile. Since current is highly proportional to light output in a well designed LED module, variances in current on the order of more than 5% will result in unacceptable variances in light output from string to string and module to module.

To manage this Vf variance and eliminate the current variances that would result if external

High reliability, low cost electrical interconnects for dual or multisubstrate LED illumination sources. John Roberts. 11/15/2005

→ A high reliability, low cost electrical interconnect is needed to establish electrical continuity across a gap in a circuit that exists between any two substrates of a dual or multisubstrate LED illumination system when the two substrates bear portions of the circuit that need to be electrically joined for the circuit to function properly. This might be the case, for example, if the two substrates are multichip LED module tiles such as Colowave Illuminator tiles and comprising a plurality of LED dice or chips mounted on a circuit board substrate and wirebonded or otherwise disposed in a fashion to allow current to flow through one or more of the LED chips when the tile is energized. Such LED illuminator tiles may be as disclosed in previously filed patents by Cree Inc. In the present invention, the tiles further comprise 2 or more pads in electrical communication with one or more of the LED chips through circuit traces or vias or other means, such that when a sufficient forward bias voltage potential is induced at the 2 pads, current flows through at least one chip causing it to emit radiation. If this radiation is visible, IR or UV, we may still refer to it as illumination.

By placing such tiles serially in a circuit and interconnecting them, chips on more than one tile may be illuminated simultaneously, provided ample voltage potential is applied at the extreme electrical poles of the combined tile pair. With additional interconnections, more tiles may be "stacked" in electrical series and substantially adjacent in space, and they'll all illuminate when energized upon application of sufficient potential. This configuration has many advantages in the way it facilitates the construction of a wide variety of distributed illumination sources from a single tile design that is compact, standard & simple. Such a distributed EX-2011 Illumination source bears

John K Roberts 11/19/2005

11/18/05 John Green

The advantage of spreading emitted light quite directly and efficiently over the large areas typically need for backlit LCD display panels, for backlit signage, and for office illumination. To name a few applications. This distributed architecture also provides for the wide and uniform distribution of dissipated heat, directly and without excessive additional thermal distribution means. Typically, if the circuit substrate is of MCPCB (metal core/clad printed circuit board) or heavy clad (4 or copper or more) conventional FR-4 with thermal vias, then the distributed light source may be mounted on an aluminum backplate or clad an isotropic carbon backplate — and no other major thermal dissipation or spreading means will be needed in a system (especially not fans). But a challenge with this architecture is that the distributed light source of interconnected tiles may be subject to stress & strain including flexure induced during assembly into a display product or subsystem, or induced by differences in the product/subsystem structure itself over time, especially during contraction or expansion induced by cooling and heating. Additionally, the distributed light source with interconnections may need to be large relative to the size of each interconnected tile (or some of them), such as when the tiles are small and the source is large in area, or both. In this case, a large # of interconnects may be needed between tiles to complete all the requisite circuits. This in turn poses several problems including systemic cost of interconnects and probability of a partial system fault due to failure of one or more interconnect. Thus, the interconnect must most preferably be inexpensive to make, must be robust with respect to temperature cycling and attendant expansion/contraction cycles, must accommodate loads and flexure without failing too readily, and must be otherwise compatible with the tile and the system the tiles go into. The interconnect must also establish

John K Roberts 11/15/2003 JKR to Gnu 11/15/03

and maintain a low resistance electrically continuous interface through normal product life exposures. In many applications, the interconnect must be very low profile protruding very little above the plane of the tiles upon which the LED's are mounted, so as not to interfere with optical performance of the LED chips or other components of the system (reflector sheets, for example).

In one embodiment of the present invention, the interconnects are "large wire" Aluminum wirebonds established by ultrasonic wedgebonding. This embodiment enjoys advantages of extremely rugged, reliable, inexpensive interconnects that can be made at high speed on automated machinery (such as from a machine maker like F&K Delovette).

All wirebonds for .008" and .012" aluminum wire on gold pads on the tiles have been demonstrated to have pull strengths in excess of 500 gm and wedge shear strengths in excess of 1000 gm. Another advantage of this system is that the bonds are made ultrasonically, without any external heat applied to the tile. In some configurations this is very useful as the tile may comprise sensitive materials like optical encapsulants or die attach epoxies or phosphors or other media that could be damaged upon excessive application of heat for interconnect processing. These bonds, while strong, are also relatively small, such that the pads on the tile may be made relatively small also, preserving space on the tile. This in turn may allow for greater spacing between pads without an overall increase in pad footprint (across all pads on a tile). Greater spacing, it should be understood, between tiles may be beneficial when adjacent pads on the tile are intended to carry large differentials in potential, in which case greater separation enabled by small interconnects and pads allows for greater isolation of insulation and helps to prevent unintended current paths (shorts or partial shorts) between pads, that might otherwise occur with humidity, salt exposures, moisture,

John K Roberts 11/15/2005 ~~John Kraus~~ 11/18/05

solvent accumulations or the invasion of biological matter onto the surface between pads, with such greater spacing, and for extreme electrical isolation between adjacent pads on a tile, slots could in fact be employed, greatly increasing the effective path length for a would-be short and thus increasing the effective dielectric strength between pads throughout the tile life. Also, the relatively small wire sizes of 'large wire' At wire bond interconnects can, when coupled with the very high bonding speeds of automated wedge bonders, allow for 2 or more bonds to be placed in a redundant fashion where there would otherwise be only one interconnect. This can increase reliability and durability of the distributed lightsource built from tiles quite substantially at low overall cost. The loop height for these interconnects can also be quite low, reaching no more than .020" in some cases, or .015" or .012" in other cases above the plane of the tiles upon which the LEDs are mounted (and/or upon which the interconnect pads are formed and interconnects are bonded).

By adjusting the loop height of these bonds, one may adjust their ability to accommodate expansion and contraction between tiles and flexure at the gap between tiles. As long as the loop height is less than the spacing between adjacent, independent, interconnects (or $\frac{1}{2}$ that spacing to be sure), the system can tolerate great strain/deflection/deformation in the manner of chain mail armor, but without adjacent wires interconnects making contact/short between one another. In the case of redundant double/triple/quadruple bonds on one set of pads forming one interconnect, of course, contact among the redundant wires would be immaterial. Another advantage of this interconnect embodiment is that it does not require lead

John K. Ranta 11/15/2005 Read & Understood
John Gurn 11/15/05

on other hazardous materials (such as in some solder-based systems) and also does not generally require reaction fluxes (which can become agents of damage on the tiles if present and not removed).

Many similar advantages can be delivered through use of a second, low-cost, high reliability, flexure-accommodating, expansion/contraction resilient, environmentally sensitive, highly automatable and optionally redundant tile to tile electrical interconnect system for hybrid multichip LED illumination modules in a distributed lighting subsystem... gold ribbon wire bonding. Almost everything

else is the same as with the large wire Au embodiment, except for the small size, and rectangular section of the interconnect wires in this embodiment. The wire may be 1 to 3 mils (.001" to .003") in height and from .005" to .015" in width, giving a rectangular section, for this Au ribbon version of the invention. Other differences in process and automated machinery may include a need for some heat application to the substrate when using the ribbon, as may be understood by those skilled in the art. Also, the Au ribbon is a little more costly, but may be more robust in certain caustic environments, may in some cases offer a lower loop height & may allow for closer pad spacing due to the lack of propensity for the rectangular-section wire to "sweep" or sway in a direction transverse to the progression of the interconnect axis. Those skilled in the art may realize that some of the same benefits and others may be garnered by substitution of different wire compositions including elements on alloys chosen from the list of all metals, carbon, silicon, phosphorus, etc or a number of different sizes or section shapes, or different bond pads in the... Ex. 204 composition, shape, size, etc.

John K. Roberts 7/15/2005

11/18/05 John Kearns

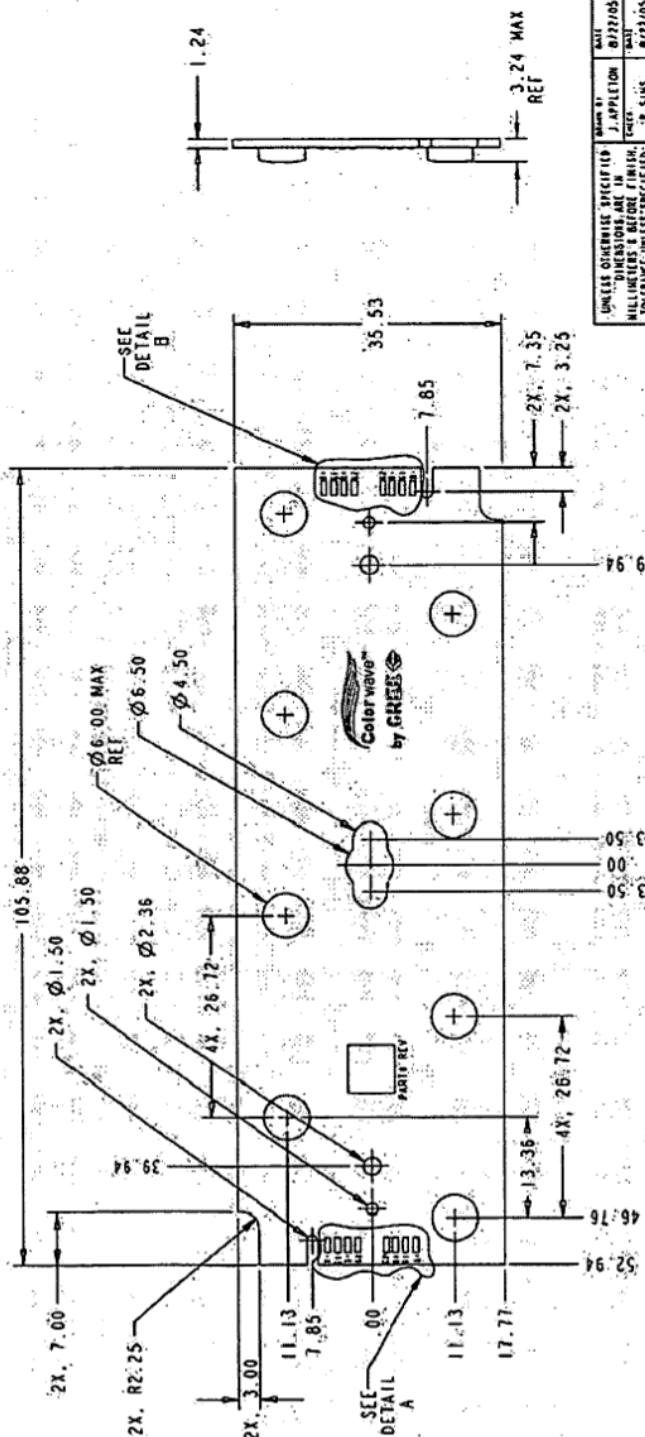
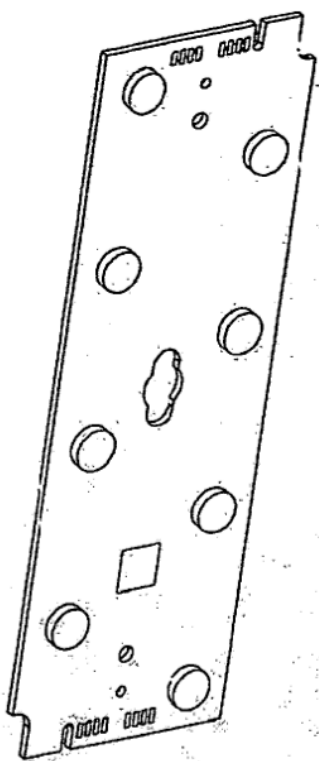
departing from the scope of the present invention.
 A process for employing the disclosed
 interconnect scheme in a cost effective
 manner and a consistent, high quality, low
 labor manner may consist of placing or
 feeding the substrate tile onto an aluminum
 backplate using digital or hand automation
 and/or registration fixture pins through the
 aluminum backplate and the tile, the aluminum
 backplate further comprising an interface adhesive
 (such as a thin acrylic PSA such as 3M VHB
 Series tapes @ .005" or less or 3M 4905 or similar
 Adhesives Research products) or a liquid-dispensed
 interface (such as RTV or other adherent or
 thermal interface). Once the tile is placed
 and settled, then the registration pins may
 be retracted, ~~and/or the tile lifted (picked) for~~
 allowing the aluminum backplate to be indexed
 along by an interval such as an even multiple
 of the tile length v. lth. (such as $\times 1.01$), and
 then allowing extension of the registration
 pins again through the aluminum backplate
 and then registered placement of the next
 tile of the bar down over the registration pins,
 the registration pins protruding through both
 the aluminum backplate and tile through the
 holes there intended for registry. This sequence
 may be repeated to sequentially register
 and affix tiles on the aluminum backplate
 strip to form a bar bearing a plurality of
 tiles in intervals that are regular. This
 bar may then be transferred and fed into
 a large wire Aluminum wedge bonder (or ribbon
 bonder for Au ribbon) to automatically bond
 from pad to pad across the gap between tiles
 on the bar. This completes the circuits running
 across & through the tiles and interconnects on
 the bar. The holes in the bar & tiles may
 be used to grip, propel and register the bar
 as it is indexed through the wire bonder. The
 bar stops momentarily such that the bonder can
 make the interconnect across tile boundaries.
 1. The Al. interconnect. 2041 the. h. ... an o. concluded.

John K Roberts 11/15/2005

John Gann 11/15/05

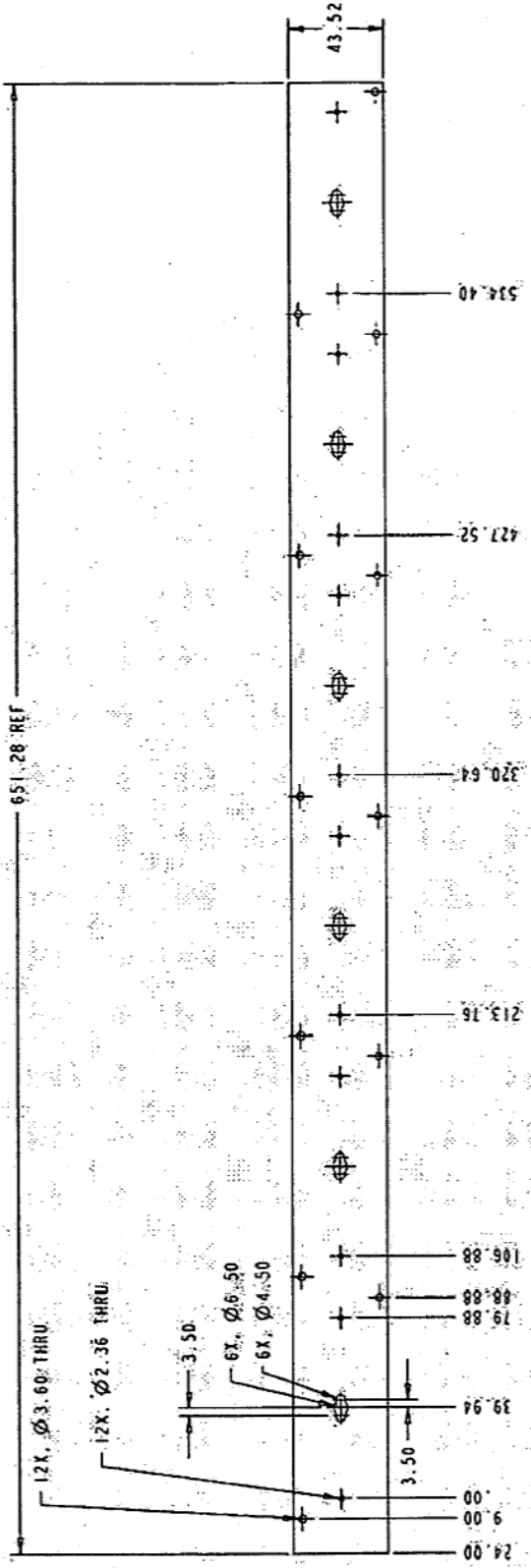
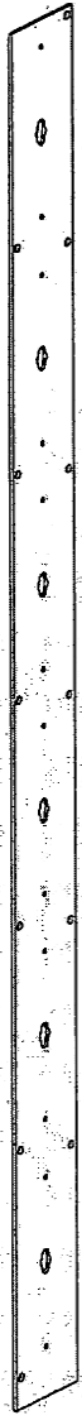
The bar is indexed out of the interconnect wirebender. The bar may then be picked up placed into a backlight cover bottom plate using a similar technique to the one used for placing tabs on a bar. The cover bottom plate may have an anisotropic expanded graphite thermal spreader such as those known as SpreaderShield and available from Brightec of Cleveland, Ohio

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REV	DESCRIPTION	INVENTOR	BY	DATE	APP'D
A	INITIAL RELEASE			8/25/05	P. SINGH
B	REVISED FOR CREE			11/7/05	A. LIN



CREE

4000 Silicon Drive
Folsom, CA 95630
TEL: 916.353.2000 FAX: 916.353.2100

MSO COLORWAYS

BAR - BOTTOM LAYOUT

DATE: 11/7/05
BY: J. APPLIN
CHECK: P. SINGH
DATE: 8/25/05

DATE: 11/7/05
BY: A. LIN
CHECK: P. SINGH
DATE: 8/25/05

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4368.00 4416.00 4464.00 4512.00 4560.00 4608.00 4656.00 4704.00 4752.00 4800.00 4848.00 4896.00 4944.00 4992.00 5040.00 5088.00 5136.00 5184.00 5232.00 5280.00 5328.00 5376.00 5424.00 5472.00 5520.00 5568.00 5616.00 5664.00 5712.00 5760.00 5808.00 5856.00 5904.00 5952.00 6000.00 6048.00 6096.00 6144.00 6192.00 6240.00 6288.00 6336.00 6384.00 6432.00 6480.00 6528.00 6576.00 6624.00 6672.00 6720.00 6768.00 6816.00 6864.00 6912.00 6960.00 7008.00 7056.00 7104.00 7152.00 7200.00 7248.00 7296.00 7344.00 7392.00 7440.00 7488.00 7536.00 7584.00 7632.00 7680.00 7728.00 7776.00 7824.00 7872.00 7920.00 7968.00 8016.00 8064.00 8112.00 8160.00 8208.00 8256.00 8304.00 8352.00 8400.00 8448.00 8496.00 8544.00 8592.00 8640.00 8688.00 8736.00 8784.00 8832.00 8880.00 8928.00 8976.00 9024.00 9072.00 9120.00 9168.00 9216.00 9264.00 9312.00 9360.00 9408.00 9456.00 9504.00 9552.00 9600.00 9648.00 9696.00 9744.00 9792.00 9840.00 9888.00 9936.00 9984.00 10032.00 10080.00 10128.00 10176.00 10224.00 10272.00 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DATE: 11/7/05
BY: J. APPLIN
CHECK: P. SINGH
DATE: 8/25/05

DATE: 11/7/05
BY: A. LIN
CHECK: P. SINGH
DATE: 8/25/05

6061 ALUMINUM

FOR SHEET METAL PARTS ONLY

THIRD ANGLE PROJECTION

ARclad® 7761

Double-Coated Film

Features

- High-shear acrylic adhesive
- Polyester film
- Densified kraft liner

Benefits

- Outstanding temperature and chemical resistance (gasoline, motor-oil, antifreeze, and brake fluid)
- Easy to die cut and apply

Applications

Excellent choice for assembly of electronic and electrical equipment. Bonds well to engineering plastics and metals.

Storage and Shelf Life

One year when stored at 70°F, 50% R.H.

Product Construction

Composite:

Liner:

Total:

Typical Values

3.5 mils

3.2 mils

6.7 mils nominal

Test Methods

PSTC-33, ASTM D-1000

Adhesive Properties - Typical Values

180° Peel Adhesion/12" min.

5 min./SS - 40oz./in.

Test Methods

PSTC-3, ASTM D-3330, ART #1005

Static Shear

Temperature:

72°F

Area

1/2" x 1/2"

Load

500 g.

Minutes to Failure

150 min.

Test Methods

PSTC-7, ART #1011

Recommended Minimum Application Temperature:

50°F (10°C)

Maximum Operating Temperature:

350°F (177°C)

APPLICATION AND STORAGE OF PRESSURE-SENSITIVE ADHESIVE TAPES

Pressure-sensitive adhesive tapes function as a mechanical product; however, the adhesive itself is a chemical composition that can be sensitive to environmental conditions. A purchaser of pressure-sensitive adhesive products should be aware of the shelf life of each product and not purchase more than it can use before the expiration date. Shipping and storage conditions affect shelf life. The optimum storage temperature is 70°F (21°C). Cool, dry storage is recommended.

For best results:

- 1.) The surfaces you wish to bond should be clean and free of oil, moisture and dust. If the surface temperature is below 40°F, it may be difficult to achieve a proper bond.
- 2.) Do not use a pressure-sensitive adhesive product where it will be exposed to temperatures lower or higher than those designated for each product. Heat can destroy the effectiveness of the bond and extreme cold can cause the adhesive to harden and not adhere properly.
- 3.) When the tape is applied, use firm hand or lamination pressure to achieve contact between the adhesive and the surface to which it is applied. Handrollers or nip rollers may be needed for certain products or applications.

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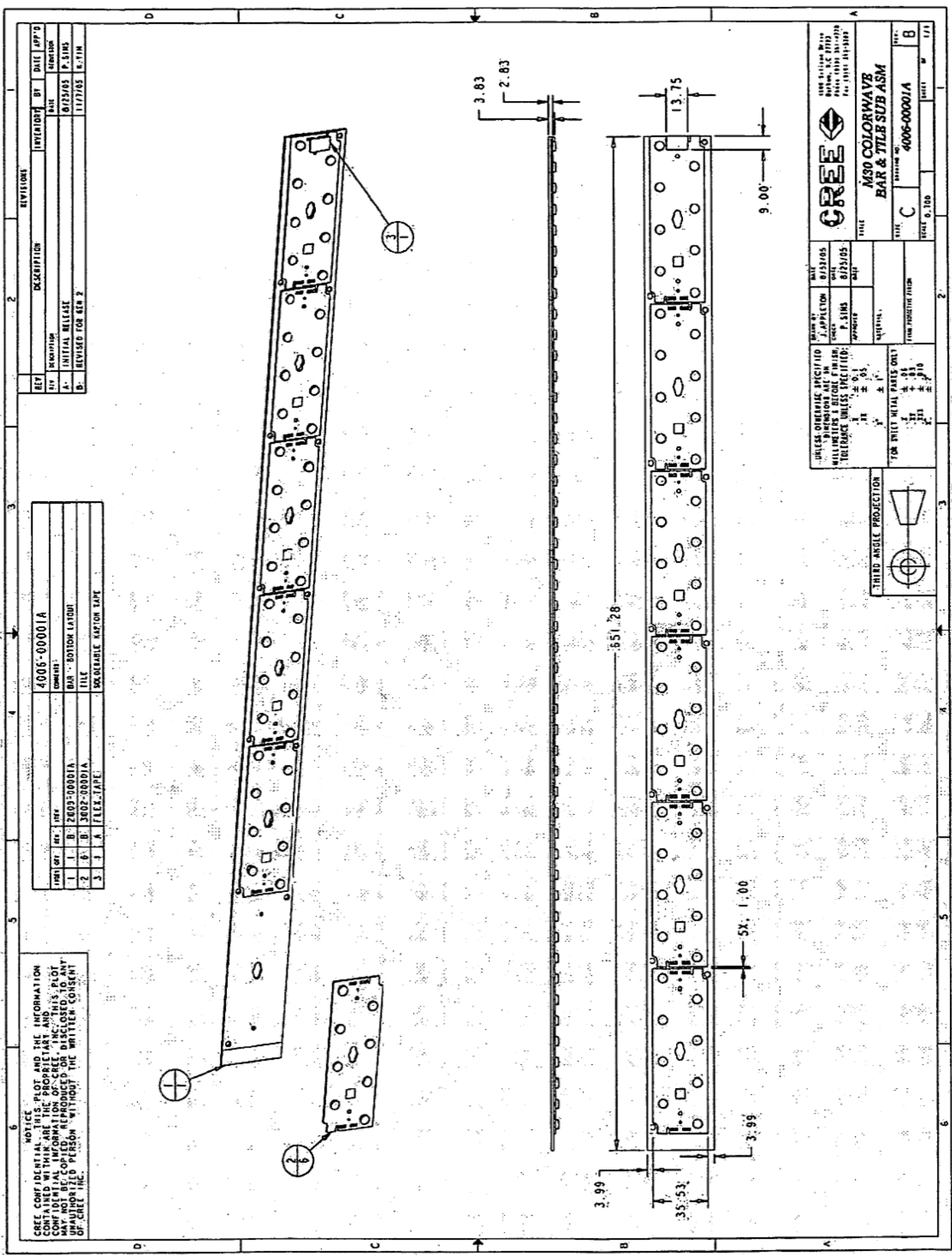
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1	1	B	2605-00001A
2	6	B	3002-00001A
3	1	A	FILE-TAPE

REV.	DATE	BY	DESCRIPTION
A	0/25/05	P. SIMS	INITIAL RELEASE
B	1/17/05	R. TIM	REVISED FOR REV 2

CREE

1906 SULLY BLVD
PHOENIX, AZ 85041-3400
TEL: (602) 972-1000

**M30 COLORWAYS
BAR & TILE SUB ASM**

DATE: C
REV: B
SCALE: 0.100

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1 ± 0.1 2 ± 0.1 3 ± 0.1	TYP. TOLERANCE FRACTION		

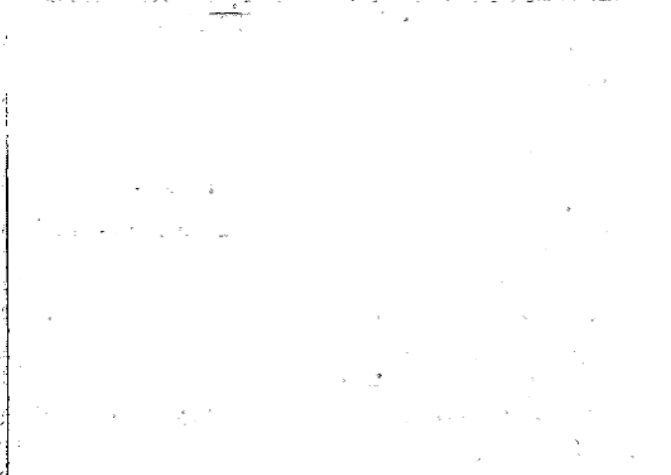
THIRD ANGLE PROJECTION

eGRAF[®] SpreaderShield[™] Thermal Solutions

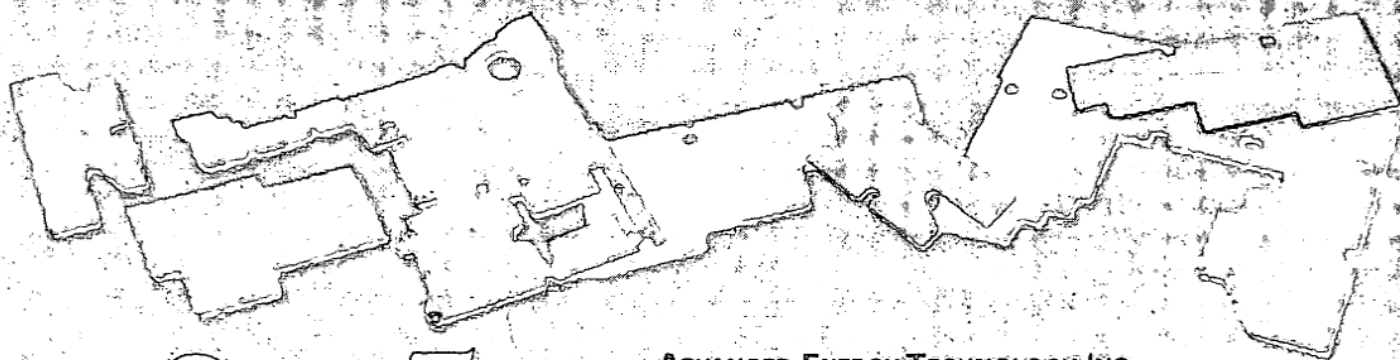
- ☐ A graphite based thermal solution that can be combined with plastics, metals or elastomers in the finished components.
- ☐ Distributes heat evenly in two dimensions, eliminating "hot spots" while simultaneously reducing touch temperature in the third dimension.
- ☐ Custom designed thermal properties, tailorable up to 500 W/m²K, and form factors to meet your needs.
- ☐ Available with adhesive backing for simple "peel and stick" use.
- ☐ Ideally suited where lightweight is critical and space for a cooling solution is limited.
- ☐ Typical applications include: laptop computers, flat panel displays, digital video cameras, cell phones and PDA's.



Thermal Image of a Laptop PC Left Palm Rest and Touchpad, average palm rest temperature 42.0 °C.



Thermal Image of a Laptop PC Left Palm Rest and Touchpad with eGraF SpreaderShield Thermal Solution, average palm rest temperature 34.5 °C.

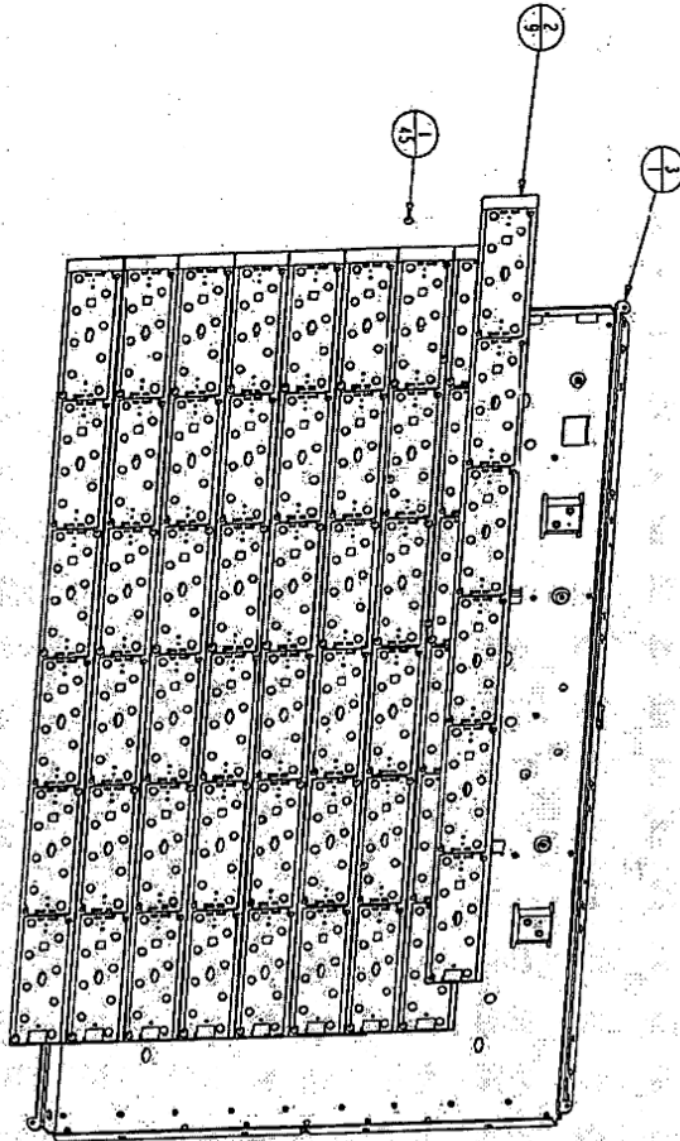


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A Graftech International Ltd. Company
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3	1	1M30W02-CB-051114	

CREC

CREC, INC.
10000 Highway 100
Suite 100
Dallas, TX 75243
Tel: 972-381-1000
Fax: 972-381-1001

MSO COLORWAYS

COVER BOTTOM GROUP

Part: 5009-00001A

Rev: B

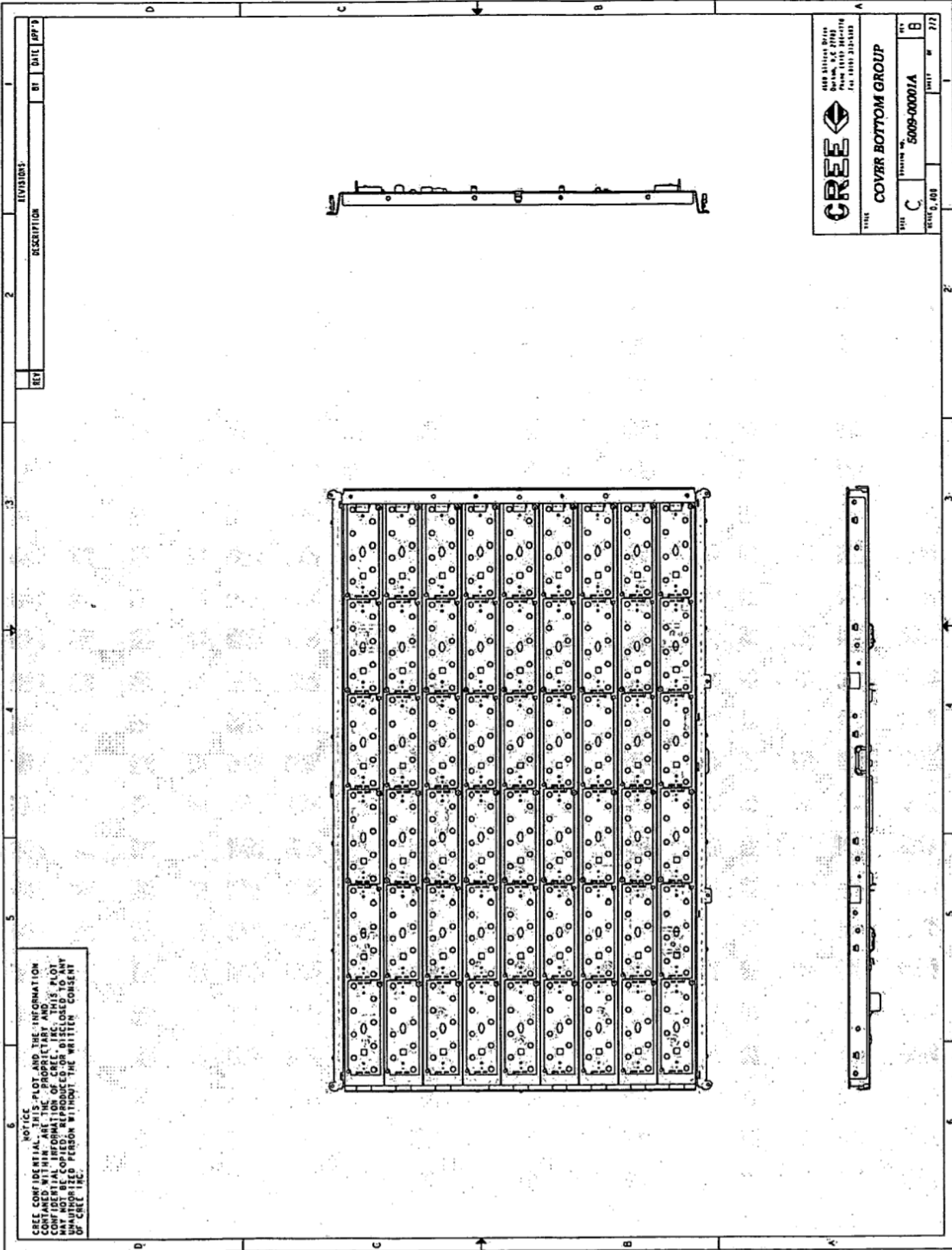
THIRD ANGLE PROJECTION

FOR SCREW METAL TRAYS ONLY

DATE: 8/15/05
DRAWN BY: J. APPELBO
CHECKED BY: P. SHER
TOLERANCE: UNLESS SPECIFIED
DIMENSIONS: SEE DRAWING

Scale: 1/2" = 1'-0"

Sheet: 1 of 1



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