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Sir:

Transmitted herewith for filing under 37 CFR § 1.53(b) is:
☒ a patent application
☐ a Continuation ☐ a Divisional ☐ a Continuation-in-Part (CIP) Application of prior application no.:_____; filed _____, the disclosure of which is incorporated herein by reference in its entirety.
☐ and claims the benefit of Provisional Application No._____ ; filed _____ .

Inventor(s) or Application Identifier:
John Roberts; Keith Vadas

Entitled: **SYSTEMS AND METHODS FOR CONTROLLING A SOLID STATE LIGHTING PANEL**

Correspondence Address: **Customer No. 65106**
Myers Bigel Sibley & Sajovec, P.A.
P. O. Box 37428
Raleigh, North Carolina 27627
Telephone: (919) 854-1400
Facsimile: (919) 854-1401

Attached (or filed concurrently herewith) are:
1. ☒ Application Transmittal Letter and Fee Transmittal Form.
2. ☒ **38** pages of Specification (including **55** claims)
3. ☒ **12** sheets of Formal Drawings (35 USC 113)
4. ☐ Oath or Declaration
   a. ☐ newly executed *(copy)*
   b. ☐ copy from prior application (37 CFR 1.63(d) *(for continuation/divisional)* **[Note Box 6 Below]**
   c. ☐ DELETION OF INVENTOR(S) *(Signed statement deleting inventor(s) named in the prior application)*
5. ☐ Application Data Sheet. See 37 CFR 1.76
6. ☐ Incorporation By Reference *(useable if box 4b is checked)*
   The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
7. ☐ Microfiche Computer Program *(Appendix)*
8. ☐ Applicant claims small entity status. See 37 CFR § 1.27.
9. ☐ Information Disclosure Statement, listing of references, and 0 references cited.

10. ☐ Preliminary Amendment *(Please enter all claim amendments prior to calculating the filing fee.)*
11. ☐ English Translation Document
12. ☐ Certified Copy of _____ Application will follow by mail.
13. ☐ Sequence Listing/ Sequence Listing Diskette will follow by mail.
14. ☐ Deletion of Inventors(s) (Signed statement attached deleting inventor(s) name in the prior application. See 37 CFR 1.63(d)(2) and 1.33(b).
15. ☐ Nonpublication Request under 35 U.S.C. 122(b)(2)(B)(i). Applicant must attach form.
16. ☐ Other:

The fee has been calculated as shown below:

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FILING FEE			$ 75.00	$300.00
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Timothy J. Wall
Registration No. 50,743

CERTIFICATION OF TRANSMISSION

I hereby certify that this correspondence is being transmitted via the Office electronic filing system in accordance with § 1.6(a)(4) to the U.S. Patent and Trademark Office on May 8, 2007.

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SYSTEMS AND METHODS FOR CONTROLLING A SOLID STATE LIGHTING PANEL

FIELD OF THE INVENTION

[0001] The present invention relates to solid state lighting, and more particularly, controlling a solid state lighting panel.

BACKGROUND

[0002] Solid state lighting arrays are used for a number of lighting applications. For example, solid state lighting panels including arrays of solid state lamps have been used as direct illumination sources, for example, in architectural and/or accent lighting. A solid state lamp may include, for example, a packaged light emitting device including one or more light emitting diodes (LEDs). Inorganic LEDs typically include semiconductor layers forming p-n junctions. Organic LEDs (OLEDs), which include organic light emission layers, are another type of solid state light emitting device. Typically, a solid state light emitting device generates light through the recombination of electronic carriers, i.e. electrons and holes, in a light emitting layer or region.

[0003] Solid state lighting panels are commonly used as backlights for small LCD display screens, such as LCD display screens used in portable electronic devices. In addition, there has been increased interest in the use of solid state lighting arrays for backlights of larger displays, such as LCD television displays.

[0004] For smaller LCD screens, backlight assemblies typically employ white LED lamps that include a blue-emitting LED coated with a wavelength conversion phosphor that converts some of the blue light emitted by the LED into yellow light. The resulting light, which is a combination of blue light and yellow light, may appear white to an observer. However, while light generated by such an arrangement may appear white, objects illuminated by such light may not appear to have a natural coloring, because of the limited spectrum of the light. For example, because the light may have little energy in the red portion of the visible spectrum, red colors in an object

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may not be illuminated well by such light. As a result, the object may appear to have an unnatural coloring when viewed under such a light source.

[0005] The color rendering index of a light source is an objective measure of the ability of the light generated by the source to accurately illuminate a broad range of colors. The color rendering index ranges from essentially zero for monochromatic sources to nearly 100 for incandescent sources. Light generated from a phosphor-based solid state light source may have a relatively low color rendering index.

[0006] For large-scale backlight and illumination applications, it is often desirable to provide a lighting source that generates a white light having a high color rendering index, so that objects and/or display screens illuminated by the lighting panel may appear more natural. Accordingly, such lighting sources may typically include an array of solid state lamps including red, green and blue light emitting devices. When red, green and blue light emitting devices are energized simultaneously, the resulting combined light may appear white, or nearly white, depending on the relative intensities of the red, green and blue sources. There are many different hues of light that may be considered "white." For example, some "white" light, such as light generated by sodium vapor lamps, may appear more yellowish, while other "white" light, such as light generated by some fluorescent lamps, may appear more bluish in color.

[0007] Solid state lamps, such as LED's, are current-controlled devices in the sense that the intensity of the light emitted from an LED is related to the amount of current driven through the LED. One common method for controlling the current driven through the solid state lamps to achieve desired intensity and color mixing is a Pulse Width Modulation (PWM) scheme. PWM schemes pulse the solid state lamps alternately to a full current "ON" state followed by a zero current "OFF" state. However, firing all of the solid state lamps simultaneously may result in undesirable electrical power system performance due, for example, to power factor spikes and/or electromagnetic interference due to the associated current rush. Sequentially firing the strings independently and/or in combinations without regard to relative string location within the display, however, can produce undesirable display characteristics.

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SUMMARY

[0008] In some embodiments, the control system may include firing logic that may determine a firing order of the multiple strings. In some embodiments, the control system may be configured to drive the multiple strings or portions thereof in a spatially non-adjacent, non-sequential or spatially random firing order. In some embodiments, the control system may be configured to drive the multiple strings or portions thereof at different times and/or phases for at least some of the multiple strings or portions thereof. In some embodiments, the control system is configured to drive the multiple strings and/or portions thereof at least partially based on the spatial relationship between the multiple strings or portions thereof and at different phases for at least some of the multiple strings or portions thereof. In some embodiments, the firing logic may include rule-based logic that may operate to generate a non-spatially-sequential firing order. In some embodiments, the rule-based logic may include a rule that a second string fired after a first string is non-adjacent the first string. In some embodiments, the rule-based logic may further include a rule that a first string is fired simultaneously with a second string and the first string is non-adjacent the second string.

[0009] A lighting panel system includes multiple strings of solid state lighting devices arranged linearly across the panel in a first direction and positioned at intervals in a second direction that is substantially orthogonal to the first direction. The system also includes a current supply circuit that can selectively supply multiple on-state drive currents to the multiple strings in response to control signals. The system further includes a control system that can selectively provide control signals to the current supply circuit to selectively drive the multiple strings. The control system can include firing logic that can determine a firing order of the multiple strings.

[0010] In other embodiments, the firing logic can include rule-based logic that can operate to generate a non-spatially-sequential firing order. The rule-based logic can include a rule that a second string fired after a first string is non-adjacent the first string. The rule-based logic can also include a rule that a first string is fired simultaneously with a second string and the first string is non-adjacent the second string.

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[0011] In further embodiments, the lighting panel can include multiple bars that extend across the panel in the first direction and are positioned adjacent one another in a substantially parallel arrangement, such that the bars each include some of the multiple strings. In some embodiments, the firing order can cause a first firing, a second firing and a third firing, which each can supply current in a string in each of the first bar, the second bar, and the third bar, where the second bar is below the first bar and the third bar is above the second bar. In other embodiments, first and second portions of the strings can include solid state lighting devices that emit light in a first dominant wavelength and a second dominant wavelength, respectively, where each of the bars includes at least one string of the first portion and at least one string of the second portion and the strings in the first portion are fired in the firing order and then the strings in the second portion are fired in the firing order. In yet other embodiments, at least one string of the first portion can be fired simultaneously with at least one string from the second portion.

[0012] Other embodiments can include a first portion of strings in a first bar and a second portion of strings in a second bar where the first and second portions are fired sequentially in the firing order and the firing order determines the location of the second bar in response to the location of the first bar.

[0013] In further embodiments, a first portion of the strings includes solid state lighting devices that emit light in a first dominant wavelength and a second portion of strings includes solid state lighting devices that emit light in a second dominant wavelength, where the first portion is fired in the firing order and then the second portion is fired in the firing order.

[0014] In yet further embodiments, the firing logic can be random logic that can operate to generate the firing order.

[0015] In other embodiments, a means for generating a feedback signal is included to provide display performance information to the control system.

[0016] Some embodiments can include methods of controlling a solid state lighting panel having multiple strings of solid state lighting devices configured to extend from a first edge of the panel to a second edge of the panel in substantially adjacent positions relative to one another. Such

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methods can include supplying pulsed drive currents to the strings in a non-spatially-sequential firing order.

[0017] In some embodiments, the firing order can be determined to supply current to a first string and second string, where the second string can be defined based on the location of the first string. In some embodiments, the second string can be defined by selecting a string that is non-adjacent the first string and/or selecting a string that is located a minimum quantity of strings from the first string. In other embodiments, a third string that is fired after the second string can be defined based on the locations of the first and second strings. In some other embodiments, the second string can be defined by selecting a string on a first side of the first string and the third string can be defined by selecting a string on a second side of the second string.

[0018] In further embodiments, multiple portions of the strings can be grouped on multiple bars that can extend across the panel from the first edge to the second edge and that are positioned adjacent one another in a substantially parallel arrangement. In yet further embodiments, the portion of strings in the same bar can be supplied current simultaneously. In other embodiments, a random number can be generated, a value can be assigned to each bar and current can be supplied to the portion of strings on a bar based on the random number.

[0019] In yet other embodiments, a first portion of strings that includes solid state lighting devices configured to emit light in a first dominant wavelength can be supplied current according to the firing order and then a second portion of strings that includes solid state lighting devices configured to emit light in a second dominant wavelength can be supplied current according to the firing order.

[0020] In further embodiments, defining the second string and/or third string can be based on a dominant wavelength emitted by the solid state lighting devices in the first string.

[0021] In yet further embodiments, a first string having solid state lighting devices configured to emit light in a first dominant wavelength and a second string having solid state lighting devices configured to emit light in a second dominant wavelength can be simultaneously supplied current.

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[0022] Other embodiments can include determining the firing order that supplies current to a first string and a second string and defining the second string based on a dominant wavelength of the first string and a relative position of the first string.

[0023] Yet other embodiments can include defining the firing order using numerical techniques. Using a numerical technique in some embodiments can include generating a random number, assigning a value to each of the strings and supplying current to one of the strings based on the value of the random number. In some other embodiments, using a numerical technique can include performing a non-linear calculation.

[0024] In further embodiments, the firing order can include using a deterministic order based on at least one rule.

[0025] A lighting panel system that includes multiple strings of solid state lighting devices that are arranged to extend across the panel in a first direction and are positioned adjacent one another in a second direction and that are supplied current by multiple current drivers can also include a controller that provides control signals to the current drivers and a sequence generator that generates a firing sequence for firing the multiple strings.

[0026] In some embodiments, the sequence generator can include a deterministic algorithm that determines a location of a subsequently fired string from the location of a previously fired string.

[0027] In other embodiments, the sequence generator can include an algorithm that generates a firing sequence to fire a first string having solid state lighting devices that emit light in a first dominant wavelength and a second string having solid state lighting devices that emit light in a second dominant wavelength, where the second string is fired after the first string.

[0028] In yet other embodiments, the sequence generator can include an algorithm that generates a sequence to simultaneously fire a first string having solid state lighting devices that emit light in a first dominant wavelength and a second string having solid state lighting devices that emit light in a second dominant wavelength.

[0029] In further embodiments, the sequence generator can generate a random sequence of firing.

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[0030] Yet further embodiments can include bars that include portions of the strings and extend across the panel in the first direction and are positioned adjacent one another in the second direction. Some embodiments can include a firing sequence that is configured to simultaneously fire a first portion of the strings and then a second portion of the strings where the first portion is located on a first bar and the second portion is located on a second bar. Other embodiments can include a firing sequence that simultaneously fires a first string on a first bar and a second string on a second bar. In some embodiments the first string can include solid state lighting devices that emit light in a first dominant wavelength and the second string can include solid state lighting devices that emit light in a second dominant wavelength.

[0031] Yet other embodiments can include a first portion of strings that include solid state lighting devices that emit light in a first dominant wavelength and a second portion of the strings that include solid state lighting devices that emit light in a second dominant wavelength where each of the bars includes at least one string of the first portion of strings and at least one string from the second portion of strings. In further embodiments, the firing sequence can be operative to cause the first portion of strings to fire in a first sequence and then to cause the second portion of strings to fire in the first sequence.

BRIEF DESCRIPTION OF THE DRAWINGS

[0032] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this application, illustrate certain embodiment(s) of the invention.

[0033] Figure 1 is a block diagram illustrating an overview of systems and methods for controlling a solid state lighting panel in accordance with some embodiments of the invention.

[0034] Figure 2 is a block diagram illustrating a front view of a solid state lighting panel according to some embodiments of the invention.

[0035] Figure 3 is a block diagram illustrating a front view of a solid state lighting panel having lighting bars according to some embodiments of the invention.

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[0036] Figure 4 is a block diagram illustrating a front view of a lighting bar as illustrated in Figure 3 according to some embodiments of the invention.

[0037] Figure 5 is a block diagram illustrating a lighting tile according to some embodiments of the invention.

[0038] Figure 6 is a block diagram illustrating a light emitter cluster according to some embodiments of the invention.

[0039] Figure 7 is a schematic diagram of a lighting tile illustrated in Figure 5 according to some embodiments of the invention.

[0040] Figure 8 is a block diagram illustrating systems and methods for controlling a solid state lighting panel in accordance with some embodiments of the invention.

[0041] Figure 9 is a block diagram illustrating systems and methods for controlling a solid state lighting panel in accordance with other embodiments of the invention.

[0042] Figure 10 is a block diagram illustrating systems and methods for controlling a solid state lighting panel using a multiple phase power supply in accordance with some embodiments of the invention.

[0043] Figures 11A and 11B illustrate a timing diagram and a corresponding graph of a dynamic power load, respectively, for systems and methods of using a single phase power supply for controlling a solid state lighting panel in accordance with some embodiments of the invention.

[0044] Figures 12A and 12B illustrate a timing diagram and a corresponding graph of a dynamic power load, respectively, for systems and methods of using a multiple phase power supply for controlling a solid state lighting panel in accordance with some embodiments of the invention.

[0045] Figures 13A and 13B illustrate a timing diagram and a corresponding graph of a dynamic power load, respectively, for systems and methods of using a multiple phase power supply for controlling a solid state lighting panel in accordance with some embodiments of the invention.

[0046] Figure 14 is a block diagram illustrating systems and methods for controlling a solid state lighting panel synchronized with an LCD display in accordance with other embodiments of the invention.

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[0047] Figure 15 is a flow diagram illustrating operations for controlling a solid state lighting panel synchronized with an LCD display in accordance with other embodiments of the invention.

[0048] Figure 16 is a flow diagram illustrating operations for controlling a solid state lighting panel according to some embodiments of the invention.

[0049] Figure 17 is a flow diagram illustrating operations for controlling a solid state lighting panel according to other embodiments of the invention.

[0050] Figure 18 is a flow diagram illustrating operations for controlling a solid state lighting panel according to further embodiments of the invention.

[0051] Figure 19 is a flow diagram illustrating operations for controlling a solid state lighting panel according to yet further embodiments of the invention.

[0052] Figure 20 is a table illustrating an exemplary string firing sequence according to some embodiments of the invention.

DETAILED DESCRIPTION OF EMBODIMENTS OF THE INVENTION

[0053] Embodiments of the present invention now will be described more fully hereinafter with reference to the accompanying drawings, in which embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. Like numbers refer to like elements throughout.

[0054] It will be understood that, although the terms first, second, etc. may be used herein to describe various elements, these elements should not be limited by these terms. These terms are only used to distinguish one element from another. For example, a first element could be termed a second element, and, similarly, a second element could be termed a first element, without departing from the scope of the present invention. As used herein,

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the term "and/or" includes any and all combinations of one or more of the associated listed items.

[0055] It will be understood that when an element such as a layer, region or substrate is referred to as being "on" or extending "onto" another element, it can be directly on or extend directly onto the other element or intervening elements may also be present. In contrast, when an element is referred to as being "directly on" or extending "directly onto" another element, there are no intervening elements present. It will also be understood that when an element is referred to as being "connected" or "coupled" to another element, it can be directly connected or coupled to the other element or intervening elements may be present. In contrast, when an element is referred to as being "directly connected" or "directly coupled" to another element, there are no intervening elements present. It will also be understood that when a first element, operation, signal, and/or value is referred to as "responsive to" another element, condition, signal and/or value, the first element, condition, signal, and/or value can exist and/or operate completely responsive to or partially responsive to the other element, condition, signal, and/or value.

[0056] The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of the invention. As used herein, the singular forms "a", "an" and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms "comprises" "comprising," "includes" and/or "including" when used herein, specify the presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof.

[0057] Unless otherwise defined, all terms (including technical and scientific terms) used herein have the same meaning as commonly understood by one of ordinary skill in the art to which this invention belongs. It will be further understood that terms used herein should be interpreted as having a meaning that is consistent with their meaning in the context of this specification and the relevant art and will not be interpreted in an idealized or overly formal sense unless expressly so defined herein.

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[0058] The present invention is described below with reference to flowchart illustrations and/or block diagrams of methods, systems and computer program products according to embodiments of the invention. It will be understood that some blocks of the flowchart illustrations and/or block diagrams, and combinations of some blocks in the flowchart illustrations and/or block diagrams, can be implemented by computer program instructions. These computer program instructions may be stored or implemented in a microcontroller, microprocessor, digital signal processor (DSP), field programmable gate array (FPGA), a state machine, programmable logic controller (PLC) or other processing circuit, general purpose computer, special purpose computer, or other programmable data processing apparatus such as to produce a machine, such that the instructions, which execute via the processor of the computer or other programmable data processing apparatus, create means for implementing the functions/acts specified in the flowchart and/or block diagram block or blocks.

[0059] These computer program instructions may also be stored in a computer readable memory that can direct a computer or other programmable data processing apparatus to function in a particular manner, such that the instructions stored in the computer readable memory produce an article of manufacture including instruction means which implement the function/act specified in the flowchart and/or block diagram block or blocks.

[0060] The computer program instructions may also be loaded onto a computer or other programmable data processing apparatus to cause a series of operational steps to be performed on the computer or other programmable apparatus to produce a computer implemented process such that the instructions which execute on the computer or other programmable apparatus provide steps for implementing the functions/acts specified in the flowchart and/or block diagram block or blocks. It is to be understood that the functions/acts noted in the blocks may occur out of the order noted in the operational illustrations. For example, two blocks shown in succession may in fact be executed substantially concurrently or the blocks may sometimes be executed in the reverse order, depending upon the functionality/acts involved. Although some of the diagrams include arrows on communication paths to

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show a primary direction of communication, it is to be understood that communication may occur in the opposite direction to the depicted arrows.

[0061] Some embodiments of the invention may arise from the recognition that where emitter strings in a panel are fired in a spatially sequential order, a noticeable "sweep" or "waterfall" across the display may result. This effect can be more exaggerated at a beat frequency that is related to the difference between the refresh frequency of the panel and the pulse-width-modulation (PWM) frequency of a pulse-width modulation signal used to adjust the brightness of the display. Accordingly, some embodiments establish a non-spatially sequential firing order to avoid or reduce the formation of a "sweep" across the panel. A lighting panel system can utilize a control system that selectively provides control signals to selectively drive the strings in the panel. Some embodiments can use firing logic to determine a firing order in a deterministic manner. Other embodiments can include a sequence generator that generates a firing sequence. Some embodiments can include a polyphase power supply configured to provide power to emitter strings in a temporally distributed manner. Some embodiments include receiving a synchronizing signal from a display controller. Moreover, in some embodiments, the subsequent firing of a string can be determined by the location and/or dominant wavelength of a previously fired string. In this manner, a noticeable "sweep" effect can be reduced.

[0062] Reference is now made to Figure 1, which is a block diagram illustrating a high level view of systems and methods for controlling a solid state lighting panel in accordance with some embodiments of the invention. A solid state lighting panel 102 can be driven by a current driver 104 that is configured to provide current to light emitting devices in the lighting panel 102. Control of the display can be achieved by controlling the current provided by the current driver 104, which is responsive to control signals generated by a controller 106. The controller 106, in conjunction with a color management unit 108, can perform the processing tasks necessary to generate the control signals for the current driver 104. The color management unit 108 and/or the controller 106 can use, for example, performance data from display performance feedback sensors 110 and user input 112 to achieve the desired display performance.

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[0063] Reference is now made to Figure 2, which is a block diagram illustrating a front view of a solid state lighting panel 200 according to some embodiments of the invention. The lighting panel 200 includes multiple strings 204 of solid state lighting devices 206. Although discussed in the context of strings 204, embodiments of the systems and methods herein may include firing modules and/or groups of modules of solid state lighting devices 206 that are not arranged as strings. In some embodiments, a string 204 may be defined by the electrical and/or the spatial relationship between the solid state lighting devices 206 therein. The strings 204 can be generally arranged to extend across the panel 200 in a first direction 214 from a first edge 210 to a second edge 212. The strings 204 can be positioned at intervals along a second direction 216. In some embodiments the strings 204 can be positioned substantially parallel to one another. In some other embodiments the first direction 214 can be substantially orthogonal to the second direction 216. The strings 204 can include electrical connection components 208 for providing electrical connectivity to an electrical power source. In some embodiments, the solid state lighting devices 206 are connected in an electrical series configuration to form each string 204. The electrical series configuration permits the solid state lighting devices in any string to be controlled together through electrical current regulation. Although not shown, some embodiments can include strings 204, or portions thereof, having solid state lighting devices 206 that are connected in an electrically parallel configuration where the string 204 can be controlled through, for example, voltage regulation.

[0064] Reference is now made to Figure 3, which is a block diagram illustrating a front view of a solid state lighting panel 300 having bars 302 according to some embodiments of the invention. In some embodiments, the bars 302 can extend across the panel 300 in a first direction 314 and be positioned adjacent one another in a second direction 316. Each bar 302 can include one or more strings 304 of solid state lighting devices 306 that can be, for example, connected in series. The strings 304 can include electrical connection components 308 for providing electrical connectivity to an electrical power source. The electrical power source can be current and/or voltage regulated, depending on the configuration of the strings. A solid state

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lighting panel of some embodiments can include bars 302 that are vertically oriented and/or arranged in a variety of row and column configurations. Moreover, bars can be configured in a combination of different sizes and/or shapes within the same panel 300.

[0065] Reference is now made to Figure 4, which is a block diagram illustrating a front view of a bar 402 according to some embodiments of the invention. In some embodiments, a bar 402 can include multiple strings 404A-C that can each include multiple solid state lighting devices 406A-C. Each string 404 can be configured to be substantially the same or each one can differ in one or more ways. In some embodiments, each string 404A-C includes solid state lighting devices 406A-C that emit light in a different dominant wavelength. For example, solid state lighting devices 406A can be configured to emit light having a dominant wavelength generally corresponding to the color red. Similarly, solid state lighting devices 406B and 406C can be configured to emit light having dominant wavelengths corresponding to the colors green and blue, respectively. A bar 402 of some embodiments can include one and/or more strings 404 having solid state lighting devices 406 of different colors. For example, a bar 402 can include at least one string 404 having red solid state lighting devices, at least one string 404 having green solid state lighting devices, and at least one string 404 having blue solid state lighting devices. In this manner, by selectively controlling the amount and/or duty cycle of current supplied to each string, the color hue and/or brightness of the light emitted by the bar can be controlled. The strings 404A-C can be controlled independent of one another or as a group corresponding to the bar 402. Although discussed with reference to solid state lighting devices configured to emit light having different dominant wavelengths, the systems and methods herein may also be utilized in systems using solid state lighting devices configured to emit light in a single dominant wavelength. Furthermore, systems, etc., may use solid state LED's including phosphors that, when energized, emit light having multiple wavelengths and/or that otherwise emit broad spectrum light. such as, for example, a phosphor coated blue LED.

[0066] Reference is now made to Figure 5, which is a block diagram illustrating a tile 502 according to some embodiments of the invention.

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Multiple tiles 502 can be connected to form a bar. The tile 502 can include a first group of strings 504 and a second group of strings 505, each including multiple light emitter clusters 506. As illustrated in Figure 6, which is a block diagram illustrating a light emitter cluster 506 according to some embodiments of the invention, a light emitter cluster 506 can include multiple solid state light emitters 508A-D. The solid state light emitters 508A-D can each emit light in a different dominant wavelength. For example, the solid state emitter cluster 506 can include a red emitter 508A, a first green emitter 508B, a second green emitter 508C and a blue emitter 508D. other colors of emitters and/or color combinations may be used.

[0067] As illustrated in Figure 5, current can be conducted to the strings through contacts 510. For example, any one or more of the first group of strings can be fired through the first group supply current contacts 512 and the first group return current contacts 513. Similarly, any one or more of the second group of strings 505 can be fired through the second group supply current contacts 515 and the second group return current contacts 514.

[0068] Reference is now made to Figure 7, which is a schematic diagram of a tile as discussed above regarding Figure 5 according to some embodiments of the invention. The tile 502 includes the first group of strings 504A-D having corresponding current supply and return contacts 512A-D and 513A-D, respectively. Each string 504 can include solid state lighting devices 508 configured to emit light in a dominant wavelength. For example, string 504A can include red emitters 508A. Other strings can include emitters configured to emit light in different dominant wavelengths or colors. In some embodiments a group of strings 504 can include one or more strings having red emitters 508A, one or more strings having green emitters 508B, 508C, and one or more strings having blue emitters 508D. In some embodiments, the first group of strings 504 can be arranged to include the emitter string anodes 512 on the same side of the bar 502 as the emitter string cathodes 514 of the second group of strings 505.

[0069] Reference is now made to Figure 8, which is a block diagram illustrating systems and/or methods for controlling a solid state lighting panel in accordance with some embodiments of the invention. A control system 800 selectively provides control signals to a current driver 808 or other type of

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electrical power supply circuit that responsively drives multiple solid state lighting devices in a solid state lighting panel 810. The control system 800 can include firing logic 802 that can determine a firing order for the multiple strings. A firing order may determine an order in which individual strings of solid state lighting devices and/or groups of strings of solid state lighting devices are supplied current. In some embodiments, the firing order may determine the order in which strings are fired within a single phase of a power supply. In the single phase context, the temporal delay between firing consecutively fired strings may be on the order of, for example, several microseconds. In some embodiments, the firing order may determine the firing order of strings supplied power from different phases of a polyphase power supply. In the polyphase context, the temporal delay between firing strings using consecutive power supply phases may be on the order of, for example, milliseconds.

[0070] One common method for controlling the current driven through the strings is a Pulse Width Modulation (PWM) scheme. PWM schemes pulse the solid state lamps alternately to a full current "ON" state followed by a zero current "OFF" state. The output of the string may be controlled by varying the duty cycle, which is the percent of the cycle that the string is placed in an "ON" state.

[0071] In some embodiments, the firing logic 802 can include rule-based logic that can generate a non-spatially-sequential firing order. For example, the rule based logic may include a rule that a second string fired after a first string is not adjacent the first string in the panel 810. In some embodiments, a rule may be that the first and second strings can be fired simultaneously and are not adjacent one another.

[0072] In some embodiments, the solid state lighting panel 810 can also include multiple bars, as discussed above regarding Figure 3, that can extend across the panel in a first direction and that can be positioned adjacent one another in a substantially parallel arrangement. The firing order can be operative to fire different strings based on the location of the bar that the strings are in. For example, the firing order may be such that each subsequently fired string is located in a bar on a different side of the previously fired string. For example, where first, second, and third strings are

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fired sequentially, the second string can be in a bar below that of the first string and the third string can be in a bar above that of the second string.

[0073] The panel 810 of some embodiments can include different portions of the strings that include solid state lighting devices that emit light in different dominant wavelengths. Some embodiments include at least one string of each dominant wavelength in each of the bars. The strings of a first dominant wavelength can be fired in the firing order and then the strings of a second dominant wavelength can be fired in the firing order. The firing order can be repeated for each of the portions of strings. In some embodiments, the string of a first dominant wavelength can be fired simultaneously with a string of a second dominant wavelength. Where the strings of first and second wavelengths are fired sequentially, the firing order can be used to determine the location of a second bar based on the location of the first bar.

[0074] The firing logic of some embodiments can also use random logic to generate the firing order. The random logic can be applied as to the bars where some or all of the strings on a bar are fired simultaneously and the bar that is fired is determined using random logic. For example, in a panel 810 having nine bars, a first fired bar determined by random logic may be bar number three, counting from top to bottom. The second fired bar can be randomly selected from remaining bars one, two, and four through nine. If the random logic selects bar number six for the second firing, the third fired bar is randomly selected from the remaining bars one, two, four, five, and seven through nine. Similarly, the random logic can be applied to individual strings.

[0075] Some embodiments can also include means for generating a feedback signal that can provide display performance information to the control system 800. The means can include performance sensors, such as thermal sensors and color sensors, among others.

[0076] Reference is now made to Figure 9, which is a block diagram illustrating systems and methods for controlling a solid state lighting panel according to some other embodiments of the invention. A system 900 for controlling a solid state lighting panel 910 that includes multiple strings of solid state lighting devices can include a sequence generator 902 that can generate a firing sequence for firing the multiple strings in the panel 910. The firing sequence is received by a controller 904 that can provide control signals

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to a current driver 908. The current driver 908 can selectively provide current to the multiple strings in the panel 910.

[0077] The sequence generator 902 can include a deterministic algorithm that determines the location and/or identity of a subsequently fired string based on the location of a previously fired string. In some embodiments, the deterministic algorithm can use locations of multiple previously fired strings to select the next string to be fired. The sequence generator 902 of some embodiments can generate a sequence where a first fired string includes solid state lighting devices that emit light in a first dominant wavelength and then a second fired string includes solid state lighting devices that emit light in a second dominant wavelength. Other embodiments can simultaneously fire two and/or more strings having solid state lighting devices that emit light in different dominant wavelengths. The sequence generator 902 can also generate a random firing sequence that can fire the strings in a random sequence based on location and/or dominant wavelength.

[0078] The system can include multiple bars that each include a portion of the strings, such that the bars extend across the panel in a first direction and are positioned adjacent one another in a second direction. In some embodiments, the first direction and the second direction can be substantially orthogonal. The firing sequence can cause the simultaneous firing of the portion of strings on one bar at a time. The firing sequence can also cause a simultaneous firing of one or more strings on one bar and one or more strings on another bar. In some embodiments, the simultaneously fired strings can include solid state lighting devices that emit light in more than one dominant wavelength. For example, a first string can emit light in a first dominant wavelength and a second string can emit light in a second dominant wavelength. Further, a single string can include different solid state lighting devices that emit light in different dominant wavelengths.

[0079] Reference is now made to Figure 10, which is a block diagram illustrating systems and methods for controlling a solid state lighting panel using a multiple phase power supply in accordance with some embodiments of the invention. A control system 1000 selectively provides control signals to a current drivers 1008 or other type of electrical power supply circuit that

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responsively drives multiple solid state lighting device strings 1012 in a solid state lighting panel 1010. The control system 1000 can include firing logic 1002 that can determine a firing order for the multiple strings. In some embodiments, the firing logic 1002 can include rule-based logic that can generate a non-spatially-sequential firing order. In some embodiments, the firing logic 1002 can include a spatially sequential firing order.

[0080] The current drivers 1008 can include multiple phase drivers 1014 corresponding to N different power phases, for example. Each of the phase drivers 1014 is configured to provide power to one or more different strings 1012 corresponding to that phase. For example, a solid state lighting panel 1010 may include twenty-seven strings that are powered by nine different phase drivers 1014. In this manner, each phase driver 1014 can provide power to three phase strings 1012. The firing order of the strings 1012 within each phase group may be configured to be non-spatially sequential. Further, the determination regarding which strings 1012 are in each phase group may also be non-spatially sequential.

[0081] By providing multiple phases, each phase driver 1014 can be configured to begin firing at a different time within the period, as determined by, for example, the firing logic. In this manner, the firing of the strings 1012 can be performed in a more uniform manner within each period. By temporally displacing the firing of the different strings 1012 using multiple phase drivers 1014, the peak dynamic power load may be reduced, which may reduce the power modulation. Reducing the power modulation may improve the performance consistency of other electrical components in a system, such as, for example, LCD drivers in a display. For example, reductions in the magnitude and duration of peak-to-peak power load changes may result in reduced output differences in the LCD display drivers that result therefrom.

[0082] Further advantages may also be realized including, for example, a reduction in electromagnetic interference (EMI), a reduction in radio frequency interference (RFI), and/or an increase in system circuit response that may be achieved by reducing the size of a power supply output filter. Since large bursts of EMI/RFI associated with large deviations in power transmission may result in higher susceptibility requirements for other system

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components, a reduction in EMI/RFI may be advantageous. Additionally, as the quantity of phases per string increases, the current per phase decreases, which may further reduce EMI.

[0083] Reference is now made to Figures 11A and 11B, which illustrate a timing diagram and a graph of a corresponding dynamic power load, respectively, for systems and methods of using a single phase power supply for controlling a solid state lighting panel in accordance with some embodiments of the invention. The timing diagram 1100 plots the string groups 1110 versus time 1120, which is divided into periods T0 and T1 that may correspond to, for example, cycles in an alternating current (AC) power system. For example, in a sixty Hertz power system, each period is approximately 16.67 milliseconds. The string groups 1110 may include one or more strings of solid state light emitters.

[0084] When driven using a single phase power supply, the string groups 1110 will begin firing near the beginning of the period. Each string group 1110 may stop firing at a different time, depending on the duty cycle determined for that particular string group 1110. For example, a first string group 1112 may have a duty cycle of 50%, which means that the string group 1112 will be driven for approximately 50% of the length of the period. Similarly, a second string group 1114 may have a 60% duty cycle and a third string group 1116 may have a 30% duty cycle.

[0085] Referring to Figure 11B, which plots the percentage of maximum power versus time, the power load is 100% of maximum when all of the string groups 1110 fire at time t1 near the beginning of the period. At time t2, the third string 1116 turns off, which reduces the power load to 66.7% of maximum. At time t3, the second string 1114 turns off, which reduces the power load to 33.3% of maximum and at time t4, the first string 1112 turns off, which drops the power load to 0. In this manner, the dynamic power load cycles between 0 and 100% each period. Moreover, since the duration of the high and low values of power load are each significant portions of the period, attempts at improving the dynamic power load through filtering may have adverse consequences regarding power supply response. Although, for illustration purposes, it is assumed that strings consume the same amount of power, this may generally not be the case. For example, a red string may

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consume more power than a blue string, which may consume more or less power than a green string.

[0086] Reference is now made to Figures 12A and 12B, which are a timing diagram and a graph of a corresponding dynamic power load, respectively, illustrating systems and methods of using a multiple phase power supply for controlling a solid state lighting panel in accordance with some embodiments of the invention. The timing diagram 1200 plots the string groups 1210 versus time 1220, which is divided into periods T and multiples thereof. The string groups 1210 may include one or more strings of solid state light emitters. Although illustrated as three phases and string groups, multiple phase embodiments may include any number of phases from 2 up to the number of strings and/or groups of emitters.

[0087] When driven using a multiple phase or polyphase power supply, the string groups 1210 will begin firing at predetermined times throughout the period T such that the dynamic power loading may be reduced by shifting some of the power load to the later portion of the period. In contrast with the string groups discussed above regarding Figure 11A, the string groups 1210 may be started at different times to eliminate the case where all string groups are firing during the first portion of the period. For example, in the case of three strings and/or groups of strings, a period T may be subdivided into three substantially equal portions. For example, a first string group 1212 may be configured to operate at a 50% duty cycle and fire near the beginning of the period 0. Similarly, a second string group 1214 may be configured to fired at a 60% duty cycle after T/3 time units and a third string group 1216 may be configured to fire at a 45% duty cycle after 2T/3 time units in the period. Thus, the first string group 1212 fires at the beginning of the first third of the period, the second string group 1214 fires at the beginning of the second third of the period and the third string group 1216 fires at the beginning of the final third of the period. This pattern continues for each subsequent period such that each string fires at a predetermined time during each period.

[0088] Referring to Figure 12B, which plots the percentage of the single phase maximum power versus time, the power load is 33.3% when the first string group 1212 fires at time t1 near the beginning of the period. At time

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t2, the second string group 1214 begins firing, which increases the power load to 66.7%. At time t3, the first string group 1214 turns off, which drops the power load to 33.3%. At time t4, the third string group 1216 fires, which increases the power load back to 66.7% until near the end of the period, when the second string group 1214 turns off. The power load continues at 33.3% into the next period until the first string group 1212 turns on again, which increases the power load back to 66.7%. The dynamic power load modulates between 33.3% and 66.7% of the single phase maximum power each period. By reducing the magnitude of the peak to peak dynamic loads the effectiveness of power supply filters such as capacitors can be improved.

[0089] Although illustrated and discussed relative to 100% of the single phase maximum power, as may be determined by the power required to fire all string groups simultaneously, in some embodiments, the maximum power load may be determined based on the maximum number of string groups that are fired at any point during a period. Thus, for example, the dynamic power load in the present example may be determined as the quantity of power required to fire two string groups simultaneously. In this manner, the dynamic power load may vary from 50% to 100%, with a brief 0% interval, that may, in some embodiments, be filtered out based on the duration of the interval. Although, as illustrated, the system utilizes three different groups, each driven by a different phase, in some embodiments, a system may use, for example, nine phases to drive, for example, twenty-seven different strings. In this manner, each string group may include three strings. It should be appreciated that as the ratio of phases to strings increases and approaches unity, the dynamic power load may decrease correspondingly. In some embodiments, a polyphase power supply may be used in conjunction with a non-spatially-sequential firing order. Although, for illustration purposes, it is assumed that strings consume the same amount of power, this may generally not be the case. For example, a red string may consume more power that a blue string and/or a green string.

[0090] Some embodiments may include providing one phase per string. For example, reference is now made to Figures 13A and 13B, which are a timing diagram and a graph of a corresponding dynamic power load, respectively, illustrating systems and methods of using a multiple phase

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power supply having a phase for each string. By way of example, a display may include nine strings 1310 of solid state light emitters that may each be fired at a different duty cycle 1312. A power supply may be included that can include one phase driver for each of the nine different strings 1310. In this manner, each string may be fired independent of the others. For example, each of the strings 1310 may begin and end firing at different time intervals 1320. In this manner, the dynamic power load, as illustrated in the graph of Figure 13B, can realize a reduced dynamic range.

[0091] Each phase may begin and end at a different time and each string may be driven at a different load factor. In some embodiments, the phases may be temporally separated responsive to the number of different phases. For example, where each cycle has a period of T seconds and there are nine phases, the delay between each successive phase may be T/9 seconds. Two consecutive periods for each of the nine phases is shown to illustrate the resulting dynamic power load during operation. For example, in the firing scheme illustrated in Figure 13A, the power load is substantially evenly distributed around an average of approximately 67% and deviates plus or minus 11% from the average value.

[0092] In some embodiments, timing the firing of the strings may be determined algorithmically and may be dynamically adjusted depending on the state of the system. Different variables within algorithms and/or different algorithms may be used at various levels and/or hues of requested light output. For example, a particular algorithm and/or set of variables may be used to determine the timing of the firing of the strings when the solid state lighting panel is in a minimum output configuration. In some embodiments, a display may include, a greater number of strings and/or phases. For example, a display may include twenty-seven strings that are configured to be driven by nine phases. In some embodiments, a twenty-seven string display may be driven by twenty-seven phases. Although, for illustration purposes, it is assumed that strings consume the same amount of power, this may generally not be the case.

[0093] Reference is now made to Figure 14, which is a block diagram illustrating systems and methods for controlling a solid state lighting panel synchronized with an LCD display in accordance with other embodiments of

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the invention. A display device 1400 may include an LCD panel 1410, including a two-dimensional arrangement of liquid crystal shutters, that is controlled by an LCD controller 1430. The LCD controller 1430 may control the output image 1460 by varying on/off values of the LCD shutters corresponding to different color pixels. Since an output image 1460 may typically include dynamic content, the LCD controller 1430 may be configured to refresh the pixels at a predetermined refresh rate.

[0094] The LCD panel 1410 relies on dynamic light transmission to control an output image 1460 so the display device 1400 may also include a solid state backlight panel 1420 configured to provide light to be selectively transmitted through the shutters of the LCD panel 1410. A solid state backlight panel 1420 may include multiple strings of solid state light emitters that can be controlled to achieve a desired color hue and/or luminous intensity. Varying the output of a string may be accomplished, for example, by firing the string for a portion of a period, which may be controlled by a backlight controller 1440. In some embodiments, the refresh rate of the LCD controller 1430 may be synchronized with the firing of the solid state backlight panel 1420 by sending a synchronizing signal from the LCD controller to the backlight controller 1440. In this manner, unwanted effects due to the interference of non-synchronized processes operating at different frequencies may be reduced. Synchronized display and backlighting may be used in conjunction with single phase power supply systems and/or polyphase power supply systems. Additionally, synchronization may be used in conjunction with a non-spatially-sequential firing order.

[0095] Reference is now made to Figure 15, which is a block diagram illustrating systems/methods for controlling a solid state backlighting panel synchronized with an LCD panel in accordance with some embodiments of the invention. An LCD panel 1510 is controlled by a display controller 1530, which refreshes the pixels in the LCD panel 1510 at a predetermined refresh rate. A solid state backlighting panel 1520 may also be included for providing luminance through the LCD panel 1510. The solid state backlighting panel 1520 may be controlled by a backlight controller 1540 that can drive multiple strings of solid state light emitters using a current driver 1560. The output of the solid state backlighting panel 1520 may be controlled by firing the emitters

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for specific portions of a period. The display controller 1530 may send a synchronizing signal 1550 to the backlight controller 1540 such that the firing rate of the strings corresponds to the refresh rate of the LCD display 1520. In this manner, the visual effects from interference between the refresh rates of the LCD display 1520 and the solid state lighting panel 1510 may be reduced.

[0096] Reference is now made to Figure 16, which is a block diagram illustrating systems/methods for controlling a solid state lighting panel according to some embodiments of the invention. The operations 1600 include supplying drive currents to strings in a solid state lighting panel in a non-spatially-sequential firing order (block 1610). The non-spatially-sequential firing order can be accomplished using, for example, a randomly generated firing order or a deterministic firing order. A deterministic firing order can be rule-based and use rules, such as a rule that the directional relationship between a subsequently fired string and a previously fired string alternates with each firing. Some embodiments can include a rule defining the minimum number of bars and/or strings between sequentially and/or simultaneously fired strings. Embodiments can also include a rule that sequentially and/or simultaneously fired strings are non-adjacent and/or are in non-adjacent bars.

[0097] Reference is now made to Figure 17, which is a block diagram illustrating systems/methods for controlling a solid state lighting panel according to other embodiments of the invention. The operations 1700 include supplying drive currents to strings of solid state lighting devices arranged in a panel in a non-spatially-sequential firing order (block 1710). A firing order for a first string and a second string is determined (block 1720). The firing order determines the order in which the strings will be supplied current. A second string is defined based on a location of the first string (block 1730). By defining the second string based on the location of the first string, a non-spatially-sequential firing order can be accomplished. In some embodiments the second string can be defined by selecting a string that is non-adjacent the first string and/or is in a bar that is non-adjacent the bar that includes the first string. The second string can also be defined by selecting a string such that a minimum quantity of strings and/or bars are between the first and second strings. A third string can also be defined based on the

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locations of the first string and the second string. For example, where the second string is in a first direction relative to the first string, the third string is selected to be in a second direction relative to the second string.

[0098] Reference is now made to Figure 18, which is a block diagram illustrating systems/methods for controlling a solid state lighting panel according to further embodiments of the invention. The operations 1800 include supplying drive currents to strings of solid state lighting devices in a solid state lighting panel in a non-spatially-sequential firing order (block 1810). The operations can also include grouping the strings on multiple bars that extend from a first edge of the panel to a second edge of the panel (block 1820). The first and second edges can be opposite one another in a panel configured in a rectilinear geometry. The bars can be arranged adjacent one another and can be substantially parallel to one another in some embodiments. Some embodiments include simultaneously supplying current to the portion of strings that are in a same one of the bars. Embodiments can also include simultaneously supplying current to strings located in more than one of the bars. In some embodiments, a random number can be generated, a value can be assigned to each bar, and current can be simultaneously supplied to the strings in the bar having a value corresponding to the random number.

[0099] Reference is now made to Figure 19, which is a block diagram illustrating systems/methods for controlling a solid state lighting panel in yet further embodiments of the invention. The operations 1900 include supplying drive currents to strings of solid state lighting devices in a solid state lighting panel in a non-spatially-sequential firing order (block 1910). The operations can also include supplying current to strings having solid state lighting devices that emit light in a first dominant wavelength in the firing order (block 1920). Embodiments can also include supplying current to strings having solid state lighting devices that emit light in a second dominant wavelength in the firing order (block 1930). In this manner, the strings of a first wavelength are fired in a sequence and then strings of a second wavelength are fired in the sequence.

[00100] Reference is now made to Figure 20, which is a table illustrating an exemplary string firing sequence according to some

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embodiments of the invention. The table 2000 corresponds to a sequence for a solid state lighting panel having three different color or wavelength strings at each of nine panel positions. The panel positions, which, in some embodiments, can be bars, are designated as the string number (column 2030) and the color of each string is designated (column 2010). The firing sequence (column 2020) indicates each string's position in the sequence of firing. A spatial delta value for each string lists the number of places between the present string and the last fired string in the sequence and is listed for each string (column 2040). This sequence, for example, provides that the strings of each color are fired as a sequential group and that one color group is fired after another color group. For example, all of the red strings are fired in a location based sequence then all of the green strings are fired in the sequence and then all of the blue strings are fired in the sequence. Note that since no value in the spatial delta column 2040 is less than three, there are no strings fired closer than three positions away from the previously fired string. Further, within each color group, since the spatial delta alternates between positive and negative values, each string fired is located in a different direction relative to the previously fired string from the direction between the previously fired string and its predecessor.

[00101] Although some embodiments are described in connection with LCD backlights, embodiments of the invention may be used for other purposes, such as general lighting. In the drawings and specification, there have been disclosed typical embodiments of the invention and, although specific terms are employed, they are used in a generic and descriptive sense only and not for purposes of limitation, the scope of the invention being set forth in the following claims.

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That which is claimed is:

1. A lighting panel system, comprising:

a lighting panel including a plurality of strings of solid state lighting devices arranged across the panel in a first direction and positioned at intervals in a second direction that is substantially orthogonal to the first direction;

a current supply circuit configured to selectively supply a plurality of on-state drive currents to the plurality of strings responsive to a plurality of control signals; and

a control system configured to selectively provide control signals to the current supply circuit to selectively drive the plurality of strings, the control system further including firing logic configured to determine a firing order of the plurality of strings.

2. The system of Claim 1, wherein the firing logic comprises rule-based logic operative to generate a non-spatially-sequential firing order.

3. The system of Claim 2, wherein the rule-based logic comprises a rule that a second string fired after a first string is non-adjacent the first string.

4. The system of Claim 2, wherein the rule-based logic comprises a rule that a first string is fired simultaneously with a second string, wherein the first string is non-adjacent the second string.

5. The system of Claim 1, wherein the lighting panel further comprises a plurality of bars that include portions of the plurality of strings, wherein the plurality of bars extend across the panel in the first direction and are positioned adjacent one another in a substantially parallel arrangement.

6. The system of Claim 5, wherein the firing order is operative to cause a first firing, a second firing and a third firing, wherein the first firing occurs before the second firing and the second firing occurs before the third

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firing, wherein the first firing supplies current for at least one string in a first bar, the second firing supplies current for at least one string in a second bar and the third firing supplies current for at least one string in a third bar, wherein the second bar is located below the first bar and the third bar is located above the second bar.

7. The system of Claim 5, further comprising:

a first portion of the plurality of strings including solid state lighting devices that emit light in a first dominant wavelength; and

a second portion of the plurality of strings including solid state lighting devices that emit light in a second dominant wavelength,

wherein each of the plurality of bars includes at least one string of the first portion of the plurality of strings and at least one string of the second portion of the plurality of strings and wherein each of the first portion of the plurality of strings is fired in the firing order and then each of the second portion of the plurality of strings is fired in the firing order.

8. The system of Claim 5, further comprising:

a first portion of the plurality of strings including solid state lighting devices that emit light in a first dominant wavelength; and

a second portion of the plurality of strings including solid state lighting devices that emit light in a second dominant wavelength,

wherein at least one string of the first portion of the plurality of strings is fired simultaneously with at least one string of the second portion of the plurality of strings.

9. The system of Claim 5, further comprising:

a first portion of the plurality of strings in a first bar; and

a second portion of the plurality of strings in a second bar,

wherein the first and second portions of the plurality of strings are fired sequentially in the firing order and wherein the firing order is configured to determine the location of the second bar relative to the location of the first bar.

10. The system of Claim 1, further comprising:

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a first portion of the plurality of strings including solid state lighting devices that emit light in a first dominant wavelength; and

a second portion of the plurality of strings including solid state lighting devices that emit light in a second dominant wavelength,

wherein each of the first portion of the plurality of strings is fired in the firing order and then each of the second portion of the plurality of strings is fired in the firing order.

11. The system of Claim 1, wherein the firing logic comprises random logic operative to generate the firing order.

12. The system of Claim 1, further comprising a means for generating a feedback signal configured to provide display performance information to the control system.

13. The system of Claim 1,

wherein the current supply circuit comprises a plurality of phase drivers configured to supply a plurality of on-state drive currents at a plurality of times in a firing cycle,

wherein the plurality of strings of solid state lighting devices comprise a plurality of string groups, each configured to receive current from one of the plurality of phase drivers, and

wherein the control system is further configured to determine the plurality of times that each of the plurality of phase drivers begin to supply current to the plurality of string groups.

14. The system of Claim 13, wherein the ratio of a quantity of the plurality of phase drivers to a quantity of the plurality of strings of solid state lighting devices is one and wherein each of the plurality of string groups comprises one of the plurality of strings of solid state lighting devices.

15. The system of Claim 1, wherein the control system is configured to receive a synchronizing signal from a display controller configured to

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control a display and wherein the firing order is synchronized with periodic operations of the display.

16. A method for controlling a solid state lighting panel including a plurality of strings of solid state lighting devices configured to extend from a first edge of the panel to a second edge of the panel in substantially adjacent positions relative to one another, the method comprising supplying a plurality of pulsed drive currents to the plurality of strings in a non-spatially-sequential firing order.

17. The method of Claim 16, further comprising:

determining the firing order that supplies current to a first string of the plurality of strings and a second string of the plurality of strings; and

defining the second string of the plurality of strings, wherein the defining is based on a location of the first string.

18. The method of Claim 17, wherein defining the second string comprises selecting one of the plurality of strings that is not adjacent to the first string.

19. The method of Claim 17, wherein defining the second string comprises selecting one of the plurality of strings that is located a minimum quantity of strings from the first string.

20. The method of Claim 17, further comprising defining a third string of the plurality of strings, wherein the third string is configured to be fired after the second string and wherein the defining is based on a location of the second string and the location of the first string.

21. The method of Claim 20, wherein defining the second string comprises selecting one of a plurality of strings that is on a first side of the first string and defining the third string comprises selecting one of the plurality of strings that is on a second side of the second string.

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22. The method of Claim 16, further comprising grouping a plurality of portions of the plurality of strings on a plurality of bars, wherein the plurality of bars extend across the panel from the first edge to the second edge and are positioned adjacent one another in a substantially parallel arrangement.

23. The method of Claim 22, further comprising simultaneously supplying current to the portion of the plurality of strings that are in the same one of the plurality of bars.

24. The method of Claim 22, further comprising simultaneously supplying current to a first string located in a first bar and a second string located in a second bar.

25. The method of Claim 22, further comprising:

generating a random number;

assigning a value to each of the plurality of bars; and

simultaneously supplying current to the portion of the plurality of strings on one of the plurality of bars based on the random number.

26. The method of Claim 16, further comprising:

supplying current to a first portion of the plurality of strings according to the firing order, wherein the first portion of the plurality of strings includes solid state lighting devices configured to emit light in a first dominant wavelength; and

supplying current to a second portion of the plurality of strings according to the firing order after supplying current to the first portion of the plurality of strings, wherein the second portion of the plurality of strings includes solid state lighting devices configured to emit light in a second dominant wavelength.

27. The method of Claim 16, wherein defining is further based on a dominant wavelength of light emitted by the solid state lighting devices in the first string.

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28. The method of Claim 16, further comprising simultaneously supplying current to a first string including solid state lighting devices configured to emit light in a first dominant wavelength and a second string including solid state lighting devices configured to emit light in a second dominant wavelength.

29. The method of Claim 16, further comprising:

determining the firing order that supplies current to a first string of the plurality of strings and a second string of the plurality of strings; and

defining the second string based on a dominant wavelength emitted by the solid state lighting devices in the first string and a relative position of the first string.

30. The method of Claim 16, comprising determining the firing order using a numerical technique.

31. The method of Claim 30, further comprising:

generating a random number;

assigning a value to each of the plurality of strings; and

supplying current to one of the plurality of strings based on the random number.

32. The method of Claim 30, wherein the numerical technique comprises performing a non-linear calculation.

33. The method of Claim 16, wherein the firing order comprises a deterministic order based on at least one rule.

34. A system for controlling a solid state lighting panel including a plurality of strings of solid state lighting devices that are arranged to extend across the panel in a first direction and are positioned adjacent one another in a second direction and that are supplied current by a plurality of current drivers, the system comprising:

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a sequence generator that generates a firing sequence for firing the plurality of strings; and

a controller that provides control signals, responsive to the sequence generator, to the plurality of current drivers.

35. The system of Claim 34, wherein the sequence generator comprises a deterministic algorithm that determines a location of a subsequently fired string based on a location of at least one previously fired string.

36. The system of Claim 34, wherein the sequence generator comprises an algorithm that generates a sequence to fire a first string having a plurality of solid state lighting devices that emit light in a first dominant wavelength and a second string having a plurality of solid state lighting devices that emit light in a second dominant wavelength, wherein the second string is fired after the first string.

37. The system of Claim 34, wherein the sequence generator comprises an algorithm that generates a sequence to simultaneously fire a first string having a plurality of solid state lighting devices that emit light in a first dominant wavelength and a second string having a plurality of solid state lighting devices that emit light in a second dominant wavelength.

38. The system of Claim 34, wherein the sequence generator generates a random sequence of firing.

39. The system of Claim 34, further comprising a plurality of bars that include portions of the plurality of strings, wherein the plurality of bars extend across the panel in the first direction and are positioned adjacent one another in the second direction.

40. The system of Claim 39, wherein the firing sequence is configured to simultaneously fire a first portion of the plurality of strings and then simultaneously fire a second portion of the plurality of strings and

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wherein the first portion is located on a first bar and the second portion is located on a second bar.

41. The system of Claim 39, wherein the firing sequence is configured to simultaneously fire a first string on a first bar and a second string on a second bar.

42. The system of Claim 41, wherein the first string includes solid state lighting devices that emit light in a first dominant wavelength and the second string includes solid state lighting devices that emit light in a second dominant wavelength.

43. The system of Claim 34, further comprising:

a first portion of the plurality of strings including solid state lighting devices that emit light in a first dominant wavelength; and

a second portion of the plurality of strings including solid state lighting devices that emit light in a second dominant wavelength;

wherein each of the plurality of bars includes at least one string of the first portion of the plurality of strings and at least one string of the second portion of the plurality of strings.

44. The system of Claim 43, wherein the firing sequence is operative to cause the first portion of strings to fire in a first sequence and to then to cause the second portion of strings to fire in the first sequence.

45. The system of Claim 34, wherein the plurality of drivers comprise a polyphase power supply configured to a supply a plurality of temporally shifted drive currents to a plurality of groups of the plurality of strings.

46. A method for controlling a solid state lighting panel including a plurality of strings of solid state lighting devices configured to extend from a first edge of the panel to a second edge of the panel in substantially adjacent

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positions relative to one another, the method comprising supplying a plurality of pulsed drive currents to a plurality of groups of the plurality of strings.

47. The method of Claim 46, wherein each group of the plurality of groups comprises one of the plurality of strings and wherein one of the plurality of pulsed drive currents is provided for each of the plurality of strings by one of a plurality of phase drivers.

48. The method of Claim 47, further comprising receiving a synchronizing signal from a display controller configured to control a refresh rate of display pixels.

49. The method of Claim 46, further comprising synchronizing the plurality of drive currents with a cycles of a periodic operation of a display panel.

50. The method of Claim 49, wherein the periodic operation comprises refreshing pixels and wherein the display panel comprises an LCD display panel.

51. A lighting panel system, comprising:

a lighting panel including a plurality of strings of solid state lighting devices arranged across the panel in a first direction and positioned at intervals in a second direction that is substantially orthogonal to the first direction;

a current supply circuit configured to selectively supply a plurality of on-state drive currents to the plurality of strings responsive to a plurality of control signals;

a control system configured to selectively provide control signals to the current supply circuit to selectively drive the plurality of strings, the control system further including firing logic configured to determine a firing order of the plurality of strings; and

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wherein the firing logic is configured to drive the plurality of strings in a spatially non-adjacent, non-sequential firing order and/or to drive the plurality of strings at different times for at least a subset of the plurality of strings.

52. The system of Claim 51, wherein the firing logic is further configured to drive the plurality of strings and/or portions thereof at least partially based on the spatial relationship between the plurality of strings and or portions thereof.

53. The system of Claim 51, wherein the firing logic comprises rule-based logic configured to generate a non-spatially sequential firing order.

54. The system of Claim 53, wherein the rule-based logic further comprises a rule that a second string fired after a first string is non-adjacent the first string.

55. The system of Claim 53, wherein the rule-based logic further comprises a rule that if first string is fired simultaneously with a second string, then the first string is non-adjacent the second string.

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SYSTEMS AND METHODS FOR CONTROLLING A SOLID STATE LIGHTING PANEL

ABSTRACT OF THE DISCLOSURE

Provided are systems and methods for controlling a solid state lighting panel. A system according to some embodiments of the invention includes a controller that provides control signals to current drivers that are configured to provide current to multiple solid state lighting devices. The system also includes a sequence generator that generates a firing sequence for firing multiple strings of slid state lighting devices.

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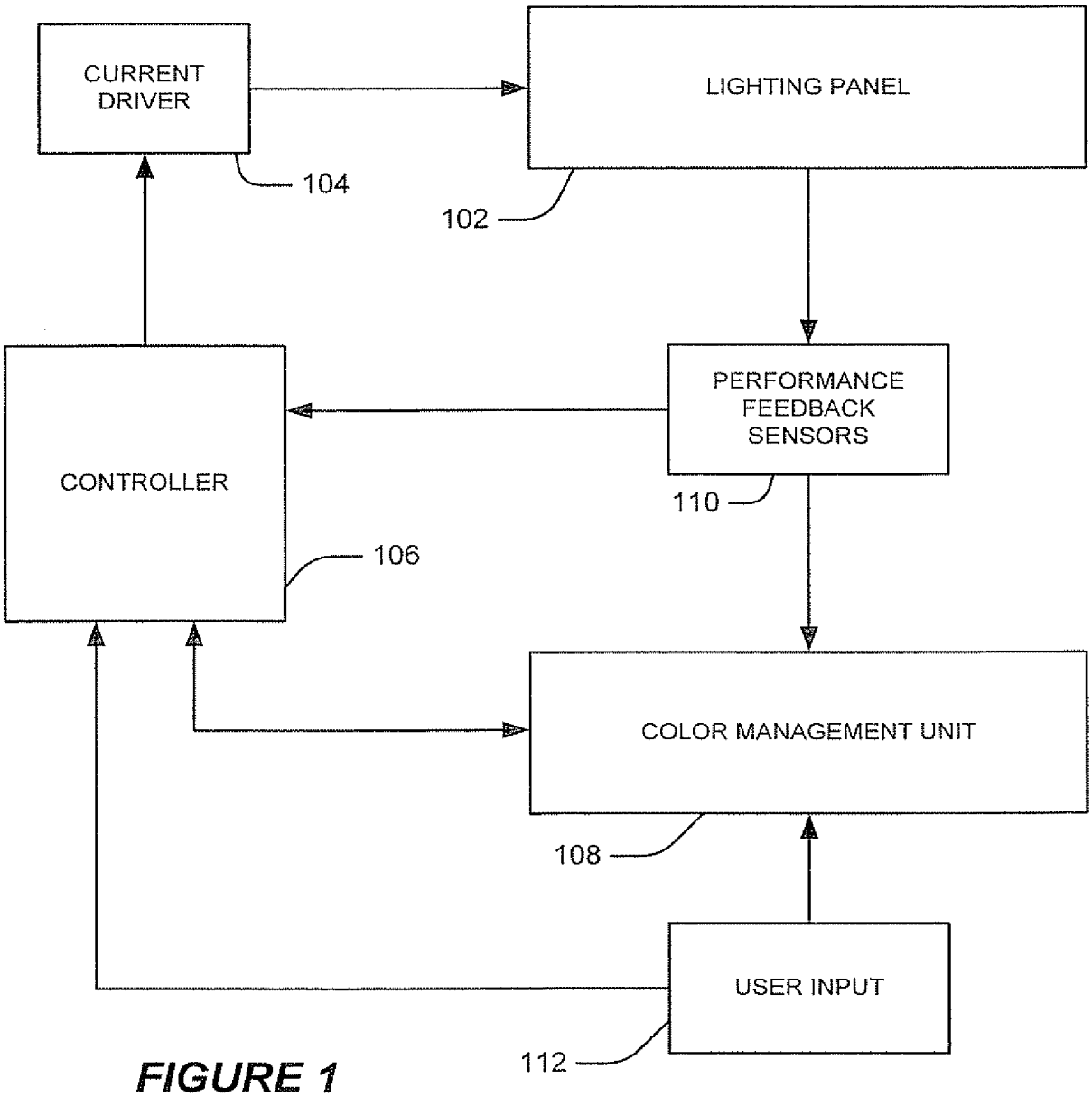

CURRENT DRIVER
LIGHTING PANEL
104
102
CONTROLLER
PERFORMANCE FEEDBACK SENSORS
110
106
COLOR MANAGEMENT UNIT
108
USER INPUT
112

FIGURE 1

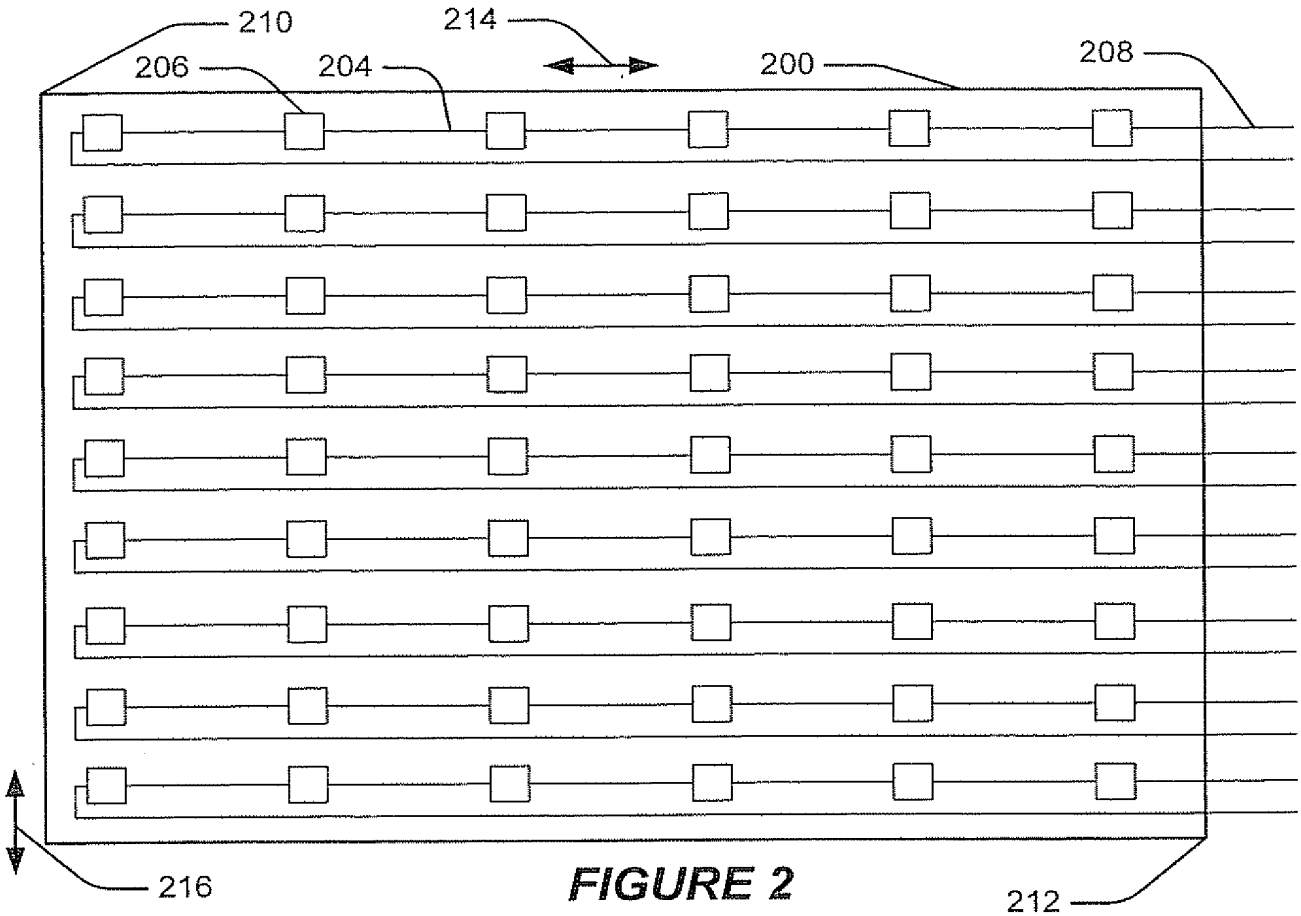


FIGURE 2

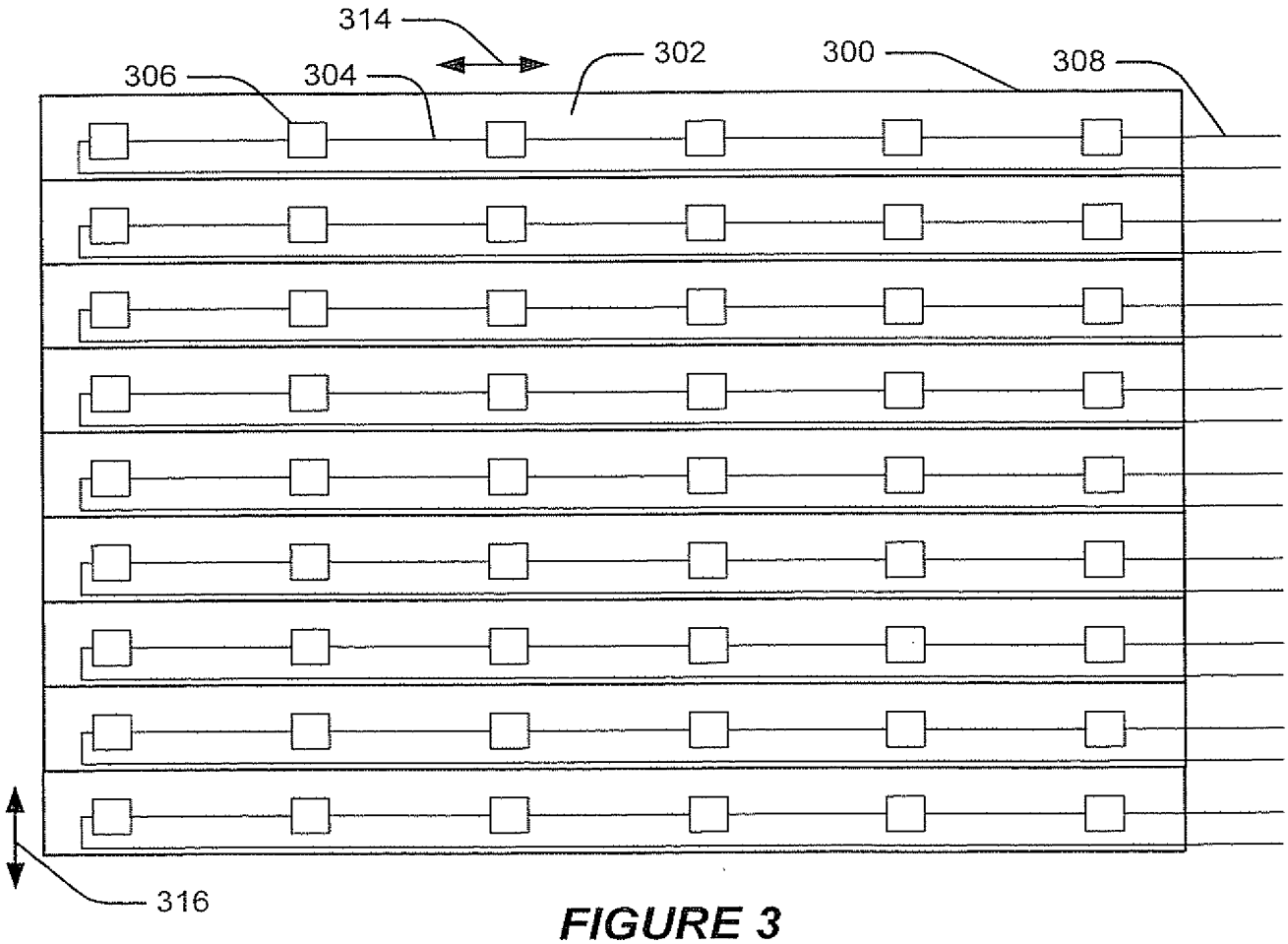


FIGURE 3

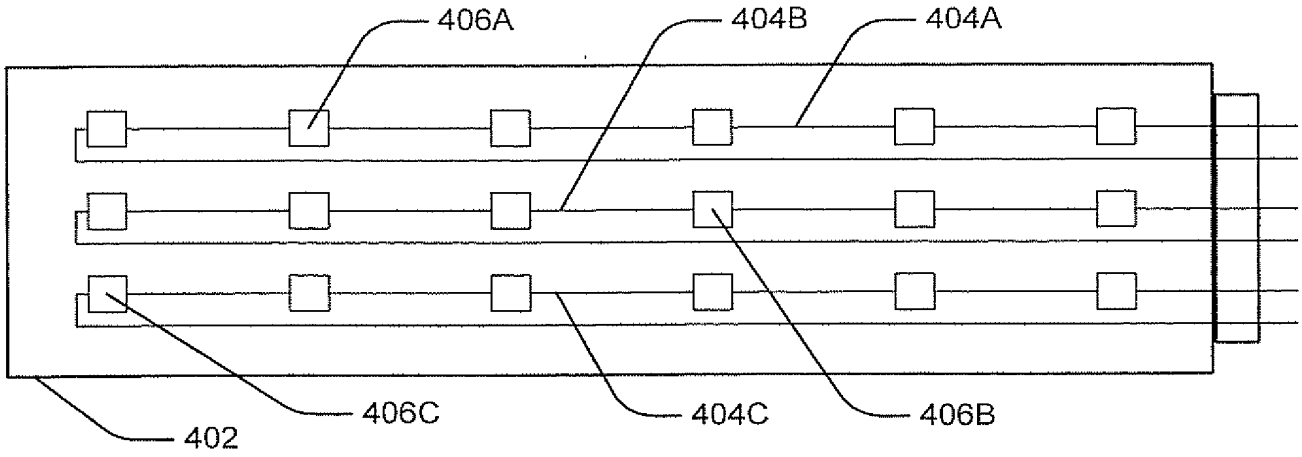


FIGURE 4

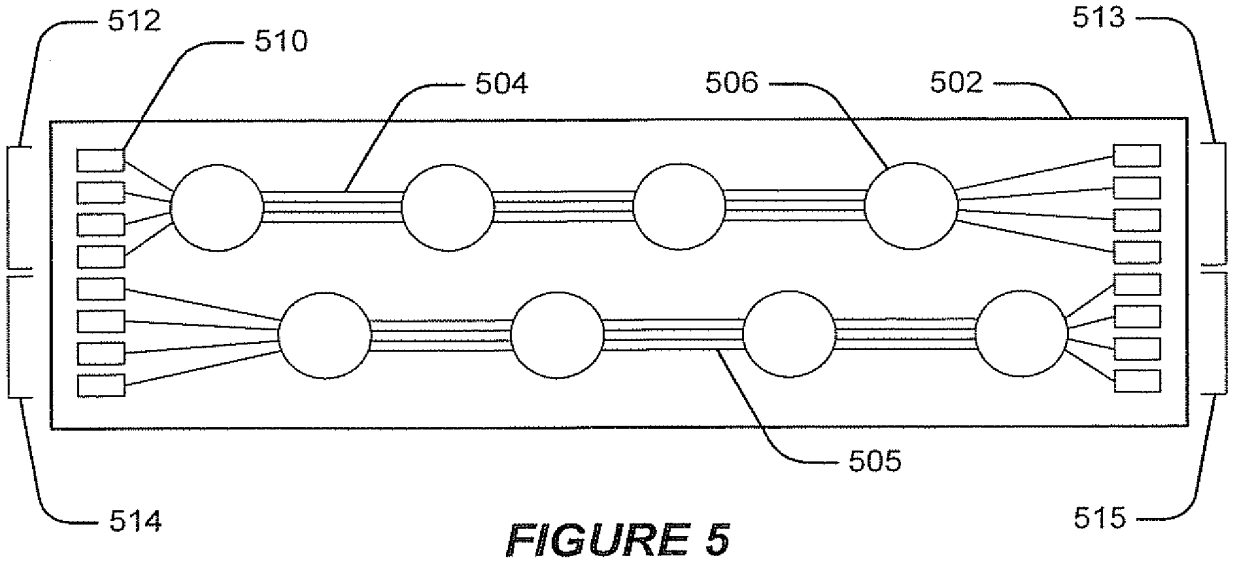


FIGURE 5

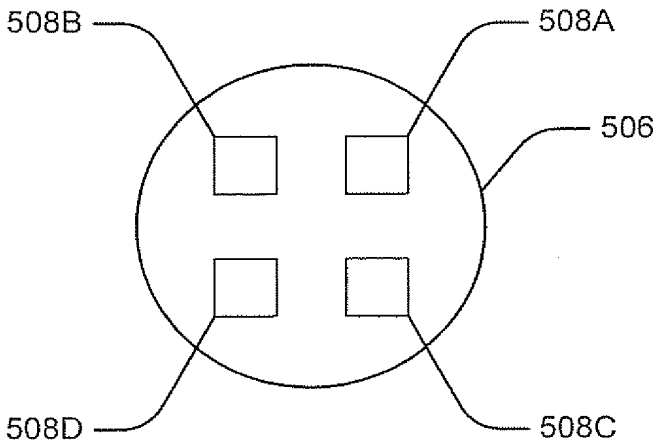


FIGURE 6

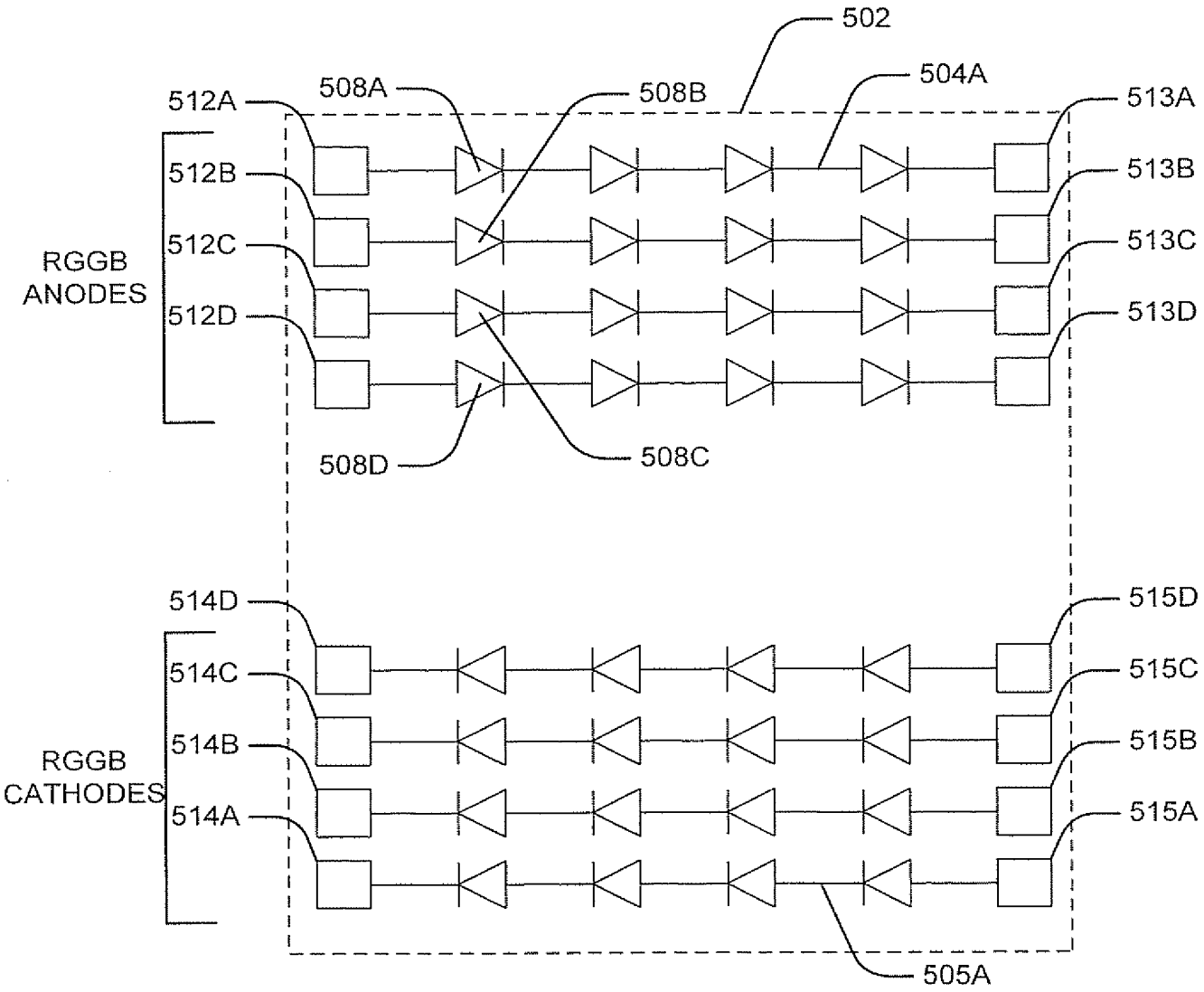

502
504A
508A
508B
512A
513A
512B
513B
RGGB
ANODES
512C
513C
512D
513D
508D
508C
514D
515D
514C
515C
RGGB
CATHODES
514B
515B
514A
515A
505A

FIGURE 7

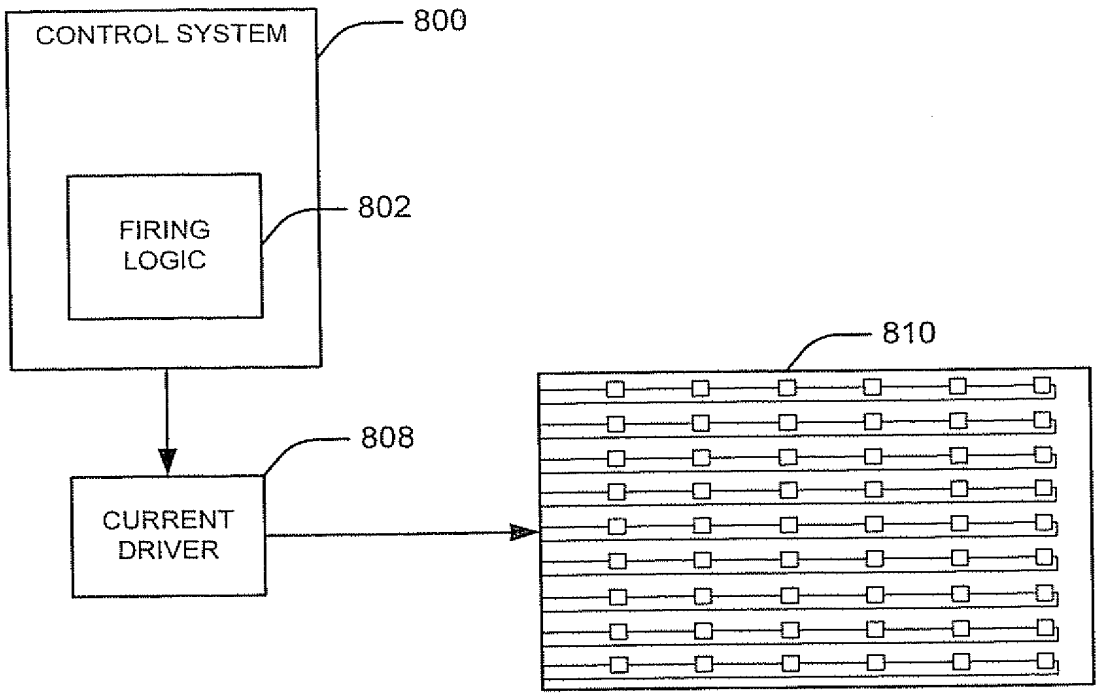


FIGURE 8

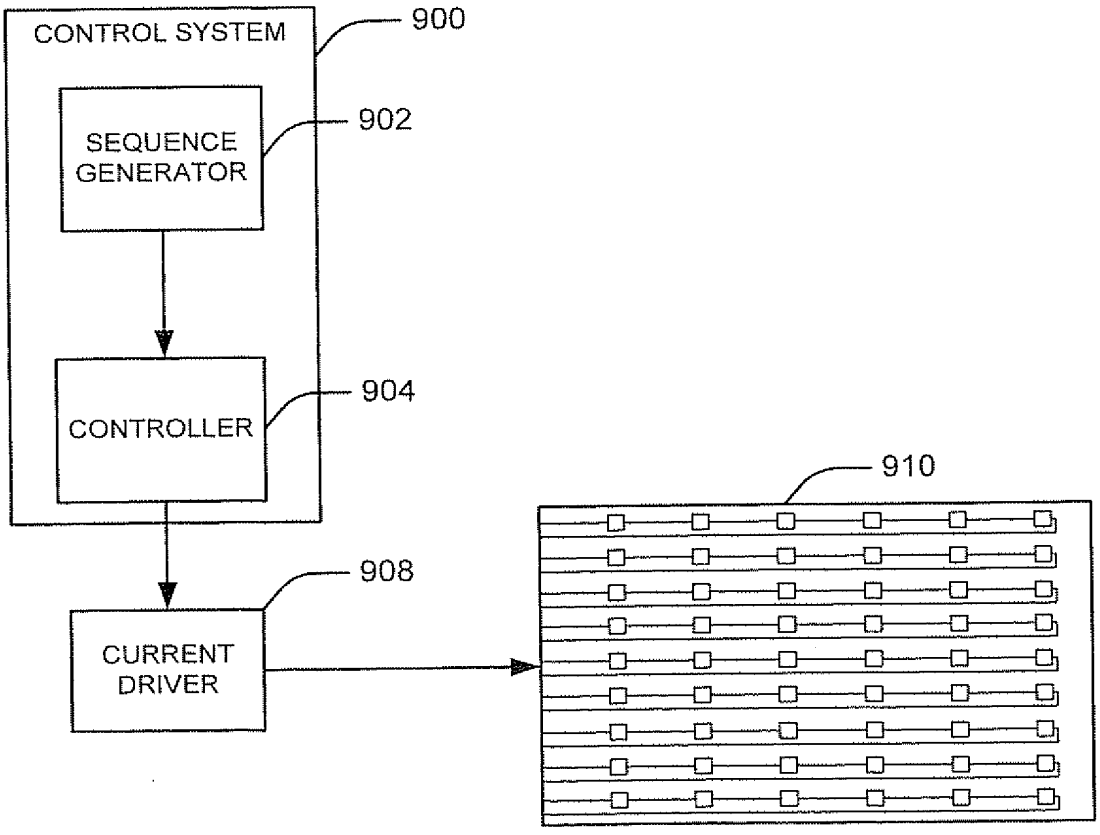


FIGURE 9

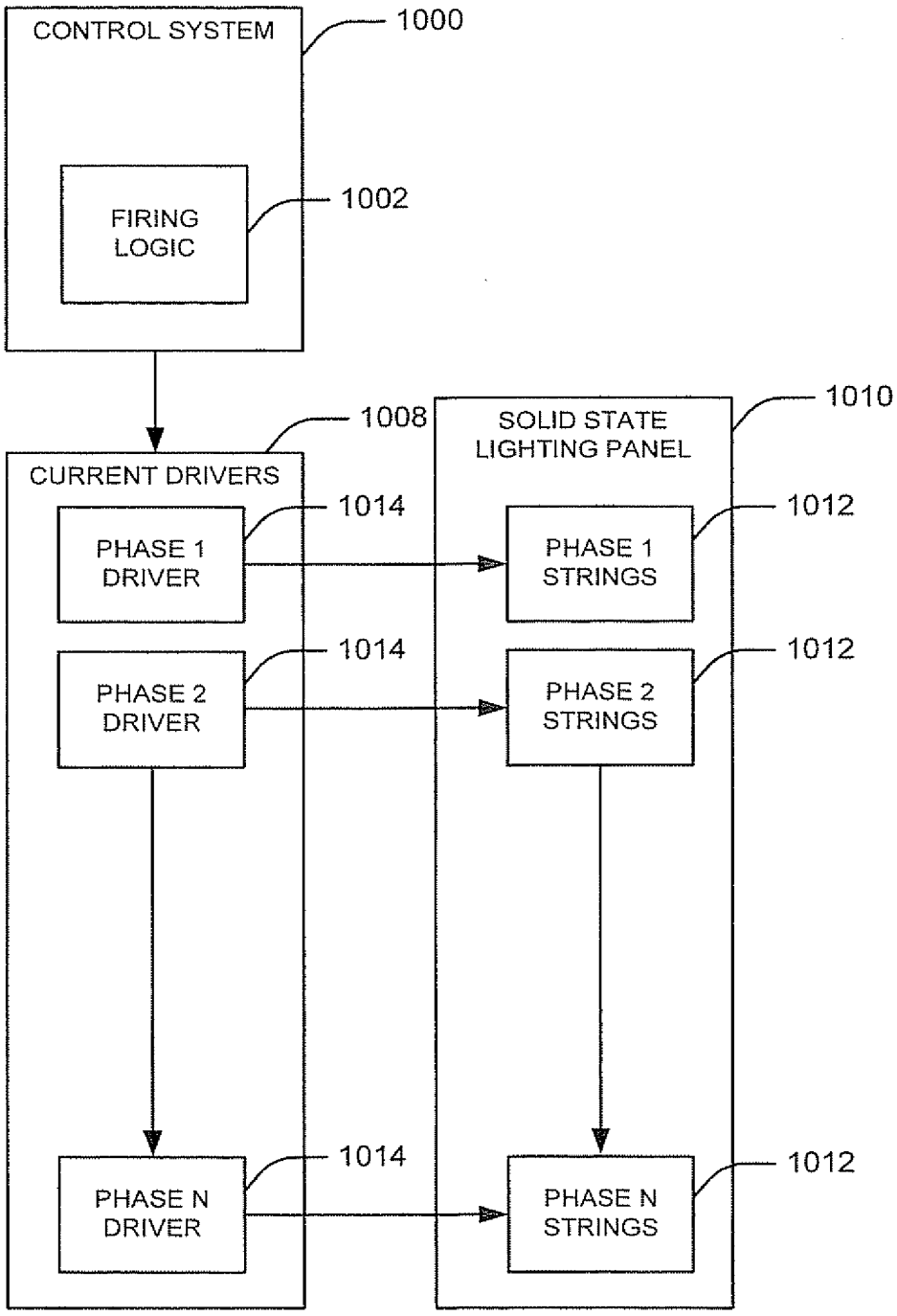

CONTROL SYSTEM
1000
FIRING LOGIC
1002
1008
CURRENT DRIVERS
1010
SOLID STATE LIGHTING PANEL
1014
PHASE 1 DRIVER
1012
PHASE 1 STRINGS
1014
PHASE 2 DRIVER
1012
PHASE 2 STRINGS
1014
PHASE N DRIVER
1012
PHASE N STRINGS

FIGURE 10

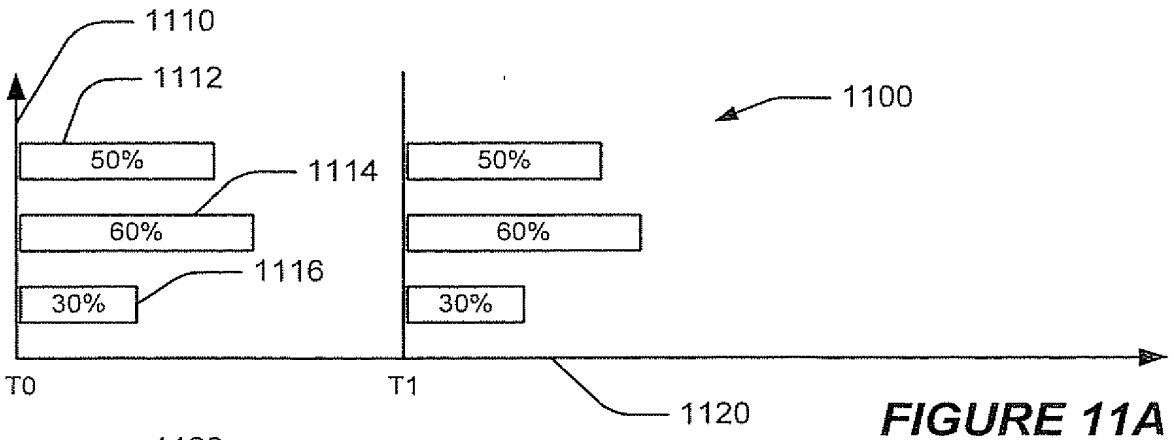


FIGURE 11A

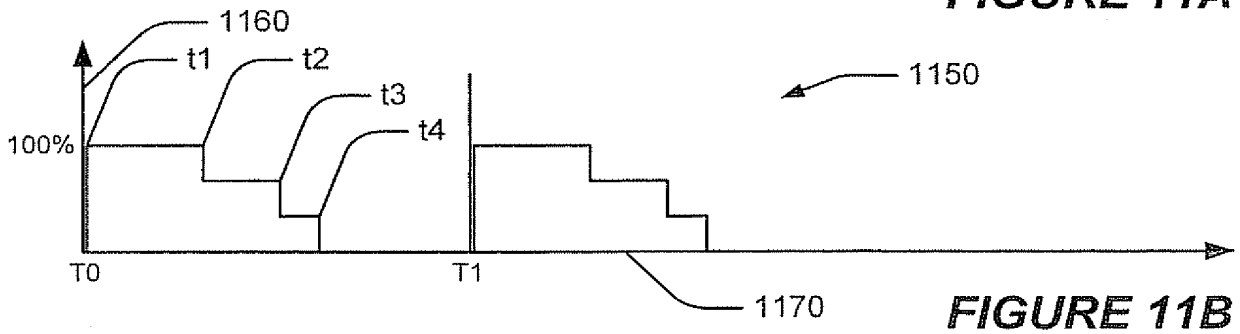


FIGURE 11B

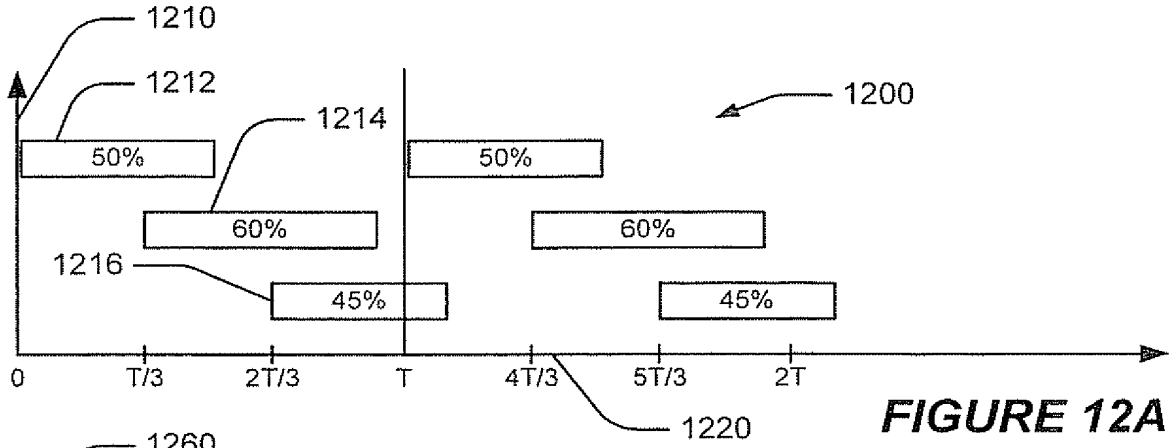


FIGURE 12A

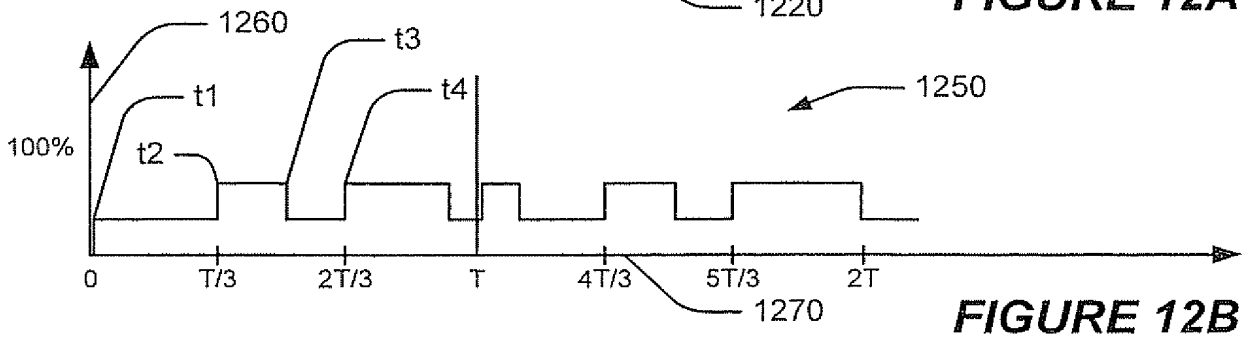


FIGURE 12B

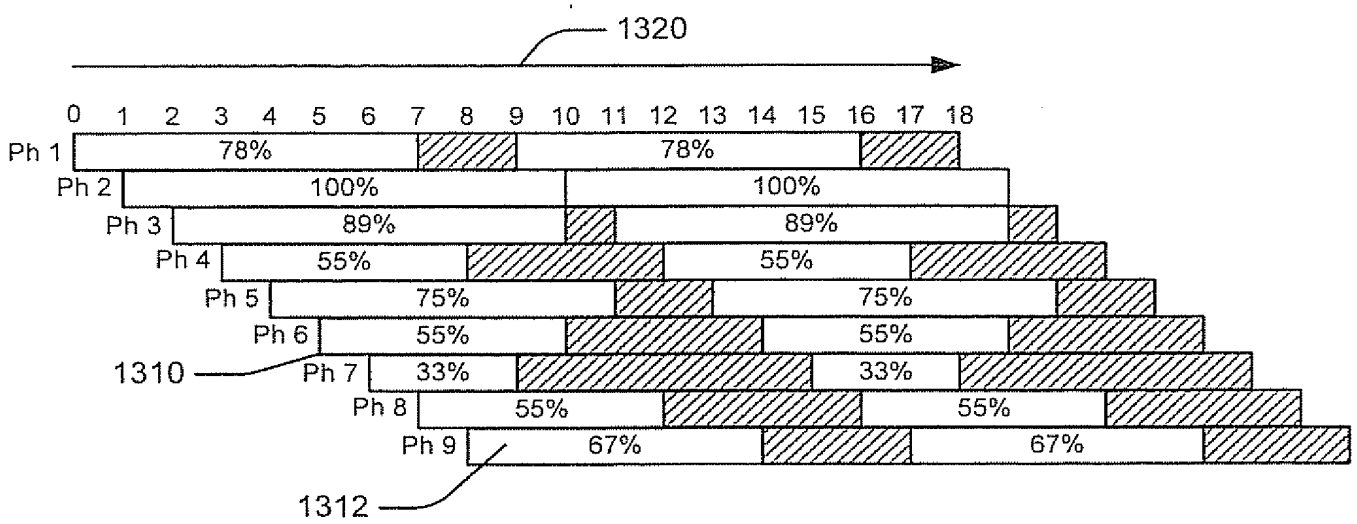


FIGURE 13A

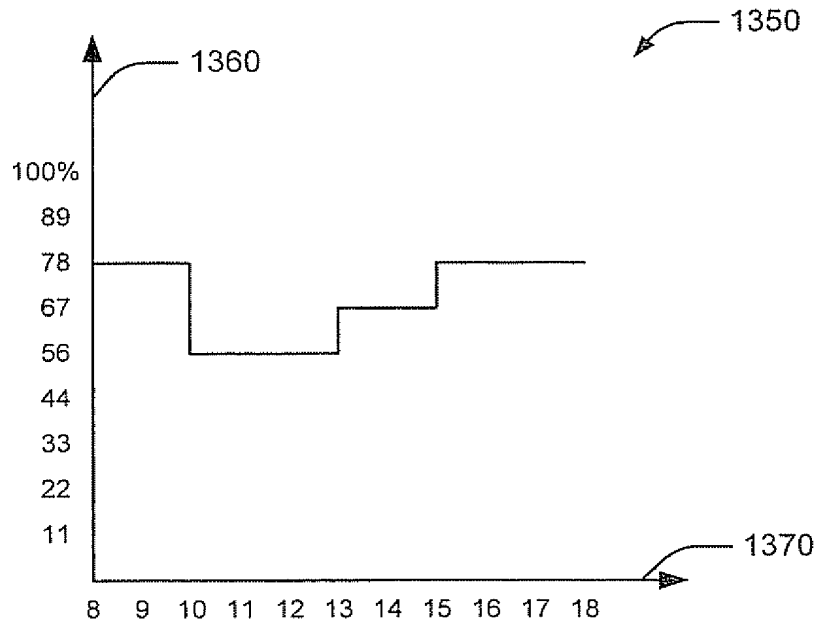


FIGURE 13B

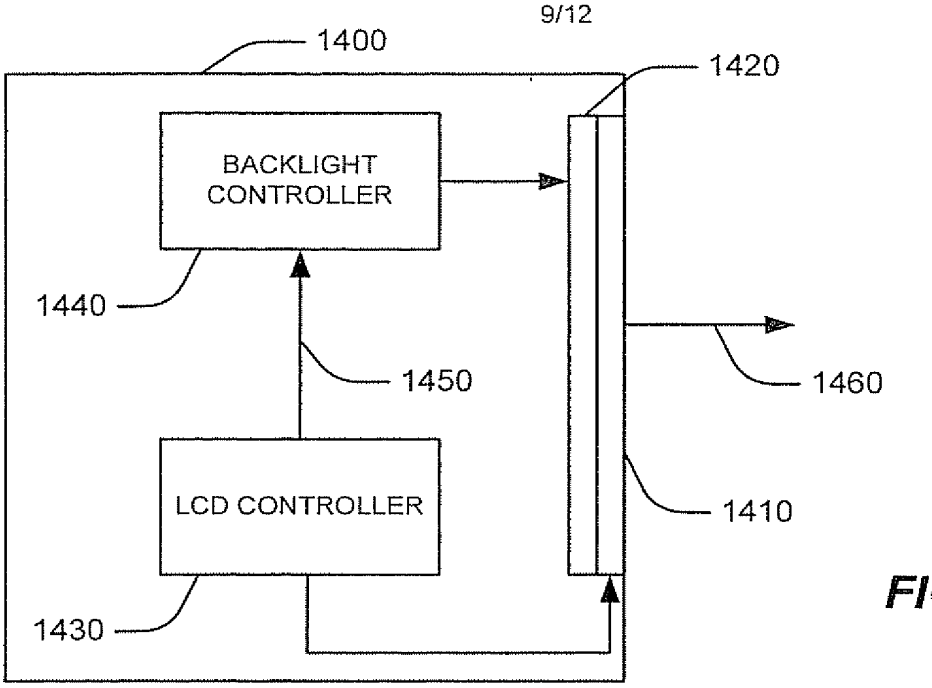


FIGURE 14

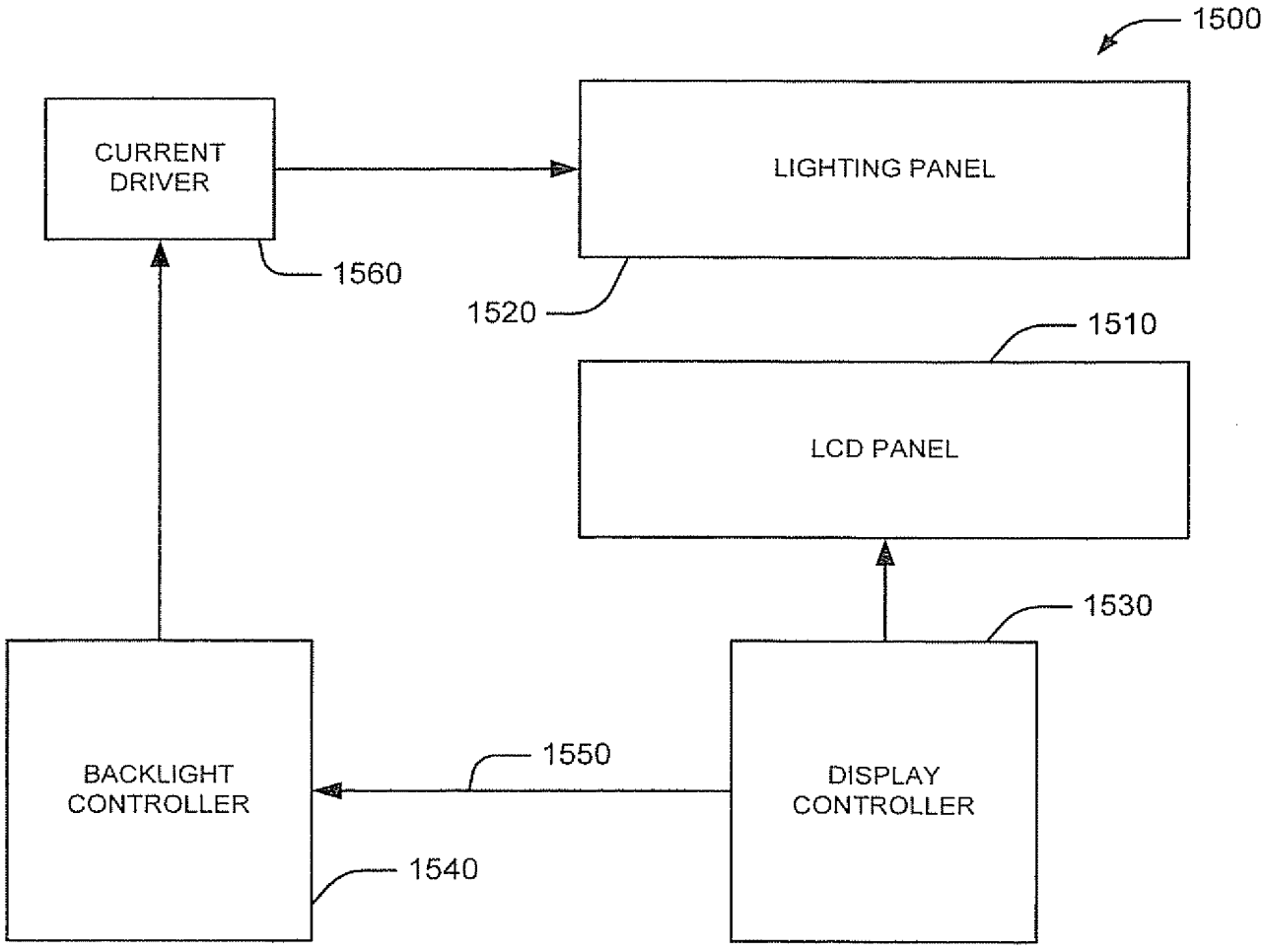


FIGURE 15

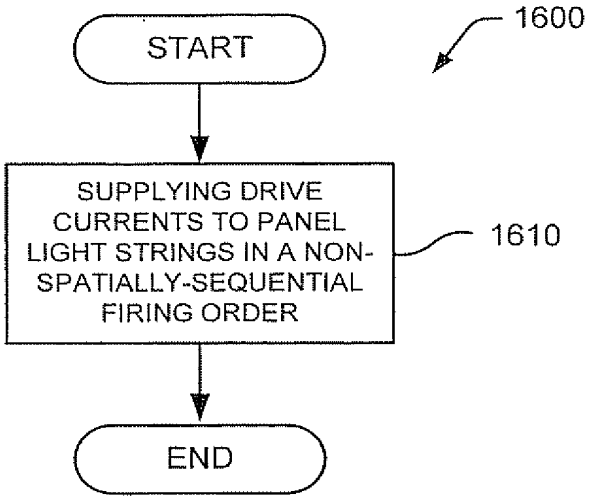


FIGURE 16

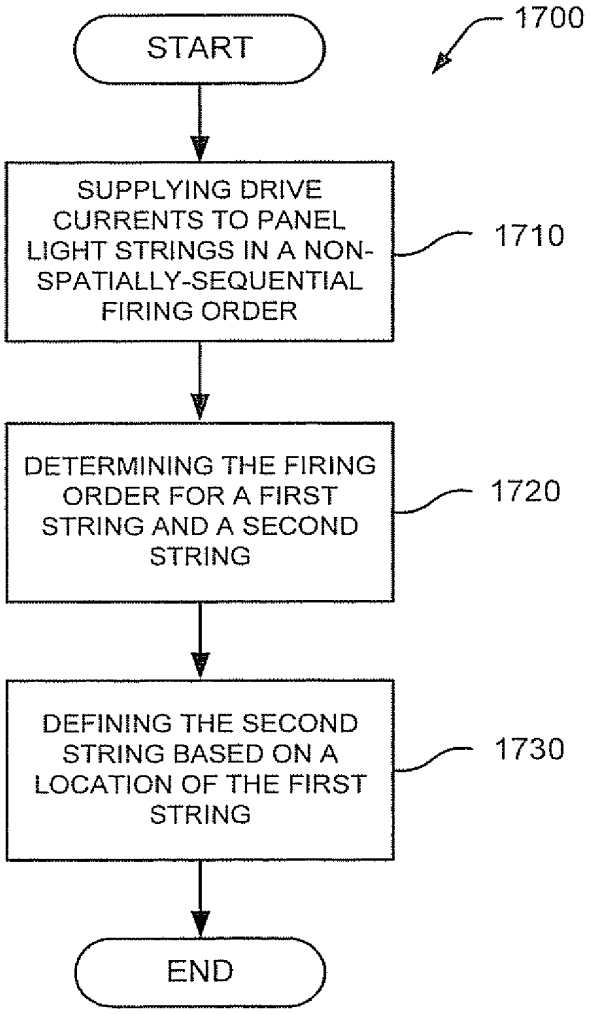


FIGURE 17

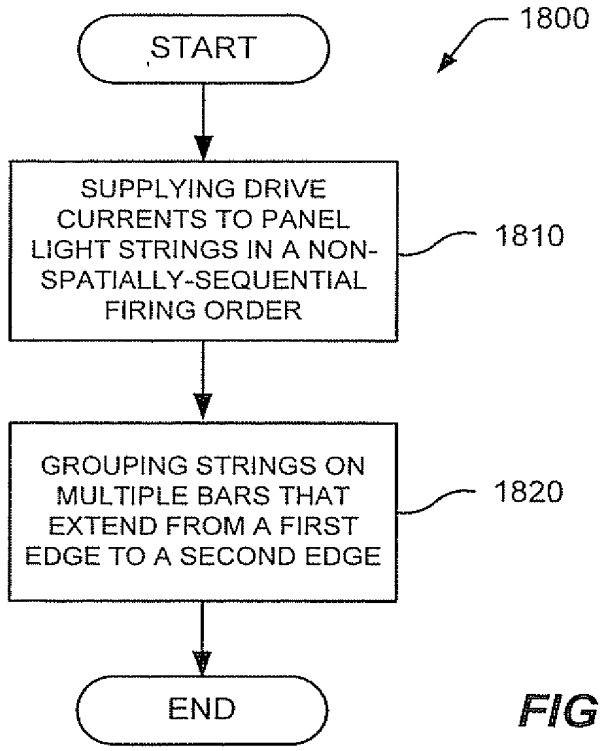


FIGURE 18

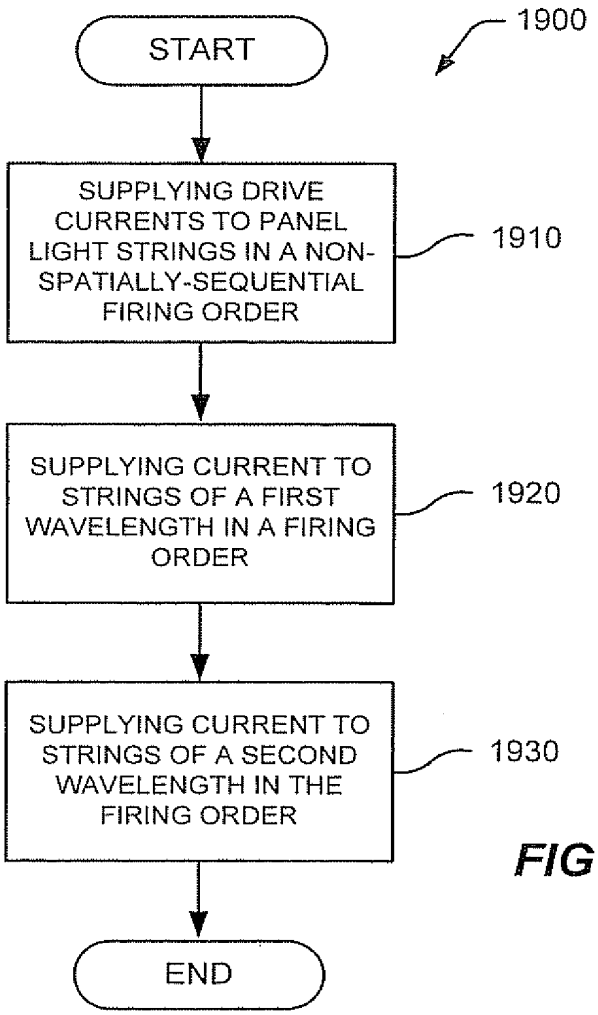


FIGURE 19

2000

2010 COLOR	2020 FIRING SEQUENCE	2030 STRING # (TOP TO BOTTOM)	2040 SPATIAL DELTA FROM PREVIOUS FIRING
RED	1	4	3
RED	2	7	-5
RED	3	2	6
RED	4	8	-3
RED	5	5	4
RED	6	9	-6
RED	7	3	3
RED	8	6	-5
RED	9	1	3
GREEN	10	4	3
GREEN	11	7	-5
GREEN	12	2	6
GREEN	13	8	-3
GREEN	14	5	4
GREEN	15	9	-6
GREEN	16	3	3
GREEN	17	6	-5
GREEN	18	1	3
BLUE	19	4	3
BLUE	20	7	-5
BLUE	21	2	6
BLUE	22	8	-3
BLUE	23	5	4
BLUE	24	9	-6
BLUE	25	3	3
BLUE	26	6	-5
BLUE	27	1	3

FIGURE 20

Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	Systems and Methods for Controlling a Solid State Lighting Panel
First Named Inventor/Applicant Name:	John Roberts
Filer:	Timothy Jennings Wall/Michele McMahan
Attorney Docket Number:	5308-703

Filed as Large Entity

Utility Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Utility application filing	1011	1	300	300
Utility Search Fee	1111	1	500	500
Utility Examination Fee	1311	1	200	200
Pages:				
Claims:				
Claims in excess of 20	1202	35	50	1750
Independent claims in excess of 3	1201	2	200	400
Miscellaneous-Filing:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**3150**

Electronic Acknowledgement Receipt

EFS ID:	1755179
Application Number:	11745713
International Application Number:	
Confirmation Number:	1290
Title of Invention:	Systems and Methods for Controlling a Solid State Lighting Panel
First Named Inventor/Applicant Name:	John Roberts
Customer Number:	65106
Filer:	Timothy Jennings Wall/Michele McMahan
Filer Authorized By:	Timothy Jennings Wall
Attorney Docket Number:	5308-703
Receipt Date:	08-MAY-2007
Filing Date:	
Time Stamp:	15:21:20
Application Type:	Utility

Payment information:

Submitted with Payment	yes
Payment was successfully received in RAM	$3150
RAM confirmation Number	169
Deposit Account	500220

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)	Multi Part /.zip	Pages (if appl.)

1		5308_703_App_Package.pdf	1786903	yes	52

Multipart Description/PDF files in .zip description		
Document Description	**Start**	**End**
Transmittal of New Application	1	2
Specification	3	29
Claims	30	39
Abstract	40	40
Drawings	41	52

Warnings:

Information:

2	Fee Worksheet (PTO-06)	fee-info.pdf	8563	no	2

Warnings:

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Total Files Size (in bytes):	1795466

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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

518107

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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PATENT APPLICATION FEE DETERMINATION RECORD
Substitute for Form PTO-875

11/745,713

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))							300
SEARCH FEE (37 CFR 1.16(k), (i), or (m))							500
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))							200
TOTAL CLAIMS (37 CFR 1.16(i))	55 minus 20 =	* 35	X$ 25		OR	X$50	1750
INDEPENDENT CLAIMS (37 CFR 1.16(h))	5 minus 3 =	* 2	X$100			X$200	400
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR						
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))			N/A			N/A	
			TOTAL			TOTAL	3150

* If the difference in column 1 is less than zero, enter "0" in column 2.

APPLICATION AS AMENDED – PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDI- TIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDI- TIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X =		OR	X =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X =		OR	X =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					N/A		OR	N/A	
					TOTAL ADD'T FEE		OR	TOTAL ADD'T FEE	

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDI- TIONAL FEE ($)	OR	RATE ($)	ADDI- TIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X =		OR	X =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X =		OR	X =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					N/A		OR	N/A	
					TOTAL ADD'T FEE		OR	TOTAL ADD'T FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
11/745,713	05/08/2007	2875	3150	5308-703	55	5

CONFIRMATION NO. 1290

65106
MYERS BIGEL SIBLEY & SAJOVEC, P.A.
P.O. BOX 37428
RALEIGH, NC27627

FILING RECEIPT

Date Mailed: 05/31/2007

Receipt is acknowledged of this regular Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please mail to the Commissioner for Patents P.O. Box 1450 Alexandria Va 22313-1450. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).**

Applicant(s)

John Roberts, Residence Not Provided;
Keith Vadas, Residence Not Provided;

Power of Attorney: None

Domestic Priority data as claimed by applicant

Foreign Applications

If Required, Foreign Filing License Granted: 05/31/2007

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US11/745,713**

Projected Publication Date: To Be Determined - pending completion of Missing Parts

Non-Publication Request: No

Early Publication Request: No

Title

Systems and Methods for Controlling a Solid State Lighting Panel

Preliminary Class

362

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the

Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371 (c) DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NUMBER
11/745,713	05/08/2007	John Roberts	5308-703

CONFIRMATION NO. 1290

FORMALITIES LETTER

65106
MYERS BIGEL SIBLEY & SAJOVEC, P.A.
P.O. BOX 37428
RALEIGH, NC 27627

Date Mailed: 05/31/2007

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The oath or declaration is missing. *A properly signed oath or declaration in compliance with 37 CFR 1.63, identifying the application by the above Application Number and Filing Date, is required.*
  Note: If a petition under 37 CFR 1.47 is being filed, an oath or declaration in compliance with 37 CFR 1.63 signed by all available joint inventors, or if no inventor is available by a party with sufficient proprietary interest, is required.

The applicant needs to satisfy supplemental fees problems indicated below.

The required item(s) identified below must be timely submitted to avoid abandonment:

- To avoid abandonment, a surcharge (for late submission of filing fee, search fee, examination fee or oath or declaration) as set forth in 37 CFR 1.16(f) of $130 for a non-small entity, must be submitted with the missing items identified in this letter.

SUMMARY OF FEES DUE:

Total additional fee(s) required for this application is **$130** for a non-small entity

- **$130** Surcharge.

Replies should be mailed to: Mail Stop Missing Parts
Commissioner for Patents

P.O. Box 1450
Alexandria VA 22313-1450

Registered users of EFS-Web may alternatively submit their reply to this notice via EFS-Web.
https://sportal.uspto.gov/authenticate/AuthenticateUserLocalEPF.html

For more information about EFS-Web please call the USPTO Electronic Business Center at **1-866-217-9197** or visit our website at http://www.uspto.gov/ebc.

If you are not using EFS-Web to submit your reply, you must include a copy of this notice.

Office of Initial Patent Examination (571) 272-4000, or 1-800-PTO-9199
PART 3 - OFFICE COPY

Attorney Docket No. 5308-703 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re: Roberts, et al.
Application No.: 11/745,713
Filed: May 8, 2007
For: *Systems and Methods for Controlling a Solid State Lighting Panel*

Confirmation No.: 1290
Group Art Unit: 2811

Date: July 13, 2007

Mail Stop MISSING PARTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO NOTICE TO FILE MISSING PARTS

Sir:

In response to the Notice to File Missing Parts of Application-Filing Date Granted (PTO-1533), mailed May 31, 2007 regarding the above-referenced patent application, enclosed is an executed Declaration and Power of Attorney document (3 pages) for this application.

The Commissioner is hereby authorized to charge $130.00 to Deposit Account No. 50-0220 for the surcharge under 37 C.F.R. § 1.16(f). This amount is believed to be correct. However, the Commissioner is hereby authorized to charge any deficiency or credit any overpayment to Deposit Account No. 50-0220.

If any extension of time for the accompanying response or submission is required, Applicant requests that this be considered a petition therefore.

Respectfully submitted,

Timothy J. Wall
Registration No. 50,743

Myers Bigel Sibley & Sajovec, P.A.
P. O. Box 37428
Raleigh, North Carolina 27627
Telephone: (919) 854-1400
Facsimile: (919) 854-1401
Customer No. 65106

CERTIFICATION OF TRANSMISSION

I hereby certify that this correspondence is being transmitted via the Office electronic filing system in accordance with § 1.6(a)(4) to the U.S. Patent and Trademark Office on July 13, 2007.

Signature: Michele P. McMahan

Michele P. McMahan

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled **"SYSTEMS AND METHODS FOR CONTROLLING A SOLID STATE LIGHTING PANEL"** the specification of which

☐ is attached hereto

OR

☒ was filed on May 8, 2007 as United States Application No. 11/745,713 or PCT

International Application Number _____ and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment specifically referred to above.

I acknowledge the duty to disclose information that is material to patentability as defined in 37 C.F.R. § 1.56, including for continuation-in-part applications, material information that became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

I hereby claim foreign priority benefits under 35 U.S.C. § 119(a)-(d) or (f), or § 365(b) of any foreign application(s) for patent, inventor's or plant breeder's rights certificate(s), or § 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below any foreign application for patent, inventor's or plant breeder's rights certificate(s), or any PCT international application having a filing date before that of the application on which priority is claimed.

NONE			☐ Yes ☐ No
Number	Country	MM/DD/YYYY Filed	Priority Claimed

Petitioner Hisense USA Corporation
Exhibit 1004 - Page 64 of 373

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below.

None	
Application Number(s)	Filing Date (MM/DD/YYYY)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following registered attorney(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

Send correspondence to: **Customer No. 65106**
Timothy J. Wall
Myers Bigel Sibley & Sajovec, P.A.
P. O. Box 37428
Raleigh, North Carolina 27627

Direct telephone calls to: Timothy J. Wall
(919) 854-1400
Facsimile: (919) 854-1401

Full name of first inventor: **John K. Roberts**

Inventor's Signature: John K Roberts Date: 5/17/2007

Residence: Grand Rapids, Michigan 49506-6524

Citizenship: United States of America

Mailing Address: 1061 Plymouth Avenue SE
Grand Rapids, Michigan 49506-6524

Petitioner Hisense USA Corporation
Exhibit 1004 - Page 65 of 373

Full name of second inventor: **Keith J. Vadas**

Inventor's Signature: K. J. V. Date: 2/9/07

Residence: ~~Lake Worth, Florida~~ Lowell, Michigan K. J. V.

Citizenship: United States of America

Post Office Address: ~~7202 Michigan Isle Road~~ ~~Lake Worth, Florida 33467~~ K. J. V.
11505 Cascade Road, SE
Lowell, Michigan 49331

Petitioner Hisense USA Corporation
Exhibit 1004 - Page 66 of 373

Electronic Patent Application Fee Transmittal

Application Number:	11745713
Filing Date:	08-May-2007
Title of Invention:	Systems and Methods for Controlling a Solid State Lighting Panel
First Named Inventor/Applicant Name:	John Roberts
Filer:	Timothy Jennings Wall/Michele McMahan
Attorney Docket Number:	5308-703

Filed as Large Entity

Utility Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Late filing fee for oath or declaration	1051	1	130	130
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
		Total in USD ($)		**130**

Electronic Acknowledgement Receipt

EFS ID:	1970045
Application Number:	11745713
International Application Number:	
Confirmation Number:	1290
Title of Invention:	Systems and Methods for Controlling a Solid State Lighting Panel
First Named Inventor/Applicant Name:	John Roberts
Customer Number:	65106
Filer:	Timothy Jennings Wall/Michele McMahan
Filer Authorized By:	Timothy Jennings Wall
Attorney Docket Number:	5308-703
Receipt Date:	13-JUL-2007
Filing Date:	08-MAY-2007
Time Stamp:	14:19:17
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment was successfully received in RAM	$130
RAM confirmation Number	6117
Deposit Account	500220

File Listing:

Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)

1		5308_703_ResponseMissingParts.pdf	250221 295fb7a94fd72723938a21af5cc71440ba9e4627	yes	4

Multipart Description/PDF files in .zip description		
Document Description	**Start**	**End**
Applicant Response to Pre-Exam Formalities Notice	1	1
Oath or Declaration filed	2	4

Warnings:

Information:

2	Fee Worksheet (PTO-06)	fee-info.pdf	8176 3478cc77bd111343449af41325fde0cfb003c75e	no	2

Warnings:

Information:

Total Files Size (in bytes):	258397

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO
11/745,713	05/08/2007	2875	3280	5308-703

CONFIRMATION NO. 1290

65106
MYERS BIGEL SIBLEY & SAJOVEC, P.A.
P.O. BOX 37428
RALEIGH, NC27627

UPDATED FILING RECEIPT

Date Mailed: 07/19/2007

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Filing Receipt Corrections. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

John K. Roberts, Grand Rapids, MI;
Keith J. Vadas, Lowell, MI;

Power of Attorney: None

Domestic Priority data as claimed by applicant

Foreign Applications

If Required, Foreign Filing License Granted: 05/31/2007

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US11/745,713**

Projected Publication Date: 11/13/2008

Non-Publication Request: No

Early Publication Request: No

Title

Systems and Methods for Controlling a Solid State Lighting Panel

Preliminary Class

362

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

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LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

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Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

Attorney Docket No. 5308-703 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re: John Roberts et al.
Application No.: 11/745,713
Filing Date: May 8, 2007
Confirmation No. 1290
Examiner: Richard A. Hjerpe
Group Art Unit: 2629
For: Systems and Methods for Controlling a Solid State Lighting Panel

Date: September 15, 2008

Mail Stop: Amendment
Commissioner for Patents
Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT COVER LETTER

Sir:

Attached is an Information Disclosure Statement listing of documents, together with a copy of any listed foreign patent document and/or non-patent literature. A copy of any listed U.S. patent and/or U.S. patent application publication is not provided herewith in accordance with 37 C.F.R. § 1.98(a)(2)(ii).

☐ In accordance with **37 CFR 1.97(b)**, the information disclosure statement is being filed:

☐ (1) within three months of the filing date of a national application other than a continued prosecution application under §1.53(d);

☐ (2) within three months of the date of entry of the national stage as set forth in §1.491 in an international application;

☐ (3) before the mailing of a first Office Action on the merits; or

☐ (4) before the mailing of a first Office Action after the filing of a request for continued examination under §1.114.

☐ In accordance with **37 CFR 1.97(c)**, the information disclosure statement is being filed after the period specified in 37 CFR 1.97(b) above, but before the mailing date of any of a final action under §1.113, a notice of allowance under §1.311, or an action that otherwise closes prosecution in the application, and is accompanied by **one** of the following:

☐ (1) The statement specified under **37 CFR 1.97(e)**, as follows:

☐ Each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement; **or**

☐ No item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in §1.56(c) more than three months prior to the filing of the information disclosure statement; **or**

☐ (2) The fee set forth in §1.17(p);

☒ In accordance with **37 CFR 1.97(d)**, the information disclosure statement is being filed after the period specified in 37 CFR 1.97(c) above, but on or before payment of the issue fee, and is accompanied by **both** of the following:

☒ (1) The statement specified under **37 CFR 1.97(e)**, as follows:

☒ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement; **or**

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in §1.56(c) more than three months prior to the filing of the information disclosure statement; **and**

☐ (2) The fee set forth in §1.17(p);

In accordance with **37 CFR 1.97(g)**, the information disclosure statement shall not be construed as a representation that a search has been made.

In accordance with **37 CFR 1.97(h)**, the information disclosure statement shall not be construed to be an admission that the information cited in the statement is, or is considered to be, material to patentability as defined in §1.56(b).

☐ The Director is hereby authorized to charge the fee specified in 37 C.F.R. § 1.17(p), and any fee deficiency or credit any overpayment, to Deposit Account No. 50-0220; or

☒ No fee is believed due. However, the Director is hereby authorized to charge any deficiency or credit any overpayment to Deposit Account No. 50-0220.

Respectfully submitted,

Timothy J. Wall
Registration No. 50,743
Attorney for Applicant(s)

Customer Number 65106
Myers Bigel Sibley & Sajovec, P.A.
P.O. Box 37428, Raleigh, NC 27627
919-854-1400
919-854-1401 (Fax)

CERTIFICATION OF TRANSMISSION

I hereby certify that this correspondence is being transmitted via the Office electronic filing system in accordance with § 1.6(a)(4) to the U.S. Patent and Trademark Office on September 15, 2008.

Paula J. Fisher

Name: Paula J. Fisher

INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Complete if Known	
				Application Number	11/745,713
				Filing Date	May 8, 2007
				First Named Inventor	John Roberts et al.
				Art Unit	2629
(use as many sheets as necessary)				Examiner Name	Richard A. Hjerpe
Sheet	A1	of	A1	Attorney Docket Number	5308-703

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No.	Document Number Number-Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1.	US- 2006/0139954 A1	06-29-2006	Kobori et al.	Pg.1; ¶ 5 – pg.5; ¶ 66; Figs. 1-12.
	2.	US- 6,459,919 B1	10-01-2002	Lys et al.	Whole Document
	3.	US- 2006/0176411 A1	08-10-2006	Furukawa	Pg.2; ¶ 27 - Pg.4; ¶ 54; Figs. 1, 2, 4-10.
	4.	US- 2005/0035728 A1	02-17-2005	Schanberger et al.	Pg.1; ¶ 14 – Pg.6; ¶ 56; Fig. 1.
	5.	US- 2002/0145392 A1	10-10-2002	Hair,III et al.	Pg.1, ¶ 6 – Pg.5; ¶ 47; Figs. 1-8.
		US-			
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FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No.	Foreign Patent Document Country Code, Number, Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T
	6.	WO 01/63977 A1	08-30-2001	Production Solutions, Inc.	Whole Document	Abstract

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(71) Applicant *(for all designated States except US)*: **PRODUCTION SOLUTIONS, INC.** [US/US]; 24 Hood Place, Cortlandt Manor, NY 10567 (US).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **FEHD, Brian** [US/US]; 123 Franklin Avenue, Suite R, Brooklyn, NY 11205 (US). **JANOWITZ, Marc** [US/US]; 123 Franklin Avenue, Suite R, Brooklyn, NY 11205 (US). **WSZOLEK, Raymond, C., III** [US/US]; 24 Hood Place, Cortlandt Manor, NY 10567 (US). **HUANG, Edmund** [CN/US]; 249 East Warren Common, Fremont, CA 94539 (US).

(74) Agents: **FANUCCI, Allan, A.** et al.; Pennie & Edmonds LLP, 1155 Avenue of the Americas, New York, NY 10036 (US).

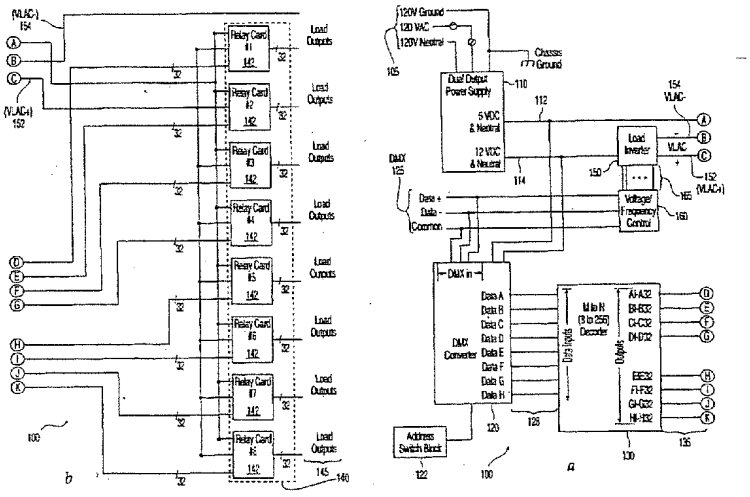
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(54) Title: SEQUENTIAL CONTROL CIRCUIT



(57) Abstract: A control circuit for driving a plurality of electrical loads, one at a time, has a converter circuit for receiving a DMX compatible digital control signal and extracting a plurality of address bits therefrom. A decoder circuit receives the digital address bits and generates a plurality of enable signals, each corresponding to a particular load. One of the load enable signals is in an active state and each other enable signal is in an inactive state at any one time. A relay circuit receives the enable signals, and in response passes an electrical drive signal to the electrical load corresponding to the enable signal that is in the active state. The relay circuit preferably includes a plurality of relay devices each coupled to one of the enable signals and a plurality of discharge circuits for rapidly discharging each electrical load when the enable signal corresponding to that load changes from the active state to the inactive state.

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SEQUENTIAL CONTROL CIRCUIT

CROSS REFERENCE TO RELATED APPLICATION

This application claims the benefit of priority from United States Provisional Patent Application No. 60/184,333 filed February 23, 2000 and entitled "Circuit Animator", the contents of which are incorporated herein by reference.

FIELD OF THE INVENTION

The present invention relates to a control circuit for driving and activating a plurality of electrical loads, especially electroluminescent loads such as electroluminescent fibers. More particularly, the present invention relates to a control circuit for sequentially driving such loads, one at a time (or one subset at a time), using the same power supply.

BACKGROUND OF THE INVENTION

Lighting controllers (e.g., lighting consoles or boards) are commonly found in theatrical, architectural, and entertainment venues. These controllers are operated by an individual and/or a computer system to activate and control relays, switches, dimmers, illuminators, and other control devices that are integrated within a lighting system. Those control devices are in turn connected to lighting devices (and possibly other devices such as mirrors, gobo wheels, and smoke machines) to operate or enable the lighting devices in a desired manner. In most lighting systems, controllers activate and interface with control devices using the Digital Multiplex (DMX) protocol. The DMX (or DMX-512) protocol is a digital control signal standard published by the United States Institute for Theatre Technology (USITT) and is used extensively within the lighting industry (a corresponding Analog Mulitplex, AMX or AMX-192, protocol also exists). A DMX signal can be used to control timed events, color changes, scene changes, and numerous other effects.

The current DMX control standard (established in 1986 and revised in 1990) provides up to 512 control channels per data link. Each device needs a certain number of DMX channels for proper operation. Some control devices require only one or two channels, while others may use 20 or more channels with separate channels controlling

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different effects such as activation, dimming, color, strobing, tilting, and rotation. Each control device in a lighting system is assigned a DMX start channel or address number (if a device uses several channels, those channels are addressed sequentially beginning at the start address). DMX channel assignment is typically achieved by setting a DIP (dual in-line package) switch on each control device. Once channels have been assigned, the devices are typically connected in a serial or daisy-chain configuration, in which the controller connects to an input of a first control device, an output of the first control device connects to an input of a second control device, and so on.

A DMX control signal provides data in an asynchronous serial format at 250 kbps via the industry standard RS-485 interface (also known as EIA-485). A typical DMX data packet includes a reset condition, followed by a start code and up to 512 bytes of control data, with one data byte for each channel. The start code is usually a "0" byte, however, a unique start code can also be used to indicate to a receiving device that a data packet containing proprietary information is being sent. Each channel byte in a packet provides information for controlling the corresponding device or device feature. Although the DMX standard was originally designed to carry dimmer information (i.e., information directly affecting the proportional output from a stage lighting dimmer), DMX control data has since evolved to carry information for moving lights, color changers, and a variety of other devices used within entertainment and architectural lighting industries. Typically, by programming or sliding a potentiometer on a control console, a control output can be varied from 0-100% (with 8-bit resolution).

The data packets in a DMX signal are transmitted continuously, optionally with no delay between packets. As a result, the fewer channels used, the higher the possible refresh rate in the DMX control signal. Generally, the number of channels used in a given lighting system will vary according to the needs of the lighting system, however many lighting controllers use only a fraction of all available DMX channels. A more thorough description of the DMX-512 protocol is provided by John Huntington in *Control Systems for Live Entertainment*, Focal Press (1994), relevant portions of which are incorporated herein by virtue of this reference.

DMX control channels are generally assigned on a one-to-one basis corresponding to the various outputs (devices or features) that need to be controlled. Power is routed to

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the dimming or switching control devices and then internally distributed to multiple outputs. Conventional DMX control devices used in the lighting industry can control from one to many thousands of outputs, either one at a time or in any combination of multiple outputs. As a result, these devices are capable of providing considerable design versatility and flexibility, especially in controlling a number of lighting devices simultaneously. However, conventional DMX control systems may be wasteful and inefficient for certain lighting applications. In particular, in many lighting systems it is often desirable to activate a large number of loads (such as electroluminescent fibers), one at a time (or one subset at a time), in a desired sequence or order. When such sequencing applications are performed using conventional DMX lighting control, a separate relay (or other control device) and separate power supply are generally used to activate and energize each lighting device or load. Consequently, at any one time during the sequencing, all but one of the power supplies is idle and unused, resulting in significant technical and economic inefficiencies.

Sequencing control systems for driving a plurality of loads using a single power supply have been developed. For example, Weiner et al. in United States Patent No. 4,215,277 describe a controller for sequentially energizing a plurality of light strings, each connected to an outlet receptacle via a triac switching device. A timing and logic circuit connects to a gating circuit for each triac switching device to provide selective energization of the triac and the corresponding light means connected to that triac. Similarly, Williams in United States Patent No. 4,410,794 discloses a switching system for sequentially connecting an alternating current supply to a plurality of loads, in particular heater loads in an aircraft de-icing system. The system includes a computer for generating switch selection data, in the form of serial bits, to a distributor arrangement that decodes the selection data and provides control signals to switch devices that connect the loads to the supply. The distributor arrangement includes a circuit for inhibiting the supply of control signals to the respective switch devices unless the voltage of the supply phase connected by the device is substantially zero. The control signals are also time-advanced with respect to the zero voltage condition so that the switch devices can be placed in states in which they can connect a load prior to disconnection of a preceding load.

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However, such prior art sequencing control systems are generally not compatible for operation with a DMX controller. This is disadvantageous since – given the wide spread adoption of the DMX protocol in the lighting industry – lighting designers, stage hands, theater electricians, architectural lighting consultants, and special effects designers are accustomed to programming DMX controllers and are familiar with the usage, distribution and maintenance of DMX systems. Compatibly with the DMX protocol also conveniently allows the same control signal used to effect the sequencing operation to also operate and activate other devices in a lighting system that are unrelated to the lighting devices being sequentially switched.

In addition, the intensity and color of electroluminescent loads, such as electroluminescent fibers, may be varied based on the voltage and frequency, respectively, of the power supply signal. For example, it may be desirable for the power supply signal to vary between 90-150 VAC and 400-2500 Hz to adequately exploit the potential for intensity and color variation in a fiber. However, the above described prior art sequencing control systems are generally unsuitable for efficiently switching between lighting devices that may be powered by a variable power supply signal having a relatively high rms voltage (e.g., up to 150 VAC or more) and high frequency (e.g., over 2 KHz). Although, the switching system of Williams switches between loads only when the voltage of the supply phase connected by the device is substantially zero, additional circuitry is needed to perform this function and limitations on the flexibility to switch between loads result.

Furthermore, it is often desirable for an electroluminescent load to appear as if it "snaps on" when enabled and "snaps off" when disabled, generally in a time less than or equal to 50 ms. Since an electroluminescent load effectively acts as a light emitting capacitor, when a driving voltage is removed from an electroluminescent load the voltage across the load discharges relatively slowly, making the snapping off effect difficult to achieve with the above described sequential control systems.

Consequently, there is a need for a control circuit that is capable of sequentially activating a plurality of electrical (particularly electroluminescent) loads in an efficient manner, that is capable of switching a relatively high voltage and frequency power supply signal between loads, that is able to provide a desired snap off effect when disabling a load, and that is compatible with DMX controllers and signaling. It would be further

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advantageous if such a control circuit used only a minimal number of DMX channels to sequentially control a large number of loads so that additional DMX channels or resources are available for controlling other devices and so that the DMX control signal is refreshed at a higher rate.

SUMMARY OF THE INVENTION

The present invention relates to a control circuit suitable for sequentially driving a plurality of electrical loads, such as electroluminescent loads in any desired order. The loads may be driven one at a time or one subset at a time.

In one aspect, the control circuit is preferably compatible with the standard lighting control signal protocol DMX-512, but alleviates many of the economic and technical burdens associated with conventional one-to-one DMX switching systems. In particular, when sequencing of plurality of electrical loads, it is not necessary to fully exploit the versatility offered in conventional DMX switching systems. In addition, it is not cost effective to use an individual power supply (such as an inverter, neon transformer, DC power supply, etc.) to drive each of the loads. The present invention exploits the convenience of using a DMX interface and control protocol but only requires a minimal number of DMX channels and only one inverter power supply (or other power source depending on load) to control and power the sequencing of a large number of outputs or loads. In another aspect, the control circuit permits the switching of an electrical drive signal (e.g., an inverter output voltage) between a plurality of electroluminescent loads in a rapid, efficient, and appropriate manner including the ability to "snap" loads on and off, even where the voltage and/or frequency of the electrical drive signal varies. The control circuit of the present invention is also preferably implemented in a modular configuration so that sequencing applications with varying numbers of loads can be easily accommodated.

Thus, in one embodiment, the present invention provides a control circuit for sequentially driving a plurality of electrical loads (e.g., one at a time) in which a converter circuit receives a DMX compatible digital control signal and extracts a plurality of address bits from that signal. A decoder circuit receives the digital address bits and in response generates a plurality of enable signals, each corresponding to a particular

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electrical load. At any one time, only a subset of the load enable signals is in an active state and each other enable signal is in an inactive state. In one embodiment, only one load enable signal can be active at any one time. A relay circuit then receives the plurality of enable signals, and in response passes an electrical drive signal, such as an inverter voltage, to each electrical load that corresponds to an enable signal that is in the active state.

Where the converter circuit extracts M address bits, the decoder circuit generates N enable signals, where N and M are integers with $N \leq 2^M$. In one preferred embodiment $N = 2^M$, e.g. M = 8 and N = 256. Preferably, the converter circuit extracts the plurality of address bits from data bytes for one or more DMX channels in the control signal. For example, the converter circuit may extract one address bit from a data byte for each of a plurality of DMX channels in the control signal. Alternatively, the converter circuit may extract the plurality of address bits from a data byte for a single DMX channel in the control signal (e.g., all eight channel bits). The converter circuit may comprise an address switch for specifying a DMX start channel.

The relay circuit may comprise a first plurality of relay devices, each coupled to one of the enable signals so that when that enable signal is in the active state, the electrical drive signal is coupled or passed to the corresponding electrical load. The first relay devices are preferably a solid state relay devices, but they may also be electromechanical relay device or any other type of relay devices. Especially in the case of electroluminescent loads, the relay circuit preferably also comprises a plurality of discharge circuits for rapidly discharging each electrical load when the enable signal corresponding to that load changes from the active state to the inactive state. Each discharge circuit preferably comprises a second relay device and also preferably establishes a low impedance shunt connection across the corresponding electrical load when the enable signal corresponding to that load changes from the active state to the inactive state.

The electrical drive signal may be an AC voltage signal and may have a variable frequency and/or voltage which are also controlled by other channels in the DMX control signal. In one implementation f the control circuit, the relay circuit is implemented on a plurality of boards, each board corresponding to a group of electrical loads. In another

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implementation, the decoder circuit and the relay circuit are implemented on a plurality of boards, each board corresponding to a group of electrical loads.

In another embodiment, the present invention provides a control circuit for sequentially driving a plurality of electroluminescent loads. The control circuit comprises a decoder circuit for receiving a digital address signal and in response generating a plurality of enable signals, each corresponding to a particular electrical load. Again, at any one time, only a subset of the load enable signals is in an active state and each other enable signal being in an inactive state. A relay circuit comprises a plurality of first relay devices each coupled to one of the plurality of enable signals as well as to the load corresponding to that enable signal. When that enable signal is in the active state, the relay device couples the electrical drive signal to the corresponding electrical load. The relay circuit also comprises a plurality of discharge circuits for rapidly discharging each electrical load when the enable signal corresponding to that load changes from the active state to the inactive state. Each discharge circuit comprises a second relay device, and both the first and second relay devices are preferably solid state relay devices.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred features of the present invention are disclosed, by way of example, in the accompanying drawings, wherein:

Figs. 1a-1b. are a block circuit diagram illustrating an overall architecture for a control circuit in accordance with a preferred embodiment of the present invention;

Figs. 2a-2c are a block circuit diagram illustrating a possible implementation for the M to N decoder circuit in the control circuit of Figs. 1a-1b;

Figs. 3a-3c are a block circuit diagram illustrating another possible implementation of the M to N decoder 130;

Fig. 4 is a circuit diagram of a portion of the relay circuit in the control circuit of Figs. 1a-1b in accordance with a preferred embodiment;

Fig. 5 is a timing diagram for several signals in Fig. 4; and

Fig. 6 is a circuit diagram of a portion of the relay circuit in accordance with another embodiment.

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DETAILED DESCRIPTION OF THE INVENTION

Figs. 1a-1b are a block diagram of a control circuit 100, in accordance with a preferred embodiment of the present invention, for sequentially driving a plurality of electrical loads in any desired order. Signal flow between Figs. 1a and 1b is identified by circle connectors A through K as shown. Sequential control circuit 100 is particularly suitable for driving electroluminescent loads or lamps such as electroluminescent fibers (e.g., LiveWire™ fibers), panels, or backlights. However, control circuit 100 may be used to control and sequence other types of electrical loads which include, but are not limited to, solenoids, loads used for pyrotechnical effect, ropelight loads, incandescent lamps, neon lamps, light emitting diodes, and loads used for confetti effects. Sequential circuit 100 generally forms part of an overall control device (not shown) and, as such, is preferably incorporated into an enclosure or housing for the device. Although, the control circuit 100 is particularly suitable for theater and architectural lighting and entertainment applications, it may be used for other types of applications as well.

Referring to Figs. 1a-1b, sequential control circuit 100 includes a power supply circuit 110, a DMX signal converter (or decoder) 120, an M-to-N address decoder circuit 130 (shown as a 8-256 decoder in the illustrated embodiment of Figs. 1a-1b), a relay circuit 140, an inverter circuit 150, and a voltage/frequency controller 160.

As shown in Figs. 1a-1b, power supply circuit 110 generally receives an AC supply signal 105, such as a conventional 120 VAC signal at 60 Hz as illustrated in Figs. 1a-1b. Alternatively, supply signal 105 may be a 240 VAC signal at 50 Hz or some other suitable power supply input signal that is preferably from 90-240 VAC at 50-60 Hz. The input power line providing signal 105 may be fused for over current protection, and a ground connection from the power line (e.g., through a ground conductor in a power cord) is preferably bonded to a chassis or enclosure of a controller device that houses control circuit 100 to ensure that all components are properly grounded where applicable. Power supply circuit 110 may include a main power switch (not shown), such as a lighted rocker style switch or equivalent.

In known manner, power supply circuit 110 converts input AC supply signal 105 into one or more DC output signals. In the illustrated embodiment of Figs. 1a-1b, circuit 110 is a dual output power supply that provides two DC output signals 112 and 114 (with

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corresponding ground or neutral references -- although only one line is shown in each case for the sake of clarity). As shown, signal 112 is a DC signal substantially at 5 VDC and 1 Amp that is provided for Vcc logic to DMX converter 120, address decoder circuit 130, and to relay circuit 140. Signal 114 is a DC signal substantially at 12 VDC and 1 Amp that is provided for Vcc logic to DMX converter 120 and, as a DC input, to inverter circuit 150. In alternate embodiments, power supply circuit 110 may only provide a single DC output, for example only signal 112 may be provided where DMX converter 120 is designed to operate with only 5VDC Vcc logic and inverter circuit 150 is similarly designed to generate a desired AC load voltage signal with a 5VDC input.

As illustrated in the preferred embodiment Figs. 1a-1b, in addition to signals 112 and 114, DMX converter circuit 120 receives a DMX control signal 125. As described above, a DMX control signals may be generated by an industry standard lighting controller (not shown) to control a number of lighting devices and/or other types of devices. DMX signal 125 is provided to converter 120 using standard DMX-compatible cable and connectors, such as a five-pin XLR connector (not shown). As shown in Figs. 1a-1b, the connector to converter 120 has a primary data true pin (Data +), a primary data complement pin (Data -), and a common or ground pin (Common). (Optionally, the cable and connectors may also support the transmission of secondary data from converter circuit 120 back to the lighting controller using pins reserved for reverse communication or "talk back" in advanced control systems.)

As shown in Figs. 1a-1b, DMX converter circuit 120 also comprises an address switch block 122, which may include a three digit push button switch or the like, for specifying a DMX start channel for converter 120. Address switch 122 is preferably mounted to allow re-addressing without having to open any device enclosure within which control circuit 100 is housed, for example by mounting address switch 122 on the front or rear panel of the device enclosure. More generally, DMX channel addressing may be achieved using any appropriate means, including a software setting. As described above, the DMX start channel address specifies to DMX converter circuit 120 which channels to monitor in DMX signal 125.

DMX converter circuit 120 outputs a plurality of M address bits 128 in parallel (each address bit 128 may be triggered using a solid state relay, not shown). The address

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bits are used to specify the particular output or load that is being driven by circuit 100 at any one time. As will be appreciated, depending on the application, each load may comprise one or more devices that are to be activated at the same time. Furthermore, although in the illustrated embodiment, the loads are sequentially driven one load at a time, it is alternatively possible, as described in more detail below, for different subsets of loads to be sequentially drive. In the embodiment specifically illustrated in Figs. 1a-1b, eight address bits 128 are generated (Data A through Data H) so that up to $2^8 = 256$ outputs or loads can be sequentially driven by circuit 100. As will be appreciated by those skilled in the art, the total number of potential outputs in circuit 100 is equal to 2^M, so that if an additional address bit 128 is provided, the number of potential outputs in circuit 100 may be doubled. In this invention, M can be any integer greater than or equal to one and N can be any integer greater than or equal to two.

In one embodiment, the M-bit address information is provided on M DMX channels in DMX control signal 125. DMX converter circuit 120 then decodes the M DMX channels, beginning at the start channel specified by address switch block 122, into M distinct address bits (preferably, as 5VDC signals). The address information may be encoded, for example, into the first bit of each of the M DMX channel data bytes (as described below, the other bits in each of the M channels may be used to provide additional control information). As noted above, each DMX data packet can potentially be decoded into as many as 512 channels, so that as many as 512 channels can be used to provide additional address bits to expand the number of outputs. In addition, channels in DMX signal 125 that are not used by DMX converter 120 may also be used to control additional devices in a lighting system. Where M = 8 (or less) in this embodiment, DMX converter circuit 120 may comprise the MR6-SSR circuit board manufactured by Fleenor Design in Arroyo Grande, California; however, other suitable decoder circuits may also be used.

In an alternative embodiment, instead of using M DMX channels to generate the M address bits 128, DMX converter 120 may alternatively be configured to use only one DMX channel to drive up to 256 outputs or loads. In this embodiment, the address information is encoded in all eight bits of the DMX channel byte (or as many of the channel bits as are needed to drive the number of outputs or loads in circuit 100, e.g., if

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128 or less outputs are needed only seven channel bits are required). Thus, where M = 8, the eight bits in the dedicated DMX channel byte correspond directly to the Data A through Data H bits 128, and DMX converter circuit 120 converts the address bits from the DMX serial format to the parallel output format of bits 128. As will be appreciated, the use of a second DMX channel to provide more than 8 bits of address information allows DMX converter 120 to support up to over 65,000 outputs or loads. Again, the DMX channel (or channels) containing the output address information is specified by the start channel address set in block 122. Advantageously, in this embodiment, fewer DMX channels are needed to encode the address information for N outputs than in the embodiment that uses M DMX channels. Furthermore, the amount of programming time necessary for an end user to select a desired output through a lighting controller is also reduced, i.e., instead of programming (or sliding) M potentiometers, a user need only program one potentiometer on a lighting controller to select one of up to 256 outputs (or two potentiometers to select one of up to more than 65,000 outputs).

As a further alternative, sequential control circuit 100 may receive a dedicated control or address signal (not shown) instead of DMX control signal 125. In this case, circuit 100 does not require DMX converter circuit 120. For example, control circuit 100 may receive an M-bit address signal generated by a DIP switch or a dedicated controller, eliminating the need for DMX decoding. In this embodiment, if the dedicated control or address signal is provided in a parallel format it may be sent directly to M to N decoder 130. Alternatively, if the control signal is sent in a serial format, a serial-to-parallel converter circuit may be employed to provide the M address bits in parallel format to decoder 130.

Referring still to Figs. 1a-1b, the M address bits 128 (Data A-H) are provided to M to N decoder circuit 130, which decodes the address bits into N decoder output or enable signals 135, where $N \leq 2^M$. As indicated, in the specific embodiment illustrated in Figs. 1a-1b, M = 8 and N = 256. Once decoded, all but one of decoder output signals 135 are in a first or enable state while all of the other N-1 decoder output signals 135 are in a second or disable state. Each decoder output signal 135 corresponds, on a one-to-one basis, with an output 145 used to drive a load (or group of loads) connected to control circuit 100. Therefore, only one load output 145 can be enabled at a time by a decoder

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output signal 135. Possible implementations of M to N decoder circuit 130 are described below in connection with Figs. 2a-2c and Figs. 3a-3c respectively.

It will be appreciated that DMX control signal 125 (or any other control signal input to circuit 100) can be programmed using a lighting controller to sequence or switch between any outputs 145 or loads in any desired order. The time to switch from one output 145 to the next in a desired sequence is dependent on the timing of address changes in address bits 128, and, the timing of address changes can also be programmed into the DMX signal 125 (or other control signal). For example, it may be desirable to switch or sequence the driving of a number of electroluminescent loads at between 50 milliseconds and 1 second, to provide a desired lighting effect. In addition, as discussed below, the ability to switch between loads at a high rate or speed, as well as the ability to "snap-off" a previously activated load, may also be affected by the operation of relay circuit 140 as well as the type of loads being sequenced.

Each decoder 130 output signal 135 is provided to relay circuit 140 where the corresponding load output signal 145 is generated, as shown in Figs. 1a-1b. Relay circuit 140 also receives the 5VDC signal 112 from power supply circuit 110 as well as the signal on one of the output lines 152 and 154 that provides a differential output AC drive voltage VLAC from inverter circuit 150. In the illustrated embodiment, inverter output line 152 (or VLAC+) is provided to relay circuit 140 while inverter output line 154 (or VLAC-) is provided directly to each load. (Thus, inverter output line 152 may be considered a hot lead while inverter output line 154 may be considered a neutral lead that is bussed out to each load.) Thus, as described in further detail below, relay circuit 140 effectively acts to relay or gate the VLAC drive voltage, in particular the signal on VLAC output line 152. As a result, the output voltage applied to each load is provided between each load output 145 (the relayed version of the signal on output line 152) and output line 154. Importantly, relay circuit 140 enables the voltage applied to each load to be switched in a rapid, efficient, and appropriate manner.

Depending on the types of components used in relay circuit 140 and on the number N of output signals 145, it may be preferable to physically implement relay circuit 140 on a plurality of different relay circuit cards 142, as shown in Figs. 1a-1b. Where this occurs, each relay circuit card 142 receives a group of decoder output signals

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135 and provides a corresponding group of load outputs 145. For example, in Figs. 1a-1b, where N = 256 outputs are provided by circuit 100, the decoder outputs 135 and load outputs 145 are grouped into eight groups of 32 signals. As described in more detail below, relay circuit cards 142 may each also include a part of M to N decoder circuit 130 thereon (so that decoder 130 is implemented in a decentralized manner, as opposed to on a separate decoder 130 card).

Referring still to Figs.1a-1b, inverter circuit 150 is a standard DC-AC inverter well known to those of ordinary skill in the art, such as an inverter manufactured by Inverter Design Inc. of Texas or Endicott Research Group in New York. Inverter circuit 150 receives the 12VDC signal 114 as a DC input and provides AC voltage VLAC between terminals 152 and 154 as an output. When used to drive electroluminescent loads, particularly electroluminescent fibers, inverter circuit 150 is preferably able to generate a VLAC signal within the following parameter ranges: 90-150 VAC in rms voltage, 50-100 mA in rms current, and 400 to 2500 Hz in frequency. It will be appreciated that other types of power supplies capable of generating a suitable output for driving an electrical load can also be used in place of inverter circuit 150.

As also shown in Figs. 1a-1b, a voltage/frequency control device 160 preferably receives DMX control signal 125 and in response provides control signals 165 to inverter circuit 150. In known manner, control device 160 may act as a dimmer by, for example, generating a control signal 165 that regulates the DC voltage input to inverter circuit 150 (i.e., signal 114 in Figs. 1a-1b). This enables the amplitude of the output voltage applied to an electroluminescent load (or other dimmable load), and thereby the load's apparent brightness or intensity, to be varied. Similarly, control device 160 may act as a color changer by generating one or more control signals 165 that modulates the frequency of VLAC (and therefore also of the load output voltage) to change the color emitted by an electroluminescent load. For example, in known manner, control signals 165 may gate switches in a bridge circuit in inverter 150 to control how often the direction of current through the bridge changes (and thereby the period or frequency of VLAC). For other type of loads, control device 160 may vary the voltage and/or frequency of VLAC to adjust other load effects that are dependent on those signal parameters.

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As noted above, DMX control signal 125 can conveniently include the necessary data for control device 160 to alter the load effects in a desired manner. In a preferred embodiment, control data for device 160 is provided within one or DMX channels (similar to converter 120, control device 160 may also have an DMX address switch for specifying a DMX start channel). For example, one DMX channel may contain information for regulating the rms voltage of VLAC, while another DMX channel may contain information for regulating the frequency of VLAC. Alternatively, where address bit 128 information in encoded as a single bit in each of M DMX channels, the other seven bits in each of those channels may contain voltage and/or frequency control information for inverter 150. Optionally, in this case, DMX converter 125 and control device 160 may be combined into a single device. Additional DMX channels in signal 125 can further be used to control the functionality of a ballast (e.g., for neon loads) or to control other electrical loads/devices independently of control circuit 100, allowing control circuit 100 to be used in a versatile and flexible manner within an application. Although the use of a DMX control signal is preferred due to the facility with which it enables different types of control information to be combined within a single signal, it will nevertheless be appreciated that other types of control signals may be used to control device 160 (as well as to provide address bits 128 as described above)

Figs. 2a-2c are a block diagram illustrating one possible implementation of M to N decoder circuit 130 for the specific case of M = 8 and N = 256. Signal flow between Figs. 2a, 2b, and 2c is identified by circle connectors L through V as shown. In this embodiment decoder circuit includes a first 4-16 decoder 210 and 16 additional 4-16 decoders 220 (only four decoders 220-1, 220-2, 220-3, and 220-4 are shown in Figs. 2a-2c) that are preferably implemented on a centralized decoder circuit board. Decoder circuit 130 receives the eight address bits 128 (Data A through Data H), for example via an 8-way male pin header. As shown, each of the signals carrying address bits Data A through Data H is preferably connected to ground (i.e., the neutral reference for the 5 VDC signal 112) through a resistor, R201 through R208 respectively. Resistors R201 through R208 (each of which may, for example, have a resistance of 1 KΩ) help ensure a true zero condition for all low data states of address bits 128.

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Referring to Figs. 2a-2c, address bits Data A to Data D are provided to decoder 210 while address data bits Data E to Data H are provided to each decoder 220. In response to address data bits Data A to Data D, one of outputs /Y0 to /Y15 of decoder 210 is set low while the other outputs are set high. An active low enable pin 212 of decoder 210 is connected to ground, and an active low input latch enable pin 214 of decoder 210 is connected to the 5VDC signal 112 (i.e., VCC). In this manner, decoder 210 is always enabled and the input address bits Data A to Data D are not latched, so that the outputs /Y0 to /Y15 of decoder 210 change as the address bits Data A to Data D change.

Outputs /Y0 to /Y15 of decoder 210 are connected to the active low enable pins 222 of decoders 220-1 to 220-16 respectively, so that only one decoder 220 is enabled at one time (the enabled decoder 220-i corresponds to the decoder 210 output that is set low by address bits Data A to Data D). In response to address data bits Data E to Data H, one of outputs Y0 to Y15 of the enabled decoder 220 is set high (active) while the other outputs are set low. The outputs Y0 to Y15 of each decoder 220 together provide the N decoder outputs 135 that are provided to relay circuit 140. Again, only one of outputs 135 is active or enabled at any one time. The active low input latch enable pin 224 of each of decoders 220 is connected to the 5VDC signal 112 (i.e., VCC), so that so that the outputs Y0 to Y15 of the enabled decoder 220 change as the address bits Data E to Data H change.

To illustrate, address bits Data A through Data D may enable a particular decoder 220 as set out in Table I below.

Address Bits 128 Data A - Data D				Enables 4-16 decoder
D	C	B	A	
0	0	0	0	220-1
0	0	0	1	220-2
0	0	1	0	220-3
0	0	1	1	220-4
0	1	0	0	220-5
0	1	0	1	220-6
0	1	1	0	220-7

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0	1	1	1	220-8
1	0	0	0	220-9
1	0	0	1	220-10
1	0	1	0	220-11
1	0	1	1	220-12
1	1	0	0	220-13
1	1	0	1	220-14
1	1	1	0	220-15
1	1	1	1	220-16

Table I

Similarly, address bits Data E through Data H may provide an active output in the enabled decoder 220-as set out in Table II below.

Address Bits 128 Data E - Data H				Output of enabled 4-16 Decoder 220-i
H	G	F	E	
0	0	0	0	Y0
0	0	0	1	Y1
0	0	1	0	Y2
0	0	1	1	Y3
0	1	0	0	Y4
0	1	0	1	Y5
0	1	1	0	Y6
0	1	1	1	Y7
1	0	0	0	Y8
1	0	0	1	Y9
1	0	1	0	Y10
1	0	1	1	Y11
1	1	0	0	Y12
1	1	0	1	Y13
1	1	1	0	Y14
1	1	1	1	Y15

Table II

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In the embodiment of Figs. 2a-2c, the 4-16 decoders 210 and 220 are preferably implemented using a high speed CMOS devices. For example, decoder 210 may comprise a Texas Instruments 74HC4515 integrated circuit (IC) with active low outputs while the 4-16 decoders 220 may each comprise a Texas Instruments 74HC4514 IC with active high outputs. Other chips of similar functionality may also be used (with some retrofitting and/or redesign of data routing, if necessary)

Figs. 3a-3c illustrate another possible implementation of a M to N decoder 130'. In this embodiment, rather than centralizing decoder ICs 210 and 220 onto one card or board (as is preferably done in the embodiment of Figs. 2a-2c), decoder circuit 130' may be decentralized onto a plurality of cards or boards 300. For the specific case of M = 8 and N = 256, decoder circuit 130' is provided on 16 separate cards, and Figs. 3a-3c show a circuit block diagram of the portion of decoder circuit 130' that resides on one of those cards. Optionally, the portion of decoder circuit 130' in Figs. 3a-3c may be combined with an associated portion or sub-circuit 400 of relay circuit 140 (shown in Fig. 4 and describe below) onto the same board 300. Decentralization of the decoder circuit in this manner conveniently provides for a broader and more flexible form of modularization, allowing the number of outputs or loads used in any given application of control circuit 100 to be varied by adding or removing such decoder/relay cards as necessary

Referring to Figs. 3a-3c, on each card 300, each decoder circuit portion 130' comprises a 4-bit comparator IC 310, a 4-16 decoder IC 320, and a 4-bit board address switch 330 in this specific embodiment. Also included on board 300 are an input/output (I/O) card 340 and a load connector 350, although the signal flow between Figs. 3a, 3b, and 3c is not shown for the sake of clarity. As indicated above, board 300 also preferably includes a portion 400 of relay circuit 140 as shown in Fig. 5, and in this case connector 350 is used to provide signals on load outputs 145 (that are generated on the particular board 300) to corresponding load devices (not shown).

As shown in Figs. 3a-3c, I/O card 340 receives the address bits 128 (Data A through Data H), the signals on lines 152 (VLAC+) and 154 (VLAC-), and the 5VDC and neutral signals 112 as inputs on to board 300. Four outputs 332, 334, 336, and 338 from switch 330 are, respectively, provided to inputs Q0, Q1, Q2, and Q3 of comparator 310. Board address switch 330 may be a rotary or equivalent style switch and provides a

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unique address (specified by outputs 332, 334, 336, and 338) for the board 300 on which switch 330 resides. Address bits Data A, Data B, Data C, and Data D are also provided as inputs P0, P1, P2, and P3 to comparator 310. Comparator 310 is configured or enabled (via a P = Q pin) to generate an active high output 312 when the board address specified by switch 330 matches the address specified by the address bits Data A through Data D. Comparator output 312 is inverted by an inverter 315 to provide an active low enable signal 314 to decoder IC 320. Decoder 320 receives address bits Data E, Data F, Data G, and Data H as inputs and generates an active low output on one of its outputs Y0 through Y15 in response. Again, only one decoder 320 output is low (the other outputs Y0 through Y15 are high) at any one time, and the relationship between address bits Data E through Data H and outputs Y0 through Y15 may be, for example, as set out in Table II above. As shown in Figs. 3a-3c, decoder outputs Y0 through Y15 provide load enable signals 135', referenced as /CH0 through /CH15, to a corresponding portion 400 of relay circuit 140, shown in Fig. 4.

As shown in Figs. 3a-3c, outputs 332, 334, 336, and 338 from switch 330 are also preferably connected to ground via a resistor R177, R178, R179, and R180 respectively, each of which may have a resistance of 5.1 kΩ. Capacitors C1 and C4 (each of which may have a capacitance of 0.1 μF) are also connected between the VCC and GND pins of comparator 310 and 4-16 decoder 320 respectively. In one implementation, comparator 310 may comprise a Texas Instruments 74HC85 IC 4-bit comparator, while decoder may comprise a 74HC154 IC which is a 4-16 decoder with active low outputs.

Referring now to Fig. 4, a portion or sub-circuit 400 of relay circuit 140 is shown in accordance with a preferred embodiment of the present invention. Each /CH load enable signal 135' generated in Figs. 3a-3c is provided to a corresponding relay sub-circuit 400 where the active low signal 135' is used to gate the application of the drive voltage VLAC to a load that also corresponds to the particular signal 135'. Thus, when incorporated onto a card 300 in the above described embodiment, each card 300 includes 16 sub-circuits 400, one for each /CH0 through /CH15 load enable signal 135'.

In addition to the active low load enable signal 135', relay sub-circuit 400 receives the VLAC+ signal on line 152 and the VLAC- signal on line 154 generated by inverter circuit 150 (as noted above these may be provided on to a modular board 300 via I/O card

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340). As shown in Fig. 4, the VLAC+ signal is coupled to a first terminal of a relay K1 via a cross-connected set of two diode pairs D2-D3 and D4-D5 and via a resistor R8. The second terminal of relay K1 is connected to the load output line 145. Relay K1 is preferably a solid state relay, such as an AD6C311 from Solid State Optronics, Inc, that is suitable to switch load driving signals that may have a relatively high voltage (e.g.90-150 VAC), and frequency (e.g., up to 2500 Hz). In known manner, when a sufficient threshold current flows through a light emitting diode (LED) 442 connected between the input terminals of relay K1, a pair of transistors 444 in relay K1 turn on to close the relay and effectively connect the first and second terminals of relay K1. Since the anode of LED 442 is coupled to the 5VDC signal or Vcc (i.e., signal 112) through a resistor R7, and since the cathode of LED 442 is connected to the load enable signal 135' or /CH, relay K1 closes when the load enable signal 135' or /CH is low or active. When relay K1 closes VLAC+ is coupled to output line 145 so that a voltage Vout can be provided to the corresponding load. Resistor R8 is preferably included to limit the current flowing through relay K1 when the latter is closed. As shown in Fig. 4, sub-circuit 400 may optionally include an indicator LED DS1 having an cathode connected to load enable signal 135' (/CH) and an anode coupled to 5 VDC (i.e.,Vcc) through a resistor R6. In this manner, when signal 135' is low or active, DS1 turns on and illuminates to provide a visual indication that the particular load is currently being driven.

As indicated above, it may be desirable to switch or sequence the driving of a plurality of electroluminescent loads at rates of up to one load every 50 milliseconds or faster to provide, for example, a desired lighting effect. Thus, relay K1 should be able to turn a load on and turn a load off at a rate that is faster than the sequencing rate between outputs. As indicated, the use of a solid state relay as opposed to an electromechanical one is generally preferable due to a solid state relay's smaller size and lack of moving parts. The AD6C311 solid state relay, for example, has a maximum turn-on or close time of 5 milliseconds and a maximum turn off time of 0.5 milliseconds. In addition, in many instances it is desirable for an electroluminescent load to appear as if it snaps on and snaps off. Again, the snapping on and snapping off may need to occur sufficiently faster than the sequencing rate between loads to ensure the desired effect. However, the snapping off effect is difficult to achieve in the case of electroluminescent loads, since

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these loads effectively act as light emitting capacitors, storing voltage or potential that must be discharged once the driving voltage Vout is removed or disabled. To facilitate the ability to rapidly sequence between loads and to permit the snapping off effect to be achieved for electroluminescent loads, relay sub-circuit 400 preferably includes a second relay for rapidly discharging the load upon the removal of the driving voltage VLAC.

Referring again to Fig. 4, the VLAC+ signal in sub-circuit 400 is also coupled to a first input of an optocoupler 410 via the cross-connected diode pairs D2-D3 and D4-D5 and a resistor R5. The VLAC+ signal is further directly connected to a second input of the optocoupler 410. A cross-connected pair of LEDS 414 and 416 are connected between the inputs of optocoupler 410, so that when sufficient current flows, in either direction, between those input terminals, a phototransistor 412 turns on. Optocoupler 410 may be an H11AA814 from Fairchild Semiconductor. When relay K1 is open, no current flows between the input terminals of optocoupler 410, and phototransistor 412 remains off (i.e., has a high impedance across it. However, when relay K1 is closed, current flows through LED 414 or LED 416 and phototransistor 412 turns on, so that optocoupler 410 effectively senses the flow of current into the load. It should be noted that diodes D2, D3, D4, and D5 are preferably included in sub-circuit 400 to prevent any overdrive of optocoupler 410, and similarly resistor R5 is preferably used to limit the current flowing through the input terminals of optocoupler 410.

Referring still to Fig. 4, phototransistor 412 in optocoupler 410 has an emitter coupled to ground and a collector coupled to 5VDC (i.e., Vcc) via a resistor R2. A capacitor C3 in series with a parallel combination of a resistor R4 and a diode D1 are also connected across phototransistor 412. More specifically, capacitor C3 has a first terminal connected to ground and a second terminal connected to a first terminal of resistor R4 and the anode of Diode D1, while the second terminal of resistor R4 and the cathode of Diode D1 are connected to the collector of phototransistor 412. The second terminal of capacitor C3, and therefore the voltage V_{C3}, is also connected to the input of an inverting Schmitt trigger 420. The output of inverting Schmitt trigger 420 is coupled through a resistor R3 to the base of a transistor Q1. The collector of transistor Q1 is coupled to the 5VDC (Vcc) signal through a resistor R1, while the emitter of Q1 is connected to ground. The collector of Q1 is also connected to a first terminal of capacitor C6. The second terminal of

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capacitor C6 is connected to the cathode of a diode D6, to a first terminal of a resistor R11, and to a first input of a NAND gate 430. The anode of diode D6 and the second terminal of resistor R11 are each connected to ground, so that D6 and R11 are connected in parallel. A second input of NAND gate 430 receives the active low enable signal 135' or /CH.

The output 435 of NAND gate 430 is coupled, via a resistor R9, to a second relay K2, that again is preferably a solid state relay and may also be implemented using a AD6C311 device. Thus, as shown, when a sufficient threshold current flows through a light emitting diode (LED) 452 connected between input terminals of relay K2, a pair of transistors 454 in relay K2 turn on to close the relay and effectively connect first and second terminals of relay K2. As shown, The first input of relay K2 (corresponding to the anode of LED 452) is connected to the 5 VDC (or Vcc) signal while the second input (corresponding to the cathode of LED 452) is coupled to output 435 of NAND gate 430. The first terminal of relay K2 is connected to the output line 145 signal while, the second terminal of relay K2 is coupled through a resistor R10 to the VLAC- signal 154. Thus, when output 435 of NAND gate 430 goes low, relay K2 closes, and a low impedance shunt connection is provided across the load.

In operation, when circuit 400 is in a steady state load off condition, load enable signal 135' (or /CH) is high, relay K1 is open, phototransistor 412 is off, and capacitor C3 is charged by the 5 VDC signal (through resistors R2 and R4) so that the voltage V_{C3} provided across capacitor C3 is high (substantially equal to Vcc). The output of inverting Schmitt trigger 420 provides a low signal at the base of transistor Q1, turning transistor Q1 off (the low output of Schmitt trigger 420 is triggered during the charging of C3, when the voltage V_{C3} rises above a threshold level, e.g., around 2.7 V). With Q1 off, capacitor C6 is charged by the 5 VDC signal (through resistors R1 and R11) so that the voltage V_{C6} provided across capacitor C6 is also high and substantially equal to Vcc. With V_{C6} high the voltage across resistor R11, V_{R11}, is at a low level. Since V_{R11}, an input to NAND gate 430, is low, the output 430 of NAND gate 435 is high and relay K2 is off.

When load enable signal 135' (/CH) goes low, i.e., becomes active, K1 turns on, coupling the VLAC+ signal 152 to output line 145. Current flows through cross-connected diode pair 414 and 416 in optoisolator 410, and in response phototransistor 412

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turns on. Diode D1 provides a low impedance path through which C3 can quickly discharge. As C3 discharges, the output of inverting Schmitt trigger 420 is triggered high, so that a high voltage is provided at the base of transistor Q1, turning transistor Q1 on. (To ensure that V_{C3} remains below a threshold voltage of inverting Schmitt trigger 420, the resistance of R2 and R4 and the capacitance of C3 is preferably chosen so that the time constant of that RC network, (R2 + R4)*C3, is substantially larger than one half period of the load driving signal VLAC.) With Q1 on, diode D6 provides a low impedance path through which C6 can quickly discharge. The voltage V_{R11} across resistor R11 remains low (as is load enable signal 135' (/CH) which is also provided as an input to NAND gate 430), and so the output 430 of NAND gate 435 stays high keeping relay K2 off. The voltage taken between the output line 145 and the inverter output voltage line 154 (VLAC-), Vout, is thereby provided to the load.

Fig. 5 is a timing diagram illustrating how the rapid load discharge circuitry in relay sub-circuit 400 operates in the case of an electroluminescent load. Fig. 5 shows waveforms for the load enable signal 135' (/CH), the voltage V_{C3} across C3, the voltage V_{R11} across R11, the output voltage 435 of NAND gate 430, and the load output voltage Vout (taken between lines 145 and 154). At the onset starting at time t0 in Fig. 5, load enable signal 135' (/CH) is low, C3 is discharged, V_{R11} is low, the output 435 of NAND gate 430 is high (maintaining relay K2 off), and Vout provides an AC voltage (essentially the VLAC output from inverter 150) to the load. At time t1, the active low enable signal 135' (/CH) disables the load by going high. As described above, phototransistor 412 turns off and C3 charges, i.e., V_{C3} rises. Also at time t1, the inverter 150 output VLAC+ signal is disconnected from the load by relay K1, and, as a result, the Vout voltage across the load starts to decrease as the electroluminescent load discharges the energy it stored during its activation. As illustrated in Fig. 5, however, the discharging of the electroluminescent load may take place relatively slowly.

Referring still to Fig. 5, at time t2 V_{C3} reaches an upper voltage threshold level of inverting Schmitt trigger 420, and Q1 is then triggered off. Subsequently, 5VDC is applied across resistor R1, capacitor C6, and resistor R11. Capacitor C6, consequently, begins to charge. Resistor R11 is preferably significantly larger than resistor R1 so that most of the 5VDC is distributed across resistor R11 and V_{R11} pulses to a high state when

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Q1 initially turns off. Since, at time t2, both inputs to NAND gate 430 (i.e., V_{R11} and load enable signal 135') are high, the NAND gate output 435 goes low, turning relay K2 on. As a result, a low impedance shunt is provided across the load enabling the residual voltage across the load to rapidly discharge, as shown after time t2 in the load voltage Vout. In the illustrated embodiment, the shunt impedance comprises the resistance between the connected terminals of relay K2 (which is relatively minimal) and the resistance of resistor R10. As will be appreciated, resistor R10 preferably has a relatively low resistance, however this resistance should also be high enough to limit the current flowing through relay K2 during the load discharge to sufficiently protect relay K2.

In the above manner, a desired snap-off effect can be provided for the electroluminescent load once application of the inverter drive voltage VLAC is disabled. As capacitor C6 continues to charge and V_{C6} increases, the V_{R11} voltage correspondingly decreases until it drops below a threshold voltage and provides a low input to NAND gate 430 at time t3. The NAND gate output 435 returns to a high state, opening relay K2 and removing the rapid load discharge shunt connection. The load then remains disabled until control circuit 100 once again activates the enable signal 135' for that load at time t4. When this occurs, relay K1 closes applying the VLAC+ signal to output line 145. Capacitor C3 also discharges since phototransistor 412 is turned on by the load current sensed by optoisolator 410. It will also be appreciated that, when load enable signal 135' goes high or inactive, as illustrated at time t1 in Fig. 5, the load enable signal should remain low at least until time t3 (plus the turn off time for relay K2) to ensure that VLAC+ is not coupled to output line 145 when K2 is closed or on. (Load enable signal 135' generally need only remain low or active long enough to accommodate the turn on time for relay K1.) Typically, such a minimum inactive time for load enable signal 135' may be about 20 milliseconds or less, which still allows rapid sequential energization, in any order, of a plurality of loads.

As an example, in one specific implementation, the components in relay sub-circuit 400 may have the following values: R1 = R2 = 5.1 kΩ; R3 = 2 kΩ; R4 = 240 kΩ; R5 = R8 = R10 = 47 Ω; R6 = R7 = R9 = 750 Ω; R11 = 56 kΩ; C3 = 0.047 μF; and C6 = 0.1 μF.

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In an alternative embodiment, Fig. 6 is a circuit diagram of a possible circuit 600 for implementing each relay board or card 142 in relay circuit 140 of Figs. 1a-1b. In the illustrated embodiment of Fig. 6, relay sub-circuit 600 on a card 142 receives 32 active high load enable signals 135 (labeled A1 through A32 in Fig. 6). Relay circuit 600 also receives the 5VDC and neutral (ground) signals 112 and the VLAC+ signal on line 152. Each load enable signal A1 through A32 is connected to the base of a transistor Q601 through Q632 respectively. Each load enable signal A1 through A32 is also coupled to ground, i.e. the neutral reference for the 5VDC signal 112, through a resistor R601 through R603 respectively. The collectors of each of transistors Q601 through Q632 are coupled to the 5 VDC or Vcc signal 112 (e.g., through resistors, not shown) while the emitters of transistors Q601 through Q632 are coupled to a first coil input of an electromechanical relay K601 through K632. As will be appreciated, when using circuit 100 to control non-electroluminescent loads, it may be necessary and/or desirable to use electromechanical relays in some cases. The other coil input of each electromechanical relay K601 through K632 is connected to ground. The coil of each relay is preferably a 5VDC relay coil. The inverter output signal VLAC+ 152 is coupled as a pass voltage to the common terminal of each relay K601 through K632.

In operation, when a load enable signal 135 goes high or active, the corresponding transistor is turned on, allowing current to flow through the transistor and through the coil of the corresponding relay. With the coil energized, the normally open connection closes coupling the VLAC+ signal on line 152 to a corresponding load (not shown). The inclusion of the transistor in the current path of the relay coil prevents the relay coil from drawing too much current (as would occur if the 5VDC coil were triggered by the logic signals 112 alone). In effect, each transistor Q601 through Q632 acts as a "pilot" for the corresponding relay coil voltage. As an alternative to the transistor/relay combination of Fig. 6, other switching and current limiting techniques may also be used. For example, relay circuit 600 may comprise "low energy" electromechanical relays designed to provide only a small amount of current through and voltage across its coil when triggered.

As indicated, control circuit 100 preferably are housed within a control device enclosure. Generally, the housed device is preferably of a reasonable size and weight for a given application, and may also conform to industry standards for mounting. However,

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when circuit 100 is used to drive a large number of loads, the dimensions and configurations of many of the components may be such that they may not fit on a single circuit board or card. Furthermore, it is often not desirable to install all the components on one board since this limits the flexibility of the control device. Consequently, as described above, components of circuit 100 may be grouped into various modules. For example with N = 256 loads, eight transistor/relay switching boards 600 (Fig. 6) may be used. Alternatively sixteen decoder/ switching boards 300, as described in connection with Figs. 3a-3c and Fig. 4, may be used. Similarly, DMX converter 120 can also be fitted onto a card or board and mounted in the housed device in any suitable manner. Within the device housing, the power supply and the various modules may be connected by any appropriate routing or bus technique to transfer power and signals within circuit 100. For example, two-way male headers or ribbon cables may be used with compatible connectors on the boards. (The housing preferably includes suitable input and output connectors as well, depending on the application and the types of loads being controlled.)

Modularization in the above manner conveniently allows an end user to use less loads and boards than the maximum N, while retaining the ability to subsequently insert additional boards to accommodate more loads or outputs. For example, if only 128 outputs are needed, only eight (and not 16) decoder/switching boards 300 are needed. A modular design also facilitates the replacement of faulty or damaged components. Thus, regardless of how many modules or how many switches the invention are configured, implementation of the control circuit of the present invention using modular elements is generally, although not always, preferential to an implementation incorporating a consolidation of all components. Where control circuit 100 is modularized onto several cards or boards, these are preferably of standard size that may fit into a card rack or the like in the control device.

In one embodiment of the invention, one of the output lines 145 (e.g., a "zero" addressed output line) may be connected to a "ghost" load that may, by default, be driven by circuit 100 in the absence of a control signal 125. In this case, a no load condition for inverter circuit 150 can be avoided. The ghost load preferably has the same draw as other loads connected to output lines 145 and may for example be a resistance or impedance network. The ghost load could also be the same type of device as the other loads. For

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instance, in the case of electroluminescent fiber loads, the ghost load may be a fiber located apart from the other fiber loads, e.g., so that the ghost load is visible to a lighting operator and not as part of an overall lighting display. In this manner, a ghost fiber load can provide a visual indication to the operator that the control circuit 100 is running before a sequencing operation begins. Furthermore, the ghost load can be used to introduce "dark steps"
at specific times during a sequential lighting operation when it is desired that no load in the lighting display be on. For example, for an intermittent effect, control circuit 100 may be programmed to drive the ghost load immediately after driving any other load.

In addition, although sequential control circuit 100 is described above as sequentially enabling one output line (or load) at a time, it will be appreciated that control circuit 100 can also be configured to sequentially drive subsets of output lines 145 (or loads). For example, in the embodiment illustrated in Figs. 3a-3c, the address switches 330 on two or more boards 300 may be set to specify the same address, so that when address bits Data A to Data D match that address, an output line connected to each board 300 identified with that address is enabled (i.e., the load on each board corresponding to the output line specified by address bits Data E to Data H). Subsets of output lines 145 (and hence loads) may also be activated at the same time in other ways. For example, subset grouping information for loads may be provided within the DMX control signal 125, and converter circuit 120 and decoder circuit 130 man be adapted to enable the simultaneous activation of subsets of output lines 145 at the same time. In all of these cases, the subset of loads being driven still changes sequentially as in the case of single load sequencing. Furthermore, where subsets of loads are sequenced sequentially, it will be appreciated that the inverter circuit 150 (or other power supply circuit used) must be capable of driving more than one load at the same time.

Although the preferred embodiments of the invention have been described in the foregoing description, it will be understood that the present invention is not limited to the specific embodiments described above.

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INSDOCID: <WO_____0163977A1_I_>

THE CLAIMS

What is claimed is:

1. A control circuit for sequentially driving a plurality of electrical loads comprising:

a converter circuit for receiving a DMX compatible digital control signal and extracting a plurality of address bits therefrom;

a decoder circuit for receiving the digital address bits and in response generating a plurality of enable signals, each corresponding to a particular electrical load, a subset of the load enable signals being in an active state and each other enable signal being in an inactive state at any one time;

a relay circuit for receiving the plurality of enable signals, and in response passing an electrical drive signal to each electrical load corresponding to the subset of enable signals that is in the active state.

2. The control circuit of claim 1 wherein the converter circuit extracts M address bits and the decoder circuit generates N enable signals, and wherein $N \leq 2^M$ where M and N are integers.

3. The control circuit of claim 2 wherein $N = 2^M$.

4. The control circuit of claim 1 wherein the converter circuit extracts the plurality of address bits from data bytes for one or more DMX channels in the control signal.

5. The control circuit of claim 1 wherein the converter circuit extracts one address bit from a data byte for each of a plurality of DMX channels in the control signal.

6. The control circuit of claim 1 wherein the converter circuit extracts the plurality of address bits from a data byte for a single DMX channel in the control signal.

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ISDOCID: <WO_____0163977A1_I_>

7. The control circuit of claim 1 wherein the converter circuit comprises an address switch for specifying a DMX start channel.

8. The control circuit of claim 1 wherein the relay circuit comprises a first plurality of relay devices each coupled to one of the enable signals as well as to the load corresponding thereto, wherein when said enable signal is in the active state the relay device couples the electrical drive signal to the corresponding electrical load.

9. The control circuit of claim 8 wherein each of the first relay devices comprises a solid state relay device.

10. The control circuit of claim 8 wherein each of the first relay devices comprises an electromechanical relay device.

11. The control circuit of claim 10 wherein each electromechanical relay device is coupled to one of the enable signals through a transistor.

12. The control circuit of claim 8 wherein the relay circuit further comprises a plurality of discharge circuits for rapidly discharging each electrical load when the enable signal corresponding to that load changes from the active state to the inactive state.

13. The control circuit of claim 12 wherein each discharge circuit comprises a second relay device.

14. The control circuit of claim 13 wherein each of the second relay devices comprises a solid state relay device.

15. The control circuit of claim 12 wherein each discharge circuit establishes a low impedance shunt connection across the corresponding electrical load when the enable signal corresponding to that load changes from the active state to the inactive state.

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3NSDOCID: <WO_____0163977A1_I_>

16. The control circuit of claim 1 wherein the electrical drive signal is an AC voltage signal.

17. The control circuit of claim 1 wherein the electrical drive signal is an AC voltage signal having a variable rms voltage.

18. The control circuit of claim 17 wherein the DMX compatible digital control signal further includes control information for varying the rms voltage.

19. The control circuit of claim 1 wherein the electrical drive signal has a variable frequency.

20. The control circuit of claim 19 wherein the DMX compatible digital control signal further includes control information for varying the frequency of the electrical drive signal.

21. The control circuit of claim 1 wherein the electrical loads are electroluminescent loads.

22. The control circuit of claim 1 wherein the relay circuit is implemented on a plurality of boards, each board corresponding to a group of electrical loads.

23. The control circuit of claim 1 wherein the decoder circuit and the relay circuit are implemented on a plurality of boards, each board corresponding to a group of electrical loads.

24. The control circuit of claim 1 wherein the subset of load enable signals in an active state at any one time consists of only one load enable signal.

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SDOCID: <WO_____0163977A1_I_>

25. A control circuit for sequentially driving a plurality of electroluminescent loads comprising:

a decoder circuit for receiving a digital address signal and in response generating a plurality of enable signals, each corresponding to a particular electrical load, a subset of the load enable signals being in an active state and each other enable signal being in an inactive state at any one time; and

a relay circuit comprising

a plurality of first relay devices each coupled to one of the plurality of enable signals as well as to the load corresponding thereto, wherein when said enable signal is in the active state the relay device couples the electrical drive signal to the corresponding electrical load.

a plurality of discharge circuits for rapidly discharging each electrical load when the enable signal corresponding to that load changes from the active state to the inactive state.

26. The control circuit of claim 25 wherein each discharge circuit comprises a second relay device.

27. The control circuit of claim 26 wherein each of the first and second relay devices comprises a solid state relay device.

28. The control circuit of claim 25 wherein each discharge circuit establishes a low impedance shunt connection across the corresponding electrical load when the enable signal corresponding to that load changes from the active state to the inactive state.

BNSDOCID: <WO_____0163977A1_I_>

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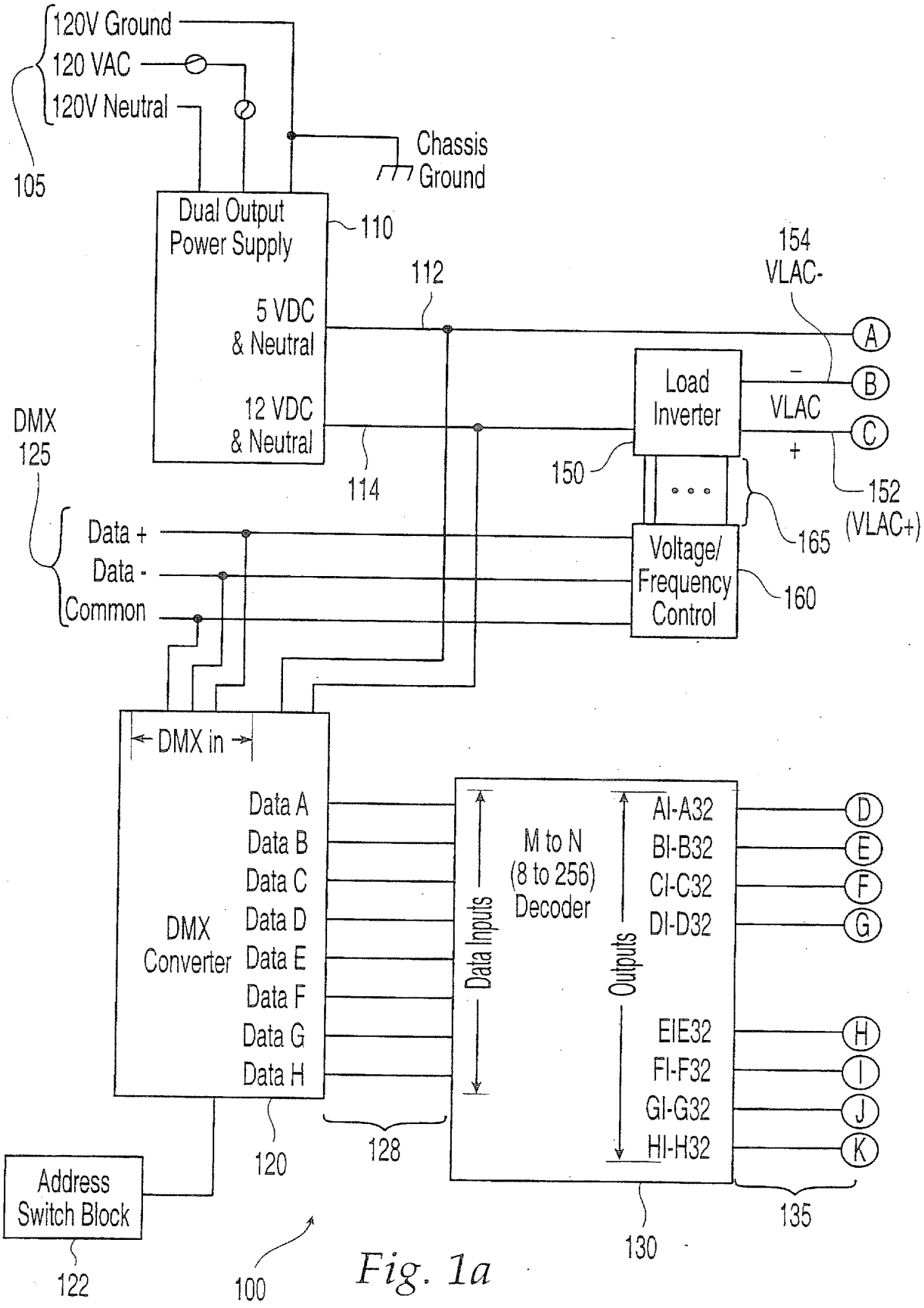


Fig. 1a

NSDOCID: <WO_____0163977A1_I_>

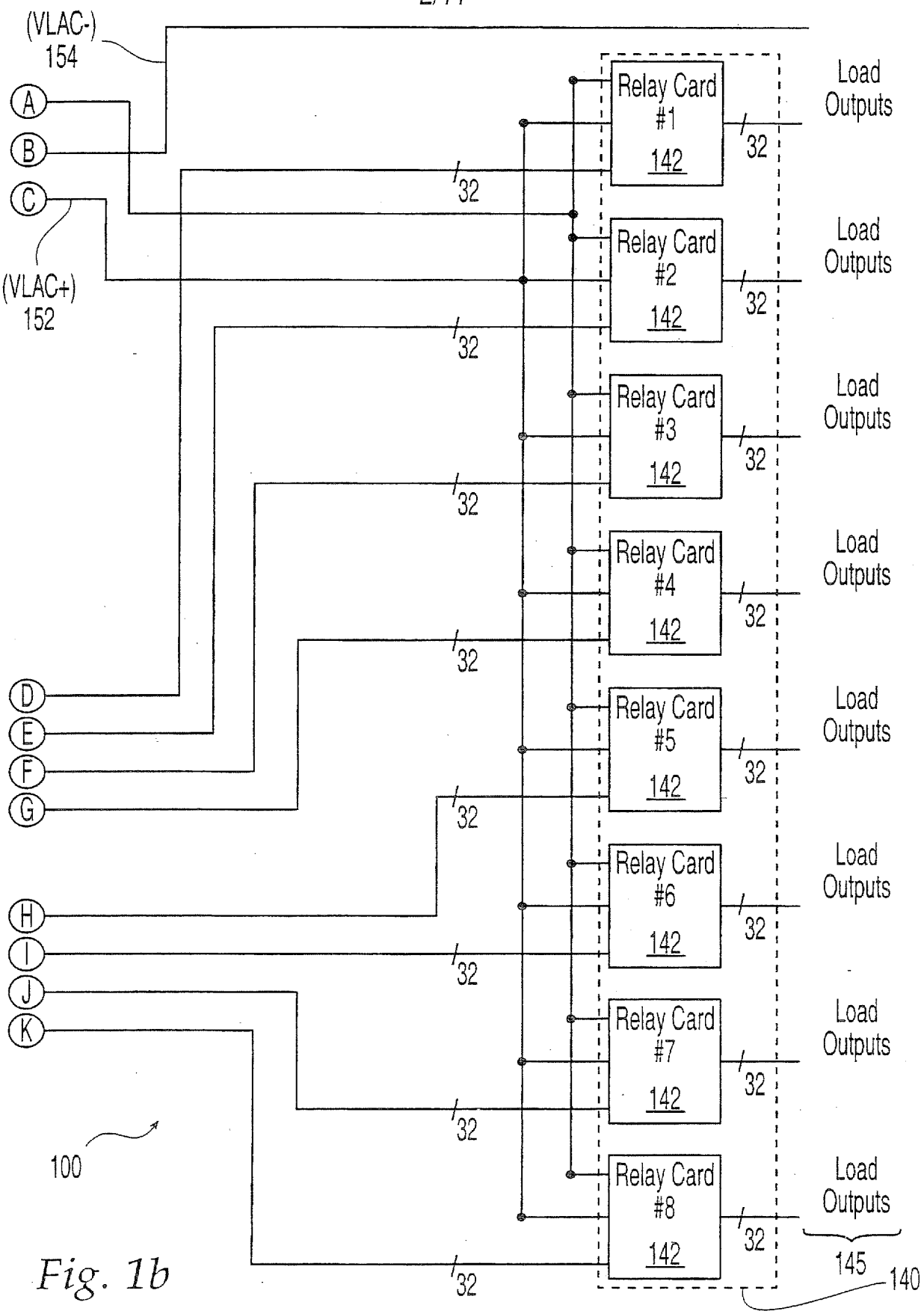


Fig. 1b

3NSDOCID: <WO_____0163977A1_I_>

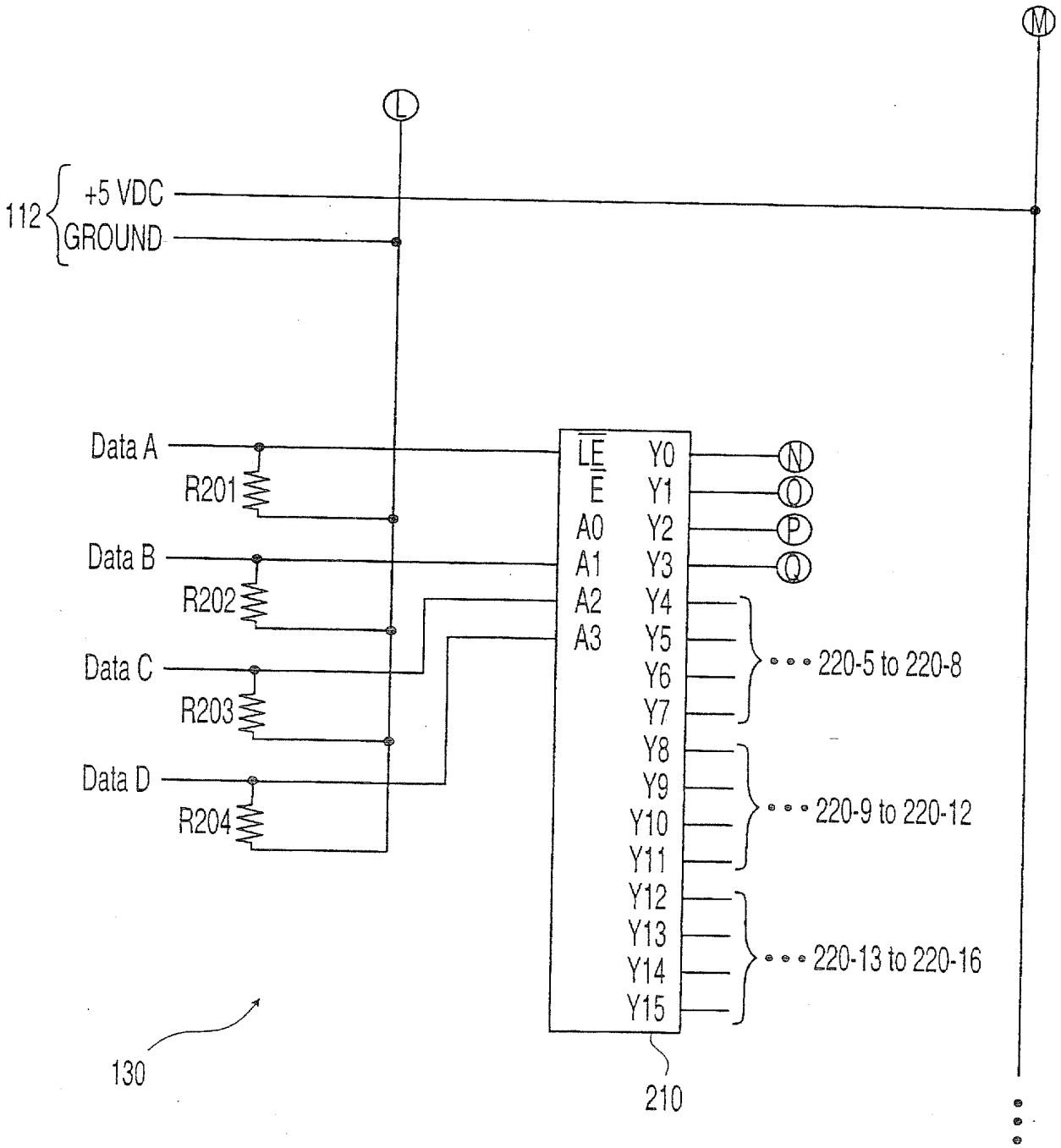


Fig. 2a

ISDOCID: <WO_____0163977A1_I_>

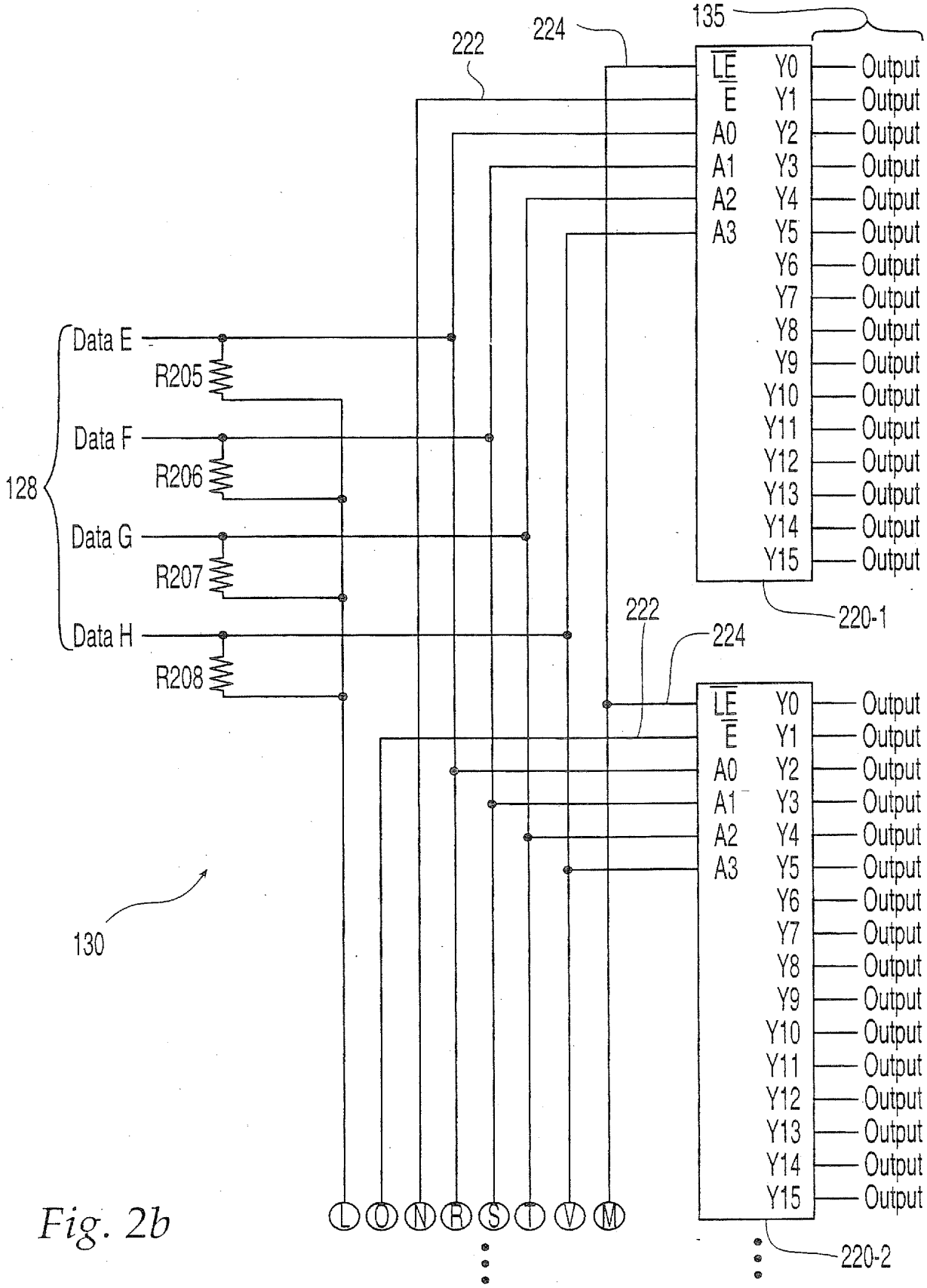


Fig. 2b

ENSDOCID: <WO_____0163977A1_I_>

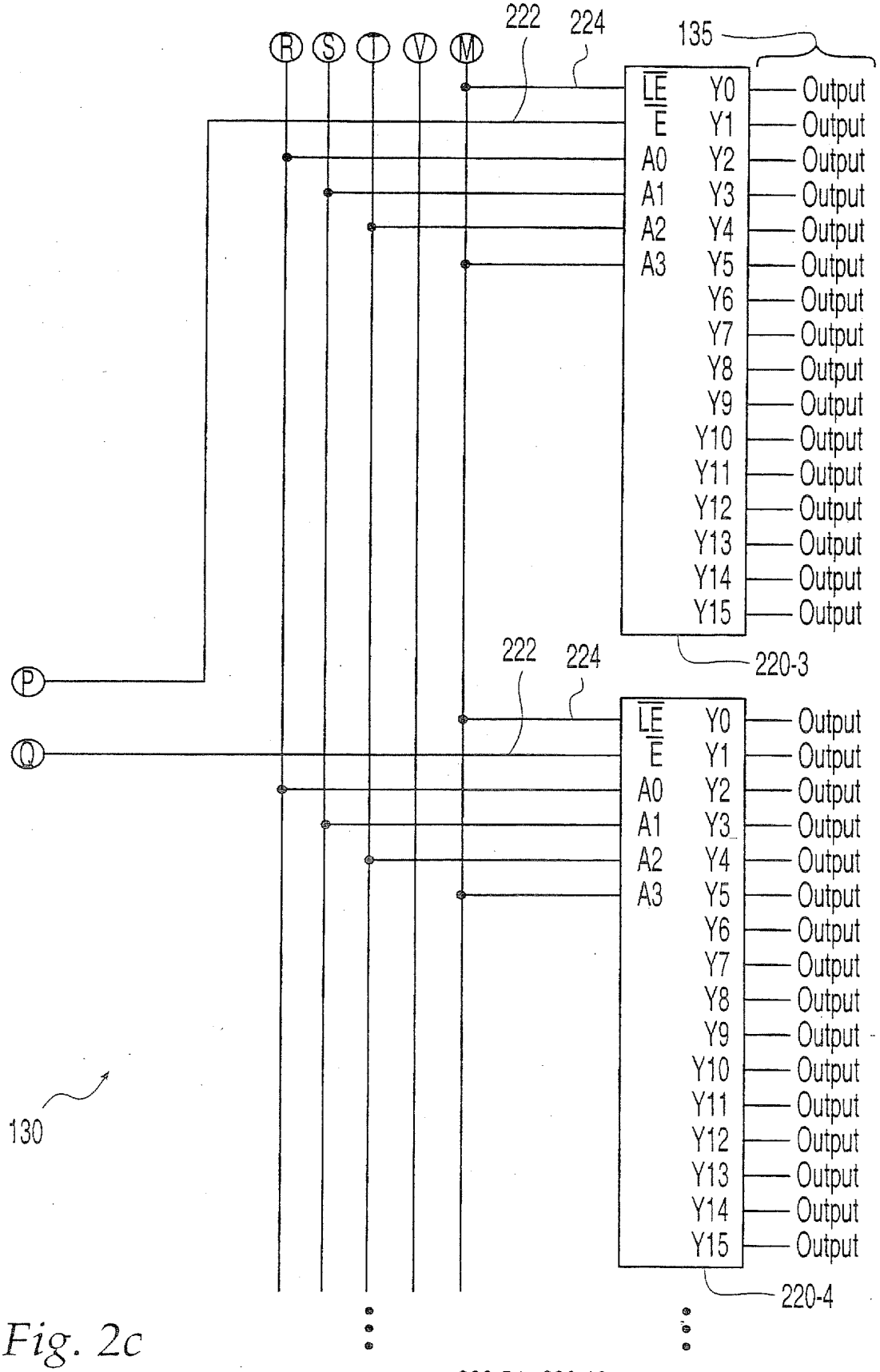


Fig. 2c

NSDOCID: <WO_____0163977A1_I_>

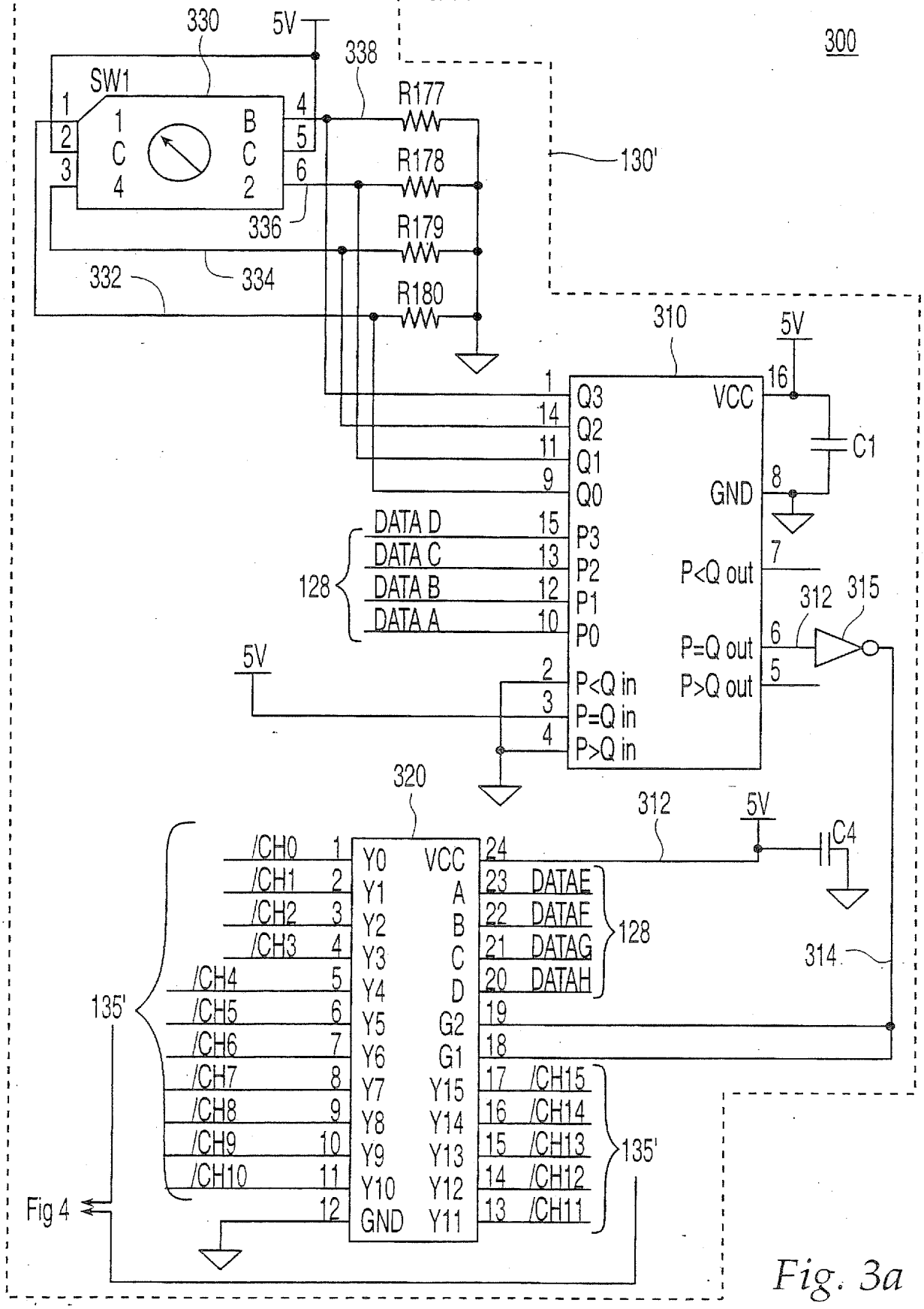


Fig. 3a

NSDOCID: <WO_____0163977A1_I_>

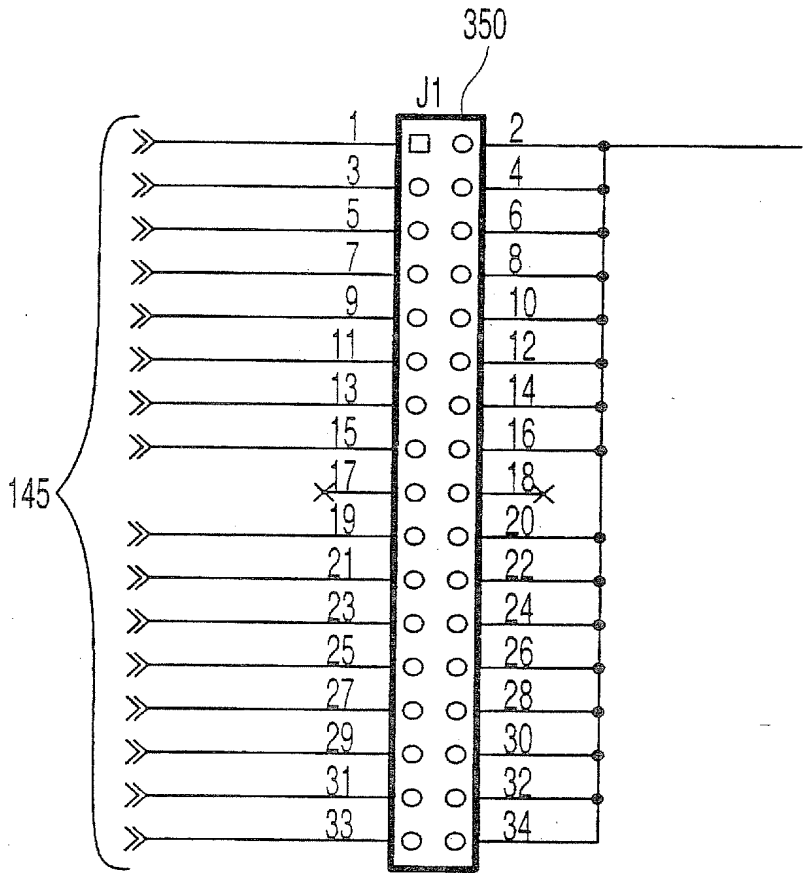


Fig. 3b

SDOCID: <WO_____0163977A1_|_>

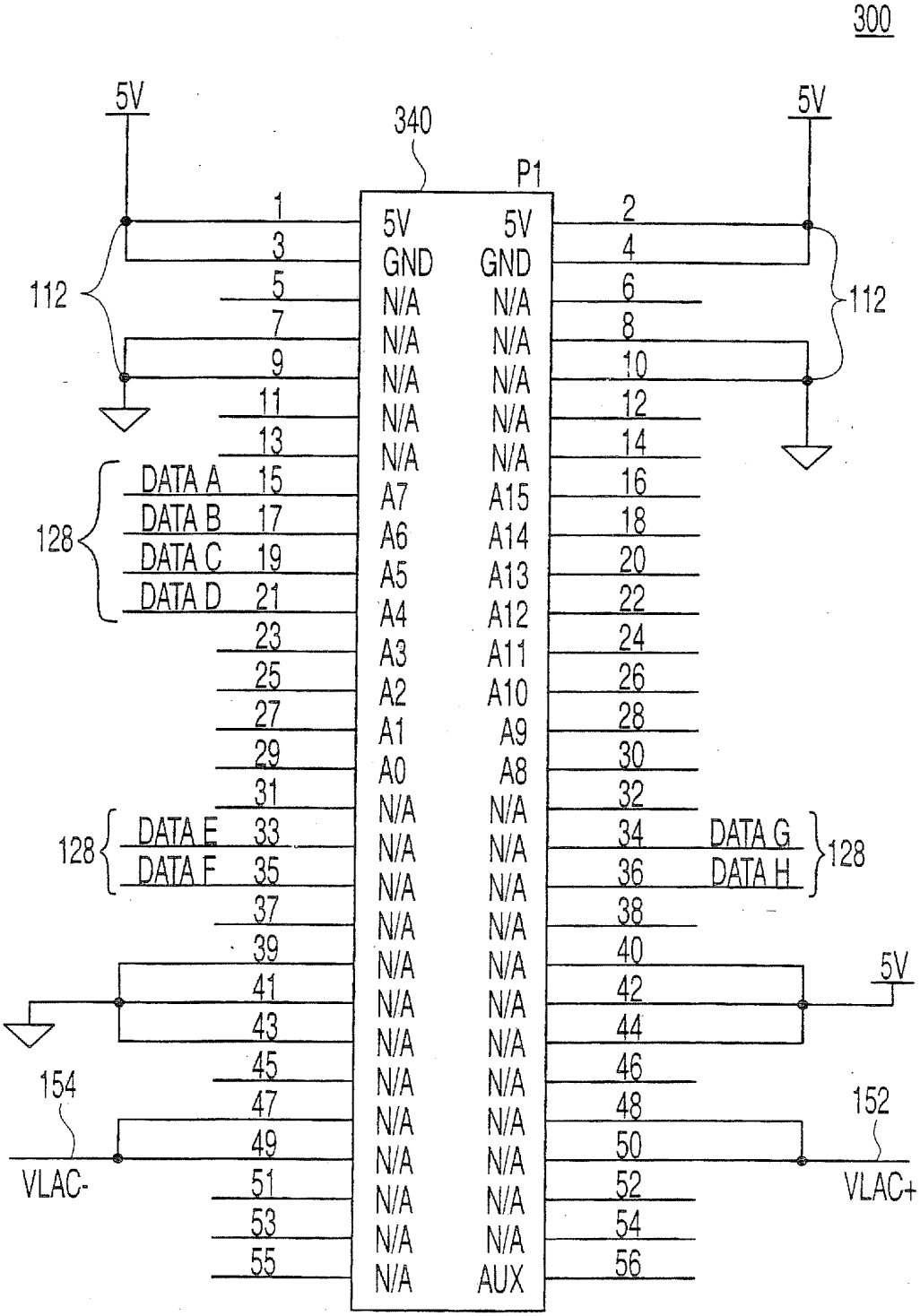


Fig. 3c

3NSDOCID: <WO_____0163977A1_I_>

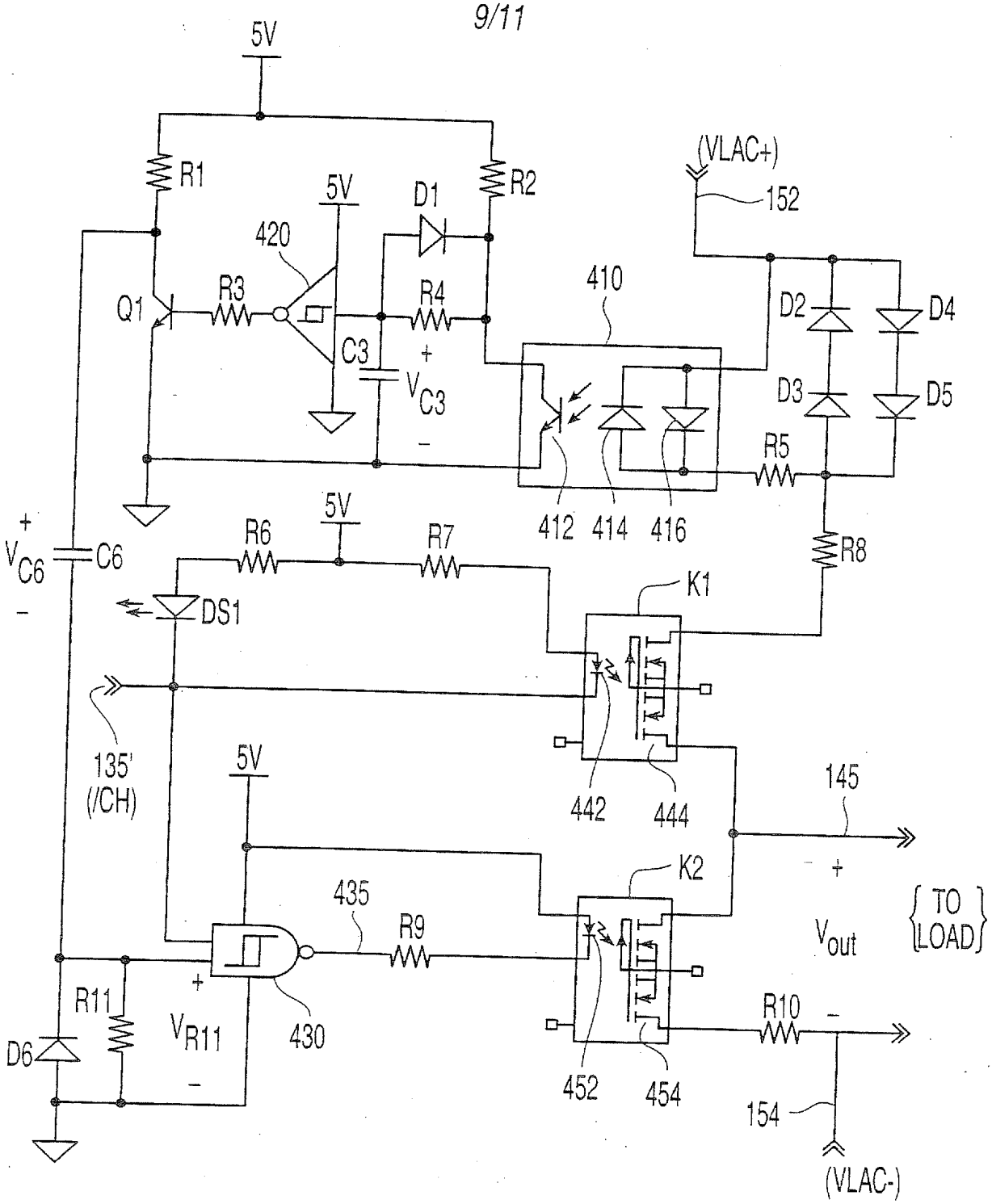


Fig. 4

SDOCID: <WO_____0163977A1_I_>

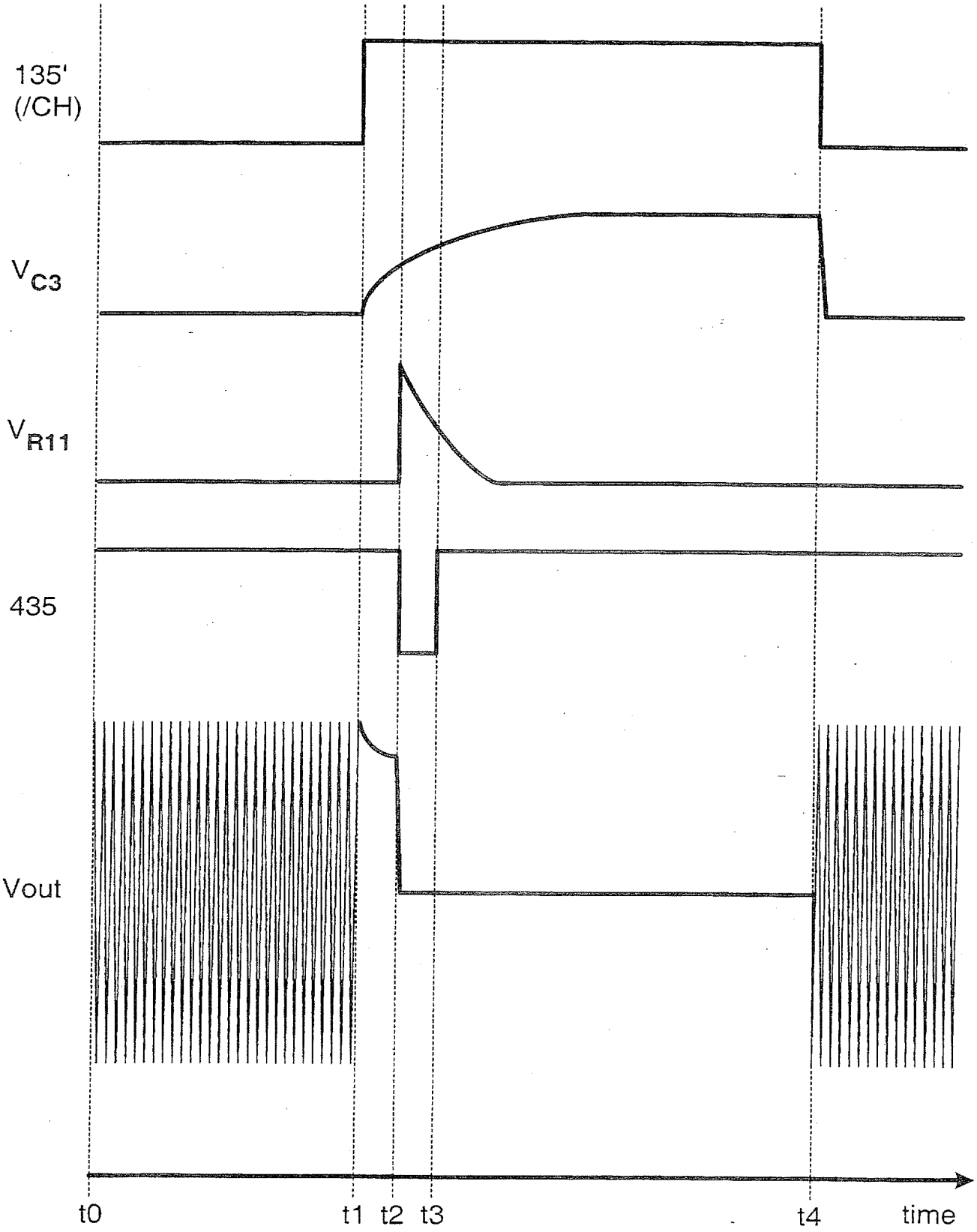


Fig. 5

BNSDOCID: <WO_____0163977A1_I_>

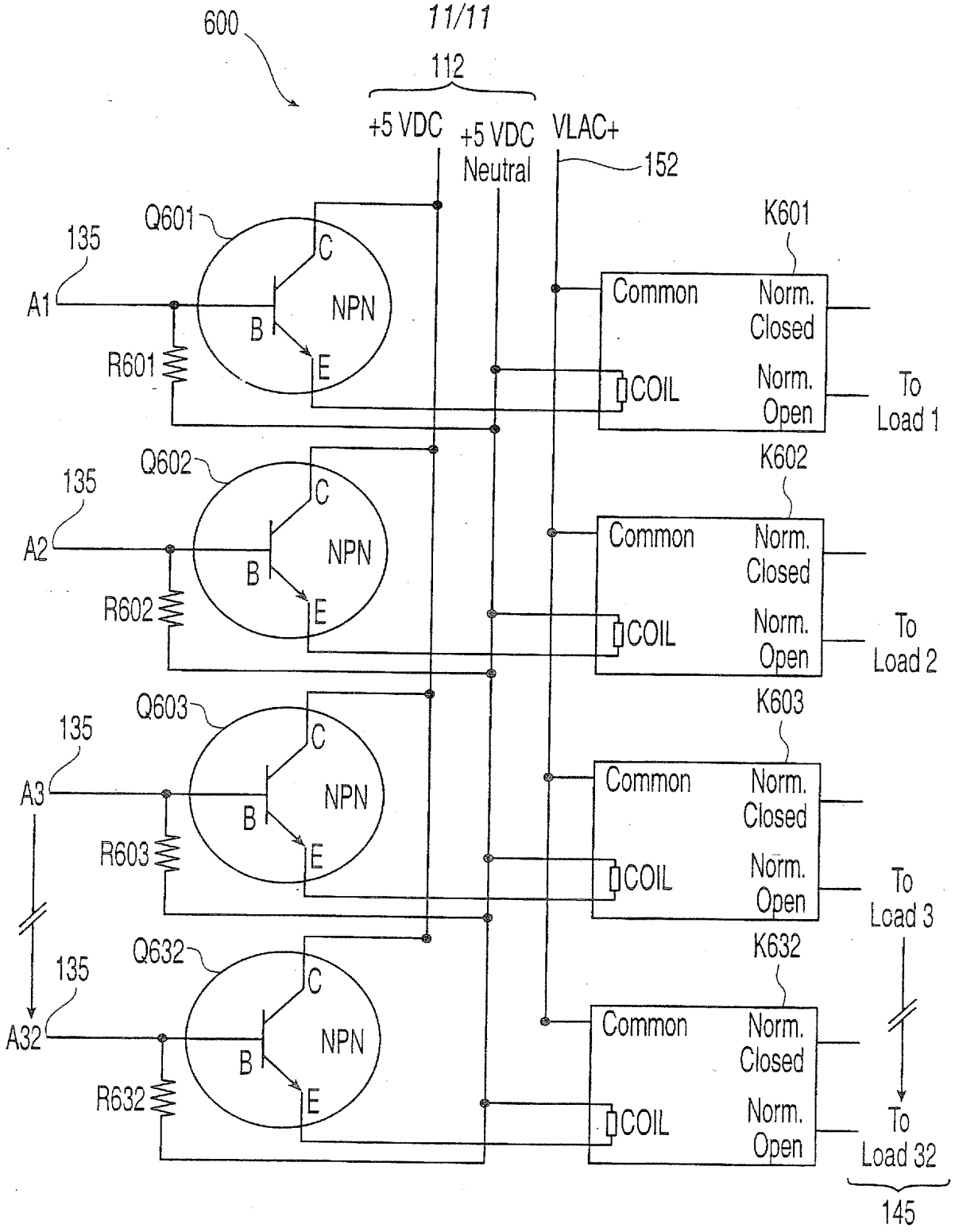


Fig. 6

NSDOCID: <WO_____0163977A1_I_>

INTERNATIONAL SEARCH REPORT

Interr ›nal Application No
PCT/US 01/05737

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H05B37/02

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H05B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No
X A	US 5 621 282 A (HASKELL WALTER) 15 April 1997 (1997-04-15) the whole document	1-16,22, 23,25 17-21, 24,26-28
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A	US 6 020 825 A (CHANSKY LEONARD M ET AL) 1 February 2000 (2000-02-01)	

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
29 May 2001	06/06/2001

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Maicas, J.

Form PCT/ISA/210 (second sheet) (July 1992)

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Exhibit 1004 - Page 119 of 373

3NSDOCID: <WO_____0163977A1_I_>

INTERNATIONAL SEARCH REPORT

Interr onal Application No
PCT/US 01/05737

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category ˇ	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	WO 99 17589 A (EBAC CORP ;EBATO HIROSHI (JP)) 8 April 1999 (1999-04-08)	

Form PCT/ISA/210 (continuation of second sheet) (July 1992)

Petitioner Hisense USA Corporation
Exhibit 1004 - Page 120 of 373

SDOCID: <WO_____0163977A1_I_>

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/US 01/05737

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INSDOCID: <WO_____0163977A1_I_>

Electronic Acknowledgement Receipt

EFS ID:	3939368
Application Number:	11745713
International Application Number:	
Confirmation Number:	1290
Title of Invention:	Systems and Methods for Controlling a Solid State Lighting Panel
First Named Inventor/Applicant Name:	John K. Roberts
Customer Number:	65106
Filer:	Timothy Jennings Wall/Paula Fisher
Filer Authorized By:	Timothy Jennings Wall
Attorney Docket Number:	5308-703
Receipt Date:	15-SEP-2008
Filing Date:	08-MAY-2007
Time Stamp:	09:44:53
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		5308-703_IDSand1449.pdf	325107 45bee26333c3e321ca673ea961758dc033bf1bf6	yes	3

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Information Disclosure Statement Letter	1	2
	Information Disclosure Statement (IDS) Filed (SB/08)	3	3

Warnings:					
Information:					
2	Foreign Reference	5308-703_Foreign_Ref_WO_0163977A1.pdf	3621868 92e491c1ef3a4384b6eda97e3629b38d51407334	no	46
Warnings:					
Information:					
3	NPL Documents	5308-703_NPL_ISRandWO_PCT_US2008_005145.pdf	1351539 20f2c53dc10556100357160e59969f2bdc7f2560	no	15
Warnings:					
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		Total Files Size (in bytes):	5298514		

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
11/745,713	05/08/2007	John K. Roberts	5308-703

CONFIRMATION NO. 1290

65106
MYERS BIGEL SIBLEY & SAJOVEC, P.A.
P.O. BOX 37428
RALEIGH, NC 27627

PUBLICATION NOTICE

OC00000033077327

Title: Systems and Methods for Controlling a Solid State Lighting Panel

Publication No.US-2008-0278097-A1
Publication Date:11/13/2008

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The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

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Office of Data Managment, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

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Exhibit 1004 - Page 125 of 373

INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Complete if Known	
				Application Number	11/745,713
				Filing Date	May 8, 2007
				First Named Inventor	John Roberts et al.
				Art Unit	2629
(use as many sheets as necessary)				Examiner Name	David Lee Lewis
Sheet	B1	of	B3	Attorney Docket Number	5308-703

U.S. PATENT DOCUMENTS						
Examiner Initials*	Cite No.	Document Number Number-Kind Code (if known)		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Complete if Known	
	Application Number	11/745,713
	Filing Date	May 8, 2007
	First Named Inventor	John Roberts et al.
	Art Unit	2629
(use as many sheets as necessary)	Examiner Name	David Lee Lewis
Sheet B2 of B3	Attorney Docket Number	5308-703

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Examiner Signature		Date Considered	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Complete if Known	
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Examiner Initials*	Cite No.	Foreign Patent Document Country Code, Number, Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T
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AB

PUBLICATION NUMBER : 10233669
PUBLICATION DATE : 02-09-98

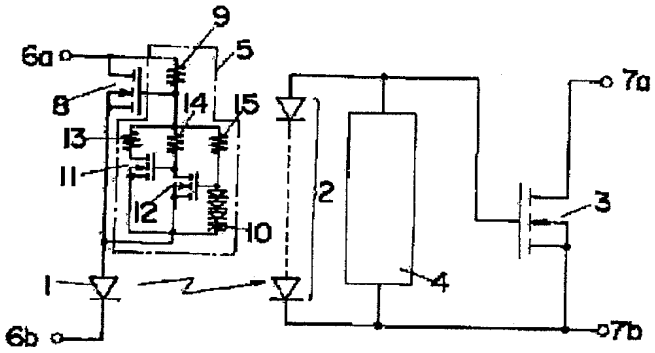
APPLICATION DATE : 21-02-97
APPLICATION NUMBER : 09037882

APPLICANT : MATSUSHITA ELECTRIC WORKS LTD;

INVENTOR : AKIYAMA SHIGEO;

INT.CL. : H03K 17/78 H03K 17/16

TITLE : SEMICONDUCTOR RELAY



ABSTRACT : PROBLEM TO BE SOLVED: To provide the semiconductor relay where thermal destruction is prevented when an overcurrent is supplied to a semiconductor switch element connected between relay output terminals.

SOLUTION: A light emitting element 1 and a photovoltaic element 2 are placed opposite to each other. A MOSFET 3 being a semiconductor switch element is conductive when a photoelectromotive force of the photovoltaic element 2 is applied between a gate and a source of the MOSFET 3. A MOSFET 8 is connected between relay input terminals 6a, 6b. A temperature sensing element 5 is connected to a gate of the MOSFET 8. The MOSFET 8 is closed when a control input is given between the relay input terminals 6a, 6b. When a voltage drop of a diode 10 is decreased by a generated heat by the MOSFET 3, a MOSFET 11 is conductive, a gate voltage of the MOSFET 8 is decreased less than the threshold voltage and the MOSFET 8 is nonconductive. A resistance of a resistor 9 is selected so that a current flowing to the light emitting element 1 via the resistor 9 is in the order of μA.

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(71)出願人　000005832
松下電工株式会社
大阪府門真市大字門真1048番地

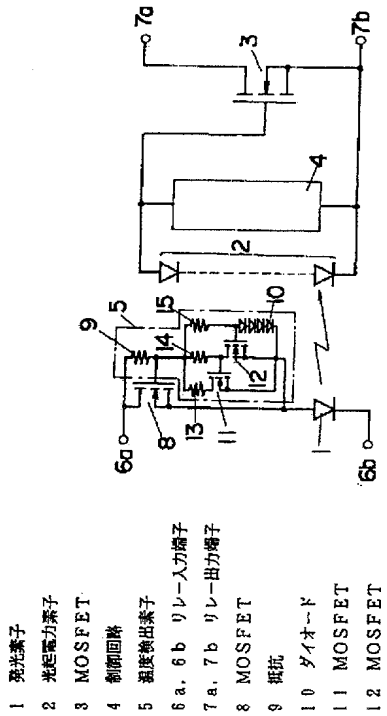
(72)発明者　野辺　武
大阪府門真市大字門真1048番地松下電工株式会社内

(72)発明者　秋山　茂夫
大阪府門真市大字門真1048番地松下電工株式会社内

(74)代理人　弁理士　西川　惠清　（外１名）

(54)【発明の名称】　半導体リレー

(57)【要約】
【課題】リレー出力端間に接続された半導体スイッチ素子に過電流が流れた時に熱破壊されるのを防ぐことができる半導体リレーを提供する。
【解決手段】発光素子１及び光起電力素子２は互いに対向する。半導体スイッチ素子たるＭＯＳＦＥＴ３は、光起電力素子２の光起電力がゲート・ソース間に印加されるとオン状態になる。リレー入力端子６ａ，６ｂ間にはＭＯＳＦＥＴ８が接続されている。ＭＯＳＦＥＴ８のゲートには温度検出素子５が接続されている。ＭＯＳＦＥＴ８は、リレー入力端子６ａ，６ｂ間に制御入力があると、オン状態になる。ＭＯＳＦＥＴ３の発熱によりダイオード１０の電圧降下が減少すると、ＭＯＳＦＥＴ１１がオン状態となり、ＭＯＳＦＥＴ８のゲート電圧が閾値よりも小さくなってＭＯＳＦＥＴ８がオフ状態となる。抵抗９の抵抗値は、抵抗９を介して発光素子１に流れる電流がμＡオーダになるように設定される。



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【特許請求の範囲】
【請求項１】　制御入力により点灯・消灯する発光素子と、前記発光素子に光結合した光起電力素子と、前記光起電力素子の光起電力が制御端に印加されることによって前記発光素子の点灯・消灯に応じてオン・オフされる半導体スイッチ素子と、周囲温度を検出し該周囲温度が所定温度以上になると前記発光素子を消灯させる温度検出素子とを備えて成ることを特徴とする半導体リレー。
【請求項２】　温度検出素子によって半導体素子がオフされた時に発光素子の消灯を維持させる自己保持回路を付加したことを特徴とする請求項１記載の半導体リレー。
【請求項３】　温度検出素子は、半導体スイッチ素子の近傍に配設されて成ることを特徴とする請求項１又は請求項２記載の半導体リレー。
【請求項４】　温度検出素子の一部がダイオード及び抵抗により構成され、前記ダイオード及び前記抵抗は、半導体スイッチ素子のゲート電極材料であるポリシリコンにより形成されて成ることを特徴とする請求項１乃至請求項３記載の半導体リレー。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明は、発光素子と光起電力素子とを光結合し、光起電力素子の出力によって半導体スイッチ素子をオン・オフさせる半導体リレーに関するものである。
【０００２】
【従来の技術】従来より、この種の半導体リレーとしては、図９に示すように、制御入力によって点灯・消灯する発光ダイオードよりなる発光素子１と、発光素子１に対置され発光素子１の光を受光して光起電力を発生するフォトダイオードや太陽電池を複数個直列に接続した光起電力ダイオードアレイよりなる光起電力素子２と、光起電力素子２の光起電力によってオン・オフする半導体スイッチ素子たるＭＯＳＦＥＴ３と、ＭＯＳＦＥＴ３のゲート・ソース間に接続された後述の制御回路４とを備えたものが提案されている。ここで、ＭＯＳＦＥＴ３はエンハンスメント型（ノーマリ・オフ型）であって、ゲート電圧が零の時はドレイン電流が流れずオフ状態である。
【０００３】以下、上記半導体リレーの動作について簡単に説明する。リレー入力端子６ａ，６ｂ間に制御入力が与えられていない時、つまり、発光素子１に電流が流れていない時は、光起電力素子２の光起電力がないので、ＭＯＳＦＥＴ３が高インピーダンス状態（オフ状態）にあり、リレー出力端子７ａ，７ｂ間はオフ状態である。
【０００４】これに対し、リレー入力端子６ａ，６ｂ間に制御入力が与えられ、発光素子１が発光すると、光起電力素子２は、発光素子１からの光を受光して電子－正孔対を発生し光起電力を出力する。すると、この光起電力がＭＯＳＦＥＴ３のゲート・ソース間に印加されるので、ＭＯＳＦＥＴ３が高インピーダンス状態（オフ状態）から低インピーダンス状態（オン状態）へ移行し、リレー出力端子７ａ，７ｂ間がオン状態となる。また、リレー入力端子６ａ，６ｂ間への制御入力が遮断されると、光起電力素子２の光起電力がなくなって、ＭＯＳＦＥＴ３のゲート静電容量に蓄積された電荷が制御回路４を介して放電され、リレー出力端子７ａ，７ｂ間がオン状態からオフ状態へ戻る。
【０００５】以上の動作により、リレー出力端子７ａ，７ｂ間に接続される負荷への電流を制御入力に応じてオン、オフすることができるのである。
【０００６】
【発明が解決しようとする課題】ところで、上記従来の半導体リレーにおいては、リレー出力端子７ａ，７ｂ間がオン状態の時に負荷の短絡などの故障が発生すると、ＭＯＳＦＥＴ３のドレイン・ソース間に過大な電流が流れ、ＭＯＳＦＥＴ３の発熱温度が高くなってＭＯＳＦＥＴ３が熱破壊してしまったり周辺部品が熱破壊されてしまい半導体リレー全体が破壊されてしまうことがあった。このため、ＭＯＳＦＥＴ３の発熱温度が所定温度以上になった場合に、ＭＯＳＦＥＴ３を強制的にオフさせることによって半導体リレーを破壊から保護することが考えられる。しかしながら、このような保護を行うためには、ＭＯＳＦＥＴ３の温度が所定温度以上になった時にＭＯＳＦＥＴ３を強制的にオフさせる保護回路を設ける必要があって、この保護回路を設けることによってＭＯＳＦＥＴ３のゲート消費電流が増大するとともにスイッチング速度が遅くなり、半導体リレーの出力特性が悪化してしまうという不具合があった。
【０００７】本発明は上記事由に鑑みて為されたものであり、その目的は、リレー出力端間に接続された半導体スイッチ素子に過電流が流れた時に熱破壊されるのを防止できる半導体リレーを提供することにある。
【０００８】
【課題を解決するための手段】請求項１の発明は、上記目的を達成するために、制御入力により点灯・消灯する発光素子と、前記発光素子に光結合した光起電力素子と、前記光起電力素子の光起電力が制御端に印加されることによって前記発光素子の点灯・消灯に応じてオン・オフされる半導体スイッチ素子と、周囲温度を検出し該周囲温度が所定温度以上になると前記発光素子を消灯させる温度検出素子とを備えて成ることを特徴とするものであり、発光素子が点灯している時に前記半導体スイッチ素子に過電流が流れて温度検出素子の周囲温度が所定温度以上になると前記発光素子が消灯されるので、従来のような保護回路を設けることなしに前記半導体スイッチ素子がオフして前記半導体スイッチ素子に過電流が流れ続けるのを防止でき、その結果、リレーの出力特性を

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維持しつつ半導体スイッチ素子が熱破壊されたり周辺部品が熱破壊されたりすることを防止することができる。

【０００９】請求項２の発明は、請求項１の発明において、温度検出素子によって半導体素子がオフされた時に発光素子の消灯を維持させる自己保持回路を付加したので、半導体スイッチ素子の温度が低くなっても発光素子の消灯が維持されるから、半導体スイッチ素子がオンすることもなく、安全性が向上する。請求項３の発明は、請求項１又は請求項２の発明において、温度検出素子が、半導体スイッチ素子の近傍に配設されているので、半導体スイッチ素子の温度上昇の検出を迅速且つ効率良く行うことが、迅速に半導体スイッチ素子をオフさせることが可能となる。

【００１０】請求項４の発明は、請求項１乃至請求項３の発明において、温度検出素子の一部がダイオード及び抵抗により構成され、前記ダイオード及び前記抵抗が、半導体スイッチ素子のゲート電極材料であるポリシリコンにより形成されているので、前記ダイオード及び前記抵抗を形成するのに別途製造装置を用意する必要もなく、簡単に形成することができる。しかも、半導体スイッチ素子と同一基板に集積化することが可能となり、部品点数を削減できるので、温度検出素子を設けたことによるリレー全体のサイズの大型化を防ぐことが可能になる。

【００１１】

【発明の実施の形態】以下、本発明の実施形態を図面に基づいて説明する。

（実施形態１）図１に本実施形態の回路図を示す。本実施形態の基本構成は図９に示した従来構成と略同じであって、制御入力によって点灯・消灯する発光ダイオードよりなる発光素子１と、発光素子１に対置され発光素子１の光を受光して光起電力を発生する光起電力ダイオードアレイよりなる光起電力素子２と、光起電力素子２の光起電力によってオン・オフする半導体スイッチ素子たるＭＯＳＦＥＴ３と、ＭＯＳＦＥＴ３のゲート・ソース間に接続された制御回路４とを備えている。ここで、ＭＯＳＦＥＴ３はエンハンスメント型であって、ゲート電圧が零の時はドレイン電流が流れずオフ状態である。また、制御回路４は、光起電力素子２に光起電力が発生した時には、ＭＯＳＦＥＴ３のゲート・ソース間電圧が速やかに上昇するように高インピーダンス状態になり、光起電力素子２の光起電力がなくなった時には、ＭＯＳＦＥＴ３のゲート・ソース間電圧が速やかに降下するように低インピーダンス状態になる。

【００１２】ところで、本実施形態では、一方の入力端子６ａにドレインが接続され発光素子１のアノードにソースが接続されるＭＯＳＦＥＴ（絶縁ゲート型半導体装置）８を備えている。また、ＭＯＳＦＥＴ８のゲートには温度検出素子５が接続されている。ここに、温度検出素子５は、ＭＯＳＦＥＴ８のゲート・ドレイン間に接続される抵抗９と、ＭＯＳＦＥＴ８のゲート・ソース間に接続される抵抗１５と複数のダイオード１０との直列回路と、一端がＭＯＳＦＥＴ８のゲートに接続される抵抗１４と、抵抗１４の他端と発光素子１のアノードとの間にドレイン・ソース間が接続されゲートが抵抗１５とダイオード１０との接続点に接続されるＭＯＳＦＥＴ１２と、一端がＭＯＳＦＥＴ８のゲートに接続される抵抗１３と、抵抗１３の他端と発光素子１のアノードとの間にドレイン・ソース間が接続されゲートが抵抗１４とＭＯＳＦＥＴ１２との接続点に接続されるＭＯＳＦＥＴ１１とで構成される。なお、ＭＯＳＦＥＴ８、１１、１２はエンハンスメント型である。また、ＭＯＳＦＥＴ８の替わりにＩＧＢＴ（絶縁ゲート型バイポーラトランジスタ）を使用してもよい。ダイオード１０の数は複数でなく、１つでもよい。

【００１３】以下、本実施形態の動作を説明する。リレー入力端子６ａ，６ｂ間に制御入力が与えられていない時は、発光素子１が消灯しており、光起電力素子２の光起電力がないので、半導体スイッチ素子たるＭＯＳＦＥＴ３がオフ状態であり、リレー出力端子７ａ，７ｂ間はオフ状態である。

【００１４】一方、リレー入力端子６ａ，６ｂ間に制御入力が与えられると、直列接続された複数のダイオード１０での電圧降下が生じることにより、ＭＯＳＦＥＴ１２がオン状態となる。なお、ＭＯＳＦＥＴ１１はオフ状態である。ここに、抵抗１４は抵抗１３に比べて十分大きな抵抗値のものを使用する。入力端子６ａ，６ｂ間に印加された電圧（制御入力）は、抵抗９と抵抗１４とにより分圧される。入力端子６ａ，６ｂ間の電圧が所定電圧以上であれば、ＭＯＳＦＥＴ８のゲート電圧が閾値より大きくなり、ＭＯＳＦＥＴ８がオン状態になる。ＭＯＳＦＥＴ８がオン状態になると、リレー入力端子６ａ、ＭＯＳＦＥＴ８、発光素子１、リレー入力端子６ｂの経路で電流が流れ発光素子１が発光する。発光素子１が発光すると、従来と同様に光起電力素子２に光起電力が発生しＭＯＳＦＥＴ３がオン状態となる。

【００１５】これに対し、リレー出力端子７ａ，７ｂ間に、つまりＭＯＳＦＥＴ３のドレイン・ソース間に、過大な電流が流れてＭＯＳＦＥＴ３の発熱温度が高くなると、各ダイオード１０での電圧降下が減少し、ＭＯＳＦＥＴ１２のゲート電圧が閾値電圧よりも小さくなってＭＯＳＦＥＴ１２がオフ状態になり、ＭＯＳＦＥＴ１１がオン状態になる。ＭＯＳＦＥＴ１１がオン状態になると、入力端子６ａ，６ｂ間に印加された電圧は、抵抗９と抵抗１３により分圧される。ここに、抵抗１３の抵抗値は、抵抗１４の抵抗値に比べて小さく設定してあり、ＭＯＳＦＥＴ８のゲート電圧が閾値よりも小さくなるよう設定されている。要するに、抵抗１４の抵抗値はＭＯＳＦＥＴ１２がオン状態になった時にＭＯＳＦＥＴ８のゲート電圧が閾値以上になるように設定され、抵抗１３

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の抵抗値はＭＯＳＦＥＴ１１がオン状態になった時にＭＯＳＦＥＴ８のゲート電圧が閾値よりも小さくなるように設定される。

【００１６】したがって、ＭＯＳＦＥＴ１１がオン状態になると、ＭＯＳＦＥＴ８がオフ状態となり、リレー入力端子６ａ、抵抗９、抵抗１３、ＭＯＳＦＥＴ１１、発光素子１、リレー入力端子６ｂの経路で電流が流れる。ここに、抵抗９の抵抗値はこの経路で流れる電流がマイクロアンペアオーダとなるように設定されており、発光素子１が発光できなくなって、その結果、光起電力素子２に光起電力が発生しなくなり、ＭＯＳＦＥＴ３がオフ状態になる。つまり、リレー出力端子７ａ，７ｂ間のＭＯＳＦＥＴ３がオン状態からオフ状態になり、ＭＯＳＦＥＴ３に過電流が流れ続けるのを防止でき、過電流によるＭＯＳＦＥＴ３の発熱によってＭＯＳＦＥＴ３自身や周辺部品が熱破壊されてしまい半導体リレーが破壊されるのを防止することができるのである。しかも、従来のような保護回路をＭＯＳＦＥＴ３に接続する必要がないので、ＭＯＳＦＥＴ３のゲート消費電流が増大したりＭＯＳＦＥＴ３のスイッチング速度が遅くなるという不具合をなくすことができる。要するに、本実施形態では、半導体リレーの出力特性の変更なしに、半導体スイッチ素子たるＭＯＳＦＥＴ３や周辺部品の破壊を防止することができるのである。

【００１７】ここに、リレー入力端子６ａ，６ｂ間に印加される電圧を入力電圧（制御入力）、リレー入力端子６ａ，６ｂ間に流れる電流を入力電流とすると、本実施形態の半導体リレーの入力特性は図２に示すようになっており、①が温度が低い時の入力特性を示し、②が温度が高い時の入力特性を示す。つまり、ＭＯＳＦＥＴ３に過電流が流れて発熱温度が高くなると、温度検出素子５が設けてあることによって②のように入力電流が小さくなり、発光素子１が発光しなくなるのである。

【００１８】ところで、本実施形態の半導体リレーのチップはトランスファーモールドにより作られたパッケージに納装されるが、例えば図３に示すように配設される。つまり、リレー入力端子６ａのリードフレーム上に、温度検出素子５が接続されたＭＯＳＦＥＴ８を配置する。また、リレー入力端子６ｂのリードフレーム上には、リードフレーム側がカソードとなるように発光素子１が配置される。発光素子１のアノードと温度検出素子５とはワイヤボンディングによって接続される。光起電力素子２及びＭＯＳＦＥＴ３はリレー入力端子７ａのリードフレーム上に配置され、光起電力素子２は発光素子１からの光を受光できかつ入出力間絶縁が得られるようになっている。また、ＭＯＳＦＥＴ３のソースはリレー入力端子７ｂにワイヤボンディングによって接続される。ここに、本実施形態では、温度検出素子５が、ＭＯＳＦＥＴ３の近傍に配設してあるので、過電流によるＭＯＳＦＥＴ３の発熱を素早く検知することができ、過電流によりＭＯＳＦＥＴ３が発熱した時に迅速に発光素子１を消灯させることができる。

【００１９】なお、抵抗９，１３，１４，１５及び各ダイオード１０をＭＯＳＦＥＴのゲート電極材料であるポリシリコンにより形成するようにすれば、ＭＯＳＦＥＴ８，１１，１２と、抵抗９，１３，１４，１５と、各ダイオード１０とを１つのシリコン基板に形成し１チップ化することができるので、部品を削減できるとともに半導体リレー全体のサイズを小型化することができる。つまり、ＭＯＳＦＥＴ８及び温度検出素子５を設けたことによって半導体リレー全体のサイズが大きくなるという不都合をなくすことができる。また、各抵抗９，１３，１４，１５及び各ダイオード１０をポリシリコン膜により形成するようにすれば、別途製造装置を用意する必要もなく、簡単に形成することができる。

【００２０】（実施形態２）図４に本実施形態の回路図を示す。本実施形態の基本構成及び基本動作は実施形態１と略同じであり、実施形態１の半導体リレーに、ＭＯＳＦＥＴ１６，１７，１８及び抵抗１９，２０からなる自己保持回路２１を付加した点で実施形態１と相違する。ここに、自己保持回路２１は、ＭＯＳＦＥＴ３の発熱を温度検出素子５が検出してＭＯＳＦＥＴ８がオフされることにより発光素子１が消灯された時に、ＭＯＳＦＥＴ３のオフ状態を保持させて発光素子１の消灯状態を保持させる回路である。以下、実施形態１と相違する点についてのみ説明する。なお、各ＭＯＳＦＥＴ３，８，１１，１２，１６，１７，１８はエンハンスメント型である。

【００２１】本実施形態では、ＭＯＳＦＥＴ３のドレイン・ソース間に過大な電流が流れてＭＯＳＦＥＴ３の発熱温度が高くなって、ＭＯＳＦＥＴ１１がオン状態になった後は、ＭＯＳＦＥＴ３の発熱温度が下がっても自己保持回路２１があることによってＭＯＳＦＥＴ１１のオン状態が保持される。つまり、発光素子１が消灯されてＭＯＳＦＥＴ３の発熱温度が下がっても、リレー入力端子６ａ，６ｂ間の制御入力をリセットしないかぎり、制御入力があっても発光素子１が発光しないようになっている。したがって、負荷が短絡してＭＯＳＦＥＴ３に過電流が流れたような場合に、負荷が短絡したまま再びＭＯＳＦＥＴ３がオン状態になることを防ぐことができるので、安全性が向上する。

【００２２】なお、本実施形態においても、実施形態１と同様に、抵抗９，１３，１４，１５，１９，２０と、各ダイオード１０とをポリシリコン膜により形成することで、ＭＯＳＦＥＴ８，１１，１２，１６，１７，１８と、抵抗９，１３，１４，１５，１９，２０と、各ダイオード１０とを１チップに形成してあり、実施形態１と同様の効果が得られる。

【００２３】（実施形態３）図５に本実施形態の回路図を示す。本実施形態の基本構成は実施形態１と略同じで

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あり、ＭＯＳＦＥＴ８がディプレション型である点、温度検出素子５がＭＯＳＦＥＴ８のソースと発光素子１のアノードとの間に接続される点、ＭＯＳＦＥＴ８のゲートが発光素子１のアノードに直接接続される点などが実施形態１と相違する。なお、実施形態１と同様の構成要素には同一の符号を付してある。以下、動作について説明する。

【００２４】リレー入力端子６ａ，６ｂ間に制御入力が与えられていない時は、発光素子１が消灯しており、光起電力素子２の光起電力がないので、半導体スイッチ素子たるＭＯＳＦＥＴ３がオフ状態であり、リレー出力端子７ａ，７ｂ間はオフ状態である。一方、リレー入力端子６ａ，６ｂ間に制御入力が与えられると、直列接続された複数のダイオード１０での電圧降下が生じることにより、ＭＯＳＦＥＴ１２がオン状態となる。なお、ＭＯＳＦＥＴ１１はオフ状態である。したがって、制御入力が与えられると、リレー入力端子６ａ、ＭＯＳＦＥＴ８、抵抗１４、ＭＯＳＦＥＴ１２、発光素子１、リレー入力端子６ｂの経路で電流が流れ、発光素子１が発光する。発光素子１が発光すると、従来と同様に光起電力素子２に光起電力が発生しＭＯＳＦＥＴ３がオン状態となる。ここに、抵抗１４は抵抗１３に比べて十分大きな抵抗値のものを使用する。

【００２５】これに対し、リレー出力端子７ａ，７ｂ間に、つまりＭＯＳＦＥＴ３のドレイン・ソース間に、過大な電流が流れてＭＯＳＦＥＴ３の発熱温度が高くなると、各ダイオード１０での電圧降下が減少し、ＭＯＳＦＥＴ１２のゲート電圧が閾値電圧よりも小さくなってＭＯＳＦＥＴ１２がオフ状態になり、ＭＯＳＦＥＴ１１がオン状態なる。ＭＯＳＦＥＴ１１がオン状態になると、リレー入力端子６ａ、ＭＯＳＦＥＴ８、抵抗１３、ＭＯＳＦＥＴ１１、発光素子１、リレー入力端子６ｂの経路で電流が流れる。ここに、抵抗１３の抵抗値は、抵抗１４に比べて大きな抵抗値で且つこの経路で流れる電流がマイクロアンペアオーダとなるように設定されている。したがって、ＭＯＳＦＥＴ１１がオン状態になると、発光素子１が発光できなくなって、その結果、光起電力素子２に光起電力が発生しなくなり、ＭＯＳＦＥＴ３がオフ状態になる。つまり、リレー出力端子７ａ，７ｂ間がオン状態からオフ状態になり、半導体スイッチ素子たるＭＯＳＦＥＴ３に過電流が流れ続けるのを防止でき、過電流による発熱によってＭＯＳＦＥＴ３や周辺部品が破壊されてしまうのを防止することができるのである。しかも、従来のような保護回路をＭＯＳＦＥＴ３に接続する必要がないので、ＭＯＳＦＥＴ３のゲート消費電流が増大したりＭＯＳＦＥＴ３のスイッチング速度が遅くなるという不具合をなくすことができる。要するに、本実施形態も、実施形態１と同様に、半導体リレーの出力特性の変更なしに、半導体スイッチ素子たるＭＯＳＦＥＴ３や周辺部品の破壊を防止することができるのである。

【００２６】ここに、リレー入力端子６ａ，６ｂ間に印加される電圧を入力電圧、リレー入力端子６ａ，６ｂ間に流れる電流を入力電流とすると、本実施形態の半導体リレーの入力特性は図６に示すようになっており、①が温度が低い時の入力特性を示し、②が温度が高い時の入力特性を示す。つまり、ＭＯＳＦＥＴ３に過電流が流れて発熱温度が高くなると、温度検出素子５を設けてあることによって入力電流が小さくなり、発光素子１が発光しなくなるのである。

【００２７】ところで、本実施形態の半導体リレーのチップは、実施形態１と同様に、例えば図７に示すように配設される。つまり、リレー入力端子６ａのリードフレーム上に、温度検出素子５が接続されたＭＯＳＦＥＴ８を配置する。また、入力端子６ｂのリードフレーム上には、リードフレーム側がカソードとなるように発光素子１が配置される。発光素子１のアノードと温度検出素子５とはワイヤボンディングによって接続される。光起電力素子２及びＭＯＳＦＥＴ３はリレー入力端子７ａのリードフレーム上に配置され、光起電力素子２は発光素子１からの光を受光できかつ入出力間絶縁が得られるようになっている。また、ＭＯＳＦＥＴ３のソースはリレー入力端子７ｂにワイヤボンディングによって接続される。ここに、本実施形態では、温度検出素子５が、ＭＯＳＦＥＴ３の近傍に配設してあるので、過電流によるＭＯＳＦＥＴ３の発熱を素早く検知することができ、過電流によりＭＯＳＦＥＴ３が発熱した時に迅速に発光素子１を消灯させることができる。

【００２８】なお、抵抗１３，１４，１５及び各ダイオード１０をＭＯＳＦＥＴのゲート電極材料であるポリシリコンにより形成するようにすれば、ＭＯＳＦＥＴ８，１１，１２と、抵抗１３，１４，１５と、各ダイオード１０とを１つのシリコン基板に形成し１チップ化することができるので、部品を削減できるとともに半導体リレー全体のサイズを小型化することができる。つまり、ＭＯＳＦＥＴ８及び温度検出素子５を設けたことによって半導体リレー全体のサイズが大きくなるという不都合をなくすことができる。また、抵抗１３，１４，１５及びダイオード１０をポリシリコン膜により形成するようにすれば、別途製造装置を用意する必要もなく、簡単に形成することができる。

【００２９】（実施形態４）図８に本実施形態の回路図を示す。本実施形態の基本構成及び基本動作は実施形態３と略同じであり、実施形態３の半導体リレーに、ＭＯＳＦＥＴ１６，１７，１８及び抵抗１９，２０からなる自己保持回路２１を付加した点で実施形態３と相違する。ここに、自己保持回路２１は、ＭＯＳＦＥＴ３の発熱を温度検出素子５が検出してＭＯＳＦＥＴ１１がオン状態になった時にＭＯＳＦＥＴ１１のオン状態を保持させることにより発光素子１の消灯を維持させる回路である。以下、実施形態３と相違する点についてのみ説明す

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る。なお、ＭＯＳＦＥＴ３，１１，１２，１６，１７，１８はエンハンスメント型であり、ＭＯＳＦＥＴ８のみディプレッション型である。

【００３０】本実施形態では、ＭＯＳＦＥＴ３のドレイン・ソース間に過大な電流が流れてＭＯＳＦＥＴ３の発熱温度が高くなって、ＭＯＳＦＥＴ１１がオン状態になった後は、ＭＯＳＦＥＴ３の発熱温度が下がっても自己保持回路２１があることによってＭＯＳＦＥＴ１１のオン状態が保持される。つまり、発光素子１が消灯されることによりＭＯＳＦＥＴ３の発熱温度が下がっても、リレー入力端子６ａ，６ｂ間の制御入力をリセットしないかぎり、制御入力があっても発光素子１が発光しないようになっている。したがって、負荷が短絡してＭＯＳＦＥＴ３に過電流が流れたような場合に、負荷が短絡したまま再びＭＯＳＦＥＴ３がオン状態になることを防ぐことができるので、安全性が向上する。

【００３１】なお、本実施形態においても、実施形態３と同様に、抵抗１３，１４，１５，１９，２０と、各ダイオード１０とをポリシリコン膜により形成することで、各ＭＯＳＦＥＴ８，１１，１２，１６，１７，１８と、各抵抗１３，１４，１５，１９，２０と、各ダイオード１０とを１チップに形成してあり、実施形態３と同様の効果が得られる。

【００３２】

【発明の効果】請求項１の発明は、制御入力により点灯・消灯する発光素子と、前記発光素子に光結合した光起電力素子と、前記光起電力素子の光起電力が制御端に印加されることによって前記発光素子の点灯・消灯に応じてオン・オフされる半導体スイッチ素子と、周囲温度を検出し該周囲温度が所定温度以上になると前記発光素子を消灯させる温度検出素子とを備えているので、発光素子が点灯している時に前記半導体スイッチ素子に過電流が流れて温度検出素子の周囲温度が所定温度以上になると前記発光素子が消灯されるから、従来のような保護回路を設けることなしに前記半導体スイッチ素子がオフして前記半導体スイッチ素子に過電流が流れ続けるのを防止でき、その結果、リレーの出力特性を維持しつつ半導体スイッチ素子が熱破壊されたり周辺部品が熱破壊されたりすることを防止することができるという効果がある。

【００３３】請求項２の発明は、請求項１の発明において、温度検出素子によって半導体素子がオフされた時に発光素子の消灯を維持させる自己保持回路を付加したので、半導体スイッチ素子の温度が低くなっても発光素子の消灯が維持されるから、半導体スイッチ素子がオンすることもなく、安全性が向上するという効果がある。請求項３の発明は、請求項１又は請求項２の発明において、温度検出素子が、半導体スイッチ素子の近傍に配設されているので、半導体スイッチ素子の温度上昇の検出を迅速且つ効率良く行うことが、迅速に半導体スイッチ素子をオフさせることが可能となるという効果がある。

【００３４】請求項４の発明は、請求項１乃至請求項３の発明において、温度検出素子の一部がダイオード及び抵抗により構成され、前記ダイオード及び前記抵抗が、半導体スイッチ素子のゲート電極材料であるポリシリコンにより形成されているので、前記ダイオード及び前記抵抗を形成するのに別途製造装置を用意する必要もなく、簡単に形成することができる。しかも、半導体スイッチ素子と同一基板に集積化することが可能となり、部品点数を削減できるので、温度検出素子を設けたことによるリレー全体のサイズの大型化を防ぐことが可能になるという効果がある。

【図面の簡単な説明】

【図１】実施形態１を示す回路図である。

【図２】同上の動作説明図である。

【図３】同上のチップ配置図である。

【図４】実施形態２を示す回路図である。

【図５】実施形態３を示す回路図である。

【図６】同上の動作説明図である。

【図７】同上のチップ配置図である。

【図８】実施形態４を示す回路図である。

【図９】従来例を示す回路図である。

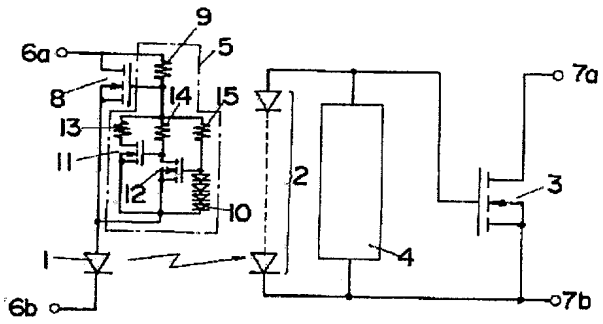
【符号の説明】

１　発光素子
２　光起電力素子
３　ＭＯＳＦＥＴ
４　制御回路
５　温度検出素子
６ａ，６ｂ　リレー入力端子
７ａ，７ｂ　リレー出力端子
８　ＭＯＳＦＥＴ
９　抵抗
１０　ダイオード
１１　ＭＯＳＦＥＴ
１２　ＭＯＳＦＥＴ

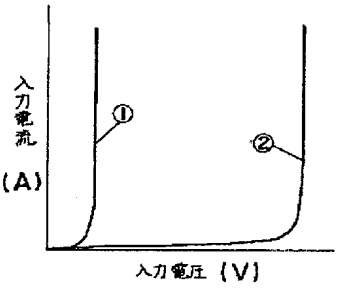
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【図１】

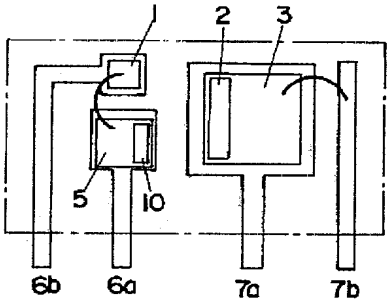
１　発光素子
２　光起電力素子
３　MOSFET
４　制御回路
５　温度検出素子
６ａ，６ｂ　リレー入力端子
７ａ，７ｂ　リレー出力端子
８　MOSFET
９　抵抗
１０　ダイオード
１１　MOSFET
１２　MOSFET



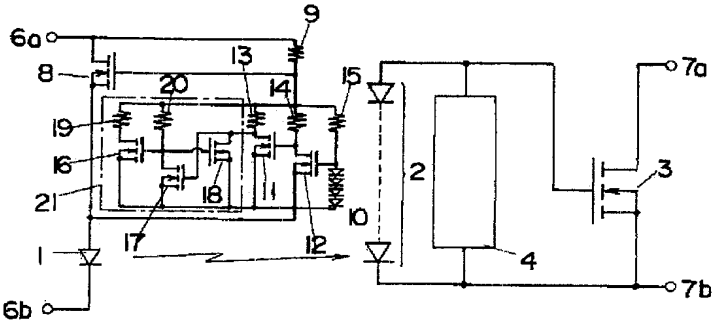
【図２】



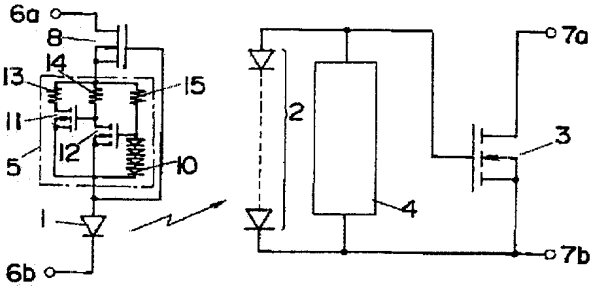
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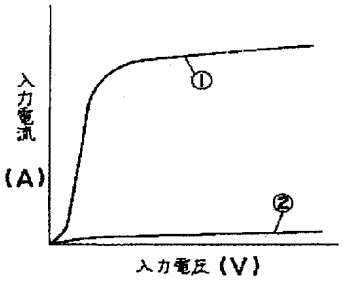
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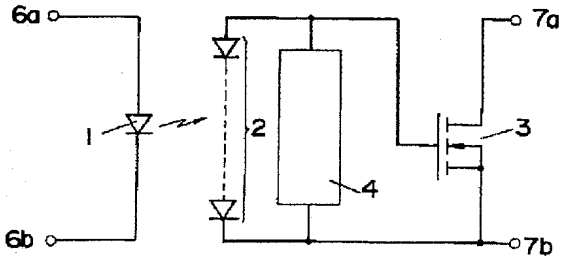
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【図６】

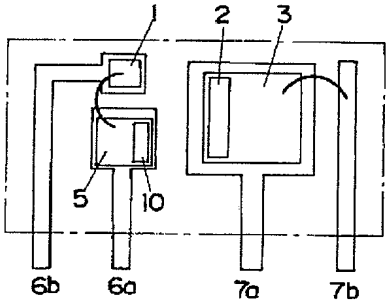


【図９】

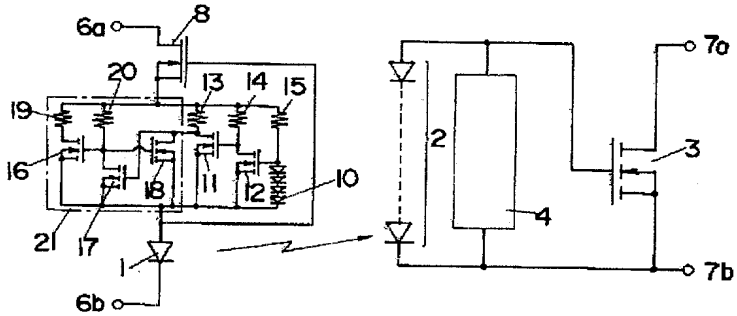


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【図７】


1
2
3
5
10
6b
6a
7a
7b

【図８】


6a
8
20
13
14
15
19
16
18
11
12
10
21
17
1
6b
2
4
3
7a
7b

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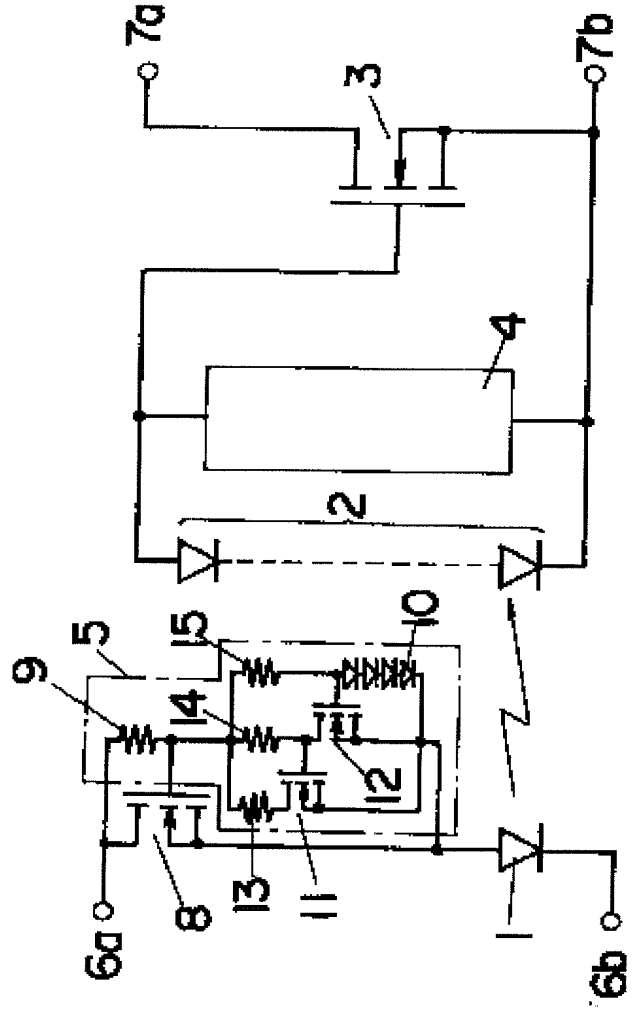
CLAIMS

[Claim(s)]
[Claim 1]A semiconductor relay comprising:
A light emitting device turned on and switched off by a control input.
A photovoltaic cell which carried out optical coupling to said light emitting device.
A semiconductor switching device turned on and off according to lighting and putting out lights of said light emitting device by impressing photoelectromotive force of said photovoltaic cell to a control end.
A temperature detector which makes said light emitting device switch off when ambient air temperature is detected and this ambient air temperature becomes more than prescribed temperature.

[Claim 2]The semiconductor relay according to claim 1 adding a holding circuit which maintains putting out lights of a light emitting device when a semiconductor device is turned off by temperature detector.
[Claim 3]The semiconductor relay according to claim 1 or 2, wherein a temperature detector is allocated near the semiconductor switching device and changes.
[Claim 4]The semiconductor relay according to claim 1 to 3 a part of temperature detector's being constituted by a diode and resistance, forming said diode and said resistance with polysilicon which is a gate electrode material of a semiconductor switching device, and changing.

[Translation done.]

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1 発光素子
2 光起電力素子
3 MOSFET
4 制御回路
5 温度検出素子
6a，6b リレー入力端子
7a，7b リレー出力端子
8 MOSFET
9 抵抗
10 ダイオード
11 MOSFET
12 MOSFET

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention]This invention carries out optical coupling of a light emitting device and the photovoltaic cell, and relates to the semiconductor relay which makes a semiconductor switching device turn on and off with the output of a photovoltaic cell.
[0002]
[Description of the Prior Art]The light emitting device 1 which consists of a light emitting diode turned on and switched off by a control input as this kind of a semiconductor relay conventionally as shown in drawing 9, The photovoltaic cell 2 which consists of a photoelectromotive-force diode array which connected to series two or more photo-diodes which are counterposed by the light emitting device 1, receive the light of the light emitting device 1, and generate photoelectromotive force, and solar cells, The thing provided with the below-mentioned control circuit 4 connected between the gate sauce of the semiconductor switching device slack MOSFET3 and MOSFET3 turned on and off according to the photoelectromotive force of the photovoltaic cell 2 is proposed. Here, MOSFET3 is an enhancement type (no Mali-off type), and when gate voltage is zero, drain current does not flow but it is an OFF state.
[0003]Hereafter, operation of the above-mentioned semiconductor relay is explained briefly. Since there is no photoelectromotive force of the photovoltaic cell 2 when the control input is not given between the relay input terminals 6a and 6b (i.e., when current is not flowing into the light emitting device 1), MOSFET3 is in a high impedance state (OFF state), and it is an OFF state between the relay output terminal 7a and 7b.
[0004]On the other hand, if a control input is given between the relay input terminals 6a and 6b and the light emitting device 1 emits light, the photovoltaic cell 2 will receive the light from the light emitting device 1, will generate an electronic-electron hole pair, and will output photoelectromotive force. Then, since this photoelectromotive force is impressed between the gate sauce of MOSFET3, MOSFET3 will shift to a low impedance condition (ON state) from a high impedance state (OFF state), and between the relay output terminal 7a and 7b will be in an ON state. If the control input of a between [the relay input terminals 6a and 6b] is intercepted, the photoelectromotive force of the photovoltaic cell 2 will be lost, the electric charge accumulated in the gate electric capacity of MOSFET3 will be discharged via the control circuit 4, and between the relay output terminal 7a and 7b will return from an ON state to an OFF state.
[0005]By the above operation, it can respond to a control input, and the current to the load connected

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between the relay output terminal 7a and 7b can be one [current] and turned off.

[0006]

[Problem(s) to be Solved by the Invention]By the way, in the above-mentioned conventional semiconductor relay, If failure of the short circuit of load, etc. occurs when between the relay output terminal 7a and 7b is an ON state, Excessive current flowed between the drain sauce of MOSFET3, MOSFET3 might carry out the thermal runaway and the whole semiconductor relay might be destroyed [the exothermic temperature of MOSFET3 might become high, the thermal runaway of the periphery article may be carried out, and]. For this reason, when the exothermic temperature of MOSFET3 becomes more than prescribed temperature, it is possible by making MOSFET3 turn off compulsorily to protect a semiconductor relay from destruction. However, in order to perform such protection. It is necessary to provide the protection circuit which makes MOSFET3 turn off compulsorily when the temperature of MOSFET3 becomes more than prescribed temperature. While the gate consumed electric current of MOSFET3 increased by providing this protection circuit, switching speed became slow, and there was fault that the output characteristics of a semiconductor relay will get worse.

[0007]In view of the above-mentioned reason, it succeeds in this invention, and the purpose is to provide the semiconductor relay which can prevent that a thermal runaway is carried out, when an over-current flows into the semiconductor switching device connected between relay output ends.

[0008]

[Means for Solving the Problem]A light emitting device which turns on and switches off an invention of claim 1 by a control input to achieve the above objects, A photovoltaic cell which carried out optical coupling to said light emitting device, and a semiconductor switching device turned on and off according to lighting and putting out lights of said light emitting device by impressing photoelectromotive force of said photovoltaic cell to a control end, It is what is provided with a temperature detector which makes said light emitting device switch off when ambient air temperature is detected and this ambient air temperature becomes more than prescribed temperature, and is characterized by things, Since said light emitting device will be switched off if an over-current flows into said semiconductor switching device and ambient air temperature of a temperature detector becomes more than prescribed temperature when a light emitting device is on, An over-current can be prevented from said semiconductor switching device turning off and continuing flowing into said semiconductor switching device, without providing a protection circuit like before, As a result, it can prevent that the thermal runaway of the semiconductor switching device is carried out, or the thermal runaway of the periphery article is carried out, maintaining the output characteristics of a relay.

[0009]Since an invention of claim 2 added a holding circuit which maintains putting out lights of a light emitting device in an invention of claim 1 when a semiconductor device was turned off by temperature detector, Safety improves without one [a semiconductor switching device] since putting out lights of a light emitting device is maintained even if temperature of a semiconductor switching device becomes low. In an invention of claim 1 or claim 2, since a temperature detector is allocated near the semiconductor switching device, it becomes possible for detecting a rise in heat of a semiconductor switching device promptly and efficiently to make a semiconductor switching device turn off promptly of an invention of claim 3.

[0010]As for an invention of claim 4, a part of temperature detector is constituted by a diode and resistance in an invention of claim 1 thru/or claim 3, Since said diode and said resistance are formed with polysilicon

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which is a gate electrode material of a semiconductor switching device, it is not necessary to prepare a manufacturing installation for forming said diode and said resistance separately, and can form easily. And since it becomes possible to be integrated to the same substrate as a semiconductor switching device and part mark can be reduced, it becomes possible to prevent enlargement of size of the whole relay by having provided a temperature detector.

[0011]

[Embodiment of the Invention]Hereafter, the embodiment of this invention is described based on a drawing. (Embodiment 1) The circuit diagram of this embodiment is shown in drawing 1. the former which showed drawing 9 the basic constitution of this embodiment -- composition -- abbreviated -- with the light emitting device 1 which consists of a light emitting diode which it is the same, and is turned on and switched off by a control input. The photovoltaic cell 2 which consists of a photoelectromotive-force diode array which is counterposed by the light emitting device 1, receives the light of the light emitting device 1, and generates photoelectromotive force, It has the control circuit 4 connected between the gate sauce of the semiconductor switching device slack MOSFET3 and MOSFET3 turned on and off according to the photoelectromotive force of the photovoltaic cell 2. Here, MOSFET3 is an enhancement type, and when gate voltage is zero, drain current does not flow but it is an OFF state. When photoelectromotive force occurs in the photovoltaic cell 2, the control circuit 4, When it is in a high impedance state so that the voltage between gate sauce of MOSFET3 may rise promptly, and the photoelectromotive force of the photovoltaic cell 2 is lost, it will be in a low impedance condition so that the voltage between gate sauce of MOSFET3 may descend promptly.

[0012]By the way, in this embodiment, it has MOSFET(insulated gate type semiconductor device) 8 by which a drain is connected to one input terminal 6a, and sauce is connected to the anode of the light emitting device 1. The temperature detector 5 is connected to the gate of MOSFET8. The resistance 9 to which the temperature detector 5 is connected between the gate drains of MOSFET8 here, The series circuit of the resistance 15 connected between the gate sauce of MOSFET8, and two or more diodes 10, MOSFET12 to which between drain sauce is connected between the resistance 14 for which one end is connected to the gate of MOSFET8, and the other end of the resistance 14 and the anode of the light emitting device 1, and a gate is connected at the node of the resistance 15 and the diode 10, Between drain sauce is connected between the resistance 13 for which one end is connected to the gate of MOSFET8, and the other end of the resistance 13 and the anode of the light emitting device 1, and a gate comprises MOSFET11 connected at the node of the resistance 14 and MOSFET12. MOSFETs 8, 11, and 12 are enhancement types. IGBT (insulated gate type bipolar transistor) may be used instead of MOSFET8. The number of the diodes 10 may not be plurality, but one may be sufficient as it.

[0013]Hereafter, operation of this embodiment is explained. Since the light emitting device 1 has gone out and there is no photoelectromotive force of the photovoltaic cell 2 when the control input is not given between the relay input terminals 6a and 6b, semiconductor switching device slack MOSFET3 is an OFF state, and it is an OFF state between the relay output terminal 7a and 7b.

[0014]On the other hand, if a control input is given between the relay input terminals 6a and 6b, when the voltage drop in two or more diodes 10 by which the series connection was carried out arises, MOSFET12 will be in an ON state. MOSFET11 is an OFF state. The resistance 14 uses the thing of sufficiently big resistance here compared with the resistance 13. The partial pressure of the input terminal 6a and the

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voltage (control input) impressed among 6b is carried out by the resistance 9 and the resistance 14. If the voltage between the input terminal 6a and 6b is more than prescribed voltage, the gate voltage of MOSFET8 will become larger than a threshold, and MOSFET8 will be turned on. If MOSFET8 is turned on, current will flow in the course of the relay input terminals 6a, MOSFET8, the light emitting device 1, and the relay input terminals 6b, and the light emitting device 1 will emit light. If the light emitting device 1 emits light, photoelectromotive force will occur in the photovoltaic cell 2 as usual, and MOSFET3 will be in an ON state.

[0015]On the other hand, if excessive current flows between the relay output terminal 7a and 7b (i.e., between the drain sauce of MOSFET3) and the exothermic temperature of MOSFET3 becomes high, The voltage drop in each diode 10 decreases, the gate voltage of MOSFET12 becomes smaller than threshold voltage, MOSFET12 is turned off, and MOSFET11 is turned on. If MOSFET11 is turned on, the partial pressure of the input terminal 6a and the voltage impressed among 6b will be carried out by the resistance 9 and the resistance 13. The resistance of the resistance 13 is small set up here compared with the resistance of the resistance 14, and it is set as it so that the gate voltage of MOSFET8 may become smaller than a threshold. In short, the resistance of the resistance 14 is set up so that the gate voltage of MOSFET8 may become beyond a threshold, when MOSFET12 is turned on, and the resistance of the resistance 13 is set up so that the gate voltage of MOSFET8 may become smaller than a threshold, when MOSFET11 is turned on.

[0016]Therefore, if MOSFET11 is turned on, MOSFET8 will be in an OFF state and current will flow in the course of the relay input terminals 6a, the resistance 9, the resistance 13, MOSFET11, the light emitting device 1, and the relay input terminals 6b. The resistance of the resistance 9 is set up here so that the current which flows in this course may serve as microampere order, and it becomes impossible to emit light in the light emitting device 1, photoelectromotive force stops occurring in the photovoltaic cell 2 as a result, and MOSFET3 is turned off. That is, MOSFET3 between the relay output terminal 7a and 7b is turned off from an ON state, An over-current can be prevented from continuing flowing into MOSFET3, and the semiconductor relay can be prevented from the thermal runaway of MOSFET3 self or the periphery article being carried out by generation of heat of MOSFET3 by an over-current, and being destroyed. And since it is not necessary to connect a protection circuit like before to MOSFET3, the fault that the gate consumed electric current of MOSFET3 increases, or the switching speed of MOSFET3 becomes slow can be abolished. In short, in this embodiment, destruction of semiconductor switching device slack MOSFET3 or a periphery article can be prevented without change of the output characteristics of a semiconductor relay.

[0017]If the current which flows through the relay input terminals 6a and the voltage impressed among 6b between input voltage (control input), the relay input terminals 6a, and 6b is made into an input current, here, The input characteristics of the semiconductor relay of this embodiment are shown in drawing 2, ** shows input characteristics when temperature is low, and ** shows input characteristics when temperature is high. If an over-current flows into MOSFET3 and exothermic temperature becomes high, an input current becomes small like ** and the light emitting device 1 stops that is, emitting light by having formed the temperature detector 5.

[0018]by the way, the package in which the chip of the semiconductor relay of this embodiment was made by the transfer mold -- ****** -- having -- although -- it is allocated as shown, for example in drawing 3. That is, MOSFET8 to which the temperature detector 5 was connected is arranged on the leadframe of the relay

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input terminals 6a. On the leadframe of the relay input terminals 6b, the light emitting device 1 is arranged so that the leadframe side may serve as a cathode. The anode and the temperature detector 5 of the light emitting device 1 are connected by wirebonding. Photovoltaic-cell 2 and MOSFET3 is arranged on the leadframe of the relay input terminals 7a, and the photovoltaic cell 2 can receive the light from the light emitting device 1, and the insulation between input and output is obtained. The sauce of MOSFET3 is connected to the relay input terminals 7b by wirebonding. Generation of heat of MOSFET3 by an over-current is quickly detectable, and when MOSFET3 generates heat according to an over-current, the light emitting device 1 can be made to switch off promptly, since the temperature detector 5 is allocated here near MOSFET3 by this embodiment.

[0019]If the resistance 9, 13, 14, and 15 and each diode 10 are formed with polysilicon which is a gate electrode material of MOSFET, Since MOSFETs 8, 11, and 12, the resistance 9, 13, 14, and 15, and each diode 10 can be formed in one silicon substrate and 1 chip making can be carried out, while parts are reducible, the size of the whole semiconductor relay can be miniaturized. That is, the inconvenience that the size of the whole semiconductor relay becomes large can be lost by having formed MOSFET8 and the temperature detector 5. If each resistance 9, 13, 14, and 15 and each diode 10 are formed with a polysilicon film, it is not necessary to prepare a manufacturing installation separately, and can form easily.

[0020](Embodiment 2) The circuit diagram of this embodiment is shown in drawing 4. the basic constitution and basic motion of this embodiment -- Embodiment 1 -- abbreviated -- it is the same and different from Embodiment 1 at the point which added the holding circuit 21 which becomes a semiconductor relay of Embodiment 1 from MOSFETs 16, 17, and 18 and the resistance 19 and 20. It is a circuit which the holding circuit 21 makes the OFF state of MOSFET3 hold [circuit] here when the light emitting device 1 is switched off by the temperature detector's 5 detecting generation of heat of MOSFET3, and turning off MOSFET8, and makes the putting-out-lights state of the light emitting device 1 hold. Hereafter, only the point which is different from Embodiment 1 is explained. Each MOSFETs 3, 8, 11, 12, 16, 17, and 18 are enhancement types.

[0021]After excessive current flows between the drain sauce of MOSFET3 in this embodiment, the exothermic temperature of MOSFET3 becomes high and MOSFET11 is turned on, Even if the exothermic temperature of MOSFET3 falls, when there is the holding circuit 21, the ON state of MOSFET11 is held. That is, even if the light emitting device 1 is switched off and the exothermic temperature of MOSFET3 falls, unless the control input between the relay input terminals 6a and 6b is reset, even if there is a control input, the light emitting device 1 emits light. Therefore, since it can prevent turning on MOSFET3 again while load had connected too hastily when load connects too hastily and an over-current flows into MOSFET3, safety improves.

[0022]By what the resistance 9, 13, 14, 15, 19, and 20 and each diode 10 are formed for with a polysilicon film like Embodiment 1 also in this embodiment. MOSFETs 8, 11, 12, 16, 17, and 18, the resistance 9, 13, 14, 15, 19, and 20, and each diode 10 are formed in one chip, and the same effect as Embodiment 1 is acquired.

[0023](Embodiment 3) The circuit diagram of this embodiment is shown in drawing 5. the basic constitution of this embodiment -- Embodiment 1 -- abbreviated -- the point that it is the same and MOSFET8 is a DIPURESHON type. The point that the temperature detector 5 is connected between the sauce of

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MOSFET8 and the anode of the light emitting device 1, the point that direct continuation of the gate of MOSFET8 is carried out to the anode of the light emitting device 1, etc. are different from Embodiment 1. The same numerals are given to the same component as Embodiment 1. Hereafter, operation is explained.

[0024]Since the light emitting device 1 has gone out and there is no photoelectromotive force of the photovoltaic cell 2 when the control input is not given between the relay input terminals 6a and 6b, semiconductor switching device slack MOSFET3 is an OFF state, and it is an OFF state between the relay output terminal 7a and 7b. On the other hand, if a control input is given between the relay input terminals 6a and 6b, when the voltage drop in two or more diodes 10 by which the series connection was carried out arises, MOSFET12 will be in an ON state. MOSFET11 is an OFF state. Therefore, if a control input is given, current will flow in the course of the relay input terminals 6a, MOSFET8, the resistance 14, MOSFET12, the light emitting device 1, and the relay input terminals 6b, and the light emitting device 1 will emit light. If the light emitting device 1 emits light, photoelectromotive force will occur in the photovoltaic cell 2 as usual, and MOSFET3 will be in an ON state. The resistance 14 uses the thing of sufficiently big resistance here compared with the resistance 13.

[0025]On the other hand, if excessive current flows between the relay output terminal 7a and 7b (i.e., between the drain sauce of MOSFET3) and the exothermic temperature of MOSFET3 becomes high, the voltage drop in each diode 10 decreases, the gate voltage of MOSFET12 becomes smaller than threshold voltage, and MOSFET12 is turned off -- MOSFET11 -- an ON state -- ** If MOSFET11 is turned on, current will flow in the course of the relay input terminals 6a, MOSFET8, the resistance 13, MOSFET11, the light emitting device 1, and the relay input terminals 6b. The resistance of the resistance 13 is set up here so that the current which is big resistance compared with the resistance 14, and flows in this course may serve as microampere order. Therefore, if MOSFET11 is turned on, it will become impossible to emit light, photoelectromotive force will stop, generating the light emitting device 1 in the photovoltaic cell 2 as a result, and MOSFET3 will be turned off. That is, between the relay output terminal 7a and 7b can be turned off from an ON state, an over-current can be prevented from continuing flowing into semiconductor switching device slack MOSFET3, and MOSFET3 and a periphery article can be prevented from being destroyed by generation of heat by an over-current. And since it is not necessary to connect a protection circuit like before to MOSFET3, the fault that the gate consumed electric current of MOSFET3 increases, or the switching speed of MOSFET3 becomes slow can be abolished. In short, this embodiment as well as Embodiment 1 can prevent destruction of semiconductor switching device slack MOSFET3 or a periphery article without change of the output characteristics of a semiconductor relay.

[0026]If the current which flows through the relay input terminals 6a and the voltage impressed among 6b between input voltage, the relay input terminals 6a, and 6b is made into an input current, here, The input characteristics of the semiconductor relay of this embodiment are shown in drawing 6, ** shows input characteristics when temperature is low, and ** shows input characteristics when temperature is high. If an over-current flows into MOSFET3 and exothermic temperature becomes high, an input current becomes small and the light emitting device 1 stops that is, emitting light by having formed the temperature detector 5.

[0027]By the way, like Embodiment 1, the chip of the semiconductor relay of this embodiment is allocated, as shown, for example in drawing 7. That is, MOSFET8 to which the temperature detector 5 was connected

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is arranged on the leadframe of the relay input terminals 6a. On the leadframe of the input terminal 6b, the light emitting device 1 is arranged so that the leadframe side may serve as a cathode. The anode and the temperature detector 5 of the light emitting device 1 are connected by wirebonding. Photovoltaic-cell 2 and MOSFET3 is arranged on the leadframe of the relay input terminals 7a, and the photovoltaic cell 2 can receive the light from the light emitting device 1, and the insulation between input and output is obtained. The sauce of MOSFET3 is connected to the relay input terminals 7b by wirebonding. Generation of heat of MOSFET3 by an over-current is quickly detectable, and when MOSFET3 generates heat according to an over-current, the light emitting device 1 can be made to switch off promptly, since the temperature detector 5 is allocated here near MOSFET3 by this embodiment.

[0028]If the resistance 13, 14, and 15 and each diode 10 are formed with polysilicon which is a gate electrode material of MOSFET, Since MOSFETs 8, 11, and 12, the resistance 13, 14, and 15, and each diode 10 can be formed in one silicon substrate and 1 chip making can be carried out, while parts are reducible, the size of the whole semiconductor relay can be miniaturized. That is, the inconvenience that the size of the whole semiconductor relay becomes large can be lost by having formed MOSFET8 and the temperature detector 5. If the resistance 13, 14, and 15 and the diode 10 are formed with a polysilicon film, it is not necessary to prepare a manufacturing installation separately, and can form easily.

[0029](Embodiment 4) The circuit diagram of this embodiment is shown in drawing 8. the basic constitution and basic motion of this embodiment -- Embodiment 3 -- abbreviated -- it is the same and different from Embodiment 3 at the point which added the holding circuit 21 which becomes a semiconductor relay of Embodiment 3 from MOSFETs 16, 17, and 18 and the resistance 19 and 20. It is a circuit which maintains putting out lights of the light emitting device 1 here by making the ON state of MOSFET11 hold when, as for the holding circuit 21, the temperature detector 5 detects generation of heat of MOSFET3 and MOSFET11 is turned on. Hereafter, only the point which is different from Embodiment 3 is explained. MOSFETs 3, 11, 12, 16, 17, and 18 are enhancement types, and only MOSFET8 is a depletion type.

[0030]After excessive current flows between the drain sauce of MOSFET3 in this embodiment, the exothermic temperature of MOSFET3 becomes high and MOSFET11 is turned on, Even if the exothermic temperature of MOSFET3 falls, when there is the holding circuit 21, the ON state of MOSFET11 is held. That is, even if the exothermic temperature of MOSFET3 falls by switching off the light emitting device 1, unless the control input between the relay input terminals 6a and 6b is reset, even if there is a control input, the light emitting device 1 emits light. Therefore, since it can prevent turning on MOSFET3 again while load had connected too hastily when load connects too hastily and an over-current flows into MOSFET3, safety improves.

[0031]By what the resistance 13, 14, 15, 19, and 20 and each diode 10 are formed for with a polysilicon film like Embodiment 3 also in this embodiment. Each MOSFETs 8, 11, 12, 16, 17, and 18, each resistance 13, 14, 15, 19, and 20, and each diode 10 are formed in one chip, and the same effect as Embodiment 3 is acquired.

[0032]

[Effect of the Invention]The light emitting device which turns on and switches off the invention of claim 1 by a control input, and the photovoltaic cell which carried out optical coupling to said light emitting device, The semiconductor switching device turned on and off according to lighting and putting out lights of said light

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emitting device by impressing the photoelectromotive force of said photovoltaic cell to a control end, Since it has the temperature detector which makes said light emitting device switch off if ambient air temperature is detected and this ambient air temperature becomes more than prescribed temperature, If an over-current flows into said semiconductor switching device and the ambient air temperature of a temperature detector becomes more than prescribed temperature, when the light emitting device is on, since said light emitting device will be switched off, An over-current can be prevented from said semiconductor switching device turning off and continuing flowing into said semiconductor switching device, without providing a protection circuit like before, As a result, it is effective in the ability to prevent that the thermal runaway of the semiconductor switching device is carried out, or the thermal runaway of the periphery article is carried out, maintaining the output characteristics of a relay.

[0033]Since the invention of claim 2 added the holding circuit which maintains putting out lights of a light emitting device in the invention of claim 1 when a semiconductor device was turned off by the temperature detector, It is effective in safety improving, without one [a semiconductor switching device] since putting out lights of a light emitting device is maintained even if the temperature of a semiconductor switching device becomes low. In the invention of claim 1 or claim 2, since the invention of claim 3 is allocated near the semiconductor switching device, a temperature detector, It is effective in it becoming possible to make a semiconductor switching device turn off promptly of detecting the rise in heat of a semiconductor switching device promptly and efficiently.

[0034]As for the invention of claim 4, a part of temperature detector is constituted by a diode and resistance in the invention of claim 1 thru/or claim 3, Since said diode and said resistance are formed with polysilicon which is a gate electrode material of a semiconductor switching device, it is not necessary to prepare a manufacturing installation for forming said diode and said resistance separately, and can form easily. And since it becomes possible to be integrated to the same substrate as a semiconductor switching device and part mark can be reduced, it is effective in becoming possible to prevent enlargement of the size of the whole relay by having provided the temperature detector.

[Translation done.]

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* NOTICES *

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2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1]It is a circuit diagram showing Embodiment 1.
[Drawing 2]It is an explanatory view of operation same as the above.
[Drawing 3]It is a chip plot plan same as the above.
[Drawing 4]It is a circuit diagram showing Embodiment 2.
[Drawing 5]It is a circuit diagram showing Embodiment 3.
[Drawing 6]It is an explanatory view of operation same as the above.
[Drawing 7]It is a chip plot plan same as the above.
[Drawing 8]It is a circuit diagram showing Embodiment 4.
[Drawing 9]It is a circuit diagram showing a conventional example.
[Description of Notations]
1 Light emitting device
2 Photovoltaic cell
3 MOSFET
4 Control circuit
5 Temperature detector
6a, 6b relay input terminals
7a, 7b relay output terminal
8 MOSFET
9 Resistance
10 Diode
11 MOSFET
12 MOSFET

[Translation done.]

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* NOTICES *

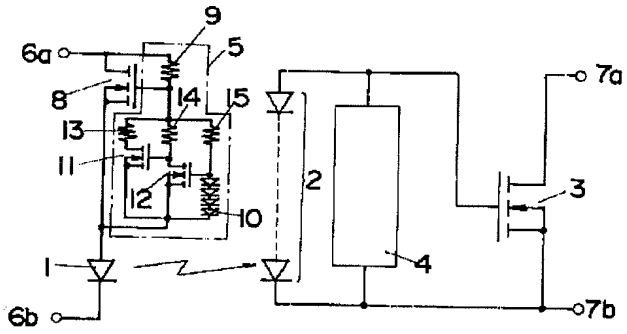
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2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

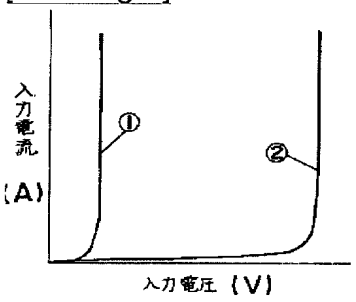
DRAWINGS

[Drawing 1]

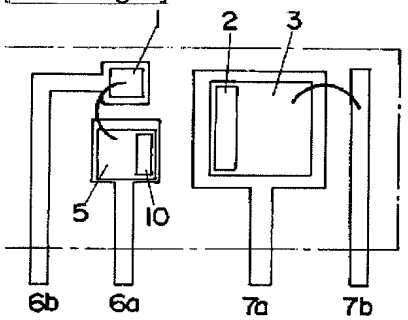
1 発光素子
2 光起電力素子
3 MOSFET
4 制御回路
5 温度検出素子
6 a，6 b リレー入力端子
7 a，7 b リレー出力端子
8 MOSFET
9 抵抗
10 ダイオード
11 MOSFET
12 MOSFET



[Drawing 2]

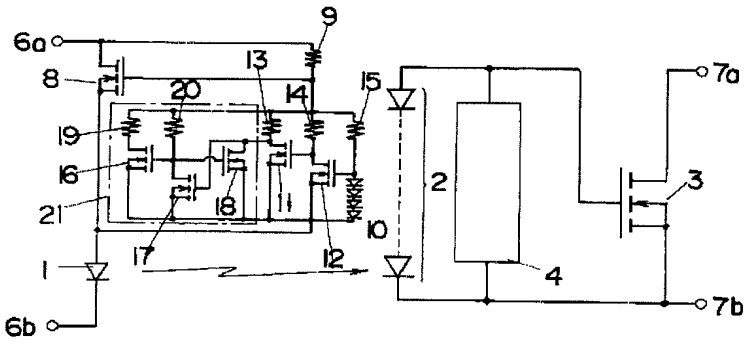


[Drawing 3]

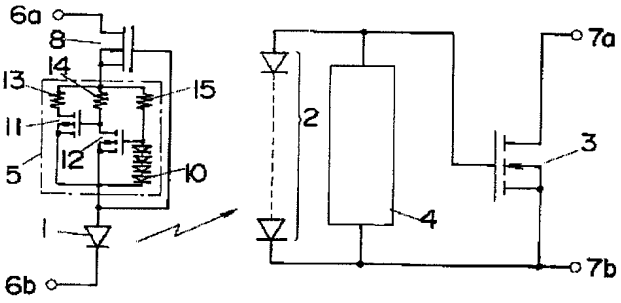


[Drawing 4]

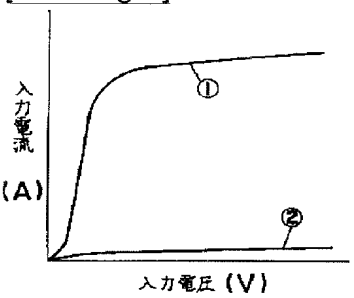
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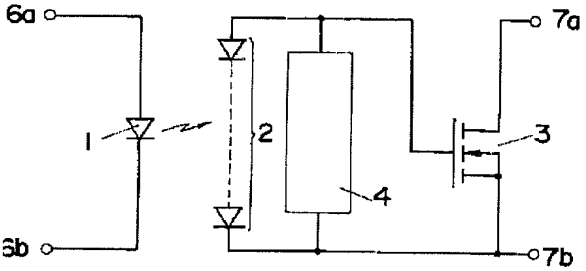
[Drawing 5]



[Drawing 6]

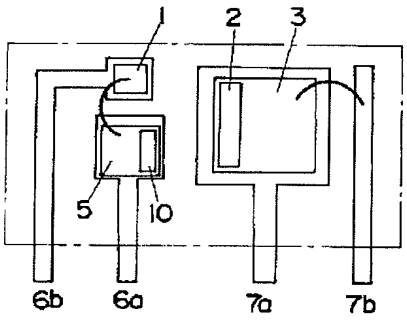


[Drawing 9]

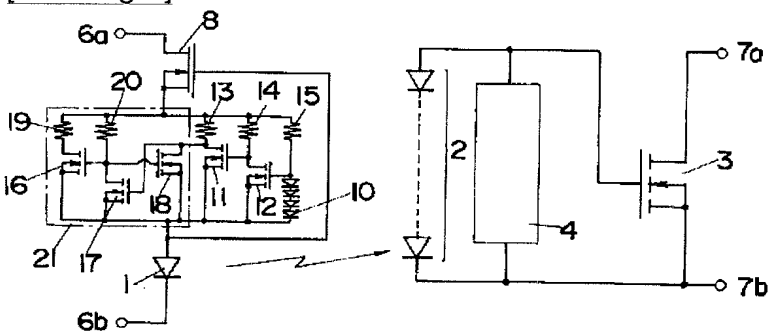


[Drawing 7]

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[Drawing 8]



[Translation done.]

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AC

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G01R 31/00

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G1U UR3100
U1S S2062

(56) Documents cited
GB 2110388 A GB 2101339 A GB 2089591 A
GB 2022849 A EP 0050417 A1

(58) Field of search
UK CL (Edition K) G1U UR3100

(71) Applicant
Alireza Ghazi Hessami
124 Park Road, Loughborough, Leics., LE11 2HH, United Kingdom

(72) Inventor
Alireza Ghazi Hessami

(74) Agent and/or Address for Service
Alireza Ghazi Hessami
124 Park Road, Loughborough, Leics., LE11 2HH, United Kingdom

(54) Universal digital input channel

(57) To detect the on/off state of a switch (SW1) in a circuit including a source (Ve) and a varistor (RV1), a bridge (BR) rectifies the voltage existing across the varistor (RV1) and energises a circuit including two transistors (TR1, TR2) and two LED's (D1, ISD1), one of the LED's (ISD1) being an opto-isolator device in an output circuit including an amplifier (ICA). With the switch on, both LED's emit light and an electrical output (01) is produced by the amplifier (ICA).

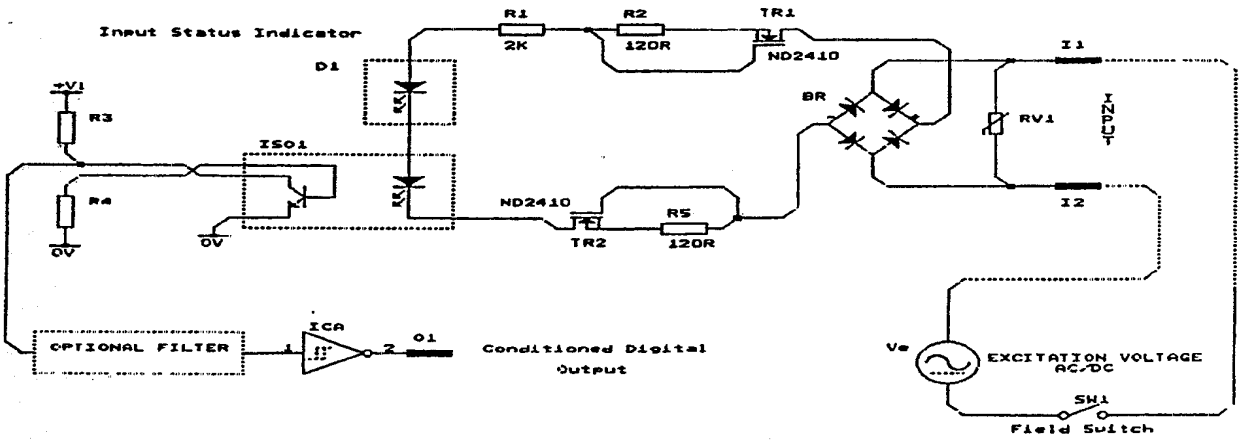


Figure 2

At least one drawing originally filed was informal and the print reproduced here is taken from a later filed formal copy.

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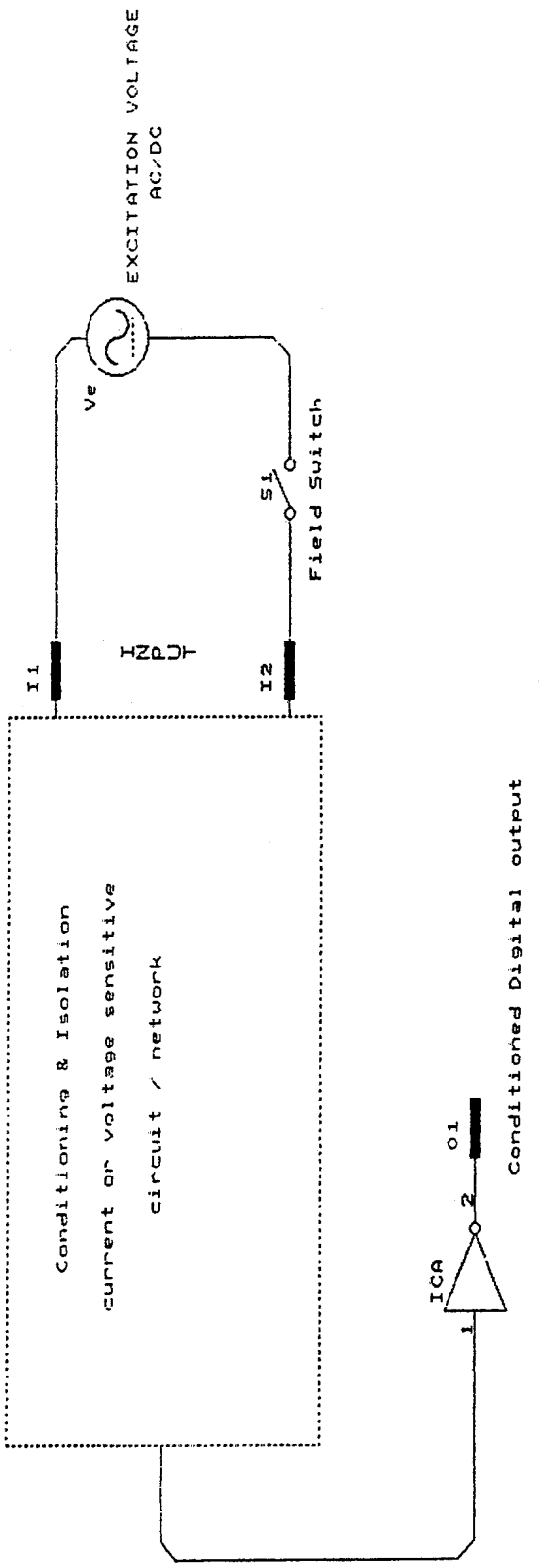

EXCITATION VOLTAGE
AC/DC
Ve
S1
Field Switch
I1
HZDH
I2
Conditioning & Isolation
current or voltage sensitive
circuit / network
ICA
O1
2
1
Conditioned Digital output

Figure 1

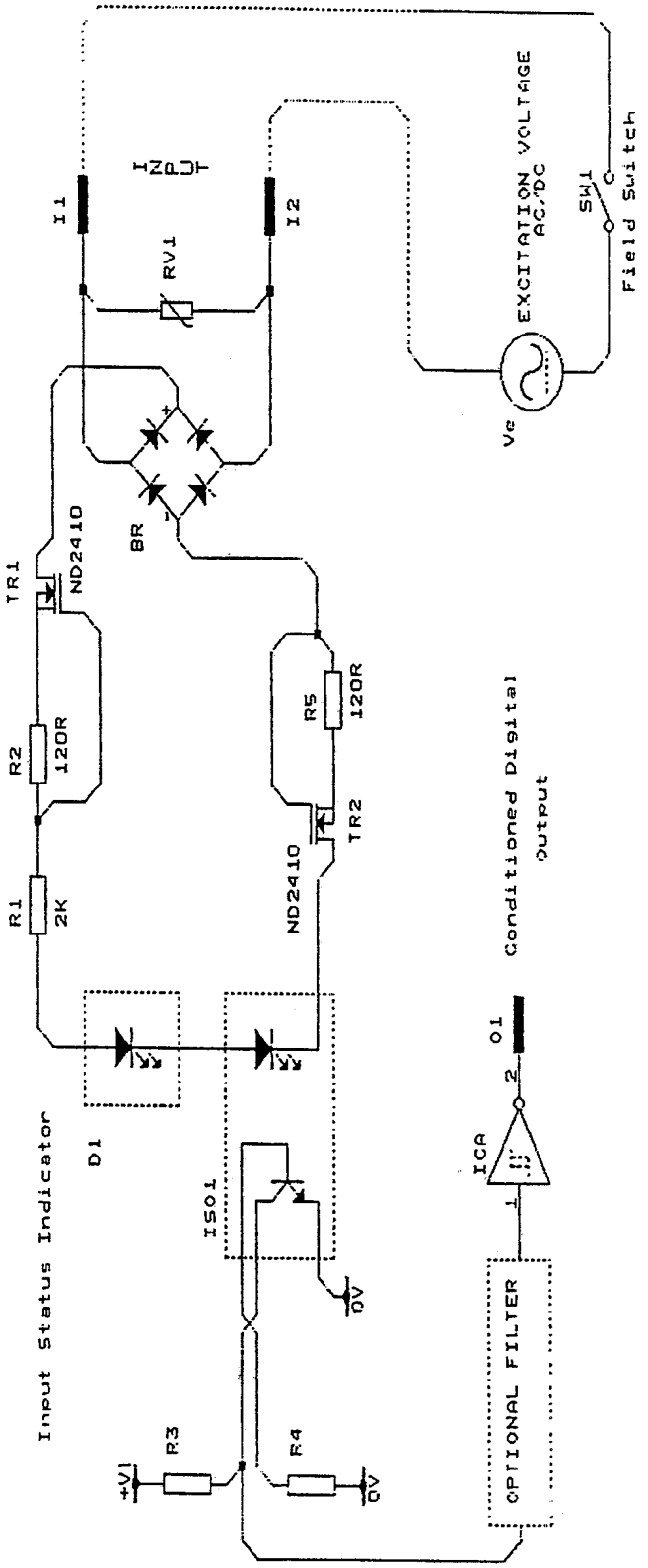

I1
I2
INPUT
RV1
EXCITATION VOLTAGE
AC/DC
SW1
Field Switch
Ve
BR
TR1
ND2410
R2
120R
R1
2K
R5
120R
TR2
ND2410
Conditioned Digital
Output
O1
2
ICA
1
OPTIONAL FILTER
D1
Input Status Indicator
ISO1
0V
R3
R4
+Vl
0V

Figure 2

UNIVERSAL DIGITAL INPUT CHANNEL

This invention,

(Universal Digital Input Channel)

relates to an electronic circuit employed for inputting ON/OFF type digital data to electronic and computing machines for processing.

It is primarily aimed at industrial automation applications where, field data from typically remote switches and binary output sensors, need to be converted to a suitable signal for interfacing to supervisory and/or control systems.

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2. Introduction :

There are three broad categories of signals to which, computing and control systems interface. These are analogue, digital and pulse types respectively.

Analogue signals such as temperature, pressure, speed, level etc., constitute the most prevalent category and generally embody a broad spectrum of amplitude and frequency varying variables encountered in most natural and man made processes.

Digital or two-state signals largely exist within the domain of man made systems and thus, can only assume one of two mutually exclusive states such as ON/OFF, HIGH/LOW etc. They can be regarded as a special type of analogue signals with pre-defined amplitude conventions. In the field, steady state digital signals typically originate from switches or sensors designed to approximate often inherently analogue variables into two state representations above or below a desired threshold.

Pulse signals constitute digital signals with a broad variation in frequency domain.

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3. Signal Interfacing Techniques :

Most electronic/computer based supervisory and control systems require a relatively large number of signal inputs. The state or value of the input variables are fed to a hardware/software control algorithm. This in turn generates a number of output states/values to be conditioned and interfaced to the process in order to mantain it within desired operating conditions.

Analogue signals typically require careful input conditioning in order to provide a true representation of the measured variable. The conditioning is often in the form of amplitude scaling, frequency limiting/filtering and analogue to digital conversion which lies beyond the scope of the present document.

Digital variables on the other hand are easier to detect and interface. For example, the ON or OFF state of a switch is readily determined by it's ability to complete an electrical circuit when closed (ON). This technique is widely employed in interfacing digital signals to electronic/computer supervisory and/or control systems. A voltage source is typically applied via the switch/sensor whose state is to be determined, to a current/voltage sensitive device/circuit. The closure of the switch completes the electrical circuit allowing voltage to appear accross or current to flow through the sensing device/circuit thus changing it's state. Figure 1 represents the principles of this method of detection.

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4. Digital Signal Interfacing:

The ability of a switch or a binary sensor such as a Thermostat to complete an electrical circuit upon closure, is widely employed to detect the state of such devices in electronic/computing supervisory and/or control systems. Normally a DC voltage source of limited amplitude is applied to such circuits as the excitation energy. The state of a switch is thus determined through an appropriate method of detecting the current flow through the circuit. The ON or OFF state of the switch corresponding to flow or no-flow of electrical current in such a circuit is thus determined through a current/voltage sensing device in the same circuit.

Figure 1 represents the general principles of ON/OFF type signal interfacing to supervisory and control systems. Programmable Logic Controllers (PLC's) are computer based machines, in widespread use throughout industry. These are often equipped with a limited number of digital (ON/OFF) input and output channels. The digital input channels on PLC's predominately employ the principles of state detection highlighted above.

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5. Universal Digital Input Channel (UDIC):

This innovation relates to an electronic circuit employed to detect the state of a switch by the application of any AC or DC excitation voltage from a few volts up to the mains level. Most digital input channels can cope with DC or AC excitation voltages of limited range.

The Universal Digital Input Channel (UDIC) differs from the common circuits, in it's ability to cope with DC and AC excitation voltages ranging from a few volts to a few hundred volts dynamically. This versatility is achieved through exploitation of a novel solid-state circuitry.

A specific embodiment of the invention will now be described by way of example with reference to the accompanying drawings in which;

- Figure 1 represents general principles of digital state detection,
- Figure 2 represents a typical UDIC circuit arrangement.

A typical field switch SW1 in series with the excitation voltage source Ve is applied to the inputs I1,I2 of the UDIC in Figure 2. The excitation voltage source may be of AC or DC type with RMS values from a few volts to 240 volts maximum. The UDIC inputs are not polarity sensitive.

The Varistor RV1 is rated at just above 240V RMS and is intended to absorb impulse noise. The bridge rectifier BR rated at 1 Ampere maximum is employed to rectify the AC inputs. TR1 and TR2 are N channel depletion mode MOSFET transistors. They are equivalent to normally ON switches each rated at V(BR)Dss > 240V. Resistors R1 & R2 are biasing elements for TR1,TR2 while R1 is intended for static current limiting. The LED D1, is employed as status indicator which is in series with the opto-isolator ISO1. The optical device is chosen to provide high voltage galvanic isolation between the input and output of UDIC.

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5.1. Circuit Operation;

The principles of operation of UDIC are now described with reference to the circuit of Figure 2 in which, a field switch SW1 in series with an AC/DC excitation voltage source are connected to the input terminals I1,I2 for illustartion only.

When SW1 is open (OFF), no current would flow through the circuit composed of the Ve, SW1 and UDIC. The status indicator D1 would <u>not</u> be lit and the UDIC output at O1 would be LOW.

Upon closure of SW1, the electrical circuit would be completed and AC or DC current would flow through the input stage of UDIC. Voltage spikes and transients greater than 240V would be absorbed by RV1. Current would flow through SW1, BR, TR1, R2, R1, D1, ISO1, TR2 and R5. At low voltage/current levels, TR1 and TR2 are almost fully ON, posing very little resistance. Hence, under these conditions, the magnitude of current would be determined by the voltage applied at I1,I2 less the drop across D1,ISO1 divided by the value of R1. With the values shown in Figure 2, the input current would be of the order of 7 mA at 24V DC nominal excitation voltage. This is termed the " Static " mode of operation.

However, as the excitation voltage is increased, there would be a tendency for the current in the input stage of UDIC to increase. Owing to the presence of TR1 & TR2 in the UDIC, the increase in current due to a rise in excitation voltage would be counteracted by the increasing negative bias produced by R2 & R5. This bias applied between the gate and source of the depletion MOSFETs, would gradually force them into less conductive region, thus dynamically increasing the circuit (UDIC) impedance. This increase in circuit impedance in turn limits the current flow, protecting SW1 and UDIC from damage which would otherwise be caused by large currents at high excitation voltages (> 100V). It is this " Dynamic " impedance characteristic which enables UDIC to cope with excitation voltages from 12 volts to 240 volts AC or DC without damage.

The closure of SW1 would produce a HIGH voltage at the output O1.

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5.2. Special Considerations;

In a typical UDIC implementation, the value of R1 would determine the " Static " i.e. low voltage (in the region of few tens of volts) current flow in the circuit. The value of R1 limiting resistor is calculated to provide sufficient current flow through the circuit under " Static " conditions. This corresponds to the lowest nominal excitation voltage which in the case of UDIC is rated at 12V RMS.

The biasing resistors R2 and R5 are typically much smaller in value than R1 and their values determine the maximum current through the input stage of UDIC at high excitation voltages (> 100V RMS) i.e. the " Dynamic " mode of operation. The highest nominal excitation voltage in the case of UDIC is rated at 240V RMS which implies that Mains voltage can be safely employed as the external excitation voltage in series with the field switch.

The sensitivity of the circuit in the " Static " mode of operation can be further adjusted via R4 which, supplies a ground path for the base current of the opto-transistor in the opto-coupler.

A UDIC channel can typically cope with excitation currents ranging from 2mA to 10mA maximum. It is also necessary to closely match the $V_{GS(th)}$ of the TR1 & TR2 in order to ensure reasonable load sharing between the devices in the " Dynamic " mode of operation.

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5.3. Application Specific Features;

The optional filtering circuit shown in figure 2 may be of simple RC type networks employed to debounce the field switch SW1.

Some operational specifications such as the isolation voltage between the front-end and the output stage largely depend upon the circuit layout as well as the isolation specifications of the opto-isolator employed in the circuit.

Depending on the real-estate available on the Printed Circuit Board (PCB), a large number of UDIC channels may be designed on a single board for simultaneous parallel operation. This may be of interest in the transmission of parallel digital data over long distances using high voltages to compensate for line drops.

If AC voltage is to be used for excitation, application of a 110V AC, safety transformer is recommended. These transformers provide a ground referenced centre tap on their secondary thus, reducing the probability of electrical shock in the event of contact with the 110V output.

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6. Claims :

° Universal Digital Input Channel (UDIC) provides an innovative, cost effective and convenient method for interfacing ON/OFF type data to electronic/computer based supervisory/control systems.

° UDIC employs a novel yet simple and low cost solid-state circuitry and provides non-polarised input terminals for convenience and ease of field wiring.

° Application of UDIC removes the requirement for often expensive special purpose power supplies employed as excitation voltage source in most digital input schemes.

° Application of UDIC permits the use of any convenient voltage source from 12V DC (Battery) up to 240V AC Mains voltage in interfacing ON/OFF data to supervisory/control systems.

° UDIC provides a universal circuit for sensing the status of ON/OFF type data while, galvanically isolating the front-end interface circuitry from the rest of the supervisory/control system.

° Application of UDIC leads to a considerable reduction in inventory of digital input interfaces for the manufacturer as well as the user. This would be of particular relevance to Programmable Logic Controllers (PLC's) which typically employ a broad range of digital input interfaces for various excitation voltage levels and AC/DC types.

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Patents Act 1977
Examiner's report to the Comptroller under Section 17 (The Search Report)

Application number 9024694.3

Relevant Technical fields

(i) UK Cl (Edition K) G1U UR3100

(ii) Int Cl (Edition)

Search Examiner

K F J NEAL

Databases (see over)

(i) UK Patent Office

(ii)

NONE

Date of Search

4.4.91

Documents considered relevant following a search in respect of claims ALL CLAIMS

Category (see over)	Identity of document and relevant passages	Relevant to claim(s)
X	GB 2110388 A (YORKSHIRE) figures 1-7	1
X	GB 2101339 A (GENERAL) figures 1-3	1
X	GB 2089591 A (RESTBURY) figures 1-4	1
X	GB 2022849 A (HONEYWELL) figures 1-4	1
X	EP 0050417 A1 (HONEYWELL) figure 1	1

SF2(p)

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3NSDOCID: <GB_____2249840A__I_>

Category	Identity of document and relevant passages	Relevant to claim(s)

Categories of documents

X: Document indicating lack of novelty or of inventive step.

Y: Document indicating lack of inventive step if combined with one or more other documents of the same category.

A: Document indicating technological background and/or state of the art.

P: Document published on or after the declared priority date but before the filing date of the present application.

E: Patent document published on or after, but with priority date earlier than, the filing date of the present application.

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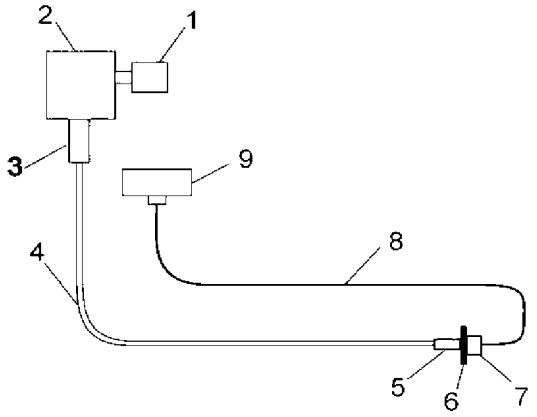
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(71)出願人　597178113
松浦　祐司
宮城県仙台市太白区三神峯２－１２－６５
(71)出願人　593138584
宮城　光信
宮城県仙台市青葉区荒巻字青葉無番地　東北大学工学部内
(72)発明者　松浦　祐司
宮城県仙台市青葉区荒巻字青葉（番地なし）　東北大学
(72)発明者　宮城　光信
宮城県仙台市青葉区荒巻字青葉（番地なし）　東北大学

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(54)【発明の名称】蛍光体の発光特性評価法

(57)【要約】
【課題】　微小蛍光体サンプルもしくは蛍光体パネル微細部の発光特性を能率よく評価するための測定系を，小型かつ低コストで提供する。
【解決手段】　分光器により単色化された紫外もしくは真空紫外励起光を，内部が真空化もしくは吸収性の小さなガスで充填された中空光ファイバによって蛍光体試料に照射し，発生した蛍光をガラス光ファイバにより検出する。
【選択図】　図1



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【特許請求の範囲】
【請求項1】
中空光ファイバによって励起光を蛍光体に照射し，発生した蛍光を検出することを特徴とする蛍光体の発光特性評価法
【請求項2】
前記励起光が，紫外光もしくは真空紫外光であることを特徴とする請求項１に記載の蛍光体の発光特性評価法
【請求項3】
前記励起光が，分光器により単色化された光であることを特徴とする請求項１に蛍光体の発光特性評価法
【請求項4】
前記中空光ファイバが，ガラス細管の内面にアルミニウム薄膜を形成した中空光ファイバであることを特徴とする請求項１に記載の蛍光体の発光特性評価法

【発明の詳細な説明】
【技術分野】
【0001】
本発明は，蛍光体の発光特性評価法に関するものである。
【背景技術】
【0002】
　プラズマディスプレイは，各画素ごとに設けられた電極において真空放電を発生させ，それにより発生した真空紫外および紫外光で蛍光体を励起することにより，可視光を得るものである。この蛍光体の開発においては，励起光波長に対する蛍光波長分布特性を評価することが必要である。しかし，励起光は空気中で減衰してしまう真空紫外領域の光も含むため，従来の評価装置では，すべての光路を真空，もしくは窒素などでガス置換された雰囲気に保つ必要があった。そのため，測定サンプルは金属チャンバーなどの試料室内に収納され，同じく金属容器内に設置されたミラーなどによりサンプルへ励起光を導光していた。
【0003】
それゆえ，蛍光体の特性評価には，規模的にもコスト的にも大きな設備が必要とされるうえ，試料室の真空化もしくはガス置換に要する時間が大きく，時間的に能率の高い評価は困難であった。また，評価サンプルは容器内に収まる程度の大きさである必要があり，パネル化されたディスプレイの各画素の評価を行うことは困難であった。
【0004】
また，各種化合物の分析にも真空紫外光励起により発生する蛍光特性が用いられる。この場合も従来の測定装置においては，測定サンプルを金属容器内に収納し，真空化もしくはガス置換を行うため，能率およびサンプルの大きさに制限があった。
【特許文献1】特許第３３４１００７号
【発明の開示】
【発明が解決しようとする課題】
【0005】
そこで本発明の目的は，微小蛍光体サンプルもしくは蛍光体パネル微細部の発光特性を能率よく評価するための測定系を，小型かつ低コストで実現することにある。
【課題を解決するための手段】
【0006】
本発明は上記の目的を達成するために，中空光ファイバによって励起光を蛍光体に照射し，発生した蛍光を検出することを特徴とする蛍光体の発光特性評価法である。
【0007】
ここで前記励起光が，紫外光もしくは真空紫外光であってもよい。
【0008】
ここで前記励起光が，分光器により単色化された光であってもよい。

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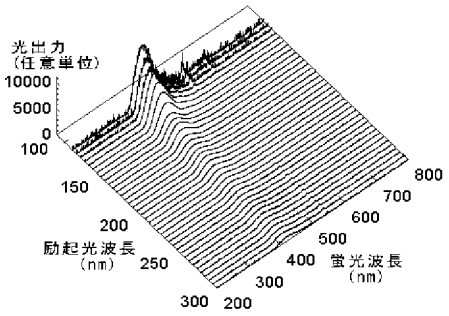
【0009】
ここで前記中空光ファイバが，ガラス細管の内面にアルミニウム薄膜を形成した中空光ファイバであってもよい。
【発明の効果】
【0010】
本発明の蛍光体の発光特性評価法であれば，微小な蛍光体試料や蛍光体パネル微細部の発光特性を能率よく評価することが可能である。
【0011】
また，蛍光体サンプルの大きさに制限がなく，大型パネルの微細部の評価が可能である。
【0012】
試料室を設ける必要がないため，真空化やガス置換にかかる時間が短縮され，高能率な評価が可能である。
【0013】
評価装置の小型化・低コスト化が可能である。
【発明を実施するための最良の形態】
【0014】
以下，本発明の実施の形態を例示して詳述する。図１に測定系の概要を示す。分光された真空紫外光をファイバ結合部３を介して中空ファイバ４によって伝送し試料６に照射する。結合部３はファイバ４に最大の光量を入射できるよう光軸を調整するためのものである。真空紫外光伝送用ファイバ４として内径１ｍｍ，長さ１ｍのアルミニウム中空ファイバを使用する。アルミニウム中空ファイバの典型的な損失波長特性においては，波長１００ｎｍから３００ｎｍにおいてほぼ平坦な損失特性となっており，励起光の波長域では，測定誤差の原因となる，急峻な損失ピークなどは存在しない。ファイバの直径を小さくすることで，より高い空間分解能を得ることができ，より小さなサンプルの測定も可能となる。ただし，充分な光量が得られるように，ファイバ内径は１００μｍ以上１ｍｍ以下であることが好ましい。また，複数の中空光ファイバを束ねて使用することによっても，より大きな光量が得られる。
【0015】
ファイバ出射端をフッ化マグネシウム，フッ化カルシウム，合成石英などの，紫外から真空紫外領域で透明な窓材で封止することにより光源から試料までの光路を真空化する。上記窓材を予め接着したシーリングキャップ５を出射端に装着することで容易に封止することができる。サンプル６は，粉末状であればエチルアルコールなどに溶いてガラス基板上に塗布・乾燥したものを用い，固体状であればそのまま用いることができる。サンプル６をファイバ出射端に押し当てて真空紫外光を照射し，発生した蛍光をサンプル背面から石英ガラスファイバ８で検出し，ファイバ入射型の可視域小型分光器９によって出力を測定する。
【0016】
図２はサンプルとしてサリチル酸ナトリウムを用いた場合の蛍光特性の測定結果である。なお，予め測定した中空ファイバ出射端部における真空紫外照射光の出力スペクトルを用いて蛍光出力を正規化している。波長約３５０ｎｍから５００ｎｍにおける蛍光の発生が観察され，そのスペクトルの照射光波長依存性の測定が可能であることを確認した。照射光の波長範囲は１４０ｎｍ
から３００ｎｍであり，短波長側は主に酸素による吸収によって制限されている。これは，ファイバ内の真空度を向上させることにより更に短波長の真空紫外光を照射することが可能である。
【図面の簡単な説明】
【0017】
【図1】本発明の一実施形態を示す配置図である。
【図2】本発明の効果を示す蛍光特性の測定結果を表す図である。
【符号の説明】

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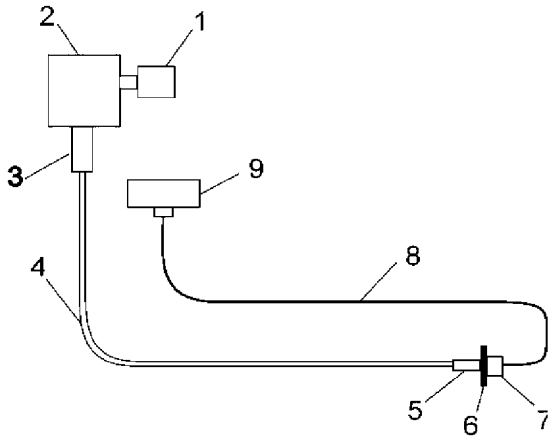
【0018】

1　重水素ランプ
2　真空紫外分光器
3　ファイバ入射結合部
4　中空光ファイバ
5　シーリングキャップ
6　試料
7　ガラス光ファイバ入射端部
8　ガラス光ファイバ
9　可視域分光器

【図2】



【図1】



PATENT ABSTRACTS OF JAPAN

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(43)Date of publication of application : 14.09.2006

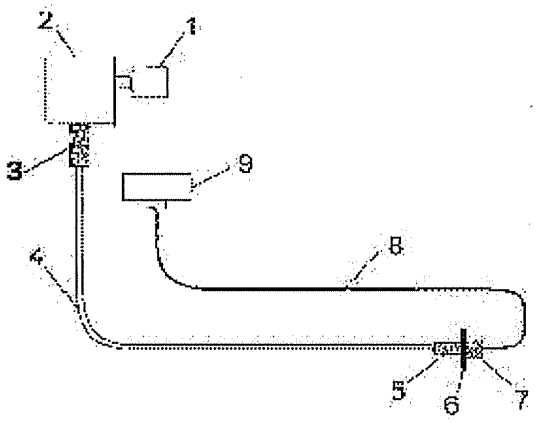
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(21)Application number : 2005-058389
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(71)Applicant : MATSUURA YUJI
MIYAGI MITSUNOBU
(72)Inventor : MATSUURA YUJI
MIYAGI MITSUNOBU

(54) EMISSION CHARACTERISTIC EVALUATING METHOD OF FLUORESCENT SUBSTANCE

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a small-sized inexpensive measuring system for efficiently evaluating the emission characteristics of a micro-fluorescent sample or the fine part of a fluorescent panel.
SOLUTION: A fluorescent sample is irradiated with ultraviolet or vacuum ultraviolet exciting light made monochromatic by a spectroscope by a hollow optical fiber which is internally evacuated or filled with a low-absorbability gas and the emitted fluorescence from the sample is detected by a glass optical fiber.



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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[Field of the Invention]
[0001]
This invention relates to the luminescent characteristic appraisal method of a fluorescent substance.
[Background of the Invention]
[0002]
A plasma display obtains visible light by exciting a fluorescent substance by the vacuum ultraviolet and ultraviolet radiation which were made to generate vacuum discharge in the electrode provided for every pixel, and this generated. In development of this fluorescent substance, it is required to evaluate the fluorescence wavelength distribution characteristic to excitation light wavelength. However, since excitation light also contained the light of the vacuum ultraviolet region decreased in the air, it needed to maintain all the optical paths at the atmosphere by which inert gas replacement was carried out with a vacuum or nitrogen in the conventional evaluation system. Therefore, the measuring sample was stored in sample chambers, such as a metal chamber, and was carrying out the light guide of the excitation light to the sample by the mirror etc. which were similarly installed in the metal vessel.
[0003]
So, the big equipment also in cost also in scale is needed for the characterization of a fluorescent substance, and also the time which vacuation or inert gas replacement of a sample chamber takes was large to it, and efficient evaluation was difficult for it in time. The evaluation sample needed to be a size of the grade settled in a container, and it was difficult to perform evaluation which is each pixel of the panel-ized display.
[0004]
The fluorescent characteristic generated by vacuum-ultraviolet-light excitation is used also for analysis of various compounds. In order to store a measuring sample in a metal vessel in the conventional measuring device also in this case and to perform vacuation or inert gas replacement, efficiency and the size of a sample had restriction.
[Patent documents 1] Patent No. 3341007
[Description of the Invention]
[Problem(s) to be Solved by the Invention]
[0005]

Then, the purpose of this invention is to realize the system of measurement for often evaluating the luminescent characteristic of a minute phosphor sample or a phosphor panel detailed part by small size and low cost.

[Means for Solving the Problem]

[0006]

This invention is a luminescent characteristic appraisal method of a fluorescent substance irradiating a fluorescent substance with excitation light with hollow optical fiber, and detecting generated fluorescence, in order to attain the above-mentioned purpose.

[0007]

Said excitation light may be ultraviolet radiation or vacuum ultraviolet light here.

[0008]

Said excitation light may be the light monochrome-ized by a spectroscope here.

[0009]

Said hollow optical fiber may be the hollow optical fiber which formed an aluminum thin film in an inner surface of a glass capillary here.

[Effect of the Invention]

[0010]

If it is a luminescent characteristic appraisal method of the fluorescent substance of this invention, it is possible to often evaluate the luminescent characteristic of a minute fluorescent substance sample or a phosphor panel detailed part.

[0011]

There is no restriction in the size of a phosphor sample, and evaluation of the detailed part of a large size panel is possible.

[0012]

Since it is not necessary to provide a sample chamber, the time concerning vacuation or inert gas replacement is shortened, and highly efficient evaluation is possible.

[0013]

A miniaturization and low-cost-izing of an evaluation system are possible.

[Best Mode of Carrying Out the Invention]

[0014]

Hereafter, an embodiment of the invention is illustrated and explained in full detail. The outline of a system of measurement is shown in drawing 1. The vacuum ultraviolet light by which the spectrum was carried out is transmitted with the hollow fiber 4 via the fiber coupling part 3, and the sample 6 is irradiated. It is for the bond part 3 adjusting an optic axis so that the maximum light volume can be entered into the fiber 4. An aluminum hollow fiber 1 mm in inside diameter and 1 m in length is used as the fiber 4 for vacuum-ultraviolet-light transmission. In the typical loss wavelength characteristic of an aluminum hollow fiber, in 300 nm, it is almost flat loss property from the wavelength of 100 nm, and steep loss peaks leading to an error of measurement do not exist in the wavelength band of excitation light. Higher spatial resolving power can be obtained by making the diameter of a fiber small, and measurement of a smaller sample is also attained. However, as for a fiber inside diameter, it is preferred that it is [not less than 100 micrometer] 1 mm or less so that sufficient light volume may be obtained. Bigger light volume is obtained also by bundling and using

two or more hollow optical fiber.

[0015]

The optical path from a light source to a sample is vacuated by closing a fiber emitting end with a transparent window material from ultraviolet [, such as magnesium fluoride, calcium fluoride, and synthetic quartz,] in a vacuum ultraviolet region. It can close easily by equipping an emitting end with the sealing cap 5 on which the above-mentioned window material was pasted up beforehand. If the sample 6 is powdered, it will be melted in ethyl alcohol etc., and using what was applied and dried on the glass substrate, if it is a solid state, it can be used as it is. The sample 6 is pressed against a fiber emitting end, it irradiates with vacuum ultraviolet light, the quartz glass fiber 8 detects the generated fluorescence from the sample back, and an output is measured with the visible range small spectroscope 9 of a fiber incoming radiational type.

[0016]

Drawing 2 is a measurement result of the fluorescent characteristic at the time of using sodium salicylate as a sample. The fluorescence output is normalized using the output spectrum of the vacuum-ultraviolet irradiation light in the hollow fiber emitting end part measured beforehand. Generating of the fluorescence at 500 nm was observed from the wavelength of about 350 nm, and it checked that measurement of the irradiation light wavelength dependency of the spectrum was possible. The wavelength range of irradiation light is 140 nm.

It is ** et al. [300-nm], and the short wavelength side is mainly restricted by absorption by oxygen. This can be further irradiated with the vacuum ultraviolet light of short wavelength by raising the degree of vacuum in a fiber.

[Brief Description of the Drawings]

[0017]

[Drawing 1]It is a plot plan showing one embodiment of this invention.

[Drawing 2]It is a figure showing the measurement result of the fluorescent characteristic which shows the effect of this invention.

[Description of Notations]

[0018]

1 Deuterium lamp
2 Vacuum-ultraviolet spectroscope
3 Fiber incidence bond part
4 Hollow optical fiber
5 Sealing cap
6 Sample
7 Glass optical fibre incident end part
8 Glass optical fibre
9 Visible range spectroscope

[Translation done.]

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CLAIMS

[Claim(s)]
[Claim 1]
A luminescent characteristic appraisal method of a fluorescent substance irradiating a fluorescent substance with excitation light with hollow optical fiber, and detecting generated fluorescence
[Claim 2]
A luminescent characteristic appraisal method of the fluorescent substance according to claim 1, wherein said excitation light is ultraviolet radiation or vacuum ultraviolet light
[Claim 3]
It is a luminescent characteristic appraisal method of a fluorescent substance to claim 1, wherein said excitation light is the light monochrome-ized by a spectroscope.
[Claim 4]
A luminescent characteristic appraisal method of the fluorescent substance according to claim 1, wherein said hollow optical fiber is the hollow optical fiber which formed an aluminum thin film in an inner surface of a glass capillary

[Translation done.]

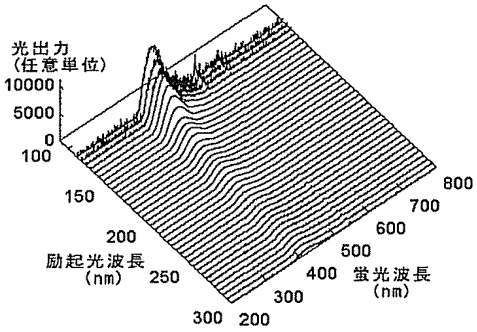
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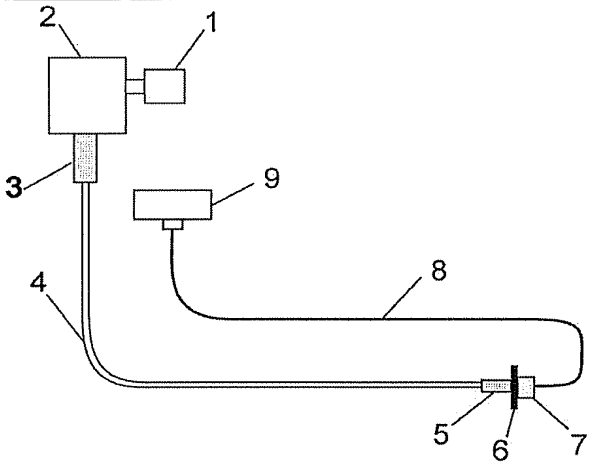
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DRAWINGS

[Drawing 2]



[Drawing 1]



[Translation done.]

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(PCT Rule 44.1)

	Date of mailing *(day/month/year)* 04/07/2008 ✓
Applicant's or agent's file reference 931_020 WO	**FOR FURTHER ACTION** See paragraphs 1 and 4 below
International application No. PCT/US2007/078368	International filing date *(day/month/year)* 13/09/2007
Applicant LED LIGHTING FIXTURES, INC.	

1. [x] The applicant is hereby notified that the international search report and the written opinion of the International Searching Authority have been established and are transmitted herewith.

   Filing of amendments and statement under Article 19:
   The applicant is entitled, if he so wishes, to amend the claims of the International Application (see Rule 46):

   When? The time limit for filing such amendments is normally two months from the date of transmittal of the International Search Report.

   Where? Directly to the International Bureau of WIPO, 34 chemin des Colombettes 1211 Geneva 20, Switzerland, Fascimile No.: (41–22) 338.82.70

   For more detailed instructions, see the notes on the accompanying sheet.

2. [ ] The applicant is hereby notified that no international search report will be established and that the declaration under Article 17(2)(a) to that effect and the written opinion of the International Searching Authority are transmitted herewith.

3. [ ] **With regard to the protest** against payment of (an) additional fee(s) under Rule 40.2, the applicant is notified that:

   [ ] the protest together with the decision thereon has been transmitted to the International Bureau together with the applicant's request to forward the texts of both the protest and the decision thereon to the designated Offices.

   [ ] no decision has been made yet on the protest; the applicant will be notified as soon as a decision is made.

4. **Reminders**

   Shortly after the expiration of **18 months** from the priority date, the international application will be published by the International Bureau. If the applicant wishes to avoid or postpone publication, a notice of withdrawal of the international application, or of the priority claim, must reach the International Bureau as provided in Rules 90*bis*.1 and 90*bis*.3, respectively, before the completion of the technical preparations for international publication.

   The applicant may submit comments on an informal basis on the written opinion of the International Searching Authority to the International Bureau. The International Bureau will send a copy of such comments to all designated Offices unless an international preliminary examination report has been or is to be established. These comments would also be made available to the public but not before the expiration of 30 months from the priority date.

   Within **19 months** from the priority date, but only in respect of some designated Offices, a demand for international preliminary examination must be filed if the applicant wishes to postpone the entry into the national phase **until 30 months** from the priority date (in some Offices even later); otherwise, the applicant must, **within 20 months** from the priority date, perform the prescribed acts for entry into the national phase before those designated Offices.

   In respect of other designated Offices, the time limit of **30 months** (or later) will apply even if no demand is filed within 19 months.

   See the Annex to Form PCT/IB/301 and, for details about the applicable time limits, Office by Office, see the *PCT Applicant's Guide*, Volume II, National Chapters and the WIPO Internet site.

Name and mailing address of the International Searching Authority	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL–2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Iveta Bujanská

NOTES TO FORM PCT/ISA/220

These Notes are intended to give the basic instructions concerning the filing of amendments under article 19. The Notes are based on the requirements of the Patent Cooperation Treaty, the Regulations and the Administrative Instructions under that Treaty. In case of discrepancy between these Notes and those requirements, the latter are applicable. For more detailed information, see also the *PCT Applicant's Guide*, a publication of WIPO.

In these Notes, "Article", "Rule", and "Section" refer to the provisions of the PCT, the PCT Regulations and the PCT Administrative Instructions, respectively.

INSTRUCTIONS CONCERNING AMENDMENTS UNDER ARTICLE 19

The applicant has, after having received the international search report and the written opinion of the International Searching Authority, one opportunity to amend the claims of the international application. It should however be emphasized that, since all parts of the international application (claims,description and drawings) may be amended during the international preliminary examination procedure, there is usually no need to file amendments of the claims under Article 19 except where, e.g. the applicant wants the latter to be published for the purposes of provisional protection or has another reason for amending the claims before international publication. Furthermore, it should be emphasized that provisional protection is available in some States only (see *PCT Applicant's Guide*, Volume I/A, Annexes B1 and B2).

The attention of the applicant is drawn to the fact that amendments to the claims under Article 19 are not allowed where the International Searching Authority has declared, under Article 17(2), that no international search report would be established (see *PCT Applicant's Guide*, Volume I/A, paragraph 296).

What parts of the international application may be amended?

Under Article 19, only the claims may be amended.

During the international phase, the claims may also be amended (or further amended) under Article 34 before the International Preliminary Examining Authority. The description and drawings may only be amended under Article 34 before the International Examining Authority.

Upon entry into the national phase, all parts of the international application may be amended under Article 28 or, where applicable, Article 41.

When?

Within 2 months from the date of transmittal of the international search report or 16 months from the priority date, whichever time limit expires later. It should be noted, however, that the amendments will be considered as having been received on time if they are received by the International Bureau after the expiration of the applicable time limit but before the completion of the technical preparations for international publication (Rule 46.1).

Where not to file the amendments?

The amendments may only be filed with the International Bureau and not with the receiving Office or the International Searching Authority (Rule 46.2).

Where a demand for international preliminary examination has been/is filed, see below.

How?

Either by cancelling one or more entire claims, by adding one or more new claims or by amending the text of one or more of the claims as filed.

A replacement sheet must be submitted for each sheet of the claims which, on account of an amendment or amendments, differs from the sheet originally filed.

All the claims appearing on a replacement sheet must be numbered in Arabic numerals. Where a claim is cancelled, no renumbering of the other claims is required. In all cases where claims are renumbered, they must be renumbered consecutively (Section 205(b)).

The amendments must be made in the language in which the international application is to be published.

What documents must/may accompany the amendments?

Letter (Section 205(b)):

The amendments must be submitted with a letter.

The letter will not be published with the international application and the amended claims. It should not be confused with the "Statement under Article 19(1)" (see below, under "Statement under Article 19(1)").

The letter must be in English or French, at the choice of the applicant. However, if the language of the international application is English, the letter must be in English; if the language of the international application is French, the letter must be in French.

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PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference	**FOR FURTHER ACTION**	see Form PCT/ISA/220 as well as, where applicable, item 5 below.
931_020 WO		
International application No.	International filing date *(day/month/year)*	(Earliest) Priority Date *(day/month/year)*
PCT/US2007/078368	13/09/2007	13/09/2006
Applicant		
LED LIGHTING FIXTURES, INC.		

This international search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This international search report consists of a total of 5 sheets.

☐ It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**
   a. With regard to the **language,** the international search was carried out on the basis of:
      ☒ the international application in the language in which it was filed
      ☐ a translation of the international application into _____, which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b))
   b. ☐ This international search report has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43.6*bis*(a)).
   c. ☐ With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, see Box No. I.

2. ☐ **Certain claims were found unsearchable** (See Box No. II)

3. ☒ **Unity of invention is lacking** (see Box No III)

4. With regard to the **title,**
   ☒ the text is approved as submitted by the applicant
   ☐ the text has been established by this Authority to read as follows:

5. With regard to the **abstract,**
   ☒ the text is approved as submitted by the applicant
   ☐ the text has been established, according to Rule 38.2(b), by this Authority as it appears in Box No. IV. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority

6. With regard to the **drawings,**
   a. the figure of the **drawings** to be published with the abstract is Figure No. 3
      ☒ as suggested by the applicant
      ☐ as selected by this Authority, because the applicant failed to suggest a figure
      ☐ as selected by this Authority, because this figure better characterizes the invention
   b. ☐ none of the figures is to be published with the abstract

Petitioner Hisense USA Corporation
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INTERNATIONAL SEARCH REPORT

International application No
PCT/US2007/078368

A. CLASSIFICATION OF SUBJECT MATTER
INV. H02M3/335

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H02M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	US 5 973 483 A (JO SANG-SOO [KR]) 26 October 1999 (1999-10-26) column 1, line 25 - column 2, line 10 figure 1	1,8,9, 22,23 2-6,9-22
Y X	JP 10 233669 A (MATSUSHITA ELECTRIC WORKS LTD) 2 September 1998 (1998-09-02) abstract	2-6,9-22 7
Y X	GB 2 249 840 A (HESSAMI ALIREZA GHAZI HESSAMI ALIREZA GHAZI [GB]) 20 May 1992 (1992-05-20) abstract figure 2	2-6,9-22 7

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
21 January 2008	04/07/2008

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Roider, Anton

1

Form PCT/ISA/210 (second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2007/078368

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers allsearchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search reportcovers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

1-6, 8-23

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

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FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-6,8-23

power converter constituted by a flyback converter and a boost converter sharing a common inductor

---

2. claim: 7

MOSFET current switching circuit for controlling current flowing through LEDs

---

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2007/078368

Patent document cited in search report		Publication date	Patent family member(s)	Publication date
US 5973483	A	26-10-1999	NONE	
JP 10233669	A	02-09-1998	NONE	
GB 2249840	A	20-05-1992	NONE	

Petitioner Hisense USA Corporation
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PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To:

see form PCT/ISA/220

PCT

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY
(PCT Rule 43*bis*.1)

Date of mailing
(day/month/year) see form PCT/ISA/210 (second sheet)

Applicant's or agent's file reference
see form PCT/ISA/220

FOR FURTHER ACTION
See paragraph 2 below

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US2007/078368	13.09.2007	13.09.2006

International Patent Classification (IPC) or both national classification and IPC
INV. H02M3/335

Applicant
LED LIGHTING FIXTURES, INC.

1. This opinion contains indications relating to the following items:

- ☒ Box No. I Basis of the opinion
- ☐ Box No. II Priority
- ☐ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- ☒ Box No. IV Lack of unity of invention
- ☒ Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- ☐ Box No. VI Certain documents cited
- ☐ Box No. VII Certain defects in the international application
- ☐ Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will usually be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notifed the International Bureau under Rule 66.1*bis*(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/220.

3. For further details, see notes to Form PCT/ISA/220.

Name and mailing address of the ISA:	Date of completion of this opinion	Authorized Officer
European Patent Office D-80298 Munich Tel. +49 89 2399 - 0 Tx: 523656 epmu d Fax: +49 89 2399 - 4465	see form PCT/ISA/210	Roider, Anton Telephone No. +49 89 2399-2330

Petitioner Hisense USA Corporation
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Box No. I Basis of the opinion

1. With regard to the **language**, this opinion has been established on the basis of:

   ☒ the international application in the language in which it was filed

   ☐ a translation of the international application into , which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1 (b)).

2. ☐ This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43bis.1(a))

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application and necessary to the claimed invention, this opinion has been established on the basis of:

   a. type of material:

      ☐ a sequence listing

      ☐ table(s) related to the sequence listing

   b. format of material:

      ☐ on paper

      ☐ in electronic form

   c. time of filing/furnishing:

      ☐ contained in the international application as filed.

      ☐ filed together with the international application in electronic form.

      ☐ furnished subsequently to this Authority for the purposes of search.

4. ☐ In addition, in the case that more than one version or copy of a sequence listing and/or table relating thereto has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

5. Additional comments:

Petitioner Hisense USA Corporation
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Box No. IV Lack of unity of invention

1. ☒ In response to the invitation (Form PCT/ISA/206) to pay additional fees, the applicant has, within the applicable time limit:

   ☐ paid additional fees

   ☐ paid additional fees under protest and, where applicable, the protest fee

   ☐ paid additional fees under protest but the applicable protest fee was not paid

   ☒ not paid additional fees

2. ☐ This Authority found that the requirement of unity of invention is not complied with and chose not to invite the applicant to pay additional fees.

3. This Authority considers that the requirement of unity of invention in accordance with Rule 13.1, 13.2 and 13.3 is

   ☐ complied with

   ☒ not complied with for the following reasons:

   see separate sheet

4. Consequently, this report has been established in respect of the following parts of the international application:

   ☐ all parts.

   ☒ the parts relating to claims Nos. 1-6, 8-23

Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes:	Claims	2-6, 9-21
	No:	Claims	1, 8, 22, 23
Inventive step (IS)	Yes:	Claims	
	No:	Claims	1-23
Industrial applicability (IA)	Yes:	Claims	1-23
	No:	Claims	

2. Citations and explanations

see separate sheet

Re Item IV Reasoned statement with regard to lack of unity of invention

1. This Authority considers that there are two inventions covered by the claims indicated as follows:

   I: Claims 1-6 and 8-23: power converter constituted by a flyback converter and a boost converter sharing a common inductor

   II: Claim 7: MOSFET current switching circuit for controlling current flowing through LEDs

2.1 As pointed out below independent claims 1, 8, 22 and 23 (Invention I) are not new in view of document US5973483 (D1). Thus, as regards the first invention there are no special technical features [Rule 13.2 PCT] to be identified with respect to D1. It remains to be stated that the two Invention are different to such an extent that they are not so linked as to form a single general inventive concept.

2.2 The application, hence does not meet the requirements of unity of invention as defined in Rules 13.1 and 13.2 PCT.

Re Item V Reasoned statement with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

3. Reference is made to the following documents:
   D1: US5973483
   D2: JP10233669
   D3: GB22498

4. The present application does not meet the criteria of Article 33(1) PCT, because the subject-matter of claims 1, 8, 22 and 23 is not new in the sense of Article 33(2) PCT.

4.1 The document D1 discloses (the references in parentheses applying to this document) a power supply (Figure 1) comprising a boost converter (Lp,D2,Q1,R2)

and a flyback converter (Lp,Ls,Q1,R2,D1) wherein the primary winding of the flyback transformer (T1) is the inductance of the boost converter. A diode (D2), a capacitor (C2) and a load (not shown) to be connected to the output voltage terminal (Vout) form the first and second "sub circuits" in the sense of claim 8. The third "sub circuit" is constituted by a diode (D1), a capacitor (C1) and a load (10). Hence, D1 discloses all the features of claim 8 and thus all the features of (the less detailed) claims 1, 22 and 23 which all therefore lack novelty in view of D1.

5. Dependent claims 2 to 6 and 9 to 21 do not contain any features which, in combination with claim 1 meet the requirements of the PCT in respect of novelty and inventive step because the resulting subject-matter is obvious from the combination of D1 with documents D2 and D3.

6. Contrary to the requirements of Rule 5.1(a)(ii) PCT, the relevant background art disclosed in the document D1 is not mentioned in the description, nor are this document identified therein.

6.1 The features of the claims are not provided with reference signs placed in parentheses (Rule 6.2(b) PCT).

Possible steps after receipt of the international search report (ISR) and written opinion of the International Searching Authority (WO-ISA)

General information	For all international applications filed on or after 01/01/2004 the competent ISA will establish an ISR. It is accompanied by the WO-ISA. Unlike the former written opinion of the IPEA (Rule 66.2 PCT), the WO-ISA is not meant to be responded to, but to be taken into consideration for further procedural steps. This document explains about the possibilities.
Amending claims under Art. 19 PCT	Within 2 months after the date of mailing of the ISR and the WO-ISA the applicant may file amended claims under Art. 19 PCT directly with the International Bureau of WIPO. The PCT reform of 2004 did not change this procedure. For further information please see Rule 46 PCT as well as form PCT/ISA/220 and the corresponding Notes to form PCT/ISA/220.
Filing a demand for international preliminary examination	In principle, the WO-ISA will be considered as the written opinion of the IPEA. This should, in many cases, make it unnecessary to file a demand for international preliminary examination. If the applicant nevertheless wishes to file a demand this must be done before expiry of 3 months after the date of mailing of the ISR/WO-ISA or 22 months after priority date, whichever expires later (Rule 54bis PCT). Amendments under Art. 34 PCT can be filed with the IPEA as before, normally at the same time as filing the demand (Rule 66.1 (b) PCT). If a demand for international preliminary examination is filed and no comments/amendments have been received the WO-ISA will be transformed by the IPEA into an IPRP (International Preliminary Report on Patentability) which would merely reflect the content of the WO-ISA. The demand can still be withdrawn (Art. 37 PCT).
Filing informal comments	After receipt of the ISR/WO-ISA the applicant may file informal comments on the WO-ISA directly with the International Bureau of WIPO. These will be communicated to the designated Offices together with the IPRP (International Preliminary Report on Patentability) at 30 months from the priority date. Please also refer to the next box.
End of the international phase	At the end of the international phase the International Bureau of WIPO will transform the WO-ISA or, if a demand was filed, the written opinion of the IPEA into the IPRP, which will then be transmitted together with possible informal comments to the designated Offices. The IPRP replaces the former IPER (international preliminary examination report).
Relevant PCT Rules and more information	Rule 43 PCT, Rule 43bis PCT, Rule 44 PCT, Rule 44bis PCT, PCT Newsletter 12/2003, OJ 11/2003, OJ 12/2003

BNSDOCID: <XS_____200704010CK_I_>

PATENT COOPERATION TREATY

From the INTERNATIONAL SEARCHING AUTHORITY

To: Kevin C. Brown
Burr & Brown
P.O. Box 7068
Syracuse, NY 13261

FEB 25 2003

PCT

NOTIFICATION OF TRANSMITTAL OF THE INTERNATIONAL SEARCH REPORT AND THE WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY, OR THE DECLARATION

(PCT Rule 44.1)

Applicant's or agent's file reference 931_018 WO	Date of mailing *(day/month/year)* **FOR FURTHER ACTION** See paragraphs 1 and 4 below
International application No. PCT/US 07/12708	International filing date *(day/month/year)* 30 May 2007 (30.05.2007)
Applicant LED Lighting Fixtures, Inc.	

1. ☒ The applicant is hereby notified that the international search report and the written opinion of the International Searching Authority have been established and are transmitted herewith.

Filing of amendments and statement under Article 19:
The applicant is entitled, if he so wishes, to amend the claims of the international application (see Rule 46):

When? The time limit for filing such amendments is normally two months from the date of transmittal of the international search report.

Where? Directly to the International Bureau of WIPO, 34 chemin des Colombettes 1211 Geneva 20, Switzerland, Facsimile No.: +41 22 740 14 35

For more detailed instructions, see the notes on the accompanying sheet.

2. ☐ The applicant is hereby notified that no international search report will be established and that the declaration under Article 17(2)(a) to that effect and the written opinion of the International Searching Authority are transmitted herewith.

3. ☐ **With regard to the protest** against payment of (an) additional fee(s) under Rule 40.2, the applicant is notified that:

☐ the protest together with the decision thereon has been transmitted to the International Bureau together with the applicant's request to forward the texts of both the protest and the decision thereon to the designated Offices.

☐ no decision has been made yet on the protest; the applicant will be notified as soon as a decision is made.

4. **Reminders**

Shortly after the expiration of **18 months** from the priority date, the international application will be published by the International Bureau. If the applicant wishes to avoid or postpone publication, a notice of withdrawal of the international application, or of the priority claim, must reach the International Bureau as provided in Rules 90*bis*.1 and 90*bis*.3, respectively, before the completion of the technical preparations for international publication.

The applicant may submit comments on an informal basis on the written opinion of the International Searching Authority to the International Bureau. The International Bureau will send a copy of such comments to all designated Offices unless an international preliminary examination report has been or is to be established. These comments would also be made available to the public but not before the expiration of 30 months from the priority date.

Within **19 months** from the priority date, but only in respect of some designated Offices, a demand for international preliminary examination must be filed if the applicant wishes to postpone the entry into the national phase **until 30 months** from the priority date (in some Offices even later); otherwise, the applicant must, **within 20 months** from the priority date, perform the prescribed acts for entry into the national phase before those designated Offices.

In respect of other designated Offices, the time limit of **30 months** (or later) will apply even if no demand is filed within 19 months.

See the Annex to Form PCT/IB/301 and, for details about the applicable time limits, Office by Office, see the *PCT Applicant's Guide*, Volume II, National Chapters and the WIPO Internet site.

Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer: Lee W. Young PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/220 (January 2004) *(See notes on accompanying sheet)*

Petitioner Hisense USA Corporation
Exhibit 1004 - Page 191 of 373

PATENT COOPERATION TREATY

From the INTERNATIONAL SEARCHING AUTHORITY

To: Kevin C. Brown
Burr & Brown
P.O. Box 7068
Syracuse, NY 13261

PCT

NOTIFICATION OF TRANSMITTAL OF THE INTERNATIONAL SEARCH REPORT AND THE WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY, OR THE DECLARATION

(PCT Rule 44.1)

	Date of mailing *(day/month/year)* 20 FEB 2008
Applicant's or agent's file reference 931_018 WO	**FOR FURTHER ACTION** See paragraphs 1 and 4 below
International application No. PCT/US 07/12708	International filing date *(day/month/year)* 30 May 2007 (30.05.2007)
Applicant LED Lighting Fixtures, Inc.	

1. ☒ The applicant is hereby notified that the international search report and the written opinion of the International Searching Authority have been established and are transmitted herewith.

Filing of amendments and statement under Article 19:
The applicant is entitled, if he so wishes, to amend the claims of the international application (see Rule 46):

When? The time limit for filing such amendments is normally two months from the date of transmittal of the international search report.

Where? Directly to the International Bureau of WIPO, 34 chemin des Colombettes 1211 Geneva 20, Switzerland, Facsimile No.: +41 22 740 14 35

For more detailed instructions, see the notes on the accompanying sheet.

2. ☐ The applicant is hereby notified that no international search report will be established and that the declaration under Article 17(2)(a) to that effect and the written opinion of the International Searching Authority are transmitted herewith.

3. ☐ **With regard to the protest** against payment of (an) additional fee(s) under Rule 40.2, the applicant is notified that:

☐ the protest together with the decision thereon has been transmitted to the International Bureau together with the applicant's request to forward the texts of both the protest and the decision thereon to the designated Offices

☐ no decision has been made yet on the protest; the applicant will be notified as soon as a decision is made.

4. **Reminders**

Shortly after the expiration of **18 months** from the priority date, the international application will be published by the International Bureau. If the applicant wishes to avoid or postpone publication, a notice of withdrawal of the international application, or of the priority claim, must reach the International Bureau as provided in Rules 90*bis*.1 and 90*bis*.3, respectively, before the completion of the technical preparations for international publication.

The applicant may submit comments on an informal basis on the written opinion of the International Searching Authority to the International Bureau. The International Bureau will send a copy of such comments to all designated Offices unless an international preliminary examination report has been or is to be established. These comments would also be made available to the public but not before the expiration of 30 months from the priority date.

Within **19 months** from the priority date, but only in respect of some designated Offices, a demand for international preliminary examination must be filed if the applicant wishes to postpone the entry into the national phase **until 30 months** from the priority date (in some Offices even later); otherwise, the applicant must, **within 20 months** from the priority date, perform the prescribed acts for entry into the national phase before those designated Offices.

In respect of other designated Offices, the time limit of **30 months** (or later) will apply even if no demand is filed within 19 months.

See the Annex to Form PCT/IB/301 and, for details about the applicable time limits, Office by Office, see the *PCT Applicant's Guide*, Volume II, National Chapters and the WIPO Internet site.

Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer: Lee W. Young PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/220 (January 2004) *(See notes on accompanying sheet)*

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference 931_018 WO	**FOR FURTHER ACTION**	see Form PCT/ISA/220 as well as, where applicable, item 5 below.
International application No. PCT/US 07/12708	International filing date *(day/month/year)* 30 May 2007 (30.05.2007)	(Earliest) Priority Date *(day/month/year)* 31 May 2006 (31.05.2006)
Applicant LED Lighting Fixtures, Inc.		

This international search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This international search report consists of a total of 2 sheets

☐ It is also accompanied by a copy of each prior art document cited in this report

1. **Basis of the report**

a. With regard to the **language**, the international search was carried out on the basis of:

☒ the international application in the language in which it was filed.

☐ a translation of the international application into _____ which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b)).

b ☐ This international search report has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43.6*bis*(a)).

c. ☐ With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, see Box No. I.

2. ☐ **Certain claims were found unsearchable** (see Box No. II).

3. ☐ **Unity of invention is lacking** (see Box No. III).

4. With regard to the **title**,

☒ the text is approved as submitted by the applicant.

☐ the text has been established by this Authority to read as follows:

5. With regard to the **abstract**,

☒ the text is approved as submitted by the applicant.

☐ the text has been established, according to Rule 38.2(b), by this Authority as it appears in Box No. IV. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.

6. With regard to the **drawings**,

a. the figure of the **drawings** to be published with the abstract is Figure No. 4

☒ as suggested by the applicant.

☐ as selected by this Authority, because the applicant failed to suggest a figure.

☐ as selected by this Authority, because this figure better characterizes the invention.

b. ☐ none of the figures is to be published with the abstract.

Petitioner Hisense USA Corporation
Exhibit 1004 - Page 193 of 373

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 07/12708

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - H01S 3/13 (2007.10)
USPC - 372/29.014
According to International Patent Classification (IPC) or to both national classification and IPC

B FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC(8): H01S 3/13 (2007.10)
USPC: 372/29.014

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
IPC(8): H01S 3/13 (2007.10)
USPC: 257/88; 362/552, 555, 612; 372/29.014

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
PubWEST(USPT,PGPB,EPAB,JPAB); Internet search via Google Web and Google Scholar search engines. Search Terms Used: white current regulator 1931 1976 CIE color coordinate MacAdam LED OLED light emitter emitting semiconductor

C DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X --- Y	US 6,630,801 B2 (SCHUURMANS) 07 October 2003 (07.10.2003) col. 3 ln. 3 to col. 6, ln. 56, claim 1, 4, 6-9, 13, 19, 20, 21, 23, 26, Fig. 1, 2	1-7, 10, 11, 22-24 and 26 --- 8, 9 and 25
X --- Y	US 2003/0011559 A1 (ADACHI) 16 January 2003 (16.01.2003) para. [0051]-[0087], Fig. 3-5, 7-9	12-19, 21, 27-30 and 32 --- 8, 20 and 31
Y	US 6,329,758 B1 (SALAM) 11 December 2001 (11.12.2001) col. 13 ln. 6-14, col. 13 ln. 28-51	9, 20, 25 and 31
A	US 7,014,336 B1 (DUCHARME et al.) 21 March 2006 (21.03.2006) col. 4 ln. 40-53, col. 6 ln. 44-57, col. 13 ln. 34 to col. 14 ln. 40, col. 17 ln. 18-49, col. 27 ln. 8-25, Fig. 6, 14, 23	1-32
A	US 6,552,495 B1 (CHANG) 22 April 2003 (22.04.2003) col. 3 ln. 27 to col. 7 ln. 20, Fig. 1, 2, 5, 6	1-32

☐ Further documents are listed in the continuation of Box C. ☐

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
20 November 2007 (20.11.2007)	20 FEB 2008
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer: Lee W. Young PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/210 (second sheet) (April 2007)

PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To: Kevin C. Brown
Burr & Brown
P.O. Box 7068
Syracuse, NY 13261

PCT

WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43*bis*.1)

	Date of mailing *(day/month/year)* 20 FEB 2008
Applicant's or agent's file reference 931_018 WO	**FOR FURTHER ACTION** See paragraph 2 below

International application No	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US 07/12708	30 May 2007 (30.05.2007)	31 May 2006 (31.05.2006)

International Patent Classification (IPC) or both national classification and IPC
IPC(8) - H01S 3/13 (2007.10)
USPC - 372/29.014

Applicant LED Lighting Fixtures, Inc.

1 This opinion contains indications relating to the following items:

- ☒ Box No. I Basis of the opinion
- ☐ Box No. II Priority
- ☐ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- ☐ Box No. IV Lack of unity of invention
- ☒ Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- ☐ Box No. VI Certain documents cited
- ☐ Box No. VII Certain defects in the international application
- ☐ Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1*bis*(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/220.

3. For further details, see notes to Form PCT/ISA/220.

Name and mailing address of the ISA/US	Date of completion of this opinion	Authorized officer:
Mail Stop PCT, Attn: ISA/US Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	20 November 2007 (20.11.2007)	Lee W. Young PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/237 (cover sheet) (April 2007)

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US 07/12708

Box No. I Basis of this opinion

1. With regard to the **language**, this opinion has been established on the basis of:

☒ the international application in the language in which it was filed.

☐ a translation of the international application into _____ which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b)).

2. ☐ This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43*bis*.1(a))

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, this opinion has been established on the basis of:

a. type of material

☐ a sequence listing

☐ table(s) related to the sequence listing

b. format of material

☐ on paper

☐ in electronic form

c. time of filing/furnishing

☐ contained in the international application as filed

☐ filed together with the international application in electronic form

☐ furnished subsequently to this Authority for the purposes of search

4. ☐ In addition, in the case that more than one version or copy of a sequence listing and/or table(s) relating thereto has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

5. Additional comments:

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WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US 07/12708

Box No. V **Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement**

1 Statement

Novelty (N)	Claims	8, 9, 13, 16, 20, 25, 28, 31	YES
	Claims	1-7, 10-12, 14, 15, 17-19, 21-24, 26, 27, 29, 30, 32	NO
Inventive step (IS)	Claims	none	YES
	Claims	1-32	NO
Industrial applicability (IA)	Claims	1-32	YES
	Claims	none	NO

2 Citations and explanations:
Claims 1-7, 10, 11, 22, 23, 24 and 26 lack novelty under PCT Article 33(2) as being anticipated by US 6,630,801 B2 (Schuurmans).

Regarding claim 1, Schuurmans discloses a lighting device (RGB based LED luminary 10, col. 2 ln. 63-65, col. 3 ln. 56-63, Fig. 1) comprising a first group of solid state light emitters (red LED light sources 11R, col. 3 ln. 64 to col. 4 ln. 9, Fig. 1), the first group of solid state light emitters comprising at least one first group solid state light emitter; a second group of solid state light emitters (green LED light sources 11G, col. 3 ln. 64 to col. 4 ln. 9, Fig. 1) the second group of solid state light emitters comprising at least one second group solid state light emitter; a first current regulator (red LED driver 14R, Fig. 1) and a second current regulator (green LED driver 14G, Fig. 1) the first current regulator being switchable among at least two first current regulator settings (forward currents based on control voltage Vcr-ref, col. 4 ln. 11-25; control voltage Vcr-ref based on analysis of feedback signals, col. 4 ln. 59 to col. 5 ln. 11) the at least two first current regulator settings comprising a first current regulator first setting (forward current based on control voltage Vcr-ref, col. 4 ln. 11-25) and a first current regulator second setting (current based on control voltage Vcr-ref based on analysis of feedback signals, col. 4 ln. 59 to col. 5 ln. 11), the second current regulator being switchable among at least two second current regulator settings (forward currents based on control voltage Vcg-ref, col. 4 ln. 11-25; and control voltage Vcg-ref based on analysis of feedback signals, col. 4 ln. 59 to col. 5 ln. 11), the at least two second current regulator settings comprising a second current regulator first setting (forward current based on control voltage Vcg-ref, col. 4 ln. 11-25) and a second current regulator second setting (current based on control voltage Vcg-ref based on analysis of feedback signals, col. 4 ln. 59 to col. 5 ln. 11; off, col. 5 ln. 56 to col. 6 ln. 2) such that: (1) if the lighting device is energized and the first current regulator is in the first current regulator first setting, a first group first current (forward current based on control voltage Vcr-ref, col. 4 ln. 11-25) would be supplied to the first group solid state light emitter; (2) if the lighting device is energized and the first current regulator is in the first current regulator second setting, a first group second current (current based on control voltage Vcr-ref based on analysis of feedback signals, col. 4 ln. 59 to col. 5 ln. 11) would be supplied to the first group solid state light emitter; (3) if the lighting device is energized and the second current regulator is in the second current regulator first setting, a second group first current (forward current based on control voltage Vcg-ref, col. 4 ln. 11-25) would be supplied to the second group solid state light emitter; and (4) if the lighting device is energized and the second current regulator is in the second current regulator second setting, a second group second current (current based on control voltage Vcg-ref based on analysis of feedback signals, col. 4 ln. 59 to col. 5 ln. 11) would be supplied to the second group solid state light emitter; the first group first current differing from the second group first current (col. 4 ln. 43-56) the first group second current differing from the second group second current (col. 4 ln. 57 to col. 5 ln. 11).

Regarding claim 2, Schuurmans discloses a lighting device (RGB based LED luminary 10, col. 2 ln. 63-65, col. 3 ln. 56-63, Fig. 1) wherein if the first group first current (forward current based on control voltage Vcr-ref, col. 4 ln. 11-25) is supplied to each of the first group of solid state light emitters (red LED light sources 11R, col. 3 ln. 64 to col. 4 ln. 9, Fig. 1) and the second group first current (forward current based on control voltage Vcg-ref, col. 4 ln. 11-25) is supplied to each of the second group of solid state light emitters (green LED light sources 11G, col. 3 ln. 64 to col. 4 ln. 9, Fig. 1), a combined intensity of the first group of solid state light emitters is a first group first intensity (luminous efficacy for the red LED sources 11R, col. 6 ln. 3-14, claim 9) and a combined intensity of the second group of solid state light emitters is a second group first intensity (luminous efficacy for the green LED sources 11G, col. 6 ln. 3-14, claim 9), if the first group second current is supplied to each of the first group of solid state light emitters and the second group second current is supplied to each of the second group of solid state light emitters, a combined intensity of the first group of solid state light emitters (output signals via filtered photodiode 21R, col. 4 ln. 26-56, col. 6 ln. 3-14) is a first group second intensity and a combined intensity of the second group of solid state light emitters (output signals via filtered photodiode 21G, col. 4 ln. 26-56, col. 6 ln. 3-14) is a second group second intensity, and a ratio of the first group first intensity to the second group first intensity differs by not more than 5 % from a ratio of the first group second intensity to the second group second intensity (luminous efficacy of each LED light sources 11R, 11G, 11B is controllable over the entire luminous spectrum by the user, col. 6 ln. 16-36, through user interface 31 of controller 30, col. 4 ln. 26 to col. 5 ln. 11).

Regarding claim 3, Schuurmans discloses a lighting device (RGB based LED luminary 10, col. 2 ln. 63-65, col. 3 ln. 56-63, Fig. 1) wherein if the first group first current (forward current based on control voltage Vcr-ref, col. 4 ln. 11-25) is supplied to each of the first group of solid state light emitters (red LED light sources 11R, col. 3 ln. 64 to col. 4 ln. 9, Fig. 1) and the second group first current (forward current based on control voltage Vcg-ref, col. 4 ln. 11-25) is supplied to each of the second group of solid state light emitters (green LED light sources 11G, col. 3 ln. 64 to col. 4 ln. 9, Fig. 1), a combined illumination from the first group of solid state light emitters and the second group of solid state light emitters would be perceived as white (col. 3 ln. 56 to col. 5 ln. 11) and if the first group second current (current based on control voltage Vcr-ref based on analysis of feedback signals, col. 4 ln. 59 to col. 5 ln. 11) is supplied to each of the first group of solid state light emitters and the second group second current (current based on control voltage Vcg-ref based on analysis of feedback signals, col. 4 ln. 59 to col. 5 ln. 11) is supplied to each of the second group of solid state light emitters, combined illumination from the first group of solid state light emitters and the second group of solid state light emitters would also be perceived as white (col. 3 ln. 56 to col. 5 ln. 11).
---See Continuation Sheet---

Petitioner Hisense USA Corporation
Exhibit 1004 - Page 197 of 373

Supplemental Box

In case **the space in any of the preceding boxes is not sufficient.**
Continuation of:
Box V, item 2, Citations and explanations:

Regarding claim 4, Schuurmans discloses a light emitting device (RGB based LED luminary 10, col. 2 ln. 63-65, col. 3 ln. 56-63, Fig. 1), wherein if the first group first current (forward current based on control voltage Vcr-ref, col. 4 ln. 11-25) is supplied to each of the first group of solid state light emitters (red LED light sources 11R, col. 3 ln. 64 to col. 4 ln. 9, Fig. 1) and the second group first current (forward current based on control voltage Vcg-ref, col. 4 ln. 11-25) is supplied to each of the second group of solid state light emitters (green LED light sources 11G, col. 3 ln. 64 to col. 4 ln. 9, Fig. 1), a combined illumination from the first group of solid state light emitters and the second group of solid state light emitters corresponds to a first point on a 1976 CIE diagram (1931 CIE coordinates (x,y) can be transformed via equations: u.= 4x/(-2x+12y+3), v.= 9y/(-2x+12y+3) to the 1976 CIE coordinates (u,v), col. 3 ln. 3-14, claim 4, 21), the first point having a first correlated color temperature (col. 1 ln. 66 to col. 2 ln. 8, correlated color temperature identifies a color temperature of a color near, but not on, the Planckian locus), if the first group second current (current based on control voltage Vcr-ref based on analysis of feedback signals, col. 4 ln. 59 to col. 5 ln. 11) is supplied to each of the first group of solid state light emitters and the second group second current (current based on control voltage Vcg-ref based on analysis of feedback signals, col. 4 ln. 59 to col. 5 ln. 11) is supplied to each of the second group of solid state light emitters, a combined illumination from the first group of solid state light emitters and the second group of solid state light emitters corresponds to a second point on the 1976 CIE diagram (1931 CIE coordinates (x,y) can be transformed via equations: u = 4x/(-2x+12y+3), v = 9y/(-2x+12y+3) to the 1976 CIE coordinates (u,v), col. 3 ln. 3-14, claim 4, 21), the second point having a second correlated color temperature (col. 1 ln. 66 to col. 2 ln. 8), the first correlated color temperature differing from the second correlated color temperature by not more than 4 MacAdam ellipses (color coordinates of each of the LED light sources 11R, 11G, 11B is controllable over the entire CIE chromaticity diagram by the user, col. 6 ln. 16-36, through user interface 31 of controller 30, col. 1 ln. 8-15, col. 2 ln. 12-25, col. 4 ln. 26 to col. 5 ln. 11, claims 1, 6-9, 13, 19, 20, 23, 26; if each color is perceived as being the same, then by definition they lie within a single MacAdam ellipse).

Regarding claim 5, Schuurmans discloses a light emitting device (RGB based LED luminary 10, col. 2 ln. 63-65, col. 3 ln. 56-63, Fig. 1), wherein if the first group first current (forward current based on control voltage Vcr-ref, col. 4 ln. 11-25) is supplied to each of the first group of solid state light emitters (red LED light sources 11R, col. 3 ln. 64 to col. 4 ln. 9, Fig. 1) and the second group first current (forward current based on control voltage Vcg-ref, col. 4 ln. 11-25) is supplied to each of the second group of solid state light emitters (green LED light sources 11G, col. 3 ln. 64 to col. 4 ln. 9, Fig. 1), a combined illumination from the first group of solid state light emitters and the second group of solid state light emitters corresponds to a first point on a 1976 CIE diagram having coordinates u', v' (1931 CIE coordinates (x,y) can be transformed via equations: u.= 4x/(-2x+12y+3), v.= 9y/(-2x+12y+3) to the 1976 CIE coordinates (u,v), col. 3 ln. 3-14, claim 4, 21), if the first group second current (current based on control voltage Vcr-ref based on analysis of feedback signals, col. 4 ln. 59 to col. 5 ln. 11) is supplied to each of the first group of solid state light emitters and the second group second current (current based on control voltage Vcg-ref based on analysis of feedback signals, col. 4 ln. 59 to col. 5 ln. 11) is supplied to each of the second group of solid state light emitters, a combined illumination from the first group of solid state light emitters and the second group of solid state light emitters corresponds to a second point on the 1976 CIE diagram having coordinates u', v', and the first point is spaced from the second point by a distance such that delta u', v' is not more than 0.005 on the 1976 CIE diagram (color coordinates of each LED light sources 11R, 11G, 11B is controllable over the entire CIE chromaticity diagram by the user, col. 6 ln. 16-36, through user interface 31 of controller 30, col. 1 ln. 8-15, col. 2 ln. 12-25, col. 4 ln. 26 to col. 5 ln. 11, claims 1, 6-9, 13, 19, 20, 23, 26).

Regarding claim 6, Schuurmans discloses a light emitting device (RGB based LED luminary 10, col. 2 ln. 63-65, col. 3 ln. 56-63, Fig. 1), further comprising a third group of solid state light emitters (blue LED light sources 11B, col. 3 ln. 64 to col. 4 ln. 9, Fig. 1), the third group of solid state light emitters comprising at least one third group solid state light emitter; and a third current regulator (blue LED driver 14B, Fig. 1) the third current regulator being switchable among at least two third current regulator settings (forward currents based on control voltage Vcb-ref, col. 4 ln. 11-25; and control voltage Vcb-ref based on analysis of feedback signals, col. 4 ln. 59 to col. 5 ln. 11), the at least two third current regulator settings comprising a third current regulator first setting (forward currents based on control voltage Vcb-ref, col. 4 ln. 11-25) and a third current regulator second setting (current based on control voltage Vcb-ref based on analysis of feedback signals, col. 4 ln. 59 to col. 5 ln. 11) such that: (5) if the lighting device is energized and the third current regulator is in the third current regulator first setting, a third group first current (forward current based on control voltage Vcb-ref) would be supplied to the third group solid state light emitter; and (6) if the lighting device is energized and the third current regulator is in the third current regulator second setting, a third group second current (current based on control voltage Vcb-ref based on analysis of feedback signals) would be supplied to the third group solid state light emitter; the third group first current differing from the first group first current (col. 4 ln. 43-56) and differing from the second group first current, and the third group second current differing from the first group second current and differing from the second group second current (col. 3 ln. 38-55, col. 4 ln. 57 to col. 5 ln. 11, claim 9, 23, 26).

---See Continuation Sheet---

Petitioner Hisense USA Corporation
Exhibit 1004 - Page 198 of 373

Supplemental Box

In case **the space in any of the preceding boxes is not sufficient.**
Continuation of:
Box V, item 2. Citations and explanations:

Regarding claim 7, Schuurmans discloses a light emitting device (RGB based LED luminary 10, col. 2 ln. 63-65, col. 3 ln. 56-63, Fig. 1) the first current regulator (red LED driver 14R, Fig. 1) is switchable among at least three first current regulator settings (red LED driver 14R can be operated over a continuous range of values, col. 5 ln. 4-11) the at least three first current regulator settings comprising the first current regulator first setting, the first current regulator second setting, and a first current regulator third setting (off, not illustrated, col. 5 ln. 56 to col. 6 ln. 2); and the second current regulator is switchable among at least three second current regulator settings (green LED driver 14G can be operated over a continuous range of values, col. 5 ln. 4-11), the at least three second current regulator settings comprising the second current regulator first setting (forward currents based on control voltage Vcg-ref, col. 4 ln. 11-25), the second current regulator second setting (off, col. 5 ln. 56 to col. 6 ln. 2) and a second current regulator third setting (current based on control voltage Vcg-ref based on analysis of feedback signals, col. 4 ln. 59 to col. 5 ln. 11); such that: (5) if the lighting device is energized and the first current regulator is in the first current regulator third setting, a first group third current (off, col. 5 ln. 56 to col. 6 ln. 2) would be supplied to the first group solid state light emitter; and (6) if the lighting device is energized and the second current regulator is in the second current regulator third setting, a second group third current (current based on control voltage Vcg-ref based on analysis of feedback signals, col. 4 ln. 59 to col. 5 ln. 11) would be supplied to the second group solid state light emitter; the first group third current differing from the second group third current. (The output of each of the red, blue and green LEDs are measured independently, e.g.: when the red LED is measured the green and blue LEDs are momentarily turned off. See: col. 5 ln. 48 to col. 6 ln. 2.)

Regarding claim 10, Schuurmans discloses a light emitting device (RGB based LED luminary 10, col. 2 ln. 63-65, col. 3 ln. 56-63, Fig. 1), wherein the first group first current (forward current based on control voltage Vcr-ref, col. 4 ln. 11-25) differs from the first group second current (current based on control voltage Vcr-ref based on analysis of feedback signals, col. 4 ln. 59 to col. 5 ln. 11), differs from the second group first current (forward current based on control voltage Vcg-ref, col. 4 ln. 11-25), and differs from the second group second current (current based on control voltage Vcg-ref based on analysis of feedback signals, col. 4 ln. 59 to col. 5 ln. 11), and the second group first current (forward current based on control voltage Vcg-ref, col. 4 ln. 11-25) differs from the first group first current (forward current based on control voltage Vcr-ref, col. 4 ln. 11-25), differs from the first group second current (current based on control voltage Vcr-ref based on analysis of feedback signals, col. 4 ln. 59 to col. 5 ln. 11), and differs from the second group second current (current based on control voltage Vcg-ref based on analysis of feedback signals, col. 4 ln. 59 to col. 5 ln. 11). (The output of each of the red, blue and green LEDs are measured independently, e.g.: when the red LED is measured the green and blue LEDs are momentarily turned off. See: col. 5 ln. 48 to col. 6 ln. 2; also, luminous efficacy of each LED light sources 11R, 11G, 11B is controllable over the entire luminous spectrum by the user, col. 6 ln. 16-36, through user interface 31 of controller 30, col. 4 ln. 26 to col. 5 ln. 11.)

Regarding claim 11, Schuurmans discloses a light emitting device (RGB based LED luminary 10, col. 2 ln. 63-65, col. 3 ln. 56-63, Fig. 1) wherein (1) if the lighting device is energized and the first current regulator (red LED driver 14R, Fig. 1) is in the first current regulator first setting (forward currents based on control voltage Vcr-ref, col. 4 ln. 11-25), the first group first current (forward current based on control voltage Vcr-ref, col. 4 ln. 11-25) would be supplied to each of the first group solid state light emitters; (2) if the lighting device is energized and the first current regulator (red LED driver 14R, Fig. 1) is in the first current regulator second setting (current based on control voltage Vcr-ref based on analysis of feedback signals, col. 4 ln. 59 to col. 5 ln. 11), the first group second current would be supplied to each of the first group solid state light emitters; (3) if the lighting device is energized and the second current regulator (green LED driver 14G, Fig. 1) is in the second current regulator first setting (forward currents based on control voltage Vcg-ref, col. 4 ln. 11-25), the second group first current would be supplied to each of the second group solid state light emitters; and (4) if the lighting device is energized and the second current regulator (green LED driver 14G, Fig. 1) is in the second current regulator second setting (currents based on control voltage Vcg-ref based on analysis of feedback signals, col. 4 ln. 59 to col. 5 ln. 11; off col. 5 ln. 56 to col. 6 ln. 2), the second group second current would be supplied to each of the second group solid state light emitters.

Regarding claim 22, Schuurmans discloses a method of lighting (RGB based LED luminary 10, col. 2 ln. 63-65, col. 3 ln. 56-63, Fig. 1), comprising: substantially simultaneously: (a) adjusting a current (via red LED driver 14R, Fig. 1) supplied to a first group of solid state light emitters (red LED light sources 11R, col. 3 ln. 64 to col. 4 ln. 9, Fig. 1) from a first group first current (forward currents based on control voltage Vcr-ref, col. 4 ln. 11-25) to a first group second current (current based on control voltage Vcr-ref based on analysis of feedback signals, col. 4 ln. 59 to col. 5 ln. 11); and (b) adjusting a current (via green LED driver 14G, Fig. 1) supplied to a second group of solid state light emitters (green LED light sources 11G, col. 3 ln. 64 to col. 4 ln. 9, Fig. 1) from a second group first current (forward current based on control voltage Vcg-ref, col. 4 ln. 11-25) to a second group second current (current based on control voltage Vcg-ref based on analysis of feedback signals, col. 4 ln. 59 to col. 5 ln. 11); the first group of solid state light emitters comprising at least one first group solid state light emitter; the second group of solid state light emitters comprising at least one second group solid state light emitter; the first group first current differing from the second group first current, the first group second current differing from the second group second current (luminous efficacy of each LED light sources 11R, 11G, 11B is controllable over the entire luminous spectrum by the user, col. 6 ln. 16-36, through user interface 31 of controller 30, col. 4 ln. 26 to col. 5 ln. 11).

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Supplemental Box

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Continuation of:
Box V, item 2. Citations and explanations:

Regarding claim 23, Schuurmans discloses a method of lighting (RGB based LED luminary 10, col. 2 ln. 63-65, col. 3 ln. 56-63, Fig. 1), comprising a combined intensity of the first group of solid state light emitters (luminous efficacy for the red LED sources 11R, col. 6 ln. 3-14, claim 9) prior to the adjusting a current supplied to the first group of solid state light emitters is a first group first intensity, a combined intensity of the second group of solid state light emitters (luminous efficacy for the green LED sources 11G, col. 6 ln. 3-14, claim 9) prior to the adjusting a current supplied to the second group of solid state light emitters is a second group first intensity, a combined intensity of the first group of solid state light emitters after the adjusting a current supplied to the first group of solid state light emitters is a first group second intensity (output signals via filtered photodiode 21R, col. 4 ln. 26-56, col. 6 ln. 3-14), a combined intensity of the second group of solid state light emitters after the adjusting a current supplied to the second group of solid state light emitters is a second group second intensity (output signals via filtered photodiode 21G, col. 4 ln. 26-56, col. 6 ln. 3-14), and a ratio of the first group first intensity to the second group first intensity differs by not more than 5 % from a ratio of the first group second intensity to the second group second intensity (luminous efficacy of each LED light sources 11R, 11G, 11B is controllable over the entire luminous spectrum by the user, col. 6 ln. 16-36, through user interface 31 of controller 30, col. 4 ln. 26 to col. 5 ln. 11).

Regarding claim 24, Schuurmans discloses a method of lighting (RGB based LED luminary 10, col. 2 ln. 63-65, col. 3 ln. 56-63, Fig. 1), wherein a combined illumination from the first group of solid state light emitters (red LED light sources 11R, col. 3 ln. 64 to col. 4 ln. 9, Fig 1) and the second group of solid state light emitters (green LED light sources 11G, col. 3 ln. 64 to col. 4 ln. 9, Fig. 1) prior to the adjusting a current (forward currents based on control voltages Vcr-ref, Vcg-ref, col. 4 ln. 11-25) supplied to the first group of solid state light emitters corresponds to a first point on a 1976 CIE diagram which has coordinates u', v', (1931 CIE coordinates (x,y) can be transformed via equations: u.= 4x/(-2x+12y+3), v.= 9y/(-2x+12y+3) to the 1976 CIE coordinates (u,v), col. 3 ln. 3-14, claim 4, 21) a combined illumination from the first group of solid state light emitters and the second group of solid state light emitters after the adjusting a current (currents based on control voltages Vcr-ref, Vcg-ref based on analysis of feedback signals, col. 4 ln. 59 to col. 5 ln. 11) supplied to the first group of solid state light emitters corresponds to a second point on the 1976 CIE diagram which has coordinates u', v', and the first point is spaced from the second point by a distance such that delta u', v' is not more than 0.005 on the 1976 CIE diagram (color coordinates of each LED light sources 11R, 11G, 11B is controllable over the entire CIE chromaticity diagram by the user, col. 6 ln. 16-36, through user interface 31 of controller 30, col. 1 ln. 8-15, col. 2 ln. 12-25, col. 4 ln. 26 to col. 5 ln. 11, claims 1, 6-9, 13, 19, 20, 23, 26).

Regarding claim 26, Schuurmans discloses a method of lighting (RGB based LED luminary 10, col. 2 ln. 63-65, col. 3 ln. 56-63, Fig. 1) wherein the first group first current (forward current based on control voltage Vcr-ref, col. 4 ln. 11-25) differs from the first group second current (current based on control voltage Vcr-ref based on analysis of feedback signals, col. 4 ln. 59 to col. 5 ln. 11), differs from the second group first current (forward current based on control voltage Vcg-ref, col. 4 ln. 11-25), and differs from the second group second current (current based on control voltage Vcg-ref based on analysis of feedback signals, col. 4 ln. 59 to col. 5 ln. 11), and the second group first current (forward current based on control voltage Vcg-ref, col. 4 ln. 11-25) differs from the first group first current (forward current based on control voltage Vcr-ref, col. 4 ln. 11-25), differs from the first group second current (current based on control voltage Vcr-ref based on analysis of feedback signals, col. 4 ln. 59 to col. 5 ln. 11), and differs from the second group second current (current based on control voltage Vcg-ref based on analysis of feedback signals, col. 4 ln. 59 to col. 5 ln. 11). (The output of each of the red, blue and green LEDs are measured independently, e.g.: when the red LED is measured the green and blue LEDs are momentarily turned off See: col. 5 ln. 48 to col. 6 ln. 2; also, luminous efficacy of each LED light sources 11R, 11G, 11B is controllable over the entire luminous spectrum by the user, col. 6 ln. 16-36, through user interface 31 of controller 30, col. 4 ln. 26 to col. 5 ln. 11.)

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Supplemental Box

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Box V, item 2. Citations and explanations:

Claims 12, 14, 15, 17-19, 21, 27, 29, 30 and 32 lack novelty under PCT Article 33(2) as being anticipated by US 2003/0011559 A1 (Adachi).

Regarding claim 12, Adachi discloses a lighting device (lighting device Fig. 8, para. [0072] through [0082], Fig. 8, 9), comprising: a first group of solid state light emitters (red LEDs 16a) the first group of solid state light emitters comprising at least one first group solid state light emitter (red LED 16a, para [0057]); a second group of solid state light emitters (green LEDs 16b), the second group of solid state light emitters comprising at least one second group solid state light emitter (green LED 16b, para [0057]); a first current regulator (red light emission control switch 24a); and a second current regulator (green light emission control switch 24b); the first current regulator being switchable among at least two first current regulator settings (eight settings are disclosed among ON and OFF states of three transistors 241, 242, 243 of red light emission control switch 24a, Fig. 9) the at least two first current regulator settings comprising a first current regulator first setting and a first current regulator second setting; the second current regulator being switchable among at least two second current regulator settings (eight settings are disclosed among ON and OFF states of three transistors 241, 242, 243 of green light emission control switch 24b), the at least two second current regulator settings comprising a second current regulator first setting and a second current regulator second setting; such that: (1) if the lighting device is energized and the first current regulator is in the first current regulator first setting (any one of the possible eight states of transistors 241, 242, 243 in either ON or OFF state), a first group first current would be supplied to the first group solid state light emitter; (2) if the lighting device is energized and the first current regulator is in the first current regulator second setting (any one of possible eight states of transistors 241, 242, 243 in either ON or OFF state, possibly distinct from first current regulator first setting), a first group second current would be supplied to the first group solid state light emitter; (3) if the lighting device is energized and the second current regulator is in the second current regulator first setting (any one of possible eight states of transistors 241, 242, 243 in either ON or OFF state, possibly distinct from second or first current regulator first setting), a second group first current would be supplied to the second group solid state light emitter; and (4) if the lighting device is energized and the second current regulator is in the second current regulator second setting, a second group second current would be supplied to the second group solid state light emitter; (see para. [0075] through [0077]) a first group second setting / first setting ratio being defined as the first group second current divided by the first group first current, a second group second setting / first setting ratio being defined as the second group second current divided by the second group first current, the first group second setting / first setting ratio differing from the second group second setting / first setting ratio by at least 5 % (if all three red current regulator transistors 241-243 were in the OFF state for the first group second setting, while all of the three red current regulator transistors were in the ON state for the first group first setting, while one of the green current regulator transistor 241-243 were in the ON state for the second group second setting and any one of the green current regulator transistors 241-243 were in the ON state for the second group first setting, the ratio would approach unity, para. [0075] through [0079]).

Regarding claim 14, Adachi discloses a lighting device (lighting device Fig. 8, para. [0072] through [0082], Fig. 8, 9) wherein if the first group first current (current supplied based on one of any eight settings disclosed among ON and OFF states of three transistors 241, 242, 243 of red light emission control switch 24a, Fig. 9) is supplied to each of the first group of solid state light emitters (red LEDs 16a) and the second group first current (current based on one of any eight settings disclosed among ON and OFF states of three transistors 241, 242, 243 of green light emission control switch 24b) is supplied to each of the second group of solid state light emitters (green LEDs 16b), a combined illumination from the first group of solid state light emitters and the second group of solid state light emitters would be perceived as white (para. [0021], [0031], [0066], [0087], claim 8, 18), and if the first group second current (current supplied based on one of eight settings are disclosed among ON and OFF states of three transistors 241, 242, 243 of red light emission control switch 24a, Fig. 9, distinct from first group first current setting) is supplied to each of the first group of solid state light emitters and the second group second current (current supplied based on one of eight settings are disclosed among ON and OFF states of three transistors 241, 242, 243 of green light emission control switch 24b, distinct from second group first current) is supplied to each of the second group of solid state light emitters, a combined illumination from the first group of solid state light emitters and the second group of solid state light emitters would also be perceived as white (para. [0021], [0031], [0066], [0087], claim 8, 18).

Regarding claim 15, Adachi discloses a lighting device (lighting device Fig. 8, para. [0072] through [0082], Fig. 8, 9) wherein if the first group first current (current supplied based on one of any eight settings disclosed among ON and OFF states of three transistors 241, 242, 243 of red light emission control switch 24a, Fig. 9) is supplied to each of the first group of solid state light emitters (red LEDs 16a) and the second group first current (current supplied based on one of any eight settings disclosed among ON and OFF states of three transistors 241, 242, 243 of green light emission control switch 24b) is supplied to each of the second group of solid state light emitters (green LEDs 16b), a combined illumination from the first group of solid state light emitters and the second group of solid state light emitters corresponds to a first point on a 1976 CIE diagram (para. [0066]) the first point having a first correlated color temperature, if the first group second current (current supplied based on one of any eight settings disclosed among ON and OFF states of three transistors 241, 242, 243 of red light emission control switch 24a, Fig. 9, possibly distinct from first group first current) is supplied to each of the first group of solid state light emitters and the second group second current (current supplied based on one of any eight settings disclosed among ON and OFF states of three transistors 241, 242, 243 of green light emission control switch 24b, possibly distinct from second group first current) is supplied to each of the second group of solid state light emitters, a combined illumination from the first group of solid state light emitters and the second group of solid state light emitters corresponds to a second point on the 1976 CIE diagram, the second point having a second correlated color temperature, the first correlated color temperature differing from the second correlated color temperature by not more than 4 MacAdam ellipses (if each color is perceived as being the same, then by definition they lie within a single MacAdam ellipse, para. [0081]).

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Box V, item 2 Citations and explanations:

Regarding claim 17, Adachi discloses a lighting device (lighting device Fig. 8, para. [0072] through [0082], Fig. 8, 9), further comprising a third group of solid state light emitters (blue LEDs 16c, para [0057], Fig. 8), the third group of solid state light emitters comprising at least one third group solid state light emitter (blue LED 16c, para [0057]); and a third current regulator (blue light emission control switch 24c); the third current regulator being switchable among at least two third current regulator settings (eight settings are disclosed among ON and OFF states of three transistors 241, 242, 243 of blue light emission control switch 24c, Fig. 9), the at least two third current regulator settings comprising a third current regulator first setting and a third current regulator second setting; such that: (5) if the lighting device is energized and the third current regulator is in the third current regulator first setting, a third group first current
(current based on one of eight settings disclosed among ON and OFF states of three transistors 241, 242, 243 of blue light emission control switch 24c) would be supplied to the third group solid state light emitter; and (6) if the lighting device is energized and the third current regulator is in the third current regulator second setting, a third group second current (current based on one of eight settings disclosed among ON and OFF states of three transistors 241, 242, 243 of blue light emission control switch 24c, possibly distinct from third group first current) would be supplied to the third group solid state light emitter; a third group second setting / first setting ratio being defined as the third group second current divided by the third group first current, the third group second setting / first setting ratio differing from the first group second setting / first setting ratio by at least 5 %, and differing from the second group second setting / first setting ratio by at least 5 % (if all three red current regulator transistors 241-243 were in the OFF state for the first group second setting, while all of the three red current regulator transistors were in the ON state for the first group first setting, while one of the green current regulator transistor 241-243 were in the ON state for the second group second setting and any one of the green current regulator transistors 241-243 were in the ON state for the second group first setting, and while one of the blue current regulator transistor 241-243 were in the ON state for the third group second setting and any one of the blue current regulator transistors 241-243 were in the ON state for the third group first setting, each first group second setting/first setting ratio and second group second setting/first setting ration ratio would approach unity, para. [0075] through [0079]).

Regarding claim 18, Adachi discloses a lighting device (lighting device Fig. 8, para. [0072] through [0082], Fig. 8, 9), wherein: the first current regulator (red light emission control switch 24a) is switchable among at least three first current regulator settings (eight settings are disclosed among ON and OFF states of three transistors 241, 242, 243 of red light emission control switch 24a, Fig. 9), the at least three first current regulator settings comprising the first current regulator first setting, the first current regulator second setting, and a first current regulator third setting; and the second current regulator (green light emission control switch 24b) is switchable among at least three second current regulator settings (eight settings are disclosed among ON and OFF states of three transistors 241, 242, 243 of green light emission control switch 24b), the at least three second current regulator settings comprising the second current regulator first setting, the second current regulator second setting and a second current regulator third setting; such that:(5) if the lighting device is energized and the first current regulator is in the first current regulator third setting, a first group third current would be supplied to the first group solid state light emitter; and
(6) if the lighting device is energized and the second current regulator is in the second current regulator third setting, a second group third current would be supplied to the second group solid state light emitter; a first group third setting / second setting ratio being defined as the first group third current divided by the first group second current, a second group third setting / second setting ratio being defined as the second group third current divided by the second group second current, the first group third setting / second setting ratio differing from the second group third setting / second setting ratio by at least 5 % (if all three red current regulator transistors 241-243 were in the OFF state for the first group third setting, while all of the three red current regulator transistors were in the ON state for the first group second setting, while one of the green current regulator transistor 241-243 were in the ON state for the second group third setting and any one of the green current regulator transistors 241-243 were in the ON state for the second group second setting, the ratio would approach unity, para. [0075] through [0079]).

Regarding claim 19, Adachi discloses a lighting device (lighting device Fig. 8, para. [0072] through [0082], Fig. 8, 9) comprising a master currents regulator (signal supply unit 5, para. [0055] through [0058], Fig. 8), the master currents regulator being switchable among at least two master currents regulator settings (ON and OFF, para. [0058]), the at least two master currents regulator settings comprising a master currents regulator first setting (ON) and a master currents regulator second setting (OFF), I such that: (1) if the master currents regulator is in the master currents regulator first setting, the first current regulator (red light emission control switch 24a) would be in the first current regulator first position (eight settings are disclosed among ON and OFF states of three transistors 241, 242, 243 of red light emission control switch 24a, Fig. 9) and the second current regulator (green light emission control switch 24b) would be in the second current regulator first position (eight settings are disclosed among ON and OFF states of three transistors 241, 242, 243 of green light emission control switch 24b), and (2) if the master currents regulator is in the master currents regulator second setting (OFF), the first current regulator would be in the first current regulator second position (all transistors 241-243 of red light emission control switch 24a in OFF position) and the second current regulator would be in the second current regulator second position (all transistors 241-243 of green light emission control switch 24b in OFF position).

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Supplemental Box

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Continuation of:
Box V, item 2. Citations and explanations:

Regarding claim 21, Adachi discloses a lighting device (lighting device Fig. 8, para. [0072] through [0082], Fig. 8, 9) wherein (1) if the lighting device is energized and the first current regulator (red light emission control switch 24a) is in the first current regulator first setting (eight settings are disclosed among ON and OFF states of three transistors 241, 242, 243 of red light emission control switch 24a, Fig. 9), the first group first current would be supplied to each of the first group solid state light emitters; (2) if the lighting device is energized and the first current regulator is in the first current regulator second setting (any of the eight settings disclosed among ON and OFF states of three transistors 241, 242, 243 of red light emission control switch 24a, distinct from the first current regulator first setting), the first group second current would be supplied to each of the first group solid state light emitters; (3) if the lighting device is energized and the second current regulator (green light emission control switch 24b) is in the second current regulator first setting (eight settings are disclosed among ON and OFF states of three transistors 241, 242, 243 of green light emission control switch 24b), the second group first current would be supplied to each of the second group solid state light emitters; and (4) if the lighting device is energized and the second current regulator is in the second current regulator second setting (any of the eight settings disclosed among ON and OFF states of three transistors 241, 242, 243 of green light emission control switch 24b, distinct from the second current regulator first setting), the second group second current would be supplied to each of the second group solid state light emitters.

Regarding claim 27, Adachi discloses a method of lighting (via lighting device Fig. 8, para. [0072] through [0082], Fig. 8, 9) comprising substantially simultaneously: (a) adjusting a current (via red light emission control switch 24a, eight settings are disclosed among ON and OFF states of three transistors 241, 242, 243 of red light emission control switch 24a, Fig. 9) supplied to a first group of solid state light emitters (red LEDs 16a) from a first group first current (current based on one of eight settings are disclosed among ON and OFF states of three transistors 241, 242, 243 of red light emission control switch 24a, Fig. 9) to a first group second current (current based on one of eight settings are disclosed among ON and OFF states of three transistors 241, 242, 243 of red light emission control switch 24a, possibly distinct from first group first current); and (b) adjusting a current (via green light emission control switch 24b, eight settings are disclosed among ON and OFF states of three transistors 241, 242, 243 of green light emission control switch 24b, Fig. 9) supplied to a second group of solid state light emitters (green LEDs 16b) from a second group first current (current based on one of eight settings are disclosed among ON and OFF states of three transistors 241, 242, 243 of green light emission control switch 24b) to a second group second current (eight settings are disclosed among ON and OFF states of three transistors 241, 242, 243 of green light emission control switch 24b, possibly distinct from first group first current); the first group of solid state light emitters comprising at least one first group solid state light emitter (red LED 16a, para [0057]); the second group of solid state light emitters comprising at least one second group solid state light emitter (green LED 16b, para [0057]); a first group second setting / first setting ratio being defined as the first group second current divided by the first group first current, a second group second setting / first setting ratio being defined as the second group second current divided by the second group first current, (see para. [0075] through [0077]), the first group second setting / first setting ratio differing from the second group second setting / first setting ratio by at least 5 % (if all three red current regulator transistors 241-243 were in the OFF state for the first group second setting, while all of the three red current regulator transistors were in the ON state for the first group first setting, while one of the green current regulator transistor 241-243 were in the ON state for the second group second setting and any one of the green current regulator transistors 241-243 were in the ON state for the second group first setting, the ratio would approach unity, para. [0075] through [0079]).

Regarding claim 29, Adachi discloses a method of lighting (via lighting device Fig. 8, para. [0072] through [0082], Fig. 8, 9) wherein: a combined illumination (para. [0021], [0031], [0066], [0087], claim 8, 18) from the first group of solid state light emitters (red LEDs 16a) and the second group of solid state light emitters (green LEDs 16b) prior to the adjusting a current supplied to the first group of solid state light emitters (current supplied based on one of any eight settings disclosed among ON and OFF states of three transistors 241, 242, 243 of red light emission control switch 24a, Fig. 9) corresponds to a first point on a 1976 CIE diagram which has coordinates u', v', (measured composite chromaticity point C, para. [0070]), a combined illumination from the first group of solid state light emitters and the second group of solid state light emitters after the adjusting a current supplied to the first group of solid state light emitters corresponds to a second point on the 1976 CIE diagram which has coordinates u', v', (standard chromaticity point S, para. [0071]), yet fails to discloses wherein the first point is spaced from the second point by a distance such that delta u', v' is not more than 0.005 on the 1976 CIE diagram (para. [0071]).

Regarding claim 30, Adachi discloses a method of lighting (via lighting device Fig. 8, para. [0072] through [0082], Fig. 8, 9) wherein the first point has first point u', v' coordinates (measured composite chromaticity point C, para. [0070]) and the second point has second point u', v' coordinates (standard chromaticity point S, para. [0070], [0071]), the second point u', v' coordinates being identical to the first point u', v' coordinates.

Regarding claim 32, Adachi discloses a method of lighting (via lighting device Fig. 8, para. [0072] through [0082], Fig. 8, 9) wherein: the first group first current (current supplied based on one of any eight settings disclosed among ON and OFF states of three transistors 241, 242, 243 of red light emission control switch 24a, para. [0073] through [0076], Fig. 9) differs from the first group second current (current supplied based on one of any eight settings disclosed among ON and OFF states of three transistors 241, 242, 243 of red light emission control switch 24a, Fig. 9), differs from the second group first current (current supplied based on one of any eight settings disclosed among ON and OFF states of three transistors 241, 242, 243 of green light emission control switch 24b, Fig. 9), and differs from the second group second current (current supplied based on one of one of seven remaining settings disclosed among ON and OFF states of three transistors 241, 242, 243 of green light emission control switch 24b, Fig. 9), and the second group first current differs from the first group first current, differs from the first group second current, and differs from the second group second current (para. [0029], [0075], [0077], [0081], [0066], [0090]).

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Box V, item 2. Citations and explanations:

Claim 13, 16 and 28 lack an inventive step under PCT Article 33(3) as being obvious over Adachi.

Regarding claim 13, Adachi discloses a lighting device (lighting device Fig. 8, para. [0072] through [0082], Fig. 8, 9) wherein if the first group first current (one of eight possible settings are disclosed among ON and OFF states of three transistors 241, 242, 243 of red light emission control switch 24a, Fig. 9) is supplied to each of the first group of solid state light emitters (red LEDs 16a) and the second group first current (eight settings are disclosed among ON and OFF states of three transistors 241, 242, 243 of green light emission control switch 24b) is supplied to each of the second group of solid state light emitters (green LEDs 16b), a combined intensity of the first group of solid state light emitters is a first group first intensity (light emission, para. [0062], Fig. 3-5) and a combined intensity of the second group of solid state light emitters is a second group first intensity (light emission, para. [0062], Fig. 3-5), if the first group second current is supplied to each of the first group of solid state light emitters and the second group second current is supplied to each of the second group of solid state light emitters, a combined intensity of the first group of solid state light emitters is a first group second intensity (light emission, para. [0062], Fig. 3-5) and a combined intensity of the second group of solid state light emitters is a second group second intensity (light emission, para. [0062], Fig. 3-5), yet fails to specifically disclose wherein a ratio of the first group first intensity to the second group first intensity differs by not more than 5 % from a ratio of the first group second intensity to the second group second intensity. However, the driving currents and voltages resulting in relative intensities are well known to the industry, it would have been obvious to one of skill in the art without undue experimentation to optimize the ratio of the first group first intensity to the second group first intensity by manipulating the input voltages and currents, so as the ratio of the first group second intensity to the second group second intensity would not differ by more than 5%, para. [0075] through [0079].

Regarding claim 16, Adachi discloses a lighting device (lighting device Fig. 8, para. [0072] through [0082], Fig. 8, 9) wherein if first group first current (current supplied based on one of any eight settings disclosed among ON and OFF states of three transistors 241, 242, 243 of red light emission control switch 24a, Fig. 9) is supplied to each of the first group of solid state light emitters (red LEDs 16a) and the second group first current (current supplied based on one of any eight settings disclosed among ON and OFF states of three transistors 241, 242, 243 of green light emission control switch 24b) is supplied to each of the second group of solid state light emitters (green LEDs 16b), a combined illumination from the first group of solid state light emitters and the second group of solid state light emitters corresponds to a first point on a 1976 CIE diagram having coordinates u', v', if the first group second current (current supplied based on one of any eight settings disclosed among ON and OFF states of three transistors 241, 242, 243 of red light emission control switch 24a, Fig. 9, possibly distinct from first group first current) is supplied to each of the first group of solid state light emitters and the second group second current (current supplied based on one of any eight settings disclosed among ON and OFF states of three transistors 241, 242, 243 of green light emission control switch 24b, possibly distinct from second group first current) is supplied to each of the second group of solid state light emitters, a combined illumination from the first group of solid state light emitters and the second group of solid state light emitters corresponds to a second point on the 1976 CIE diagram having coordinates u', v', yet fails to disclose a light device wherein the first point is spaced from the second point by a distance such that delta u', v' is not more than 0.005 on the 1976 CIE diagram. Adachi further discloses manipulating the power used for two colors other than the low-efficiency color is reduced, wherein each of the distances traveled by the chromaticity points of red and green is calculated based on the distance between the measured composite chromaticity point C and a standard chromaticity point S at the color temperature of 6500 degrees (white light), and the light emission time of LED of each of red and green is determined on the basis of the relation between the distance traveled and the light emission time; when determining the relation between the distance traveled and the light emission time, it is desirable to take it into account that there are some cases where the relative light emission intensity is significantly reduced if the light emission time is shortened (para. [0070]). However, the driving currents and voltages resulting in relative intensities are well known to the industry, it would have been obvious to one of skill in the art without undue experimentation to manipulate the first group first current, the first group second current, the second group first current and the second group second current to realize two distinct points on the 1976 CIE diagram having distinct coordinates, such that the first point is spaced from the second point by a distance such that delta u', v' is not more than 0.005 on the 1976 CIE diagram, para. [0075] through [0079].

---See Continuation Sheet---

Petitioner Hisense USA Corporation
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Supplemental Box

In case **the space in any of the preceding boxes is not sufficient.**
Continuation of:
Box V, item 2. Citations and explanations:

Regarding claim 28, Adachi discloses a method of lighting (via lighting device Fig. 8, para. [0072] through [0082], Fig. 8, 9) wherein a combined intensity of the first group of solid state light emitters (red LEDs 16a) prior to the adjusting a current (current based on one of eight possible settings among ON and OFF states of three transistors 241, 242, 243 of red light emission control switch 24a, Fig. 9) supplied to the first group of solid state light emitters is a first group first intensity (light emission, para. [0062], Fig. 3-5), a combined intensity of the second group of solid state light emitters (green LEDs 16b) prior to the adjusting a current (current based on one of eight settings among ON and OFF states of three transistors 241, 242, 243 of green light emission control switch 24b) supplied to the second group of solid state light emitters is a second group first intensity (light emission, para. [0062], Fig. 3-5), a combined intensity of the first group of solid state light emitters after the adjusting a current supplied to the first group of solid state light emitters is a first group second intensity (intensity based on current based on one of eight possible settings among ON and OFF states of three transistors 241, 242, 243 of red light emission control switch 24a, Fig. 9), a combined intensity of the second group of solid state light emitters after the adjusting a current supplied to the second group of solid state light emitters is a second group second intensity (intensity based on current based on one of eight settings among ON and OFF states of three transistors 241, 242, 243 of green light emission control switch 24b), yet fails to disclose a ratio of the first group first intensity to the second group first intensity differs by not more than 5 % from a ratio of the first group second intensity to the second group second intensity. However, the driving currents and voltages resulting in relative intensities are well known to the industry, it would have been obvious to one of skill in the art without undue experimentation to optimize the ratio of the first group first intensity to the second group first intensity to differ by not more than 5% from a ratio of the first group second intensity to the second group second intensity (para. [0075] through [0079]).

Claim 8 lacks an inventive step under PCT Article 33(3) as being obvious over Schuurmans in view of Adachi.

Regarding claim 8, Schuurmans discloses a light emitting device (RGB based LED luminary 10, col. 2 ln. 63-65, col. 3 ln. 56-63, Fig. 1), further comprising a master currents regulator (controller 30, col. 4 ln. 43 to col. 5 ln. 25) the master currents regulator being switchable among at least two master currents regulator settings (switchable among multiple voltages for each LED driver 14R, 14B, 14G, based on user input, including ON and OFF for each LED driver, or any forward current based on control voltages Vcr-ref, Vcg-ref, Vcb-ref and currents based on feedback signals), yet specifically fails to disclose wherein the at least two master currents regulator settings comprising a master currents regulator first setting and a master currents regulator second setting, such that: (1) if the master currents regulator is in the master currents regulator first setting, the first current regulator would be in the first current regulator first position and the second current regulator would be in the second current regulator first position, and (2) if the master currents regulator is in the master currents regulator second setting, the first current regulator would be in the first current regulator second position and the second current regulator would be in the second current regulator second position. Adachi discloses a liquid crystal display device comprising a master current regulator (signal supply unit 5, Fig. 8) and individual red, green and blue LED drivers (light emission control switches 24a, 24b, 24c, para. [0073] through [0079], [0084], Fig. 8) wherein at least two master currents regulator settings comprising a master currents regulator first setting (ON, para. [0054] through [0058]) and a master currents regulator second setting (OFF, para. [0055] through [0058]) such that: (1) if the master currents regulator is in the master currents regulator first setting, the first current regulator would be in the first current regulator first position (ON, para. [0058]) and the second current regulator would be in the second current regulator first position (ON, para. [0058]), and (2) if the master currents regulator is in the master currents regulator second setting, the first current regulator would be in the first current regulator second position (OFF, para. [0058]) and the second current regulator would be in the second current regulator second position (OFF, para. [0058]). Since both references are directed toward driving multiple LEDs, it would have been obvious to one of skill in the art to combine the light emitting device (RGB based LED luminary 10) of Schuurmans with the driving characteristics of Adachi, to construct a lighting device further comprising a master currents regulator, the master currents regulator being switchable among at least two master currents regulator settings, the at least two master currents regulator settings comprising a master currents regulator first setting and a master currents regulator second setting, such that: (1) if the master currents regulator is in the master currents regulator first setting, the first current regulator would be in the first current regulator first position and the second current regulator would be in the second current regulator first position, and (2) if the master currents regulator is in the master currents regulator second setting, the first current regulator would be in the first current regulator second position and the second current regulator would be in the second current regulator second position, since such a combination would result in a combination with greater control over the resultant color chromaticity.

---See Continuation Sheet---

Petitioner Hisense USA Corporation
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WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US 07/12708

Supplemental Box

In case **the space in any of the preceding boxes is not sufficient.**
Continuation of:
Box V, item 2. Citations and explanations:

Claims 9 and 25 lack an inventive step under PCT Article 33(3) as being obvious over Schuurmans in view of US 6,329,758 B1 (Salam).

Regarding claim 9, Schuurmans discloses a light emitting device (RGB based LED luminary 10, col. 2 ln. 63-65, col. 3 ln. 56-63, Fig. 1) comprising first group solid state light emitters (red LED light sources 11R, col. 3 ln. 64 to col. 4 ln. 9, Fig. 1) and second group solid state light emitters (green LED light sources 11G, col. 3 ln. 64 to col. 4 ln. 9, Fig. 1), yet fails to discloses wherein each of the first group solid state light emitters has a dominant wavelength within 20 nanometers of a first group wavelength; and each of the second group solid state light emitters has a dominant wavelength within 20 nanometers of a second group wavelength. Salam discloses an LED lamp 81 (col. 13 ln. 6-14, Fig. 8) comprising first and second sets of LED lamps (red LED 81 and green LEDs 80, 82, 83) wherein each of the first group solid state light emitters has a dominant wavelength within 20 nanometers of a first group wavelength (col. 13 ln. 28-51); and each of the second group solid state light emitters has a dominant wavelength within 20 nanometers of a second group wavelength (col. 13 ln. 28-51), for color matching. Since both references are directed toward LED lighting, it would have been obvious to one of skill in the art to combine the light emitting device (RGB based LED luminary 10) of Schuurmans with the first group and second group solid state light emitters (red LED 81 and green LEDs 80, 82, 83) of Salam, to construct a light emitting device wherein each of the first group solid state light emitters has a dominant wavelength within 20 nanometers of a first group wavelength; and each of the second group solid state light emitters has a dominant wavelength within 20 nanometers of a second group wavelength, since such a combination would result in a lighting device with improved color matching.

Regarding claim 25, Schuurmans discloses a method of lighting (RGB based LED luminary 10, col. 2 ln. 63-65, col. 3 ln. 56-63, Fig. 1), comprising first group solid state light emitters (red LED light sources 11R, col. 3 ln. 64 to col. 4 ln. 9, Fig. 1) and second group solid state light emitters (green LED light sources 11G, col. 3 ln. 64 to col. 4 ln. 9, Fig. 1), yet fails to disclose a method wherein each of the first group solid state light emitters has a dominant wavelength within 20 nanometers of a first group wavelength; and each of the second group solid state light emitters has a dominant wavelength within 20 nanometers of a second group wavelength. Salam discloses an LED lamp 81 (col. 13 ln. 6-14, Fig. 8) comprising first and second sets of LED lamps (red LED 81 and green LEDs 80, 82, 83) wherein each of the first group solid state light emitters has a dominant wavelength within 20 nanometers of a first group wavelength (col. 13 ln. 28-51); and each of the second group solid state light emitters has a dominant wavelength within 20 nanometers of a second group wavelength (col. 13 ln. 28-51), for color matching. Since both references are directed toward LED lighting, it would have been obvious to one of skill in the art to combine the lighting device (lighting device Fig. 8) of Adachi with the first group and second group solid state light emitters (red LED 81 and green LEDs 80, 82, 83) of Salam, to construct a light emitting device wherein each of the first group solid state light emitters has a dominant wavelength within 20 nanometers of a first group wavelength; and each of the second group solid state light emitters has a dominant wavelength within 20 nanometers of a second group wavelength, since such a combination would result in a lighting device with improved color matching.

Claims 20 and 31 lack an inventive step under PCT Article 33(3) as being obvious over Adachi in view of Salam.

Regarding claim 20, Adachi discloses a lighting device (lighting device Fig. 8, para. [0072] through [0082], Fig. 8, 9) comprising a first group solid state light emitters (red LEDs 16a); and a second group solid state light emitters (green LEDs 16b), yet fails to disclose wherein each of the first group solid state light emitters has a dominant wavelength within 20 nanometers of a first group wavelength; and each of the second group solid state light emitters has a dominant wavelength within 20 nanometers of a second group wavelength. Salam discloses an LED lamp 81 (col. 13 ln. 6-14, Fig. 8) comprising first and second sets of LED lamps (red LED 81 and green LEDs 80, 82, 83) wherein each of the first group solid state light emitters has a dominant wavelength within 20 nanometers of a first group wavelength (col. 13 ln. 28-51); and each of the second group solid state light emitters has a dominant wavelength within 20 nanometers of a second group wavelength (col. 13 ln. 28-51), for color matching. Since both references are directed toward LED lighting, it would have been obvious to one of skill in the art to combine the lighting device (lighting device Fig. 8) of Adachi with the first group and second group solid state light emitters (red LED 81 and green LEDs 80, 82, 83) of Salam, to construct a light emitting device wherein each of the first group solid state light emitters has a dominant wavelength within 20 nanometers of a first group wavelength; and each of the second group solid state light emitters has a dominant wavelength within 20 nanometers of a second group wavelength, since such a combination would result in a lighting device with improved color matching.

Regarding claim 31, Adachi discloses a method of lighting (via lighting device Fig. 8, para. [0072] through [0082], Fig. 8, 9) comprising a first group solid state light emitters (red LEDs 16a); and a second group solid state light emitters (green LEDs 16b), yet fails to disclose a method wherein each of the first group solid state light emitters has a dominant wavelength within 20 nanometers of a first group wavelength; and each of the second group solid state light emitters has a dominant wavelength within 20 nanometers of a second group wavelength. Salam discloses an LED lamp 81 (col. 13 ln. 6-14, Fig. 8) comprising first and second sets of LED lamps (red LED 81 and green LEDs 80, 82, 83) wherein each of the first group solid state light emitters has a dominant wavelength within 20 nanometers of a first group wavelength (col. 13 ln. 28-51); and each of the second group solid state light emitters has a dominant wavelength within 20 nanometers of a second group wavelength (col. 13 ln. 28-51), for color matching. Since both references are directed toward LED lighting, it would have been obvious to one of skill in the art to combine the lighting device (lighting device Fig. 8) of Adachi with the first group and second group solid state light emitters (red LED 81 and green LEDs 80, 82, 83) of Salam, to construct a light emitting device wherein each of the first group solid state light emitters has a dominant wavelength within 20 nanometers of a first group wavelength; and each of the second group solid state light emitters has a dominant wavelength within 20 nanometers of a second group wavelength, since such a combination would result in a lighting device with improved color matching.

Claims 1-32 have industrial applicability as defined by PCT Article 33(4) because the subject matter can be made or used by industry.

Petitioner Hisense USA Corporation
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NOTES TO FORM PCT/ISA/220

These Notes are intended to give the basic instructions concerning the filing of amendments under Article 19. The Notes are based on the requirements of the Patent Cooperation Treaty, the Regulations and the Administrative Instructions under that Treaty. In case of discrepancy between these Notes and those requirements, the latter are applicable. For more detailed information, see also the *PCT Applicant's Guide*, a publication of WIPO.

In these Notes, "Article," "Rule" and "Section" refer to the provisions of the PCT, the PCT Regulations and the PCT Administrative Instructions, respectively.

INSTRUCTIONS CONCERNING AMENDMENTS UNDER ARTICLE 19

The applicant has, after having received the international search report and the written opinion of the International Searching Authority, one opportunity to amend the claims of the international application. It should however be emphasized that, since all parts of the international application (claims, description and drawings) may be amended during the international preliminary examination procedure, there is usually no need to file amendments of the claims under Article 19 except where, e.g. the applicant wants the latter to be published for the purposes of provisional protection or has another reason for amending the claims before international publication. Furthermore, it should be emphasized that provisional protection is available in some States only (see *PCT Applicant's Guide*, Volume I/A, Annexes B1 and B2).

The attention of the applicant is drawn to the fact that amendments to the claims under Article 19 are not allowed where the International Searching Authority has declared, under Article 17(2), that no international search report would be established (see *PCT Applicant's Guide*, Volume I/A, paragraph 296).

What parts of the international application may be amended ?

Under Article 19, only the claims may be amended.

During the international phase, the claims may also be amended (or further amended) under Article 34 before the International Preliminary Examining Authority. The description and drawings may only be amended under Article 34 before the International Preliminary Examining Authority.

Upon entry into the national phase, all parts of the international application may be amended under Article 28 or, where applicable, Article 41.

When ? Within 2 months from the date of transmittal of the international search report or 16 months from the priority date, whichever time limit expires later. It should be noted, however, that the amendments will be considered as having been received on time if they are received by the International Bureau after the expiration of the applicable time limit but before the completion of the technical preparations for international publication (Rule 46.1).

Where not to file the amendments ?

The amendments may only be filed with the International Bureau and not with the receiving Office or the International Searching Authority (Rule 46.2).

Where a demand for international preliminary examination has been/is filed, see below.

How ? Either by cancelling one or more entire claims, by adding one or more new claims or by amending the text of one or more of the claims as filed.

A replacement sheet must be submitted for each sheet of the claims which, on account of an amendment or amendments, differs from the sheet originally filed.

All the claims appearing on a replacement sheet must be numbered in Arabic numerals. Where a claim is cancelled, no renumbering of the other claims is required. In all cases where claims are renumbered, they must be renumbered consecutively (Section 205(b)).

The amendments must be made in the language in which the international application is to be published.

What documents must/may accompany the amendments ?

Letter (Section 205(b)):

The amendments must be submitted with a letter.

The letter will not be published with the international application and the amended claims. It should not be confused with the "Statement under Article 19(1)" (see below, under "Statement under Article 19(1)").

The letter must be in English or French, at the choice of the applicant. However, if the language of the international application is English, the letter must be in English; if the language of the international application is French, the letter must be in French.

Petitioner Hisense USA Corporation
Exhibit 1004 - Page 207 of 373

NOTES TO FORM PCT/ISA/220 (continued)

The letter must indicate the differences between the claims as filed and the claims as amended. It must, in particular, indicate, in connection with each claim appearing in the international application (it being understood that identical indications concerning several claims may be grouped), whether

(i) the claim is unchanged;

(ii) the claim is cancelled;

(iii) the claim is new;

(iv) the claim replaces one or more claims as filed;

(v) the claim is the result of the division of a claim as filed.

The following examples illustrate the manner in which amendments must be explained in the accompanying letter:

1 [Where originally there were 48 claims and after amendment of some claims there are 51]:
"Claims 1 to 29, 31, 32, 34, 35, 37 to 48 replaced by amended claims bearing the same numbers, claims 30, 33 and 36 unchanged; new claims 49 to 51 added."

2 [Where originally there were 15 claims and after amendment of all claims there are 11]:
"Claims 1 to 15 replaced by amended claims 1 to 11."

3 [Where originally there were 14 claims and the amendments consist in cancelling some claims and in adding new claims]:
"Claims 1 to 6 and 14 unchanged; claims 7 to 13 cancelled; new claims 15, 16 and 17 added." or
"Claims 7 to 13 cancelled; new claims 15, 16 and 17 added; all other claims unchanged."

4 [Where various kinds of amendments are made]:
"Claims 1-10 unchanged; claims 11 to 13, 18 and 19 cancelled; claims 14, 15 and 16 replaced by amended claim 14; claim 17 subdivided into amended claims 15, 16 and 17; new claims 20 and 21 added."

"Statement under Article 19(1)" (Rule 46.4)

The amendments may be accompanied by a statement explaining the amendments and indicating any impact that such amendments might have on the description and the drawings (which cannot be amended under Article 19(1)).

The statement will be published with the international application and the amended claims.

It must be in the language in which the international application is to be published.

It must be brief, not exceeding 500 words if in English or if translated into English.

It should not be confused with and does not replace the letter indicating the differences between the claims as filed and as amended. It must be filed on a separate sheet and must be identified as such by a heading, preferably by using the words "Statement under Article 19(1)."

It may not contain any disparaging comments on the international search report or the relevance of citations contained in that report. Reference to citations, relevant to a given claim, contained in the international search report may be made only in connection with an amendment of that claim.

Consequence if a demand for international preliminary examination has already been filed

If, at the time of filing any amendments and any accompanying statement, under Article 19, a demand for international preliminary examination has already been submitted, the applicant must preferably, at the time of filing the amendments (and any statement) with the International Bureau, also file with the International Preliminary Examining Authority a copy of such amendments (and of any statement) and, where required, a translation of such amendments for the procedure before that Authority (see Rules 55.3(a) and 62.2, first sentence). For further information, see the Notes to the demand form (PCT/IPEA/401).

If a demand for international preliminary examination is made, the written opinion of the International Searching Authority will, except in certain cases where the International Preliminary Examining Authority did not act as International Searching Authority and where it has notified the International Bureau under Rule 66.1*bis*(b), be considered to be a written opinion of the International Preliminary Examining Authority. If a demand is made, the applicant may submit to the International Preliminary Examining Authority a reply to the written opinion together, where appropriate, with amendments before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later (Rule 43*bis*.1(c)).

Consequence with regard to translation of the international application for entry into the national phase

The applicant's attention is drawn to the fact that, upon entry into the national phase, a translation of the claims as amended under Article 19 may have to be furnished to the designated/elected Offices, instead of, or in addition to, the translation of the claims as filed.

For further details on the requirements of each designated/elected Office, see the *PCT Applicant's Guide*, Volume II.

Petitioner Hisense USA Corporation
Exhibit 1004 - Page 208 of 373

PATENT COOPERATION TREATY

From the INTERNATIONAL SEARCHING AUTHORITY

To: Kevin C Brown
PO Box 7068
Syracuse NY 13261

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NOTIFICATION OF TRANSMITTAL OF THE INTERNATIONAL SEARCH REPORT AND THE WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY, OR THE DECLARATION

(PCT Rule 44.1)

Applicant's or agent's file reference 931_007 WO	Date of mailing *(day/month/year)* **FOR FURTHER ACTION** See paragraphs 1 and 4 below
International application No. PCT/US 07/01834	International filing date *(day/month/year)* 24 January 2007 (24.01.2007)
Applicant LED Lighting Fixtures Inc	

1. ☒ The applicant is hereby notified that the international search report and the written opinion of the International Searching Authority have been established and are transmitted herewith.

   Filing of amendments and statement under Article 19:
   The applicant is entitled, if he so wishes, to amend the claims of the international application (see Rule 46):

   When? The time limit for filing such amendments is normally two months from the date of transmittal of the international search report.

   Where? Directly to the International Bureau of WIPO, 34 chemin des Colombettes 1211 Geneva 20, Switzerland, Facsimile No.: +41 22 740 14 35

   For more detailed instructions, see the notes on the accompanying sheet.

2. ☐ The applicant is hereby notified that no international search report will be established and that the declaration under Article 17(2)(a) to that effect and the written opinion of the International Searching Authority are transmitted herewith.

3. ☐ **With regard to the protest** against payment of (an) additional fee(s) under Rule 40.2, the applicant is notified that:

   ☐ the protest together with the decision thereon has been transmitted to the International Bureau together with the applicant's request to forward the texts of both the protest and the decision thereon to the designated Offices.

   ☐ no decision has been made yet on the protest; the applicant will be notified as soon as a decision is made.

4. **Reminders**

   Shortly after the expiration of **18 months** from the priority date, the international application will be published by the International Bureau. If the applicant wishes to avoid or postpone publication, a notice of withdrawal of the international application, or of the priority claim, must reach the International Bureau as provided in Rules 90*bis*.1 and 90*bis*.3, respectively, before the completion of the technical preparations for international publication.

   The applicant may submit comments on an informal basis on the written opinion of the International Searching Authority to the International Bureau. The International Bureau will send a copy of such comments to all designated Offices unless an international preliminary examination report has been or is to be established. These comments would also be made available to the public but not before the expiration of 30 months from the priority date.

   Within **19 months** from the priority date, but only in respect of some designated Offices, a demand for international preliminary examination must be filed if the applicant wishes to postpone the entry into the national phase **until 30 months** from the priority date (in some Offices even later); otherwise, the applicant must, **within 20 months** from the priority date, perform the prescribed acts for entry into the national phase before those designated Offices.

   In respect of other designated Offices, the time limit of **30 months** (or later) will apply even if no demand is filed within 19 months.

   See the Annex to Form PCT/IB/301 and, for details about the applicable time limits, Office by Office, see the *PCT Applicant's Guide*, Volume II, National Chapters and the WIPO Internet site.

Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer: Lee W. Young PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/220 (January 2004) *(See notes on accompanying sheet)*

PATENT COOPERATION TREATY

From the INTERNATIONAL SEARCHING AUTHORITY

To: Kevin C Brown
PO Box 7068
Syracuse NY 13261

PCT

NOTIFICATION OF TRANSMITTAL OF THE INTERNATIONAL SEARCH REPORT AND THE WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY, OR THE DECLARATION

(PCT Rule 44.1)

	Date of mailing *(day/month/year)* 28 APR 2008
Applicant's or agent's file reference 931_007 WO	**FOR FURTHER ACTION** See paragraphs 1 and 4 below
International application No. PCT/US 07/01834	International filing date *(day/month/year)* 24 January 2007 (24.01.2007)
Applicant LED Lighting Fixtures Inc	

1. ☒ The applicant is hereby notified that the international search report and the written opinion of the International Searching Authority have been established and are transmitted herewith.

   Filing of amendments and statement under Article 19:
   The applicant is entitled, if he so wishes, to amend the claims of the international application (see Rule 46):

   When? The time limit for filing such amendments is normally two months from the date of transmittal of the international search report.

   Where? Directly to the International Bureau of WIPO, 34 chemin des Colombettes 1211 Geneva 20, Switzerland, Facsimile No.: +41 22 740 14 35

   For more detailed instructions, see the notes on the accompanying sheet.

2. ☐ The applicant is hereby notified that no international search report will be established and that the declaration under Article 17(2)(a) to that effect and the written opinion of the International Searching Authority are transmitted herewith.

3. ☐ **With regard to the protest** against payment of (an) additional fee(s) under Rule 40.2, the applicant is notified that:

   ☐ the protest together with the decision thereon has been transmitted to the International Bureau together with the applicant's request to forward the texts of both the protest and the decision thereon to the designated Offices.

   ☐ no decision has been made yet on the protest; the applicant will be notified as soon as a decision is made.

4. **Reminders**

   Shortly after the expiration of **18 months** from the priority date, the international application will be published by the International Bureau. If the applicant wishes to avoid or postpone publication, a notice of withdrawal of the international application, or of the priority claim, must reach the International Bureau as provided in Rules 90*bis*.1 and 90*bis*.3, respectively, before the completion of the technical preparations for international publication.

   The applicant may submit comments on an informal basis on the written opinion of the International Searching Authority to the International Bureau. The International Bureau will send a copy of such comments to all designated Offices unless an international preliminary examination report has been or is to be established. These comments would also be made available to the public but not before the expiration of 30 months from the priority date.

   Within **19 months** from the priority date, but only in respect of some designated Offices, a demand for international preliminary examination must be filed if the applicant wishes to postpone the entry into the national phase **until 30 months** from the priority date (in some Offices even later); otherwise, the applicant must, **within 20 months** from the priority date, perform the prescribed acts for entry into the national phase before those designated Offices.

   In respect of other designated Offices, the time limit of **30 months** (or later) will apply even if no demand is filed within 19 months.

   See the Annex to Form PCT/IB/301 and, for details about the applicable time limits, Office by Office, see the *PCT Applicant's Guide*, Volume II, National Chapters and the WIPO Internet site.

Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer: Lee W. Young PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/220 (January 2004) *(See notes on accompanying sheet)*

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference 931_007 WO	**FOR FURTHER ACTION**	see Form PCT/ISA/220 as well as, where applicable, item 5 below.
International application No. PCT/US 07/01834	International filing date *(day/month/year)* 24 January 2007 (24.01.2007)	(Earliest) Priority Date *(day/month/year)* 25 January 2006 (25.01.2006)
Applicant LED Lighting Fixtures Inc		

This international search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This international search report consists of a total of 1 sheets.

☐ It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**
   a. With regard to the **language**, the international search was carried out on the basis of:
      ☒ the international application in the language in which it was filed.
      ☐ a translation of the international application into _____ which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b)).
   b. ☐ This international search report has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43.6*bis*(a)).
   c. ☐ With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, see Box No. I.

2. ☐ **Certain claims were found unsearchable** (see Box No. II).

3. ☐ **Unity of invention is lacking** (see Box No. III).

4. With regard to the **title**,
   ☒ the text is approved as submitted by the applicant.
   ☐ the text has been established by this Authority to read as follows:

5. With regard to the **abstract**,
   ☒ the text is approved as submitted by the applicant.
   ☐ the text has been established, according to Rule 38.2(b), by this Authority as it appears in Box No. IV. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.

6. With regard to the **drawings**,
   a. the figure of the **drawings** to be published with the abstract is Figure No. 1
      ☒ as suggested by the applicant.
      ☐ as selected by this Authority, because the applicant failed to suggest a figure.
      ☐ as selected by this Authority, because this figure better characterizes the invention.
   b. ☐ none of the figures is to be published with the abstract.

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 07/01834

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8): H05 B 37/00 (2007.01)
USPC: 315/185R, 192
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
USPC: 315/185R, 192
IPC(8): H05 B 37/00 (2007.01)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
USPC: 315/187, 189, 190, 291, 293, 294 (text search - see terms below)

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

PubWEST(PGPB,USPT,USOC,EPAB,JPAB); Google
Search Terms: organic LED, organic light emitting diode, OLED, LED, light emitting diode, schematic, regulator, LM317, LM117, series, parallel, PWM, pulse wave modulation, regulator, heat sink, fan, cool$, cooling.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X --- Y	US 2006/0001381 A1 (ROBINSON et al.) 05 January 2006 (05.01.2006), para, [0003], [0037], [0038], [0046], [0050], [0052], [0054] through [0060]	1-3, 5, 10, 11 --- 4, 6-9, 12-27
Y	US 2005/0093473 A1 (YEH et al.) 05 May 2005 (05.05.2005), para. [0013]	7, 8
Y	US 2004/0135522 A1 (BERMAN et al.) 15 July 2004 (15.07.2004), para. [0031]-[0032]	9, 25
Y	US 6,515,434 B1 (BIEBL) 04 February 2003 (04.02.2003), col 1, ln. 10-50.	12-27
Y	US 6,793,374 B2 (BEGEMANN) 21 September 2004 (21.09.2004), col 2, ln. 44-50, col 4, ln. 19-28	4, 6, 20, 22, 23
A	US 2005/0077838 A1 (BLUMEL) 14 April 2005 (14.04.2005), entire document, especially para. [0056]	1-27
A	US 4,298,869 A (OKUNO) 03 November 1981 (03.11.1981), entire document	1-27

☐ Further documents are listed in the continuation of Box C. ☐

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
28 June 2007 (28.06.2007)	28 APR 2008

Name and mailing address of the ISA/US	Authorized officer:
Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Lee W. Young PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/210 (second sheet) (April 2007)

PATENT COOPERATION TREATY

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From the
INTERNATIONAL SEARCHING AUTHORITY

To: Kevin C Brown
PO Box 7068
Syracuse NY 13261

PCT

WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43*bis*.1)

Date of mailing *(day/month/year)*	28 APR 2008
Applicant's or agent's file reference 931_007 WO	**FOR FURTHER ACTION** See paragraph 2 below

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US 07/01834	24 January 2007 (24.01.2007)	25 January 2006 (25.01.2006)

International Patent Classification (IPC) or both national classification and IPC
IPC(8) - 315/185R, 192
USPC - H05 B 37/00 (2007.01)

Applicant LED Lighting Fixtures Inc

1. This opinion contains indications relating to the following items:

- [x] Box No. I Basis of the opinion
- [ ] Box No. II Priority
- [ ] Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- [ ] Box No. IV Lack of unity of invention
- [x] Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- [ ] Box No. VI Certain documents cited
- [ ] Box No. VII Certain defects in the international application
- [ ] Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1*bis*(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/220.

3. For further details, see notes to Form PCT/ISA/220.

Name and mailing address of the ISA/US	Date of completion of this opinion	Authorized officer:
Mail Stop PCT, Attn: ISA/US Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	29 June 2007 (29.06.2007)	Lee W. Young PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/237 (cover sheet) (April 2007)

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US 07/01834

Box No. I Basis of this opinion

1. With regard to the **language**, this opinion has been established on the basis of:

   ☒ the international application in the language in which it was filed.

   ☐ a translation of the international application into _____ which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b)).

2. ☐ This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43*bis*.1(a))

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, this opinion has been established on the basis of:

   a. type of material

      ☐ a sequence listing

      ☐ table(s) related to the sequence listing

   b. format of material

      ☐ on paper

      ☐ in electronic form

   c. time of filing/furnishing

      ☐ contained in the international application as filed

      ☐ filed together with the international application in electronic form

      ☐ furnished subsequently to this Authority for the purposes of search

4. ☐ In addition, in the case that more than one version or copy of a sequence listing and/or table(s) relating thereto has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

5. Additional comments:

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WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US 07/01834

Box No. V **Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement**

1. Statement

Novelty (N)	Claims	4, 6-9, 12-27	YES
	Claims	1-3, 5, 10, 11	NO
Inventive step (IS)	Claims	none	YES
	Claims	1-27	NO
Industrial applicability (IA)	Claims	1-27	YES
	Claims	none	NO

2. Citations and explanations:

Claims 1-3, 5, 10 and 11 lack novelty under PCT Article 33(2) as being anticipated by US 2006/0001381 A1 to Robinson et al. (hereinafter Robinson).

With respect to claim 1, Robinson teaches the claimed circuit for a lighting device comprising at least a first sub-circuit (FIG. 3, elements: voltage converter 221, transistor 231, light-emitting element load 241 and signal conditioner 291), the first sub-circuit comprising at least a first series current regulator (transistor 231) and a first group of solid state light emitters (light-emitting element load 241), the first group of solid state light emitters comprising a plurality of first group solid state light emitters, and first series current regulator (transistor 231) and the plurality of first group solid state light emitters (light-emitting element load 241) being arranged in series. (See Robinson, para. [0050].)

With respect to claim 2, Robinson teaches a circuit as recited in claim 1, wherein the circuit further comprises at least one rectifier (power supply 21). The term "power supply" as used by Robinson to define a means for providing power from a power source to electronic circuitry, the power being of a particular type, i.e. AC or DC, and magnitude. (See Robinson, para. [0046].)

With respect to claim 3, Robinson teaches a circuit further comprising at least one capacitor. In the embodiment illustrated in FIG. 1a, power supply 11 may be used to convert AC power to DC power for example, and the voltage conversion means may be a DC-to-DC converter. The DC-to-DC converter may be a step-down switch mode power supply (SMPS), such as a Buck converter. A Buck converter, or other converter, may be used with standard external components such as a diode, capacitor, inductor and feedback components, as taught by Robinson. (See Robinson, para. [0052].)

With respect to claim 5, Robinson teaches a circuit as further comprising at least a second sub-circuit (see FIG. 3, elements: voltage converter 222, transistor 232, light-emitting element load 242 and signal conditioner 292), the second sub-circuit comprising at least a second series current regulator (transistor 232) and a second group of solid state light emitters (light-emitting element load 242), the second group of solid state light emitters comprising a plurality of second group solid state light emitters, the second series current regulator (transistor 232) and the plurality of second group solid state light emitters (light-emitting element load 242) being arranged in series, the first sub-circuit and said second sub-circuit being arranged in parallel relative to each other. (See Robinson, para. [0054]-[0055].)

With respect to claim 10, Robinson teaches a circuit wherein the first sub-circuit comprises fewer than 10 solid state light emitters. Robinsn 381 discloses a string of one or more light emitting diodes. (See Robinson, claim 1.)

With respect to claim 11, Robinson teaches a circuit wherein the first sub-circuit comprises fewer than 5 solid state light emitters. Robinson 381 discloses a string of one or more light emitting diodes. (See Robinson, claim 1.)

Claims 7 and 8 lack an inventive step under PCT Article 33(3) as being obvious over Robinson in view of US 2005/0093473 A1 to Yeh et al. (hereinafter Yeh)

With respect to claim 7, Robinson does not teach a circuit for a lighting device wherein an anode of the first series current regulator is electrically connected to a cathode of one of said first group solid state light emitters. Yeh teaches such a circuit for a lighting device wherein an anode of the first series of a current regulator (transistor 216, FIG. 2, col 2, ln 60-67) being electrically connected to a cathode of one of the first group solid state light emitters (lamp string 204). It would have been obvious to one of ordinary skill in the art connect the lighting devices of Robinson as taught by Yeh in order to regulate the driving currents supplied to the lamp strings (204, 206, 208, 210) with current mirror (212) having respective reference branches connected to respective lamp strings (204, 206, 208, 210).

With respect to claim 8, Yeh further teaches a circuit for a lighting device wherein all of the first group solid state light emitters (lamp strings 204, 206, 208, 210) are upstream of the first series current regulators (transistor 216) to regulate the driving currents supplied to the lamp strings (204, 206, 208, 210) with current mirror (212) having respective reference branches connected to respective lamp strings (2(204, 206, 208, 210). (See Yeh, para. [0013] and Robinson, claim 1).

---See continuation in supplemental box---

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Exhibit 1004 - Page 215 of 373

Supplemental Box

In case **the space in any of the preceding boxes is not sufficient.**
Continuation of:
Box No. V.2 - Citations and explinations:

Claims 4 and 6 lack an inventive step under PCT Article 33(3) as being obvious over Robinson in view of US 6,793,374 B2 to (Begemann).

With respect to claim 4, Robinson discloses a circuit for a lighting device, yet fails to disclose a circuit further comprises at least one fan, wherein the fan is electrically connected in series in at least the first sub-circuit. Begemann discloses an LED lamp (LED lamp, Fig. 2) with a fan used during operation of the lamp to generate forced air cooling. Hence it would have been obvious to one of ordinary skill in the art to combine the fan of Begemann with the circuit of Robinson to construct a circuit comprising a series connected fan to balance the series load and to enable heat dissipation from the circuit, as taught by Begemann. (See Robinson, para. [0050], and Begemann, col. 2, ln. 44-50, and col. 4, ln. 19-28.)

With respect to claim 6, Robinson discloses a circuit for a lighting device, yet fails to disclose a circuit further comprises at least one fan, wherein the fan is electrically connected in series in at least the first sub-circuit. Begemann discloses an LED lamp (LED lamp, Fig. 2) with a fan used during operation of the lamp to generate forced air cooling. Hence it would have been obvious to one of ordinary skill in the art to combine the fan of Begemann with the circuit of Robinson to construct a circuit comprising a series connected fan to balance the series load and to enable heat dissipation from the circuit, as taught by Begemann. (See Robinson 381, para. [0050], and Begemann 374, col. 2, ln. 44-50, and col. 4, ln. 19-28.)

Claims 12-19, 21, 24, 26 and 27 lack an inventive step under PCT Article 33(3) as being obvious over Robinson in view of US 6,515,434 B2 (Biebl).

With respect to claim 12, Robinson teaches a method of lighting a circuit for a lighting device comprising at least a first sub-circuit (FIG. 3, elements: voltage converter 221, transistor 231, light-emitting element load 241 and signal conditioner 291), the first sub-circuit comprising at least a first series current regulator (transistor 231) and a first group of solid state light emitters (light-emitting element load 241), the first group of solid state light emitters comprising a plurality of first group solid state light emitters, and first series current regulator (transistor 231) and the plurality of first group solid state light emitters (light-emitting element load 241) being arranged in series. Robinson fails to disclose specifically a circuit wherein a sum voltage drops across the plurality of first group solid state light emitters and the first series current regulator is in the range of from 1.2 to 1.6 times the first voltage. (See Robinson 381, para. [0050]). However, Biebl discloses that the typical voltage drop across LEDs is a few volts (for Power TOPLED U=2.1V), the voltage drop across the LED remains constant during voltage fluctuations, and LEDs are generally connected in series (cluster) in order to achieve better drive efficiency. Depending on the power supply system (12 V or 42 V), an appropriate number of LEDs can be combined to form a cluster. Hence it would have been obvious to one of skill in the art to combine the circuit of Robinson with the appropriate number of LEDs in a first group of solid state emitters and the first series current regulator, with a known resistance, with a sum voltage drop of 1.2 to 1.6 times the first voltage as taught by Biebl. (See Biebl, col. 1, ln. 10-50.)

With respect to claim 13, Robinson discloses a method wherein the first voltage is in the range of from about 90 volts to about 140 volts. Robinson discloses a power supply used to define a means for providing power from a power source to electronic circuitry, the power being of a particular type, i.e. AC or DC, and magnitude and solid state devices are used for general illumination. North American and Japanese domestic AC power supplies are of typical domestic voltages, between 110-127 VAC. (See Robinson, para. [0003] & [0037].)

With respect to claim 14, Robinson discloses a method wherein the first voltage is about 110 volts. Robinson discloses a power supply used to define a means for providing power from a power source to electronic circuitry, the power being of a particular type, i.e. AC or DC, and magnitude and solid state devices are used for general illumination. North American and Japanese domestic AC power supplies are of typical domestic voltages, between 110-127 VAC. (See Robinson, para. [0003] & [0037].)

With respect to claim 15, Robinson discloses a method wherein the first voltage is about 220 volts. Robinson discloses a power supply used to define a means for providing power from a power source to electronic circuitry, the power being of a particular type, i.e. AC or DC, and magnitude and solid state devices are used for general illumination. Asian, European, African and Australian domestic AC power supplies are of typical domestic voltages, between 220-240 VAC. (See Robinson, para. [0003] & [0037].)

With respect to claim 16, Robinson ,discloses a method wherein the first voltage is about 240 volts. Robinson discloses a power supply used to define a means for providing power from a power source to electronic circuitry, the power being of a particular type, i.e. AC or DC, and magnitude and solid state devices are used for general illumination. Asian, European, African and Australian domestic AC power supplies are of typical domestic voltages, between 220-240 VAC. (See Robinson, para. [0003] & [0037].)

With respect to claim 17, Robinson discloses a method wherein the first voltage is about 277 volts. Robinson discloses a power supply used to define a means for providing power from a power source to electronic circuitry, the power being of a particular type, i.e. AC or DC, and magnitude and solid state devices are used for general illumination. Asian, European, African and Australian domestic AC power supplies are of typical domestic voltages, between 220-240 VAC. 240V being about 277V. (See Robinson, para. [0003] & [0037].)

With respect to claim 18, Robinson discloses a circuit further comprising at least one rectifier. Robinson discloses, power source input to the power supply may be of any magnitude and type, and the output from the power supply may also be of any magnitude and type. DC power supplies are typically rectified. (See Robinson, para. [0038].)

With respect to claim 19, Robinson discloses a circuit further comprising at least one capacitor. (See Robinson, para. [0052] & Fig. 1a.)

---See continuation in supplemental box---

Petitioner Hisense USA Corporation
Exhibit 1004 - Page 216 of 373

Supplemental Box

In case **the space in any of the preceding boxes is not sufficient.**
Continuation of:
Box No. V.2 - Citations and explinations:

With respect to claim 21, Robinson discloses a circuit (Fig. 3) further comprising at least a second sub-circuit (voltage converter 222, node 202, signal conditioner 292, transistor 232, light emitting element load 242), the second sub-circuit comprising at least a second series current regulator (signal conditioner 292, transistor 232) and a second group of solid state light emitters (light emitting element load 242), the second group of solid state light emitters comprising a plurality of second group solid state light emitters (individual light emitting elements illustrated), the second series current regulator (switching device 900, FET, BJT, relay) and the plurality of second group solid state light emitters being arranged in series (Figs. 1a 1f), the first sub-circuit and the second sub-circuit being arranged in parallel relative to each other. (See Robinson , paras. [0058], [0060].)

With respect to claim 24, Robinson discloses a method wherein all of the first group solid state light emitters (light-emitting element load 15, Fig. 1c) are upstream of the first series current regulator (switching device 900, Fig. 1c). (See Robinson, para. [0057] through [0060].)

With respect to claim 26, Robinson teaches a circuit wherein the first sub-circuit comprises fewer than 10 solid state light emitters. Robinsn discloses a string of one or more light emitting diodes. (See Robinson, claim 1.)

With respect to claim 27, Robinson teaches a circuit wherein the first sub-circuit comprises fewer than 5 solid state light emitters. Robinson discloses a string of one or more light emitting diodes. (See Robinson, claim 1.)

Claim 9 lacks an inventive step under PCT Article 33(3) as being obvious over Robinson in view of US 2004/0135522 A1 to Berman et al. (hereinafter Berman).

With respect to claim 9, Robinson discloses a circuit yet fails to disclose a circuit wherin the first sub-circuit comprises at least 40 solid state light emitters. Berman discloses an LED lighting system comprising 96 green LEDs, 72 red LEDs, and 24 blue LEDs. Selecting the number of LEDs in each string can be based on equalization of voltage drops across each the multiple strings arranged in parallel, so as reduce the wasted power in the control module, thus improving efficiency of the circuit. Hence it would have been obvious to one of skill in the art to combine the amount of LEDs used in each sub-circuit of Robinson with the LED selection of Berman to improve the efficiency of the control module and circuit. (See Berman para. [0031]-[0032])

Claims 20, 22 and 23 lack an inventive step under PCT Article 33(3) as being obvious over Robinson and Biebl as applied to claim 12, in further view of Begemann.

With respect to claim 20, Robinson fails to discloses a method wherein the circuit further comprises at least one fan. Begemann discloses an LED lamp (LED lamp, Fig. 2) with a fan used during operation of the lamp to generate forced air cooling. Hence it would have been obvious to one of ordinary skill in the art to combine the fan of Begemann with the circuit of Robinson to construct a circuit further comprising at least one fan, wherein the fan is electrically connected in series in at least the first sub-circuit to balance the series load and to enable heat dissipation from the circuit, as taught by Begemann. (See Begemann, col. 2, ln. 44-50, and col. 4, ln. 19-28.)

With respect to claim 22, Robinson discloses a method for a circuit for a lighting device, yet fails to disclose a circuit further comprises at least one fan, wherein the fan is electrically connected in series to at least the first sub-circuit and said second sub-circuit. Begemann discloses an LED lamp (LED lamp, Fig. 2) with a fan used during operation of the lamp to generate forced air cooling. Hence it would have been obvious to one of ordinary skill in the art to combine the fan of Begemann with the circuit of Robinson to construct a circuit comprising a fan, electrically connected in series to at least the first sub-circuit and the second sub-circuit to balance the series load and to enable heat dissipation from the circuit, as taught by Begemann. (See Robinson, para. [0050], and Begemann 374, col. 2, ln. 44-50, and col. 4, ln. 19-28.)

With respect to claim 23, Robinson discloses a method for a circuit wherein an anode of the first series current regulator (switching device 900, Fig. 1c) is electrically connected to a cathode (downstream electrode of light-emitting element load 15) of one of the first group solid state light emitters. (See Robinson, para. [0057] through [0060].)

Claim 25 lacks an inventive step under PCT Article 33(3) as being obvious over Robinson and Biebel, as applied to claim 12 in further view of Berman.

With respect to claim 25, Robinson discloses a method yet fails to disclose a circuit wherein the first sub-circuit comprises at least 40 solid state light emitters. Berman discloses an LED lighting system comprising 96 green LEDs, 72 red LEDs, and 24 blue LEDs. Selecting the number of LEDs in each string can be based on equalization of voltage drops across each the multiple strings arranged in parallel, so as reduce the wasted power in the control module, thus improving efficiency of the circuit. Hence it would have been obvious to one of skill in the art to combine the amount of LEDs used in each sub-circuit of Robinson with the LED selection of Berman to improve the efficiency of the control module and circuit. (See Berman para. [0031]-[0032].)

Claims 1 through 27 have industrial applicability as set out in PCT Article 33(4), because the subject matter claimed can be made or used in industry.

Petitioner Hisense USA Corporation
Exhibit 1004 - Page 217 of 373

NOTES TO FORM PCT/ISA/220

These Notes are intended to give the basic instructions concerning the filing of amendments under Article 19. The Notes are based on the requirements of the Patent Cooperation Treaty, the Regulations and the Administrative Instructions under that Treaty. In case of discrepancy between these Notes and those requirements, the latter are applicable. For more detailed information, see also the *PCT Applicant's Guide*, a publication of WIPO.

In these Notes, "Article," "Rule" and "Section" refer to the provisions of the PCT, the PCT Regulations and the PCT Administrative Instructions, respectively.

INSTRUCTIONS CONCERNING AMENDMENTS UNDER ARTICLE 19

The applicant has, after having received the international search report and the written opinion of the International Searching Authority, one opportunity to amend the claims of the international application. It should however be emphasized that, since all parts of the international application (claims, description and drawings) may be amended during the international preliminary examination procedure, there is usually no need to file amendments of the claims under Article 19 except where, e.g. the applicant wants the latter to be published for the purposes of provisional protection or has another reason for amending the claims before international publication. Furthermore, it should be emphasized that provisional protection is available in some States only (see *PCT Applicant's Guide*, Volume I/A, Annexes B1 and B2).

The attention of the applicant is drawn to the fact that amendments to the claims under Article 19 are not allowed where the International Searching Authority has declared, under Article 17(2), that no international search report would be established (see *PCT Applicant's Guide*, Volume I/A, paragraph 296).

What parts of the international application may be amended ?

Under Article 19, only the claims may be amended.

During the international phase, the claims may also be amended (or further amended) under Article 34 before the International Preliminary Examining Authority. The description and drawings may only be amended under Article 34 before the International Preliminary Examining Authority.

Upon entry into the national phase, all parts of the international application may be amended under Article 28 or, where applicable, Article 41.

When ? Within 2 months from the date of transmittal of the international search report or 16 months from the priority date, whichever time limit expires later. It should be noted, however, that the amendments will be considered as having been received on time if they are received by the International Bureau after the expiration of the applicable time limit but before the completion of the technical preparations for international publication (Rule 46.1).

Where not to file the amendments ?

The amendments may only be filed with the International Bureau and not with the receiving Office or the International Searching Authority (Rule 46.2).

Where a demand for international preliminary examination has been/is filed, see below.

How ? Either by cancelling one or more entire claims, by adding one or more new claims or by amending the text of one or more of the claims as filed.

A replacement sheet must be submitted for each sheet of the claims which, on account of an amendment or amendments, differs from the sheet originally filed.

All the claims appearing on a replacement sheet must be numbered in Arabic numerals. Where a claim is cancelled, no renumbering of the other claims is required. In all cases where claims are renumbered, they must be renumbered consecutively (Section 205(b)).

The amendments must be made in the language in which the international application is to be published.

What documents must/may accompany the amendments ?

Letter (Section 205(b)):

The amendments must be submitted with a letter.

The letter will not be published with the international application and the amended claims. It should not be confused with the "Statement under Article 19(1)" (see below, under "Statement under Article 19(1)").

The letter must be in English or French, at the choice of the applicant. However, if the language of the international application is English, the letter must be in English; if the language of the international application is French, the letter must be in French.

Petitioner Hisense USA Corporation
Exhibit 1004 - Page 218 of 373

NOTES TO FORM PCT/ISA/220 (continued)

The letter must indicate the differences between the claims as filed and the claims as amended. It must, in particular, indicate, in connection with each claim appearing in the international application (it being understood that identical indications concerning several claims may be grouped), whether

(i) the claim is unchanged;

(ii) the claim is cancelled;

(iii) the claim is new;

(iv) the claim replaces one or more claims as filed;

(v) the claim is the result of the division of a claim as filed.

The following examples illustrate the manner in which amendments must be explained in the accompanying letter:

1. [Where originally there were 48 claims and after amendment of some claims there are 51]:
"Claims 1 to 29, 31, 32, 34, 35, 37 to 48 replaced by amended claims bearing the same numbers, claims 30, 33 and 36 unchanged; new claims 49 to 51 added."

2. [Where originally there were 15 claims and after amendment of all claims there are 11]:
"Claims 1 to 15 replaced by amended claims 1 to 11."

3. [Where originally there were 14 claims and the amendments consist in cancelling some claims and in adding new claims]:
"Claims 1 to 6 and 14 unchanged; claims 7 to 13 cancelled; new claims 15, 16 and 17 added." or
"Claims 7 to 13 cancelled; new claims 15, 16 and 17 added; all other claims unchanged."

4. [Where various kinds of amendments are made]:
"Claims 1-10 unchanged; claims 11 to 13, 18 and 19 cancelled; claims 14, 15 and 16 replaced by amended claim 14; claim 17 subdivided into amended claims 15, 16 and 17; new claims 20 and 21 added."

"Statement under Article 19(1)" (Rule 46.4)

The amendments may be accompanied by a statement explaining the amendments and indicating any impact that such amendments might have on the description and the drawings (which cannot be amended under Article 19(1)).

The statement will be published with the international application and the amended claims.

It must be in the language in which the international application is to be published.

It must be brief, not exceeding 500 words if in English or if translated into English.

It should not be confused with and does not replace the letter indicating the differences between the claims as filed and as amended. It must be filed on a separate sheet and must be identified as such by a heading, preferably by using the words "Statement under Article 19(1)."

It may not contain any disparaging comments on the international search report or the relevance of citations contained in that report. Reference to citations, relevant to a given claim, contained in the international search report may be made only in connection with an amendment of that claim.

Consequence if a demand for international preliminary examination has already been filed

If, at the time of filing any amendments and any accompanying statement, under Article 19, a demand for international preliminary examination has already been submitted, the applicant must preferably, at the time of filing the amendments (and any statement) with the International Bureau, also file with the International Preliminary Examining Authority a copy of such amendments (and of any statement) and, where required, a translation of such amendments for the procedure before that Authority (see Rules 55.3(a) and 62.2, first sentence). For further information, see the Notes to the demand form (PCT/IPEA/401).

If a demand for international preliminary examination is made, the written opinion of the International Searching Authority will, except in certain cases where the International Preliminary Examining Authority did not act as International Searching Authority and where it has notified the International Bureau under Rule 66.1*bis*(b), be considered to be a written opinion of the International Preliminary Examining Authority. If a demand is made, the applicant may submit to the International Preliminary Examining Authority a reply to the written opinion together, where appropriate, with amendments before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later (Rule 43*bis*.1(c)).

Consequence with regard to translation of the international application for entry into the national phase

The applicant's attention is drawn to the fact that, upon entry into the national phase, a translation of the claims as amended under Article 19 may have to be furnished to the designated/elected Offices, instead of, or in addition to, the translation of the claims as filed.

For further details on the requirements of each designated/elected Office, see the *PCT Applicant's Guide*, Volume II.

Petitioner Hisense USA Corporation
Exhibit 1004 - Page 219 of 373

PATENT COOPERATION TREATY

From the
INTERNATIONAL PRELIMINARY EXAMINING AUTHORITY

To:
KEVIN C. BROWN
P.O. BOX 7068
SYRACUSE, NY 13261

RECEIVED
OCT 2 3 2008
BURR & BROWN

PCT

WRITTEN OPINION OF THE INTERNATIONAL PRELIMINARY EXAMINING AUTHORITY

(PCT Rule 66)

Applicant's or agent's file reference 931_007 WO	Date of mailing (*day/month/year*) 20 OCT 2008 **REPLY DUE** within 2 months/days from the above date of mailing

International application No.	International filing date (*day/month/year*)	Priority date (*day/month/year*)
PCT/US07/01834	24 January 2007 (24.01.2007)	25 January 2006 (25.01.2006)

International Patent Classification (IPC) or both national classification and IPC

IPC: **H05B 37/00**(2006.01)
USPC: 315/185R,185S,200A,312-325

Applicant

LED LIGHTING FIXTURES INC

1. ☒ The written opinion established by the International Searching Authority:

   ☒ is ☐ is not

   considered to be a written opinion of the International Preliminary Examining Authority.

2. This second (first, etc.) opinion contains indications relating to the following items:

   ☒ Box No. I Basis of the opinion
   ☒ Box No. II Priority
   ☐ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
   ☐ Box No. IV Lack of unity of invention
   ☒ Box No. V Reasoned statement under Rule 66.2 (a)(ii) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
   ☐ Box No. VI Certain documents cited
   ☐ Box No. VII Certain defects in the international application
   ☐ Box No. VIII Certain observations on the international application

3. The applicant is hereby **invited to reply** to this opinion.

   When? See the time limit indicated above. ~~The applicant may, before the expiration of that time limit, request this Authority to grant an extension, see Rule 66.2(e).~~

   How? By submitting a written reply, accompanied, where appropriate, by amendments, according to Rule 66.3. For the form and the language of the amendments, see Rules 66.8 and 66.9.

   Also For the examiner's obligation to consider amendments and/or arguments, see Rule 66.4*bis*. For an informal communication with the examiner, see Rule 66.6. For an additional opportunity to submit amendments, see Rule 66.4.

   If no reply is filed, the international preliminary examination report will be established on the basis of this opinion.

4. The final date by which the international preliminary report on patentability (Chapter II of the PCT) must be established according to Rule 69.2 is: 25 May 2008 (25.05.2008)

Name and mailing address of the IPEA/ US Mail Stop PCT, Attn: IPEA/US Commissioner for Patents P.O. Box 1450 Alexandria, Virginia 22313-1450 Facsimile No. (703) 305-3230	Authorized officer TUYET VO Telephone No. 571 272 1830

Form PCT/IPEA/408 (cover sheet)(April 2007)

WRITTEN OPINION OF THE INTERNATIONAL PRELIMINARY EXAMINING AUTHORITY

International application No.
PCT/US07/01834

Box No. I Basis of the opinion

1. With regard to the **language**, this opinion had been established on the basis of:

☒ the international application in the language in which it was filed.

☐ a translation of the international application into English, which is the language of a translation furnished for the purposes of:

- ☐ international search (under Rules 12.3(a) and 23.1(b))
- ☐ publication of the international application (under Rule 12.4(a))
- ☐ international preliminary examination (under Rules 55.2(a) and/or 55.3(a))

2. With regard to the elements of the international application, this opinion has been established on the basis of *(replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this opinion as "originally filed.")*:

☐ the international application as originally filed/furnished

☒ the description:
pages 1-20 as originally filed/furnished
pages NONE received by this Authority on _____
pages NONE received by this Authority on _____

☒ the claims:
pages 21-24 as originally filed/furnished
pages NONE as amended (together with any statement) under Article 19
pages 21 received by this Authority on 25 July 2008 (25.07.2008)
pages NONE received by this Authority on _____

☐ the drawings:
pages NONE as originally filed/furnished
pages NONE received by this Authority on _____
pages NONE received by this Authority on _____

☐ a sequence listing and/or any related table(s) - see Supplemental Box Relating to Sequence Listing.

3. ☒ The amendments have resulted in the cancellation of:

- ☒ the description, pages NONE
- ☒ the claims, Nos. 4
- ☒ the drawings, sheets/figs NONE
- ☒ the sequence listing (*specify*): NONE
- ☒ any table(s) related to the sequence listing (*specify*): NONE

4. ☐ This opinion has been established as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed, as indicated in the Supplemental Box (Rule 70.2(c)).

- ☐ the description, pages _____
- ☐ the claims, Nos. _____
- ☐ the drawings, sheets/figs _____
- ☐ the sequence listing (*specify*): _____
- ☐ any table(s) related to the sequence listing (*specify*): _____

5. ☐ This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 66.1(*d-bis*))

Petitioner Hisense USA Corporation
Exhibit 1004 - Page 221 of 373

WRITTEN OPINION OF THE INTERNATIONAL PRELIMINARY EXAMINING AUTHORITY

International application No.
PCT/US07/01834

Box No. II Priority

1. ☐ This opinion has been established as if no priority has been claimed due to the failure to furnish within the prescribed time limit the requested:

   ☐ copy of the earlier application whose priority has been claimed (Rule 66.7(a)).

   ☐ translation of the earlier application whose priority has been claimed (Rule 66.7(b)).

2. ☒ This opinion has been established as if no priority had been claimed due to the fact that the priority claim has been found invalid (Rule 64.1). Thus for the purposes of this opinion, the international filing date indicated above is considered to be the relevant date.

3. Additional observations, if necessary:
The priority claim has been found invalid because the filing date of the priority application is outside the time period provided in PCT Rule 4.10.

Petitioner Hisense USA Corporation
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WRITTEN OPINION OF THE INTERNATIONAL PRELIMINARY EXAMINING AUTHORITY

International application No.
PCT/US07/01834

Box No. V **Reasoned statement under Rule 66.2(a)(ii) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement**

1. Statement

Novelty (N)	Claims NONE	YES
	Claims 12, 18, 19, 21 and 23	NO
Inventive Step (IS)	Claims NONE	YES
	Claims 1-3 and 5-27	NO
Industrial Applicability (IA)	Claims 1-3 AND 5-27	YES
	Claims NONE	NO

2. Citations and Explanations:
Please See Continuation Sheet

Petitioner Hisense USA Corporation
Exhibit 1004 - Page 223 of 373

Supplemental Box
(To be used when the space in any of the preceding boxes is not sufficient.)

TIME LIMIT:
The time limit set for response to a Written Opinion may not be extended. 37 CFR 1.484(d). Any response received after the expiration of the time limit set in the Written Opinion will not be considered in preparing the International Preliminary Report on Patentability (Chapter II of the Patent Cooperation Treaty).

V. 2. Citations and Explanations:

Claims 12, 18, 19, 21 and 23 do not meet novelty under PCT Article 33(2) as being anticipated by Ball (US Pat. 7,239,087).
Liked claim invention, Ball discloses a circuit for driving plural groups of LEDs strings having different numbers of LEDs connected in series in one string while these strings connected in parallel. Each groups of LEDs string is controlled by each switch (820, 822, 824, 826) combine with a controller to act as regulator for regulating each LEDs string, wherein the regulator will boost/buck the power supply to the LEDs according to a number of LEDs, In this instance, the regulator boost the total power provide to the lamp is about 1.33 times of the supply source (col. 17, lines 59) and wherein the circuit comprises a rectifier (Fig. 3A) and a capacitor (Fig. 3B).

Claims 1-3, 5-11, 13-17, 20, 22 and 24-27 do not meet an inventive step under PCT Article 33(3) as being obvious over Ball in view of Branc (US Pat. 4,685,303).

Regarding claims 1- 3, 5-7, 20 and 22, Ball discloses a circuit for driving plural groups of LEDs strings having different numbers of LEDs connected in series in one string while these strings connected in parallel. Each groups of LEDs string is controlled by each switch (820, 822, 824, 826) combine with a controller to act as regulator for regulating each LEDs string, wherein the regulator will boost/buck the power supply to the LEDs according to a number of LEDs and wherein the circuit comprises a rectifier (Fig. 3A) and a capacitor (Fig. 3B).
However Ball does not teach the circuit including a fan connected in series with LEDs in the circuit.

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WRITTEN OPINION OF THE INTERNATIONAL PRELIMINARY EXAMINING AUTHORITY

International application No.
PCT/US07/01834

Supplemental Box
(To be used when the space in any of the preceding boxes is not sufficient.)

Branc discloses a circuit having cooler/fan (73, 98) either connected in parallel/series with LEDs (108, 109).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize fan/cooler as a load connected in series to LEDs as taught by Branc into the Ball lighting circuitry for purpose of cooling the lamp system, made it free from undesired heat, or the circuit can drive different (mechanic) load beside a lamp load.

Regarding claims 8- 11, 13-17 and 24-27, Ball in view of Branc discloses substantially the claim invention as noted above except for LEDs are upstream of the series regulator or the supplied voltage in specific range such as 90-277volts or a number of LEDs in one string are at a certain limited.

It would have been obvious matter of design choices to arrange regulators in downstream or upstream of LEDs string as long as the regulators limit/regulate proper current values flow through the LEDs strings. The number of LEDs can be extended in different arrangement more or less LEDs will affect the value of power supply provided to a whole LEDs string. One skill in the art would obtain the above possible features to optimum the lighting system at a desired manner. Such implementation is considered as a routine skill in the art.

---------- NEW CITATIONS ----------

BALL US 7,239,087 B2 (03.07.2007)

BRANC et al US 4,685,303 (08.11.1987)

Petitioner Hisense USA Corporation
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PATENT COOPERATION TREATY

From the INTERNATIONAL SEARCHING AUTHORITY

PCT

INVITATION TO PAY ADDITIONAL FEES

(PCT Article 17(3)(a) and Rule 40.1)

To:
BURR & BROWN
Attn. Brown, Kevin C.
P.O.Box 7068
Syracuse, NY 13261
ETATS-UNIS D'AMERIQUE

RECEIVED
FEB 15 2008

EINSCHREIBEN

Date of mailing *(day/month/year)* 05/02/2008	
Applicant's or agent's file reference 931_020 WO	**PAYMENT DUE** within **ONE MONTH** from the above date of mailing ✓
International application No. PCT/US2007/078368	International filing date *(day/month/year)* 13/09/2007

Applicant

LED LIGHTING FIXTURES, INC.

1. This International Searching Authority

(i) considers that there are 2 *(number of)* inventions claimed in the international application covered by the claims indicated ~~below~~/on the extra sheet:

and it considers that the international application does not comply with the requirements of unity of invention (Rules 13.1, 13.2 and 13.3) for the reasons indicated ~~below~~/on the extra sheet:

(ii) [X] has carried out a partial international search (see Annex) [ ] will establish the international search report on those parts of the international application which relate to the invention first mentioned in claims Nos.:

see annex

(iii) will establish the international search report on the other parts of the international application only if, and to the extent to which, additional fees are paid

2. The applicant is hereby **invited,** within the time limit indicated above, to pay the amount indicated below:

EUR 1.615,00	x	1	=	EUR 1.615
Fee per additional invention		number of additional inventions		total amount of additional fees
Or, _____	x	_____	=	_____

The applicant is informed that, according to Rule 40.2(c), **the payment of any additional fee may be made under protest,** i.e., a reasoned statement to the effect that the international application complies with the requirement of unity of invention or that the amount of the required additional fee is excessive.

3. [ ] Claim(s) Nos. _____ have been found to be unsearchable under Article 17(2)(b) because of defects under Article 17(2)(a) and therefore have not been included with any invention.

Name and mailing address of the International Searching Authority	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL-2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Christine Voigt

Form PCT/ISA/206 (July 1992)

Annex to Form PCT/ISA/206
COMMUNICATION RELATING TO THE RESULTS OF THE PARTIAL INTERNATIONAL SEARCH

International Application No
PCT/US2007/078368

1. The present communication is an Annex to the invitation to pay additional fees (Form PCT/ISA/206). It shows the results of the international search established on the parts of the international application which relate to the invention first mentioned in claims Nos.:
see 'Invitation to pay additional fees'
2. This communication is not the international search report which will be established according to Article 18 and Rule 43.
3. If the applicant does not pay any additional search fees, the information appearing in this communication will be considered as the result of the international search and will be included as such in the international search report.
4. If the applicant pays additional fees, the international search report will contain both the information appearing in this communication and the results of the international search on other parts of the international application for which such fees will have been paid.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	US 5 973 483 A (JO SANG-SOO [KR]) 26 October 1999 (1999-10-26) column 1, line 25 - column 2, line 10 figure 1	1,8,9, 22,23 2-6,9-22
Y X	JP 10 233669 A (MATSUSHITA ELECTRIC WORKS LTD) 2 September 1998 (1998-09-02) abstract	2-6,9-22 7
Y X	GB 2 249 840 A (HESSAMI ALIREZA GHAZI HESSAMI ALIREZA GHAZI [GB]) 20 May 1992 (1992-05-20) abstract figure 2	2-6,9-22 7

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

1

Petitioner Hisense USA Corporation
Exhibit 1004 - Page 227 of 373

INVITATION TO PAY ADDITIONAL FEES

International application No.
PCT/US2007/078368

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-6,8-23

power converter constituted by a flyback converter and a boost converter sharing a common inductor

---

2. claim: 7

MOSFET current switching circuit for controlling current flowing through LEDs

---

see Re Item IV of the Written Opinion of the International Searching Authoroty of the present application

Petitioner Hisense USA Corporation
Exhibit 1004 - Page 228 of 373

Patent Family Annex

Information on patent family members

International Application No
PCT/US2007/078368

Patent document cited in search report		Publication date	Patent family member(s)	Publication date
US 5973483	A	26-10-1999	NONE	
JP 10233669	A	02-09-1998	NONE	
GB 2249840	A	20-05-1992	NONE	

Petitioner Hisense USA Corporation
Exhibit 1004 - Page 229 of 373

Important Information

General

- The claims cannot be changed at this point in the procedure, the transmitted report is not the international search report (see Art. 19 PCT).
- Any payment has to be made directly to this ISA, payments to other entities will not be accepted.
- In case of a total of more than 2 inventions found: when paying please specify exactly which claims should be searched.
- An extension of the set time limit cannot be granted.

Payment by cheque:

- The date to be considered as the date on which the payment is made is the date of receipt of the cheque at the EPO, provided that the cheque is met.
- Copies of cheques sent by fax or by post are not considered to be a valid payment.
- The fees shall be paid in euro, no equivalents in other currencies.

Payment or transfer to a bank account:

- The date to be considered as the date on which the payment is made is the date on which the amount of the payment or the transfer is actually entered in a bank account or Giro account held by the EPO.
- The fees shall be paid in euro, no equivalents in other currencies.

Payment by deposit account with the EPO:

- The date to be considered as the date on which the payment is made is the date that the authorisation to deduct fees from the deposit account is received at the EPO.

Note: If you don't have a deposit account with the EPO yourself you might want to consider using the account of an associate as a safe and quick way of paying.

Payment by credit card:

- Payments by credit card are not possible.

Payments under protest according to Rule 40 PCT:

- The protest will not be accepted without a payment of additional fees.
- The protest has to be accompanied by a technical reasoning.

New amounts for procedural fees as from 01/04/2006 (see OJ EPO 2006,8)!

- additional search fee: EUR 1615,00
- protest fee: EUR 1065,00

Important information

Rule 40 PCT has been amended as of 1 April 2005. For general information on the protest procedure at ISA/EP, please refer to OJ EPO 3/2005, pages 226/227.

1. As in the past the payment of any additional fee may be made under protest i.e. accompanied by a reasoned statement to the effect that the international application complies with the requirement of unity of invention or that the amount of the required additional fees is excessive according to amended Rule 40.2(c) PCT.

2. After due receipt of the payment of the additional search fee(s) under protest (i.e. within one month from the date of the invitation), the EPO will, prior to examination of the protest by the Board of Appeal, subject the invitation to pay additional fees to an internal review. The result of this review will be communicated to the applicant.

3. The fee for examination of the protest (Rule 40.2(e) PCT) is payable within one month from the date of the invitation to pay additional fees (Rule 40.1(iii) PCT). However, in order to allow the applicant to consider the result of the internal review, the applicant may pay the protest fee within one month from the date of notification of the result of the review.

4. Should the applicant wish to maintain his protest in light of the review he must pay the protest fee within one month from the date of notification of the result of the internal review, in which case the protest will be referred to the Board of Appeal. Should the Board of Appeal find that the protest was entirely justified, the protest fee shall be refunded.

5. In the event of the applicant already having paid the protest fee before notification of the result of the review, the protest will be referred to the Board of Appeal unless the result of the internal review was that the protest was entirely justified or the applicant indicates within one month from the date of notification of the result of the review that he does not wish to continue the protest. In both cases, the protest fee will be refunded.

European Patent Organisation

Account details

Bank account

N° 3 338 800 00 (BLZ 700 800 00)
Dresdner Bank
Promenadeplatz 7
D-80273 München
SWIFT Code: DRESDEFF700
IBAN: DE20 7008 0000 0333 880000
BIC: DRESDEFF

Giro account

N° 300-800 (BLZ 700 100 80)
Deutsche Postbank AG
Bayerstr. 49
D-80138 München

Electronic Acknowledgement Receipt

EFS ID:	6796188
Application Number:	11745713
International Application Number:	
Confirmation Number:	1290
Title of Invention:	Systems and Methods for Controlling a Solid State Lighting Panel
First Named Inventor/Applicant Name:	John K. Roberts
Customer Number:	65106
Filer:	David C. Hall/Jessica French
Filer Authorized By:	David C. Hall
Attorney Docket Number:	5308-703
Receipt Date:	12-JAN-2010
Filing Date:	08-MAY-2007
Time Stamp:	16:51:42
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		5308-703_IDS.pdf	708263 0fe44519e891710f60c2c4f5c21ca795969dd95e	yes	5

	Multipart Description/PDF files in .zip description					
	Document Description		Start		End	
	Transmittal Letter		1		2	
	Information Disclosure Statement (IDS) Filed (SB/08)		3		5	
Warnings:						
Information:						
2	Foreign Reference	JP10233669_ref_Abstract_and_machine_translation.pdf	3158719 242920b07575fcce426fe4c1844d36c5c98b8f98	no	23	
Warnings:						
Information:						
3	Foreign Reference	GB2249840.pdf	956572 f491fd38f29aa8d4cc6b02f345dfc1f324315b28	no	14	
Warnings:						
Information:						
4	Foreign Reference	JP2006242733_ref_abstract_and_machine_translation.pdf	766270 74cc5522bb8d317ba1ba7830f74f2e45ae6b2ce9	no	12	
Warnings:						
Information:						
5	NPL Documents	In_Plug_series.pdf	2381605 f57792a9ec30c70e990c9a6381aab5472fa8534c	no	18	
Warnings:						
Information:						
6	NPL Documents	ISR_and_Written_Opinion_July_4_2008.pdf	1441954 1ae15ae48d59777b0b36e75949c4ee4148840ade	no	13	
Warnings:						
Information:						
7	NPL Documents	ISR_and_Written_Opinion_Feb_20_2008.pdf	2809803 e629eaa46c5b2c5e8e5efa2a27d265c5345c8aa6	no	18	
Warnings:						
Information:						
8	NPL Documents	ISR_and_Written_Opinion_April_28_2008.pdf	1664278 5583be5bc896cf1aec3f69f282c103963071cfa2	no	11	
Warnings:						
Information:						

9	NPL Documents	2nd_Written_Opinion_of_the_I PEA_Oct_20_2008.pdf	574806 3d5b1ff051fea4703ad3fb44b423464dd8907d7e	no	6
Warnings:					
Information:					
10	NPL Documents	Partial_ISR_and_Invitation.pdf	582503 72c49989556f8695de991941f9a1ffc55e58f74b	no	7
Warnings:					
Information:					
11	NPL Documents	Perduijn.pdf	4798218 9e7627a5229300b68827deff27bfd1b95f9d85b2	no	22
Warnings:					
Information:					
12	NPL Documents	US_Provisional_Appl_No_6103 9926.pdf	2596216 5c04eb8e20e2d7b0446ca873f54197042b1d6e31	no	50
Warnings:					
Information:					
		Total Files Size (in bytes):	22439207		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Attorney Docket No. 5308-703 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re: John Roberts et al.
Application No.: 11/745,713
Filing Date: May 8, 2007
Confirmation No. 1290
Examiner: David Lee Lewis
Group Art Unit: 2629
For: Systems and Methods for Controlling a Solid State Lighting Panel

Date: January 12, 2010

Commissioner for Patents
Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT COVER LETTER

Sir:

Attached is an Information Disclosure Statement listing of documents, together with a copy of any listed foreign patent document and/or non-patent literature. A copy of any listed U.S. patent and/or U.S. patent application publication is not provided herewith in accordance with 37 C.F.R. § 1.98(a)(2)(ii).

☒ In accordance with **37 CFR 1.97(b)**, the information disclosure statement is being filed:

☐ (1) within three months of the filing date of a national application other than a continued prosecution application under §1.53(d);

☐ (2) within three months of the date of entry of the national stage as set forth in §1.491 in an international application;

☒ (3) before the mailing of a first Office Action on the merits; or

☐ (4) before the mailing of a first Office Action after the filing of a request for continued examination under §1.114.

☐ In accordance with **37 CFR 1.97(c)**, the information disclosure statement is being filed after the period specified in 37 CFR 1.97(b) above, but before the mailing date of any of a final action under §1.113, a notice of allowance under §1.311, or an action that otherwise closes prosecution in the application, and is accompanied by **one** of the following:

☐ (1) The statement specified under **37 CFR 1.97(e)**, as follows:

☐ Each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement; **or**

☐ No item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in §1.56(c) more than three months prior to the filing of the information disclosure statement; **or**

☐ (2) The fee set forth in §1.17(p);

☐ In accordance with **37 CFR 1.97(d)**, the information disclosure statement is being filed after the period specified in 37 CFR 1.97(c) above, but on or before payment of the issue fee, and is accompanied by **both** of the following:

☐ (1) The statement specified under **37 CFR 1.97(e)**, as follows:

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement; **or**

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in §1.56(c) more than three months prior to the filing of the information disclosure statement; **and**

☐ (2) The fee set forth in §1.17(p);

In accordance with **37 CFR 1.97(g)**, the information disclosure statement shall not be construed as a representation that a search has been made.

In accordance with **37 CFR 1.97(h)**, the information disclosure statement shall not be construed to be an admission that the information cited in the statement is, or is considered to be, material to patentability as defined in §1.56(b).

☐ The Director is hereby authorized to charge the fee specified in 37 C.F.R. § 1.17(p), and any fee deficiency or credit any overpayment, to Deposit Account No. 50-0220; or

☒ No fee is believed due. However, the Director is hereby authorized to charge any deficiency or credit any overpayment to Deposit Account No. 50-0220.

Respectfully submitted,

David C. Hall
Registration No.: 38,904
Attorney for Applicant(s)

Customer Number 65106
Myers Bigel Sibley & Sajovec, P.A.
P.O. Box 37428, Raleigh, NC 27627
919-854-1400
919-854-1401 (Fax)

CERTIFICATION OF TRANSMISSION

I hereby certify that this correspondence is being transmitted via the Office electronic filing system in accordance with § 1.6(a)(4) to the U.S. Patent and Trademark Office on January 12, 2010.

Jessica French

Name: Jessica French

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/745,713	05/08/2007	John K. Roberts	5308-703	1290

65106 7590 07/29/2010

MYERS BIGEL SIBLEY & SAJOVEC, P.A.
P.O. BOX 37428
RALEIGH, NC 27627

EXAMINER	
PATEL, NITIN	

ART UNIT	PAPER NUMBER
2629	

MAIL DATE	DELIVERY MODE
07/29/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	11/745,713	ROBERTS ET AL.	
	Examiner	Art Unit	
	DAVID L. LEWIS	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 May 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-55* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-55* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 May 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *1/12/2010; 9/15/2008;*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

2. **Claims 1-55 are rejected under 35 U.S.C. 102(a) as being anticipated by Chida (WO 2007/049489) and English translation of detailed description (Taisuke, JP2007-114628).**

As in claim 1, Chida teaches of a lighting panel system, **figure 1**, comprising: a lighting panel including a plurality of strings of solid state lighting devices arranged across the panel in a first direction and positioned at intervals in a second direction that is substantially orthogonal to the first direction, **figure 1 item 40**;

a current supply circuit configured to selectively supply a plurality of on-state drive currents to the plurality of strings responsive to a plurality of control signals, **figure 1 item 30**;

and a control system configured to selectively provide control signals to the current supply circuit to selectively drive the plurality of strings, **figure 1 item 10**,

the control system further including firing logic configured to determine a firing order of the plurality of strings, **figure 1 item 20**.

As in claim 2, Chida teaches of, wherein the firing logic comprises rule-based logic operative to generate a non-spatially-sequential firing order, figure 1 item 20, paragraph 24, 32, 39-41.

As in claim 3, Chida teaches of, wherein the rule-based logic comprises a rule that a second string fired after a first string is non-adjacent the first string, paragraph 24, 32, 39-41.

As in claim 4, Chida teaches of, wherein the rule-based logic comprises a rule that a first string is fired simultaneously with a second string, wherein the first string is non-adjacent the second string, paragraph 24, 32, 39-41.

As in claim 5, Chida teaches of, wherein the lighting panel further comprises a plurality of bars that include portions of the plurality of strings, wherein the plurality of bars extend across the panel in the first direction and are positioned adjacent one another in a substantially parallel arrangement, paragraph 24, 32, 39-41.

As in claim 6, Chida teaches of, wherein the firing order is operative to cause a first firing, a second firing and a third firing, wherein the first firing occurs before the second firing and the second firing occurs before the third firing, wherein the first firing supplies current for at least one string in a first bar, the second firing supplies current for at least one string in a second bar and the third firing supplies current for at least one string in a third bar, wherein the second bar is located below the first bar and the third bar is located above the second bar, paragraph 24, 32, 39-41.

As in claim 7, Chida teaches of, further comprising:a first portion of the plurality of strings including solid state lighting devices that emit light in a first dominant wavelength, paragraph 24, 32, 39-41; and a second portion of the plurality of strings including solid state lighting devices that emit light in a second dominant wavelength, wherein each of the plurality of bars includes at least one string of the first portion of the plurality of strings and at least one string of the second portion of the plurality of strings and wherein each of the first portion of the plurality of strings is fired in the firing order and then each of the second portion of the plurality of strings is fired in the firing order, paragraph 24, 32, 39-41.

As in claim 8, Chida teaches of, further comprising: a first portion of the plurality of strings including solid state lighting devices that emit light in a first

dominant wavelength, paragraph 24, 32, 39-41; and a second portion of the plurality of strings including solid state lighting devices that emit light in a second dominant wavelength, wherein at least one string of the first portion of the plurality of strings is fired simultaneously with at least one string of the second portion of the plurality of strings, figure 1, paragraph 24, 32, 39-41.

As in claim 9, Chida teaches of, further comprising: a first portion of the plurality of strings in a first bar, figure 1, paragraph 24, 32, 39-41; and a second portion of the plurality of strings in a second bar, wherein the first and second portions of the plurality of strings are fired sequentially in the firing order and wherein the firing order is configured to determine the location of the second bar relative to the location of the first bar, figure 1, paragraph 24, 32, 39-41.

As in claim 10, Chida teaches of, further comprising: a first portion of the plurality of strings including solid state lighting devices that emit light in a first dominant wavelength, figure 1, paragraph 24, 32, 39-41; and a second portion of the plurality of strings including solid state lighting devices that emit light in a second dominant wavelength, wherein each of the first portion of the plurality of strings is fired in the firing order and then each of the second portion of the plurality of strings is fired in the firing order, figure 1, paragraph 24, 32, 39-41.

As in claim 11, Chida teaches of, wherein the firing logic comprises random logic operative to generate the firing order, figure 1, paragraph 24, 32, 39-41.

As in claim 12, Chida teaches of, further comprising a means for generating a feedback signal configured to provide display performance information to the control system, figure 1, paragraph 24, 32, 39-41.

As in claim 13, Chida teaches of,wherein the current supply circuit comprises a plurality of phase drivers configured to supply a plurality of on-state drive currents at a plurality of times in a firing cycle,wherein the plurality of strings of solid state lighting devices comprise a plurality of string groups, each configured to receive current from one of the plurality of phase drivers, figure 1, paragraph 24, 32, 39-41, and wherein the control system is further configured to determine the plurality of times that each of the plurality of phase drivers begin to supply current to the plurality of string groups, figure 1, paragraph 24, 32, 39-41.

As in claim 14, Chida teaches of, wherein the ratio of a quantity of the plurality of phase drivers to a quantity of the plurality of strings of solid state lighting devices is one and wherein each of the plurality of string groups comprises one of the plurality of strings of solid state lighting devices, figure 1, paragraph 24, 32, 39-41.

As in claim 15, Chida teaches of, wherein the control system is configured to receive a synchronizing signal from a display controller configured to control a display and wherein the firing order is synchronized with periodic operations of the display, figure 1, paragraph 24, 32, 39-41.

As in claim 16, Chida teaches of method for controlling a solid state lighting panel including a plurality of strings of solid state lighting devices configured to extend from a first edge of the panel to a second edge of the panel in substantially adjacent positions relative to one another, **figure 1, paragraph 24, 32, 39-41**,

the method comprising supplying a plurality of pulsed drive currents to the plurality of strings in a non-spatially-sequential firing order, **figure 1 item 20, paragraph 24, 32, 39-41**.

As in claim 17, Chida teaches of, further comprising:determining the firing order that supplies current to a first string of the plurality of strings and a second string of the plurality of strings, figure 1, paragraph 24, 32, 39-41; and defining the second string of the plurality of strings, wherein the defining is based on a location of the first string, figure 1, paragraph 24, 32, 39-41.

As in claim 18, Chida teaches of, wherein defining the second string comprises selecting one of the plurality of strings that is not adjacent to the first string, figure 1, paragraph 24, 32, 39-41.

As in claim 19, Chida teaches of, wherein defining the second string comprises selecting one of the plurality of strings that is located a minimum quantity of strings from the first string, figure 1, paragraph 24, 32, 39-41.

As in claim 20, Chida teaches of, further comprising defining a third string of the plurality of strings, wherein the third string is configured to be fired after the second string and wherein the defining is based on a location of the second string and the location of the first string, figure 1, paragraph 24, 32, 39-41.

As in claim 21, Chida teaches of, wherein defining the second string comprises selecting one of a plurality of strings that is on a first side of the first string and defining the third string comprises selecting one of the plurality of strings that is on a second side of the second string, figure 1, paragraph 24, 32, 39-41.

As in claim 22, Chida teaches of, further comprising grouping a plurality of portions of the plurality of strings on a plurality of bars, wherein the plurality of bars extend across the panel from the first edge to the second edge and are

positioned adjacent one another in a substantially parallel arrangement, figure 1, paragraph 24, 32, 39-41.

As in claim 23, Chida teaches of, further comprising simultaneously supplying current to the portion of the plurality of strings that are in the same one of the plurality of bars, figure 1, paragraph 24, 32, 39-41.

As in claim 24, Chida teaches of, further comprising simultaneously supplying current to a first string located in a first bar and a second string located in a second bar, figure 1, paragraph 24, 32, 39-41.

As in claim 25, Chida teaches of, further comprising: generating a random number; assigning a value to each of the plurality of bars; and simultaneously supplying current to the portion of the plurality of strings on one of the plurality of bars based on the random number, figure 1, paragraph 24, 32, 39-41.

As in claim 26, Chida teaches of, further comprising: supplying current to a first portion of the plurality of strings according to the firing order, wherein the first portion of the plurality of strings includes solid state lighting devices configured to emit light in a first dominant wavelength, figure 1, paragraph 24, 32, 39-41; and supplying current to a second portion of the plurality of strings according to the firing order after supplying current to the first portion of the plurality of strings,

wherein the second portion of the plurality of strings includes solid state lighting devices configured to emit light in a second dominant wavelength, figure 1, paragraph 24, 32, 39-41.

As in claim 27, Chida teaches of, wherein defining is further based on a dominant wavelength of light emitted by the solid state lighting devices in the first string, figure 1, paragraph 24, 32, 39-41.

As in claim 28, Chida teaches of, further comprising simultaneously supplying current to a first string including solid state lighting devices configured to emit light in a first dominant wavelength and a second string including solid state lighting devices configured to emit light in a second dominant wavelength, figure 1, paragraph 24, 32, 39-41.

As in claim 29, Chida teaches of, further comprising: determining the firing order that supplies current to a first string of the plurality of strings and a second string of the plurality of strings, figure 1, paragraph 24, 32, 39-41; and defining the second string based on a dominant wavelength emitted by the solid state lighting devices in the first string and a relative position of the first string, figure 1, paragraph 24, 32, 39-41.

As in claim 30, Chida teaches of, comprising determining the firing order using a numerical technique, figure 1, paragraph 24, 32, 39-41.

As in claim 31, Chida teaches of, further comprising: generating a random number; assigning a value to each of the plurality of strings, figure 1, paragraph 24, 32, 39-41; and supplying current to one of the plurality of strings based on the random number, figure 1, paragraph 24, 32, 39-41.

As in claim 32, Chida teaches of, wherein the numerical technique comprises performing a non-linear calculation., figure 1, paragraph 24, 32, 39-41

As in claim 33, Chida teaches of, wherein the firing order comprises a deterministic order based on at least one rule, figure 1, paragraph 24, 32, 39-41.

As in claim 34, Chida teaches of a system for controlling a solid state lighting panel including a plurality of strings of solid state lighting devices that are arranged to extend across the panel in a first direction and are positioned adjacent one another in a second direction and that are supplied current by a plurality of current drivers, **figure 1, paragraph 24, 32, 39-41,**

the system comprising: a sequence generator that generates a firing sequence for firing the plurality of strings; and a controller that provides control signals,

responsive to the sequence generator, to the plurality of current drivers, **figure 1 item 20, paragraph 24, 32, 39-41**.

As in claim 35, Chida teaches of, wherein the sequence generator comprises a deterministic algorithm that determines a location of a subsequently fired string based on a location of at least one previously fired string, figure 1, paragraph 24, 32, 39-41.

As in claim 36, Chida teaches of, wherein the sequence generator comprises an algorithm that generates a sequence to fire a first string having a plurality of solid state lighting devices that emit light in a first dominant wavelength and a second string having a plurality of solid state lighting devices that emit light in a second dominant wavelength, wherein the second string is fired after the first string, figure 1, paragraph 24, 32, 39-41.

As in claim 37, Chida teaches of, wherein the sequence generator comprises an algorithm that generates a sequence to simultaneously fire a first string having a plurality of solid state lighting devices that emit light in a first dominant wavelength and a second string having a plurality of solid state lighting devices that emit light in a second dominant wavelength, figure 1, paragraph 24, 32, 39-41.

As in claim 38, Chida teaches of, wherein the sequence generator generates a random sequence of firing, figure 1, paragraph 24, 32, 39-41.

As in claim 39, Chida teaches of, further comprising a plurality of bars that include portions of the plurality of strings, wherein the plurality of bars extend across the panel in the first direction and are positioned adjacent one another in the second direction, figure 1, paragraph 24, 32, 39-41.

As in claim 40, Chida teaches of, wherein the firing sequence is configured to simultaneously fire a first portion of the plurality of strings and then simultaneously fire a second portion of the plurality of strings and wherein the first portion is located on a first bar and the second portion is located on a second bar, figure 1, paragraph 24, 32, 39-41.

As in claim 41, Chida teaches of, wherein the firing sequence is configured to simultaneously fire a first string on a first bar and a second string on a second bar, figure 1, paragraph 24, 32, 39-41.

As in claim 42, Chida teaches of, wherein the first string includes solid state lighting devices that emit light in a first dominant wavelength and the second string includes solid state lighting devices that emit light in a second dominant wavelength, figure 1, paragraph 24, 32, 39-41.

As in claim 43, Chida teaches of, further comprising: a first portion of the plurality of strings including solid state lighting devices that emit light in a first dominant wavelength, figure 1, paragraph 24, 32, 39-41; and a second portion of the plurality of strings including solid state lighting devices that emit light in a second dominant wavelength, figure 1, paragraph 24, 32, 39-41; wherein each of the plurality of bars includes at least one string of the first portion of the plurality of strings and at least one string of the second portion of the plurality of strings, figure 1, paragraph 24, 32, 39-41.

As in claim 44, Chida teaches of, wherein the firing sequence is operative to cause the first portion of strings to fire in a first sequence and to then to cause the second portion of strings to fire in the first sequence, figure 1, paragraph 24, 32, 39-41.

As in claim 45, Chida teaches of, wherein the plurality of drivers comprise a polyphase power supply configured to a supply a plurality of temporally shifted drive currents to a plurality of groups of the plurality of strings, figure 1, paragraph 24, 32, 39-41.

As in claim 46, Chida teaches of a method for controlling a solid state lighting panel including a plurality of strings of solid state lighting devices configured to

extend from a first edge of the panel to a second edge of the panel in substantially adjacent positions relative to one another, **figure 1, paragraph 24, 32, 39-41**,

the method comprising supplying a plurality of pulsed drive currents to a plurality of groups of the plurality of strings, **figure 1 item 20, paragraph 24, 32, 39-41**.

As in claim 47, Chida teaches of, wherein each group of the plurality of groups comprises one of the plurality of strings and wherein one of the plurality of pulsed drive currents is provided for each of the plurality of strings by one of a plurality of phase drivers.

As in claim 48, Chida teaches of, further comprising receiving a synchronizing signal from a display controller configured to control a refresh rate of display pixels, figure 1, paragraph 24, 32, 39-41.

As in claim 49, Chida teaches of, further comprising synchronizing the plurality of drive currents with a cycles of a periodic operation of a display panel, figure 1, paragraph 24, 32, 39-41.

As in claim 50, Chida teaches of, wherein the periodic operation comprises refreshing pixels and wherein the display panel comprises an LCD display panel, figure 1, paragraph 24, 32, 39-41.

As in claim 51, Chida teaches of lighting panel system, figure 1,

comprising: a lighting panel including a plurality of strings of solid state lighting devices arranged across the panel in a first direction and positioned at intervals in a second direction that is substantially orthogonal to the first direction, **figure 1 item 40, paragraph 24, 32, 39-41**;

a current supply circuit configured to selectively supply a plurality of on-state drive currents to the plurality of strings responsive to a plurality of control signals, **figure 1 item 30, paragraph 24, 32, 39-41** ;

a control system configured to selectively provide control signals to the current supply circuit to selectively drive the plurality of strings, the control system further including firing logic configured to determine a firing order of the plurality of strings, **figure 1 item 10/20, paragraph 24, 32, 39-41**;

and wherein the firing logic is configured to drive the plurality of strings in a spatially non-adjacent, non-sequential firing order and/or to drive the plurality of

strings at different times for at least a subset of the plurality of strings**, paragraph 24, 32, 39-41**.

As in claim 52, Chida teaches of, wherein the firing logic is further configured to drive the plurality of strings and/or portions thereof at least partially based on the spatial relationship between the plurality of strings and or portions thereof, figure 1, paragraph 24, 32, 39-41.

As in claim 53, Chida teaches of, wherein the firing logic comprises rule-based logic configured to generate a non-spatially sequential firing order, figure 1, paragraph 24, 32, 39-41.

As in claim 54, Chida teaches of, wherein the rule-based logic further comprises a rule that a second string fired after a first string is non-adjacent the first string, figure 1, paragraph 24, 32, 39-41.

As in claim 55, Chida teaches of, wherein the rule-based logic further comprises a rule that if first string is fired simultaneously with a second string, then the first string is non-adjacent the second string, figure 1, paragraph 24, 32, 39-41.

Conclusion

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **David L. Lewis** whose telephone number is **(571) 272-7673**. The examiner can normally be reached on M T W TH F from 9 to 5. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala, can be reached on **(571) 272-7681**. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571)-273-8300.

4. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Examiner: David L. Lewis
April 12, 2010
/David L Lewis/
Primary Examiner, Art Unit 2629

Notice of References Cited	Application/Control No. 11/745,713	Applicant(s)/Patent Under Reexamination ROBERTS ET AL.	
	Examiner DAVID L. LEWIS	Art Unit 2629	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-7,642,725	01-2010	Cusinato et al.	345/102
*	B	US-2003/0112216	06-2003	Choi, Kyu-Don	345/102
*	C	US-5,461,397	10-1995	Zhang et al.	345/102
*	D	US-2009/0021471	01-2009	Park et al.	345/102
*	E	US-2008/0136770	06-2008	PEKER et al.	345/102
*	F	US-2005/0231459	10-2005	Furukawa, Norimasa	345/102
*	G	US-2007/0247414	10-2007	Roberts, John K.	345/102
*	H	US-2008/0150877	06-2008	Chao et al.	345/102
*	I	US-2008/0198112	08-2008	Roberts, John	345/102
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N	JP2007-114628	05-2007	JP	Taisuke	G09G 3/36
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	2007-114628, Taisuke, Senda 5/10/2007, 12 pages, translation of Detailed Description.
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11745713	ROBERTS ET AL.
	Examiner	Art Unit
	DAVID L LEWIS	2629

SEARCHED			
Class	Subclass	Date	Examiner
345	72, 88, 102, 204	4/12/10	DL

SEARCH NOTES		
Search Notes	Date	Examiner
EAST SEARCH, keywords and subclasses, uspat, uspgpubs, epo, jpo, derwent, ibm; inventor name search;	4/12/10	DL

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

	/DAVID L LEWIS/ Primary Examiner.Art Unit 2629

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11745713	ROBERTS ET AL.
	Examiner	Art Unit
	DAVID L LEWIS	2629

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	04/12/2010								
	1	✓								
	2	✓								
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	28	✓								
	29	✓								
	30	✓								
	31	✓								
	32	✓								
	33	✓								
	34	✓								
	35	✓								
	36	✓								

Petitioner Hisense USA Corporation
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Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11745713	ROBERTS ET AL.
	Examiner	**Art Unit**
	DAVID L LEWIS	2629

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	04/12/2010								
	37	✓								
	38	✓								
	39	✓								
	40	✓								
	41	✓								
	42	✓								
	43	✓								
	44	✓								
	45	✓								
	46	✓								
	47	✓								
	48	✓								
	49	✓								
	50	✓								
	51	✓								
	52	✓								
	53	✓								
	54	✓								
	55	✓								

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CONFIRMATION NO. 1290

SERIAL NUMBER	FILING or 371(c) DATE RULE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
11/745,713	05/08/2007	362	2629	5308-703

APPLICANTS

John K. Roberts, Grand Rapids, MI;
Keith J. Vadas, Lowell, MI;

**** CONTINUING DATA ***************************

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****

05/31/2007

Foreign Priority claimed	35 USC 119(a-d) conditions met	Verified and Acknowledged	Met after Allowance	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
☐ Yes ☑ No	☐ Yes ☑ No	/DAVID LEE LEWIS/ Examiner's Signature	☐ Initials	MI	12	55	5

ADDRESS

MYERS BIGEL SIBLEY & SAJOVEC, P.A.
P.O. BOX 37428
RALEIGH, NC 27627
UNITED STATES

TITLE

Systems and Methods for Controlling a Solid State Lighting Panel

FILING FEE RECEIVED		
3280	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1	backlight.ab. and random.ab. and cycle. ab. and frame.ab.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/12 01:53
L2	10	("20060139954" or "6459919" or "20060176411" or "20050035728" or "20020145392").pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/12 02:12
L3	5245	((JOHN) near2 (ROBERTS)).INV.	US-PGPUB; USPAT	OR	ON	2010/04/12 02:41
L4	43	((KEITH) near2 (VADAS)).INV.	US-PGPUB; USPAT	OR	ON	2010/04/12 02:42
S1	0	345/102.ccls. and (phase with driver) and (random with number)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/07 14:33
S2	29	345/102.ccls. and (phase with driver)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/07 14:34
S3	1	345/102.ccls. and (phase adj driver)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/07 14:35
S4	77	345/102.ccls. and string	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/07 14:46
S5	14	345/102.ccls. and string and random	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/07 14:53

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S6	1	345/102.ccls. and string and random.clm.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/07 14:56
S7	2	345/102.ccls. and string and (random or chaotic or nonlinear or "non linear").clm.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/07 15:00
S8	19	345/102.ccls. and (random or chaotic).clm.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/07 15:03
S9	19	345/102.ccls. and (random).clm.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/07 15:06
S10	8280	string and (random).clm.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/07 15:07
S11	63	string and (random).clm. and backlight	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/07 15:07
S12	6	string.clm. and (random).clm. and backlight	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/07 15:14
S13	1655	string.clm. and (random).clm.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/07 15:16
S14	40	string.clm. and (random).clm. and "345"/$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/07 15:16
S15	77	345/102.ccls. and string	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/07 15:17

S16	104	345/102.ccls. and order. ab.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/08 14:32
S17	12	345/102.ccls. and order. ab. and scan$5.ab.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/08 14:32
S18	15	345/102.ccls. and logic. ab.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/08 14:54
S19	19	345/102.ccls. and logic and string	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/08 14:59
S20	0	345/102.ccls. and logic and string and (nonsequenctial or (non adj sequential))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/08 15:04
S21	2	345/102.ccls. and (nonsequential or (non adj sequential)).ab.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/08 15:05
S22	2	345/102.ccls. and (nonsequential or (non adj sequential)).clm.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/08 15:07
S23	6	345/102.ccls. and (nonsequential or (non adj sequential))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/08 15:07
S24	2	07/175,405	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/08 15:09
S25	339	"345"/$.ccls. and (nonsequential or (non adj sequential))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/08 15:10

S26	18	"345"/$.ccls. and (nonsequential or (non adj sequential)).ab.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/08 15:10
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S28	0	(string and backight) and (nonsequential or (non adj sequential))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/08 15:16
S29	229	(string and backlight) and (nonsequential or (non adj sequential))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/08 15:16
S30	29	(nonsequential or (non adj sequential)) and (345/204 or 345/102).ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/08 16:02
S31	29	(nonsequential or (non adj sequential)) and (345/204.ccls. or 345/102.ccls.)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/08 16:04
S32	142	(nonsequential or (non adj sequential) or random).clm. and (345/204.ccls. or 345/102.ccls.)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/08 16:10
S33	25	(nonsequential or (non adj sequential) or random).clm. and (345/204.ccls. or 345/102.ccls.) and (backlight or (back adj light))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/08 16:10
S34	161	(nonsequential or (non adj sequential) or random).ab. and (backlight or (back adj light)).ab.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/08 16:12

S35	12	(nonsequential or (non adj sequential) or random).ab. and (backlight or (back adj light)).ab.	US-PGPUB; USPAT	OR	ON	2010/04/08 17:12
S36	12	(nonsequential or (non adj sequential) or random).ab. and (backlight or (back adj light)).ab.	US-PGPUB; USPAT; USOCR	OR	ON	2010/04/08 17:12
S37	83	(nonsequential or (non adj sequential) or random).ab. and (backlight or (back adj light) or led).ab.	US-PGPUB; USPAT; USOCR	OR	ON	2010/04/08 17:13
S38	308	(nonsequential or (non adj sequential) or random).ab. and (string).ab.	US-PGPUB; USPAT; USOCR	OR	ON	2010/04/08 17:16
S39	7	(random adj number) and 345/102.ccls.	US-PGPUB; USPAT; USOCR	OR	ON	2010/04/08 17:19
S40	79	string and 345/102.ccls.	US-PGPUB; USPAT; USOCR	OR	ON	2010/04/08 17:21
S41	19	string and 345/102.ccls. and logic	US-PGPUB; USPAT; USOCR	OR	ON	2010/04/08 17:24
S42	420	backlight and (random adj number) and led	US-PGPUB; USPAT; USOCR	OR	ON	2010/04/08 17:30
S43	1	backlight same (random adj number) same led	US-PGPUB; USPAT; USOCR	OR	ON	2010/04/08 17:31
S44	3	backlight and (random adj number) and led and 345/102.ccls.	US-PGPUB; USPAT; USOCR	OR	ON	2010/04/08 17:38
S45	1	(random adj order) and 345/102.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/09 10:50
S46	62	((random adj order) or (random adj number)) and (345/102.ccls. or 345/88.ccls. or 345/72.ccls. or 345/204.ccls.)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/09 10:57
S47	0	(firing adj order) and (345/102.ccls. or 345/88.ccls. or 345/72.ccls. or 345/204.ccls.)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/09 12:06

S48	335	(firing adj order).clm.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/09 12:06
S49	5	(firing adj order).clm. and red and blue and green	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/09 12:07
S50	342	(sequence adj generator) and red and blue and green	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/09 12:08
S51	327	(sequence adj generator) and red and blue and green and order	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/09 12:08
S52	269	(sequence adj generator) and red and blue and green and order and simultaneously	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/09 12:09
S53	240	(sequence adj generator) and red and blue and green and order and simultaneously and (adjacent or nonadjacent)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/09 12:09
S54	226	(sequence adj generator) and red and blue and green and order and simultaneously and (adjacent or nonadjacent) and current	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/09 12:11
S55	222	(sequence adj generator) and red and blue and green and order and simultaneously and (adjacent or nonadjacent) and current and random	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/09 12:12

S56	0	simultaneously.clm. and (("non adjacent") or nonadjacent).clm. and 345/102.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/09 12:38
S57	13	simultaneously.clm. and (("non adjacent") or nonadjacent).clm. and "345"/$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/09 12:38
S58	31	simultaneously.clm. and (("non adjacent") or nonadjacent).clm. and string	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/09 12:40
S59	0	345/102.ccls. and (("non adjacent") or nonadjacent).clm. and string	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/09 12:41
S60	6	345/102.ccls. and (("non adjacent") or nonadjacent or adjacent).clm. and string	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/09 12:41
S61	12	345/102.ccls. and sequen$6.clm. and string	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/09 12:44
S62	1	11/745713	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/11 20:29

4/12/10 2:45:36 AM
C:\Documents and Settings\dlewis\My Documents\EAST\Workspaces\11_745713.wsp

INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Complete if Known	
				Application Number	11/745,713
				Filing Date	May 8, 2007
				First Named Inventor	John Roberts et al.
				Art Unit	2629
(use as many sheets as necessary)				Examiner Name	David Lee Lewis
Sheet	B1	of	B3	Attorney Docket Number	5308-703

U.S. PATENT DOCUMENTS						
Examiner Initials*	Cite No.	Document Number Number-Kind Code (if known)		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1.	US	7,557,524	07/07/2009	Chevalier et al.	
	2.	US	7,317,287	01/08/2008	Blumel	
	3.	US	7,239,087	07/03/2007	Ball	
	4.	US	7,213,940	05/08/2007	Van De Ven et al.	
	5.	US	7,202,608	04/10/2007	Robinson et al.	
	6.	US	7,148,632	12/12/2006	Berman et al.	
	7.	US	7,122,971	10/17/2006	Yeh et al.	
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	9.	US	7,038,399	05/02/2006	Lys et al.	
	10.	US	7,014,336	03/21/2006	Ducharme et al.	
	11.	US	6,858,994	02/22/2005	Vollrath	
	12.	US	6,836,081	12/28/2004	Swanson et al.	
	13.	US	6,793,374	09/21/2004	Begemann	
	14.	US	6,630,801	10/07/2003	Schuurmans	
	15.	US	6,618,031	09/09/2003	Bohn Jr., et al.	
	16.	US	6,616,291	09/09/2003	Love	
	17.	US	6,586,890	07/01/2003	Min et al.	
	18.	US	6,577,512	06/10/2003	Tripathi et al.	
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	20.	US	6,552,495	04/22/2003	C. Chang	
	21.	US	6,515,434	02/04/2003	Biebl	
	22.	US	6,510,995	01/28/2003	Muthu et al.	
	23.	US	6,441,558	08/27/2002	Muthu et al.	
	24.	US	6,388,393	05/14/2002	Illingworth	
	25.	US	6,362,578	03/26/2002	Swanson et al.	
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	27.	US	6,329,764	12/11/2001	Van de Ven	
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	29.	US	6,329,758	12/11/2001	Salam	
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	31.	US	6,236,331	05/22/2001	Dussureault	
	32.	US	6,161,910	12/19/2000	Reisenauer et al.	
	33.	US	6,153,985	11/28/2000	Grossman	
	34.	US	6,150,771	11/21/2000	Perry	
	35.	US	6,051,935	04/18/2000	Bucks et al.	
	36.	US	5,973,483	10/26/1999	Jo	
	37.	US	5,812,105	09/22/1998	Van de Ven	

Examiner Signature	/David Lewis/	Date Considered	04/12/2010

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /DL/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Complete if Known	
	Application Number	11/745,713
	Filing Date	May 8, 2007
	First Named Inventor	John Roberts et al.
	Art Unit	2629
(use as many sheets as necessary)	Examiner Name	David Lee Lewis
Sheet B2 of B3	Attorney Docket Number	5308-703

	38.	US	5,783,909	07/21/1998	Hochstein	
	39.	US	5,661,645	08/26/1997	Hochstein	
	40.	US	5,128,595	07/07/1992	Hara	
	41.	US	4,988,889	01/29/1991	Oughton, Jr.	
	42.	US	4,685,303	08/11/1987	Branc et al.	
	43.	US	4,298,869	11/03/1981	Okuno	
	44.	US	3,787,752	01/22/1974	Delay	
	45.	US	2009/0184666	07/23/2009	Myers et al.	
	46.	US	2008/0278097	11/13/2008	Roberts et al.	
	47.	US	2008/0259589	10/23/2008	Van De Ven	
	48.	US	2008/0136313	06/12/2008	Van De Ven et al.	
	49.	US	2008/0130285	06/05/2008	Negley et al.	
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	53.	US	2008/0106895	05/08/2008	Van De Ven et al.	
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	57.	US	2008/0084700	04/10/2008	Van De Ven	
	58.	US	2008/0084685	04/10/2008	Van De Ven et al.	
	59.	US	2008/0048582	02/28/2008	Robinson	
	60.	US	2007/0280624	12/06/2007	Negley et al.	
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	63.	US	2007/0278934	12/06/2007	Van De Ven et al.	
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	65.	US	2007/0274080	11/29/2007	Negley et al.	
	66.	US	2007/0274063	11/29/2007	Negley	
	67.	US	2007/0267983	11/22/2007	Van De Ven et al.	
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	70.	US	2007/0171145	07/26/2007	Coleman et al.	
	71.	US	2007/0170447	07/26/2007	Negley et al.	
	72.	US	2007/0139923	06/21/2007	Negley et al.	
	73.	US	2007/0139920	06/21/2007	Van De Ven et al.	
	74.	US	2007/0137074	06/21/2007	Van De Ven et al.	
	75.	US	2007/0115248	05/24/2007	Roberts et al.	
	76.	US	2004/0046510	03/11/2004	Allen	
	77.	US-	2001/0024112	09/27/2001	Jacobs et al.	

Examiner Signature	/David Lewis/	Date Considered	04/12/2010

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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(use as many sheets as necessary)				Examiner Name	David Lee Lewis
Sheet	B3	of	B3	Attorney Docket Number	5308-703

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No.	Foreign Patent Document Country Code, Number, Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T
	78.	JP 10-233669	09-02-1998	Matsushita Electric Works Ltd.	JPO Machine Translation	Abstract
	79.	GB 2 249 840	05-20-1992	Alireza Ghazi Hessami		Abstract
	80.	JP 2006-242733	09-02-1994	Matsuura Yuji Miyagi Mitsunobu	JPO Machine Translation	Abstract

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T
	81.	In-Plug® series: IPS401, "High Efficiency, High Power Factor, Universal High Brightness WHITE LED Controller", ASIC Advantage Inc.	
	82.	International Search Report and Written Opinion corresponding to International Application No. PCT/US2007/078368; Mailing Date: July 4, 2008.	
	83.	International Search Report and Written Opinion corresponding to International Application No. PCT/US2007/012708; Mailing Date: February 20, 2008.	
	84.	International Search Report and Written Opinion corresponding to International Application No. PCT/US2007/001834; Mailing Date: April 28, 2008.	
	85.	Second Written Opinion corresponding to International Application No. PCT/US2007/001834; Mailing Date: October 20, 2008.	
	86.	Partial International Search Report corresponding to International Application No. PCT/US2007/078368; Mailing Date: February 5, 2008.	
	87.	Perduijn, "Light Output Feedback Solution for RGB LED Backlight Applications"	
	88.	U.S. Provisional Application No. 61/039,926, filed March 27, 2008.	

iDoc# 853530

Examiner Signature	/David Lewis/	Date Considered	04/12/2010

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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /DL/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Complete if Known	
				Application Number	11/745,713
				Filing Date	May 8, 2007
				First Named Inventor	John Roberts et al.
				Art Unit	2629
(use as many sheets as necessary)				Examiner Name	Richard A. Hjerpe
Sheet	A1	of	A1	Attorney Docket Number	5308-703

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No.	Document Number Number-Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
/DL/	1.	US- 2006/0139954 A1	06-29-2006	Kobori et al.	Pg.1; ¶ 5 – pg.5; ¶ 66; Figs. 1-12.
/DL/	2.	US- 6,459,919 B1	10-01-2002	Lys et al.	Whole Document
/DL/	3.	US- 2006/0176411 A1	08-10-2006	Furukawa	Pg.2; ¶ 27 - Pg.4; ¶ 54; Figs. 1, 2, 4-10.
/DL/	4.	US- 2005/0035728 A1	02-17-2005	Schanberger et al.	Pg.1; ¶ 14 – Pg.6; ¶ 56; Fig. 1.
/DL/	5.	US- 2002/0145392 A1	10-10-2002	Hair,III et al.	Pg.1, ¶ 6 – Pg.5; ¶ 47; Figs. 1-8.
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FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No.	Foreign Patent Document Country Code, Number, Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T
/DL/	6.	WO 01/63977 A1	08-30-2001	Production Solutions, Inc.	Whole Document	Abstract

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T
/DL/	7.	International Search Report and Written Opinion (15 pages) corresponding to International Application No. PCT/US2008/005145; Mailing Date: September 2, 2008.	

iDoc# 707389

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PATENT ABSTRACTS OF JAPAN

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G02F 1/133 (2006.01)

(21)Application number : 2005-307944
(22)Date of filing : 24.10.2005

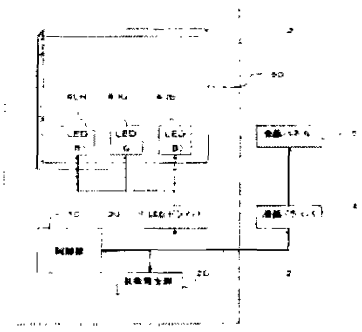
(71)Applicant : ROHM CO LTD
(72)Inventor : SENDA TAISUKE

(54) BACKLIGHT DEVICE AND IMAGE DISPLAY DEVICE USING THE SAME

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a backlight device configured to prevent the light of the same color from being continually recognized during the movement of a visual point on a display regardless of an image recognition period (a period in which the image is recognized on movement of the visual point on the display), and an image display device equipped therewith.

SOLUTION: The backlight device is equipped with a light emitting section which emits light in N (specifying N≥2) kinds of colors and a light controller which makes the light emitting section emit light in any of the above colors, field by field, in which the light controller randomizes the order of the light emitting colors, frame by frame, within the frames. The image display device is equipped therewith.



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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[Field of the Invention]
[0001]
This invention relates to the back light device used for the image display device of a field sequential system, and the image display device using this.
[Background of the Invention]
[0002]
In recent years, development of the device which adopted the field sequential system ("FS method" is called suitably hereafter) is furthered about the image display device. In FS method, the back light unit which used LED [Light Emitting Diode:light emitting diode] of each color of RGB (red, green, and blue) as the light source as a back light of a display panel has provided, It is supposed that image display is performed by carrying out the time sharing of each LED, and making it turn on by turns. By this method, since a color filter is not needed, there is an advantage with reduction of a manufacturing cost and sufficient securable luminosity. In an application concerned, each section by which time sharing was carried out as mentioned above is called the "field."
[0003]
However, on the other hand, in the image display device of FS method, since it has the peculiarity which was mentioned above, a new problem has also been generated about the luminescent color. For example, if an image moves, the problem that coloring occurs in the edge part of the video pattern is mentioned to the patent documents 1.
The solving means for this is introduced.

[0004]
If its attention is paid in order of the luminescent color of each LED, with the image display device by the conventional FS method, light will be emitted, for example like "... /RGB/RGB/RGB/R ..." so that an order of the luminescent color in each frame may become fixed.
[Patent documents 1] JP,2005-233982,A
[Description of the Invention]
[Problem(s) to be Solved by the Invention]

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[0005]
A motion of the viewpoint of the user in the case of seeing the picture of a display here is considered. Like drawing 5 as an example, the case where a viewpoint tries to be moved at a B point is considered from the state which has kept the viewpoint at the A point on a display. thus, a while moving a viewpoint viewpoint -- almost -- the line segment AB top -- P1 and P2 ... as -- it moves and picture information is recognized. Since the frequency of such recognition of picture information is based on peculiar visual capability for every user, it has a certain fixed cycle corresponding to the capability in many cases.
[0006]
Next, about the case where recognition of picture information is made a fixed cycle (this cycle is hereafter called an "image recognition cycle") as mentioned above, the relation between the movement state of a viewpoint and the luminescent color of a back light is shown in drawing 6. The image recognition cycle in the user A presupposes as an example that it is a part for the 4 fields here, and suppose similarly that it is a part for the 6 fields by part for the 3 fields, and the user C by the user B.
[0007]
It will be set to B (blue) in P2, and will be set to R (red) in P3, and if it sees about the user A first, it continues, and in the moment the position of P1 has a viewpoint, the luminescent color of a back light will be G (green), and it will be set to G (green) in P4. Thus, the user A does not produce sense of incongruity in particular in order to recognize two or more colors one by one for a short time.
[0008]
However, if it sees about the user B, in the moment the position of P1 has a viewpoint, the luminescent color of a back light is R (red), and P2, P3, and ... will also be continuously set to R (red). Therefore, the user B will almost recognize the color of R (red) during movement of a viewpoint. Thus, when the light of the same color is recognized continuously, since only the color is emphasized and recognized by human being's eyes, there is a problem of producing sense of incongruity visually in them. The illusion of the stripes-like pattern divided for every luminescent color depending on the case arises.
[0009]
In a passage clear from drawing 6, the problem mentioned above also in the user C arises. That is, in the image display device of FS method, in what becomes constant [an order of the luminescent color for every frame] like conventional technology, when an image recognition cycle serves as an integral multiple of a frame period, the problem mentioned above will arise.
[0010]
Then, this invention aims at offer of the image display device provided with the back light device and this only the light of the same color was made not to recognize to be during movement of the viewpoint on a display continuously regardless of an image recognition cycle in view of the above-mentioned problem.
[Means for Solving the Problem]
[0011]
To achieve the above objects, a back light device concerning this invention, A light-emitting part which emits light in a color of N (referred to as N>=2) kind, and an emission control part which makes the above-mentioned light-emitting part emit light for every field they to be [any of each above-mentioned color], It is a back light device used for an image display device of a ******** field sequential system, and the above-

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mentioned emission control part considers an order of the luminescent color in a frame as composition (the 1st composition) made random for every frame.

[0012]

According to this composition, an order of the luminescent color for every frame becomes random. Therefore, if a back light device of this composition is applied to an image display device of FS method, that only the same color is continuously recognized during movement of a viewpoint on a display will decrease regardless of an image recognition cycle. As a result, it becomes possible to make hard to produce problems, such as only for the color to be emphasized and recognized and to feel uncomfortable visually. It is a period assigned in order to make one picture display it as a "frame", and consists of two or more fields.

[0013]

In the 1st composition of the above, the above-mentioned emission control part is good also in which frame also as composition (the 2nd composition) which makes a color of the above-mentioned N kind said-field [every]-emit light respectively. If it has this composition, a light-emitting part will emit light at same rate as each color of N kind also in which frame. Therefore, only a specific color does not emit light by high frequency, and suitable image display is not barred.

[0014]

In the 2nd composition of the above, the above-mentioned emission control part has the luminescent color concerning the field of the last in a frame of 1, and the good luminescent color concerning the first field in the following frame also as composition (the 3rd composition) it is made to differ.

[0015]

If it has this composition, the same color will not emit light continuously by the 2 fields, for example like "B/B" in "... /RGB/BGR/..." Therefore, compared with what may emit light continuously by the 2 fields, more natural image display of the same color becomes possible.

[0016]

In the 1st or 2nd composition of the above, it has further a random number generator made to generate a random number corresponding to each frame, and the above-mentioned emission control part is good also as composition (the 4th composition) which determines an order of the luminescent color in the above-mentioned frame according to the above-mentioned random number corresponding to the frame.

[0017]

If it has this composition, an order of the luminescent color for every frame will be decided according to a random number which a predetermined random number generator generates. Therefore, by using a general-purpose random number generator, for example, making an order of the luminescent color random for every frame can be realized easily.

[0018]

A light-emitting part with which a back light device concerning this invention emits light in a color of N (referred to as N>=2) kind, An emission control part which makes the above-mentioned light-emitting part emit light for every field they to be [any of each above-mentioned color], It is a back light device used for an image display device of a ******** field sequential system, and the above-mentioned emission control part considers the length of the above-mentioned field as composition (the 5th composition) made random for this every field.

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[0019]
According to this composition, the length of the field becomes random for every field, and width of emission time of each color becomes random. Thereby, if a back light device of this composition is applied to an image display device of FS method, the periodicity of an interval at which the same color emits light can be broken down. Therefore, that only the same color is continuously recognized during movement of a viewpoint on a display decreases regardless of an image recognition cycle. As a result, it becomes possible to make hard to produce problems, such as only for the color to be emphasized and recognized and to feel uncomfortable visually. It is possible to break down the periodicity of an interval at which the same color emits light in this composition, even if an order of the luminescent color is constant.
[0020]
If it is an image display device by a field sequential system using a back light device applied to which 5th composition from the above 1st, an image display device of FS method which made problems, such as feeling uncomfortable visually, hard to produce is realizable.
[Effect of the Invention]
[0021]
If it is a back light device concerning this invention as described above, an order of the luminescent color for every frame will become random. Therefore, if the back light device of this composition is applied to the image display device of FS method, that only the same color is continuously recognized during movement of the viewpoint on a display will decrease regardless of an image recognition cycle. As a result, it becomes possible to make hard to produce problems, such as only for the color to be emphasized and recognized and to feel uncomfortable visually.
[Best Mode of Carrying Out the Invention]
[0022]
As one working example of this invention, the liquid crystal display by FS method is mentioned, and it explains below. The overall lineblock diagram of the liquid crystal display concerning this example is shown in drawing 1. As shown in a figure, this liquid crystal display comprises the back light device 1, the liquid crystal driver 4, and liquid crystal panel 5 grade.
[0023]
The composition of the back light device 1 is explained in detail. The back light device 1 comprises the control section 10, the random number generation part 20, and LED driver 30 grade, and is divided roughly into the emission control part 2 which makes the light-emitting part 3 emit light they to be [any of RGB], and the light-emitting part 3 which comprises LED40R-40B and light guide plate 50 grade, and emits light to any of RGB.
[0024]
The control section 10 has ROM, a register, an arithmetic unit, etc. which made the information etc. which start in order of the control program concerning each device, or the luminescent color memorize, and controls the overall processing operation in a liquid crystal display. A light emission pattern signal is outputted to LED driver 30 and the liquid crystal driver 4. A light emission pattern signal plays the role which transmits the information, including an order of the luminescent color, etc., on a light emission pattern as it is mentioned later.

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[0025]
The random number generation part 20 is a general-purpose random number generator etc., and generates the random number corresponding to each frame. It is made to generate as a random number at this example in the probability almost same in any of six kinds of integers from zero to five they are. This random number breaks down the periodicity in an order of the luminescent color for every frame, and it is used in order to prevent recognizing the same color continuously, so that it may state also later. Therefore, since the random number which the random number generation part 20 generates does not interfere even if it does not necessarily need to be completely random and it has the periodicity of the grade which is a range which can attain the above-mentioned purpose, arbitrary random number generators can be used for it.
[0026]
LED driver 30 accepts a light emission pattern signal from the control section 10, and supplies electric power to LED40R - 40B corresponding to this signal. LED driver 30 comprises PWM signal generation part 31, AND gates 32R-32B, the switches 33R-33B, the constant current sources 34R-34B, etc., as shown in drawing 2. R, G, and B which were given to the right of each number express the exception (red, green, blue) of a color. It is good also as one per each color, and may be constituted from plurality per each color by the number of LED40R - 40B.
[0027]
PWM signal generation part 31 generates a PWM signal in order to control the current amount supplied to LED40R - 40B by an PWM [Pulse Width Modulation:Pulse Density Modulation] method. That is, by controlling the width of the high-level pulse in a PWM signal, the duty ratio of current is adjusted through opening and closing of the switches 33R-33B mentioned later.
[0028]
AND gates 32R-32B accept the light emission pattern signal from the control section 10, and the PWM signal from PWM signal generation part 31, and output these logical products to the switches 33R-33B.
[0029]
The switches 33R-33B are closed when high-level signals are received from AND gates 32R-32B, and they open conversely at the time of the signal carrier beam of a low level. Only when the switches 33R-33B have closed, current is supplied to LED40R - 40B by the constant current sources 34R-34B.
[0030]
The emission control part 2 supplies predetermined electric power to LED40R - 40B by the above composition. In response, LED40R - 40B will emit light, and the light will be led to the rear face of the liquid crystal panel 5 by the light guide plate 50.
[0031]
The liquid crystal driver 4 accepts the light emission pattern signal and picture signal which were mentioned above, and makes a liquid crystal panel drive. The liquid crystal panel 5 comprises two substrates which countered mutually and were formed via the liquid crystal layer, an electrode provided on the substrate corresponding to each pixel, TFT [Thin Film Transistor:thin film transistor] which functions as a switching element, etc. The penetration degree of the light from a back light can be adjusted, and a desired picture can be displayed because this controls the optical rotation of a liquid crystal through the voltage between picture element electrodes.

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[0032]
Next, it explains flowing into the processing in the emission control part 2, referring to drawing 3. About an order of the luminescent color, an order corresponding to a next frame is first decided in each frame. Specifically, the random number generation part 20 generates the random number corresponding to a next frame. And the control section 10 reads this random number information, and writes in a register the information which starts in order of the luminescent color corresponding to the random number concerned as control information on a next frame. The information which starts in order of the luminescent color is matched with the kind of random number by ROM in a control section, and is memorized.
[0033]
Next, according to the information which starts in order of the luminescent color (written in the register) decided by the previous frame about luminescence processing, the control section 10 outputs a light emission pattern signal to LED driver 30. LED driver 30 receives this, supplies electric power for any of LED40R - 40B being for every field, and makes a light-emitting part emit light in a predetermined color.
[0034]
The information which starts in order of the luminescent color is set up like drawing 4 as an example here, and the case where "3" occurs is explained as a random number corresponding to the n-th frame. In this case, the control section 10 writes the information of "GBR" (mind made to emit light in order of G, B, and R) which is an order of the luminescent color corresponding to a random number "3" in a register.
[0035]
Subsequently, if the n-th frame comes, based on the information in a register, in the 1st field in the frame, a high level signal will be outputted to AND gate 32G, and the control section 10 will output a low-level signal to other AND gates. As a result, only the switch 33G will open and close corresponding to a PWM signal, and only LED40G [green] emits light. Only red LED40R is made to emit light and only blue LED40B is made to emit light in the 2nd field in a similar manner succeedingly in the 3rd field.
[0036]
The control section 10 outputs an image display signal to the liquid crystal driver 4. In the period when the light emission pattern signal is being interlocked with in, and the light emission pattern signal of a certain color is outputted, an image display signal is a signal which specifies the pixel on which the color should be displayed. The liquid crystal driver 4 makes the liquid crystal panel 5 drive in response to this image display signal, so that a predetermined picture may be displayed.
[0037]
As for this liquid crystal display, an order of the luminescent color within a frame becomes random for every frame by the above composition. Therefore, regardless of an image recognition cycle, that the same color is continuously recognized during movement of the viewpoint on a display decreases. As a result, only the color is emphasized and recognized and it becomes difficult to produce problems, such as feeling uncomfortable visually.
[0038]
Although an order of the luminescent color for every frame is made random, within each frame, it is supposed also with which color of RGB that light is emitted the said field part (a part for the 1 field [This example]) every respectively. That is, a light-emitting part emits light at same rate as each color of RGB also

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in which frame. Therefore, only a specific color does not emit light by high frequency, and suitable image display is not barred.

[0039]

While changing the rate of each color at random, it may be made for the rate of each color within a prescribed period to become approximately regulated. For example, since the periodicity of the interval which emits light in the same color also by making the length of the field random for every field collapses, that the same color is continuously recognized during movement of the viewpoint on a display decreases regardless of an image recognition cycle. According to the case where making the length of the field random makes random an order of the luminescent color mentioned above, before the field comes, it is attained by using a random number generator etc.

[0040]

For example, according to drawing 3, in each of 3rd field of the n-1st frame, and 1st field of the n-th frame, the luminescent color is G (green) and the same color is emitting light continuously by the 2 fields. In order to avoid continuation luminescence of such the same color, the luminescent color concerning the field of the last in the frame of 1 and the luminescent color concerning the first field in the following frame may control to differ.

[0041]

What is necessary is just to keep the order concerned in the n+1st frame from specifically serving as "RGB" or "RBG", when an order of the luminescent color in the n-th frame is "GBR", for example. Therefore, when information is set up like drawing 4, it is making a random number choose from 2-5, and this control is attained so that a random number may not be set to 0 or 1. By doing in this way, the more natural image display of the same color becomes possible compared with what may carry out continuation luminescence.

[0042]

Although one embodiment of this invention was described as above, the composition of this invention can add various change in the range which is not restricted to this and does not deviate from the main point of an invention.

[Industrial applicability]

[0043]

This invention is useful art about the image display device by a field sequential system.

[Brief Description of the Drawings]

[0044]

[Drawing 1]It is an overall lineblock diagram of a liquid crystal display concerning working example of this invention.

[Drawing 2]It is a lineblock diagram of a LED driver concerning working example of this invention.

[Drawing 3]It is an explanatory view about the contents of processing of an emission control part concerning working example of this invention.

[Drawing 4]It is an explanatory view about the information which starts in order of the luminescent color concerning working example of this invention.

[Drawing 5]It is an explanatory view about movement of the viewpoint on a display.

[Drawing 6]It is an explanatory view about the relation between an image recognition cycle and the

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luminescent color.

[Description of Notations]

[0045]

1 Back light device
2 Emission control part
3 Light-emitting part
4 Liquid crystal driver
5 Liquid crystal panel
10 Control section
20 Random number generation part (random number generator)
30 LED driver
31 PWM signal generation part
32R, 32G, 32B AND gate
33R, 33G, and 33B Switch
34R, 34G, and 34B Constant current source
40R, 40G, 40B LED
50 Light guide plate

[Translation done.]

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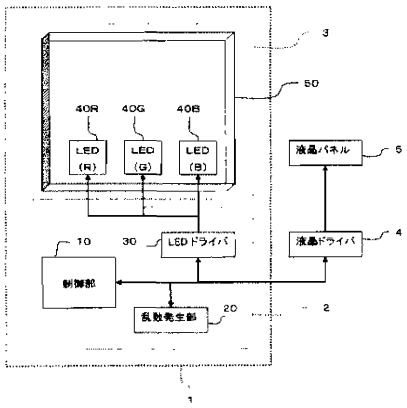
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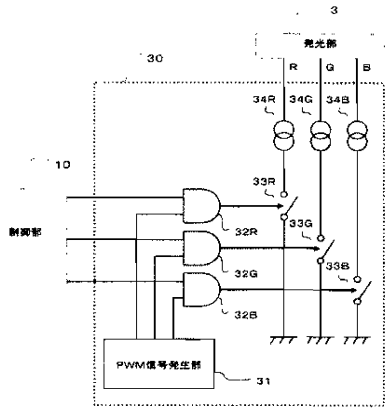
DRAWINGS

[Drawing 1]

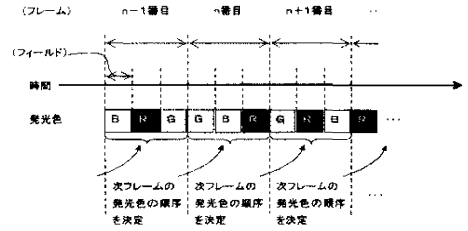


[Drawing 2]

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[Drawing 3]

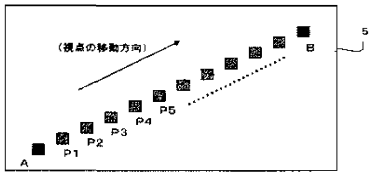


[Drawing 4]

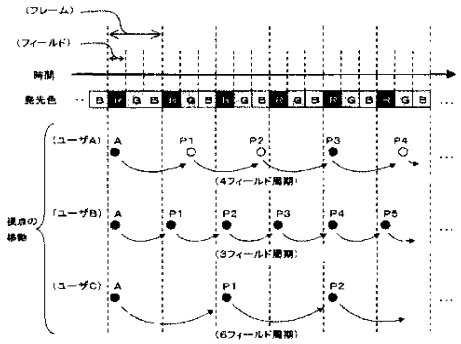
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1	:	R B G
2	:	G R B
3	:	G B R
4	:	B R G
5	:	B G R

[Drawing 5]

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[Drawing 6]



[Translation done.]

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Attorney Docket No. 5308-703 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re: Roberts, et al. Confirmation No.: 1290
Application No.: 11/745,713 Group Art Unit: 2629
Filed: May 8, 2007 Examiner: David Lewis
For: *Systems and Methods for Controlling a Solid State Lighting Panel*

Date: October 18, 2010

Mail Stop AMENDMENT
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE

Sir:

The present response is provided to address the issues raised in the Office Action mailed July 29, 2010.

It is not believed that either an extension of time or payment of additional fees – including fees for net addition of claims – is required, beyond those that may otherwise be provided for in documents accompanying this paper. In the event, however, that an extension of time is necessary to allow consideration of this paper, such an extension is hereby petitioned under 37 C.F.R. §1.136(a). Any additional fees believed to be due in connection with this paper may be charged to Deposit Account No. 50-0220.

A **Listing of Claims** is provided for the Examiner's convenience, beginning on page 2 of this paper.

Remarks begin on page 12 of this paper.

Amendments to the claims:

This listing of the claims will replace all prior versions and listings of the claims in the application:

Listing of Claims:

1. (Original) A lighting panel system, comprising:

a lighting panel including a plurality of strings of solid state lighting devices arranged across the panel in a first direction and positioned at intervals in a second direction that is substantially orthogonal to the first direction;

a current supply circuit configured to selectively supply a plurality of on-state drive currents to the plurality of strings responsive to a plurality of control signals; and

a control system configured to selectively provide control signals to the current supply circuit to selectively drive the plurality of strings, the control system further including firing logic configured to determine a firing order of the plurality of strings.

2. (Original) The system of Claim 1, wherein the firing logic comprises rule-based logic operative to generate a non-spatially-sequential firing order.

3. (Original) The system of Claim 2, wherein the rule-based logic comprises a rule that a second string fired after a first string is non-adjacent the first string.

4. (Original) The system of Claim 2, wherein the rule-based logic comprises a rule that a first string is fired simultaneously with a second string, wherein the first string is non-adjacent the second string.

5. (Original) The system of Claim 1, wherein the lighting panel further comprises a plurality of bars that include portions of the plurality of strings, wherein the plurality of bars extend across the panel in the first direction and are positioned adjacent one another in a substantially parallel arrangement.

6. (Original) The system of Claim 5, wherein the firing order is operative to cause a first firing, a second firing and a third firing, wherein the first firing occurs before the second firing and the second firing occurs before the third firing, wherein the first firing supplies current for at least one string in a first bar, the second firing supplies current for at least one string in a second bar and the third firing supplies current for at least one string in a third bar, wherein the second bar is located below the first bar and the third bar is located above the second bar.

7. (Original) The system of Claim 5, further comprising:

a first portion of the plurality of strings including solid state lighting devices that emit light in a first dominant wavelength; and

a second portion of the plurality of strings including solid state lighting devices that emit light in a second dominant wavelength,

wherein each of the plurality of bars includes at least one string of the first portion of the plurality of strings and at least one string of the second portion of the plurality of strings and wherein each of the first portion of the plurality of strings is fired in the firing order and then each of the second portion of the plurality of strings is fired in the firing order.

8. (Original) The system of Claim 5, further comprising:

a first portion of the plurality of strings including solid state lighting devices that emit light in a first dominant wavelength; and

a second portion of the plurality of strings including solid state lighting devices that emit light in a second dominant wavelength,

wherein at least one string of the first portion of the plurality of strings is fired simultaneously with at least one string of the second portion of the plurality of strings.

9. (Original) The system of Claim 5, further comprising:

a first portion of the plurality of strings in a first bar; and

a second portion of the plurality of strings in a second bar,

wherein the first and second portions of the plurality of strings are fired sequentially in the firing order and wherein the firing order is configured to determine the location of the second bar relative to the location of the first bar.

10. (Original) The system of Claim 1, further comprising:

a first portion of the plurality of strings including solid state lighting devices that emit light in a first dominant wavelength; and

a second portion of the plurality of strings including solid state lighting devices that emit light in a second dominant wavelength,

wherein each of the first portion of the plurality of strings is fired in the firing order and then each of the second portion of the plurality of strings is fired in the firing order.

11. (Original) The system of Claim 1, wherein the firing logic comprises random logic operative to generate the firing order.

12. (Original) The system of Claim 1, further comprising a means for generating a feedback signal configured to provide display performance information to the control system.

13. (Original) The system of Claim 1,

wherein the current supply circuit comprises a plurality of phase drivers configured to supply a plurality of on-state drive currents at a plurality of times in a firing cycle,

wherein the plurality of strings of solid state lighting devices comprise a plurality of string groups, each configured to receive current from one of the plurality of phase drivers, and

wherein the control system is further configured to determine the plurality of times that each of the plurality of phase drivers begin to supply current to the plurality of string groups.

14. (Original) The system of Claim 13, wherein the ratio of a quantity of the plurality of phase drivers to a quantity of the plurality of strings of solid state lighting devices is one and wherein each of the plurality of string groups comprises one of the plurality of strings of solid state lighting devices.

15. (Original) The system of Claim 1, wherein the control system is configured to receive a synchronizing signal from a display controller configured to control a display and wherein the firing order is synchronized with periodic operations of the display.

16. (Original) A method for controlling a solid state lighting panel including a plurality of strings of solid state lighting devices configured to extend from a first edge of the panel to a second edge of the panel in substantially adjacent positions relative to one another, the method comprising supplying a plurality of pulsed drive currents to the plurality of strings in a non-spatially-sequential firing order.

17. (Original) The method of Claim 16, further comprising:

determining the firing order that supplies current to a first string of the plurality of strings and a second string of the plurality of strings; and

defining the second string of the plurality of strings, wherein the defining is based on a location of the first string.

18. (Original) The method of Claim 17, wherein defining the second string comprises selecting one of the plurality of strings that is not adjacent to the first string.

19. (Original) The method of Claim 17, wherein defining the second string comprises selecting one of the plurality of strings that is located a minimum quantity of strings from the first string.

20. (Original) The method of Claim 17, further comprising defining a third string of the plurality of strings, wherein the third string is configured to be fired after the second string and wherein the defining is based on a location of the second string and the location of the first string.

21. (Original) The method of Claim 20, wherein defining the second string comprises selecting one of a plurality of strings that is on a first side of the first string and defining the third string comprises selecting one of the plurality of strings that is on a second side of the second string.

22. (Original) The method of Claim 16, further comprising grouping a plurality of portions of the plurality of strings on a plurality of bars, wherein the plurality of bars extend across the panel from the first edge to the second edge and are positioned adjacent one another in a substantially parallel arrangement.

23. (Original) The method of Claim 22, further comprising simultaneously supplying current to the portion of the plurality of strings that are in the same one of the plurality of bars.

24. (Original) The method of Claim 22, further comprising simultaneously supplying current to a first string located in a first bar and a second string located in a second bar.

25. (Original) The method of Claim 22, further comprising:

generating a random number;

assigning a value to each of the plurality of bars; and

simultaneously supplying current to the portion of the plurality of strings on one of the plurality of bars based on the random number.

26. (Original) The method of Claim 16, further comprising:

supplying current to a first portion of the plurality of strings according to the firing order, wherein the first portion of the plurality of strings includes solid state lighting devices configured to emit light in a first dominant wavelength; and

supplying current to a second portion of the plurality of strings according to the firing order after supplying current to the first portion of the plurality of strings, wherein the second portion of the plurality of strings includes solid state lighting devices configured to emit light in a second dominant wavelength.

27. (Original) The method of Claim 16, wherein defining is further based on a dominant wavelength of light emitted by the solid state lighting devices in the first string.

28. (Original) The method of Claim 16, further comprising simultaneously supplying current to a first string including solid state lighting devices configured to emit light in a first dominant wavelength and a second string including solid state lighting devices configured to emit light in a second dominant wavelength.

29. (Original) The method of Claim 16, further comprising:

determining the firing order that supplies current to a first string of the plurality of strings and a second string of the plurality of strings; and

defining the second string based on a dominant wavelength emitted by the solid state lighting devices in the first string and a relative position of the first string.

30. (Original) The method of Claim 16, comprising determining the firing order using a numerical technique.

31. (Original) The method of Claim 30, further comprising:

generating a random number;

assigning a value to each of the plurality of strings; and

supplying current to one of the plurality of strings based on the random number.

32. (Original) The method of Claim 30, wherein the numerical technique comprises performing a non-linear calculation.

33. (Original) The method of Claim 16, wherein the firing order comprises a deterministic order based on at least one rule.

34. (Original) A system for controlling a solid state lighting panel including a plurality of strings of solid state lighting devices that are arranged to extend across the panel in a first direction and are positioned adjacent one another in a second direction and that are supplied current by a plurality of current drivers, the system comprising:

a sequence generator that generates a firing sequence for firing the plurality of strings; and

a controller that provides control signals, responsive to the sequence generator, to the plurality of current drivers.

35. (Original) The system of Claim 34, wherein the sequence generator comprises a deterministic algorithm that determines a location of a subsequently fired string based on a location of at least one previously fired string.

36. (Original) The system of Claim 34, wherein the sequence generator comprises an algorithm that generates a sequence to fire a first string having a plurality of solid state lighting devices that emit light in a first dominant wavelength and a second string having a plurality of solid state lighting devices that emit light in a second dominant wavelength, wherein the second string is fired after the first string.

37. (Original) The system of Claim 34, wherein the sequence generator comprises an algorithm that generates a sequence to simultaneously fire a first string having a plurality

of solid state lighting devices that emit light in a first dominant wavelength and a second string having a plurality of solid state lighting devices that emit light in a second dominant wavelength.

38. (Original) The system of Claim 34, wherein the sequence generator generates a random sequence of firing.

39. (Original) The system of Claim 34, further comprising a plurality of bars that include portions of the plurality of strings, wherein the plurality of bars extend across the panel in the first direction and are positioned adjacent one another in the second direction.

40. (Original) The system of Claim 39, wherein the firing sequence is configured to simultaneously fire a first portion of the plurality of strings and then simultaneously fire a second portion of the plurality of strings and wherein the first portion is located on a first bar and the second portion is located on a second bar.

41. (Original) The system of Claim 39, wherein the firing sequence is configured to simultaneously fire a first string on a first bar and a second string on a second bar.

42. (Original) The system of Claim 41, wherein the first string includes solid state lighting devices that emit light in a first dominant wavelength and the second string includes solid state lighting devices that emit light in a second dominant wavelength.

43. (Original) The system of Claim 34, further comprising:

a first portion of the plurality of strings including solid state lighting devices that emit light in a first dominant wavelength; and

a second portion of the plurality of strings including solid state lighting devices that emit light in a second dominant wavelength;

wherein each of the plurality of bars includes at least one string of the first portion of the plurality of strings and at least one string of the second portion of the plurality of strings.

44. (Original) The system of Claim 43, wherein the firing sequence is operative to cause the first portion of strings to fire in a first sequence and to then to cause the second portion of strings to fire in the first sequence.

45. (Original) The system of Claim 34, wherein the plurality of drivers comprise a polyphase power supply configured to a supply a plurality of temporally shifted drive currents to a plurality of groups of the plurality of strings.

46. (Original) A method for controlling a solid state lighting panel including a plurality of strings of solid state lighting devices configured to extend from a first edge of the panel to a second edge of the panel in substantially adjacent positions relative to one another, the method comprising supplying a plurality of pulsed drive currents to a plurality of groups of the plurality of strings.

47. (Original) The method of Claim 46, wherein each group of the plurality of groups comprises one of the plurality of strings and wherein one of the plurality of pulsed drive currents is provided for each of the plurality of strings by one of a plurality of phase drivers.

48. (Original) The method of Claim 47, further comprising receiving a synchronizing signal from a display controller configured to control a refresh rate of display pixels.

49. (Original) The method of Claim 46, further comprising synchronizing the plurality of drive currents with a cycles of a periodic operation of a display panel.

50. (Original) The method of Claim 49, wherein the periodic operation comprises refreshing pixels and wherein the display panel comprises an LCD display panel.

51. (Original) A lighting panel system, comprising:

a lighting panel including a plurality of strings of solid state lighting devices arranged across the panel in a first direction and positioned at intervals in a second direction that is substantially orthogonal to the first direction;

a current supply circuit configured to selectively supply a plurality of on-state drive currents to the plurality of strings responsive to a plurality of control signals;

a control system configured to selectively provide control signals to the current supply circuit to selectively drive the plurality of strings, the control system further including firing logic configured to determine a firing order of the plurality of strings; and

wherein the firing logic is configured to drive the plurality of strings in a spatially non-adjacent, non-sequential firing order and/or to drive the plurality of strings at different times for at least a subset of the plurality of strings.

52. (Original) The system of Claim 51, wherein the firing logic is further configured to drive the plurality of strings and/or portions thereof at least partially based on the spatial relationship between the plurality of strings and or portions thereof.

53. (Original) The system of Claim 51, wherein the firing logic comprises rule-based logic configured to generate a non-spatially sequential firing order.

54. (Original) The system of Claim 53, wherein the rule-based logic further comprises a rule that a second string fired after a first string is non-adjacent the first string.

55. (Original) The system of Claim 53, wherein the rule-based logic further comprises a rule that if first string is fired simultaneously with a second string, then the first string is non-adjacent the second string.

REMARKS

Applicants appreciate the thorough examination of the present application as evidenced by the Office Action of July 29, 2010. Applicants respectfully submit that the pending claims are in condition for allowance for at least the reasons discussed herein.

Withdrawal of the Art Rejections Based on Chida Is Respectfully Requested

Claims 1-55 stand rejected under 35 U.S.C. §102(a) as being anticipated by PCT Patent Publication WO 2007/049489 to Chida ("Chida"). (Office Action, page 2.) Since Chida, which has a publication date of May 3, 2007, was not published in the English language, the Office Action further bases the rejection on the English translation of the detailed description of Japanese Patent Publication No. 2007-114628 to Taisuke ("Taisuke"). (Office Action, page 2.)

Applicants respectfully submit that Taisuke has a publication date of May 10, 2007, which is after the filing date of the present application. In this regard, Taisuke is not prior art under 35 U.S.C. §102(a) with respect to the present application.

Additionally, even if Taisuke may be used to provide an English translation of Chida, Chida is not prior art with respect to these claims for at least the reasons set forth in the attached Declaration Pursuant to 37 C.F.R. 1.131. In particular, Chida is effective as a prior art reference as of May 3, 2010, the publication date of the international application.

However, Applicants have established conception of at least the subject matter of the claims in the present application prior to May 3, 2007, coupled with diligence from prior to that date to the filing of the present application on May 8, 2007, as set forth in the Declaration Pursuant to 37 C.F.R. 1.131. More specifically, the invention disclosure of **Appendix A** (referenced in Section 3 of the attached Declaration) shows that the subject matter of the claims was conceived on or before May 3, 2007. In particular, the invention disclosure of Appendix A establishes conception of modified firing order of strings in a solid state backlight unit. In fact, the invention disclosure of Appendix A includes figures and written description that directly correspond at least to FIGS. 1, 5, 6, and 7 of the present application. Moreover, prior invention may be established because the conception and reduction to

practice of the invention occurred in the United States, in accordance with the requirements of 37 C.F.R. 1.131(a). Accordingly, Chida is not prior art with respect to the claims in the present application.

In summary, the above statements, along with the attached Declaration and accompanying documents, provide evidence of reduction to practice of the claims in the present application prior to May 3, 2007, coupled with diligence from prior to May 3, 2007 to the filing of the present application.

Because Chida and/or Taisuke are not prior art with respect to the present application and presently pending Claims 1-55 therein, Applicants respectfully request withdrawal of all prior art rejections of Claims 1-55 based on Chida and/or Taisuke. Applicants respectfully request that the Examiner contact the undersigned attorney if any additional issues regarding the art rejections and/or the attached Declaration should need to be addressed. Applicants have removed Chida and Taisuke as prior art to advance prosecution of the present application to allowance without conceding any teachings of the cited art or agreeing with the Examiner's assertions regarding the rejections of Claims 1-55.

CONCLUSION

Applicants respectfully submit that pending claims are in condition for allowance, which is respectfully requested in due course. Favorable reconsideration of this application is respectfully requested. If any informal matters arise, the Examiner is encouraged to contact the undersigned by telephone at (919) 854-1400.

Respectfully submitted,

Timothy J. Wall
Registration No. 50,743

Myers Bigel Sibley & Sajovec, P.A.
P. O. Box 37428
Raleigh, North Carolina 27627
Telephone: (919) 854-1400
Facsimile: (919) 854-1401
Customer No. 65106

CERTIFICATION OF TRANSMISSION

I hereby certify that this correspondence is being transmitted via the Office electronic filing system in accordance with § 1.6(a)(4) to the U.S. Patent and Trademark Office on October 18, 2010.

Signature: Michele P. McMahan
Michele P. McMahan

Attorney Docket No. 5308-703 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re: Roberts, et al. Confirmation No.: 1290
Application No.: 11/745,713 Group Art Unit: 2629
Filed: May 8, 2007 Examiner: David Lewis
For: *Systems and Methods for Controlling a Solid State Lighting Panel*

DECLARATION PURSUANT TO 37 C.F.R. §1.131

Sir:

I, Keith J. Vadas, hereby declare and say that:

1. I am a named inventor of the subject matter of the inventions disclosed and claimed in U.S. Patent Application Serial No. 11/745,713, filed on May 8, 2007 (hereinafter "the present application").

2. Prior to May 3, 2007, I conceived the invention claimed in the rejected claims.

3. In support of the above statement of Section 2, I hereby submit as **Appendix A** a copy of an invention disclosure I prepared and submitted to the Cree, Inc. patent department before May 3, 2007 showing conception of the claimed invention. The dates within this document have been blocked out, but are before May 3, 2007.

4. Due diligence was exercised from prior to May 3, 2007 to the filing of the present patent application.

5. In support of the above statements of Section 4, I hereby submit as **Appendix B** a copy of an email from Myers Bigel Sibley and Sajovec, P.A. dated April 19, 2007, forwarding a final draft of the present application for my review; and as **Appendix C** a copy of a letter from Myers Bigel Sibley & Sajovec, P.A. dated May 8, 2007, referring to the email of April 19, 2007 and reporting the filing of the present application.

6. In summary, my statements herein and the documents I have concurrently submitted show conception of the invention prior to May 3, 2007 coupled with due diligence from prior to May 3, 2007 to the filing of the present application on May 8, 2007.

7. I hereby declare that all statements made herein of my own knowledge are true, and that all statements made on information and belief are believed to be true. I further declare that these statements were made with knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Keith J. Vadas

October 18, 2010

Keith J. Vadas Date

Electronic Acknowledgement Receipt

EFS ID:	8651400
Application Number:	11745713
International Application Number:	
Confirmation Number:	1290
Title of Invention:	Systems and Methods for Controlling a Solid State Lighting Panel
First Named Inventor/Applicant Name:	John K. Roberts
Customer Number:	65106
Filer:	Timothy Jennings Wall/Michele McMahan
Filer Authorized By:	Timothy Jennings Wall
Attorney Docket Number:	5308-703
Receipt Date:	19-OCT-2010
Filing Date:	08-MAY-2007
Time Stamp:	11:20:41
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		5308_703_Response.pdf	1222714 5b0765e909d2516d5c4cef6198aeccdec5ad9709	yes	14

	Multipart Description/PDF files in .zip description				
	Document Description		**Start**	**End**	
	Amendment/Req. Reconsideration-After Non-Final Reject		1	1	
	Claims		2	11	
	Applicant Arguments/Remarks Made in an Amendment		12	14	
Warnings:					
Information:					
2	Rule 130, 131 or 132 Affidavits	5308_703_131_Declaration.pdf	124978 24d0a7f9445453825a71cdfb705e88bd9d9f4809	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	1347692		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
11/745,713	05/08/2007	

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY ☐ RATE ($)	SMALL ENTITY ☐ FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT 10/19/2010	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 55	Minus	** 55	= 0	X $ =		OR	X $52=	0
Independent (37 CFR 1.16(h))	* 5	Minus	***5	= 0	X $ =		OR	X $220=	0
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0

AMENDMENT	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/DAVINA G. BUTLER/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/745,713	05/08/2007	John K. Roberts	5308-703	1290

65106 7590 01/06/2011

MYERS BIGEL SIBLEY & SAJOVEC, P.A.
P.O. BOX 37428
RALEIGH, NC 27627

EXAMINER	
PATEL, NITIN	

ART UNIT	PAPER NUMBER
2629	

MAIL DATE	DELIVERY MODE
01/06/2011	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	11/745,713	ROBERTS ET AL.	
	Examiner	Art Unit	
	Nitin Patel	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 October 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-55* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-55* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 1-55 are rejected under 35 U.S.C. 102(e) as being anticipated by Yen et al., (US 7,724,220).

As per claims 1, 16, 34,46, 51 Yen shows a lighting panel system, comprising: a lighting panel (element 214 in fig.2)including a plurality of strings of solid state lighting devices(RGB LED device in fig.3) arranged across the panel in a first direction and positioned at intervals in a second direction that is substantially orthogonal to the first direction; a current supply circuit(LED driver with current driving signal in fig.2) configured to selectively supply a plurality of on-state drive currents to the plurality of strings responsive to a plurality of control signals; and a control system 9element 22 in

fig.2)configured to selectively provide control signals to the current supply circuit to selectively drive the plurality of strings, the control system further including firing logic(in fig.1b) configured to determine a firing order of the plurality of strings(in col.6 lines 36-67) and sequence generator as taught by yen reference element 24 interface device.

As per claims 2-15, 17-33,35-45,47-50,52-55 it is well known in the art that programming a controller to a do a function to randomly or sequentially order of frames or scanning line as taught by Yen timing controller would have done the logic sequencing as claimed in claim 2-5,17-33,35-45,47-50,52-55.

Conclusion

2. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Patel whose telephone number is 571-272-7677. The examiner can normally be reached on 8:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Shalwala Bipin can be reached on 571-272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free)? If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Nitin Patel/
Primary Examiner, Art Unit 2629

Notice of References Cited	Application/Control No. 11/745,713	Applicant(s)/Patent Under Reexamination ROBERTS ET AL.	
	Examiner Nitin Patel	Art Unit 2629	Page 1 of 2

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-5,767,818 A	06-1998	Nishida, Shinsuke	345/1.1
*	B	US-5,793,343 A	08-1998	Hart et al.	345/84
*	C	US-2002/0070914 A1	06-2002	Bruning et al.	345/102
*	D	US-6,847,342 B2	01-2005	Tsuji, Ryuhei	345/82
*	E	US-2005/0231459 A1	10-2005	Furukawa, Norimasa	345/102
*	F	US-6,985,124 B1	01-2006	Nogawa, Masashi	345/55
*	G	US-2006/0125773 A1	06-2006	Ichikawa et al.	345/102
*	H	US-2006/0214876 A1	09-2006	Jendbro et al.	345/046
*	I	US-2007/0046590 A1	03-2007	UMEZAKI et al.	345/076
*	J	US-2007/0159434 A1	07-2007	Yen et al.	345/092
*	K	US-7,285,923 B2	10-2007	Yu, Byung-Cheol	315/307
*	L	US-7,327,337 B2	02-2008	Callahan, Jeffrey Scott	345/82
*	M	US-7,365,717 B2	04-2008	Lee et al.	345/77

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Notice of References Cited	Application/Control No. 11/745,713	Applicant(s)/Patent Under Reexamination ROBERTS ET AL.	
	Examiner Nitin Patel	Art Unit 2629	Page 2 of 2

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2009/0066687 A1	03-2009	Oke et al.	345/214
*	B	US-7,557,779 B2	07-2009	Tanada, Yoshifumi	345/76
*	C	US-7,633,577 B2	12-2009	Moon et al.	349/69
*	D	US-7,724,220 B2	05-2010	Yen et al.	345/83
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	1060890	led or (light near2 emit $4 near2 (diode or element or display))or lightnin$4 near2 device $2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/03 03:48
S2	189679	S1 same (current or voltage)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/03 03:49
S3	33224	S2 same (on or off or idle)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/03 03:49
S4	5185	S3 same control$4 near3 (line$2 or signal $2)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/03 03:50
S5	905	S4 and "345"/$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/03 03:51
S6	796	S5 and @ay<="2008"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/03 03:53
S7	300601	current with (on or off)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/03 05:50
S8	474621	(current or voltage) with (on or off)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/03 05:50
S9	155254	"1" same S8	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/03 05:50

Petitioner Hisense USA Corporation
Exhibit 1004 - Page 311 of 373

S10	19908	S9 same (order or sequenc$4 or pattern or non near2 adjac$4 or non near2 sequent$4 or sequent$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/03 05:52
S11	8840	S10 same (control$4 or cpu or mpu or processor or microprocessor)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/03 05:53
S12	72	S11 and 345/102,204.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/03 05:53
S13	1060890	led or (light near2 emit $4 near2 (diode or element or display))or lightnin$4 near2 device $2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/03 05:55
S14	19138	S13 same S8	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/03 05:55
S15	2574	S14 same (order or sequenc$4 or pattern or non near2 adjac$4 or non near2 sequent$4 or sequent$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/03 05:55
S16	1424	S15 same (control$4 or cpu or mpu or processor or microprocessor)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/03 05:55
S17	232	S16 and "345"/$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/03 05:56

EAST Search History (Interference)

<This search history is empty>

1/3/2011 9:28:53 AM
H:\EAST\Workspaces\11745713.wsp

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
11745713	11745713	ROBERTS ET AL.
	Examiner	Art Unit
	Nitin Patel	2629

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	04/12/2010	01/03/2011							
	1	✓	✓							
	2	✓	✓							
	3	✓	✓							
	4	✓	✓							
	5	✓	✓							
	6	✓	✓							
	7	✓	✓							
	8	✓	✓							
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	11	✓	✓							
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	14	✓	✓							
	15	✓	✓							
	16	✓	✓							
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	26	✓	✓							
	27	✓	✓							
	28	✓	✓							
	29	✓	✓							
	30	✓	✓							
	31	✓	✓							
	32	✓	✓							
	33	✓	✓							

Petitioner Hisense USA Corporation
Exhibit 1004 - Page 313 of 373

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
11745713	11745713	ROBERTS ET AL.
	Examiner	**Art Unit**
	Nitin Patel	2629

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	04/12/2010	01/03/2011							
	34	✓	✓							
	35	✓	✓							
	36	✓	✓							
	37	✓	✓							
	38	✓	✓							
	39	✓	✓							
	40	✓	✓							
	41	✓	✓							
	42	✓	✓							
	43	✓	✓							
	44	✓	✓							
	45	✓	✓							
	46	✓	✓							
	47	✓	✓							
	48	✓	✓							
	49	✓	✓							
	50	✓	✓							
	51	✓	✓							
	52	✓	✓							
	53	✓	✓							
	54	✓	✓							
	55	✓	✓							

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
11745713	11745713	ROBERTS ET AL.
	Examiner	**Art Unit**
	Nitin Patel	2629

SEARCHED			
Class	**Subclass**	**Date**	**Examiner**
345	72, 88, 102, 204	1/3/2011	NP

SEARCH NOTES		
Search Notes	**Date**	**Examiner**
EAST SEARCH, keywords and subclasses, uspat, uspgpubs, epo, jpo, derwent, ibm; inventor name search;	1/3/2011	NP

INTERFERENCE SEARCH			
Class	**Subclass**	**Date**	**Examiner**

	/DAVID L LEWIS/ Primary Examiner.Art Unit 2629

INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Complete if Known	
				Application Number	11/745,713
				Filing Date	May 8, 2007
				First Named Inventor	John K. Roberts
				Art Unit	2629
(use as many sheets as necessary)				Examiner Name	Patel, Nitin
Sheet	C1	of	C1	Attorney Docket Number	5308-703

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No.	Document Number Number-Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1.	US- 2006/139954 A1	06-29-2006	Kobori Tomoki et al.	
		US-			
		US-			
		US-			
		US-			

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No.	Foreign Patent Document Country Code, Number, Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T
	2.	Communication pursuant to Article 94(3) EPC dated February 7, 2011 corresponding to European Application No. 08 743 161.5; 6 pages	

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Electronic Acknowledgement Receipt

EFS ID:	9670887
Application Number:	11745713
International Application Number:	
Confirmation Number:	1290
Title of Invention:	Systems and Methods for Controlling a Solid State Lighting Panel
First Named Inventor/Applicant Name:	John K. Roberts
Customer Number:	65106
Filer:	Timothy Jennings Wall/Gwen Bailey
Filer Authorized By:	Timothy Jennings Wall
Attorney Docket Number:	5308-703
Receipt Date:	16-MAR-2011
Filing Date:	08-MAY-2007
Time Stamp:	14:45:41
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		IDS703.pdf	294176 0b3be1f4aba44a7e59c957d7c311bfae641fd3f8	yes	3

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Transmittal Letter	1	2
	Information Disclosure Statement (IDS) Filed (SB/08)	3	3

Warnings:					
Information:					
2	NPL Documents	EPComm.pdf	477466 9c864c056fa731dab7709cc10b649d4052b5f598	no	6
Warnings:					
Information:					
		Total Files Size (in bytes):	771642		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Attorney Docket No. 5308-703 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re: Roberts et al. Confirmation No. 1290
Application No.: 11/745,713 Examiner: Patel, Nitin
Filing Date: May 8, 2007 Group Art Unit: 2629
For: SYSTEMS AND METHODS FOR CONTROLLING A SOLID STATE LIGHTING PANEL

Date: March 16, 2011

Commissioner for Patents
Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT COVER LETTER

Sir:

Attached is an Information Disclosure Statement listing of documents, together with a copy of any listed foreign patent document and/or non-patent literature. A copy of any listed U.S. patent and/or U.S. patent application publication is not provided herewith in accordance with 37 C.F.R. § 1.98(a)(2)(ii).

☐ In accordance with **37 CFR 1.97(b)**, the information disclosure statement is being filed:

☐ (1) within three months of the filing date of a national application other than a continued prosecution application under §1.53(d);

☐ (2) within three months of the date of entry of the national stage as set forth in §1.491 in an international application;

☐ (3) before the mailing of a first Office Action on the merits; or

☐ (4) before the mailing of a first Office Action after the filing of a request for continued examination under §1.114.

☒ In accordance with **37 CFR 1.97(c)**, the information disclosure statement is being filed after the period specified in 37 CFR 1.97(b) above, but before the mailing date of any of a final action under §1.113, a notice of allowance under §1.311, or an action that otherwise closes prosecution in the application, and is accompanied by **one** of the following:

☒ (1) The statement specified under **37 CFR 1.97(e)**, as follows:

☒ Each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement; **or**

☐ No item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in §1.56(c) more than three months prior to the filing of the information disclosure statement; **or**

☐ (2) The fee set forth in §1.17(p);

☐ In accordance with **37 CFR 1.97(d)**, the information disclosure statement is being filed after the period specified in 37 CFR 1.97(c) above, but on or before payment of the issue fee, and is accompanied by **both** of the following:

☐ (1) The statement specified under **37 CFR 1.97(e)**, as follows:

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement; **or**

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in §1.56(c) more than three months prior to the filing of the information disclosure statement; **and**

☐ (2) The fee set forth in §1.17(p);

In accordance with **37 CFR 1.97(g)**, the information disclosure statement shall not be construed as a representation that a search has been made.

In accordance with **37 CFR 1.97(h)**, the information disclosure statement shall not be construed to be an admission that the information cited in the statement is, or is considered to be, material to patentability as defined in §1.56(b).

☐ The Director is hereby authorized to charge the fee specified in 37 C.F.R. § 1.17(p), and any fee deficiency or credit any overpayment, to Deposit Account No. 50-0220; or

☒ No fee is believed due. However, the Director is hereby authorized to charge any deficiency or credit any overpayment to Deposit Account No. 50-0220.

Respectfully submitted,

Timothy J. Wall
Registration No.: 50,743
Attorney for Applicant(s)

Customer Number 65106
Myers Bigel Sibley & Sajovec, P.A.
P.O. Box 37428, Raleigh, NC 27627
919-854-1400
919-854-1401 (Fax)

CERTIFICATION OF TRANSMISSION

I hereby certify that this correspondence is being transmitted via the Office electronic filing system in accordance with § 1.6(a)(4) to the U.S. Patent and Trademark Office on March 16, 2011.

Gwen R. Bailey

Attorney Docket No. 5308-703 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re: Roberts, et al.
Application No.: 11/745,713
Filed: May 8, 2007
For: SYSTEMS AND METHODS FOR CONTROLLING A SOLID STATE LIGHTING PANEL

Confirmation No.: 1290
Group Art Unit: 2629
Examiner: Nitin Patel

April 6, 2011

Mail Stop AMENDMENT
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE

Sir:

The present response is provided to address the issues raised in the Office Action mailed January 06, 2011.

It is not believed that either an extension of time or payment of additional fees – including fees for net addition of claims – is required, beyond those that may otherwise be provided for in documents accompanying this paper. In the event, however, that an extension of time is necessary to allow consideration of this paper, such an extension is hereby petitioned under 37 C.F.R. §1.136(a). Any additional fees believed to be due in connection with this paper may be charged to Deposit Account No. 50-0220.

A **Listing of Claims** is provided for the Examiner's convenience, beginning on page 2 of this paper.

Remarks begin on page 12 of this paper.

Amendments to the claims:

This listing of the claims will replace all prior versions and listings of the claims in the application:

Listing of Claims:

1. (Original) A lighting panel system, comprising:

a lighting panel including a plurality of strings of solid state lighting devices arranged across the panel in a first direction and positioned at intervals in a second direction that is substantially orthogonal to the first direction;

a current supply circuit configured to selectively supply a plurality of on-state drive currents to the plurality of strings responsive to a plurality of control signals; and

a control system configured to selectively provide control signals to the current supply circuit to selectively drive the plurality of strings, the control system further including firing logic configured to determine a firing order of the plurality of strings.

2. (Original) The system of Claim 1, wherein the firing logic comprises rule-based logic operative to generate a non-spatially-sequential firing order.

3. (Original) The system of Claim 2, wherein the rule-based logic comprises a rule that a second string fired after a first string is non-adjacent the first string.

4. (Original) The system of Claim 2, wherein the rule-based logic comprises a rule that a first string is fired simultaneously with a second string, wherein the first string is non-adjacent the second string.

5. (Original) The system of Claim 1, wherein the lighting panel further comprises a plurality of bars that include portions of the plurality of strings, wherein the

plurality of bars extend across the panel in the first direction and are positioned adjacent one another in a substantially parallel arrangement.

6. (Original) The system of Claim 5, wherein the firing order is operative to cause a first firing, a second firing and a third firing, wherein the first firing occurs before the second firing and the second firing occurs before the third firing, wherein the first firing supplies current for at least one string in a first bar, the second firing supplies current for at least one string in a second bar and the third firing supplies current for at least one string in a third bar, wherein the second bar is located below the first bar and the third bar is located above the second bar.

7. (Original) The system of Claim 5, further comprising:

a first portion of the plurality of strings including solid state lighting devices that emit light in a first dominant wavelength; and

a second portion of the plurality of strings including solid state lighting devices that emit light in a second dominant wavelength,

wherein each of the plurality of bars includes at least one string of the first portion of the plurality of strings and at least one string of the second portion of the plurality of strings and wherein each of the first portion of the plurality of strings is fired in the firing order and then each of the second portion of the plurality of strings is fired in the firing order.

8. (Original) The system of Claim 5, further comprising:

a first portion of the plurality of strings including solid state lighting devices that emit light in a first dominant wavelength; and

a second portion of the plurality of strings including solid state lighting devices that emit light in a second dominant wavelength,

wherein at least one string of the first portion of the plurality of strings is fired simultaneously with at least one string of the second portion of the plurality of strings.

9. (Original) The system of Claim 5, further comprising:

a first portion of the plurality of strings in a first bar; and

a second portion of the plurality of strings in a second bar,

wherein the first and second portions of the plurality of strings are fired sequentially in the firing order and wherein the firing order is configured to determine the location of the second bar relative to the location of the first bar.

10. (Original) The system of Claim 1, further comprising:

a first portion of the plurality of strings including solid state lighting devices that emit light in a first dominant wavelength; and

a second portion of the plurality of strings including solid state lighting devices that emit light in a second dominant wavelength,

wherein each of the first portion of the plurality of strings is fired in the firing order and then each of the second portion of the plurality of strings is fired in the firing order.

11. (Original) The system of Claim 1, wherein the firing logic comprises random logic operative to generate the firing order.

12. (Original) The system of Claim 1, further comprising a means for generating a feedback signal configured to provide display performance information to the control system.

13. (Original) The system of Claim 1,

wherein the current supply circuit comprises a plurality of phase drivers configured to supply a plurality of on-state drive currents at a plurality of times in a firing cycle,

wherein the plurality of strings of solid state lighting devices comprise a plurality of string groups, each configured to receive current from one of the plurality of phase drivers, and

wherein the control system is further configured to determine the plurality of times that each of the plurality of phase drivers begin to supply current to the plurality of string groups.

14. (Original) The system of Claim 13, wherein the ratio of a quantity of the plurality of phase drivers to a quantity of the plurality of strings of solid state lighting devices is one and wherein each of the plurality of string groups comprises one of the plurality of strings of solid state lighting devices.

15. (Original) The system of Claim 1, wherein the control system is configured to receive a synchronizing signal from a display controller configured to control a display and wherein the firing order is synchronized with periodic operations of the display.

16. (Original) A method for controlling a solid state lighting panel including a plurality of strings of solid state lighting devices configured to extend from a first edge of the panel to a second edge of the panel in substantially adjacent positions relative to one another, the method comprising supplying a plurality of pulsed drive currents to the plurality of strings in a non-spatially-sequential firing order.

17. (Original) The method of Claim 16, further comprising:

determining the firing order that supplies current to a first string of the plurality of strings and a second string of the plurality of strings; and

defining the second string of the plurality of strings, wherein the defining is based on a location of the first string.

18. (Original) The method of Claim 17, wherein defining the second string comprises selecting one of the plurality of strings that is not adjacent to the first string.

19. (Original) The method of Claim 17, wherein defining the second string comprises selecting one of the plurality of strings that is located a minimum quantity of strings from the first string.

20. (Original) The method of Claim 17, further comprising defining a third string of the plurality of strings, wherein the third string is configured to be fired after the second string and wherein the defining is based on a location of the second string and the location of the first string.

21. (Original) The method of Claim 20, wherein defining the second string comprises selecting one of a plurality of strings that is on a first side of the first string and defining the third string comprises selecting one of the plurality of strings that is on a second side of the second string.

22. (Original) The method of Claim 16, further comprising grouping a plurality of portions of the plurality of strings on a plurality of bars, wherein the plurality of bars extend across the panel from the first edge to the second edge and are positioned adjacent one another in a substantially parallel arrangement.

23. (Original) The method of Claim 22, further comprising simultaneously supplying current to the portion of the plurality of strings that are in the same one of the plurality of bars.

24. (Original) The method of Claim 22, further comprising simultaneously supplying current to a first string located in a first bar and a second string located in a second bar.

25. (Original) The method of Claim 22, further comprising:

generating a random number;

assigning a value to each of the plurality of bars; and

simultaneously supplying current to the portion of the plurality of strings on one of the plurality of bars based on the random number.

26. (Original) The method of Claim 16, further comprising:

supplying current to a first portion of the plurality of strings according to the firing order, wherein the first portion of the plurality of strings includes solid state lighting devices configured to emit light in a first dominant wavelength; and

supplying current to a second portion of the plurality of strings according to the firing order after supplying current to the first portion of the plurality of strings, wherein the second portion of the plurality of strings includes solid state lighting devices configured to emit light in a second dominant wavelength.

27. (Original) The method of Claim 16, wherein defining is further based on a dominant wavelength of light emitted by the solid state lighting devices in the first string.

28. (Original) The method of Claim 16, further comprising simultaneously supplying current to a first string including solid state lighting devices configured to emit light in a first dominant wavelength and a second string including solid state lighting devices configured to emit light in a second dominant wavelength.

29. (Original) The method of Claim 16, further comprising:

determining the firing order that supplies current to a first string of the plurality of strings and a second string of the plurality of strings; and

defining the second string based on a dominant wavelength emitted by the solid state lighting devices in the first string and a relative position of the first string.

30. (Original) The method of Claim 16, comprising determining the firing order using a numerical technique.

31. (Original) The method of Claim 30, further comprising:

generating a random number;

assigning a value to each of the plurality of strings; and

supplying current to one of the plurality of strings based on the random number.

32. (Original) The method of Claim 30, wherein the numerical technique comprises performing a non-linear calculation.

33. (Original) The method of Claim 16, wherein the firing order comprises a deterministic order based on at least one rule.

34. (Original) A system for controlling a solid state lighting panel including a plurality of strings of solid state lighting devices that are arranged to extend across the panel in a first direction and are positioned adjacent one another in a second direction and that are supplied current by a plurality of current drivers, the system comprising:

a sequence generator that generates a firing sequence for firing the plurality of strings; and

a controller that provides control signals, responsive to the sequence generator, to the plurality of current drivers.

35. (Original) The system of Claim 34, wherein the sequence generator comprises a deterministic algorithm that determines a location of a subsequently fired string based on a location of at least one previously fired string.

36. (Original) The system of Claim 34, wherein the sequence generator comprises an algorithm that generates a sequence to fire a first string having a plurality of solid state lighting devices that emit light in a first dominant wavelength and a second string having a

plurality of solid state lighting devices that emit light in a second dominant wavelength, wherein the second string is fired after the first string.

37. (Original) The system of Claim 34, wherein the sequence generator comprises an algorithm that generates a sequence to simultaneously fire a first string having a plurality of solid state lighting devices that emit light in a first dominant wavelength and a second string having a plurality of solid state lighting devices that emit light in a second dominant wavelength.

38. (Original) The system of Claim 34, wherein the sequence generator generates a random sequence of firing.

39. (Original) The system of Claim 34, further comprising a plurality of bars that include portions of the plurality of strings, wherein the plurality of bars extend across the panel in the first direction and are positioned adjacent one another in the second direction.

40. (Original) The system of Claim 39, wherein the firing sequence is configured to simultaneously fire a first portion of the plurality of strings and then simultaneously fire a second portion of the plurality of strings and wherein the first portion is located on a first bar and the second portion is located on a second bar.

41. (Original) The system of Claim 39, wherein the firing sequence is configured to simultaneously fire a first string on a first bar and a second string on a second bar.

42. (Original) The system of Claim 41, wherein the first string includes solid state lighting devices that emit light in a first dominant wavelength and the second string includes solid state lighting devices that emit light in a second dominant wavelength.

43. (Original) The system of Claim 34, further comprising:

a first portion of the plurality of strings including solid state lighting devices that emit light in a first dominant wavelength; and

a second portion of the plurality of strings including solid state lighting devices that emit light in a second dominant wavelength;

wherein each of the plurality of bars includes at least one string of the first portion of the plurality of strings and at least one string of the second portion of the plurality of strings.

44. (Original) The system of Claim 43, wherein the firing sequence is operative to cause the first portion of strings to fire in a first sequence and to then to cause the second portion of strings to fire in the first sequence.

45. (Original) The system of Claim 34, wherein the plurality of drivers comprise a polyphase power supply configured to a supply a plurality of temporally shifted drive currents to a plurality of groups of the plurality of strings.

46. (Original) A method for controlling a solid state lighting panel including a plurality of strings of solid state lighting devices configured to extend from a first edge of the panel to a second edge of the panel in substantially adjacent positions relative to one another, the method comprising supplying a plurality of pulsed drive currents to a plurality of groups of the plurality of strings.

47. (Original) The method of Claim 46, wherein each group of the plurality of groups comprises one of the plurality of strings and wherein one of the plurality of pulsed drive currents is provided for each of the plurality of strings by one of a plurality of phase drivers.

48. (Original) The method of Claim 47, further comprising receiving a synchronizing signal from a display controller configured to control a refresh rate of display pixels.

49. (Original) The method of Claim 46, further comprising synchronizing the plurality of drive currents with a cycles of a periodic operation of a display panel.

50. (Original) The method of Claim 49, wherein the periodic operation comprises refreshing pixels and wherein the display panel comprises an LCD display panel.

51. (Original) A lighting panel system, comprising:

a lighting panel including a plurality of strings of solid state lighting devices arranged across the panel in a first direction and positioned at intervals in a second direction that is substantially orthogonal to the first direction;

a current supply circuit configured to selectively supply a plurality of on-state drive currents to the plurality of strings responsive to a plurality of control signals;

a control system configured to selectively provide control signals to the current supply circuit to selectively drive the plurality of strings, the control system further including firing logic configured to determine a firing order of the plurality of strings; and

wherein the firing logic is configured to drive the plurality of strings in a spatially non-adjacent, non-sequential firing order and/or to drive the plurality of strings at different times for at least a subset of the plurality of strings.

52. (Original) The system of Claim 51, wherein the firing logic is further configured to drive the plurality of strings and/or portions thereof at least partially based on the spatial relationship between the plurality of strings and or portions thereof.

53. (Original) The system of Claim 51, wherein the firing logic comprises rule-based logic configured to generate a non-spatially sequential firing order.

54. (Original) The system of Claim 53, wherein the rule-based logic further comprises a rule that a second string fired after a first string is non-adjacent the first string.

55. (Original) The system of Claim 53, wherein the rule-based logic further comprises a rule that if first string is fired simultaneously with a second string, then the first string is non-adjacent the second string.

REMARKS

Applicants appreciate the thorough examination of the present application as evidenced by the Office Action of January 6, 2011. Applicants respectfully submit that the pending claims are in condition for allowance for at least the reasons discussed herein.

Claims 1, 16, 34, 46 and 51 Are Patentable Over Yen

Claims 1-55 stand rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 7,724,220 to Yen et al. ("Yen"). (Office Action, page 2.)

As an initial matter, Applicants note that the Office Action concludes that the prior art date of the reference is determined under the provisions of §102(e) prior to the amendment by AIPA because the changes made to §102(e) do not apply when the reference is a U.S. Patent resulting directly or indirectly from an international application filed before November 29, 2000. (Office Action, page 2.) Applicants respectfully note that the foreign application priority data corresponding to Yen appears to be Jan. 12, 2006, which is substantially after November 29, 2000. In this regard, a §102(e) priority date for Yen would be determined using the current provisions of §102(e).

Additionally, Applicants respectfully submit that Claims 1, 16, 34, 46 and 51 are patentable over Yen for at least the reason that Yen fails to disclose or suggest several of the recitations therein. For example, Claim 1 recites:

> A lighting panel system, comprising:
> **a lighting panel including a plurality of strings of solid state lighting devices** arranged across the panel in a first direction and positioned at intervals in a second direction that is substantially orthogonal to the first direction;
> **a current supply circuit configured to selectively supply a plurality of on-state drive currents to the plurality of strings** responsive to a plurality of control signals; and
> **a control system** configured to selectively provide control signals to the current supply circuit to selectively drive the plurality of strings, the control system further **including firing logic configured to determine a firing order of the plurality of strings**. (*Emphasis added.*)

Regarding Claim 1, the Office Action asserts that Yen shows a lighting panel system including a lighting panel (element 214 in fig. 2) including a plurality of strings of solid state lighting devices (RGB LED device in fig. 3). (Office Action, page 2.) Applicants respectfully disagree. Other than using solid state light emitters (LEDs), Yen appears to be entirely non-analogous art. For example, Yen appears to describe an LED current driving system 20 for an LCOS display that includes an LCOS panel that "is used to receive image data and to display image." (Yen, column 2, lines 48-49 and 61-62.) In contrast with a lighting panel, an LCOS panel includes a "micro-projection" or "micro-display" technology that uses liquid crystals instead of individual mirrors. Thus, Yen does not disclose or suggest a lighting panel, as recited in Claim 1.

Additionally, as Yen appears to describe controlling current to individual ones of the LEDs, Yen does not disclose or suggest a lighting panel including "a plurality of strings of solid state lighting devices," as recited in Claim 1. For example, Yen describes combined current sources "to stably and precisely control the current flowing through the corresponding LED, and to improve the color quality of the image." (Yen, column 2, lines 14-19.) In contrast with providing current to strings of LEDs, Yen describes that "[e]ach LED driving unit outputs a driving current to a corresponding LED." (Yen, column 3, lines 19-21.) In this regard, Yen does not disclose or suggest selectively providing current to the strings of solid state lighting devices.

Further, Yen does not disclose or suggest "a control system... including firing logic configured to determine a firing order of the plurality of strings," as recited in Claim 1. As discussed above, since Yen does not disclose providing current to strings of solid state lighting devices, then Yen necessarily does not disclose or suggest determining a firing order of strings of solid state lighting devices. Applicants respectfully submit that Claim 1 is patentable over Yen for at least the reason that Yen does not disclose or suggest several of the recitations of Claim 1, the allowance of which is respectfully requested.

Claims 16, 34, 46 and 51 are distinguishable over Yen for similar reasons as discussed above regarding Claim 1. For example, Claim 16 recites, in part "supplying a plurality of pulsed drive currents to the plurality of strings in a non-spatially-sequential firing order." As

discussed above, Yen does not disclose or suggest strings of solid state lighting devices. In this regard, Yen is wholly silent regarding a firing order of strings, much less "a non-spatially sequential firing order," as recited in Claim 16. Accordingly, Yen does not disclose of suggest several recitations of Claim 16, the allowance of which is respectfully requested.

Similarly, Claim 34 recites, in part "a solid state lighting panel including a plurality of strings of solid state lighting devices...a sequence generator that generates a firing sequence for firing the plurality of strings." As discussed above, Yen does not disclose or suggest strings of solid state lighting devices. In this regard, Yen is wholly silent regarding "a sequence generator that generates a firing sequence for firing the plurality of strings," as recited in Claim 34. Accordingly, Yen does not disclose of suggest several recitations of Claim 34, the allowance of which is respectfully requested.

Similarly, Claim 46 recites, in part "supplying a plurality of pulsed drive currents to a plurality of groups of the plurality of strings." As discussed above, Yen does not disclose or suggest strings of solid state lighting devices. The recitations of Claim 46 include even further distinctions in that the strings of solid state lighting devices are fired in groups, in contrast with individual LED drivers in Yen. In this regard, Yen is wholly silent regarding "supplying a plurality of pulsed drive currents to a plurality of groups of the plurality of strings," as recited in Claim 46. Accordingly, Yen does not disclose of suggest several recitations of Claim 46, the allowance of which is respectfully requested.

Similarly, Claim 51 includes multiple recitations similar to those discussed above regarding Claims 1, 16, 34 and 46 and is patentable over Yen for at least the same reasons, the allowance of which is respectfully requested.

Dependent Claims are Patentable

Applicants traverse the rejection of the dependent claims as each of these claims depends from a base claim that is believed to be in condition for allowance. Additionally, several of the claims are separately patentable over the cited art. For example, Claim 2 recites "rule-based logic operative to generate a non-spatially-sequential firing order." For at least the same reasons discussed above regarding Claim 34, Yen does not disclose or suggest non-

spatially-sequential firing order. Although Yen does describe that the three LEDs 13, 14, 15 can be conducted sequentially, such sequence is wholly unrelated to relative spatial properties among the LEDs much less strings of LEDs. As such, dependent Claim 2 is separately patentable over Yen, the allowance of which is respectfully requested. Additionally, Claims 3 and 4 depend from Claim 2 and include additional recitations corresponding to the rule-based logic recited in Claim 2. As such, dependent Claims 3 and 4 are separately patentable over Yen, the allowance of which is respectfully requested. Claim 52 includes similar recitations as discussed above regarding Claim 2 and thus is separately patentable over Yen for at least the same reasons.

Additionally, dependent Claim 5 recites, in part "a plurality of bars that include portions of the plurality of strings." The Office Action does not allege and Yen does not disclose or suggest that ones of the LEDs described therein are arranged in and/or include a plurality of bars that include the plurality of strings. Accordingly, dependent Claim 5 is separately patentable over Yen, the allowance of which is respectfully requested. Additionally, Claims 6-9 depend from Claim 5 and include additional recitations corresponding to the plurality of bars recited in Claim 5. As such, dependent Claims 6-9 are separately patentable over Yen, the allowance of which is respectfully requested. Claims 22-25 and 39-41 include similar recitations as discussed above regarding Claims 5 and 6-9 and thus are separately patentable over Yen for at least the same reasons.

Additionally, dependent Claim 15 recites, in part "wherein the control system is configured to receive a synchronizing signal from a display controller configured to control a display and wherein the firing order is synchronized with periodic operations of the display." The recitations of dependent Claim 15 further emphasize the non-analogous nature of Yen relative to Applicants' invention. For example, as discussed above, Yen appears to describe a LCOS display. As such, Yen cannot reasonably be interpreted to receive a synchronizing signal from display controller to synchronize the firing order with the periodic operations of the display since Yen appears to be describing the display itself. Accordingly, dependent Claim 15 is separately patentable over Yen, the allowance of which is respectfully requested.

Additionally, Claims 47-49 include similar recitations as discussed above regarding Claim 15 and thus are separately patentable over Yen for at least the same reasons. Yet further, dependent Claim 50 depends from Claim 49 and recites that the display panel comprises an LCD display panel, a technology that is wholly distinct and superfluous relative to the LCOS display described in Yen. Accordingly, Claim 50 is separately patentable over Yen, the allowance of which is respectfully requested.

Regarding the remaining dependent claims, Applicants do not believe that it is necessary to argue the allowability of each dependent claim individually. Applicants do not necessarily concur with the interpretation of these claims, nor with the bases for rejection set forth in the Office Action. Applicants therefore reserve the right to address the patentability of these claims individually as necessary in the future.

CONCLUSION

Applicants respectfully submit that pending claims are in condition for allowance, which is respectfully requested in due course. Favorable reconsideration of this application is respectfully requested. If any informal matters arise, the Examiner is encouraged to contact the undersigned by telephone at (919) 854-1400.

Respectfully submitted,

Timothy J. Wall
Registration No. 50,743

Myers Bigel Sibley & Sajovec, P.A.
P. O. Box 37428
Raleigh, North Carolina 27627
Telephone: (919) 854-1400
Facsimile: (919) 854-1401
Customer No. 65106

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EFS ID:	9825380
Application Number:	11745713
International Application Number:	
Confirmation Number:	1290
Title of Invention:	Systems and Methods for Controlling a Solid State Lighting Panel
First Named Inventor/Applicant Name:	John K. Roberts
Customer Number:	65106
Filer:	Timothy Jennings Wall/Audra Wooten
Filer Authorized By:	Timothy Jennings Wall
Attorney Docket Number:	5308-703
Receipt Date:	06-APR-2011
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Application Type:	Utility under 35 USC 111(a)

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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		Response.pdf	1532849 ac0b3d6fc81e70bc6ea1fb5ec6104008834d bf7a	yes	17

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Amendment/Req. Reconsideration-After Non-Final Reject	1	1
	Claims	2	12
	Applicant Arguments/Remarks Made in an Amendment	13	17
Warnings:			
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PATENT APPLICATION FEE DETERMINATION RECORD

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Application or Docket Number	Filing Date	☐ To be Mailed
11/745,713	05/08/2007	

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY ☐ RATE ($)	SMALL ENTITY ☐ FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
			TOTAL			TOTAL	

* If the difference in column 1 is less than zero, enter "0" in column 2.

APPLICATION AS AMENDED – PART II

AMENDMENT 04/06/2011	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 55	Minus	** 55	= 0	X $ =		OR	X $52=	0
Independent (37 CFR 1.16(h))	* 5	Minus	***5	= 0	X $ =		OR	X $220=	0
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0

AMENDMENT	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

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** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

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ART UNIT	PAPER NUMBER
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DATE MAILED: 07/11/2011

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/745,713	05/08/2007	John K. Roberts	5308-703	1290

TITLE OF INVENTION: SYSTEMS AND METHODS FOR CONTROLLING A SOLID STATE LIGHTING PANEL

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	10/11/2011

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

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II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

Petitioner Hisense USA Corporation
Exhibit 1004 - Page 341 of 373

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

65106 7590 07/11/2011
MYERS BIGEL SIBLEY & SAJOVEC, P.A.
P.O. BOX 37428
RALEIGH, NC 27627

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/745,713	05/08/2007	John K. Roberts	5308-703	1290

TITLE OF INVENTION: SYSTEMS AND METHODS FOR CONTROLLING A SOLID STATE LIGHTING PANEL

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	10/11/2011

EXAMINER	ART UNIT	CLASS-SUBCLASS
PATEL, NITIN	2629	345-102000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
❑ Issue Fee
❑ Publication Fee (No small entity discount permitted)
❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
❑ A check is enclosed.
❑ Payment by credit card. Form PTO-2038 is attached.
❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
❑ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
❑ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Petitioner Hisense USA Corporation
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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/745,713	05/08/2007	John K. Roberts	5308-703	1290

65106 7590 07/11/2011

MYERS BIGEL SIBLEY & SAJOVEC, P.A.
P.O. BOX 37428
RALEIGH, NC 27627

EXAMINER	
PATEL, NITIN	

ART UNIT	PAPER NUMBER
2629	

DATE MAILED: 07/11/2011

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 751 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 751 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

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Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No.	Applicant(s)	
	11/745,713	ROBERTS ET AL.	
	Examiner	Art Unit	
	NITIN PATEL	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *4/6/2011*.

2. ☒ The allowed claim(s) is/are *1-55*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 3/16/2011
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

/Nitin Patel/
Primary Examiner, Art Unit 2629

Petitioner Hisense USA Corporation
Exhibit 1004 - Page 345 of 373

Issue Classification

Application/Control No.	Applicant(s)/Patent Under Reexamination
11745713	ROBERTS ET AL.
Examiner	**Art Unit**
NITIN PATEL	2629

ORIGINAL		INTERNATIONAL CLASSIFICATION														
CLASS	SUBCLASS	CLAIMED									NON-CLAIMED					
345	102	G	0	9	G	3 / 36 (2006.01)										

CROSS REFERENCE(S)					
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				

☒ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
	1		17		33		49								
	2		18		34		50								
	3		19		35		51								
	4		20		36		52								
	5		21		37		53								
	6		22		38		54								
	7		23		39		55								
	8		24		40										
	9		25		41										
	10		26		42										
	11		27		43										
	12		28		44										
	13		29		45										
	14		30		46										
	15		31		47										
	16		32		48										

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	55	
/NITIN PATEL/ Primary Examiner.Art Unit 2629	06/30/2011	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	8, 9

Petitioner Hisense USA Corporation
Exhibit 1004 - Page 346 of 373

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11745713	ROBERTS ET AL.
	Examiner	**Art Unit**
	Nitin Patel	2629

SEARCHED

Class	Subclass	Date	Examiner
345	72, 88, 102, 204	6/17/2011	NP

SEARCH NOTES

Search Notes	Date	Examiner
EAST SEARCH, keywords and subclasses, uspat, uspgpubs, epo, jpo, derwent, ibm; inventor name search;	6/17/2011	NP

INTERFERENCE SEARCH

Class	Subclass	Date	Examiner
UPDATED	ABOVE CLASS AND SUBCLASS	6/17/2011	NP
PGPUB	DATABASE	6/17/2011	NP

	/DAVID L LEWIS/ Primary Examiner.Art Unit 2629

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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P.O. Box 1450
Alexandria, Virginia 22313-1450
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BIB DATA SHEET

CONFIRMATION NO. 1290

SERIAL NUMBER	FILING or 371(c) DATE RULE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
11/745,713	05/08/2007	345	2629	5308-703

APPLICANTS

John K. Roberts, Grand Rapids, MI;
Keith J. Vadas, Lowell, MI;

**** CONTINUING DATA ***************************

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****

05/31/2007

Foreign Priority claimed ☐ Yes ☑ No 35 USC 119(a-d) conditions met ☐ Yes ☑ No Verified and Acknowledged /NITIN PATEL/ Examiner's Signature	☐ Met after Allowance Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		MI	12	55	5

ADDRESS

MYERS BIGEL SIBLEY & SAJOVEC, P.A.
P.O. BOX 37428
RALEIGH, NC 27627
UNITED STATES

TITLE

Systems and Methods for Controlling a Solid State Lighting Panel

FILING FEE RECEIVED		
3280	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	1060890	led or (light near2 emit $4 near2 (diode or element or display))or lightnin$4 near2 device $2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/03 03:48
S2	189679	S1 same (current or voltage)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/03 03:49
S3	33224	S2 same (on or off or idle)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/03 03:49
S4	5185	S3 same control$4 near3 (line$2 or signal $2)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/03 03:50
S5	905	S4 and "345"/$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/03 03:51
S6	796	S5 and @ay<="2008"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/03 03:53
S7	300601	current with (on or off)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/03 05:50
S8	474621	(current or voltage) with (on or off)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/03 05:50
S9	155254	"1" same S8	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/03 05:50

S10	19908	S9 same (order or sequenc$4 or pattern or non near2 adjac$4 or non near2 sequent$4 or sequent$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/03 05:52
S11	8840	S10 same (control$4 or cpu or mpu or processor or microprocessor)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/03 05:53
S12	72	S11 and 345/102,204.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/03 05:53
S13	1060890	led or (light near2 emit $4 near2 (diode or element or display))or lightnin$4 near2 device $2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/03 05:55
S14	19138	S13 same S8	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/03 05:55
S15	2574	S14 same (order or sequenc$4 or pattern or non near2 adjac$4 or non near2 sequent$4 or sequent$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/03 05:55
S16	1424	S15 same (control$4 or cpu or mpu or processor or microprocessor)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/03 05:55
S17	232	S16 and "345"/$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/03 05:56
S18	1193856	led or light near2 emit $4 near2 (element or diode) or solid near2 state near3 (device or diode or element)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/17 11:28
S19	28639	S18 same current near2 (supply or control$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/17 11:29

S20	18595	S19 same (on or off or idle$4 or emit$4 or static or dynamic)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/17 11:30
S21	2227	S20 same (order or sequen$4 or parti$4 or cluster or chunk$2)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/17 11:31
S22	475	S21 and "345"/$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/17 11:31
S23	1388608	non near2 order or non near2 sequent$6 or random$4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/17 13:08
S24	18980	S23 same S18	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/17 13:08
S25	59	S24 and 345/102.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/17 13:09
S26	14336	(non near2 sequential $4 or iregular$$ or nonsequential$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/17 13:21
S27	1470	S26 with (element or device or diode)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/17 13:21
S28	86	S27 and "345"/$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/17 13:21
S29	104121	(strings or panle or rows)with (light or bulb or tube or solid near2 state or diode or led)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/17 15:36

S30	10513	S29 same current	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/17 15:36
S31	28	S30 same (non-spatially or nonspatially or non near2 adjacent$4 or irregular$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/17 15:42
S32	1151	S30 same (non-spatially or nonspatially or non near2 adjacent$4 or irregular$4or alternat $4)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/17 15:43
S33	1173	S30 same (non-spatially or nonspatially or non near2 adjacent$4 or irregular$4 or alternat $4)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/17 15:43
S34	120	S33 and "345"/$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/17 15:43
S35	1036	control$5 with (non-sequential$4 or nonsequential$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/17 22:01
S36	32	S35 same (light or led or tube or bulb or solid near2 state)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/17 22:02
S37	370	control$5 same (non-sequential$4 or nonsequential$4)same (led or light or devcices or elements or cluster or chunks or group$4 or bulb or tube)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/17 22:10
S38	36	S37 and "345"/$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/17 22:11
S39	257	control$5 same (non-sequential$4 or nonsequential$4).clm.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/17 22:14

S40	0	S39 and 345/4.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/17 22:15
S41	20	S39 and "345"/$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/06/17 22:15

EAST Search History (Interference)

<This search history is empty>

6/30/2011 7:10:07 PM
H:\EAST\Workspaces\11745713.wsp

INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Complete if Known	
				Application Number	11/745,713
				Filing Date	May 8, 2007
				First Named Inventor	John K. Roberts
				Art Unit	2629
(use as many sheets as necessary)				Examiner Name	Patel, Nitin
Sheet	C1	of	C1	Attorney Docket Number	5308-703

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No.	Document Number Number-Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1.	US- 2006/139954 A1	06-29-2006	Kobori Tomoki et al.	
		US-			
		US-			
		US-			
		US-			

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No.	Foreign Patent Document Country Code, Number, Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T
	2.	Communication pursuant to Article 94(3) EPC dated February 7, 2011 corresponding to European Application No. 08 743 161.5; 6 pages	

Examiner Signature	/Nitin Patel/	Date Considered	06/30/2011

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /NP/

Petitioner Hisense USA Corporation
Exhibit 1004 - Page 354 of 373

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

65106 7590 07/11/2011
MYERS BIGEL SIBLEY & SAJOVEC, P.A.
P.O. BOX 37428
RALEIGH, NC 27627

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/745,713	05/08/2007	John K. Roberts	5308-703	1290

TITLE OF INVENTION: SYSTEMS AND METHODS FOR CONTROLLING A SOLID STATE LIGHTING PANEL

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	10/11/2011

EXAMINER	ART UNIT	CLASS-SUBCLASS
PATEL, NITIN	2629	345-102000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Myers Bigel Sibley & Sajovec
2
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: Cree, Inc.

(B) RESIDENCE: (CITY and STATE OR COUNTRY): Durham, NC

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
- ☒ Issue Fee
- ☒ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 50-0220 (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
- ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date 9-21-11

Typed or printed name Timothy J. Wall Registration No. 50,743

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Petitioner Hisense USA Corporation
Exhibit 1004 - Page 355 of 373

Electronic Patent Application Fee Transmittal

Application Number:	11745713
Filing Date:	08-May-2007
Title of Invention:	SYSTEMS AND METHODS FOR CONTROLLING A SOLID STATE LIGHTING PANEL
First Named Inventor/Applicant Name:	John K. Roberts
Filer:	Timothy Jennings Wall/Michele McMahan
Attorney Docket Number:	5308-703

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl issue fee	1501	1	1510	1510
Publ. Fee- early, voluntary, or normal	1504	1	300	300

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**1810**

Electronic Acknowledgement Receipt

EFS ID:	10996611
Application Number:	11745713
International Application Number:	
Confirmation Number:	1290
Title of Invention:	SYSTEMS AND METHODS FOR CONTROLLING A SOLID STATE LIGHTING PANEL
First Named Inventor/Applicant Name:	John K. Roberts
Customer Number:	65106
Filer:	Timothy Jennings Wall/Michele McMahan
Filer Authorized By:	Timothy Jennings Wall
Attorney Docket Number:	5308-703
Receipt Date:	21-SEP-2011
Filing Date:	08-MAY-2007
Time Stamp:	09:52:06
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$1810
RAM confirmation Number	14678
Deposit Account	500220
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part/.zip	Pages (if appl.)

Petitioner Hisense USA Corporation
Exhibit 1004 - Page 358 of 373

1	Issue Fee Payment (PTO-85B)	5308-703-Issue-Fee.pdf	154159 e3c477b368b79ab9cf0387ba9e2928f8deefd8c5	no	1
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	31981 9e87843e569e86bbab2d2efac15a2c119534d4d8	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	186140	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/745,713	11/01/2011	8049709	5308-703	1290

65106 7590 10/12/2011

MYERS BIGEL SIBLEY & SAJOVEC, P.A.
P.O. BOX 37428
RALEIGH, NC 27627

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 1211 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

John K. Roberts, Grand Rapids, MI;
Keith J. Vadas, Lowell, MI;

PTO/AIA/80 (07-12)
Approved for use through 11/30/2014. OMB 0651-0035
U.S. Patent and Trademark Office; U.S DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO

I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(c).

I hereby appoint:

■ Practitioners associated with Customer Number: 146366

OR

☐ Practitioner(s) named below (if more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number	Name	Registration Number

As attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications assigned only to the undersigned according to the USPTO assignment records or assignments documents attached to this form in accordance with 37 CFR 3.73(c).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(c) to:

■ The address associated with Customer Number: 146366

OR

☐	Firm or Individual Name			
	Address			
	City		State	Zip
	Country			
	Telephone		Email	

Assignee Name and Address: Cree, Inc.
4600 Silicon Drive
Durham, NC 27703

A copy of this form, together with a statement under 37 CFR 3.73(c) (Form PTO/AIA/96 or equivalent) is required to be Filed in each application in which this form is used. The statement under 37 CFR 3.73(c) may be completed by one of The practitioners appointed in this form, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE of Assignee of Record

The individual whose signature and title is supplied below is authorized to act on behalf of the assignee

Signature	Julio Garceran	Date	2/13/17
Name	Julio Garceran	Telephone	919-407-5343
Title	Chief Intellectual Property Counsel - Cree, inc.		

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/AIA/96 (08-12)
Approved for use through 01/31/2013. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

STATEMENT UNDER 37 CFR 3.73(c)

Applicant/Patent Owner: Cree, Inc.

Application No./Patent No.: 11/745,713 Filed/Issue Date: 5/8/2007

Titled: SYSTEMS AND METHODS FOR CONTROLLING A SOLID STATE LIGHTING PANEL

Cree, Inc., a Corporation

(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose **one** of options 1, 2, 3 or 4 below):

1. ☑ The assignee of the entire right, title, and interest.

2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):

   ☐ The extent (by percentage) of its ownership interest is _____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.

   ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (*e.g.*, bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose **one** of options A or B below):

A. ☑ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel 019555, Frame 0719, or for which a copy thereof is attached.

B. ☐ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

   1. From: _____ To: _____

      The document was recorded in the United States Patent and Trademark Office at

      Reel _____, Frame _____, or for which a copy thereof is attached.

   2. From: _____ To: _____

      The document was recorded in the United States Patent and Trademark Office at

      Reel _____, Frame _____, or for which a copy thereof is attached.

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/AIA/96 (08-12)
Approved for use through 01/31/2013. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

STATEMENT UNDER 37 CFR 3.73(c)

3. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

4. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

5. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

6. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☑ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Timothy J. Wall/	2/20/2017
Signature	Date
Timothy J. Wall	50,743
Printed or Typed Name	Title or Registration Number

Electronic Acknowledgement Receipt

EFS ID:	28405161
Application Number:	11745713
International Application Number:	
Confirmation Number:	1290
Title of Invention:	SYSTEMS AND METHODS FOR CONTROLLING A SOLID STATE LIGHTING PANEL
First Named Inventor/Applicant Name:	John K. Roberts
Customer Number:	65106
Filer:	Timothy Jennings Wall/Cheryl Ramey
Filer Authorized By:	Timothy Jennings Wall
Attorney Docket Number:	5308-703
Receipt Date:	20-FEB-2017
Filing Date:	08-MAY-2007
Time Stamp:	16:25:48
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		5308_000703_373_Statement_and_POA.pdf	444920 ddddd183d030446ef466de7dbdb10ed3b7dfe1e3	yes	3

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Power of Attorney	3	3
	Assignee showing of ownership per 37 CFR 3.73	1	2
Warnings:			
Information:			
	Total Files Size (in bytes):	444920	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
11/745,713	05/08/2007	John K. Roberts	5308-703

CONFIRMATION NO. 1290

146366
Sage Patent Group/Cree
PO BOX 30789
RALEIGH, NC 27622-0789

POA ACCEPTANCE LETTER

OC00000089444019

Date Mailed: 02/24/2017

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 02/20/2017.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/dtdinh/

Petitioner Hisense USA Corporation
Exhibit 1004 - Page 366 of 373

Doc Code: PA..
Document Description: Power of Attorney

PTO/AIA/82B (07-13)
Approved for use through 03/31/2021. OMB 0651-0035
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number	Filing Date

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)

☑ I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above: 158862

OR

☐ I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

Please recognize or change the correspondence address for the application identified in the attached transmittal letter or the boxes above to:

☑ The address associated with the above-mentioned Customer Number

OR

☐ The address associated with Customer Number:

OR

☐ Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Email			

I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

IDEAL INDUSTRIES LIGHTING LLC

☐ Inventor or Joint Inventor (title not required below)

☐ Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)

☑ Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)

☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature		Date (Optional)	September 19, 2019
Name	Craig K. Atwater		
Title	Senior Vice President and General Manager		

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.

☑ Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Acknowledgement Receipt

EFS ID:	37940668
Application Number:	11745713
International Application Number:	
Confirmation Number:	1290
Title of Invention:	SYSTEMS AND METHODS FOR CONTROLLING A SOLID STATE LIGHTING PANEL
First Named Inventor/Applicant Name:	John K. Roberts
Customer Number:	146366
Filer:	Dennis J. Williamson/Meredith DeRosa
Filer Authorized By:	Dennis J. Williamson
Attorney Docket Number:	4308-703
Receipt Date:	05-DEC-2019
Filing Date:	08-MAY-2007
Time Stamp:	14:24:45
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		1535-703.pdf	160266 88965334346f736edea6be04cde0df0abff23152	yes	3

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Assignee showing of ownership per 37 CFR 3.73	1	2
	Power of Attorney	3	3
Warnings:			
Information:			
	Total Files Size (in bytes):	160266	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

1535-703

PTO/AIA/96 (08-12)
Approved for use through 01/31/2013. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

STATEMENT UNDER 37 CFR 3.73(c)

Applicant/Patent Owner: Ideal Industries Lighting LLC

Application No./Patent No.: 11/745,713 Filed/Issue Date: 05-08-2007

Titled: SYSTEMS AND METHODS FOR CONTROLLING A SOLID STATE LIGHTING PANEL

Ideal Industries Lighting LLC, a corporation

(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose **one** of options 1, 2, 3 or 4 below):

1. [✓] The assignee of the entire right, title, and interest.

2. [ ] An assignee of less than the entire right, title, and interest (check applicable box):

   [ ] The extent (by percentage) of its ownership interest is _____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.

   [ ] There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. [ ] The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. [ ] The recipient, via a court proceeding or the like (*e.g.*, bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose **one** of options A or B below):

A. [ ] An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.

B. [✓] A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: John K. Roberts, Keith J. Vadas To: Cree, Inc.

   The document was recorded in the United States Patent and Trademark Office at

   Reel 019555, Frame 0719, or for which a copy thereof is attached.

2. From: Cree, Inc. To: Ideal Industries Lighting LLC

   The document was recorded in the United States Patent and Trademark Office at

   Reel 049902, Frame 0679, or for which a copy thereof is attached.

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/AIA/96 (08-12)
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STATEMENT UNDER 37 CFR 3.73(c)

3. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

4. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

5. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

6. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☐ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

Signature	Date: 12/5/2019
Dennis J. Williamson	32,338
Printed or Typed Name	Title or Registration Number

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
11/745,713	05/08/2007	John K. Roberts	4308-703

CONFIRMATION NO. 1290

158862
MYERS BIGEL, P.A.
P.O. BOX 37428
RALEIGH, NC 27627

POA ACCEPTANCE LETTER

OC000000113199853

Date Mailed: 12/09/2019

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 12/05/2019.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/zretta/

UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
11/745,713	05/08/2007	John K. Roberts	4308-703

CONFIRMATION NO. 1290

POWER OF ATTORNEY NOTICE

146366
Sage Patent Group/Cree
PO BOX 30789
RALEIGH, NC 27622-0789

OC000000113199834

Date Mailed: 12/09/2019

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 12/05/2019.

- The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/zretta/