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Miguel Tarver
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APPLICANTS

OROR HALABMI TEL AVIV ISRAEL YORAN

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Yes JAL

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Yes JAL

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71058 U.S. PTO

08/912243



08/15/97

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PATENT APPLICATION TRANSMITTAL LETTER

ATTORNEY DOCKET NO.
SC0034WI

TO THE HONORABLE COMMISSIONER OF PATENTS & TRADEMARKS:
Transmitted herewith for filing is the patent application of:

Dror HALAHMI and Yoram SALANT

For: "A METHOD FOR DIGITAL SIGNAL PROCESSING, DSP, MOBILE
COMMUNICATION AND AUDIO-DEVICE"

Enclosed are:

- ☒ 2 sheet(s) of drawings and 25 page(s) of specification
☒ A Declaration and Power of Attorney
☒ A Disclosure Statement and Cited Art

CLAIMS AS FILED

FOR	NUMBER FILED	NUMBER EXTRA	RATE	FEE
TOTAL CLAIM(S)	10	0	X \$22.00	\$0.00
INDEPENDENT CLAIM(S)	4-3	1	X \$80.00	\$80.00
MULTIPLE DEPENDENT CLAIM(S)		0	X \$260.00	\$0.00
BASIC FEE				\$770.00
TOTAL FILING FEE				\$850.00

- ☒ Please charge deposit account No. 13-4773 in the amount of \$850.00.
- ☒ The Commissioner is hereby authorized to charge any fees under 37 CFR 1.16 and 1.17 which may be required during the entire pendency of this application, or credit any overpayment, to deposit account No. 13-4773.

This sheet is submitted in triplicate.

21 July 1997
(date-spell month)

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30,261

REG. NO.

PATENT APPLICATION TRANSMITTAL LETTER		ATTORNEY DOCKET NUMBER SC0034WI
TO THE HONORABLE COMMISSIONER OF PATENTS & TRADEMARKS: Transmitted herewith for filing is the patent application of: Dror HALAHMI and Yoram SALANT For: "A METHOD FOR DIGITAL SIGNAL PROCESSING, DSP, MOBILE COMMUNICATION AND AUDIO-DEVICE" Enclosed are: ☒ 2 sheet(s) of drawings and 25 page(s) of specification ☒ A Declaration and Power of Attorney ☒ A Disclosure Statement and Cited Art		
CLAIMS AS FILED		
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CLAIM(S)	10	0
INDEPENDENT CLAIM(S)	4-3	1
MULTIPLE DEPENDENT CLAIM(S)		0
BASIC FEE	\$770.00	
TOTAL FILING FEE	\$850.00	
☒ Please charge deposit account No. 13-4773 in the amount of \$850.00. ☒ The Commissioner is hereby authorized to charge any fees under 37 CFR 1.16 and 1.17 which may be required during the entire pendency of this application, or credit any overpayment, to deposit account No. 13-4773. This sheet is submitted in triplicate.		
<u>21 Feb 1997</u> (date-spell month)	 ATTORNEY OF RECORD Robert M. Handy MOTOROLA, INC. Intellectual Property Department - 505 Barton Springs Road Suite 500, MD: TX07/F4 Austin, Texas 78704 Telephone No.: (512) 505-8910 Facsimile No.: (512) 505-8912 30,261 REG. NO.	

PATENT
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: : Date: July 21, 1997

Dror HALAHMI, et al. :

Serial No.: :

Filed: : Art Unit:

For: **A Method for Digital Signal Processing, DSP, Mobile
Communication and Audio-Device**

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CHANGE OF NAME AND NUMBER FOR TELEPHONE CALLS
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APPOINTMENT OF ASSOCIATE ATTORNEYS AND AGENTS

HONORABLE COMMISSIONER OF PATENTS AND TRADEMARKS,
SIR:

With respect to the above-identified patent application:

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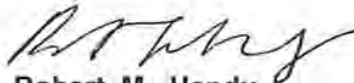
The undersigned, attorney of record in the above-entitled application, hereby appoints:

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of Motorola, Inc., Intellectual property Department, 505 Barton Springs Road, Suite 500, MD: TX07/F4, Austin, Texas 78704, as associate attorney or agent with full power to transact all business in the Patent and Trademark Office connected therewith.

Respectfully submitted,

Dror HALAHMI, et al.



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/td

**A Method for Digital Signal Processing, DSP, Mobile Communication and
Audio-Device**

5

Field of Invention

This invention relates generally to a field of digital signal processing, and more particularly to digital signal processing operations requiring memory access to consecutive data words.

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Background of the Invention

15 In the digital signal processing technology typically one or more analog signals which are representative of some real physical property are filtered or undergo some other kind of arithmetic evaluation or transformation. For this purpose, it is necessary to sample the incoming analog signals. For each analog signal this results in a continuous stream of digital samples. Furthermore, it is known in the art to store such separate sequences of
20 digital samples separately from each other in different memories or in the same memory but separated address spaces. An example for micro processors which incorporate these principles is the DSP 56300 family of 24-bit digital signal processors which are commercially available from Motorola, Inc.

25

Digital signal processors are applied in virtually all fields of technology and apparatuses. One application is to replace the functionality of an analog device, such as an analog filter, by a digital filter which allows for an enhanced quality and more compact design. Other fields are for digital
30 audio devices, such as compact disc players or digital audio tapes, as well as communication devices, such as mobile telephones or radios. Such applications typically require a high processor throughput, either because of the high band width of the sample's analog signal or because of the complexity of the digital transformations to be carried out on the sampled
35 signal or a combination of both.

A need therefore exists to increase the performance of digital signal processors.

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Summary of the Invention

The underlying problem of the invention is substantially met by applying the features laid down in the independent claims. Preferred embodiments are given in the dependent claims.

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The invention is advantageous in that it allows to significantly improve the processing performance of a digital signal processor by adding only minimal hardware.

15

According to a preferred embodiment of the invention, four data accesses can be carried out in a single processing cycle. The corresponding data sequences can be processed in a finite impulse response type processing step which typically involves data processing in multiply-accumulate loops. Preferably two multiplication units are used, each of which can multiply two of the data words provided in each cycle. The results of the two multiplications is added and accumulated.

20

If the architecture of a digital signal processor designed in accordance with the principles of the invention is pipelined, this allows two multiply-accumulate operations in one cycle without increasing the clock frequency. As a consequence, such a digital signal processor is also advantageous with respect to power dissipation. This is particularly beneficial for battery powered applications, since the minimized power dissipation of the digital signal processor allows longer intervals between recharging the battery.

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30

Furthermore, it is particularly advantageous that only a single address generation unit is required even though at least two data words can be accessed from each memory device or address region in a memory device. Thus, by using only a single address generation unit, up to four data words can be accessed in a single cycle.

35

Brief Description of the Drawings

FIG.1 is a schematic block diagram of a first embodiment of a digital device including a digital signal processor designed in accordance with the principles of the invention; and

Fig. 2 is a flow diagram which illustrates one embodiment of the method of the invention.

Detailed Description of the Preferred Embodiments

With reference to FIG.1 a digital device 10 which incorporates a digital signal processor 12 is explained in detail. The digital device 10 can be for example and not intended to be limiting a digital audio device, such as a compact disc player, or a digital communication device, such as a mobile telephone or radio.

In the later case typically an analog signal is received from an antenna of the digital device 10. Such a signal is shown as signal 14 in FIG. 1. The signal is fed into analog-digital converter 16. The samples of the signal 14 delivered by the analog-digital converter 16 are inputted via data line 18 into a memory 20. The memory 20 has a storage array 22. The sampled data words which are inputted via data line 18 to the memory 20 are stored in the address space of the storage array 22 in consecutive order. This means that the first data word, which is inputted into the storage array 22, is stored at the lowest order address and that consecutive further data words are stored at increasing addresses. Other address schemes are also possible such as starting with the highest address and filling up the storage array 22 at consecutive storage locations of decreasing addresses.

The address space of the storage array 22 is logically divided into even and odd addresses. The same applies analogously for memory 24 which has a storage array 26. The memory 24 can serve to store data words which are representative of samples of another input signal or of filter coefficients to be used in the digital signal processing of the signal 14.

In the case of a digital audio device, such as a compact disc player, the signal 14 provided by the laser beam which scans the rotating compact disc is already digital information so that no analog-digital converter 16 is required. Instead the signal 14 is directly inputted into memory 20 without a need for analog to digital conversion.

For the addressing of the memories 20 and 24, the digital signal processor 12 has address generation unit 28 which is coupled via control line 30 to control logic 32. The control logic 32 is also coupled via the control lines 34 and 36 to the memories 20 and 24, respectively. Control line 38 couples the control logic 32 to register file 40 whereas control line 42 couples the control logic 32 to a multiply accumulator 44. The multiply accumulator 44 has multipliers 46 and 48 having their outputs connected to an adder-accumulator 50.

The address generation unit 28 has a register 52 for storage of an address for the memory 20 and a register 54 for storage of an address for the memory 24. Further the address generation unit 28 has registers 56 and 58 to specify the amount of change required for the addresses stored in register 52 and 54, respectively, for the next processing interval. In registers 60 and 61 the mode in which the address generation unit 28 operates is specified.

The address generation unit 28 is connected by address buses 62 and 63 to the memories 20 and 24, respectively. Both of the memories 20 and 24 have two data busses for outputting data: memory 20 is connected by data busses 64 and 66 to the register file 40 whereas memory 24 is connected by data busses 68 and 70 to the register file 40. The data busses 66 and 70 are also coupled to buffers 72 and 74, respectively. The buffers 72 and 74 are connected to the register file 40 by the data busses 76 and 78.

The register file 40 has registers 80, 82, 84 and 86. Each of these registers can store one data word. The registers 80 and 82 are coupled via data lines 88 and 90 to the multiplier 46. Likewise the registers 84 and 86 are coupled via data lines 92 and 94 to the multiplier 48.

The result of a digital signal processing operation is outputted by adder 50 to digital-analog converter 92. The resulting analog signal 94 is the result of the digital signal processing operation carried out on the signal 14.

- 5 In operation the control logic 32 controls the processing of the incoming signal 14 according to the required digital signal processing operation.

In order to initialize the required digital signal processing operation the start addresses for both the memory 20 and the memory 24 have to be
10 specified. For simplicity, the memory 20 and 24 will be referred to as X MEM and Y MEM, respectively, whereas the registers 52 and 54 will be referred to as RX and RY, respectively. The registers 80, 82, 84, and 86 of the register file 40 will be referred to as X0, X0', Y0 and Y0', respectively.

- 15 The start address for the required data sequence to be outputted from the X MEM is programmed in the register RX by the control logic 32 via control line 30. The start address for the required data sequence from the Y MEM is programmed in the register RY also by means of the control logic 32 via control line 30.

20 The control logic 32 checks the start address stored in the RX whether it is an even or an odd address. If the start address for the X MEM is even, the parameter CHANGE X which is stored in the register 56 is set to a value of 2 - provided that the addressing mode is incremental.

- 25 If the start address for the X MEM is odd, the value of the parameter CHANGE X is set to be equal to the value 1 by the control logic 32 via control line 30 - again provided that the addressing mode is incremental. The same check is carried out for the start address stored in the RY. If the start
30 address for the Y MEM is even, the parameter CHANGE Y stored in the register 58 is set to be equal to the value of 2; if the start address for the Y MEM is odd, the value of CHANGE Y is set to be equal to the value of 1 - analogous to the process carried out for the start address for the X MEM.

- 35 The parameters MODE X and MODE Y are stored in the registers 60 and 61, respectively. The parameters MODE X and MODE Y specify the addressing mode for the X MEM and the Y MEM, respectively. If, for

example, the value of MODE X is equal to 0, this means that the data words are to be outputted from the X MEM in increasing address order, so that after each iteration the address stored in the RX is incremented by the value specified by the parameter CHANGE X. Likewise, if the value of
5 MODE X is logically 1, this means that the address stored in X is decremented after each processing interval by the value as specified by CHANGE X. The same applies analogously to the setting of the parameter MODE Y in the register 61. Both parameters MODE X and MODE Y are set via the control line 30 by the control logic 32.

10 Thus, during an initialization interval the start addresses for the sequence of data words to be outputted from X MEM and Y MEM are programmed in the registers RX and RY, respectively, as well as the corresponding parameters CHANGE X, CHANGE Y, MODE X and MODE Y.

15 If, for example, the start address for the X MEM is even and MODE X equals logically 0 (incrementing address mode), the data word which comes next after the data word having the start address stored in RX has an address which is incremented by 1 with respect to the first data word in
20 the sequence. As a consequence, the second data word in the X MEM sequence has an address which is odd and thus differs only in its least significant bit from the start address stored in RX. Since both address words are required for the processing, it is signaled to the X MEM via control line 34 to output both the data word stored on the start address
25 stored in RX and the consecutive data word being stored on the address next to the start address which differs only in its least significant bit in response to the reception of an address via the address bus 62. In other words: If the control line 34 is raised, the least significant bit line of the address bus 62 becomes a "Don't care" bit, since both data words having an
30 address matching all the higher order address bits will be outputted by the X MEM. As a consequence two data words are outputted from X MEM during one initialization interval, so that for the next interval the address has to be increased by 2 in order to output the consecutive two data words of the required sequence from the X MEM.

35 If the start address RX is odd and the address mode X is logically 0 (incrementing address mode), this means that there is no data word in the



required output sequence which has an address that differs only in its least significant bit from the start address of the sequence stored in RX. As a consequence, the control line 34 is dropped by the control logic 32 to logically 0, so that the X MEM only outputs the data word being stored on exactly the start address stored in RX, but no other data word. Since only one data word is outputted in this alternative first initialization interval, the value of CHANGE X is set to be equal 1, so that for the next initialization interval the value of the address stored in RX is incremented only by 1. After this increment operation has been carried out, the address stored in RX no longer is odd, but even. As a consequence the control line 34 is raised, so that in response to the reception of the even address stored in RX via the address bus 62 again the least significant address bit becomes a "Don't care" bit position, so that the X MEM outputs two data words at a time in the alternative second initialization interval. As a consequence in this alternative case two initialization intervals are required as opposed to the first case considered here in which only one initialization interval is required before the main processing loop can be entered.

Whether the first or the second case is present can be determined according to the following table

	LSB	MODE
CASE 1	0	incremental (+)
	1	decremental (-)
CASE 2	0	decremental (-)
	1	incremental (+)

where the column LSB stands for the least significant bit of the address stored in RX and MODE for the addressing mode.

25

The logic of the above table can advantageously be implemented within control logic 32 by a XOR gate which is not shown in the drawing. If one input terminal of the XOR gate receives the logical value of the parameter MODE X and the other input terminal receives the least significant bit of the address which is stored in the RX, the resulting output of the XOR gate is logically 1 to indicate the first case and logically 0 in the second case.

Thus, the output of such a XOR gate within control logic 32 can serve to determine which of the two cases mentioned above is present.

5 The same applies analogously for the Y MEM and the corresponding programming of the address generation unit and issuing of control signals via control line 36 to the Y depending on whether the least significant bit of the address bus 63 is relevant or "Don't care". Also the control logic 32 can comprise an additional XOR gate which has MODE Y and the least significant address bit of the address stored in RY as input signals. Again
10 the output of this additional XOR gate is 1 in the first case and 0 in the second case as described above.

If the first case is present, for both the X MEM and the Y MEM the total time period required for the initialization is just one initialization interval.
15 If either for the X MEM or the Y MEM or for both the second case is present, an additional initialization interval is required as described above.

If the first case is present for the X MEM, the two data words which are outputted from X MEM in the same initialization interval are transferred
20 via the data busses 64 and 66, respectively, to the registers X0 and X0'. If the same applies for the Y MEM, correspondingly two output data words are transferred via the data busses 68 and 70 and stored in the registers Y0 and Y0'.

25 If, however, the case 2 is present for the Y MEM, only one data word is outputted in the first initialization interval from Y MEM. In the consecutive second initialization interval two data words are outputted only one of which is to be stored in the register file 40. The other output data word is intercepted in the buffer 74 by control logic 32. The same applies
30 analogously if the second case is present for the X MEM, so that one of the data words which are outputted in the second initialization interval is intercepted by buffer 72 which is also controlled by the control logic 32.

After the initialization phase is completed, each register X0, X0', Y0, Y0' of
35 the register file 40 carries one data word. Now the operation of the multiply accumulator 44 can start in the main processing loop. In the main processing loop the required digital signal processing operation is carried

out by means of the multiplier accumulator 44. Typically, such digital signal processing operations are finite impulse response signal processing operations. When the main processing loop starts in the first processing interval, the data stored in registers X0 and X0' is transferred via the data lines 88 and 90, respectively, to the multiplier 46. Likewise the data stored in registers Y0 and Y0' are transferred via the data lines 92 and 94, respectively, to the multiplier 48. The output of the respective multiplications is transferred to adder-accumulator 50 in which the two outputs of the multipliers 46 and 48 as well as the value stored in the accumulator are added and stored back into the accumulator. The presence of two multipliers 46 and 48 has the advantage that two multiplications can be carried out within the same time interval. After the completion of such two parallel multiplications another set of four data words is required to be transferred to the multipliers 46 and 48. This is accomplished by the control logic 32:

If the case 1 was present in the initialization interval, each output operation of two data words results in an increase of the addressed store in RX by 2, so that in the consecutive time interval the consecutive two data words of the required sequence are outputted and stored in the appropriate registers of register file 40. If, however, the case 2 was present during the initialization interval, one of the required data words is already present in the buffer 72 or 74 - depending on whether the second case was present for the X MEM or the Y MEM. Carrying out the next processing cycle in the main loop, the data word stored in the buffer 72 or 74 is transferred to the register file 40 to be stored in the appropriate register. Also after the completion of the initialization interval in the second case, the value of CHANGE X or CHANGE Y has been set to 2, so that the value of the address stored in RX or RY is changed by 2 after each output operation. As a consequence one of the data words of the pair of data words outputted by the corresponding memory is transferred to the register file 40 and the other one stored as a replacement in the buffer 72 or 74 depending on which one of the memories X MEM or Y MEM the second case applies. Therefore, also in the second case one multiplication and accumulation operation can be carried out in the main processing loop with four operands due to this pipelined structure.

As a result the throughput of the digital signal processor 12 is doubled as compared to a prior art signal processor having just one multiplication unit. This is accomplished by adding only a minimal number of hardware elements.

5

In the following, a digital processing operation according to formula (1)

TeX (1)
$$a = \sum_{i=0..5; j=1..6} (x[i] \cdot y[j]),$$

10 is described by way of example, where $x[i]$ refers to the data word stored in the X MEM on the address i and $y[j]$ refers to data word stored in Y MEM on the address j . According to the formula (1), a total of six multiplications and summations has to be carried out in order to calculate the value of a . In order to prepare the execution of the digital signal processing operation
15 according to formula (1) the digital signal processor 12 has to be initialized by the control logic 32. For this purpose the control logic 32 receives input commands from a user or from a program control at its input 92. By the instruction (i1)

20 (i1) move # 0, RX

the address $i = 0$ is moved to the register RX as a start address for the sequence of data words to be outputted from X MEM. Likewise the instruction (i2)

25 (i2) move # 1, RY

causes the control logic 32 to move the address 1 into the register RY as a start address of the sequence of data words to be outputted from Y MEM.

30 The instruction (i3)

(i3) clr a

causes the control logic 32 to issue a control signal via control line 42 to
35 clear the value a , which is stored in the accumulator of the adder-accumulator 50. Next the instruction (i4)

//

(i4) move 2 x: (RX)+, X0 y: (RY)+, Y0

is received by the control logic 32 at its input 92. This instruction means that the data word being stored on the address of the register RX is to be moved from the X MEM to the register X0. Further, as it is indicated by (RX) + the addressing mode is incrementing, so that the parameter MODE X is set to logically 1. Further, the fact that X0 is part of the instruction (i4) indicates that the consecutive data word of the incremented starting address is to be moved to X0'. The same applies analogously for the part y: (RY)+, Y0 of the instruction i4 which relates to the data words in the Y MEM.

As the start address for the sequence of data words to be outputted from X MEM in the register RX is even, the case 1 is present for X MEM, so that the least significant bits of the addresses outputted by address generation unit 28 via the address bus 62 is "Don't care". As a consequence - as described above in more detail - the two data words x[0] and x[1] are outputted concurrently from the X MEM via the data busses 64 and 66, respectively. The data word of the address 0 which is x[0] is stored in the register X0 and the data word of the consecutive incremented address 1 which is x[1] is stored in the register X0' under control of the control logic 32 via control line 38. This happens in the first initialization interval.

In parallel to the addressing, outputting and storing of the two first data words of the X MEM data sequence, the Y MEM is also accessed. Since the address stored in the register RY is 1, an odd address is the starting address of the Y MEM output sequence, so that the second case is present. This means that only the first data word of the Y MEM sequence can be addressed, outputted and stored in the register file during the first initialization interval because the least significant bit position of the address stored in RY is relevant.

After the data word Y[1] has been outputted from the Y MEM the parameter CHANGE Y stored in the register 58 is set to be equal 1, so that the address stored in RY is incremented by 1. As a consequence in the following second initialization interval the two consecutive data words y[2] and y [3] are outputted. The address word y[2] is stored in the register Y0'

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in the register file 40 - the data word y[1] has already been stored in the previous first initialization interval in the register Y0 as specified by the instruction i(4). Since at this time the data word y[3] is not yet needed, it is stored in the buffer 74 for usage in a consecutive processing interval.

5

After the buffering of the data word y[3], the second initialization interval is completed, so that the main processing loop can be started. The parameter CHANGE Y will also be set two 2 because in the following always two data words are to be outputted at a time from Y MEM:

10

The main processing loop can be started by the control logic 32 after an instruction (i5)

(i5) mac2 X0, Y0, a X: (RX)+, X) Y: (Y)+, Y0

15

has been received. According to the instruction i(5), the data words of the registers X0 and Y0 have to be multiplied and accumulated as well as the data words stored in registers X0' and Y0'. The corresponding multiplications are carried out by multipliers 46 and 48, and the accumulation by the adder-accumulator 50. Further, the instruction i(5) specifies that after each processing step the address stored in register RX has to be incremented by 2 as well as the address stored in register RY. This is made clear by the symbols (RX) + and (RY) +, respectively, instruction i(5). Also it is specified that the first data word having the lower address is stored in the register X0 and Y0, respectively, and the higher order address data word in the registers X0' and Y0', respectively. If instead of the "+" - sign a "-" -sign would be present, this would have the opposite meaning.

25

30 When the instruction i(5) is carried out the first time by the multiply accumulator 44, the following over all calculation is performed:

$$a := a + x[0] * y[1] + x[1] * y[2]$$

35 This means that in one processing interval two consecutive data words of both the X and the Y MEM sequence are processed. Since at this stage both parameters CHANGE X and CHANGE Y have been set to be equal 2, in the

12

next processing step the next pair of two data words of each sequence is processed - in other words :

$$a := a + x[2] * y[3] + x[3] * y[4].$$

5

After a further increase of both the addresses stored in RX and RY, the next processing interval already yields the final result for a:

$$a := a + x[4] * y[5] + x[5] * y[6].$$

10

Since the case 1 is present for the X MEM (the X start address is odd), all the data words from X MEM are directly transferred to the register file 40. As opposed to this, the data words y[3] and y[5] are sequentially buffered in the buffer 74 prior to their transfer to register file 40.

15

In the following with reference to Fig. 2 one embodiment of the method of the invention is described in greater detail.:

- 20 In step 100 digital samples are stored in the X and Y Memory. In step 102 the processing of the samples stored in the X Memory is initialized; likewise the processing of the samples stored in the Y Memory is initialized in step 104. In the following the initialization processing is only explained in detail with respect to the samples stored in the X Memory, but not for the
- 25 Y samples, since both processes carried out in step 102 and step 104 in parallel are analogous.

For the initialization first the start address of the sequence of data words to be outputted is moved into the register RX of the address generation unit (AGU). This is done in step 106. In step 108 the address mode for the X

30 Memory is set to be either incrementing or decrementing depending on whether the output sequence starts on top or on the bottom of the address range.

- 35 In step 110 it is checked whether the start address of the sequence to be outputted from the X Memory is even. If the address stored in the RX register is even, this means that the least significant bit of this address is

"Don't care". When the X Memory is accessed by an even start address in step 110, this results in an output of two data words from the X Memory having the same address bits except the least significant address bit.

- 5 If the start address stored in the register RX is odd, this means that case 2 is present, since at the same time the address mode is incrementing. This means that the least significant bit of the start address is relevant, so that only a data word of the start address stored in RX is outputted from the X Memory in step 114. In step 116 the address stored in RX is incremented by 1, so that an even address stored in RX results. As a consequence the least significant bit of the new address stored in RX becomes "Don't care". As a consequence in the next initialization step 118 the memory outputs the next two consecutive data words of the output sequence from the X Memory whereby the two data words have an address which differs only in the least significant bit from each other. Since the data word having the higher address is not yet required at this stage, it is buffered in step 120 for later use. In step 122 the address stored in the register RX is incremented by 2 according to the selected incrementing address mode irrespective of whether case 1 or case 2 is present.

- 20 After the initialization phase two data words from the output sequence of the X Memory as well as from the Y Memory are available for processing. As a consequence the main processing 124 is started. In step 126 the available X and Y Memory output data is accessed from the register file and processed according to the required digital signal processing operation. At the same time two consecutive data words in the required output sequence from the X Memory are addressed and outputted from the X Memory. If the case 1 is present, this is done in step 130 by getting two more data words from the X Memory whereby the two more data words have an address which differs only in its least significant bit.

- If the case 2 is present the lower order address data word is fetched from the buffer and the higher order data word from X Memory, the further data word which is also outputted from the X Memory at the same time and which has an address which is incremented by 1 with respect to the higher order data word is buffered to replace the previous lower order address data word. This is done in step 132. In step 134, the address stored in the register

RX is incremented by 2 again, according to the applicable addressing mode. The operations carried out in step 128 are carried out the same way for the Y Memory in step 136. Step 136 is carried out in parallel to the steps 126 and 128. After the steps 126, 128, and 136 have been carried out, a further
5 iteration 138 of the main loop is initiated so that the step 124 is repeated for a number of times required to complete the digital signal processing operation as specified.

Typically the initialization intervals as well as the processing intervals
10 referred to above are carried out in one machine cycle only. If a pipelined implementation is chosen, this means that in each machine cycle two accumulate-multiply operations can be carried out.

ACCEPTED

1/1

We Claim:

1. A method for carrying out a digital signal processing operation, said
5 operation requiring consecutive data words for each processing interval,
said data words being stored in a memory device, said method comprising
the steps of:
- in a first initialization interval:
- 10 - addressing a first data word by a first address, said first data word having
a consecutive second data word having a second address;
- in a case 1: if said second address differs only in its least significant bit
15 from said first data address,
- outputting said first and second data words from said memory device;
storing said first and second data words in a register file;
- 20 - in a case 2: if said case 1 is not present,
- outputting said first data word; storing said first data word in said register
file; changing said first address by one;
- 25 in a second initialization interval:
- addressing said second data word by said changed first address;
outputting said second data word and a consecutive third data word;
storing said second data word in said register file and storing said
30 third data word in a buffer register;

17

in a first processing interval:

5 accessing said data words stored in said register file for carrying out a digital signal processing step;

changing said first address by two;

10 addressing two further consecutive data words by said changed first address;

in said case 1:

storing said further consecutive data words in said register file;

15 in said case 2:

storing said data word of said buffer register in said register file;

storing one of said further consecutive data words in said register file;

storing the other one of said further consecutive data words in said buffer;

20 carrying out as many of said processing intervals as required to complete said digital signal processing operation.

15

2. The method according to claim 1 said digital signal processing operation requiring at least two sequences of said consecutive data words, said data words of different sequences being stored in memory devices which are
5 separately addressable, said method being carried out for each of said sequences, whereby said register file is a common file for all data words.
3. The method according to claim 2 said digital signal processing step being a multiply accumulate processing step.
- 10 4. The method according to claim 1 whereby either a decrementing or incrementing address mode is used, said method further comprising the step of XORing said address mode and the least significant bit of said first address in order to determine said case 2.
- 15 5. A digital signal processor comprising
- a digital signal processing core;
- 20 a memory device for storing a sequence of consecutive data words;
- an address generation unit for generating addresses for said memory device;
- 25 an output buffer register for said memory devices;
- a register file coupled to said memory device, to said output buffer register and to said digital signal processing core;
- 30 a control logic coupled to said memory device, to said address generation unit, to said digital signal processing core and to said output buffer register, said control logic being adapted to control input/output operations for said data words into/from said register file according to the following control scheme:

14

in a first initialization interval:

for a first address of a first data word of said sequence which is generated
5 by said address generation unit, said first data word having a consecutive
second data word of a second address:

- in a case 1: if said second address differs only in its least significant bit
10 from said first data address,

causing said memory device to output said first and second data words;
inputting said first and second data words into said register file;

- in a case 2: if said case 1 is not present,
15 causing said memory device to output said first data word; inputting said
first data word into said register file; causing said address generation unit
to change said first address by one;

20 in a second initialization interval:

causing said address generation unit to address said second data
word by said changed first address; causing said memory device to
output said second data word and a consecutive third data word;
25 inputting said second data word into said register file and storing
said third data word in a buffer register;

in a first processing interval:

30 causing said register file to output said data words to said digital signal
processing core for carrying out a digital signal processing step;

causing the address generation unit to change said first address by two;

35 causing said addressing unit to address two further consecutive data words
by said changed first address;

in said case 1:

inputting said further consecutive data words into said register file;

in said case 2:

- 5 inputting said data word of said buffer register into said register file;
inputting one of said further consecutive data words into said register file;
storing the other one of said further consecutive data words in said buffer;

- 10 carrying out as many of said processing intervals as required to complete
said digital signal processing operation.

- 15 6. The digital signal processor according to claim 5 said digital signal
processing core being adapted to process at least two sequences of
consecutive data words at a time, said digital signal processor further
comprising one of said memory devices for each said sequence of
consecutive data words, said register file being adapted to receive data
words originating from any of said memory devices under control of said
control logic according to said control scheme applied to each one of said
memory devices.

- 20 7. The digital signal processor according to claim 6 having two of said
memory devices, said digital signal processing core comprising two
multipliers being coupled to said register file, each of said multipliers
receiving two data words per processing interval from said register file.

- 25 8. The digital signal processor according to claim 5 whereby said control
logic causes said address generation unit to operate either in a
decrementing or incrementing address mode, said control logic further
comprising a XOR logic gate having said address mode and the least
30 significant bit of said first address as inputs, an output signal of said XOR
gate determining whether said case 1 or said case 2 is present.

9. A communication device comprising sender and/or receiver means to send and/or receive a signal and a signal processor for digitally processing said signal, said signal processor comprising

5

a digital signal processing core;

a memory device for storing a sequence of consecutive data words being representative of said signal;

10

an address generation unit for generating addresses for said memory device;

an output buffer register for said memory devices;

15

a register file coupled to said memory device, to said output buffer register and to said digital signal processing core;

a control logic coupled to said memory device, to said address generation unit, to said digital signal processing core and to said output buffer register, said control logic being adapted to control input/output operations for said data words into/from said register file according to the following control scheme:

20

25 in a first initialization interval:

for a first address of a first data word of said sequence which is generated by said address generation unit, said first data word having a consecutive second data word of a second address:

30

- in a case 1: if said second address differs only in its least significant bit from said first data address,

causing said memory device to output said first and second data words;
35 inputting said first and second data words into said register file;

- in a case 2: if said case 1 is not present,

causing said memory device to output said first data word; inputting said first data word into said register file; causing said address generation unit to change said first address by one;

5

in a second initialization interval:

causing said address generation unit to address said second data word by said changed first address; causing said memory device to output said second data word and a consecutive third data word; inputting said second data word into said register file and storing said third data word in a buffer register;

10

in a first processing interval:

15

causing said register file to output said data words to said digital signal processing core for carrying out a digital signal processing step;

causing the address generation unit to change said first address by two;

20

causing said addressing unit to address two further consecutive data words by said changed first address;

in said case 1:

inputting said further consecutive data words into said register file;

in said case 2:

inputting said data word of said buffer register into said register file;

inputting one of said further consecutive data words into said register file;

storing the other one of said further consecutive data words in said buffer;

30

carrying out as many of said processing intervals as required to complete said digital signal processing operation.

35

10. A digital audio device comprising means for recording and/or reproducing an audio signal and a signal processor for digitally processing said signal, said signal processor comprising

5 a digital signal processing core;

a memory device for storing a sequence of consecutive data words being representative of said signal;

10 an address generation unit for generating addresses for said memory device;

an output buffer register for said memory devices;

15 a register file coupled to said memory device, to said output buffer register and to said digital signal processing core;

a control logic coupled to said memory device, to said address generation unit, to said digital signal processing core and to said output buffer

20 register, said control logic being adapted to control input/output operations for said data words into/from said register file according to the following control scheme:

in a first initialization interval:

25

for a first address of a first data word of said sequence which is generated by said address generation unit, said first data word having a consecutive second data word of a second address:

30 - in a case 1: if said second address differs only in its least significant bit from said first data address,

causing said memory device to output said first and second data words; inputting said first and second data words into said register file;

35

- in a case 2: if said case 1 is not present,



causing said memory device to output said first data word; inputting said first data word into said register file; causing said address generation unit to change said first address by one;

5 in a second initialization interval:

causing said address generation unit to address said second data word by said changed first address; causing said memory device to output said second data word and a consecutive third data word;
10 inputting said second data word into said register file and storing said third data word in a buffer register;

in a first processing interval:

15 causing said register file to output said data words to said digital signal processing core for carrying out a digital signal processing step;

causing the address generation unit to change said first address by two;

20 causing said addressing unit to address two further consecutive data words by said changed first address;

in said case 1:

inputting said further consecutive data words into said register file;

25

in said case 2:

inputting said data word of said buffer register into said register file;
inputting one of said further consecutive data words into said register file;
storing the other one of said further consecutive data words in said buffer;

30

carrying out as many of said processing intervals as required to complete said digital signal processing operation.

25

**A Method for Digital Signal Processing, DSP, Mobile Communication and
Audio-Device**

5

Abstract of the Disclosure

The invention relates to a digital signal processor in which two multiply
accumulate operations are carried out in one machine cycle. Only one
address generation unit is required for addressing two data words of both
10 the X and Y memories, since in the main processing loop the least
significant address bit is considered as "Don't care", so that an access
operation to the memory results in two output data words at a time.

COMBINED DECLARATION AND POWER OF ATTORNEY
FOR PATENT APPLICATION

Attorney Docket SC0034WI

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled **A METHOD FOR DIGITAL SIGNAL PROCESSING, DSP, MOBILE COMMUNICATION AND AUDIO-DEVICE** (Attorney Docket No. SC0034WI) the specification of which is attached hereto unless the following box is checked:

☐ was filed on _____
as Application No. _____
and was amended on _____.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119(a)-(d) of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s) Priority Claimed:

			☐ Yes	☐ No
(Number)	(Country)	(Day/Month/Year Filed)		
			☐ Yes	☐ No
(Number)	(Country)	(Day/Month/Year Filed)		

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(Application Number)	(Filing Date)
(Application Number)	(Filing Date)

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

(Application Number)	(Filing Date)	(Status - patented, pending, abandoned)
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(Application Number)	(Filing Date)	(Status - patented, pending, abandoned)
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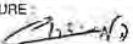
I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

ROBERT M. HANDY, Reg. No. 30,261; VINCENT B. INGRASSIA, Reg. No. 25,732; HARRY A. WOLIN, Reg. No. 32,638; MIRIAM JACKSON, Reg. No. 33,911; KEVIN B. JACKSON, Reg. No. 38,502; ROBERT D. ATKINS, Reg. No. 34,288; ROBERT F. HIGHTOWER, Reg. No. 36,163; BRUCE T. NEEL, Reg. No. 37,406; RENNIE WILLIAM DOVER, Reg. No. 36,503.

Address all telephone calls to Mr. RENNIE WILLIAM DOVER at telephone no. (602) 441-5419.

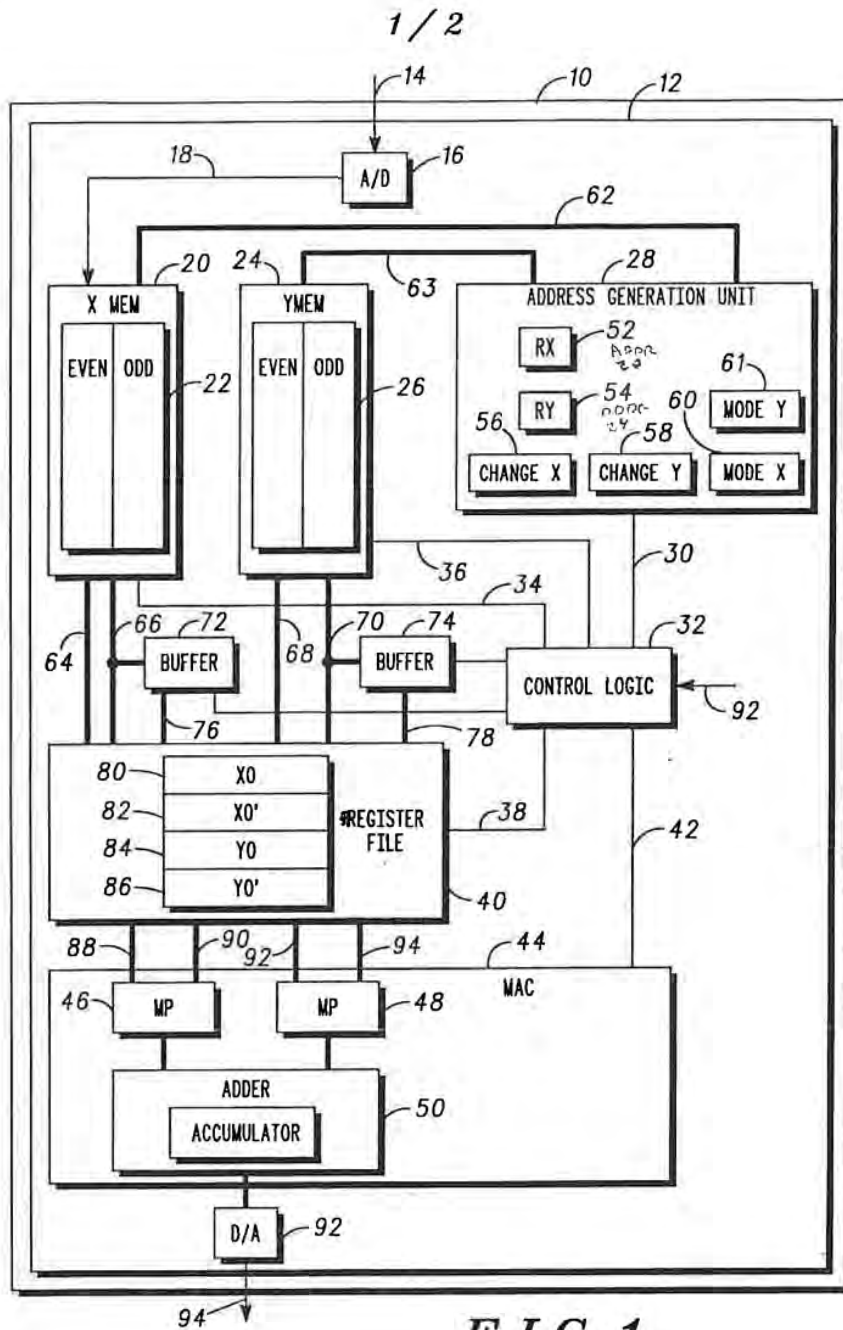
Address all correspondence to Vincent B. Ingrassia, Motorola, Inc., Intellectual Property Department - Suite R3108, P.O. Box 10219, Scottsdale, Arizona 85271-0219.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

FULL NAME OF FIRST INVENTOR Dror HALAHMI	INVENTOR'S SIGNATURE 	DATE: June 22, 1991
RESIDENCE: 6 Amirim St., Tel Aviv, Israel,		CITIZENSHIP: Israel
POST OFFICE ADDRESS Same as above		

FULL NAME OF FIRST INVENTOR Yoram SALANT	INVENTOR'S SIGNATURE 	DATE: June 22, 1991
RESIDENCE: 57 He-Beiyar St., Rosh-Haain, Israel,		CITIZENSHIP: Israel
POST OFFICE ADDRESS Same as above		

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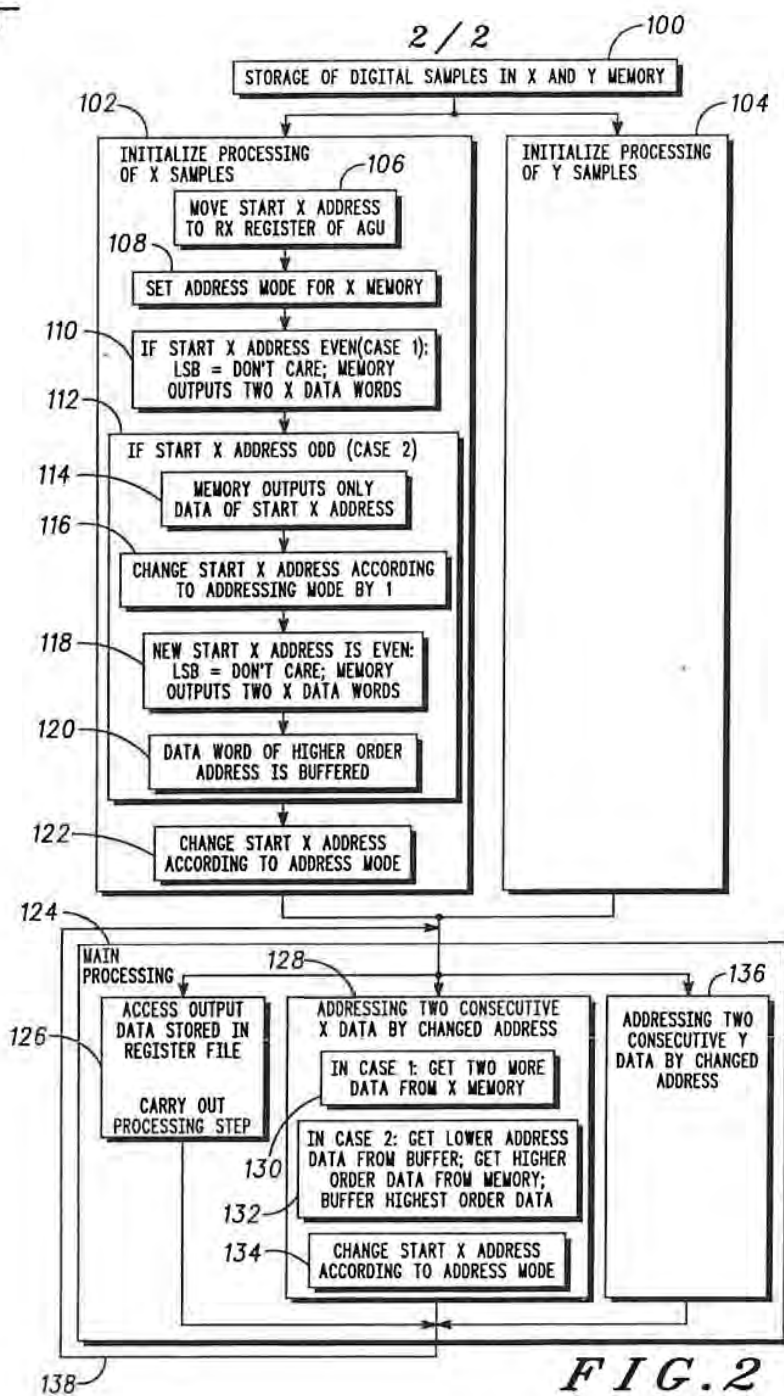


FIG. 2

#2
3-16-97
2a

PATENT
Disclosure

71058 U.S. PAT. & TM. OFF.
08/912243
08/15/97

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: : Date: 21 July , 1997

INVENTOR et al. : Dror HALAHMI et al.

Docket No.: : SC0034WI

Filed: Concurrently herewith :

For: A Method for Digital Signal Processing, DSP, Mobile
Communication and Audio-Device

DISCLOSURE STATEMENT UNDER 37 CFR 1.56

Honorable Assistant Commissioner for Patents
Washington, D.C. 20231

SIR:

It is respectfully requested that the art listed on FORM PTO-1449 be considered in the examination of the subject application and made of record therein. A copy of the listed art is enclosed herewith.

No representation is made or intended that a search has been made or that no better art than that listed is available.

Respectfully Submitted,

INVENTOR et al.

Robert M. Handy

Robert M. Handy
Attorney for Applicants
Reg. No. 30,261
(512) 505 8910

MOTOROLA, INC.
Intellectual Property Dept.
505 Barton Springs Road
Suite 500, MD:TX07/F4
Austin, Texas 78704

CHECKLIST FOR PROCESSING NEW APPLICATIONS

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D. CLAIMS (as filed)

- ☒ 1. Complete form 1360 and 875: (forms on right side of file)
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G. PTO-1556

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 - b. Excess independent claims more than 3.
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Notice of References Cited

Application No. 08/912,243	Applicant(s) Halahmi et al.
Examiner Jack Lane	Group Art Unit 2751

Page 1 of 1

U.S. PATENT DOCUMENTS

*		DOCUMENT NO.	DATE	NAME	CLASS	SUBCLASS
x	A	4,609,996	11-1986	Kummer	711	2
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(See Manual of Patent Examining Procedure, Section 707.05(a).)

[19]

[11] Patent Number: 4,609,996

[45]

- Primary Examiner—James D. Thomas
Assistant Examiner—David L. Clark

[57] ABSTRACT

A microcomputer includes a main memory system which is accessed, substantially independently, by the CPU and a subsystem, for example a video display subsystem. The memory system comprises a base memory and an optical add on expansion memory. When only the base memory is installed, consecutive locations have consecutively numbered addresses, and both the CPU and subsystem access individual locations. When both memories are installed, one has even numbered addresses and the other odd numbered addresses. With both memories installed, the CPU still accesses individual locations, but the subsystem addresses even addresses to obtain, for each access, data from the even address and the next higher odd address, thereby accessing a location in both memories. Thus the memory bandwidth for the subsystem is effectively doubled when the expansion memory is installed.

4 Claims, 6 Drawing Figures

4 Claims, 6 Drawing Figures

4 Claims, 6 Drawing Figures

4 Claims, 6 Drawing Figures

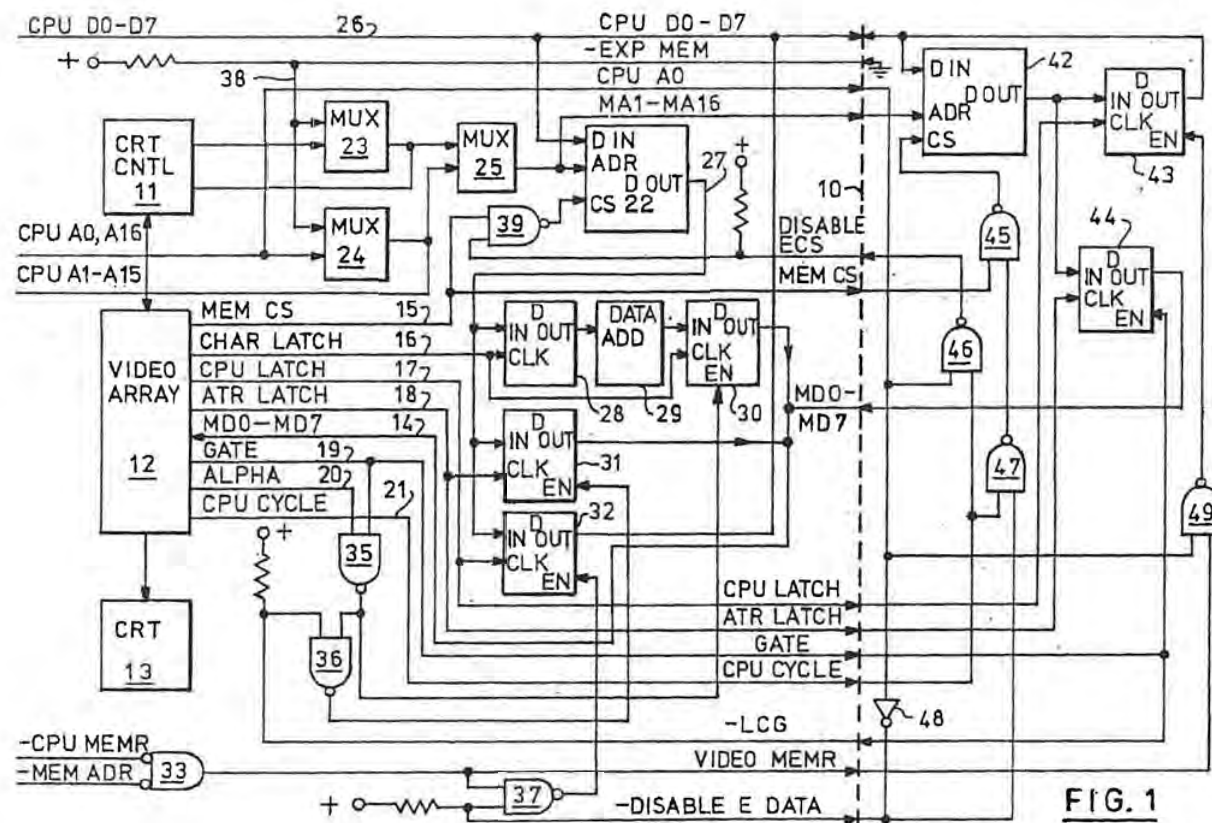
4 Claims, 6 Drawing Figures

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4 Claims, 6 Drawing Figures





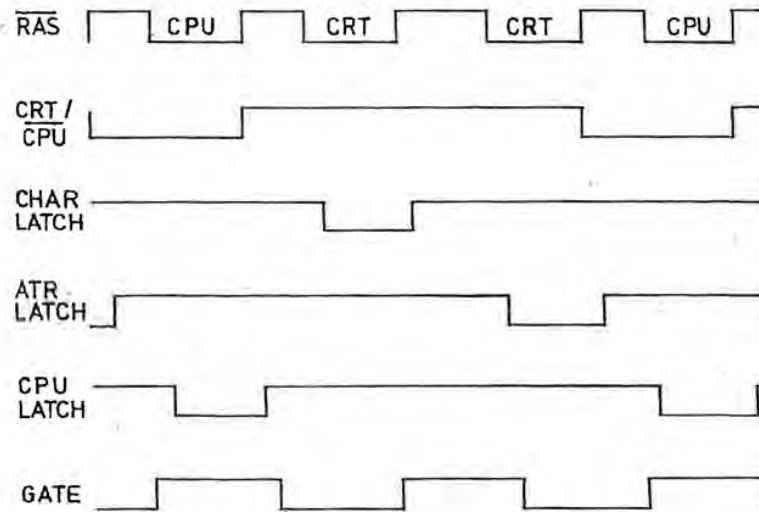


FIG. 2

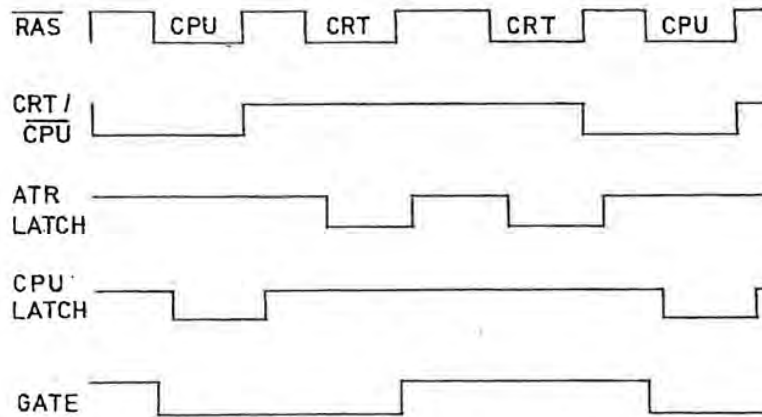


FIG. 3

MEMORY 22

F F F F
F F F E
8 0 0 3 (ATR)
8 0 0 2 (CHAR)
8 0 0 1 (ATR)
8 0 0 0 (CHAR)
0 0 0 2
0 0 0 1
0 0 0 0

FIG. 4

MEMORY 22	MEMORY 42
1 F F F E	1 F F F F
1 F F F C	1 F F F D
0 8 0 0 6 (CHAR)	0 8 0 0 7 (ATR)
0 8 0 0 4 (CHAR)	0 8 0 0 5 (ATR)
0 8 0 0 2 (CHAR)	0 8 0 0 3 (ATR)
0 8 0 0 0 (CHAR)	0 8 0 0 1 (ATR)
0 0 0 0 4	0 0 0 0 5
0 0 0 0 2	0 0 0 0 3
0 0 0 0 0	0 0 0 0 1

FIG. 5

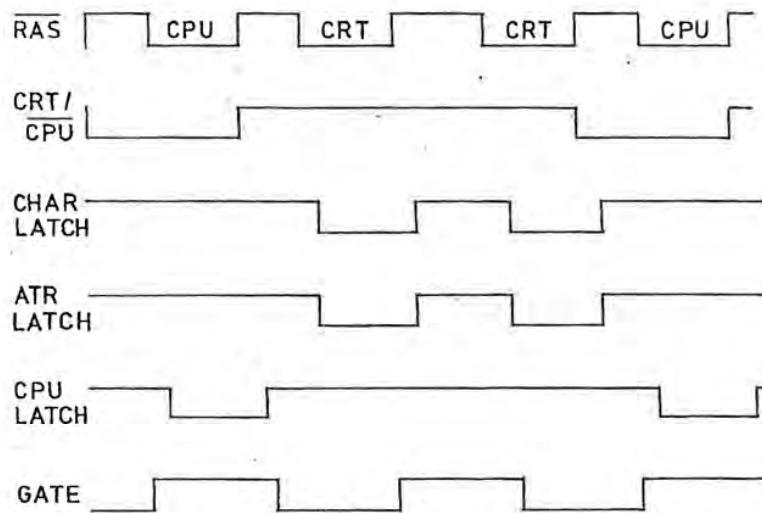


FIG. 6

MEMORY ACCESS SYSTEM FOR A COMPUTER SYSTEM ADAPTED TO ACCEPT A MEMORY EXPANSION MODULE

DESCRIPTION

1. Technical Field

The present invention relates to a memory access system for a computer system of the type which is arranged to accept a memory expansion module to increase its total memory capacity.

2. Background Art

The great majority of microcomputers at present marketed allow for main memory expansion by adding memory modules. The TI Home Computer, produced by Texas Instruments Corporation, starts with a main memory capacity of 16K bytes which can be expanded up to 52K bytes by adding expansion memory cards. The Olivetti M20 microcomputer has a basic 128K byte R.A.M. which can be expanded by a single expansion board to 512K bytes, and the VIC 20 machine, marketed by Commodore Business Machines Corporation has a basic memory of 5K bytes, which is expanded in steps up to 32K bytes. In these, as in all prior systems of which we have knowledge, this memory expansion does not require substantial revision of the memory addressing arrangements. All that happens is that the memory addresses for the added memory are added on top of the addresses for the base memory. Thus, if the base memory is of 128K bytes, then, with an expansion memory of 128K bytes, the base memory provides the addresses up to 128K and the expansion memory provides the addresses up from 128K to 512K. For this to happen, of course, the addressing scheme must allow for the extra address bit required for the expanded memory.

In microcomputer systems, and especially those employing a limited amount of memory, certain functions are limited by the bandwidth of the memory. The bandwidth is determined by the operational speed of the memory and the size of each location therein. The location size is determined by bus width of the system and the microprocessor data width. Most microcomputers use an 8 bit bus system which limits the memory location size to 8 bits. This limited bandwidth restricts the operation of some subsystems which access the memory system without direct CPU intervention. One such subsystem is a video subsystem for driving a CRT display. This operates essentially independently of the CPU to retrieve data from the memory system for display. In a microcomputer which shares its memory between CPU and video operations, the CPU accesses the memory in cycles between the video system cycles. With the requirement to share the memory with the CPU, and with 8 bit storage accesses, the video bandwidth can be severely limited, thereby limiting the display definition.

It is therefore, an object of the invention to provide, in a microcomputer system, a memory access system which, when an expansion memory is added to the base memory, automatically increases the memory bandwidth for a subsystem using the memory. In the embodiment of the invention to be described in detail hereinafter,

the subsystem is a video subsystem. It is, however, contemplated that other subsystems, such as communications subsystems, could employ the inventive features to advantage.

DISCLOSURE OF THE INVENTION

The present invention provides a memory access system for a microcomputer which is adapted to accept a memory expansion module. The microcomputer includes a subsystem which accesses the system memory substantially independently of CPU accesses. When an expansion module is fitted, the memory access system defines addresses in one of the base or expansion memories as even address and in the other as odd addresses. Then, the CPU accesses both memories by individual location therein, but the subsystem addresses a single address from which an even location from one memory and an adjacent odd location from the other memory are fetched.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of a microcomputer system showing the base memory and its access circuits and elements of its video subsystem together with details of a memory expansion module.

FIG. 2 is a waveform diagram showing signals occurring in the FIG. 1 system without the expansion module and with the video subsystem operating in an alphanumeric mode.

FIG. 3 is a waveform diagram showing signals occurring in the FIG. 1 system without the expansion module and with the video subsystem operating in a graphics mode.

FIG. 4 shows the arrangement of the base memory in the FIG. 1 system when the expansion module is not fitted.

FIG. 5 shows the arrangement of both the base and expansion memories when the expansion module is fitted.

FIG. 6 is a waveform diagram showing signals occurring in the FIG. 1 system when the expansion module is fitted.

FIG. 1 is a block diagram of the memory and video circuits of a microcomputer. A broken line 10 indicates an interface between the base circuits of the microcomputer, positioned to the left of line 10, and an expansion memory module, positioned to the right of line 10. Initially, we will consider the construction and operation of the base system, and thereafter the base system together with the expansion module will be discussed. Turning now to the base system, this comprises a CRT controller 11, which may be of the type MC6845 manufactured by Motorola Inc. This, as is well known, provides memory addresses and raster timings to display images on a CRT display. A video array 12 is coupled to the CRT controller 11 and to a CRT display 13. Array 12 is responsive to control signals from controller 11 and data signals (MDO-MD7) on a data bus 14 to develop the drive signals for the CRT display 13. In addition it generates various control signals for the system. These include a memory chip select signal

(MEM CS) on line 15, a character latch signal (CHAR LATCH) on line 16, a signal CPU LATCH on line 17, an attribute latch signal (ATR LATCH) on line 18, a GATE signal on line 19, an ALPHA signal on line 20 and a CPU CYCLE signal on line 21. These signals will be discussed in more detail later. A dynamic random access memory 22 is addressed either from controller 11 or CPU input addresses through a group of multiplexers 23 through 25. Memory 22 is coupled to receive data from the CPU on a bus 26 and to develop output data on a bus 27. Video data may be held in the memory as alphanumeric character data for conversion to display data, or directly as graphics display data, in which digits in the memory directly represent display elements. These modes of operation will hereinafter be called alpha (representing alphanumeric) and graphics modes respectively. Note the (EN) inputs to the latch circuits 28, 30, 31, 32, 43 and 44, and (CS) inputs to memories 22, 42 are responsive to low input signals.

In the alpha mode, data on bus 27 is applied through a latch circuit 28 to a character generator 29, for example, a read-only memory, which, in response to this data and CRT line scan signals (not shown) develops the display data for the respective scan lines of characters to be displayed. These signals are applied through a further latch circuit 30 to the data input bus 14 to video array 12. Latch circuits 28 and 30 are controlled by the CHAR LATCH signals over line 16 from video array 10. In addition attribute data from memory 22 is applied over bus 27 to a latch circuit 31, controlled by an ATR LATCH signal on line 18. The video array 12 includes a color palette system, the principle of which was described in an article by Peter B. Denes entitled "Computer Graphics In Color" which appeared in the Bell Laboratories Record, May 1974, at pages 139 through 146. Essentially, this comprises a plurality of CPU loadable registers which are addressed by the video data from memory 22. Each register stores data bits to provide a set of CRT color drive signals representing one color. The input video data addresses different ones of these registers to provide the required sequence of color drive signals from display. In the present system in the alpha mode, a byte of attribute data from latch 31 is applied to a multiplexer in the video array 12. Thereafter, a byte of character data from latch 30 is serialized in the video array 30. The serialized bits are then applied to control the multiplexer to provide either the upper or the lower four bits of the attribute byte therein to address the color palette registers to provide, for each bit of character data, a set of four CRT drive signals, representing three colors and an intensity.

In the graphics mode, the character generator 29 is, of course, not used. Consequently, the CHAR LATCH output on line 16 is not used, and latch circuit 30 is disabled by an output (high) from NAND gate 35. Instead, the ATR LATCH signals on line 18 and an enable signal (low) from a NAND gate 36 cause successive bytes from the memory, representing video data, to pass from latch 31 to video array 12 over bus 14. These successive bytes are combined in video array 12 to

address the color palette system to produce video drive signals for the CRT display 13.

Lastly, memory 22 is used not only as a video memory, but also the base memory for the C.P.U. In some video display operations and all other operations data is transferred from this memory back to the CPU. This is done through a latch circuit 32 in response to CPU LATCH signals from line 17 of the video array 12 and an enable signal from NAND gate 37. With this configuration, data from the memory passes through latch 32 to the CPU data bus (CPU D0-D7) 26.

FIGS. 2 and 3 show the waveforms of some of the signals generated in the system, without the memory expansion module fitted, for the alpha and the graphics modes respectively.

Referring firstly to FIG. 2, this shows the alpha mode. The first waveform is the memory row address strobe (RAS) signal. This, together with the column address strobe signals, times the addressing of dynamic random access stores. For simplicity these signals are not shown in FIG. 1, but they are generated by the gate array. The RAS signal is shown in FIG. 2 to indicate the timing of the memory read/write for CPU data and read for the CRT display data. It will be noted that there are two CRT memory cycles for each CPU cycle. The second waveform indicates the periods in which the CPU has access to the memory and those in which the CRT signals are derived. In the third line, the CHAR LATCH signal is shown indicating that in the first CRT memory cycle a character byte is read from the memory. The fourth line similarly shows that the ATR LATCH signal causes an attribute byte to be read in the second CRT memory cycle. The CPU LATCH signal in the fifth line shows the timing of CPU access to the memory. Lastly the bottom line shows the GATE signal from video array 12 which is used, together with the alpha signal, to provide the latch 30 enable input (low) from NAND circuit 35, and also latch 31 enable input (low) from NAND circuit 36. The GATE signal enables latch 30 when reading character data into the video array and enables latch 31 when reading attributes into the video array.

In the graphics mode, the signals are as shown in FIG. 3. Here, the RAS, CRT/CPU and CPU LATCH waveforms are the same as in FIG. 2. Now, however, the ATR LATCH on the third line, operates latch circuit 31 for both of the CRT memory cycles. The gate output from video array 12 shown at the bottom line changes, but this now has no effect on the operation since the ALPHA signal on line 20 is now forcing NAND circuit 35 high which does not generate an enable signal for latch 30. Latch 31 is always enabled since NAND circuit 36 is low.

FIG. 4 shows the memory addressing arrangement for memory 22 when the memory expansion module is not mounted. The memory has a capacity of 64K bytes which have consecutively numbered addresses, expressed in FIG. 4 in hexadecimal form, from 0000 to FFFF. A portion of the memory, including four locations 8000 through 8003, contains the video data. Adjacent locations of the video memory store character

(either alpha or graphics) bytes and attribute bytes as shown. This memory requires sixteen address bits (A0 through A15) for the 64K address locations.

In order to expand the memory to 128K bytes by adding an expansion module, the normal arrangement employed is to address the base memory in the same way as shown in FIG. 4, and to add the further addresses provided by the expansion module on top of the addresses in the base memory. Thus, the base memory addresses would go from 0000 through FFFF and the expansion module addresses from 10000 through 1FFFF.

FIG. 5 shows a novel addressing scheme for the two memories in accordance with the invention. In this arrangement, memory 22 contains all the even addresses from 00000 through 1FFFE, and the expansion memory (42, FIG. 1) contains all the odd addresses from 00001 through 1FFFF. In the area of the memories used for video data, of which addresses 8000 through 8007 are shown, the character bytes (either alphanumeric or graphics) are still held in even address locations and the associated attribute bytes are still held in adjacent odd address locations. Thus, memory addressing for the video data follows the same pattern as that when only the base memory is used. This arrangement has the great advantage that video bandwidth can be doubled. Video bandwidth is determined by the speed of the memories and the size of each memory location. In the arrangement described above, using only memory 22, the memory cycles are grouped in threes, one for the CPU and two for the CRT. A typical time for these operations is 1.1μ secs. for the three cycles. In these cycles, the CPU accesses one location, and a character byte and an attribute byte are retrieved for the CRT. Now, when the memory is expanded as shown in FIG. 5, if, for the video data we regard the lowest order bit as a 'don't care' bit, then from each set of address bits we retrieve both a character and an attribute byte. This means that in the 1.1μ secs., we can now fetch two character bytes and two attribute bytes for the CRT in addition to the single byte access for an 8 bit micro-processor CPU. Thus, the CRT system can provide a considerably higher definition display including more alphanumeric or graphics information.

Turning back again to FIG. 1, we will now assume that the memory expansion module is coupled to the microcomputer. This adds memory 42, and latch circuits 43 and 44 to the system. Latch circuit 43 couples the data output bus of memory 42 to the CPU data bus 26, and therefore equates to latch circuit 32 in the base system. Latch circuit 44 couples the data output bus of memory 42 to the video array data bus 14 and accordingly equates to latch 31 in the base system.

Looking now at the addressing scheme, we have 128K bytes of memory which require 17 address bits A0 through A16 to access all of them. However, as all of the even addresses are in the base memory 22 and the odd addresses are in memory 42, all the lowest order bit, A0, does is to select one of the memories. In other words, if A0 is '0', then memory 22 is selected and if it is '1' then memory 42 is selected. Now, if we add the highest order bit A16 to bits A1 through A15, each

memory is again addressed by 16 bits. This is achieved for the CRT addresses by multiplexer 23, and for CPU addresses by multiplexer 24. Each of these multiplexers receives a control input from line 38. When the expansion memory module is plugged in, this line is automatically reduced from a high state to a low state as it is earthed at the expansion module end. Multiplexer 23 receives address bits A0 and A16 from the CRT controller and, when line 38 is high, passes A0 and when this line is low, passes A16. Accordingly, when the expansion module is mounted, the input to multiplexer 25 from the CRT controller comprises addresses A1 through A15 from the lower address output of controller 11, and A16 from multiplexer 23. Multiplexer 24 operates in a similar manner to multiplexer 23, only for the CPU addresses. It receives the CPU A0 and A16 addresses and, when the memory expansion module is fitted, passes the A16 address to multiplexer 25, which also receives the CPU A1 through A15 addresses. Multiplexer 25 is responsive to a CRT/CPU signal, shown in FIGS. 2, 3 and 6, to pass either the CRT or the CPU address to memory 22 when only this memory is present or to both memories when the expansion module is fitted through the MA1-MA16 link. This leaves the selection of the memories for odd and even addresses by the A0 address bit, which is achieved by controlling the chip select (CS) inputs to the memories from a memory chip select (MEM CS) output from the video array. The CS input of memory 22 is driven from a NAND gate 39 which, in the absence of the expansion module, has one input, on a DISABLE ECS line, always high. Thus with no expansion module, the input to the CS input is the inverse of the MEM CS output. This output goes high for each memory access time, giving a low input to the memory CS to enable the memory. With both memories installed, what is required is to select both memories for each CRT access and either one or the other, in accordance with the value of the A0 bit, for each CPU access.

Taking the CRT addressing first, the memory 22 CS input is fed from NAND gate 39, as before, and the memory 42 CS input is fed from a NAND gate 45. Both have one input coupled to receive the MEM CS output of the video array 12. For the CRT accesses, the second inputs of each must be high. The second input to NAND gate 39 comes from a NAND gate 46. With no CPU CYCLE input to this module from the video array, the output of NAND gate 46 is high. The second input to NAND gate 45 is delivered from a NAND gate 47. This, with no input from the CPU CYCLE line, also provides a high output. Thus, for CRT accesses, the CS inputs to both memories are raised to enable the memories together.

For CPU accesses, the CPU CYCLE input to the expansion module from the video array 12 is high. Therefore, for a CPU A0 input to NAND gate 46 of '1' during a CPU cycle, the output from NAND gate 46 goes low, thereby disabling memory 22 through NAND gate 39. The CPU A0 line passes through an inverter 48, so this input is low, giving a high output to enable memory 42 through NAND gate 45. Clearly,

when the CPU A0 line carries a '0' bit, this situation is reversed, so that memory 22 is enabled and memory 42 disabled.

Data to be written into the memories is applied from the CPU over the CPU D0-D7 lines. When the expansion module is not present, the DISABLE ECS line to NAND gate 39 is always high, so when the MEM CS line 15 is raised, the memory 22 can be written into the location addressed, through multiplexors 24 and 25, by the CPU A0-A15 signals. When the expansion module is fitted, and the CPU wishes to write to an even location, the DISABLE ECS line is forced high as the CPU A0 line to NAND gate 46 is low allowing the write to occur in memory 22. At this time, the inverted A0 signal from inverter 48 forces NAND gate 47 output high to force the output of NAND gate 45 low. Thus, memory 42 is disabled and can not be overwritten. When the CPU wishes to write to an odd location, the CPU A0 line is high, so memory 42 is selected from NAND gate 45 and memory 22 is disabled thereby preventing destruction of its data.

Data read from memories 22 and 42 for the CPU passes through either latch circuit 32 from memory 22 or latch circuit 43 from memory 42. Latch circuit 32 is enabled from the output of a NAND gate 37. Without the expansion module, the lower input of this gate is always high, so gate 37 enables latch circuit 32 in response to a signal on the VIDEO MEMR line resulting from a negative CPU memory read signal and negative memory address signal applied to a NOR gate 33 from the CPU. With the expansion memory in place, the NOR gate 33 output on the VIDEO MEMR line is applied to both NAND gates 37 and 49. The other inputs to these NAND gates come from the CPU A0 line and the output of inverter 48, through the -DISABLE DATA line respectively. Consequently, when the CPU A0 line carries a '1' bit, latch circuit 43 is enabled through NAND gate 49, and latch circuit 32 is disabled through NAND gate 37. When the CPU A0 line carries a '0' bit, latch circuit 32 is then enabled through NAND gate 37 and latch circuit 43 disabled through NAND gate 49. Thus, data is read from either of these latches to the CPU D0-D7 line.

For the CRT data, as has been mentioned above, the memories are accessed together so that character data, alpha or graphics, is retrieved from memory 22, and attribute data from memory 42. The character data is latched into latch circuits 28 and 31 for both alpha and graphics data. This is because, as can be seen at the third and fourth lines of FIG. 6, the CHAR. LATCH and ATR. LATCH signals from video array 12 now coincide. The attribute data from memory 44 is latched into latch circuit 44 which is also clocked by the ATR LATCH data from video array 12. Data from latch circuit 28 is passed to the character generator 29, as before, and the character line data from the generator is latched into latch circuit 30. Each of these latch circuits is read out by means of a low signal applied to its enable input. The GATE signal from video array 22 on line 20, shown at the bottom line of FIG. 6, controls the read

out of firstly latch circuit 30 or 31 and then latch circuit 44.

In the alphanumeric mode, the ALPHA signal on line 20 from the video array 22 is high. Accordingly, when the GATE signal is high, the output of NAND circuit 35 is low, enabling latch circuit 30 to output its data to the MD0-MD7 bus into the video array. When the GATE signal subsequently goes low, latch circuit 44 is enabled to deliver its data to the MD0-MD7 bus and, as the output of NAND gate 35 is now high, latch circuit 30 is disabled. During this time NAND gate 36, which receives the GATE signal, fed back from the expansion module on a -LGG line, together with the output of NAND gate 35, never provides a low output, so latch circuit 31 remains disabled. Thus, a character byte is read from latch circuit 30 followed by an attribute byte from latch 44 for each CRT cycle.

In the graphics mode, the ALPHA signal is low. Accordingly, the output of NAND gate 35 is always high, so latch 30 is never enabled. When the GATE signal is high, this signal, returned from the expansion module on the -LGG line, together with the high output from NAND gate 35, provide a low output from NAND gate 36. This enables latch circuit 31 to read out its graphics character data to the MD0-MD7 bus. Thereafter, when the GATE signal goes low, latch circuit 31 is disabled and latch circuit 44 enabled to provide the corresponding attribute data.

In summary, what has been shown is, in a microcomputer system, a memory access arrangement which, when an expansion memory is added treats the main memory locations as the even addresses and the expansion memory locations as the odd addresses. The microcomputer system includes a video subsystem which accesses the memory in cycles between CPU access cycles. When the expansion memory is added, the video subsystem, in each of its access cycles, addresses the memory to retrieve data from both an even and an adjacent odd address, thereby doubling the data rate for each of these cycles. This allows higher definition displays.

It is, of course, clear that other subsystems, for example communications subsystems, which require access to memory substantially independently of the CPU, may with advantage use the increased memory bandwidth provided by the invention. In the embodiment described above, for each three operating cycles, one was used by the CPU and two by the video system to enhance display definition. Equally well, these three cycles could be used by the CPU, the video subsystem and a communications subsystem respectively. Thus, with the expansion memory installed, the video subsystem would have the same bandwidth as if it used two of the three cycles with single byte transfer and in addition the communications subsystem has its own cycle with the double byte access rate.

While the invention has been particularly shown and described with reference to preferred embodiments thereof, it will be understood by those skilled in the art that various other changes in form and detail may be

made without departing from the spirit and scope of the invention.

I claim:

1. A computer system comprising:

(a) a central processor unit (CPU) having a parallel $n+1$ bit memory address output comprising bits $A(0)$ through $A(n)$, of which bits $A(0)$ and $A(n)$ are respectively the lowest and highest order bits, and n is an integer;

(b) a processing subsystem (PS) having a parallel $n+1$ bit memory address output comprising bits $A(0)$ through $A(n)$, of which bits $A(0)$ and $A(n)$ are respectively the lowest and highest order bits;

(c) a memory address logic system (MALS) having logic inputs, and address inputs coupled to said memory address outputs of the CPU and the PS, and having an n bit memory address output;

(d) a base memory having 2^n locations and an n bit address input coupled to the memory address output of said MALS;

(e) a memory expansion module (MEM) comprising an expansion memory having 2^n locations and an n bit address input, and a control system having control outputs;

(f) coupling means for removably coupling said MEM to said MALS, including means for removably coupling said address input of the expansion memory to the memory address output of said MALS, and for removably coupling the control outputs of said control system to the logic inputs of said MALS;

(g) said MALS being switched from a first condition to a second condition on connection of the control outputs of the control system of said MEM through said coupling means to said logic inputs, and being responsive, in said first condition, to address bits $A(0)$ through $A(n-1)$ in each set of address bits from the CPU or from the PS to address an individual location in the base memory, and being responsive, in said second condition, to each set of address bits $A(0)$ through $A(n)$ from the CPU to address an individual location within one of the two memories or to bits $A(1)$ through $A(n)$ in each set of address bits from the PS to simulta-

neously address a pair of locations, comprising a location in each of said memories.

2. A computer system according to claim 1, in which said base memory and said expansion memory each have a data output, and said CPU and said PS each have a data input, and including first data latch means connected between the data output of the base memory and the data input of the CPU, second data latch means connected between the data output of the base memory and the PS, the third data latch means connected between the data output of the expansion memory and, through said coupling means, to the data input of the CPU, fourth data latch means connected between the data output of the expansion memory and, through said coupling means, to the data input of the PS, each of said data latch means having a enable input, and latch control means coupled to the enable input of said second data latch means and, through said coupling means, to the enable input of said fourth data latch means, said latch control means being effective on said simultaneous addressing of a pair of locations to enable said second data latch means to transfer data from said base memory to the PS and thereafter to enable said fourth data latch means to transfer data from the expansion memory to the PS.

3. A computer system according to claim 2, in which said latch control means is further coupled to the enable inputs of said first and third data latch means and is effective, on addressing of a single one of said memories, to enable a single one of said data latch means coupled to the addressed memory.

4. A computer system according to claim 1, in which said MALS includes a first multiplexer coupled to the $A(0)$ and $A(n)$ address outputs of the CPU and a second multiplexer coupled to the $A(0)$ and $A(n)$ address outputs of the PS, said multiplexers being coupled to a common control line switched from a first condition to a second condition on connection thereto of a control output of the control system of said MEM through said coupling means, thereby to select the $A(0)$ bits or the $A(n)$ bits respectively for memory addressing.

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Form PTO-1449 LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT (Use Several Sheets if Necessary)	ATTY. DOCKET NO.	SERIAL NO.
	SC0034W1	08/912,243
	APPLICANT Dror HALAHMI Yoram SALANT	
	FILING DATE	GROUP 2851



REFERENCE DESIGNATION U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	AA					
	AB					
	AC					
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	AG					
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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES/NO
	AM					
	AN					
	AO					
	AP					
	AQ					
	AR					

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

jd	AR	Motorola Semiconductor Technical Data, Advance Information DSP56301, pg. 01, Motorola Inc., 1995
	AS	
	AT	

EXAMINER J. LANE

DATE CONSIDERED 11/18/98

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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DSP56301

Advance Information

24-Bit General Purpose Digital Signal Processor

The DSP56301, is the first member in the new DSP56300 Family. This family uses a high performance, single clock cycle per instruction engine providing two fold performance increase over Motorola's popular DSP56000 Family, while retaining code compatibility. Several significant architectural enhancements include a barrel shifter, 24 bit addressing, instruction cache, and DMA functionality.

The DSP56301 offers 66 MIPS using an internal 66 MHz clock and will soon be available at 80 MIPS using an internal 80 MHz clock at 3.0 - 3.6 volts. The DSP56300 Family offers a new level of performance in MIPS, rich instruction set, and low power dissipation enabling a new generation of products in wireless, telecommunications, and multimedia.

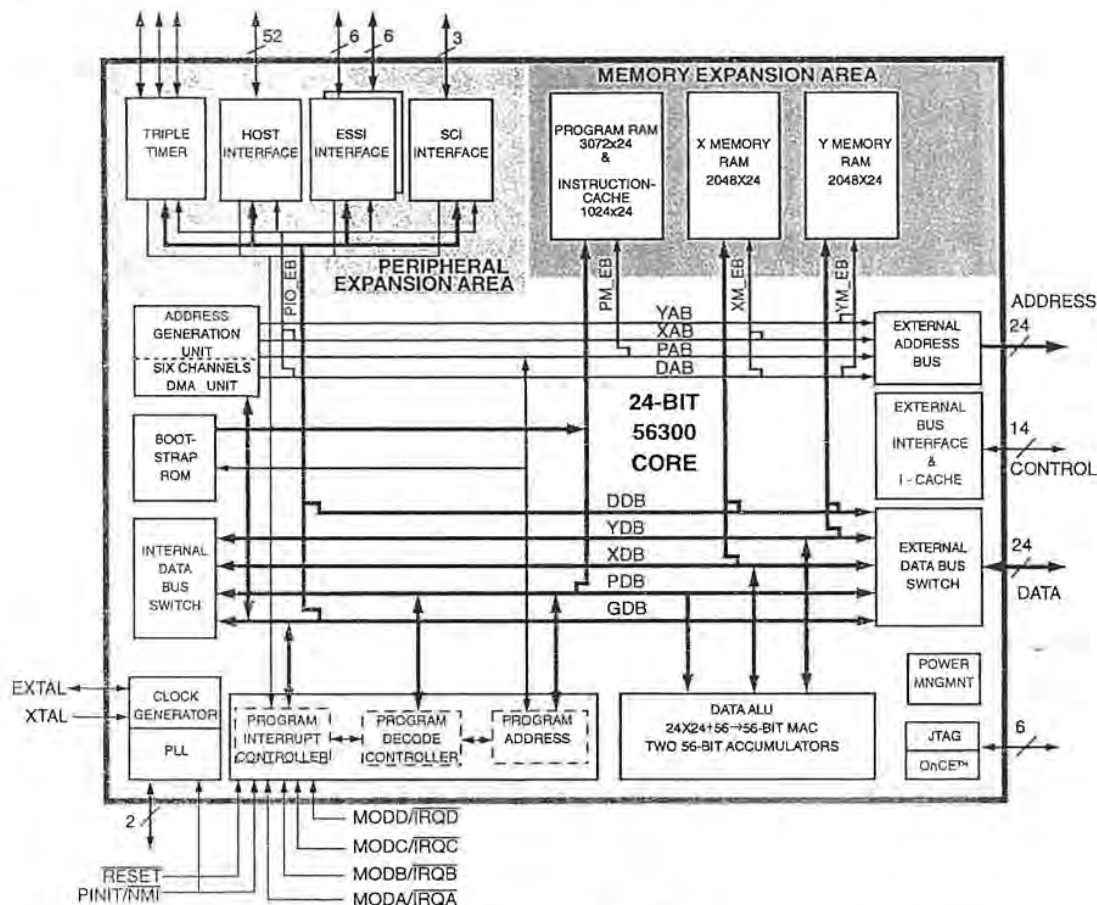


Figure 1 DSP56301 Block Diagram

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09/497,986 B

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	
Dror Halahmi et al.	Examiner: Unknown
Application No.: To be assigned - A Divisional of Application No. 08/912,243 filed August 15, 1997	Group Art Unit: Unknown
Filed: February 4, 2000	Docket No: SC0034WI D01
Title: A METHOD FOR DIGITAL SIGNAL PROCESSING, DSP, MOBILE COMMUNICATION AND AUDIO- DEVICE	

Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

PRELIMINARY AMENDMENT

Dear Assistant Commissioner:

Please amend the current Application as set forth below.

FEES/EXTENSION OF TIME

Please charge Deposit Account No. 13-4773 for any and all fees required under 37 C.F.R. §§ 1.16 or 1.17, or credit Deposit Account No. 13-4773 for any and all refunds. One copy of this page is enclosed for deposit account purposes.

Below is a table of fees related to the claims.

	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST No. PREVIOUSLY PAID FOR	CURRENT EXTRA (no less than zero)	RATE	FEE
TOTAL CLAIMS	23	MINUS	20	= 3	X \$18.00	\$54.00
INDEPENDENT CLAIMS	2	MINUS	3	= 0	X \$78.00	0.00
MULTIPLE DEPENDENT CLAIM(S)					\$260.00	0.00
TOTAL ADDITIONAL FEE:						\$54.00

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2-15-2000 Charli Ariens CHARLI ARIENS
Date Signature Printed or Typed

IN THE CLAIMS

Please cancel claim 1 and add claims 11-33.

11. (New Claim) In a digital signal processor having a first memory, a first buffer, and a register file, a method for performing a digital signal processing operation having a first data word located at a misaligned starting address within the first memory, comprising:
outputting the first data word to the register file during a first interval;
during a second interval, reading a second data word and a third data word from the first memory, wherein the second data word is output to the register file and the third data word is output to the first buffer; and
completing the digital signal processing operation.
12. (New Claim) The method of claim 11, further comprising:
during subsequent intervals, outputting to the register file two data words, wherein one of the two data words is read from the first buffer and the other one of the two data words is read from the first memory.
13. (New Claim) The method of claim 12, further comprising:
during the subsequent intervals, accessing two data words stored within the register file in order to perform the digital signal operation.
14. (New Claim) The method of claim 12, wherein the digital signal processor comprises a second memory and a second buffer for providing another two data words to the register file.
15. (New Claim) The method of claim 14, further comprising accessing two pairs of data words stored within the register file during the subsequent intervals, wherein one of the two pairs corresponds to the first memory, and the other one of the two pairs corresponds to the second memory.
16. (New Claim) The method of claim 12, wherein the first and second intervals correspond to a first instruction and the subsequent intervals correspond to a second instruction.

17. (New Claim) The method of claim 11, further comprising:
during subsequent intervals, accessing from the first memory a next pair of data words, wherein one of the next pair of data words is stored into the first buffer, and the other one of the next pair is stored into the register file.
18. (New Claim) The method of claim 17, wherein the next pair of data words is a consecutive pair of data words.
19. (New Claim) The method of claim 17, further comprising:
during the subsequent intervals, outputting to the register file two data words, wherein one of the two data words is read from the first buffer and the other one of the two data words is read from the first memory.
20. (New Claim) The method of claim 19, wherein the two data words are consecutive data words.
21. (New Claim) The method of claim 19, further comprising:
during the subsequent intervals, accessing two data words stored within the register file in order to perform the digital signal operation.
22. (New Claim) The method of claim 21, wherein the digital signal processor comprises a first multiplier and a first accumulator, and wherein the two data words accessed from the register file are output from the register file to the first multiplier for performing at least a portion of the digital signal processor operation.
23. (New Claim) The method of claim 17, wherein the first and second intervals correspond to a first instruction and the subsequent intervals correspond to a second instruction.
24. (New Claim) The method of claim 11, wherein the first memory includes even and odd addresses, and the misaligned starting address is an odd address.
25. (New Claim) A digital device capable of performing the method of claim 11.
26. (New Claim) A digital signal processor comprising:

an address generation unit;
a first memory coupled to the address generation unit;
a first buffer coupled to the first memory and capable of receiving data words from the first memory; and
a register file coupled to the first memory and the first buffer, and capable of receiving one data word from the first memory and one data word from the first buffer during each of a plurality of processing intervals for performing a digital signal operation.

27. (New Claim) The digital signal processor of claim 26, further comprising:
a second memory coupled to the address generation unit;
a second buffer coupled to the second memory and the register file, and capable of receiving data words from the second memory, wherein the register file is capable of receiving one data word from the second memory and one data word from the second buffer during each of the plurality of processing intervals.
28. (New Claim) The digital signal processor of claim 27, further comprising:
a first multiplier coupled to the register file and capable of receiving from the register file two data words corresponding to the first memory and the first buffer, during one of the plurality of processing intervals; and
a second multiplier coupled to the register file and capable of receiving from the register file two data words corresponding to the second memory and the second buffer during the one of the plurality of processing intervals.
29. (New Claim) The digital signal processor of claim 28, wherein the digital signal processor comprises only one address generation unit and is further characterized as being capable of performing two parallel multiplications on a set of four data words during a same time interval.
30. (New Claim) The digital signal processor of claim 27, wherein the first memory and the second memory each include:
a storage array having even and odd addresses and capable of storing a plurality of consecutive data words.

31. (New Claim) The digital signal processor of claim 26, wherein the digital signal processor is capable of performing a first initialization interval if a starting address of the digital signal operation is an odd address.
32. (New Claim) The digital signal processor of claim 31, wherein the first initialization interval stores a first data word into the register file, and a second initialization interval stores a second data word into the register file and a third data word into the first buffer.
33. (New Claim) The digital signal processor of claim 32, wherein the first and second initialization intervals occur prior to the plurality of processing intervals.

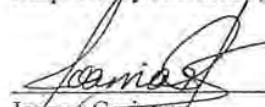
REMARKS

Claims 11-33 are pending in the current application. Claims 2-10 were canceled with the filing of the Divisional Application, and claim 1 is canceled in this Preliminary Amendment. Applicants submit that the amendments do not add new matter to the current Application.

Applicants respectfully solicit allowance of the pending claims. Contact me if there are any issues regarding this communication or the current Application.

Respectfully submitted,

2/15/00
Date


Joanna Gariazzo
Attorney for Applicants
Registration No. 43,629
Telephone No. (512) 996-6839
Facsimile No. (512) 996-6854



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	
Dror Halahmi et al.	Examiner: Unknown
Application No.: To be assigned - A Divisional of Application No. 08/912,243 filed August 15, 1997	Group Art Unit: Unknown
Filed: February 4, 2000	Docket No: SC0034WI D01
Title: A METHOD FOR DIGITAL SIGNAL PROCESSING, DSP, MOBILE COMMUNICATION AND AUDIO- DEVICE	

Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

PRELIMINARY AMENDMENT

Dear Assistant Commissioner:

Please amend the current Application as set forth below.

FEES/EXTENSION OF TIME

Please charge Deposit Account No. 13-4773 for any and all fees required under 37 C.F.R. §§ 1.16 or 1.17, or credit Deposit Account No. 13-4773 for any and all refunds. One copy of this page is enclosed for deposit account purposes.

Below is a table of fees related to the claims.

	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST No. PREVIOUSLY PAID FOR	CURRENT EXTRA (no less than zero)	RATE	FEE
TOTAL CLAIMS	23	MINUS	20	= 3	X \$18.00	\$54.00
INDEPENDENT CLAIMS	2	MINUS	3	= 0	X \$78.00	0.00
MULTIPLE DEPENDENT CLAIM(S)					\$260.00	0.00
TOTAL ADDITIONAL FEE:						\$54.00

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2-15-2000 Charli Ariens CHARLI ARIENS
Date Signature Printed or Typed

OFFICIAL

Fax Received
OCT 20 1999
Group 2700

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	
Halahmi et al. et al.	Examiner: J. Lane
Application No.: 08/912,243	Group Art Unit: 2751
Filed: August 15, 1997	Docket No: SC0034WI
Title: A METHOD FOR DIGITAL SIGNAL PROCESSING, DSP, MOBILE COMMUNICATION AND AUDIO- DEVICE	

Fax No. (703) 305-9731
Date: October 20, 1999

Examiner J. Lane:

In September, our office received a corrected copy of the Notice of Allowance and Issue Fee Due for the above case (08/912,243). However, we never received the original mailing of the Notice of Allowance and its corresponding papers. I believe our office has contacted you before, making you aware of this situation. Therefore, we are requesting that you please resend the papers from this original mailing so that we may have them in our records before paying the issue fee due December 10, 1999. Thank you so much for your help; I appreciate your time. If you have any other questions regarding this communication or case, please feel free to let me know.

Thanks,



Joanna P. Gariazzo
Agent for Applicants
Registration No. 43,629

[illegible]

100-100000

2000 \$700

155770





IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	
Dror Halahmi et al.	Examiner: J. Lane
Application No.: 08/912,243	Group Art Unit: 2751
Filed: August 15, 1997	Docket No: SC0034WI
Title: METHOD FOR DIGITAL SIGNAL PROCESSING, DSP, MOBILE COMMUNICATION AND AUDIO- DEVICE	Batch: M03 Class: 711-217

Assistant Commissioner for Patents
Box Issue Fee
Washington, DC 20231

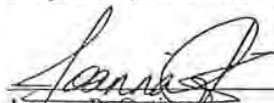
SUBMISSION OF FORMAL DRAWINGS

Dear Assistant Commissioner:

The Notice of Allowance for the current Application indicated that formal drawings are now required. Enclosed herewith are formal drawings for the current Application.

Respectfully submitted,

12/10/99
Date


Joanna P. Gariazzo
Attorney for Applicants
Registration No. 43,629
Telephone No. (512) 996-6839
Facsimile No. (512) 996-6854

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12/10/99 Elaine Cox Elaine Cox
Date Signature Printed or Typed

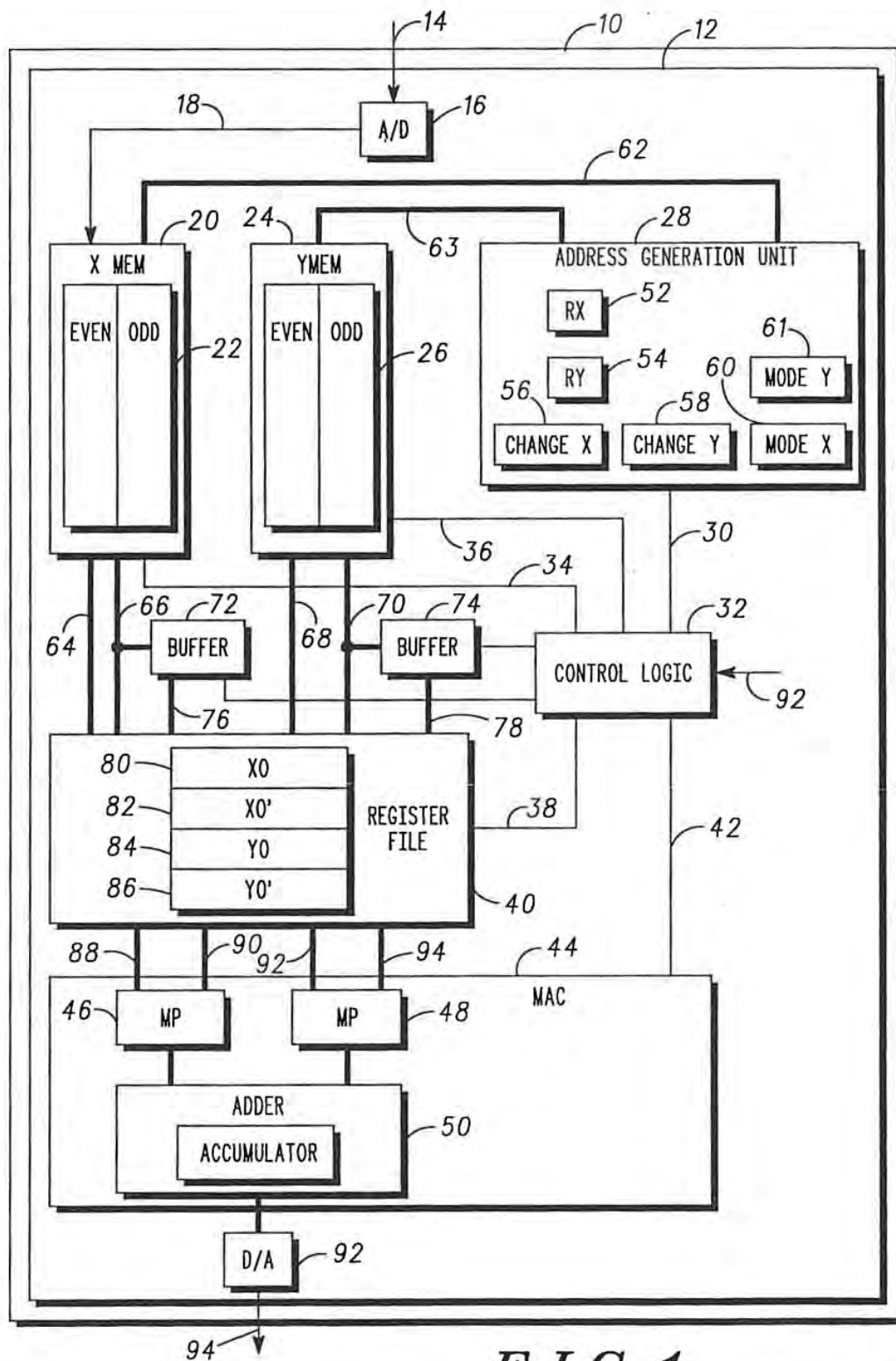
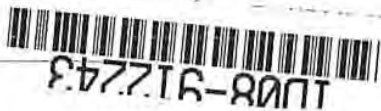


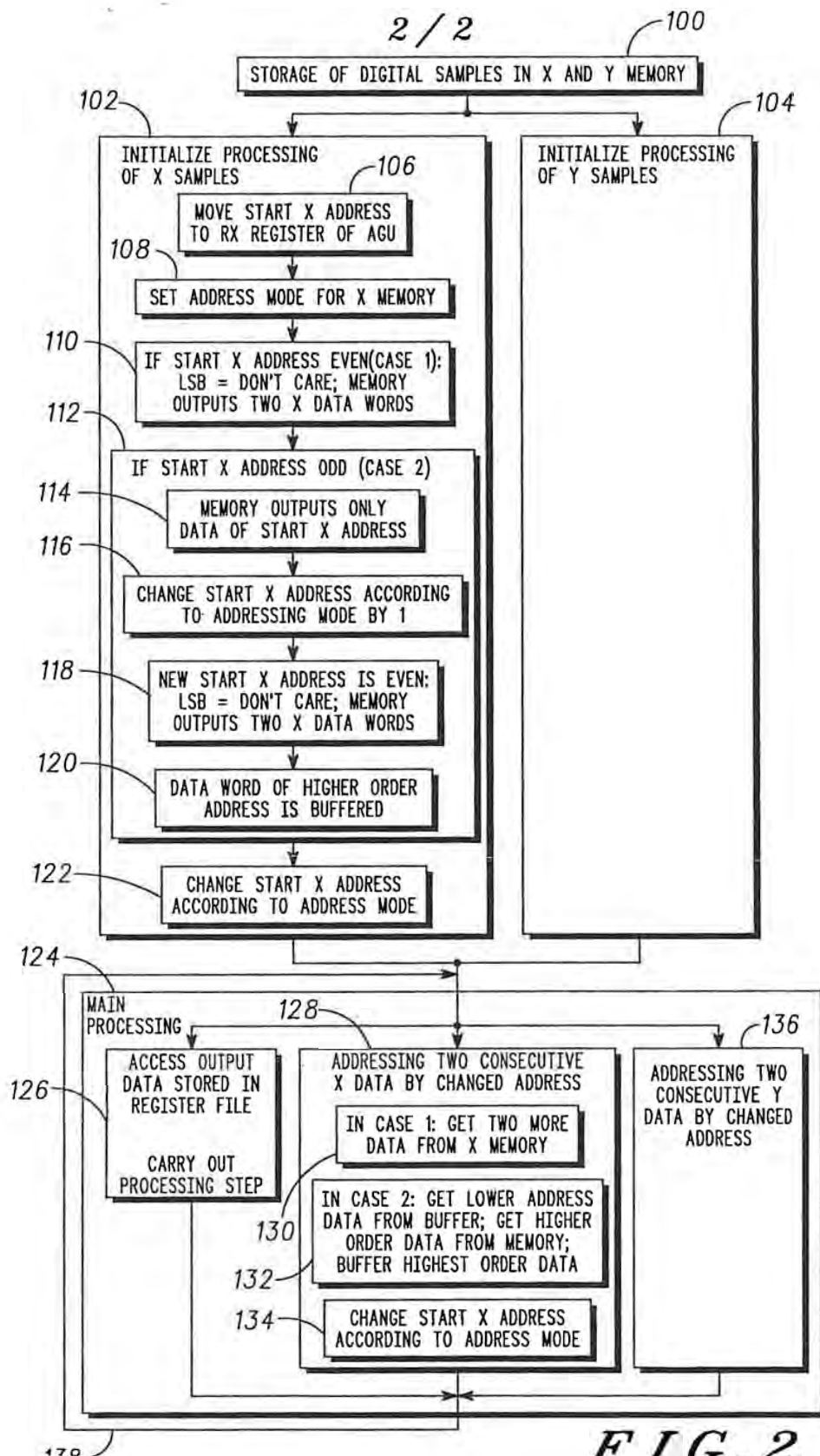
FIG. 1



HALAHMI et al
SC0034WI
MOTOROLA
JOANNA P. GARIAZZO
(512) 996-6839

APPLICATION NO.: 08/912, 243
GROUP ART UNIT: 2745







HALAHMI et al
SC0034WI
MOTOROLA
JOANNA P. GARIAZZO
(512) 996-6839

APPLICATION NO.: 08/912, 243
GROUP ART UNIT: 2745

PART B—ISSUE FEE TRANSMITTAL

Complete and mail this form, together with applicable fees, to:

Box ISSUE FEE
Assistant Commissioner for Patents
Washington, D.C. 20231

MAILING INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE. Blocks 1 through 4 should be completed when appropriate. All further correspondence including the Issue Fee Receipt, the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Legibly mark-up with any corrections or use Block 1)

Note: The certificate of mailing below can only be used for domestic mailings of the Issue Fee Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing.

Certificate of Mailing

I hereby certify that this Issue Fee Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Box Issue Fee address above on the date indicated below.

Elaine Cox

(Depositor's name)

Elaine Cox

(Signature)

12/10/99

(Date)

APPLICATION NO.	FILING DATE	TOTAL CLAIMS	EXAMINER AND GROUP ART UNIT	DATE MAILED
01/11/99	04/11/99	010	1-200	2751 10/10/99

First Named Applicant: ELAINE COX

TITLE OF INVENTION

METHOD FOR IMPROVING SIGNAL TRANSMISSIONS USING MOBILE COMMUNICATION AND SUBSTITUTION

ATTY'S DOCKET NO.	CLASS-SUBCLASS	BATCH NO.	APPLN. TYPE	SMALL ENTITY	FEE DUE	DATE DUE
2-1000000	710 212.000	003	UTILITY	NO	\$1210.00	12/10/99

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363). Use of PTO form(s) and Customer Number are recommended, but not required.

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47) attached.

2. For printing on the patent front page, list (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Robert Handy

2

3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)
PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. Inclusion of assignee data is only appropriate when an assignment has been previously submitted to the PTO or is being submitted under separate cover. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE MOTOROLA, INC.

(B) RESIDENCE: (CITY & STATE OR COUNTRY) Schaumburg, IL

Please check the appropriate assignee category indicated below (will not be printed on the patent)

☐ individual ☒ corporation or other private group entity ☐ government

4a. The following fees are enclosed (make check payable to Commissioner of Patents and Trademarks):

☐ Issue Fee☐ Advance Order - # of Copies

4b. The following fees or deficiency in these fees should be charged to:

DEPOSIT ACCOUNT NUMBER 13-4773
(ENCLOSE AN EXTRA COPY OF THIS FORM)

☒ Issue Fee☐ Advance Order - # of Copies

The COMMISSIONER OF PATENTS AND TRADEMARKS IS requested to apply the Issue Fee to the application identified above.

(Authorized Signature) 43,629

Joanna P. Gariazzo

(Date)

12/10/99

NOTE: The Issue Fee will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the Patent and Trademark Office.

Burden Hour Statement: This form is estimated to take 0.2 hours to complete. Time will vary depending on the needs of the individual case. Any comments on the amount of time required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, D.C. 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND FEES AND THIS FORM TO: Box Issue Fee, Assistant Commissioner for Patents, Washington D.C. 20231

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Patent and Trademark Office

Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO.
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08/912,243 08/15/97 HALAHMI

SC003401

EXAMINER

LM51/1124

VINCENT B INGRASSIA
MOTOROLA INC
INTELLECTUAL PROPERTY DEPT
P O BOX 10219 SUITE R3108
SCOTTSDALE AZ 85271-0219

ART UNIT	PAPER NUMBER
----------	--------------

2751

DATE MAILED:

11/24/98

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

NOTICE OF ALLOWABILITY

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance and Issue Fee Due or other appropriate communication will be mailed in due course.

☒ This communication is responsive to the prior art filed 8/15/97

☒ The allowed claim(s) is/are 1-10

☐ The drawings filed on _____ are acceptable.

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

A SHORTENED STATUTORY PERIOD FOR RESPONSE to comply with the requirements noted below is set to EXPIRE THREE MONTHS FROM THE "DATE MAILED" of this Office action. Failure to timely comply will result in ABANDONMENT of this application. Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

☐ Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL APPLICATION, PTO-152, which discloses that the oath or declaration is deficient. A SUBSTITUTE OATH OR DECLARATION IS REQUIRED.

☒ Applicant MUST submit NEW FORMAL DRAWINGS

☐ because the originally filed drawings were declared by applicant to be informal.

☒ including changes required by the Notice of Draftperson's Patent Drawing Review, PTO-948, attached hereto or to Paper No. _____

☐ including changes required by the proposed drawing correction filed on _____, which has been approved by the examiner.

☐ including changes required by the attached Examiner's Amendment/Comment.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the reverse side of the drawings. The drawings should be filed as a separate paper with a transmittal letter addressed to the Official Draftperson.

☐ Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Any response to this letter should include, in the upper right hand corner, the APPLICATION NUMBER (SERIES CODE/SERIAL NUMBER). If applicant has received a Notice of Allowance and Issue Fee Due, the ISSUE BATCH NUMBER and DATE of the NOTICE OF ALLOWANCE should also be included.

Attachment(s)

☒ Notice of References Cited, PTO-892

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Notice of Draftperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

☐ Interview Summary, PTO-413

☐ Examiner's Amendment/Comment

☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material

☐ Examiner's Statement of Reasons for Allowance



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

GP 2745
#4

In re Application of:
Dror Halahmi, et al.

Serial No.: 08/912,243

File Date: August 15, 1997

Title: METHOD FOR DIGITAL SIGNAL
PROCESSING, DSP, MOBILE
COMMUNICATION AND AUDIO-
DEVICE

) Examiner: Unknown

) Group Art Unit: 2745

) Docket No.: SC0034W1

) RECEIVED

) JUN 08 1999

) Group 2700

Assistant Commissioner for Patents
Washington, DC 20231

CHANGE OF CORRESPONDENCE ADDRESS

Dear Assistant Commissioner:

Please send all future correspondence regarding the above-referenced application to:

Harry A. Wolin
Motorola, Inc.
Austin Intellectual Property Law Section
MD: TX32/PL02
7700 West Parmer Lane
Austin, Texas 78729

Direct all telephone and facsimile communications to the numbers listed below.

Respectfully submitted,

George R. Meyer

George R. Meyer
Attorney for Applicant(s)
Registration No. 35,284
Telephone No. (512) 996-6849
Facsimile No. (512) 996-6854

5/27/99
Date

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Publishing Division

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on 5/28/99
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Elaine Cox
Signature - Assignee: MOTOROLA INC.

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office

#5

NOTICE OF ALLOWANCE AND ISSUE FEE DUE

$$f(x) = f_1(x) + f_2(x) + \dots + f_n(x) \quad (1)$$

1998, 1999, 2000, 2001, 2002, 2003, 2004, 2005, 2006, 2007, 2008, 2009, 2010, 2011, 2012, 2013, 2014, 2015, 2016, 2017, 2018, 2019, 2020, 2021, 2022, 2023, 2024, 2025, 2026, 2027, 2028, 2029, 2030, 2031, 2032, 2033, 2034, 2035, 2036, 2037, 2038, 2039, 2040, 2041, 2042, 2043, 2044, 2045, 2046, 2047, 2048, 2049, 2050, 2051, 2052, 2053, 2054, 2055, 2056, 2057, 2058, 2059, 2060, 2061, 2062, 2063, 2064, 2065, 2066, 2067, 2068, 2069, 2070, 2071, 2072, 2073, 2074, 2075, 2076, 2077, 2078, 2079, 2080, 2081, 2082, 2083, 2084, 2085, 2086, 2087, 2088, 2089, 2090, 2091, 2092, 2093, 2094, 2095, 2096, 2097, 2098, 2099, 2100, 2101, 2102, 2103, 2104, 2105, 2106, 2107, 2108, 2109, 2110, 2111, 2112, 2113, 2114, 2115, 2116, 2117, 2118, 2119, 2120, 2121, 2122, 2123, 2124, 2125, 2126, 2127, 2128, 2129, 2130, 2131, 2132, 2133, 2134, 2135, 2136, 2137, 2138, 2139, 2140, 2141, 2142, 2143, 2144, 2145, 2146, 2147, 2148, 2149, 2150, 2151, 2152, 2153, 2154, 2155, 2156, 2157, 2158, 2159, 2160, 2161, 2162, 2163, 2164, 2165, 2166, 2167, 2168, 2169, 2170, 2171, 2172, 2173, 2174, 2175, 2176, 2177, 2178, 2179, 2180, 2181, 2182, 2183, 2184, 2185, 2186, 2187, 2188, 2189, 2190, 2191, 2192, 2193, 2194, 2195, 2196, 2197, 2198, 2199, 2200, 2201, 2202, 2203, 2204, 2205, 2206, 2207, 2208, 2209, 2210, 2211, 2212, 2213, 2214, 2215, 2216, 2217, 2218, 2219, 2220, 2221, 2222, 2223, 2224, 2225, 2226, 2227, 2228, 2229, 2230, 2231, 2232, 2233, 2234, 2235, 2236, 2237, 2238, 2239, 2240, 2241, 2242, 2243, 2244, 2245, 2246, 2247, 2248, 2249, 2250, 2251, 2252, 2253, 2254, 2255, 2256, 2257, 2258, 2259, 2260, 2261, 2262, 2263, 2264, 2265, 2266, 2267, 2268, 2269, 2270, 2271, 2272, 2273, 2274, 2275, 2276, 2277, 2278, 2279, 2280, 2281, 2282, 2283, 2284, 2285, 2286, 2287, 2288, 2289, 2290, 2291, 2292, 2293, 2294, 2295, 2296, 2297, 2298, 2299, 2300, 2301, 2302, 2303, 2304, 2305, 2306, 2307, 2308, 2309, 2310, 2311, 2312, 2313, 2314, 2315, 2316, 2317, 2318, 2319, 2320, 2321, 2322, 2323, 2324, 2325, 2326, 2327, 2328, 2329, 2330, 2331, 2332, 2333, 2334, 2335, 2336, 2337, 2338, 2339, 2340, 2341, 2342, 2343, 2344, 2345, 2346, 2347, 2348, 2349, 2350, 2351, 2352, 2353, 2354, 2355, 2356, 2357, 2358, 2359, 2360, 2361, 2362, 2363, 2364, 2365, 2366, 2367, 2368, 2369, 2370, 2371, 2372, 2373, 2374, 2375, 2376, 2377, 2378, 2379, 2380, 2381, 2382, 2383, 2384, 2385, 2386, 2387, 2388, 2389, 2390, 2391, 2392, 2393, 2394, 2395, 2396, 2397, 2398, 2399, 2400, 2401, 2402, 2403, 2404, 2405, 2406, 2407, 2408, 2409, 2410, 2411, 2412, 2413, 2414, 2415, 2416, 2417, 2418, 2419, 2420, 2421, 2422, 2423, 2424, 2425, 2426, 2427, 2428, 2429, 2430, 2431, 2432, 2433, 2434, 2435, 2436, 2437, 2438, 2439, 2440, 2441, 2442, 2443, 2444, 2445, 2446, 2447, 2448, 2449, 2450, 2451, 2452, 2453, 2454, 2455, 2456, 2457, 2458, 2459, 2460, 2461, 2462, 2463, 2464, 2465, 2466, 2467, 2468, 2469, 2470, 2471, 2472, 2473, 2474, 2475, 2476, 2477, 2478, 2479, 2480, 2481, 2482, 2483, 2484, 2485, 2486, 2487, 2488, 2489, 2490, 2491, 2492, 2493, 2494, 2495, 2496, 2497, 2498, 2499, 2500, 2501, 2502, 2503, 2504, 2505, 2506, 2507, 2508, 2509, 2510, 2511, 2512, 2513, 2514, 2515, 2516, 2517, 2518, 2519, 2520, 2521, 2522, 2523, 2524, 2525, 2526, 2527, 2528, 2529, 2530, 2531, 2532, 2533, 2534, 2535, 2536, 2537, 2538, 2539, 2540, 2541, 2542, 2543, 2544, 2545, 2546, 2547, 2548, 2549, 2550, 2551, 2552, 2553, 2554, 2555, 2556, 2557, 2558, 2559, 2560, 2561, 2562, 2563, 2564, 2565, 2566, 2567, 2568, 2569, 2570, 2571, 2572, 2573, 2574, 2575, 2576, 2577, 2578, 2579, 2580, 2581, 2582, 2583, 2584, 2585, 2586, 2587, 2588, 2589, 2590, 2591, 2592, 2593, 2594, 2595, 2596, 2597, 2598, 2599, 2600, 2601, 2602, 2603, 2604, 2605, 2606, 2607, 2608, 2609, 2610, 2611, 2612, 2613, 2614, 2615, 2616, 2617, 2618, 2619, 2620, 2621, 2622, 2623, 2624, 2625, 2626, 2627, 2628, 2629, 2630, 2631, 2632, 2633, 2634, 2635, 2636, 2637, 2638, 2639, 2640, 2641, 2642, 2643, 2644, 2645, 2646, 2647, 2648, 2649, 2650, 2651, 2652, 2653, 2654, 2655, 2656, 2657, 2658, 2659, 2660, 2661, 2662, 2663, 2664, 2665, 2666, 2667, 2668, 2669, 2670, 2671, 2672, 2673, 2674, 2675, 2676, 2677, 2678, 2679, 26

$$E_{\text{eff}} = E_{\text{eff}}^{\text{eff}} + E_{\text{eff}}^{\text{eff}} \quad (14)$$
$$\| \mathbf{u} \|_{\mathbf{H}^1(\Omega)} = \left(\int_{\Omega} |\nabla \mathbf{u}|^2 dx \right)^{1/2} \quad (1.1)$$

2. Fill in the blank: _____

[illegible]

US7111 1 98-2-1

APPLICATION NO.	FILING DATE	TOTAL CLAIMS	EXAMINER AND GROUP ART UNIT	DATE MAILED
08/912,243	08/15/97	010	LANE, J	2751 09/10/99
First Named Applicant	JALANE	DROR		

TITLE OF INVENTION METHOD FOR DIGITAL SIGNAL PROCESSING, DSP, MOBILE COMMUNICATION AND ACCORD-TO-SERVICE

ATTY'S DOCKET NO.	CLASS-SUBCLASS	BATCH NO.	APPLN. TYPE	SMALL ENTITY	FEE DUE	DATE DUE
2 SC00PRAW1	701-213.666	003	UTB ITY	NO	\$1210.00	12/10/99

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NOTICE OF ALLOWANCE AND ISSUE FEE DUE

APPLICATION NO.	FILING DATE	TOTAL CLAIMS	EXAMINER AND GROUP ART UNIT	DATE MAILED
2013-0248	06/15/97	010	ARE-7	2/25/13 11/20/98
First Named Applicant: [illegible] (U.S. 154th term exp. - 0 days)				

TITLE OF INVENTION: METHOD FOR DIGITAL IMAGE PROCESSING, AND, IMAGE COMMUNICATION AND STORAGE SYSTEM

ATTY'S DOCKET NO.	CLASS-SUBCLASS	BATCH NO.	APPLN. TYPE	SMALL ENTITY	FEE DUE	DATE DUE
2013-0248	211-212.000	NO3	UTILITY	NO	\$1510.00	02/26/98

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1 / 2

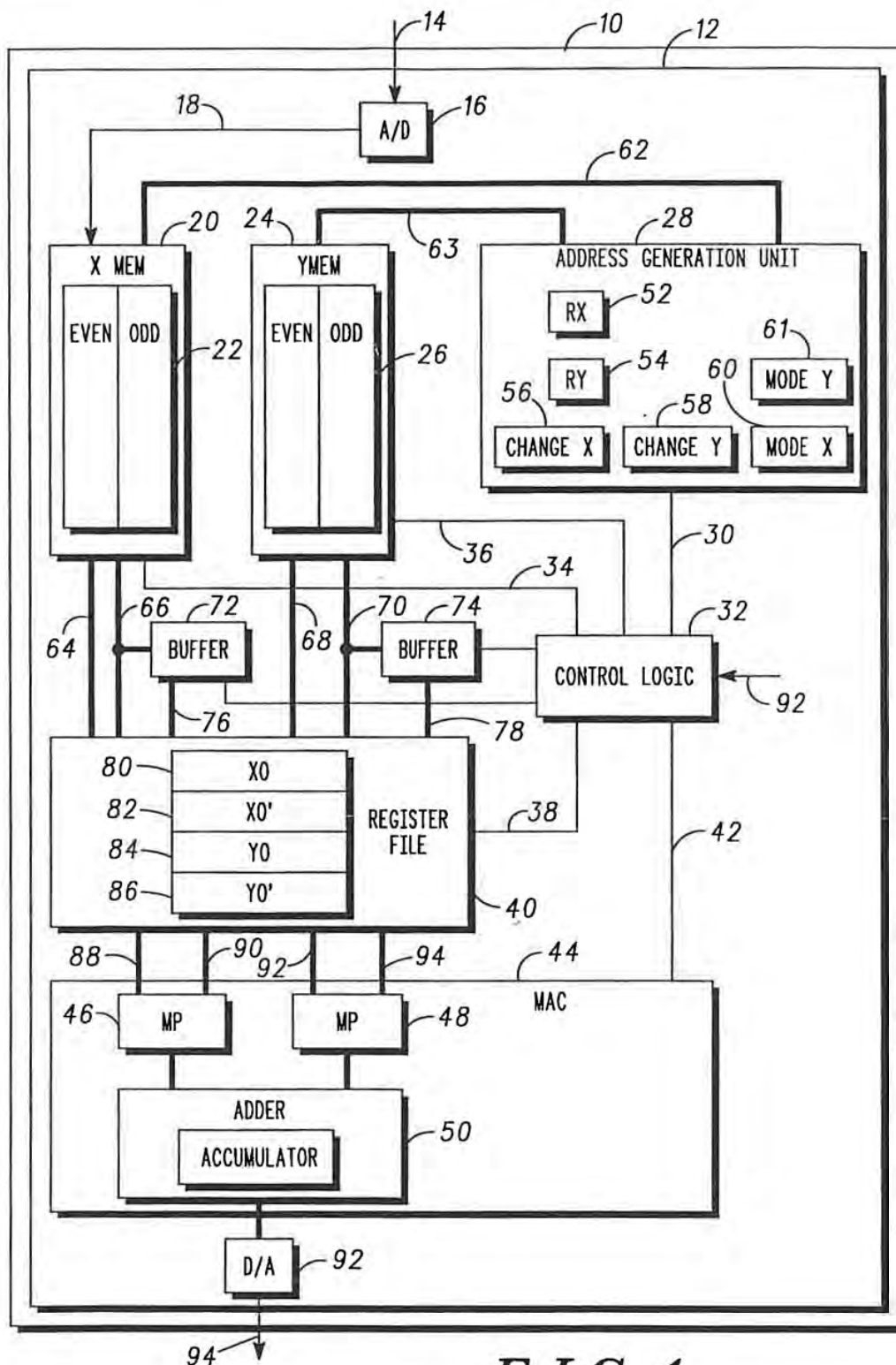


FIG. 1

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SERIAL NO.:
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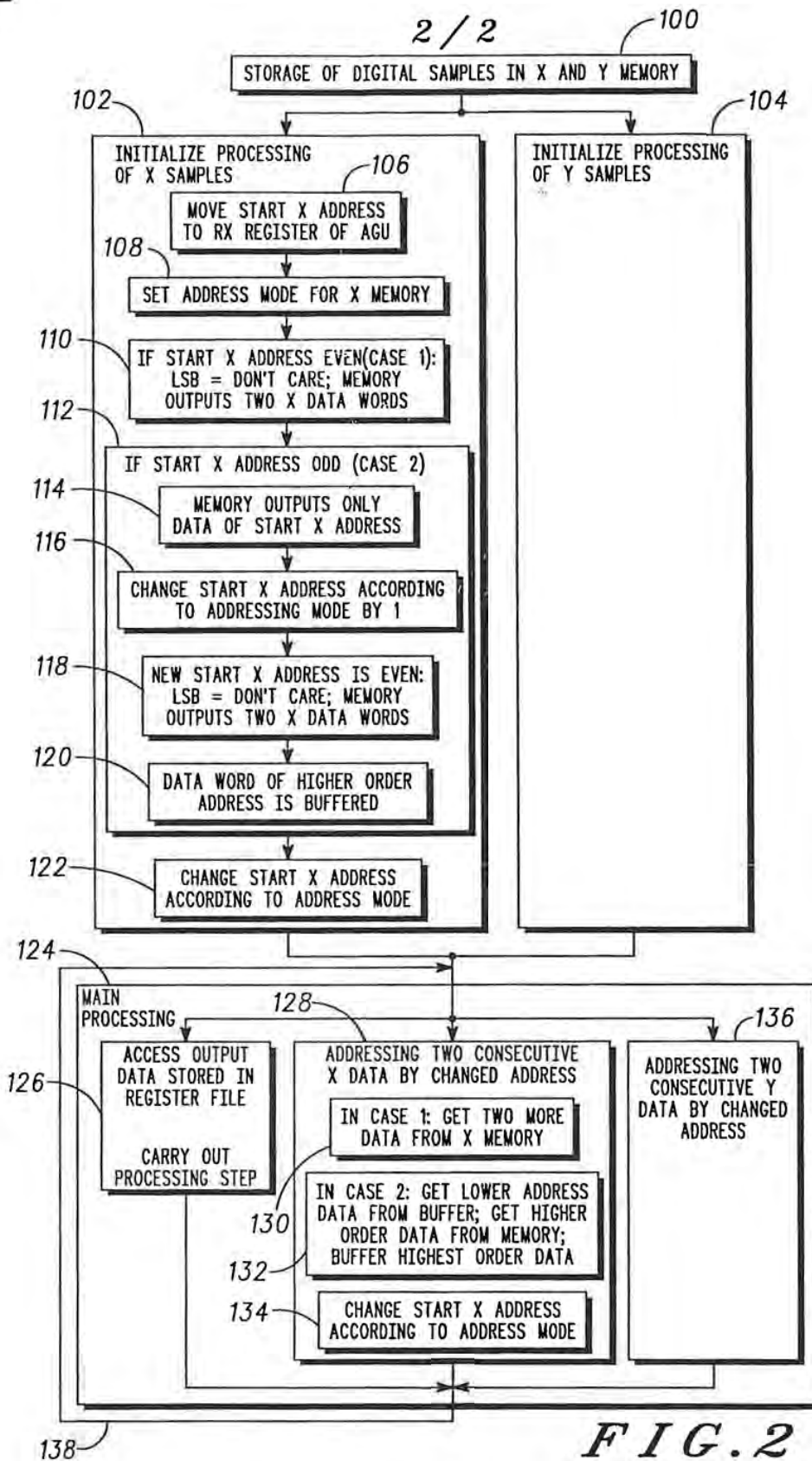


FIG. 2

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US006145070A

United States Patent [19]
Halahmi et al.

[11] **Patent Number:** 6,145,070
[45] **Date of Patent:** Nov. 7, 2000

[54] **METHOD FOR DIGITAL SIGNAL
PROCESSING, DSP, MOBILE
COMMUNICATION AND AUDIO-DEVICE**

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Motorola Semiconductor Technical Data, Advance Information DSP56301, p. 01, Motorola Inc., 1995.

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[21] **Appl. No.:** 08/912,243

[57] **ABSTRACT**

[22] **Filed:** Aug. 15, 1997

The invention relates to a digital signal processor in which two multiply accumulate operations are carried out in one machine cycle. Only one address generation unit is required for addressing two data words of both the X and Y memories, since in the main processing loop the least significant address bit is considered as "Don't care", so that an access operation to the memory results in two output data words at a time.

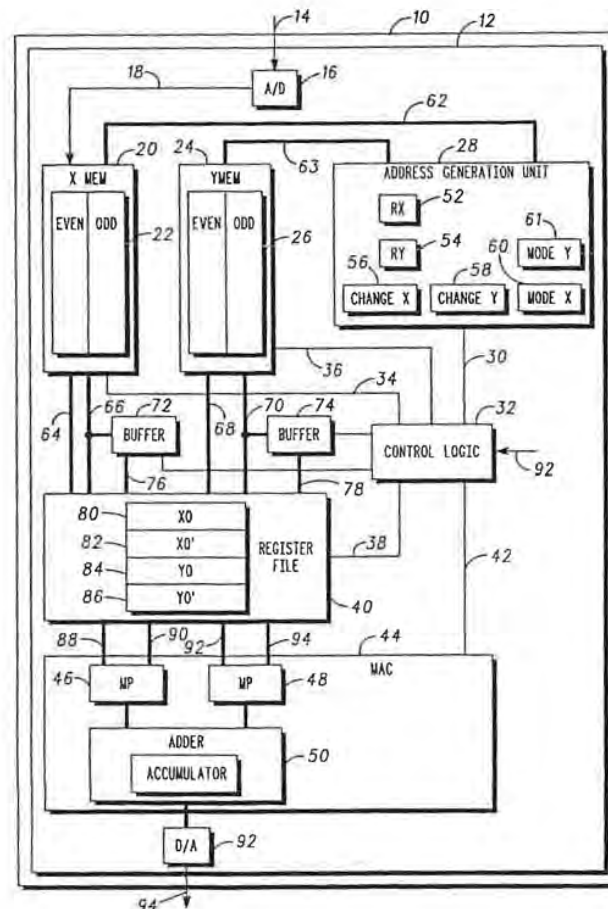
[51] **Int. Cl.⁷** G06F 12/00
[52] **U.S. Cl.** 711/217; 711/5
[58] **Field of Search** 711/217, 218,
711/219, 2, 5

[56] **References Cited**

U.S. PATENT DOCUMENTS

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10 Claims, 2 Drawing Sheets



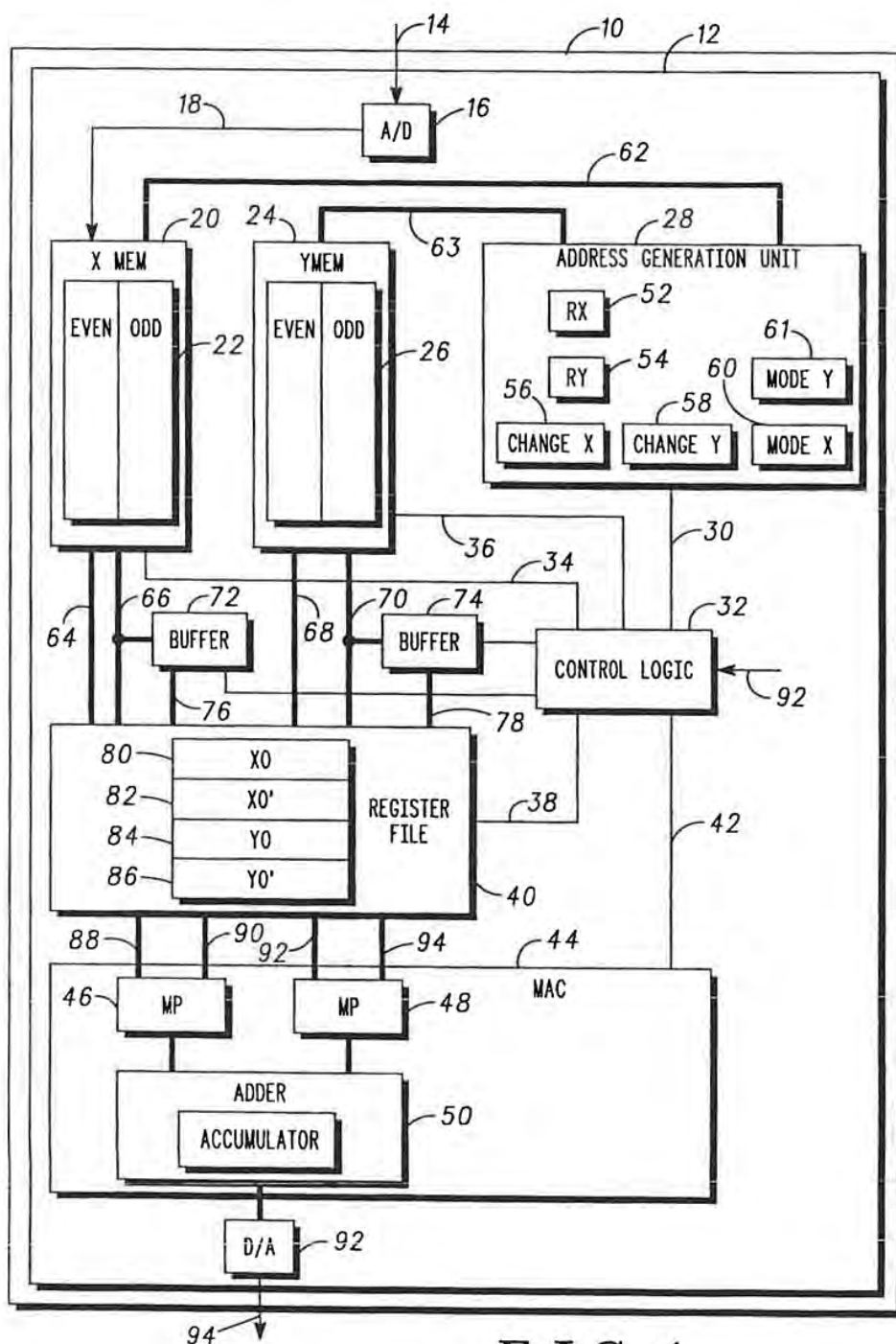


FIG. 1

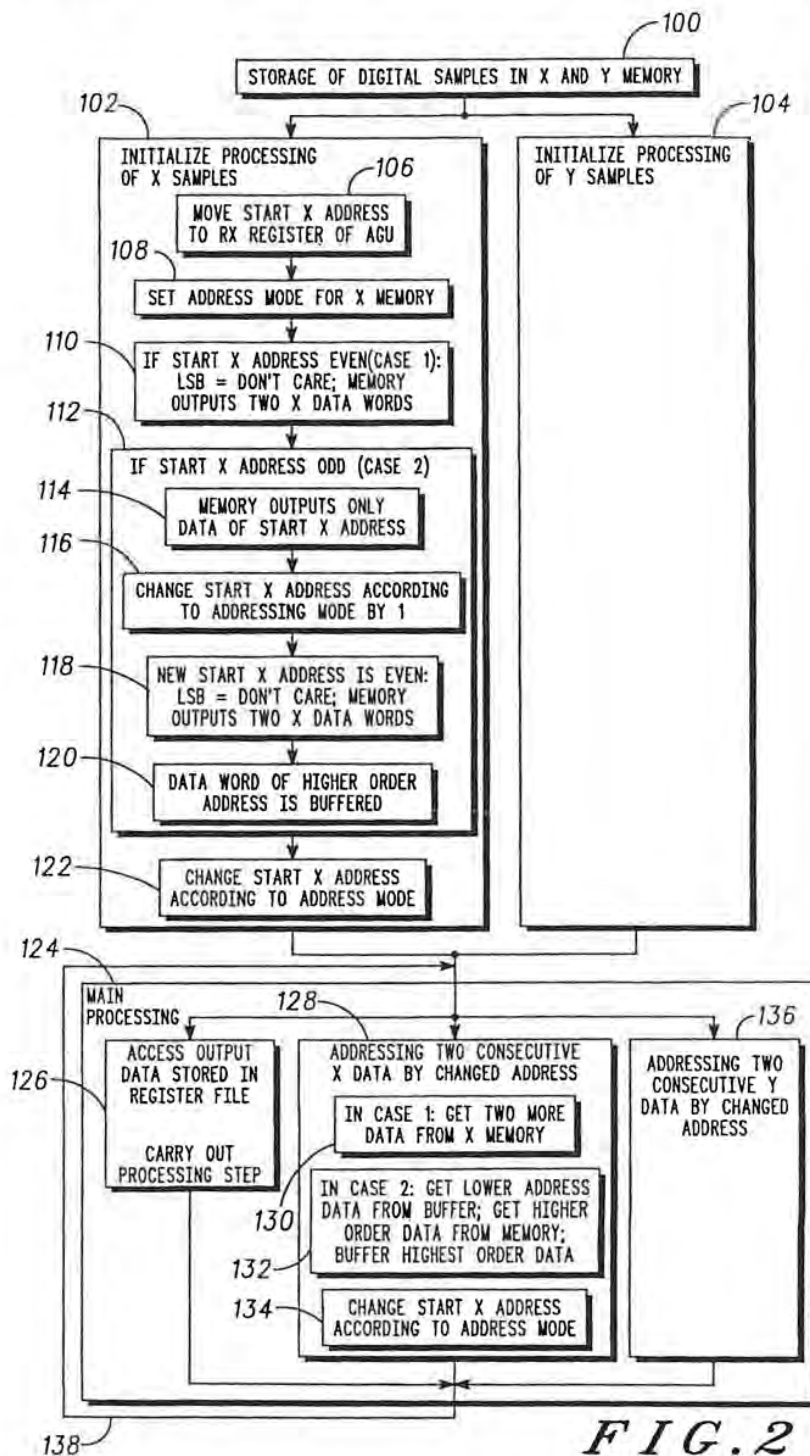


FIG. 2

METHOD FOR DIGITAL SIGNAL PROCESSING, DSP, MOBILE COMMUNICATION AND AUDIO-DEVICE

FIELD OF INVENTION

This invention relates generally to a field of digital signal processing, and more particularly to digital signal processing operations requiring memory access to consecutive data words.

BACKGROUND OF THE INVENTION

In the digital signal processing technology typically one or more analog signals which are representative of some real physical property are filtered or undergo some other kind of arithmetic evaluation or transformation. For this purpose, it is necessary to sample the incoming analog signals. For each analog signal this results in a continuous stream of digital samples. Furthermore, it is known in the art to store such separate sequences of digital samples separately from each other in different memories or in the same memory but separated address spaces. An example for micro processors which incorporate these principles is the DSP 56300 family of 24-bit digital signal processors which are commercially available from Motorola, Inc.

Digital signal processors are applied in virtually all fields of technology and apparatuses. One application is to replace the functionality of an analog device, such as an analog filter, by a digital filter which allows for an enhanced quality and more compact design. Other fields are for digital audio devices, such as compact disc players or digital audio tapes, as well as communication devices, such as mobile telephones or radios. Such applications typically require a high processor throughput, either because of the high band width of the sample's analog signal or because of the complexity of the digital transformations to be carried out on the sampled signal or a combination of both.

A need therefore exists to increase the performance of digital signal processors.

SUMMARY OF THE INVENTION

The underlying problem of the invention is substantially met by applying the features laid down in the independent claims. Preferred embodiments are given in the dependent claims.

The invention is advantageous in that it allows to significantly improve the processing performance of a digital signal processor by adding only minimal hardware.

According to a preferred embodiment of the invention, four data accesses can be carried out in a single processing cycle. The corresponding data sequences can be processed in a finite impulse response type processing step which typically involves data processing in multiply-accumulate loops. Preferably two multiplication units are used, each of which can multiply two of the data words provided in each cycle. The results of the two multiplications is added and accumulated.

If the architecture of a digital signal processor designed in accordance with the principles of the invention is pipelined, this allows two multiply-accumulate operations in one cycle without increasing the clock frequency. As a consequence, such a digital signal processor is also advantageous with respect to power dissipation. This is particularly beneficial for battery powered applications, since the minimized power dissipation of the digital signal processor allows longer intervals between recharging the battery.

Furthermore, it is particularly advantageous that only a single address generation unit is required even though at least two data words can be accessed from each memory device or address region in a memory device. Thus, by using only a single address generation unit, up to four data words can be accessed in a single cycle.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic block diagram of a first embodiment of a digital device including a digital signal processor designed in accordance with the principles of the invention; and

FIG. 2 is a flow diagram which illustrates one embodiment of the method of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

With reference to FIG. 1 a digital device 10 which incorporates a digital signal processor 12 is explained in detail. The digital device 10 can be for example and not intended to be limiting a digital audio device, such as a compact disc player, or a digital communication device, such as a mobile telephone or radio.

In the later case typically an analog signal is received from an antenna of the digital device 10. Such a signal is shown as signal 14 in FIG. 1. The signal is fed into analog-digital converter 16. The samples of the signal 14 delivered by the analog-digital converter 16 are inputted via data line 18 into a memory 20. The memory 20 has a storage array 22. The sampled data words which are inputted via data line 18 to the memory 20 are stored in the address space of the storage array 22 in consecutive order. This means that the first data word, which is inputted into the storage array 22, is stored at the lowest order address and that consecutive further data words are stored at increasing addresses. Other address schemes are also possible such as starting with the highest address and filling up the storage array 22 at consecutive storage locations of decreasing addresses.

The address space of the storage array 22 is logically divided into even and odd addresses. The same applies analogously for memory 24 which has a storage array 26. The memory 24 can serve to store data words which are representative of samples of another input signal or of filter coefficients to be used in the digital signal processing of the signal 14.

In the case of a digital audio device, such as a compact disc player, the signal 14 provided by the laser beam which scans the rotating compact disc is already digital information so that no analog-digital converter 16 is required. Instead the signal 14 is directly inputted into memory 20 without a need for analog to digital conversion.

For the addressing of the memories 20 and 24, the digital signal processor 12 has address generation unit 28 which is coupled via control line 30 to control logic 32. The control logic 32 is also coupled via the control lines 34 and 36 to the memories 20 and 24, respectively. Control line 38 couples the control logic 32 to register file 40 whereas control line 42 couples the control logic 32 to a multiply accumulator 44. The multiply accumulator 44 has multipliers 46 and 48 having their outputs connected to an adder-accumulator 50.

The address generation unit 28 has a register 52 for storage of an address for the memory 20 and a register 54 for storage of an address for the memory 24. Further the address generation unit 28 has registers 56 and 58 to specify the amount of change required for the addresses stored in

register 52 and 54, respectively, for the next processing interval. In registers 60 and 61 the mode in which the address generation unit 28 operates is specified.

The address generation unit 28 is connected by address buses 62 and 63 to the memories 20 and 24, respectively. Both of the memories 20 and 24 have two data buses for outputting data: memory 20 is connected by data buses 64 and 66 to the register file 40 whereas memory 24 is connected by data buses 68 and 70 to the register file 40. The data buses 66 and 70 are also coupled to buffers 72 and 74, respectively. The buffers 72 and 74 are connected to the register file 40 by the data buses 76 and 78.

The register file 40 has registers 80, 82, 84 and 86. Each of these registers can store one data word. The registers 80 and 82 are coupled via data lines 88 and 90 to the multiplier 46. Likewise the registers 84 and 86 are coupled via data lines 92 and 94 to the multiplier 48.

The result of a digital signal processing operation is outputted by adder 50 to digital-analog converter 92. The resulting analog signal 94 is the result of the digital signal processing operation carried out on the signal 14.

In operation the control logic 32 controls the processing of the incoming signal 14 according to the required digital signal processing operation.

In order to initialize the required digital signal processing operation the start addresses for both the memory 20 and the memory 24 have to be specified. For simplicity, the memory 20 and 24 will be referred to as X MEM and Y MEM, respectively, whereas the registers 52 and 54 will be referred to as RX and RY, respectively. The registers 80, 82, 84, and 86 of the register file 40 will be referred to as X0, X0', Y0 and Y0', respectively.

The start address for the required data sequence to be outputted from the X MEM is programmed in the register RX by the control logic 32 via control line 30. The start address for the required data sequence from the Y MEM is programmed in the register RY also by means of the control logic 32 via control line 30.

The control logic 32 checks the start address stored in the RX whether it is an even or an odd address. If the start address for the X MEM is even, the parameter CHANGE X which is stored in the register 56 is set to a value of 2—provided that the addressing mode is incremental.

If the start address for the X MEM is odd, the value of the parameter CHANGE X is set to be equal to the value 1 by the control logic 32 via control line 30—again provided that the addressing mode is incremental. The same check is carried out for the start address stored in the RY. If the start address for the Y MEM is even, the parameter CHANGE Y stored in the register 58 is set to be equal to the value of 2; if the start address for the Y MEM is odd, the value of CHANGE Y is set to be equal to the value of 1—analogueous to the process carried out for the start address for the X MEM.

The parameters MODE X and MODE Y are stored in the registers 60 and 61, respectively. The parameters MODE X and MODE Y specify the addressing mode for the X MEM and the Y MEM, respectively. If, for example, the value of MODE X is equal to 0, this means that the data words are to be outputted from the X MEM in increasing address order, so that after each iteration the address stored in the RX is incremented by the value specified by the parameter CHANGE X. Likewise, if the value of MODE X is logically 1, this means that the address stored in X is decremented after each processing interval by the value as specified by CHANGE X. The same applies analogously to the setting of

the parameter MODE Y in the register 61. Both parameters MODE X and MODE Y are set via the control line 30 by the control logic 32.

Thus, during an initialization interval the start addresses for the sequence of data words to be outputted from X MEM and Y MEM are programmed in the registers RX and RY, respectively, as well as the corresponding parameters CHANGE X, CHANGE Y, MODE X and MODE Y.

If, for example, the start address for the X MEM is even and MODE X equals logically 0 (incrementing address mode), the data word which comes next after the data word having the start address stored in RX has an address which is incremented by 1 with respect to the first data word in the sequence. As a consequence, the second data word in the X MEM sequence has an address which is odd and thus differs only in its least significant bit from the start address stored in RX. Since both address words are required for the processing, it is signaled to the X MEM via control line 34 to output both the data word stored on the start address stored in RX and the consecutive data word being stored on the address next to the start address which differs only in its least significant bit in response to the reception of an address via the address bus 62. In other words: If the control line 34 is raised, the least significant bit line of the address bus 62 becomes a "Don't care" bit, since both data words having an address matching all the higher order address bits will be outputted by the X MEM. As a consequence two data words are outputted from X MEM during one initialization interval, so that for the next interval the address has to be increased by 2 in order to output the consecutive two data words of the required sequence from the X MEM.

If the start address RX is odd and the address mode X is logically 0 (incrementing address mode), this means that there is no data word in the required output sequence which has an address that differs only in its least significant bit from the start address of the sequence stored in RX. As a consequence, the control line 34 is dropped by the control logic 32 to logically 0, so that the X MEM only outputs the data word being stored on exactly the start address stored in RX, but no other data word. Since only one data word is outputted in this alternative first initialization interval, the value of CHANGE X is set to be equal 1, so that for the next initialization interval the value of the address stored in RX is incremented only by 1. After this increment operation has been carried out, the address stored in RX no longer is odd, but even. As a consequence the control line 34 is raised, so that in response to the reception of the even address stored in RX via the address bus 62 again the least significant address bit becomes a "Don't care" bit position, so that the X MEM outputs two data words at a time in the alternative second initialization interval. As a consequence in this alternative case two initialization intervals are required as opposed to the first case considered here in which only one initialization interval is required before the main processing loop can be entered.

Whether the first or the second case is present can be determined according to the following table

	LSB	MODE
CASE 1	0	incremental (+)
	1	decremental (-)
CASE 2	0	decremental (-)
	1	incremental (+)

where the column LSB stands for the least significant bit of the address stored in RX and MODE for the addressing mode.

The logic of the above table can advantageously be implemented within control logic 32 by a XOR gate which is not shown in the drawing. If one input terminal of the XOR gate receives the logical value of the parameter MODE X and the other input terminal receives the least significant bit of the address which is stored in the RX, the resulting output of the XOR gate is logically 1 to indicate the first case and logically 0 in the second case.

Thus, the output of such a XOR gate within control logic 32 can serve to determine which of the two cases mentioned above is present.

The same applies analogously for the Y MEM and the corresponding programming of the address generation unit and issuing of control signals via control line 36 to the Y depending on whether the least significant bit of the address bus 63 is relevant or "Don't care". Also the control logic 32 can comprise an additional XOR gate which has MODE Y and the least significant address bit of the address stored in RY as input signals. Again the output of this additional XOR gate is 1 in the first case and 0 in the second case as described above.

If the first case is present, for both the X MEM and the Y MEM the total time period required for the initialization is just one initialization interval. If either for the X MEM or the Y MEM or for both the second case is present, an additional initialization interval is required as described above.

If the first case is present for the X MEM, the two data words which are outputted from X MEM in the same initialization interval are transferred via the data busses 64 and 66, respectively, to the registers X0 and X0'. If the same applies for the Y MEM, correspondingly two output data words are transferred via the data busses 68 and 70 and stored in the registers Y0 and Y0'.

If, however, the case 2 is present for the Y MEM, only one data word is outputted in the first initialization interval from Y MEM. In the consecutive second initialization interval two data words are outputted only one of which is to be stored in the register file 40. The other output data word is intercepted in the buffer 74 by control logic 32. The same applies analogously if the second case is present for the X MEM, so that one of the data words which are outputted in the second initialization interval is intercepted by buffer 72 which is also controlled by the control logic 32.

After the initialization phase is completed, each register X0, X0', Y0, Y0' of the register file 40 carries one data word. Now the operation of the multiply accumulator 44 can start in the main processing loop. In the main processing loop the required digital signal processing operation is carried out by means of the multiplier accumulator 44. Typically, such digital signal processing operations are finite impulse response signal processing operations. When the main processing loop starts in the first processing interval, the data stored in registers X0 and X0' is transferred via the data lines 88 and 90 respectively, to the multiplier 46. Likewise the data stored in registers Y0 and Y0' are transferred via the data lines 92 and 94, respectively, to the multiplier 48. The output of the respective multiplications is transferred to adder-accumulator 50 in which the two outputs of the multipliers 46 and 48 as well as the value stored in the accumulator are added and stored back into the accumulator. The presence of two multipliers 46 and 48 has the advantage that two multiplications can be carried out within the same time interval. After the completion of such two parallel multiplications another set of four data words is required to be transferred to the multipliers 46 and 48. This is accomplished by the control logic 32.

If the case 1 was present in the initialization interval, each output operation of two data words results in an increase of

the addressed store in RX by 2, so that in the consecutive time interval the consecutive two data words of the required sequence are outputted and stored in the appropriate registers of register file 40. If, however, the case 2 was present during the initialization interval, one of the required data words is already present in the buffer 72 or 74—depending on whether the second case was present for the X MEM or the Y MEM. Carrying out the next processing cycle in the main loop, the data word stored in the buffer 72 or 74 is transferred to the register file 40 to be stored in the appropriate register. Also after the completion of the initialization interval in the second case, the value of CHANGE X or CHANGE Y has been set to 2, so that the value of the address stored in RX or RY is changed by 2 after each output operation. As a consequence one of the data words of the pair of data words outputted by the corresponding memory is transferred to the register file 40 and the other one stored as a replacement in the buffer 72 or 74 depending on which one of the memories X MEM or Y MEM the second case applies. Therefore, also in the second case one multiplication and accumulation operation can be carried out in the main processing loop with four operands due to this pipelined structure.

As a result the throughput of the digital signal processor 12 is doubled as compared to a prior art signal processor having just one multiplication unit. This is accomplished by adding only a minimal number of hardware elements.

In the following, a digital processing operation according to formula (1)

$$a = \sum_{i=0}^5 \sum_{j=0}^5 (x[i] \cdot y[j]), \quad (1)$$

is described by way of example, where $x[i]$ refers to the data word stored in the X MEM on the address i and $y[j]$ refers to data word stored in Y MEM on the address j . According to the formula (1), a total of six multiplications and summations has to be carried out in order to calculate the value of a . In order to prepare the execution of the digital signal processing operation according to formula (1) the digital signal processor 12 has to be initialized by the control logic 32. For this purpose the control logic 32 receives input commands from a user or from a program control at its input 92. By the instruction (i1)

move #0, RX (i1)

the address $i=0$ is moved to the register RX as a start address for the sequence of data words to be outputted from X MEM. Likewise the instruction (i2)

move #1, RY (i2)

causes the control logic 32 to move the address 1 into the register RY as a start address of the sequence of data words to be outputted from Y MEM. The instruction (i3)

clr a (i3)

causes the control logic 32 to issue a control signal via control line 42 to clear the value a , which is stored in the accumulator of the adder-accumulator 50. Next the instruction (i4)

move 2 x: (RX) ← X0 y: (RY) ← Y0 (i4)

is received by the control logic 32 at its input 92. This instruction means that the data word being stored on the

address of the register RX is to be moved from the X MEM to the register X0. Further, as it is indicated by (RX)+the addressing mode is incrementing, so that the parameter MODE X is set to logically 1. Further, the fact that X0 is part of the instruction (i4) indicates that the consecutive data word of the incremented starting address is to be moved to X0'. The same applies analogously for the part y: (RY)+, Y0 of the instruction i4 which relates to the data words in the Y MEM.

As the start address for the sequence of data words to be outputted from X MEM in the register RX is even, the case 1 is present for X MEM, so that the least significant bits of the addresses outputted by address generation unit 28 via the address bus 62 is "Don't care". As a consequence—as described above in more detail—the two data words x[0] and x[1] are outputted concurrently from the X MEM via the data busses 64 and 66, respectively. The data word of the address 0 which is x[0] is stored in the register X0 and the data word of the consecutive incremented address 1 which is x[1] is stored in the register X0' under control of the control logic 32 via control line 38. This happens in the first initialization interval.

In parallel to the addressing, outputting and storing of the two first data words of the X MEM data sequence, the Y MEM is also accessed. Since the address stored in the register RY is 1, an odd address is the starting address of the Y MEM output sequence, so that the second case is present. This means that only the first data word of the Y MEM sequence can be addressed, outputted and stored in the register file during the first initialization interval because the least significant bit position of the address stored in RY is relevant.

After the data word Y[1] has been outputted from the Y MEM the parameter CHANGE Y stored in the register 58 is set to be equal 1, so that the address stored in RY is incremented by 1. As a consequence in the following second initialization interval the two consecutive data words y[2] and y[3] are outputted. The address word y[2] is stored in the register Y0' in the register file 40—the data word y[1] has already been stored in the previous first initialization interval in the register Y0 as specified by the instruction i(4). Since at this time the data word y[3] is not yet needed, it is stored in the buffer 74 for usage in a consecutive processing interval.

After the buffering of the data word y[3], the second initialization interval is completed, so that the main processing loop can be started. The parameter CHANGE Y will also be set two 2 because in the following always two data words are to be outputted at a time from Y MEM.

The main processing loop can be started by the control logic 32 after an instruction (i5)

$\text{mac2 X0, Y0, a X: (RX)+, X Y: (Y)+, Y0}$ (i5)

has been received. According to the instruction i(5), the data words of the registers X0 and Y0 have to be multiplied and accumulated as well as the data words stored in registers X0' and Y0'. The corresponding multiplications are carried out by multipliers 46 and 48, and the accumulation by the adder-accumulator 50. Further, the instruction i(5) specifies that after each processing step the address stored in register RX has to be incremented by 2 as well as the address stored in register RY. This is made clear by the symbols (RX)+ and (RY)+, respectively, instruction i(5). Also it is specified that the first data word having the lower address is stored in the register X0 and Y0, respectively, and the higher order address data word in the registers X0' and Y0', respectively. If instead of the "+"—sign a "—"—sign would be present, this would have the opposite meaning.

When the instruction i(5) is carried out the first time by the multiply accumulator 44, the following over all calculation is performed:

$$a_i = a + x[0] \cdot y[1] + x[1] \cdot y[2]$$

This means that in one processing interval two consecutive data words of both the X and the Y MEM sequence are processed. Since at this stage both parameters CHANGE X and CHANGE Y have been set to be equal 2, in the next processing step the next pair of two data words of each sequence is processed—in other words:

$$a_i = a + x[2] \cdot y[3] + x[3] \cdot y[4]$$

After a further increase of both the addresses stored in RX and RY, the next processing interval already yields the final result for a:

$$a_i = a + x[4] \cdot y[5] + x[5] \cdot y[6]$$

Since the case 1 is present for the X MEM (the X start address is odd), all the data words from X MEM are directly transferred to the register file 40. As opposed to this, the data words y[3] and y[5] are sequentially buffered in the buffer 74 prior to their transfer to register file 40.

In the following with reference to FIG. 2 one embodiment of the method of the invention is described in greater detail.

In step 100 digital samples are stored in the X and Y Memory. In step 102 the processing of the samples stored in the X Memory is initialized; likewise the processing of the samples stored in the Y Memory is initialized in step 104. In the following the initialization processing is only explained in detail with respect to the samples stored in the X Memory, but not for the Y samples, since both processes carried out in step 102 and step 104 in parallel are analogous.

For the initialization first the start address of the sequence of data words to be outputted is moved into the register RX of the address generation unit (AGU). This is done in step 106. In step 108 the address mode for the X Memory is set to be either incrementing or decrementing depending on whether the output sequence starts on top or on the bottom of the address range.

In step 110 it is checked whether the start address of the sequence to be outputted from the X Memory is even. If the address stored in the RX register is even, this means that the least significant bit of this address is "Don't care". When the X Memory is accessed by an even start address in step 110, this results in an output of two data words from the X Memory having the same address bits except the least significant address bit.

If the start address stored in the register RX is odd, this means that case 2 is present, since at the same time the address mode is incrementing. This means that the least significant bit of the start address is relevant, so that only a data word of the start address stored in RX is outputted from the X Memory in step 114. In step 116 the address stored in RX is incremented by 1, so that an even address stored in RX results. As a consequence the least significant bit of the new address stored in RX becomes "Don't care". As a consequence in the next initialization step 118 the memory outputs the next two consecutive data words of the output sequence from the X Memory whereby the two data words have an address which differs only in the least significant bit from each other. Since the data word having the higher address is not yet required at this stage, it is buffered in step 120 for later use. In step 122 the address stored in the register RX is incremented by 2 according to the selected incrementing address mode irrespective of whether case 1 or case 2 is present.

After the initialization phase two data words from the output sequence of the X Memory as well as from the Y Memory are available for processing. As a consequence the main processing 124 is started. In step 126 the available X and Y Memory output data is accessed from the register file and processed according to the required digital signal processing operation. At the same time two consecutive data words in the required output sequence from the X Memory are addressed and outputted from the X Memory. If the case 1 is present, this is done in step 130 by getting two more data words from the X Memory whereby the two more data words have an address which differs only in its least significant bit.

If the case 2 is present the lower order address data word is fetched from the buffer and the higher order data word from X Memory, the further data word which is also outputted from the X Memory at the same time and which has an address which is incremented by 1 with respect to the higher order data word is buffered to replace the previous lower order address data word. This is done in step 132. In step 134, the address stored in the register RX is incremented by 2 again, according to the applicable addressing mode. The operations carried out in step 128 are carried out the same way for the Y Memory in step 136. Step 136 is carried out in parallel to the steps 126 and 128. After the steps 126, 128, and 136 have been carried out, a further iteration 138 of the main loop is initiated so that the step 124 is repeated for a number of times required to complete the digital signal processing operation as specified.

Typically the initialization intervals as well as the processing intervals referred to above are carried out in one machine cycle only. If a pipelined implementation is chosen, this means that in each machine cycle two accumulate-multiply operations can be carried out.

We claim:

1. A method for carrying out a digital signal processing operation, said operation requiring consecutive data words for each processing interval, said data words being stored in a memory device, said method comprising the steps of:

in a first initialization interval:

addressing a first data word by a first address, said first data word having a consecutive second data word having a second address;

in a case 1: if said second address differs only in its least significant bit from said first data address,

outputting said first and second data words from said memory device;

storing said first and second data words in a register file;

in a case 2: if said case 1 is not present,

outputting said first data word; storing said first data word in said register file; changing said first address by one;

in a second initialization interval:

addressing said second data word by said changed first address;

outputting said second data word and a consecutive third data word;

storing said second data word in said register file and storing said third data word in a buffer register;

in a first processing interval:

accessing said data words stored in said register file for carrying out a digital signal processing step;

changing said first address by two;

addressing two further consecutive data words by said changed first address;

in said case 1:

storing said further consecutive data words in said register file;

in said case 2:

storing said data word of said buffer register in said register file;

storing one of said further consecutive data words in said register file;

storing the other one of said further consecutive data words in said buffer;

carrying out as many of said processing intervals as required to complete said digital signal processing operation.

2. The method according to claim 1 said digital signal processing operation requiring at least two sequences of said consecutive data words, said data words of different sequences being stored in memory devices which are separately addressable, said method being carried out for each of said sequences, whereby said register file is a common file for all data words.

3. The method according to claim 2 said digital signal processing step being a multiply accumulate processing step.

4. The method according to claim 1 whereby either a decrementing or incrementing address mode is used, said method further comprising the step of XORing said address mode and the least significant bit of said first address in order to determine said case 2.

5. A digital signal processor comprising

a digital signal processing core;

a memory device for storing a sequence of consecutive data words;

an address generation unit for generating addresses for said memory device;

an output buffer register for said memory devices;

a register file coupled to said memory device, to said output buffer register and to said digital signal processing core;

a control logic coupled to said memory device, to said address generation unit, to said digital signal processing core and to said output buffer register, said control logic being adapted to control input/output operations for said data words into/from said register file according to the following control scheme:

in a first initialization interval:

for a first address of a first data word of said sequence which is generated by said address generation unit, said first data word having a consecutive second data word of a second address;

in a case 1: if said second address differs only in its least significant bit from said first data address, causing said memory device to output said first and second data words;

inputting said first and second data words into said register file;

in a case 2: if said case 1 is not present,

causing said memory device to output said first data word; inputting said first data word into said register file; causing said address generation unit to change said first address by one;

in a second initialization interval:

causing said address generation unit to address said second data word by said changed first address; causing said memory device to output said second data word and a consecutive third data word;

inputting said second data word into said register file and storing said third data word in a buffer register;

in a first processing interval:

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causing said register file to output said data words to said digital signal processing core for carrying out a digital signal processing step;
 causing the address generation unit to change said first address by two;
 causing said addressing unit to address two further consecutive data words by said changed first address;
 in said case 1:
 inputting said further consecutive data words into said register file;
 in said case 2:
 inputting said data word of said buffer register into said register file;
 inputting one of said further consecutive data words into said register file;
 storing the other one of said further consecutive data words in said buffer;
 carrying out as many of said processing intervals as required to complete said digital signal processing operation.
 6. The digital signal processor according to claim 5 said digital signal processing core being adapted to process at least two sequences of consecutive data words at a time, said digital signal processor further comprising one of said memory devices for each said sequence of consecutive data words, said register file being adapted to receive data words originating from any of said memory devices under control of said control logic according to said control scheme applied to each one of said memory devices.
 7. The digital signal processor according to claim 6 having two of said memory devices, said digital signal processing core comprising two multipliers being coupled to said register file, each of said multipliers receiving two data words per processing interval from said register file.
 8. The digital signal processor according to claim 5 whereby said control logic causes said address generation unit to operate either in a decrementing or incrementing address mode, said control logic further comprising a XOR logic gate having said address mode and the least significant bit of said first address as inputs, an output signal of said XOR gate determining whether said case 1 or said case 2 is present.
 9. A communication device comprising sender and/or receiver means to send and/or receive a signal and a signal processor for digitally processing said signal, said signal processor comprising
 a digital signal processing core;
 a memory device for storing a sequence of consecutive data words being representative of said signal;
 an address generation unit for generating addresses for said memory device;
 an output buffer register for said memory devices;
 a register file coupled to said memory device, to said output buffer register and to said digital signal processing core;
 a control logic coupled to said memory device, to said address generation unit, to said digital signal processing core and to said output buffer register, said control logic being adapted to control input/output operations for said data words into/from said register file according to the following control scheme:
 in a first initialization interval:
 for a first address of a first data word of said sequence which is generated by said address generation unit, said first data word having a consecutive second data word of a second address:

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in a case 1: if said second address differs only in its least significant bit from said first data address, causing said memory device to output said first and second data words;
 inputting said first and second data words into said register file;
 in a case 2: if said case 1 is not present, causing said memory device to output said first data word; inputting said first data word into said register file; causing said address generation unit to change said first address by one;
 in a second initialization interval:
 causing said address generation unit to address said second data word by said changed first address; causing said memory device to output said second data word and a consecutive third data word;
 inputting said second data word into said register file and storing said third data word in a buffer register;
 in a first processing interval:
 causing said register file to output said data words to said digital signal processing core for carrying out a digital signal processing step;
 causing the address generation unit to change said first address by two;
 causing said addressing unit to address two further consecutive data words by said changed first address;
 in said case 1:
 inputting said further consecutive data words into said register file;
 in said case 2:
 inputting said data word of said buffer register into said register file;
 inputting one of said further consecutive data words into said register file;
 storing the other one of said further consecutive data words in said buffer;
 carrying out as many of said processing intervals as required to complete said digital signal processing operation.
 10. A digital audio device comprising means for recording and/or reproducing an audio signal and a signal processor for digitally processing said signal, said signal processor comprising
 a digital signal processing core;
 a memory device for storing a sequence of consecutive data words being representative of said signal;
 an address generation unit for generating addresses for said memory device;
 an output buffer register for said memory devices;
 a register file coupled to said memory device, to said output buffer register and to said digital signal processing core;
 a control logic coupled to said memory device, to said address generation unit, to said digital signal processing core and to said output buffer register, said control logic being adapted to control input/output operations for said data words into/from said register file according to the following control scheme:
 in a first initialization interval:
 for a first address of a first data word of said sequence which is generated by said address generation unit, said first data word having a consecutive second data word of a second address:

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in a case 1: if said second address differs only in its
least significant bit from said first data address,
causing said memory device to output said first and
second data words;
inputting said first and second data words into said 5
register file;
in a case 2: if said case 1 is not present,
causing said memory device to output said first data
word; inputting said first data word into said register
file; causing said address generation unit to change 10
said first address by one;
in a second initialization interval:
causing said address generation unit to address
said second data word by said changed first
address; causing said memory device to output 15
said second data word and a consecutive third
data word;
inputting said second data word into said register
file and storing said third data word in a buffer
register; 20
in a first processing interval:

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causing said register file to output said data words to
said digital signal processing core for carrying out a
digital signal processing step;
causing the address generation unit to change said first
address by two;
causing said addressing unit to address two further
consecutive data words by said changed first address;
in said case 1:
inputting said further consecutive data words into said
register file;
in said case 2:
inputting said data word of said buffer register into said
register file;
inputting one of said further consecutive data words
into said register file;
storing the other one of said further consecutive data
words in said buffer;
carrying out as many of said processing intervals as
required to complete said digital signal processing
operation.

* * * * *

APPLICATION TRANSFER REQUEST

Section I. APPLICATION TRANSFER REQUEST

Date _____ S.N. 08/912243

TO: Receiving A.U. _____ Class/sub _____ Examiner _____

FROM: Originating A.U. _____ Class/Sub _____ Examiner _____

REASON:

☐ Request for Reconsideration
(Return to Classification)

Section II. DISPOSITION BY RECEIVING A.U.

Date 2/18/98 EXT [Signature]

☒ Accepted (keep in receiving A.U.)

Not Accepted ☐ Forward to _____ Classification Group _____

☐ Return to Originating A.U. _____ Nonclassification issue only:

REASON:

accepted by Exr.

☐ Restriction
☐ Other

Section III. DISPOSITION BY _____ Classification Group _____ Date _____

Art Unit: 2751

1. The following is an examiner's statement of reasons for allowance:

The closest art of record, namely Kummer (4,609,996) does not teach the present invention including the steps/function for address generation and memory access as outlined in each of independent claims 1, 5, 9 and 10. The steps/function correspond closely with the function found in the flow diagram of figure 2. Kummer's device is limited to data access from the even address and the next higher address.

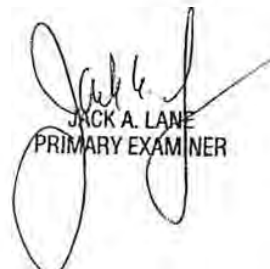
Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

2. Claims 1-10 are allowed over the prior art of record.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jack Lane whose telephone number is (703) 305-3818.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-9600.

JAL
November 23, 1998



JACK A. LANE
PRIMARY EXAMINER

NOTICE OF DRAFTERPERSON'S PATENT DRAWING REVIEW

The drawing filed (insert date) 8/15/97A ☒ not objected to by the Drafterperson under 37 CFR 1.84 or 1.152.B ☒ objected to by the Drafterperson under 37 CFR 1.84 or 1.152 as indicated below. The Examiner will require submission of new, corrected drawings when necessary. Corrected drawings must be submitted according to the instructions on the back of this notice.

- | | |
|---|--|
| <p>1. DRAWINGS. 37 CFR 1.84(a): Acceptable categories of drawings:
Black ink. Color.
Color drawing are not acceptable until petition is granted.
Fig.(s) _____
Pencil and non black ink is not permitted. Fig(s) _____</p> <p>2. PHOTOGRAPHS. 37 CFR 1.84(b)
Photographs are not acceptable until petition is granted,
3 full-tone sets are required. Fig(s) _____
Photographs not properly mounted (must hystol board or photographic double-weight paper). Fig(s) _____
Poor quality (half-tone). Fig(s) _____</p> <p>3. TYPE OF PAPER. 37 CFR 1.84(c)
Paper not flexible, strong, white and durable.
Fig.(s) _____
Erasures, alterations, overwritings, interlineations, folds, copy machine marks not acceptable. (too thin) <u>B-2</u>
Mylar, vellum paper is not acceptable (too thin).
Fig(s) _____</p> <p>4. SIZE OF PAPER. 37 CFR 1.84(F): Acceptable sizes:
21.0 cm by 29.7 cm (DIN size A4)
21.6 cm by 27.9 cm (8 1/2 x 11 inches)
All drawings sheets not the same size.
Sheet(s) _____</p> <p>5. MARGINS. 37 CFR 1.84(g): Acceptable margins:
Top 2.5 cm Left 2.5 cm Right 1.5 cm Bottom 1.0 cm
SIZE: A4 Size
Top 2.5 cm Left 2.5 cm Right 1.5 cm Bottom 1.0 cm
SIZE: 8 1/2 x 11
Margins not acceptable. Fig(s) _____
Top (T) _____ Left (L)
Right (R) _____ Bottom (B)</p> <p>6. VIEWS. CFR 1.84(h)
REMINER: Specification may require revision to correspond to drawing changes.
Views connected by projection lines or lead lines.
Fig.(s) _____
Partial views. 37 CFR 1.84(h)(2)
Brackets needed to show figure as one entity.
Fig.(s) _____
Views not labeled separately or properly.
Fig.(s) _____
Enlarged view not labeled separately or properly.
Fig.(s) _____</p> | <p>7. SECTIONAL VIEWS. 37 CFR 1.84(h)(3)
Hatching not indicated for sectional portions of an object.
Fig.(s) _____
Sectional designation should be noted with Arabic or Roman numbers. Fig.(s) _____</p> <p>8. ARRANGEMENT OF VIEWS. 37 CFR 1.84(i)
Words do not appear on a horizontal, left-to-right fashion when page is either upright or turned, so that the top becomes the right side, except for graphs. Fig.(s) _____
Views not on the same plane on drawing sheet. Fig.(s) _____</p> <p>9. SCALE. 37 CFR 1.84(k)
Scale not large enough to show mechanism with crowding when drawing is reduced in size to two-thirds in reproduction.
Fig.(s) _____</p> <p>10. CHARACTER OF LINES, NUMBERS, & LETTERS. 37 CFR 1.84(l)
Lines, numbers & letters not uniformly thick and well defined, clean, durable and black (poor line quality).
Fig.(s) _____</p> <p>11. SHADING. 37 CFR 1.84(m)
Solid black areas pale. Fig.(s) _____
Solid black shading not permitted. Fig.(s) _____
Shade lines, pale, rough and blurred. Fig.(s) _____</p> <p>12. NUMBERS, LETTERS, & REFERENCE CHARACTERS. 37 CFR 1.84(p)
Numbers and reference characters not plain and legible.
Fig.(s) _____
Figure legends are poor. Fig.(s) _____
Numbers and reference characters not oriented in the same direction as the view. 37 CFR 1.84(p)(3) Fig.(s) _____
English alphabet not used. 37 CFR 1.84(p)(3) Fig.(s) _____
Numbers, letters and reference characters must be at least .32 cm (1/8 inch) in height. 37 CFR 1.84(p)(3) Fig.(s) _____</p> <p>13. LEAD LINES. 37 CFR 1.84(q)
Lead lines cross each other. Fig.(s) _____
Lead lines missing. Fig.(s) _____</p> <p>14. NUMBERING OF SHEETS OF DRAWINGS. 37 CFR 1.84(r)
Sheets not numbered consecutively, and in Arabic numerals beginning with number 1. Fig.(s) _____</p> <p>15. NUMBERING OF VIEWS. 37 CFR 1.84(u)
Views not numbered consecutively, and in Arabic numerals, beginning with number 1. Fig.(s) _____</p> <p>16. CORRECTIONS. 37 CFR 1.84(w)
Corrections not made from PTO-948 dated _____</p> <p>17. DESIGN DRAWINGS. 37 CFR 1.152
Surface shading shown not appropriate. Fig.(s) _____
Solid black shading not used for color contrast.
Fig.(s) _____</p> |
|---|--|

COMMENTS

REVIEWER WJDATE 12/18/97TELEPHONE NO. 2033058404ATTACHMENT TO PAPER NO. 3

PTO COPY

REMINDER

Drawing changes may also require changes in the specification, e.g., if Fig. I is changed to Fig. IA, Fig. IB, Fig. IC, etc., the specification, at the Brief Description of the Drawings, must likewise be changed. Please make such changes by 37 CFR 1.312 Amendment at the time of submitting drawing changes.

INFORMATION ON HOW TO EFFECT DRAWING CHANGES

1. Correction of Informalities--37 CFR 1.85

File new drawings with the changes incorporated therein. The application number or the title of the invention, inventor's name, docket number (if any), and the name and telephone number of a person to call if the Office is unable to match the drawings to the proper application, should be placed on the back of each sheet of drawings in accordance with 37 CFR 1.84(c). Applicant may delay filing of the new drawings until receipt of the Notice of Allowability (PTOL-37). Extensions of time may be obtained under the provisions of 37 CFR 1.136. The drawing should be filed as a separate paper with a transmittal letter addressed to the Drawing Review Branch.

2. Timing of Corrections

Applicant is required to submit acceptable corrected drawings within the three-month shortened statutory period set in the Notice of Allowability (PTOL-37). If a correction is determined to be unacceptable by the Office, applicant must arrange to have acceptable correction resubmitted within the original three-month period to avoid the necessity of obtaining an extension of time and paying the extension fee. Therefore, applicant should file corrected drawings as soon as possible.

Failure to take corrective action within set (or extended) period will result in ABANDONMENT of the Application.

3. Corrections other than Informalities Noted by the Drawing Review Branch on the Form PTO 948

All changes to the drawings, other than informalities noted by the Drawing Review Branch, **MUST** be approved by the examiner before the application will be allowed. No changes will be permitted to be made, other than correction of informalities, unless the examiner has approved the proposed changes.

=> d his

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(FILE 'USPAT' ENTERED AT 08:31:53 ON 23 NOV 1998)
L1      192384 S ADDRESS?
L2      349549 S SEQUENC?
L3      26485 S ODD(P) EVEN
L4      75874 S CONSECUTIVE?
L5      625 S L1(P) L2(P) L3
L6      625 S L5 AND L3
L7      1311 S L1(P) L2(P) L4
L8      303 S L7 AND L3
L9      3433 S REGISTER(2A) FILE
L10     41 S L9 AND L8
L11     6536 S L1(P) L4
L12     261 S L11(P) L3
L13     34 S L12 AND L9
L14     4 S L12(P) L9
L15     15317 S (CHANG? OR INCREMENT OR ADD) (3A) ADDRESS?
L16     334 S L15(P) L11
L17     19 S L16(P) L3
L18     135 S L16(P) (L9 OR BUFFER? OR REGISTER?)
L19     2 S L16(P) L9
L20     284 S (711*217 OR 711*218 OR 711*219)/CCLS
L21     2 S L18 AND L20
L22     9 S L16 AND L20
L23     63 S L11 AND L20
L24     54 S L23 NOT L22
L25     84 S L16 AND L3
L26     7 S L17 AND L18

FILE 'JPOABS' ENTERED AT 10:56:42 ON 23 NOV 1998
L27     14 S L16

FILE 'EPOABS' ENTERED AT 11:04:48 ON 23 NOV 1998
L28     10 S L16
L29     261 S L11
L30     0 S L9 AND L29
L31     223 S L9
L32     0 S L31 AND L29

FILE 'JPOABS' ENTERED AT 11:10:32 ON 23 NOV 1998
L33     518 S L11
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ABSTRACT:

A microcomputer includes a main memory system which is accessed, substantially independantly, by the CPU and a subsystem, for example a video display subsystem. The memory system comprises a base memory and an optical add on expansion memory. When only the base memory is installed, consecutive locations have consecutively numbered addresses, and both the CPU and subsystem access individual locations. When both memories are installed, one has even numbered addresses and the other odd numbered addresses. With both memories installed, the CPU still accesses individual locations, but the subsystem addresses even addresses to obtain, for each access, data from the even address and the next higher odd address, thereby accessing a location in both memories. Thus the memory bandwidth for the subsystem is effectively doubled

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(FILE 'USPAT' ENTERED AT 13:33:01 ON 23 NOV 1998)

L1	362	S	(ODD AND EVEN)/AB AND (MEMORY OR STORAGE)/AB
L2	28966	S	365*/CCLS OR 711*/CCLS
L3	121	S	L2 AND L1
L4	192384	S	ADDRESS?
L5	23607	S	L4/AB
L6	65	S	L5 AND L3
L7	384315	S	CONSECUTIVE? OR SEQUENCE
L8	37084	S	L7/AB
L9	13	S	L8 AND L6
L10	545399	S	MEMORY OR STORAGE
L11	192384	S	ADDRESS?
L12	78413	S	AUDIO OR VOICE
L13	3506	S	L10(P) L11(P) L12
L14	129639	S	TELEPHONE OR RADIO
L15	525	S	L13(P) L7
L16	114373	S	L10/AB
L17	23607	S	L11/AB
L18	1250	S	L8 AND L17 AND L16
L19	174519	S	L12 OR L14

[19]

Kummer

[11] Patent Number:

[45] **Date of Patent:**

[54] MEMORY ACCESS SYSTEM FOR A COMPUTER SYSTEM ADAPTED TO ACCEPT A MEMORY EXPANSION MODULE

[75] Inventor: David A. Kummer, Boca Raton, Fla.

[73] Assignee: International Business Machines Corporation, Armonk, N.Y.

[21] Appl. No.: 522,893

[22] Filed: Aug. 12, 1983

[51] Int. CL⁴ G06F 13/00

[52] U.S. Cl. 364/900

[58] Field of Search 365/222; 364/200, 900;
340/703, 735, 750, 790

[56] References Cited

U.S. PATENT DOCUMENTS

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4,471,465 9/1984 Mayer et al. ————— 364/900

4,485,457 11/1984 Balaska et al. _____ 364/900

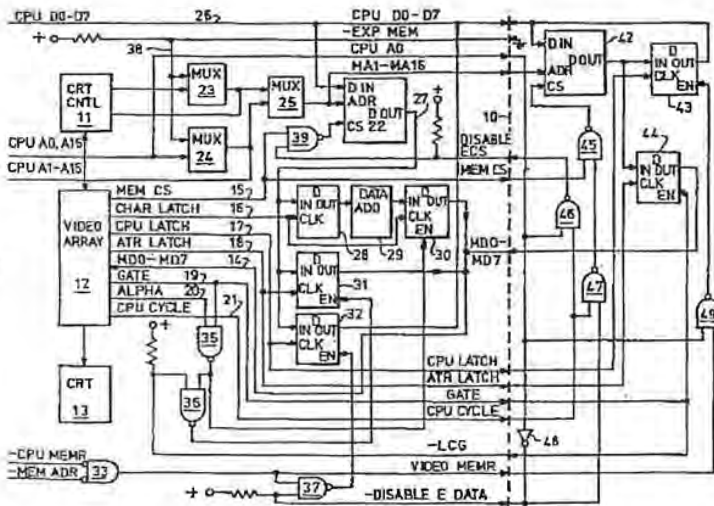
Primary Examiner—James D. Thomas

Assistant Examiner—David L. Clark

[57] **ABSTRACT**

A microcomputer includes a main memory system which is accessed, substantially independently, by the CPU and a subsystem, for example a video display subsystem. The memory system comprises a base memory and an optical add on expansion memory. When only the base memory is installed, consecutive locations have consecutively numbered addresses, and both the CPU and subsystem access individual locations. When both memories are installed, one has even numbered addresses and the other odd numbered addresses. With both memories installed, the CPU still accesses individual locations, but the subsystem addresses even addresses to obtain, for each access, data from the even address and the next higher odd address, thereby accessing a location in both memories. Thus the memory bandwidth for the subsystem is effectively doubled when the expansion memory is installed.

4 Claims, 6 Drawing Figures



APPLICATION TRANSFER REQUEST					
3. TO GROUP ART UNIT	4. EXAMINER (if known)	5. TRANSFER IS REQUESTED FROM	CLASS	TO	CLASS/SUB
24			2152		215-
6. REASON(S) (give details where possible)					
			7. EXAMINER	8. GROUP ART UN	
			K. W. W.	2745	
DISPOSITION OF APPLICATION BY RECEIVING GROUP ART UNIT					
9. ☐ ACCEPTED		☐ FORWARDED TO THE		BY (Examiner)	DATE
☒ NOT ACCEPTED		FOLLOWING DOC. DIV.		RSW	1/27/9
10. REASON(S)					
more reason: getting along = class 711					
DISPOSITION OF APPLICATION BY DOCUMENTATION					
11. ☐ TRANSFER NOT APPROVED, RETURNED TO ORIGINATING GROUP		☒ TRANSFER APPROVED FORWARDED TO: →		GROUP ART UNIT	CLASS/SUB
				2312	711
12. REASON(S) ☐ AS SET FORTH BY ORIGINATING GROUP. ☐ OTHER:					
13. CLASSIFIER	14. DOCUMENTATION DIV.	15. DATE	16. CONCURRING CLASSIFIER		

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**PRIOR ART/OR
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MISCELLANEOUS
DOCUMENTS**

PATENT NUMBER

ORIGINAL CLASSIFICATION

CLASS

SUBCLASS

711

217

APPLICATION SERIAL NUMBER

08/912,243

CROSS REFERENCE(S)

CLASS

SUBCLASS
(ONE SUBCLASS PER BLOCK)

711

5

APPLICANT'S NAME (PLEASE PRINT)

HALAHMI

IF REISSUE, ORIGINAL PATENT NUMBER

INTERNATIONAL CLASSIFICATION

G 06 F

12/00

GROUP
ART UNIT

ASSISTANT EXAMINER (PLEASE STAMP OR PRINT FULL NAME)

PRIMARY EXAMINER (PLEASE STAMP OR PRINT FULL NAME)

2751

JACK A. LANE

PTO 270
(REV. 5-91)

ISSUE CLASSIFICATION SLIP

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

PACE DATA ENTRY CODING SHEET

U.S. DEPARTMENT OF COMMERCE
Patent and Trademark Office

1ST EXAMINER

DATE

2ND EXAMINER

DATE

APPLICATION NUMBER

08/912243



TYPE
APPL

☐

FILING DATE

MONTH	DAY	YEAR

SPECIAL
HANDLING

☐

GROUP
ART UNIT

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SHEETS OF
DRAWING

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TOTAL
CLAIMS

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INDEPENDENT
CLAIMS

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SMALL
ENTITY?

☐

FILING FEE

--	--	--	--

FOREIGN
LICENSE

☐

ATTORNEY DOCKET NUMBER

--	--	--	--	--	--	--	--	--	--	--	--

CONTINUITY DATA

CONT STATUS
CODE CODE

PARENT APPLICATION
SERIAL NUMBER

PCT APPLICATION SERIAL NUMBER

P	C	T	/					/						
P	C	T	/					/						
P	C	T	/					/						
P	C	T	/					/						
P	C	T	/					/						

PARENT PATENT
NUMBER

PARENT FILING
DATE

MONTH	DAY	YEAR

PCT/FOREIGN APPLICATION DATA

FOREIGN
PRIORITY
CLAIMED

COUNTRY
CODE

PCT/FOREIGN APPLICATION SERIAL NUMBER

FOREIGN
FILING DATE

MONTH	DAY	YEAR

[illegible][illegible][illegible]

AUTHORITY CODE		APPLICANT/INVENTOR DATA																												NAME SUFFIX	
FAMILY NAME																															
GIVEN NAME																														STATE/CTRY CODE	
CITY																															

AUTHORITY CODE																														NAME SUFFIX	
FAMILY NAME																															
GIVEN NAME																														STATE/CTRY CODE	
CITY																															

MORE

MORE

PATENT APPLICATION FEE DETERMINATION RECORD

Effective October 1, 1996

Application or Docket Number

912943

CLAIMS AS FILED - PART I

(Column 1)

(Column 2)

FOR	NUMBER FILED	NUMBER EXTRA
BASIC FEE		
TOTAL CLAIMS	10 minus 20 = *	
INDEPENDENT CLAIMS	4 minus 3 = *	
MULTIPLE DEPENDENT CLAIM PRESENT		

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY

OR

OTHER THAN
SMALL ENTITY

RATE	FEE		RATE	FEE
	385.00	OR		770.00
x\$11=		OR	x\$22=	
x40=		OR	x80=	80
+130=		OR	+260=	
TOTAL		OR	TOTAL	850

CLAIMS AS AMENDED - PART II

(Column 1)

(Column 2)

(Column 3)

AMENDMENT A

	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				

SMALL ENTITY

OR

OTHER THAN
SMALL ENTITY

RATE	ADDI- TIONAL FEE		RATE	ADDI- TIONAL FEE
x\$11=		OR	x\$22=	
x40=		OR	x80=	
+130=		OR	+260=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

(Column 1)

(Column 2)

(Column 3)

AMENDMENT B

	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				

SMALL ENTITY

OR

OTHER THAN
SMALL ENTITY

RATE	ADDI- TIONAL FEE		RATE	ADDI- TIONAL FEE
x\$11=		OR	x\$22=	
x40=		OR	x80=	
+130=		OR	+260=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

(Column 1)

(Column 2)

(Column 3)

AMENDMENT C

	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				

SMALL ENTITY

OR

OTHER THAN
SMALL ENTITY

RATE	ADDI- TIONAL FEE		RATE	ADDI- TIONAL FEE
x\$11=		OR	x\$22=	
x40=		OR	x80=	
+130=		OR	+260=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
 ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
 *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
 The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

PARTITION		PARTITION	
1	1	1	1
2	2	2	2
3	3	3	3
4	4	4	4
5	5	5	5
6	6	6	6
7	7	7	7
8	8	8	8
9	9	9	9
10	10	10	10
11	11	11	11
12	12	12	12
13	13	13	13
14	14	14	14
15	15	15	15
16	16	16	16
17	17	17	17
18	18	18	18
19	19	19	19
20	20	20	20
21	21	21	21
22	22	22	22
23	23	23	23
24	24	24	24
25	25	25	25
26	26	26	26
27	27	27	27
28	28	28	28
29	29	29	29
30	30	30	30
31	31	31	31
32	32	32	32
33	33	33	33
34	34	34	34
35	35	35	35
36	36	36	36
37	37	37	37
38	38	38	38
39	39	39	39
40	40	40	40
41	41	41	41
42	42	42	42
43	43	43	43
44	44	44	44
45	45	45	45
46	46	46	46
47	47	47	47
48	48	48	48
49	49	49	49
50	50	50	50
51	51	51	51
52	52	52	52
53	53	53	53
54	54	54	54
55	55	55	55
56	56	56	56
57	57	57	57
58	58	58	58
59	59	59	59
60	60	60	60
61	61	61	61
62	62	62	62
63	63	63	63
64	64	64	64
65	65	65	65
66	66	66	66
67	67	67	67
68	68	68	68
69	69	69	69
70	70	70	70
71	71	71	71
72	72	72	72
73	73	73	73
74	74	74	74
75	75	75	75
76	76	76	76
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78	78	78	78
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80	80	80	80
81	81	81	81
82	82	82	82
83	83	83	83
84	84	84	84
85	85	85	85
86	86	86	86
87	87	87	87
88	88	88	88
89	89	89	89
90	90	90	90
91	91	91	91
92	92	92	92
93	93	93	93
94	94	94	94
95	95	95	95
96	96	96	96
97	97	97	97
98	98	98	98
99	99	99	99
100	100	100	100

MULTIPLE DEPENDENT CLAIM
FEE CALCULATION SHEET
(FOR USE WITH FORM PTO-876)

912243 8-15-97

CLAIMS

	AS FILED		AFTER 1st AMENDMENT		AFTER 2nd AMENDMENT								
	IND.	DEP.	IND.	DEP.	IND.	DEP.		IND.	DEP.	IND.	DEP.	IND.	DEP.
1	/						61						
2		/					62						
3		/					63						
4		/					64						
5	/						65						
6		/					66						
7		/					67						
8		/					68						
9	/						69						
10	/						70						
11							71						
12							72						
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15							75						
16							76						
17							77						
18							78						
19							79						
20							80						
21							81						
22							82						
23							83						
24							84						
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26							86						
27							87						
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29							89						
30							90						
31							91						
32							92						
33							93						
34							94						
35							95						
36							96						
37							97						
38							98						
39							99						
40							100						
41													
42													
43													
44													
45													
46													
47													
48													
49													
50													
TOTAL IND.	4						TOTAL IND.						
TOTAL DEP.	8						TOTAL DEP.						
TOTAL CLAIMS	12						TOTAL CLAIMS						

SEARCHED			
Class	Sub.	Date	Exmr.
711	217 218 219 2 5	11/23/95	JAL
		2	2

SEARCH NOTES		
	Date	Exmr.
APS search enclosed	11/24/98	J.A.L.

INTERFERENCE SEARCHED			
Class	Sub.	Date	Exmr.
711	5 217	11/25/98	J.A.



FPI-LDM



Do
3/16/98

Staple Issue Slip Here

POSITION	ID NO.	DATE
CLASSIFIER	57	10-28-97
EXAMINER	70303	12-17-97
TYPIST	↓	↓
VERIFIER		
CORPS CORR.		
SPEC. HAND		
FILE MAINT.		
DRAFTING		

INDEX OF CLAIMS

Claim	Date
Final	Original
1	11/28/97
2	2
3	3
4	4
5	5
6	6
7	7
8	8
9	9
10	10
11	
12	
13	
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Claim	Date
Final	Original
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SYMBOLS

- ✓ Rejected
- Allowed
- (Through numeral) Canceled
- + Restricted
- N Non-elected
- I Interference
- A Appeal
- O Objected

14
M
SI
614
R

71058 U.S. PTO

08/912243



08/15/97

PATENT APPLICATION



08912243

APPROVED FOR LICENSE

INITIALS OCT 28 97 37

Date
Entered
or
Counted

CONTENTS

Date
Received
or
Mailed

1.	Application <u>2</u> papers.	
2.	<u>Priority Act</u>	<u>8-15-97</u>
3.	<u>Notice of Allowability</u>	<u>11-24-98 M.L.</u>
4.	<u>Change of Address</u>	<u>6-1-99</u>
5.	<u>CORRECTED COPY OF PTOL-85</u>	<u>09-10-99</u>
6.	<u>Formal Drawings (2 sheets) set 1</u>	<u>12-16-99</u>
7.		
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