SPAD-Based Sensors

Edoardo Charbon, Matt Fishburn, Richard Walker, Robert K. Henderson and Cristiano Niclass

1 Introduction

3D imaging and multi-pixel rangefinding constitute one of the most important and innovative fields of research in image sensor science and engineering in the past years. In rangefinding, one computes the Time-Of-Flight of a ray of light, generated by a mono-chromatic or wide-spectral source, from the source through the reflection of a target object and to a detector. There exist at least two techniques to measure the Time-Of-Flight (TOF): a direct and an indirect technique. In direct techniques (D-TOF), the time difference between a START pulse, synchronized with the light source, and a STOP signal generated by the detector is evaluated. In indirect techniques (I-TOF), a continuous sinusoidal light wave is emitted and the phase difference between outgoing and incoming signals is measured. From the phase difference, the time difference is derived using well-known formulae.

Single-photon avalanche diodes (SPADs) or Geiger-mode avalanche photodiodes (GAPDs) are detectors capable of capturing individual photons with very high time-of-arrival resolution, of the order of a few tens of picoseconds. They

E. Charbon (✉) · M. Fishburn
TU Delft, Mekelweg 4 2628CD Delft, The Netherlands
e-mail: e.charbon@tudelft.nl

M. Fishburn
e-mail: m.w.fishburn@tudelft.nl

R. Walker · R. K. Henderson
The University of Edinburgh, Faraday Bldg., King's Buildings
EH9 3JL Edinburgh, Scotland, U.K
e-mail: richard.walker@ed.ac.uk

R. K. Henderson
e-mail: robert.henderson@ed.ac.uk

C. Niclass
EPFL, 1015 Lausanne, Switzerland
e-mail: cristiano.niclass@epfl.ch

F. Remondino and D. Stoppa (eds.), *TOF Range-Imaging Cameras*,
DOI: 10.1007/978-3-642-27523-4_2, © Springer-Verlag Berlin Heidelberg 2013

Ouster Exhibit 2013
IPR2023-01456 - Page 001

may be fabricated in dedicated silicon processes or in standard CMOS technologies. Most SPADs generally operate at room temperature, but they may also be cooled for better noise performance. Even though solid-state SPADs implemented in III–V materials exist, and the literature on the subject is extensive, in this chapter, we limit our attention to silicon devices.

Cova and McIntyre started advocating the use of SPADs for fast timing applications in the 1980s [1, 2]. Thanks to their picosecond timing resolution, SPADs are a natural candidate for D-TOF techniques. If one wants a distance resolution of, say, 1 mm, one needs to discriminate light pulses with a resolution of 6.6 ps (a round-trip Time-Of-Flight is assumed). However, such a time uncertainty is not achievable with a room temperature SPAD implemented in any silicon technology. Thus, averaging and multi-measurement techniques must be employed. A common choice is the use of time-correlated single-photon counting (TCSPC). The technique assumes that a START or synchronization signal is always present at the beginning of each measurement cycle, while the STOP signal is provided by the detector, in our case a SPAD, at a much smaller frequency, typically 10^4–10^6 smaller than that of the synchronization. If this condition is satisfied—and it is often required to minimize pile-up effects—several thousands of time-of-arrival evaluations are needed for each frame to achieve an accurate Time-Of-Flight measurement. A reverse START-STOP arrangement is also possible, depending upon the architecture of the imager, whereas a higher jitter of the measurement system might incur if high intra-optical-pulses jitter is present in the light source.

SPADs may also be used in I-TOF mode of operation. In this chapter two complementary techniques are presented. The common principle is that of quickly switching the SPAD to divert its output signal appropriately, depending on the time-of-arrival. Indirect detection techniques may also be handled in a completely digital environment, thus simplifying the electronics and control signals and enabling large arrays of pixels to be implemented in standard CMOS technologies.

The chapter is organized as follows. After an introduction to the physical mechanisms underlying SPADs, an overview of SPAD fabrication techniques is given, followed by a detailed description of direct and indirect techniques for Time-Of-Flight measurement; the description is complemented by examples of SPAD array implementations in CMOS and relative characterization. An outlook concludes the chapter.

2 The Physics of SPADs

An avalanche photodiode (APD) is a p-n junction that relies on impact ionization effects to multiply photon-generated electrons and holes. APDs output a pulse of electric current synchronous, with some time uncertainty, to the arrival of a single photon. In APD-based, Time-Of-Flight detectors and image sensors, external circuitry senses and analyzes this current pulse to find the photon's time-of-arrival, thus inferring the range; this process, known as rangefinding, enables the reconstruction

Ouster Exhibit 2013
IPR2023-01456 - Page 002

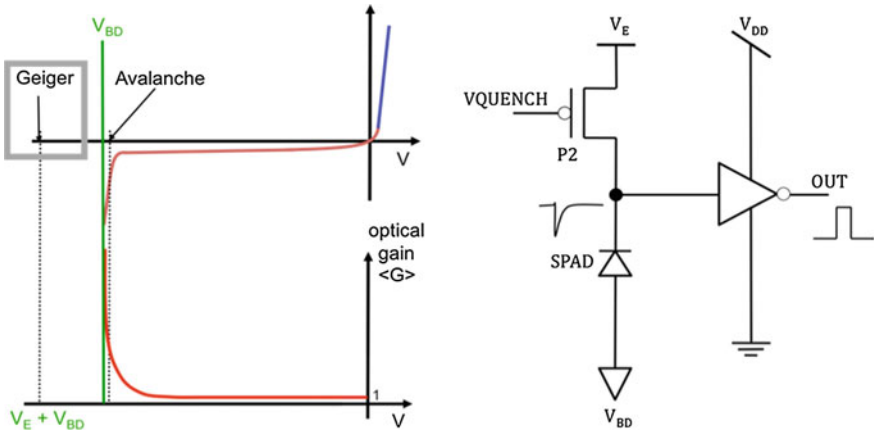

Fig. 1 Steady-state I–V characteristics for a p-n junction with Geiger and avalanche mode of operation (*left*). Passively quenched SPAD (*right*). V_E is known as the excess bias voltage at which a diode must be biased in Geiger mode; it represents the voltage in excess of or above the breakdown voltage V_{BD}. A comparator or inverter is used to shape the output pulse of the detector

of 3D scenes non-destructively. This section gives an overview of the fundamental mechanisms governing the avalanche pulse, focusing on the factors that contribute to the time uncertainty and ultimately the distance estimation accuracy.

Generally, when electrical engineers think of the I–V characteristics of a p-n junction, they think of the steady state curve, shown in Fig. 1. However, there is a pseudo-steady-state in the breakdown operating condition—a voltage above[1] the breakdown voltage can be applied so long as no carriers exist in the diode's depletion region. As soon as a carrier is injected into the depletion region, impact ionization may cause an avalanche to occur, and the diode will shift operating points to the steady-state curve. Impact ionization's underlying statistical process, which is dependent on the electric field, material, and ambient conditions, governs the probability that an avalanche will occur. If the electric field magnitude is high enough, then both electrons and holes are expected to cause significant ionization, the avalanche will become self-sustaining, and the avalanche photodiode is operating in Geiger mode.[2]

If the field magnitude is only sufficient for electrons to cause significant ionization but not holes, the APD is in linear mode. Quantitatively a diode is in Geiger mode when it meets the condition

$$1 \leq \int_0^W \alpha \cdot \exp\left(\int_x^W (\beta - \alpha)\mathrm{d}x'\right) \mathrm{d}x, \tag{1}$$

[1] The preposition "above" is used because researchers working with APDs consider the cathode to be the terminal with the higher voltage.

[2] Termed after the similarity to a Geiger counter.

with α and β representing the impact ionization rates (per m) of electrons and holes, respectively, and W is the depletion width. The bias at which Eq. (1) is an equality is called the breakdown voltage, V_{BD}. The bias applied to the diode, V_{OP}, exceeds breakdown by a voltage known as excess bias voltage, V_E. Henceforth the discussion will be restricted to SPAD technologies [3].

A SPAD is able to detect more than a single carrier by the inclusion of external circuitry, which quenches an avalanche by: sensing an avalanche; lowering the voltage applied to the SPAD; and after some time, raising the applied voltage above the breakdown voltage. The simplest such circuit is a resistor placed in series with the diode, also known as ballast resistor. The circuit works as follows. First, when there are no free carriers in the junction, the applied voltage on the diode is V_{OP}. When light injects a carrier into the junction, impact ionization may or may not cause the rapid build-up of free carriers in a small part of the diode. If significant ionization does not occur and all free carriers are swept out of the depletion region, the incident photon is not detected. If ionization does occur, it will continue until the space-charge phenomena limits the local carrier concentration. The avalanche will spread to other regions of the diode via a multiplication-assisted diffusion process. The decrease in voltage across the diode, dependent on both any parasitic capacitances and the quenching resistor, will eventually reach the excess bias. At this point the diode is quenched—no further current should flow from impact ionization and there are no free carriers in the diode itself. The voltage will then be recharged by the flow of electric current through the quenching resistor into the parasitic capacitances, with the diode being ready to detect another carrier after this dead time [4].

The probability that a single photon's generated carriers are detected is called the photon detection probability (PDP). A number of factors influence the PDP, including electric field conditions, doping levels, whether electrons or holes primarily initiate avalanches, and the applied voltage. Photons are not the only source of initial carriers; uncorrelated or correlated noise can also cause free carrier injection and undesirable avalanches. Uncorrelated noise sources include: ambient light; tunneling from an electric field that is too high; and fabrication defects which ease valence-to-conduction band transitions, such as thermally generated or tunneling carriers. The last factor, fabrication defects, can also cause afterpulsing, a type of time-correlated noise. Traps in the forbidden energy band can fill, only to release free carriers on the time scale of tens of nanoseconds following an avalanche. Afterpulsing prevents an instant recharge phase in SPADs, and places constraints on the minimum dead time.

There are other sources of correlated noise besides afterpulsing—optical and electrical crosstalk are the most common, but in practice afterpulsing is the dominant type of correlated noise. Whether the initial carrier is photon-generated or not, several factors cause time uncertainty between the injection time and the sense time. The most important timing factor is whether the carrier is generated in the depletion region itself, or if it must diffuse into the depletion region. Carriers that successfully diffuse into the depletion region do so following an exponential

Ouster Exhibit 2013
IPR2023-01456 - Page 004

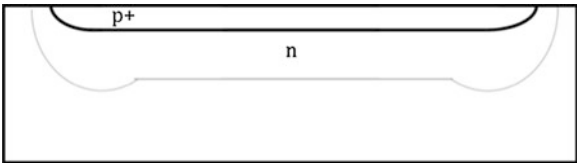

Fig. 2 Cross-sections of a generic pn junction in a planar process with the depletion region (*gray line*) forming in the structure upon reverse-biasing, assuming a large doping differential between the p and n regions

time distribution [5]. Once the initial carrier is in the depletion region, the statistics of impact ionization will create a time uncertainty that is roughly a normal distribution. The overall timing response of a SPAD to a pulsed laser can be described as a background noise plus a normal distribution convolved with the addition of an impulse function (describing carriers generated in the depletion region) with an exponential distribution.

3 CMOS SPAD Design

Building SPADs in CMOS substrates requires knowledge of the process and layers available to the designer to implement junctions that can be reverse-biased at high voltages. Figure 2 shows a generic pn junction implemented in a planar process. The figure shows the depletion region, as it forms upon reverse biasing the junction (assuming a large doping differential between the p and n regions).

Implementing a pn junction in a planar process first involves finding a way to prevent premature edge breakdown (PEB). Several techniques exist to implement PEB prevention. In essence, the techniques have in common the reduction of the electric field or the increase of the breakdown voltage at the edges of the junction, so as to maximize the probability that the avalanche is initiated in the center of the multiplication region, i.e. the region where the critical electric field for impact ionization is reached and, possibly, exceeded.

Figure 3 illustrates four of the most used structures. In (a) the n+ layer maximizes the electric field in the middle of the diode. In (b) the lightly doped p-implant reduces the electric field at the edge of the p+ implant. In (c) a floating p implant locally increases the breakdown voltage. A polysilicon gate is usually drawn to prevent the creation of a shallow trench, however, it can also be used to further extend the depletion region.

Shallow trench isolation (STI) can also be used to delimit the junction, provided that it is surrounded by a multi-layer of doped silicon so as to force recombination of those charges generated in the defect-rich STI as shown in structure (d) [6]. These structures are usually shaped as a ring around the junction; they are known as *guard rings*. Guard rings can also be defined *implicitly* by proper definition of drawn layers [7].

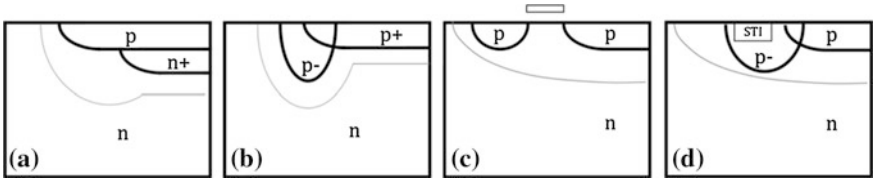

Fig. 3 Cross-sections of doping profiles that may be used to prevent premature edge breakdown in planar processes

There exist a variety of avalanche quenching techniques, partitioned in active and passive methods. The literature on these variants is extensive [8]. In active methods, the avalanche is detected and stopped by acting on the bias. In passive methods the pn junction bias is self-adjusted e.g. by a ballast resistor. Recharge methods can also be active and passive. In active methods, the bias across the diode is re-established by a switch activated by an avalanche detector. In passive methods the recharge occurs through the ballast.

Upon photon detection, the device generates a current pulse that is converted to a digital voltage level by means of a pulse shaping circuitry, also shown in the figure. The pulse shaper is also acting as an impedance adapter to drive the load of the column readout often employed in a SPAD matrix.

The main parameters characterizing individual SPADs are sensitivity, measured as **photon detection probability** (PDP), noise, measured as the rate of spurious pulses due to thermal events or **dark count rate** (DCR). Other parameters include **timing jitter**, also known somewhat inappropriately as **timing resolution**, **afterpulsing probability** and the aforementioned **dead time**. These parameters have been used in the literature for a variety of CMOS processes [9–17].

When implemented in an array, other performance measures become relevant to the quality of the imager. Dead time uniformity relates to the variability in dead time, which determines the dynamic range of each detector. Timing jitter uniformity and PDP uniformity, as well as DCR uniformity and crosstalk have to be accounted for and properly characterized [9]. PDP of course will also be a function of the input wavelength. In CMOS SPAD implementations, the sensitivity range is mostly in the visible spectrum, with a somewhat reduced near infrared and near ultraviolet PDP.

Crosstalk is also a chip-level effect similar to PDP and DCR non-uniformities; it relates to the interaction between an aggressor pixel and a victim pixel, where the aggressor may cause a spurious avalanche in a victim. The effect can be electrical and/or optical. Electrical crosstalk is due to electrical interference through substrate or supply noise. Optical crosstalk may occur when an avalanche is triggered in the aggressor; by impact ionization, several photons may be emitted, thus causing the victim to detect them. While electrical crosstalk is strongly dependent on the design of supply lines and of substrate noise rejection measures, optical crosstalk may only be influenced by the number of carriers involved in an avalanche and by pixel pitch.

Ouster Exhibit 2013
IPR2023-01456 - Page 006

4 TCSPC Based TOF Camera Systems

Using TCSPC for optical rangefinding in D-TOF mode has been proposed several decades ago, since the introduction of the LIDAR concepts. SPAD based single-pixel detectors, in combination with scanning, powerful pulsed light sources. One of the first examples of this combination was proposed in [18, 19]. In this work, the light source is synchronized to the SPAD to produce an accurate evaluation of the Time-Of-Flight of the reflected photons and thereby of the distance to the target.

In [20] this concept was made scannerless thanks to the use of monolithic arrays of SPADs implemented in CMOS technology. The concept, described in Fig. 4, is enabled by the use of a cone of light reaching approximately simultaneously the target source.

The photons reflected by the surface are imaged through a lens system to the array. With the use of an accurate chronometer or stop watch, it is possible to derive the distance of the reflecting point using the following relation

$$d \cong \frac{c}{2} \cdot \tau_{TOF}, \tag{2}$$

where τ_{TOF} is the Time-Of-Flight or the time difference between the light pulse synchronization signal and the time-of-arrival in the detector, and c is the speed of light in vacuum. Since SPADs are dynamic devices, they generate a digital pulse upon detection of a photon, and thus, unlike conventional diodes, they cannot hold a charge proportional to the overall photon count. Thus, the Time-Of-Flight must be computed in situ (either on pixel, on column, or on chip) or outside the image sensor. The same holds with integrated time-of-arrival evaluation: it can only be (1) in-pixel, (2) in-column, or (3) on-chip. To address this limitation, researchers have adopted a number of architectures that take advantage of the low propagation delay or high level of miniaturization achievable in standard submicron and deep-submicron CMOS technologies.

The simplest readout architecture implementing photon counting on-chip in combination with random-access single-photon detection, was demonstrated for the first time in a matrix of 32 × 32 pixels, each with an independent SPAD, a

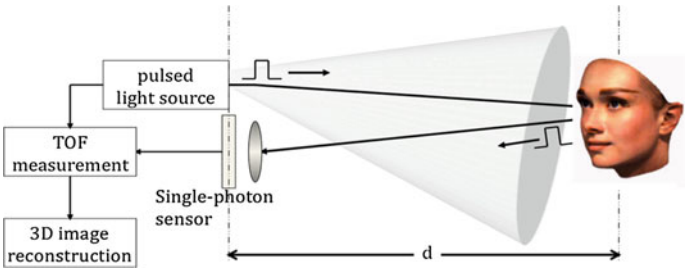

Fig. 4 Time-correlated single-photon counting (TCSPC) for optical rangefinding and 3D imaging

quenching mechanism, a pulse shaping and column access circuitry [20]. In this readout scheme, all time-sensitive operations had to be performed sequentially. This design has the main drawback in that it can only "see" one pixel at any point in time, while all the other pixels are operating but their output is lost. The micrograph of the chip is shown in Fig. 5; the chip was implemented in a 0.8 μm high-voltage CMOS process.

Addressing the readout bottleneck required some degree of sharing. The column is the obvious place to start from, since it is a repetitive structure that touches all pixel rows. The first known such approach involved interpreting the column as a bus. The bus is used as transfer time and address over the same hardware. The time is coded in partially processed pulses generated in the pixel of which the time-of-arrival is evaluated. The address is coded as a unique combination over the lines present in the bus sent to the bottom of the column where the time-of-arrival is evaluated, either off or on chip [11].

The second approach, known as latchless pipelined readout, has a passive type of coding, whereas time-of-arrival also contain the information of the row position where the pulse was generated. Every photon triggers a pulse that is injected onto the pipeline at a precise location that corresponds to the physical place where the pixel is located. Since the propagation time is across the column is too short to enable any time-based discrimination, a timing-preserving delay line is added to the column. At the bottom of the column time discrimination is performed by a column-based TDC that also returns the row code [21]. The photomicrograph

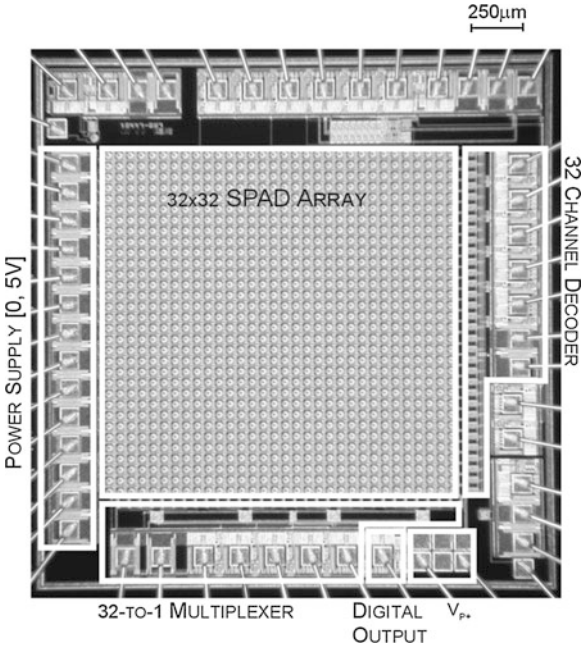

Fig. 5 The first large SPAD array with random access readout. The chip was implemented in 0.8 μm CMOS technology

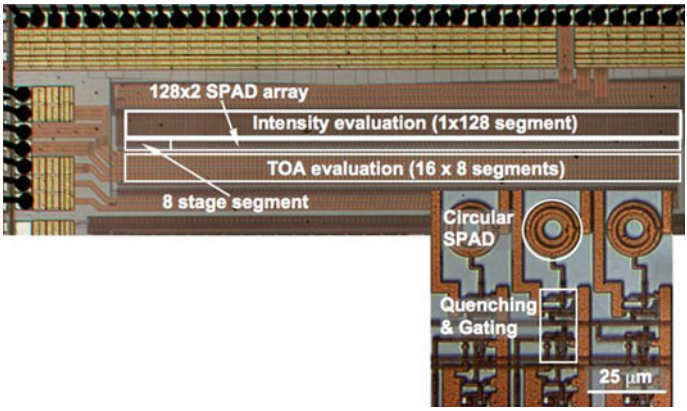

Fig. 6 CMOS version of a latchless pipeline based readout fabricated in 0.35 µm CMOS technology [21]

shown in Fig. 6 illustrates the actual implementation of the concept for a latchless pipelined 128 × 2 SPAD array fabricated in 0.35 µm CMOS.

An important step towards full parallelism was achieved with LASP [10], a 128 × 128 SPAD array, where a bank of 32 column-parallel time-to-digital converters (TDCs) was used to simultaneously process 128 in-line SPADs using an event-driven 4-to-1 column-multiplexer (one per column). Figure 7 shows the block diagram of LASP. Each TDC in the 32-array can generate 10 MS/s with a time resolution of 97 ps. The resolution can be further increased to 70 ps by acting on the clock frequency. Each TDC in LASP is a 3-tier partial TDC based on three different architectures: a clocked counter (2 MSBs, 25 ns resolution), a phase

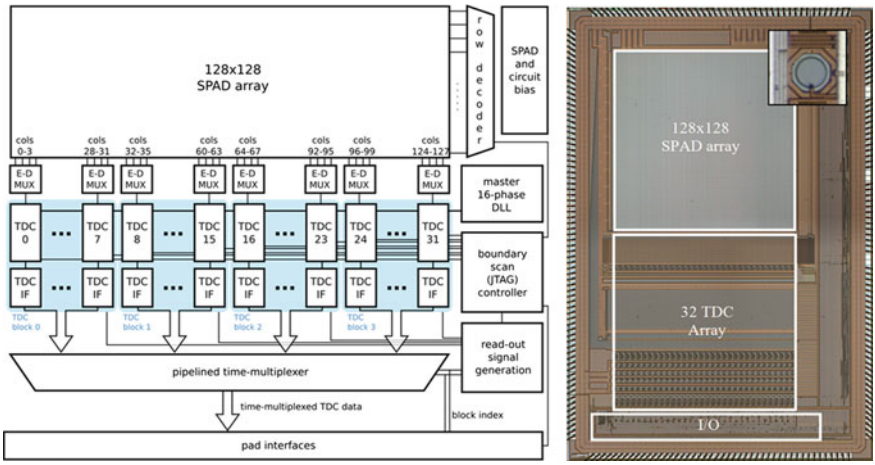

Fig. 7 Schematic and micrograph of LASP; an array of 32 TDCs processes the pulses generated by 128 SPADs at any time by means of a 4-to-1 event-driven multiplexer (one for each TDC)

interpolator controlled by a temperature-compensated DLL (4 intermediate bits, 1.56 ns resolution), and a 16-taps Vernier line (4 LSBs, 97.6 ps resolution). The total time resolution of 10bits is routed outside the chip through a high-speed digital network operating at 3.2 Gb/s. The differential non-linearity (DNL) and integral non-linearity (INL) were recently improved to ±0.1LSB and ±0.25LSB, respectively [22].

The chip was tested in TCSPC mode to compute a scene's depth via a pixel-by-pixel Time-Of-Flight evaluation of a defocused beam hitting the target. The results of the experiment are shown in the histogram of Fig. 8. The jitter is dominated by the SPAD timing uncertainty, whereas the characteristic tail of the device also appears from the picture.

The distance evaluation result is shown in Fig. 9 as a function of the real distance measured using a precision device from 40 cm to 3.75 m. Each distance measurement was derived from the centroid of the corresponding histogram, whereas the uncertainty as a function of distance is plotted in also plotted in the figure.

In Fig. 10 the resulting 3D image of a mannequin illuminated by a cone of pulsed laser light with a wavelength of 637 nm is shown after a 1 s exposure. The 3D points represent the centroid of the histograms of each pixel.

The integration of time-resolving electronics on a per-column or per-chip basis represents a trade-off between fill-factor, processing bandwidth and circuit area. Unlike integrating image sensors based on photodiodes, photons falling on SPAD pixels which are not multiplexed to available time-resolving channels are lost. In an efficient SPAD sensor operating in D-TOF mode, a time-stamp must be generated for every impinging photon at every pixel detector. This necessitates the combination of per-pixel time-digitization circuitry and high speed array readout.

The integration of a large array of in-pixel TDCs or time-to-amplitude converters (TACs) poses several challenges with respect to single channel architectures found in the literature [23–26]:

1. Circuit area is limited to a few 100 μm^2 to achieve practical pixel fill-factor and pitch.
2. Power consumption cannot exceed a few 100 μA per pixel, in order to allow array size to be scaled to 10's of kilopixels without excessive heating.

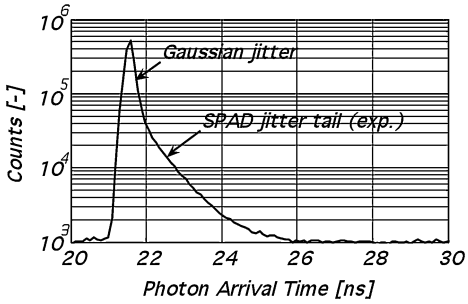

Fig. 8 TCSPC experiment. The laser pulse is pointed toward a SPAD in the array and the time-of-arrival of the first detected photon is evaluated by the corresponding TDC. The resulting histogram, shown in the plot in logarithmic scale, is then computed [10]

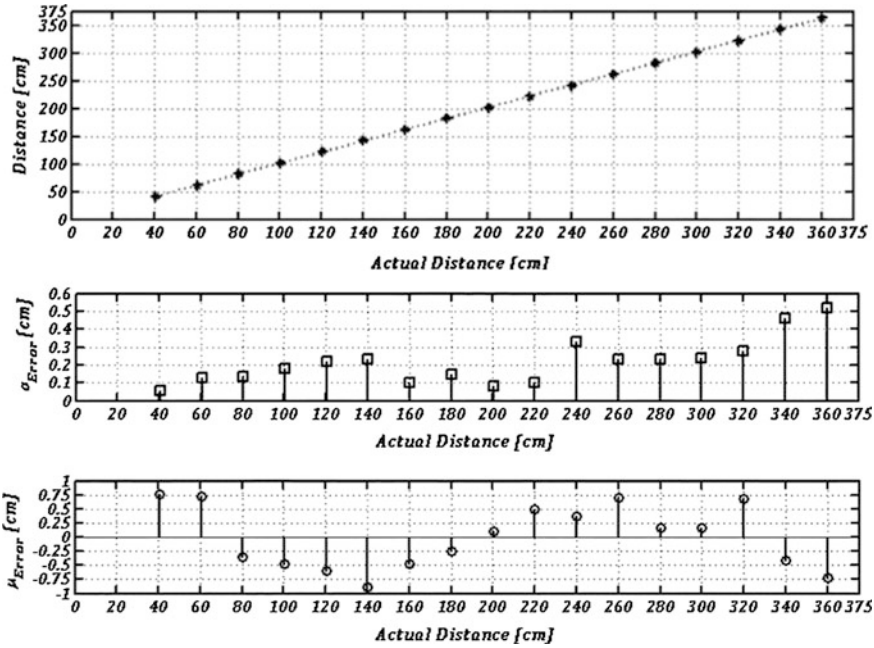

Fig. 9 Actual distance versus estimated distance computed in LASP at room temperature (*top*); average error versus distance (*middle*); standard deviation versus distance (*bottom*) [10]

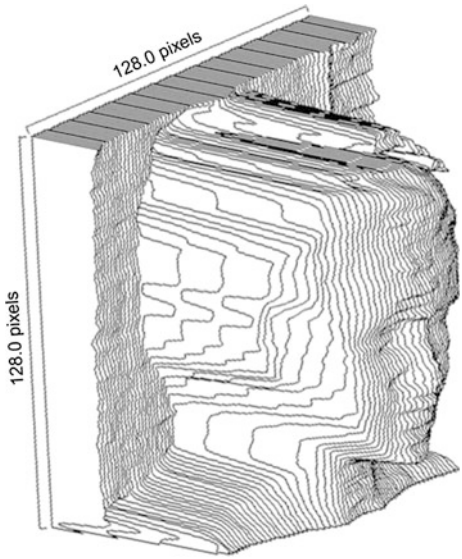

Fig. 10 Target image computed by LASP in 1 s exposure at room temperature [10]

3. Uniformity requires around 1 percent matching of time resolution for acceptable image quality without requiring a frame store for pixel calibration.
4. Throughput must assure conversion of photon arrivals within typical pulsed illumination period of 100's of nanoseconds to avoid statistical distortions leading to non-linearity.
5. Time resolution is required to be a few 10's picoseconds in a full-scale range of around 25–50 ns resolution for indoor applications where human body features are to be distinguished at a maximum distance of a few meters.

These stringent specifications discount many of the conventional TDC architectures which achieve sub gate-delay resolution. Two scalable in-pixel TDC approaches were proposed in [27] and [28], differing by the adoption of an internal clock (IC-TDC) or an external clock (EC-TDC) as a source of timing accuracy (Fig. 11). Both converters operate in reverse START-STOP mode whereby they are started by a photon detected by the SPAD front-end circuit and stopped by a global clock synchronous with the pulsed optical source.

The IC-TDC integrates a gigahertz gated ring oscillator within each pixel, which clocks an n-bit ripple counter providing coarse photon arrival time estimates. Fine time estimates are obtained by decoding the frozen internal state of the ring providing the 3 least significant bits, which represent single inverter delays. A four-stage differential ring oscillator is chosen with a binary number of internal

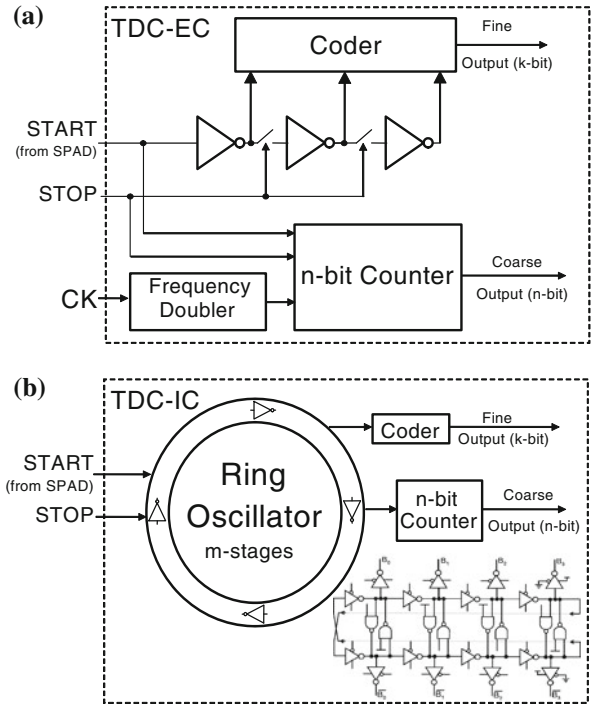

Fig. 11 Time-to-digital conversion pixels: **a** external clock **b** internal clock

states for simplicity of decoding logic. Two implementations have been studied, a chain of tri-stateable inverters provide static internal state memory [29] while the second, a chain of inverters connected by pass-gates provide a dynamic internal state memory [27]. Care must be taken to avoid metastability when gating the ring oscillator clock to the ripple counter, by employing hysteresis in the clock input stage. Tuning of the ring oscillator loop delay is achieved by current starving the differential inverters through a NMOS regulating transistor. This is also effective in diminishing the effect of supply noise induced jitter. IC-TDCs have the advantage of consuming power only when activated by an impinging photon, thus the power consumption of a large array is directly proportional to photon flux. This in turn has the potential disadvantage of introducing a light-flux-dependency of the TDC resolution, due to variable IR drops.

The EC-TDC achieves coarse time measurement in the similar manner to the IC-TDC, by means of an n-bit counter, clocked by an *external* high frequency clock distributed to the entire pixel array. Fine resolution is determined by the propagation delay of the SPAD pulse through an inverter chain. The state of inverter chain is frozen by the subsequent rising edge of the clock that is synchronized with the STOP signal and decode logic converts the thermometer code into a k-bit binary number. The STOP signal also halts the coarse counter. Time resolution calibration is performed by current-starving the inverter chain, through a feedback loop [28]. EC-TDCs consume an almost constant power level irrespective of input illumination but provide good global time resolution accuracy and negligible resolution dependency on photon flux.

Scaling of the per-pixel TDC approach from early prototypes of 32 × 32 to 160 × 128 pixels has been demonstrated with good performance. Characterization of a large IC-TDC image array has shown good DNL, INL, and pixel-to-pixel uniformity [29].

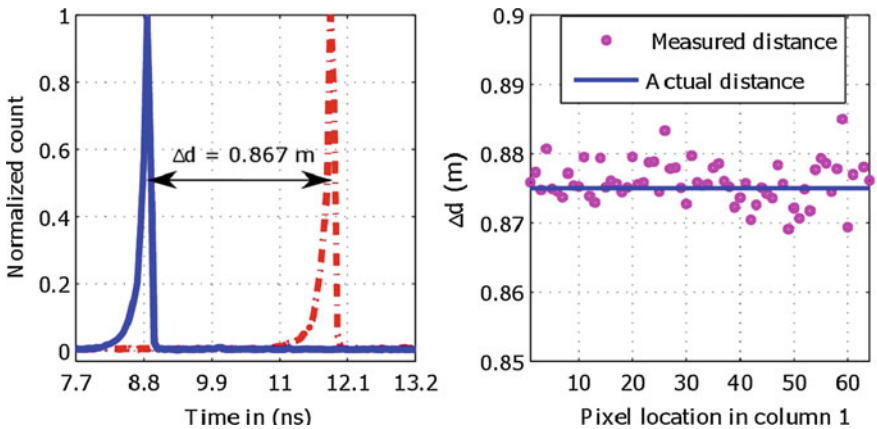

Fig. 12 Time of flight measurements with IC-TDC array

In Fig. 12, a TOF experiment is conducted for a single column of pixels, using a pulsed laser at a constant distance from the sensor. Future implementations of these architectures in advanced nanoscale CMOS technologies bring the prospect of considerable gains in fill factor, time resolution, power consumption, and pixel pitch.

Figure 13 shows an analog approach to per-pixel time estimation, employing an in-pixel TAC and ADC converter [30]. A current source (IbiasP) charges a capacitor Cs when the switch-structure, composed of Mp1, Mp2, Mp3, and IbiasN, is enabled. Three layout-matched replicas of the ramp-generator building block are employed: Stage1 and Stage2 are used alternately to measure the number of events or the event arrival time in a time interleaved way as Vo1 (or Vo2); StageREF is used to generate a reference voltage ramp Vo_{REF} for the embedded single-slope ADC. Analog time encoding is started on detection of a photon, by the charging of capacitor Cs, and stopped by the subsequent STOP clock rising edge. At the end of this interval, a voltage has accumulated on capacitor Cs that is proportional to the photon arrival time.

After an exposure time, the pixel array is switched over to analogue to digital conversion mode. The clock signal CNT and an n-bit Gray code count sequence operate synchronously and are globally distributed to the pixel array. The Stage-REF block generates a stepped analog ramp voltage Vo_{REF}, which is compared to

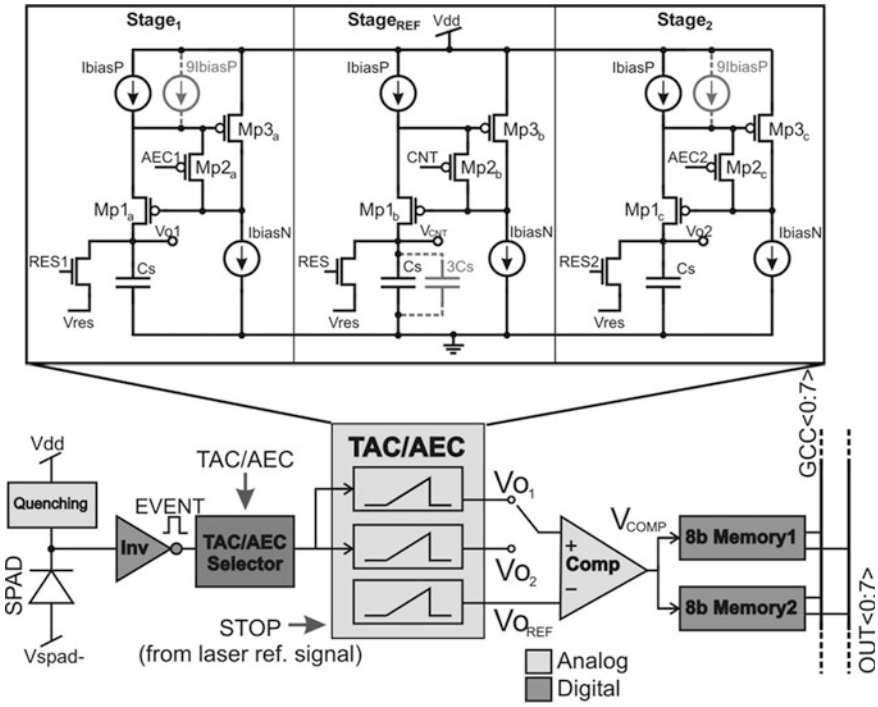

Fig. 13 Time-to-amplitude converter pixel architecture

Table 1 Performance comparison of per-pixel TAC/TDC arrays

Parameter	TAC [30]	TDC-EC [28]	TDC-IC [27]	Unit
Technology node	130	130	130	nm
Pixel pitch	50	50	50	μm
Bit resolution	6	10	10	bits
Time resolution (LSB)	160	119	178/52	ps
Uniformity	±2	±2	8	LSB
INL	1.9	±1.2	±0.4/1.4	LSB
DNL	0.7	±0.4	±0.5/2.4	LSB
Time jitter	<600	185	107/32	ps @ FWHM
Power consumption	300	94	28/38	μW @ 500kframe/sec

Vo1 (or Vo2) by an in-pixel comparator. When Vo_{REF} exceeds Vo1 (or Vo2) the voltage comparator toggles, sampling the Gray code into the memory. Hence the stored value of the Gray code is directly proportional to the analog voltage determined previously by the time-to-analog conversion process. Two memories are employed to allow one to participate in conversion while the other is being read-out. While the performance of the per-pixel TAC array was less favorable than the TDC counterparts (Table 1), this architecture shows greater promise in terms of scaling for area and power without the need for advanced nanoscale CMOS technology.

Highly parallel readout schemes must be employed to handle the extremely high volumes of per-pixel timestamp data generated by both per-pixel TDC and TAC image arrays. Single-photon detectors produce events at each pixel at much greater rates than conventional integrating image sensors, especially those generated by ambient lighting or DCR distribution. Data rates of several Gbps have been attained in recent imagers [29, 31].

Per-pixel time-resolving arrays, which integrated the TAC/TDC in same CMOS substrate as the SPAD detector face, have two practical drawbacks:

1. The bandgap of silicon limits detection to wavelengths below 1125 nm. Common CMOS SPADs have poor PDP (below 5 %) at suitable NIR wavelengths (850 or 930 nm) due to the shallow active junction.
2. The pixel fill factor is low due to the large insensitive area devoted to the time-resolving electronics; around 1–2 % have been demonstrated in the above research.

Hybrid 3D wafer technology offers a solution to this dilemma. Itzler et al. [32] have developed InGaAs/InP avalanche diode structures in the wavelength range of 0.92 to 1.67 μm, which are hybridized to CMOS read-out integrated circuits (ROICs) that enable independent laser radar Time-Of-Flight measurements for each pixel. The 9 % fill-factor of the SPAD array is improved to 75 % by employing a micro lens array and an average photon detection efficiency (PDE[3]) of

[3] PDE is defined as the multiplication of fill facto and PDP.

39 % is obtained. The ROIC consists of an array of 100 μm pitch pixels containing pseudorandom counters in a 0.18 μm CMOS process clocked from an external PLL distributed to all pixels. The power consumption of the array is only 50 mW at 20 kHz frame rate and 320 mW at 200 kHz. Aull et al. reported a similar 64 × 64, 50 μm pitch ROIC in 0.18 μm CMOS for a similar 3D stacked technology with a time resolution of 110 ps [33].

5 Single-Photon Synchronous Detection

The technique known as single-photon synchronous detection (SPSD) is an I-TOF measurement, the SPAD-digital equivalent of lock-in detection [34–38]. In SPSD, proposed for the first time in [39], the scene is illuminated with a sinusoidal or pseudo-sinusoidal light intensity and the phase of the return photons. As in lock-in systems, distance d is computed as

$$d \cong \frac{c\varphi}{2 \cdot 2\pi f_0}, \tag{3}$$

where c is the speed of light in vacuum, f_0 is the modulation frequency, and φ is the measured phase difference between outgoing signal and measured signal. In SPSD, unlike in lock-in systems, the phase φ is computed directly by counting photons in a structured way.

In SPSD the period of the illumination is discretized in N_C uniform time segments ΔT_0, ΔT_1,…, ΔT_k,…, $\Delta T_{N_{C-1}}$. At the end of the integration period, every counter stores a value C_k, corresponding to the counted photons in the time period ΔT_k during the integration period. For each segment the SPAD's output is directed to a counter that is activated only during that segment, the photon counter results C_k. shows how the illumination source is modulated and discretized. The figure also shows how the SPAD's output is distributed to the various counters to

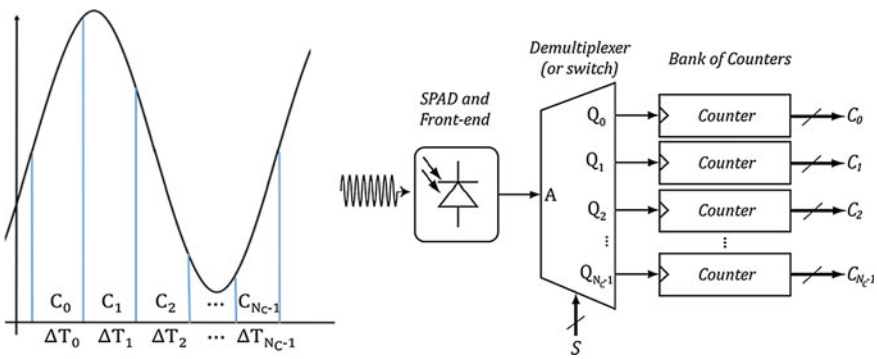

Fig. 14 Possible discretization of a period of illumination, with resulting partial counts (*left*); block diagram of the pixel in an SPSD camera as described in [39] (*right*)

generate C_0 through $C_{N_{C-1}}$ in a possible block diagram implementation of the technique on pixel (Fig. 14).

For the case $N_C = 4$, with only four partial counters C_0, C_1, C_2 and C_3, the phase becomes

$$\varphi = \arctan\left(\frac{C_3 - C_1}{C_0 - C_2}\right). \tag{4}$$

As a byproduct of this computation we also achieve an estimate of the offset and amplitude of the illumination intensity, as

$$A' = \frac{(C_3 - C_1)^2 + (C_0 - C_2)^2}{2}; \quad B' = \frac{C_0 + C_1 + C_2 + C_3}{4}. \tag{5}$$

The parameters A′ and B′ are illustrated in Fig. 15 which shows a sequence of photon detection where the partial counts are progressively building up the waveform corresponding to a single period by superimposing adjacent measurements, thus enabling the computation of phase, offset, and amplitude.

A SPSD image sensor based on the concept outlined in Fig. 15 was implemented in an array of 60 × 48 pixels operating in real-time with an integration period as low as 10 ms and a frame rate as high as 100fps. A block diagram and a photomicrograph of the image sensor is shown in Fig. 16, whereas the pixel in this design comprises two 8-bit counters to compute alternatively C_0/C_2 and C_1/C_3.

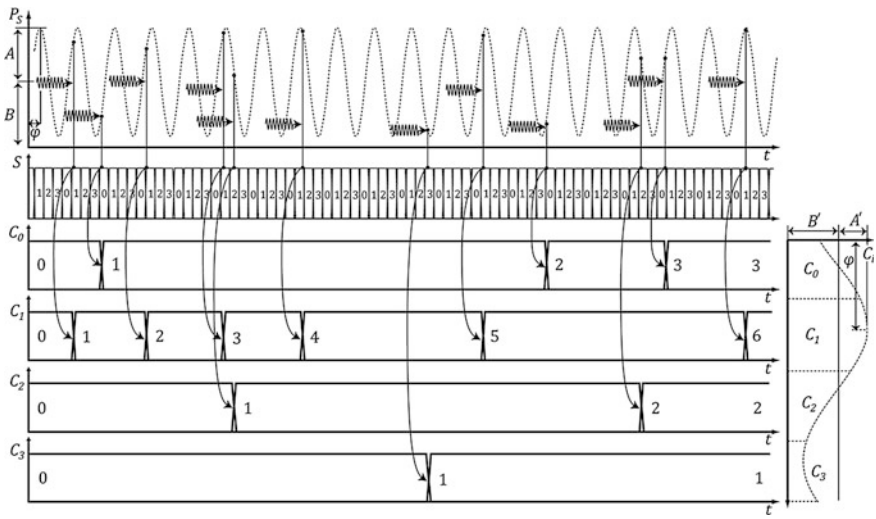

Fig. 15 Principle of operation of SPSD cameras. Impinging photons are detected and "assigned" to the appropriate bin depending upon the time-of-arrival with respect to the outgoing optical signal

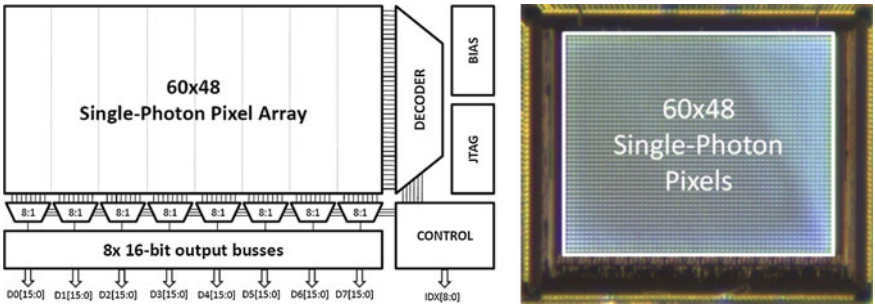

Fig. 16 Block diagram (*left*) and photomicrograph of the SPSD image sensor (*right*) proposed in [39] for the first time and fabricated in 0.35 μm CMOS technology

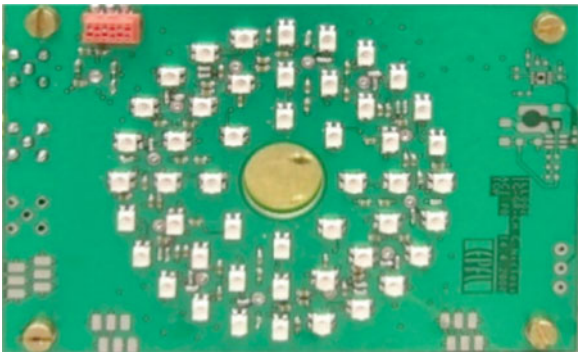

Fig. 17 Illuminator used in combination with the integrated SPSD image sensor. The total optical power emitted by the illuminator is 800 mW. The frequency of operation is 30 MHz, with a 3rd harmonic component suppressed at 37 dB

The pixel has a pitch of 85 μm and a fill factor of 1%, which can be compensated to a partial extent by the use of a microlens array [40].

The chip was used in several experiments to test its robustness to ambient light and interferences. The illuminator used was an array of 48 850 nm LEDs (Osram GmBH, Germany) located in three concentric circles as shown in Fig. 17.

The plots shown in Fig. 18 show the estimated distance versus the actual distance measured in a similar distance range as in the TCSPC experiments. The figure also shows mean errors and standard deviations as a function of the distance.

The same mannequin used in LASP was also used in the SPSD experiments. The results confirmed the estimated error. Figures 19 and 20 show a target at two exposure times, evidencing the relation between exposure, or number of the counting iterations, and overall distance error at the pixel level.

The images show the expected dependency of accuracy from exposure time. This behavior can be quantitatively analyzed looking at the demodulation contrast. Let us consider the statistical error of the distance measurement,

$$\sigma_{Error} = \frac{c}{2 \cdot 2\pi f_0} \sigma_\varphi, \tag{6}$$

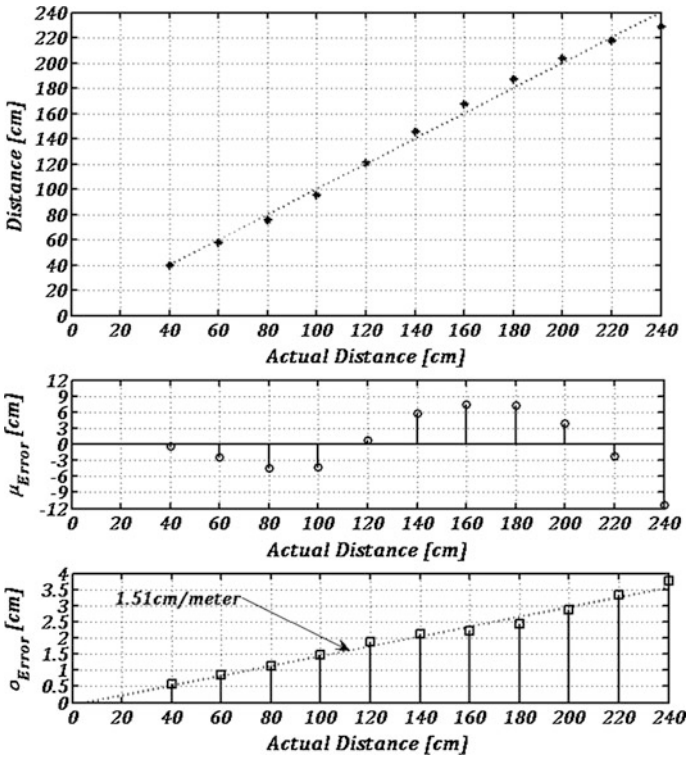

Fig. 18 Estimated versus actual distance using a SPSD pixel (*top*). Mean error versus distance (*middle*) and standard deviation of the error versus distance (*bottom*). All the data are reported at room temperature [39]

where σ_φ is the standard deviation of the phase measured using SPSD. Assuming $N_C = 4$, Eq. (6) can be rewritten in terms of the illumination parameters, as

$$\sigma_{Error} = \frac{R_D}{\sqrt{8}\pi}\frac{\sqrt{B'}}{A'}, \text{with } R_D = \frac{c}{2f_0}. \tag{7}$$

Rearranging the terms and substituting, we obtain the following equality

$$\sigma_{Error} \cong \frac{R_D}{\sqrt{8}\pi c_D}\frac{1}{\sqrt{T \cdot SBR \cdot S_R}}, \tag{8}$$

where T is the integration period, SBR is the signal-to-background ratio, and S_R is the signal count rate (the sum of all counters) on the image sensor. The term c_D is known as demodulation contrast, defined as

$$c_D = sinc\left(\pi\frac{\Delta T}{T_0}\right), \tag{9}$$

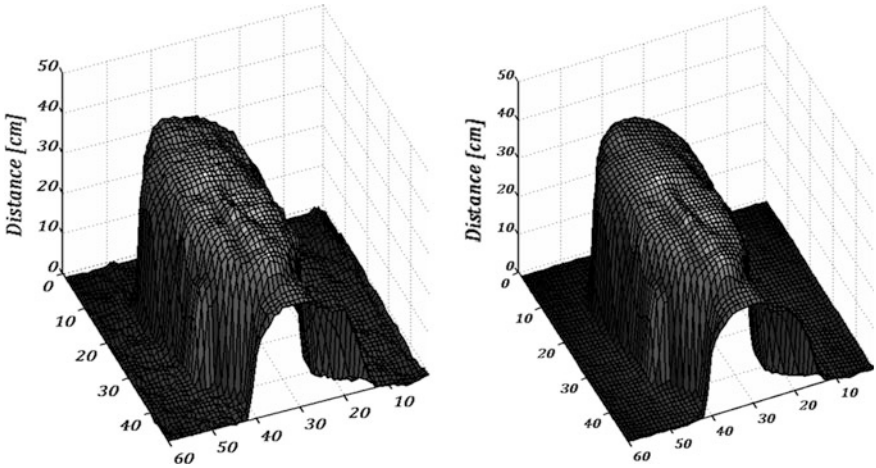

Fig. 19 3D image of mannequin in real-time exposure (30fps) at room temperature [39] at a different integration times

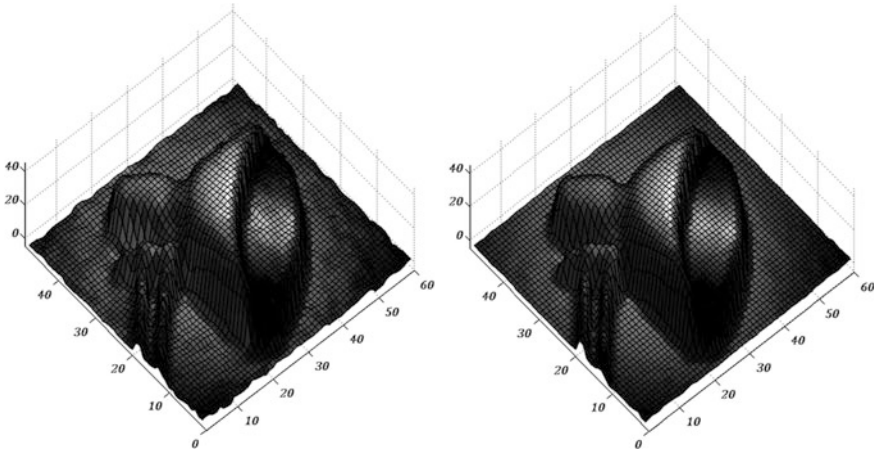

Fig. 20 Target image computed by SPSD in real-time exposure (30fps) at a shorter (50 ms) and longer (500 ms) integration times

where ΔT is the mean time segment duration, in this case ¼ of the total modulation period $T_0 = 1/f_0$. In this configuration, the demodulation contrast is 0.9, whereas 1.0 is the maximum achievable value. By increasing the number of samples to, say 8, the demodulation contrast would only increase to 0.974, but at a cost extra hardware and thus fill factor. Also note that the actual demodulation contrast decreases with modulation frequency. However, in SPSD it reduces very slowly while in lock-in systems it quickly degrades due to the limits in transit time in the pixels. The plot of Fig. 21 shows the relation between the demodulation contrast

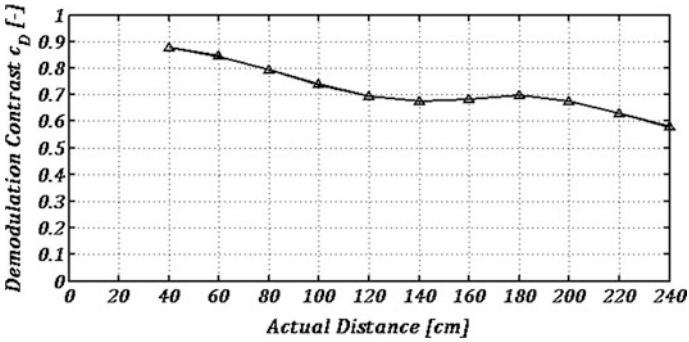

Fig. 21 Measured demodulation contrast as a function of distance in SPSD at room temperature [39]

and the availability of the signal S_R, as the target is further and the Time-Of-Flight increases.

6 Phase-Domain Delta-Sigma TOF Imaging

As has been discussed, phase-demodulating systems typically generate two or more bin values per frame requiring readout and external processing in order to produce a depth map. This IO and processing burden can result in a significant portion of the complete system's power consumption and computational load. Recent trends have seen an increasing level of complexity integrated into the sensor's focal plane to boost acquisition speed and reduce the required external circuitry. For example, while the first TOF 3D imaging systems were based on scanned single point range sensors comprising a discrete APD and external time-stamping circuitry, recent sensors have combined arrays of SPADs with on-chip time-stamping or binning logic, such as the TDC and SPSD systems discussed earlier in this chapter.

A natural extension of this theme of integration is the use of modern CMOS processes to construct sensors with additional focal-plane logic to allow the on-chip creation of depth-maps, reducing the IO and external processing needs of such systems. One such approach is to place a *Phase-Domain* Delta-Sigma (PDΔΣ) loop in the pixel. Figure 22 below compares the architecture of a simple ΔΣ ADC with its phase-domain equivalent. While the ΔΣ ADC measures the magnitude of an input *voltage* with respect to two reference voltages, the phase-domain implementation instead measures the mean *phase* of its input with respect to a pair of reference phases. This approach has been successfully demonstrated in applications including magnetic flux [41] and temperature [42] sensing, where the particular sensing elements used created a phase shift in response to the property to be measured.

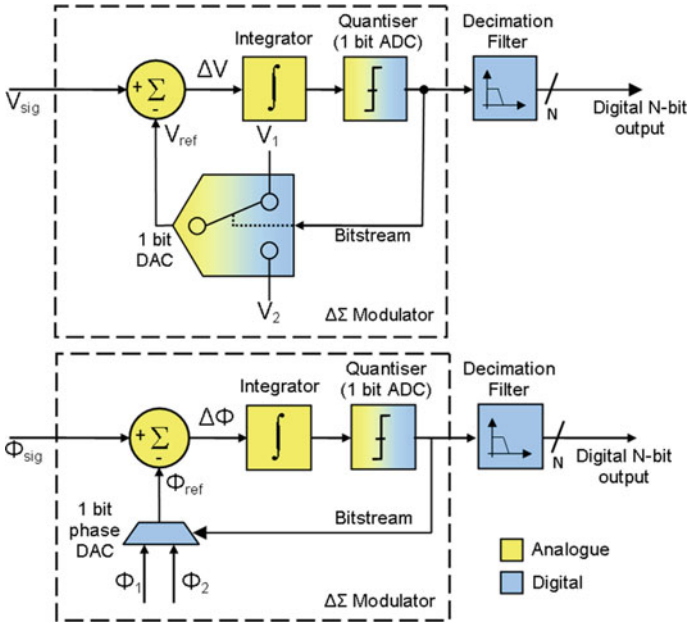

Fig. 22 Comparison of: conventional ΔΣ ADC (*top*), phase-domain ΔΣ converter for 3D imaging (*bottom*)

I-TOF 3D imaging systems also of course depend on the measurement of a phase shift. Crucially, an all-digital PDΔΣ loop may be constructed which locally processes the SPAD pulses created within a pixel and converges to estimate this depth related phase shift directly. This approach was employed in the 128 × 96 pixel sensor reported in [31], as illustrated in the architecture block diagram and die micrograph shown in Figs. 23 and 24 below.

The loop operates in a similar fashion to existing two-bin demodulating approaches [43], dividing the returning pulse energy into two bins: in phase and 180° out of phase with the transmitted modulated light. However, instead of simply integrating the energy in these bins over a period of time and transmitting their contents for external processing, the loop continually seeks to drive its internal integrator towards zero by integrating positively during φ_1 and negatively during φ_2, as the timing diagram contained in Fig. 25 below illustrates. The resulting bitstream density, r, indicates the mean phase of the input pulses, as governed by Eq. 10, where $N_{\varphi 1}$ and $N_{\varphi 2}$ represent the number of photons counted in bins φ_1 and φ_2 respectively.

$$r = \frac{N_{\phi_2}}{N_{\phi_1} + N_{\phi_2}} \tag{10}$$

This calculation is of course influenced by the DC component of the detected light, which must be corrected, for example by subtracting the DC component

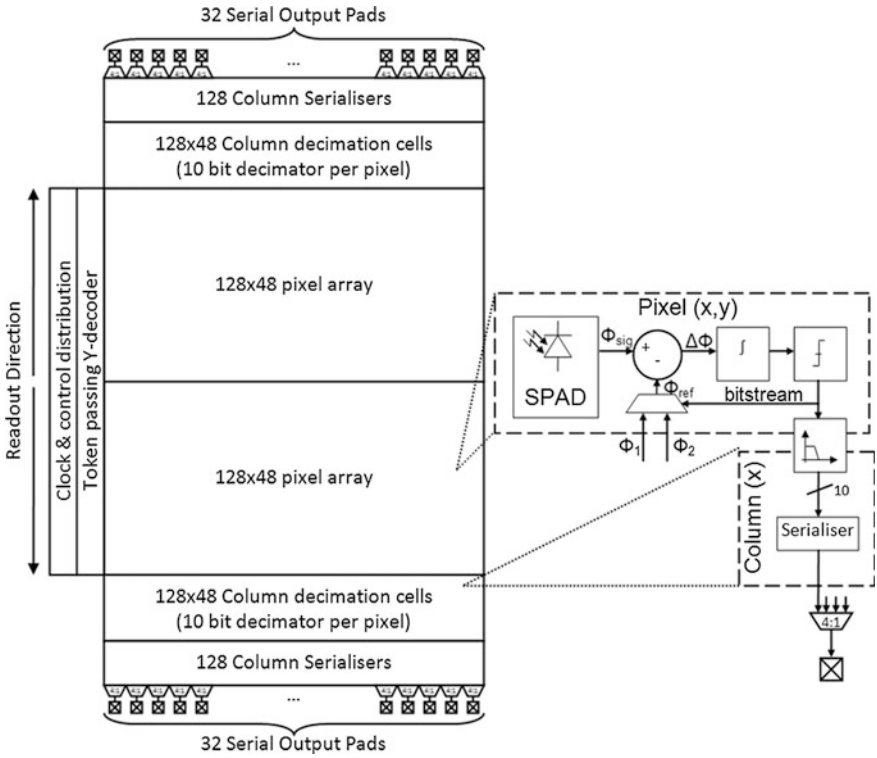

Fig. 23 Architecture of 128 × 96 pixel, all-digital, phase-domain ΔΣ based sensor reported in [31]

from each bin value using an integration of equal exposure time with the illumination source disabled.

Characterization data for the PDΔΣ, including INL and repeatability error characterization was presented in [31]. Relatively low illumination power and pulse rates were used at the expense of repeatability error. However, the PDΔΣ approach achieved an excellent linearity of ±5 mm over a 0.4–2.4 m range, with photon pile up being the dominant effect limiting accuracy at very short distances.

Figure 26 shows example images captured using the PDΔΣ sensor, serving as the first demonstration of the on-chip creation of depth-maps with only simple inter-frame averaging and defect correction being applied externally before rendering.

The use of an in-pixel, phase-domain ΔΣ loop to directly sense the mean phase of incident photons detected synchronously to the modulation of the outgoing illumination light is one approach to the management of the large volumes of data produced by single-photon 3D imagers and the associated computational burden on the host system. With the increasing commercial relevance of 3D imaging systems, such techniques seem likely to continue to develop, facilitated by the

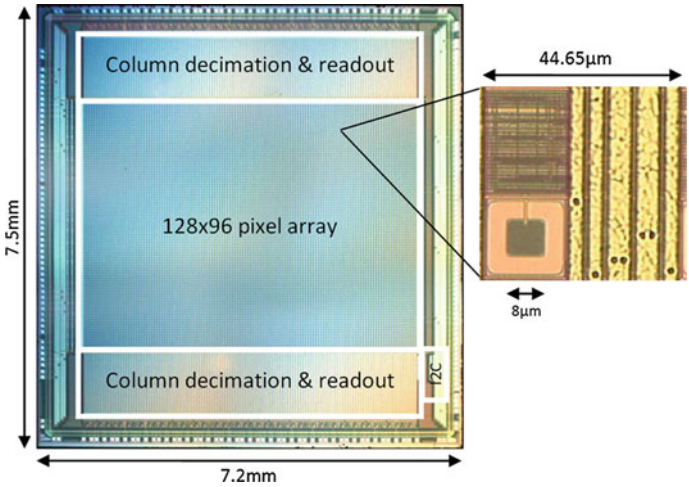

Fig. 24 Die micrograph of 128 × 96 pixel, all-digital, phase-domain ΔΣ based sensor reported in [31]

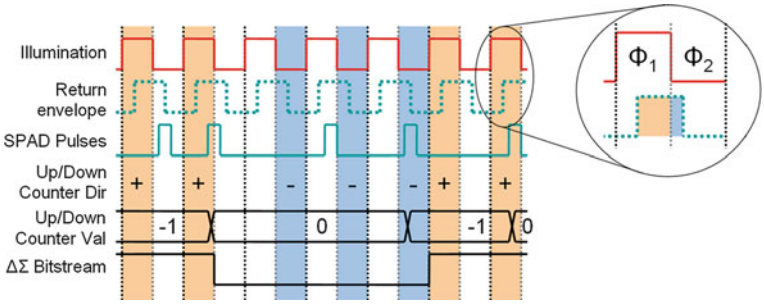

Fig. 25 Timing diagram of all-digital, phase-domain ΔΣ based pixel [31]

capabilities of modern CMOS imaging processes to yield highly integrated imaging systems.

7 Perspectives and Outlook

More recently, scanned 3D cameras have appeared based on relatively small arrays of relatively large pixels whose core is a so-called silicon photomultiplier (SiPM). SiPMs are essentially an array of non-imaged SPADs connected so as to sum all avalanche currents in one point. The more recent digital SiPM replaces the analog summing node with an OR operation. The advantage of d-SiPMs is a faster response to photon bunches and the capability of turning off individual noisy

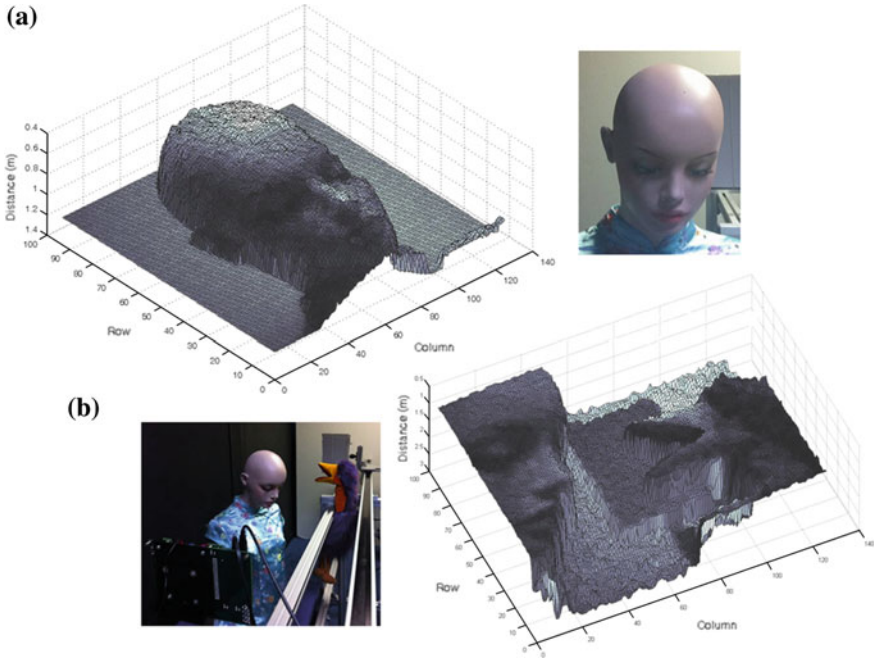

Fig. 26 Example images captured using PDΔΣ sensor [31]: **a** 20 second exposure showing mannequin at 1m distance. **b** 1 second exposure showing objects at 0.75m, 1.1m, and 1.8m

SPADs. An example of this trend has been reported by [44], where four 10 × 10 mini SiPMs have been implemented in 0.18 μm HV CMOS technology in combination with a mirror to scan large areas in TCSPC mode.

The use of mini SiPMs is spreading to other fields and applications. An example is that of medical sensors for positron emission tomography that rely on time-of-arrival detection. Borrowing technologies developed in 3D camera technology, more TDC integration together with SPADs and SPAD arrays is a clear trend.

Recent SPAD structures demonstrated in nanoscale CMOS exhibit improving DCR and spectral efficiency, as well as compatibility with TSV and backside processing [45–47]. Adoption of these advanced processes brings the prospect of simultaneous improvements in time resolution, fill factor, pixel pitch as well as the capacity to integrate on-chip Time-Of-Flight computation to ease I/O data rate demands. Analog approaches to time-resolved SPAD pixels offer a route to the smallest pixel pitch provided uniformity issues are addressed [48].

On another front, the emergence of III-V materials in configurations that are fully compatible with a CMOS fabrication line may bring these materials to the mainstream in 3D imaging. Examples of this trend are two independent works reporting the first Ge-on-Si SPADs fabricated in a way that is fully compatible with a conventional CMOS technology [49, 50]. More activity in this domain is expected, especially in the creation of larger and more compact arrays.

Ouster Exhibit 2013
IPR2023-01456 - Page 0025

Finally, 3D integration of CMOS devices is becoming a commercial reality, hence, we expect that it will extend to 3D image sensors based on SPADs where through silicon via and backside illuminated devices will become routine in the near future. This will have an immediate impact on fill factor and imager sizes. Later cost will be positively impacted and packaging simplified.

Acknowledgments The authors are grateful to the Swiss National Science Foundation, the Swiss Government sponsored Nano-Tera and MICS grants, and Xilinx Inc.'s University Program.

References

1. S. Cova, A. Longoni, A. Andreoni, Towards picosecond resolution with single-photon avalanche diodes. Rev. Sci. Instr. **52**(3), 408–412 (1981)
2. R.J. McIntyre, Recent developments in silicon avalanche photodiodes. Measurement **3**(4), 146–152 (1985)
3. S.M. Sze, Physics of Semiconductor Devices, 2nd edn. (Wiley-Interscience, New York, 1981)
4. A. Spinelli, A. Lacaita, Physics and numerical simulation of single photon avalanche diodes. IEEE Trans. Electron Devices **44**, 1931–1943 (1997)
5. G. Ripamonti, S. Cova, Carrier diffusion effects in the time-response of a fast photodiode. Solid-State Electron. **28**(9), 925–931 (1985)
6. M. Gersbach, J. Richardson, E. Mazaleyrat, S. Hardillier, C. Niclass, R.K. Henderson, L. Grant, E. Charbon, A low-noise single-photon detector implemented in a 130 nm CMOS imaging process. Solid-State Electron. **53**(7), 803–808 (2009)
7. J. Richardson, L. Grant, R. Henderson, A low-dark count single-photon avalanche diode structure compatible with standard nanometer scale CMOS technology, *International Image Sensor Workshop* (2009)
8. S. Cova, M. Ghioni, A. Lacaita, C. Samori, F. Zappa, Avalanche photodiodes and quenching circuits for single-photon detection. Appl. Opt. **35**(12), 1956–1976 (1996)
9. A. Rochas et al., Single photon detector fabricated in a complementary metal–oxide–semiconductor high-voltage technology. Rev. Sci. Instr. **74**(7), 3263–3270 (2003)
10. C. Niclass, C. Favi, T. Kluter, M. Gersbach, E. Charbon, A 128x128 Single-Photon Image Sensor with Column-Level 10-bit Time-to-Digital Converter Array. IEEE J. Solid-State Circuits **43**(12), 2977–2989 (2008)
11. C. Niclass, M. Sergio, and E. Charbon, A single photon avalanche diode array fabricated in deep-submicron CMOS technology, IEEE Design, Automation and Test in Europe, 1–6 (2006)
12. H. Finkelstein, M.J. Hsu, S.C. Esener, STI-Bounded single-photon avalanche diode in a deep-submicrometer CMOS technology. IEEE Electron Device Lett. **27**(11), 887–889 (2006)
13. C. Niclass, M. Sergio, E. Charbon, *A Single Photon Avalanche Diode Array Fabricated in 0.35μm CMOS and based on an Event-Driven Readout for TCSPC Experiments* (SPIE Optics East, Boston, 2006)
14. D. Stoppa, L. Pacheri, M. Scandiuzzo, L. Gonzo, G.-F. Della Betta, A. Simoni, A CMOS 3-D imager based on single photon avalanche diode. IEEE Trans. Circuits Syst. **54**(1), 4–12 (2007)
15. L. Pancheri, D. Stoppa, Low-noise CMOS Single-photon Avalanche Diodes with 32 ns Dead Time, in *IEEE European Solid-State Device Conference* (2007)

16. N. Faramarzpour, M.J. Deen, S. Shirani, Q. Fang, Fully integrated single photon avalanche diode detector in standard CMOS 0.18-um technology. IEEE Trans. Electron Devices **55**(3), 760–767 (2008)
17. C. Niclass, M. Sergio, E. Charbon, A CMOS 64x48 single photon avalanche diode array with event-driven readout, in *IEEE European Solid-State Circuit Conference* (2006)
18. J.S. Massa, G.S. Buller, A.C. Walker, S. Cova, M. Umasuthan, A.M. Wallace, Time-pf-flight optical ranging system based on time-correlated single-photon counting. App. Opt. **37**(31), 7298–7304 (1998)
19. M.A. Albota et al., Three-dimensional imaging laser radars with Geiger-mode avalanche photodiode arrays. Lincoln Labs J. **13**(2) (2002)
20. C. Niclass, A. Rochas, P.A. Besse, E. Charbon, Design and characterization of a CMOS 3-D image sensor based on single photon avalanche diodes. IEEE J. Solid-State Circuits **40**(9), 1847–1854 (2005)
21. M. Sergio, C. Niclass, E. Charbon, A 128x2 CMOS single photon streak camera with timing-preserving latchless pipeline readout, in *IEEE International Solid-State Circuits Conference* (2007), pp. 120–121
22. J.M. Pavia, C. Niclass, C. Favi, M. Wolf, E. Charbon, 3D near-infrared imaging based on a SPAD image sensor, *International Image Sensor Workshop* (2011)
23. J.-P. Jansson et al., A CMOS time-to-digital converter with better than 10 ps single-shot precision. IEEE J. Solid-State Circuits **41**(6), 1286–1296 (2006)
24. A.S. Yousif et al., A fine resolution TDC architecture for next generation PET imaging. IEEE Trans. Nucl. Sci. **54**(5), 1574–1582 (2007)
25. M. Lee, et al., A 9b, 1.25 ps resolution coarse-fine time-to-digital converter in 90 nm cmos that amplifies a time residue, in *IEEE Symposium on VLSI Circuits* (2007), pp. 168–169
26. P. Chen et al., A low-cost low-power CMOS time-to-digital converter based on pulse stretching. IEEE Trans. Nucl. Sci. **53**(4), 2215–2220 (2006)
27. J. Richardson, R. Walker, L. Grant, D. Stoppa, F. Borghetti, E. Charbon, M. Gersbach, R.K. Henderson, A 32x32 50 ps resolution 10 bit time to digital converter array in 130 nm CMOS for time correlated imaging, in *IEEE Custom Integrated Circuits Conference* (2009), pp. 77–80
28. M. Gersbach, Y. Maruyama, E. Labonne, J. Richardson, R. Walker, L. Grant, R.K. Henderson, F. Borghetti, D. Stoppa, E. Charbon, A Parallel 32x32 time-to-digital converter array fabricated in a 130 nm imaging CMOS technology, in *IEEE European Solid-State Device Conference* (2009)
29. C. Veerappan, J. Richardson, R. Walker, D.U. Li, M.W. Fishburn, Y. Maruyama, D. Stoppa, F. Borghetti, M. Gersbach, R.K. Henderson, E. Charbon, A 160x128 single-photon image sensor with on-pixel, 55 ps 10b time-to-digital converter,in *IEEE International Solid-State Circuits Conference* (2011), pp. 312–314
30. D. Stoppa, F. Borghetti, J. Richardson, R. Walker, L. Grant, R.K. Henderson, M. Gersbach, E. Charbon, A 32x32-pixel array with in-pixel photon counting and arrival time measurement in the analog domain, in *IEEE European Solid-State Device Conference* (2009), pp. 204–207
31. R.J. Walker, J.R. Richardson, R.K. Henderson; A 128 $\times$ 96 pixel event-driven phase-domain $\Delta\Sigma$-Based fully digital 3D camera in 0.13 μm CMOS imaging technology", in *IEEE International Solid-State Circuits Conference* (2011), pp. 410–412
32. M.A. Itzler, M. Entwistle, M. Owens, K. Patel, X. Jiang, K. Slomkowski, S. Rangwala, Geiger-mode avalanche photodiode focal plane arrays for three-dimensional imaging LADAR, in *SPIE Infrared Remote Sensing and Instrumentation* (2010), p. 7808
33. B. Aull, J. Burns, C. Chenson, B. Felton, H. Hanson, C. Keast, J. Knecht, A. Loomis, M. Renzi, A. Soares, S. Vyshnavi, K. Warner, D. Wolfson, D. Yost, D. Young, Laser radar imager based on 3D integration of Geiger-Mode avalanche photodiodes with two SOI timing circuit layers, in *Proceedings of the IEEE International Solid-State Circuits* (2006), 304–305
34. T. Spirig, P. Seitz, O. Vietze, F. Heitger, The lock-in CCD-two-dimensional synchronous detection of light. IEEE J. Quantum Electron. **31**(9), 1705–1708 (1995)

35. R. Miyagawa, T. Kanade, CCD-based range-finding sensor. IEEE Trans. Electron Devices **41**(10), 1648–1652 (1997)
36. R. Lange, P. Seitz, Solid-state Time-Of-Flight range camera. IEEE J. Quantum Electron. **37**(3), 390–397 (2001)
37. R. Schwarte, Z. Xu, H. Heinol, J. Olk, B. Buxbaum, New optical four-quadrant phase detector integrated into a photogate array for small and precise 3D cameras. SPIE Three-Dimensional Image Capture **3023**, 119–128 (1997)
38. C. Bamji, E. Charbon, Systems for CMOS-compatible three-dimensional image sensing using quantum efficiency modulation, US Patent 6,580,496 (2003)
39. C. Niclass, C. Favi, T. Kluter, F. Monnier, E. Charbon, Single-photon synchronous detection. IEEE J. Solid-State Circuits **44**(7), 1977–1989 (2009)
40. S. Donati, G. Martini, M. Norgia, Microconcentrators to recover fill-factor in image photodetectors with pixel on-board processing circuits. Opt. Express **15**(26), 18066–18075 (2007)
41. S. Kawahito, A. Yamasawa, S. Koga, Y. Tadokoro, K. Mizuno, O. Tabata; Digital interface circuits using sigma-delta modulation for integrated micro-fluxgate magnetic sensors, in *IEEE International Symposium on Circuits and Systems*, vol. 4 (1996), pp. 340–343
42. C. van Vroonhoven, K. Makinwa, A CMOS temperature-to-digital converter with an inaccuracy of $\pm$ 0.5°C (3σ) from -55 to 125°C, in *IEEE International Solid-State Circuits Conference* (2008), pp. 576–637
43. S. Kawahito, I.A. Halin, T. Ushinaga, T. Sawada, M. Homma, Y. Maeda, A CMOS Time-Of-Flight range image sensor with gates-on-field-oxide structure. IEEE Sens. J. **7**(12), 1578–1586 (2007)
44. C. Niclass, M. Soga, S. Kato, A 0.18 μm CMOS single-photon sensor for coaxial laser rangefinders, in *Asian Solid-State Circuits Conference* (2010)
45. M. Karami, M. Gersbach, E. Charbon, A new single-photon avalanche diode in 90 nm standard CMOS technology, SPIE Optics + Photonics, NanoScience Engineering, Single-Photon Imaging (2010)
46. R.K. Henderson, E. Webster, R. Walker, J.A. Richardson, L.A. Grant, A 3x3, 5um Pitch, 3-transistor single photon avalanche diode array with integrated 11 V bias generation in 90 nm CMOS technology, in *IEEE International Electron Device Meeting* (2010), pp. 1421–1424
47. E.A.G.Webster, J.A. Richardson, L.A. Grant, D. Renshaw, R.K. Henderson, An infra-red sensitive, low noise, single-photon avalanche diode in 90 nm CMOS. International Image Sensor Workshop (IISW), Hokkaido, 8–11 June 2011
48. L. Pancheri, N. Massari, F. Borghetti, D. Stoppa, A 32x32 SPAD pixel array with nanosecond gating and analog readout. International Image Sensor Workshop (IISW), Hokkaido, 8–11 June 2011
49. A. Sammak, M. Aminian, L. Qi, W.D. de Boer, E. Charbon, L. Nanver, A CMOS Compatible Ge-on-Si APD Operating in Proportional and Geiger Modes at Infrared Wavelengths, in *International Electron Device Meeting* (2011)
50. Z. Lu, Y. Kang, C. Hu, Q. Zhou, H.-D. Liu, J.C. Campbell, Geiger-mode operation of Ge-on-Si avalanche photodiodes. IEEE J. Quantum Electron. **47**(5), 731–735 (2011)

Ouster Exhibit 2013
IPR2023-01456 - Page 0028