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Paper 29
Date: April 23, 2024

PUBLIC VERSION

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

CIRRUS LOGIC, INC. and
OMNIVISION TECHNOLOGIES, INC.,[1]
Petitioner,

v.

GREENTHREAD, LLC,
Patent Owner.

IPR2024-00001
Patent 10,734,481 B2

Before KRISTINA M. KALAN, JON B. TORNQUIST, and MONICA S. ULLAGADDI, *Administrative Patent Judges*.

ULLAGADDI, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

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[1] AMS Sensors USA Inc. merged into ams-OSRAM Inc. (Paper 23), which was then terminated (Paper 27). The caption has been revised to reflect the same.

I. INTRODUCTION

A. Background and Summary

Cirrus Logic, Inc., OmniVision Technologies, Inc., and ams-OSRAM USA Inc. (collectively, "Petitioner") filed a petition for an *inter partes* review (Paper 1 ("Pet.")) challenging claims 1–9, 12–27, and 30–36 of U.S. Patent No. 10,734,481 B2 (Ex. 1001 ("the '481 patent")).[2] Greenthread, LLC ("Patent Owner") filed a Preliminary Response. Paper 15 ("Prelim. Resp."). With our authorization, Petitioner filed a Preliminary Reply (Paper 19, "Prelim. Reply"), and Patent Owner filed a Preliminary Sur-Reply (Paper 21, "Prelim. Sur-Reply").

We have authority to determine whether to institute an *inter partes* review. 35 U.S.C. § 314 (2018); 37 C.F.R. § 42.4(a) (2023). The standard for instituting an *inter partes* review is set forth in 35 U.S.C. § 314(a), which provides that an *inter partes* review may not be instituted "unless the Director determines . . . there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition."

For the reasons set forth below, we determine the information presented in the Petition establishes a reasonable likelihood that Petitioner would prevail with respect to at least one of the challenged claims. Accordingly, we institute an *inter partes* review on all claims and grounds challenged in the Petition.

[2] *Supra* n.1 (terminating the instant proceeding as to ams-OSRAM USA Inc.).

B. Real Parties-in-Interest

Each party identifies itself as a real party-in-interest. Pet. 1; Paper 6, 1. In addition, Petitioner identifies OSRAM GmbH, ams-OSRAM AG, and GlobalFoundries U.S., Inc. as real parties-in-interest. Pet. 1. In its Updated Mandatory Notices, Petitioner further identifies "ams-OSRAM USA Inc., Heptagon Holding CA Inc., ams Sensors USA, Inc.," as "real parties-in-interest." Paper 23, 1 (emphasis omitted). As noted above in footnote 1, the instant proceeding has been terminated with respect to ams-OSRAM. Paper 27.

C. Related Matters

The parties identify several proceedings involving the '481 patent as related matters, including:

Greenthread, LLC v. Cirrus Logic, Inc., No. 1:23-cv-00369 (W.D. Tex.);

Greenthread, LLC v. OmniVision Technologies, Inc., No. 2:23-cv-00212 (E.D. Tex.);

Greenthread, LLC v. OSRAM GmbH et al., No. 2:23-cv-00179 (E.D. Tex.);

Greenthread, LLC v. Texas Instruments Inc., No. 2:23-cv-00157 (E.D. Tex.); and

Greenthread, LLC v. Monolithic Power Systems, Inc., No. 1:23-cv-00579 (D. Del.). Pet. 1–2; Paper 6, 1–2.

D. The '481 Patent

The '481 patent, titled "Semiconductor Devices with Graded Dopant Regions," issued on August 4, 2020. Ex. 1001, codes (45), (54). The '481 patent "relates to all semiconductor devices and systems." *Id.* at 1:36–37.

According to the '481 patent, in bipolar junction transistors, "[e]fforts have been made in graded base transistors to create an aiding drift field to enhance the diffusing minority carrier's speed from emitter to collector." *Id.* at 1:59–61. This improvement has not been implemented in "most semiconductor devices, including various power MOSFETs . . . [and] IGBT[s]," which "still use a uniformly doped 'drift epitaxial' region in the base." *Id.* at 1:61–66. The invention of the '481 patent implements graded dopant concentration in these devices, which causes "[t]wo important performance enhancements." *Id.* at 3:42–43. These include sweeping electrons "from source to drain rapidly" and simultaneously causing holes to "be recombined closer to the n^+ buffer layer," which "can improve t_{on} and t_{off} in the same device." *Id.* at 3:43–47.

E. Illustrative Claim

Of the challenged claims, claims 1 and 20 are independent. Claim 1 is illustrative and reproduced below.

> 1. A semiconductor device, comprising:
>
> a substrate of a first doping type at a first doping level having first and second surfaces;
>
> a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;
>
> a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;
>
> transistors formed in at least one of the first active region or second active region;
>
> at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to

aid carrier movement from the first surface to the second surface of the substrate; and

at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the first surface to the second surface of the substrate.

Ex. 1001, 4:50–5:3.

F. Asserted Unpatentability Challenges

Petitioner asserts that claims 1–9, 12–27, and 30–36 are unpatentable based on the following challenges:

Claim(s) Challenged	35 U.S.C. §[3]	Reference(s)/Basis
1–9, 12–14, 16–27, 30–36	103	Kawagoe[4]
1–9, 12–14, 16–27, 30–36	103	Kawagoe, Gupta[5]
1, 2, 4–9, 12–22, 24–27, 30–36	103	Wieczorek,[6] Wolf[7]
1, 2, 4–9, 12–22, 24–27, 30–36	103	Wieczorek, Wolf, Gupta
19, 36	103	Kawagoe, Silverbrook[8]
19, 36	103	Wieczorek, Wolf, Silverbrook

Petitioner relies on the Declaration of Dr. Sanjay Banerjee. Ex. 1003.

[3] The Leahy-Smith America Invents Act ("AIA"), Pub. L. No. 112-29, 125 Stat. 284 (2011), amended 35 U.S.C. § 103, effective March 16, 2013. Because applications from which the '481 patent claims priority were filed before this date, the pre-AIA version of § 103 applies.

[4] US 6,043,114, issued Mar. 28, 2000 (Ex. 1007).

[5] US 6,163,877, issued Dec. 19, 2000 (Ex. 1014).

[6] US 2003/0183856 A1, published Oct. 2, 2003 (Ex. 1006).

[7] STANLEY WOLF & RICHARD N. TAUBER, SILICON PROCESSING FOR THE VLSI ERA, Vols. 1–4 (Lattice Press 2000) (Ex. 1008).

[8] US 6,614,560 B1, issued Sept. 2, 2003 (Ex. 1042).

II. ANALYSIS

A. Legal Standards

"In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable." *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016). The burden of persuasion never shifts to Patent Owner. *Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015).

A claim is unpatentable under 35 U.S.C. § 103 if "the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains." 35 U.S.C. § 103. The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) when present, objective evidence of nonobviousness. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

To show obviousness, it is not enough to merely show that the prior art includes separate references covering each separate limitation in a challenged claim. *Unigene Labs., Inc. v. Apotex, Inc.*, 655 F.3d 1352, 1360 (Fed. Cir. 2011). "Rather, obviousness requires the additional showing that a person of ordinary skill at the time of the invention would have selected and combined those prior art elements in the normal course of research and development to yield the claimed invention." *Id.* (citing *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 421 (2007)). "This is so because inventions in

most, if not all, instances rely upon building blocks long since uncovered, and claimed discoveries almost of necessity will be combinations of what, in some sense, is already known." *KSR*, 550 U.S. at 418–19. On the other hand, an obviousness analysis "need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ." *Id.* at 418; *accord In re Translogic Tech., Inc.*, 504 F.3d 1249, 1259 (Fed. Cir. 2007). Nevertheless, "[a] factfinder should be aware, of course, of the distortion caused by hindsight bias and must be cautious of arguments reliant upon *ex post* reasoning." *KSR*, 550 U.S. at 421.

"A person who is not a party to a suit generally has not had a 'full and fair opportunity to litigate' the claims and issues settled in that suit." *Taylor v. Sturgell*, 553 U.S. 880, 892 (2008). Thus, in general, Petitioner should not be precluded from addressing the unpatentability of a patent based on [redacted]. *See id.* (explaining that, in general, one is not bound by a judgment "in which he is not designated as a party or to which he has not been made a party by service of process"); *WesternGeco LLC v. ION Geophysical Corp.*, 889 F.3d 1308, 1319 (Fed. Cir. 2018) (noting the "general rule against nonparty preclusion"). This rule is deeply-rooted in the "historic tradition that everyone should have his own day in court." *Taylor*, 553 U.S. at 892–93 (quoting *Richards v. Jefferson County*, 517 U.S. 793, 798 (1996)).

An exception to this deeply-rooted rule exists for parties that are in privity with a defendant in an earlier litigation. *See WesternGeco*, 889 F.3d at 1319 (noting that "the standards for the privity inquiry must be grounded

in due process"). The Supreme Court in *Taylor* identified considerations where nonparty preclusion would be justified, including:

> (1) an agreement to be bound; (2) pre-existing substantive legal relationships between the person to be bound and a party to the judgment (e.g., "preceding and succeeding owners of property"); (3) adequate representation by someone with the same interests who was a party (e.g., "class actions" and "suits brought by trustees, guardians, and other fiduciaries"); (4) assumption of control over the litigation in which the judgment was rendered; (5) where the nonparty to an earlier litigation acts as a proxy for the named party to relitigate the same issues; and (6) a special statutory scheme expressly foreclosing successive litigation by nonlitigants.

Id. (citing *Taylor*, 553 U.S. at 894–95).

As this list of considerations indicates, "the mere existence of some relationship between a petitioner and another entity is not sufficient" to place that petitioner in privity with that entity. *Google LLC v. DDC Technology, LLC*, IPR2023-00707, Paper 27 at 37 (PTAB Oct. 25, 2023). Instead, "that relationship must be related to [an earlier] lawsuit and be sufficiently close that it can be fairly said the petitioner had a full and fair opportunity to litigate the validity of the patent in that lawsuit," or the evidence must demonstrate "that petitioner is simply serving as a proxy to allow another party to litigate the patent validity question that the other party raised in an earlier filed litigation." *Id.*; *WesternGeco*, 889 F.3d at 1319; *see also Ventex Co. v. Columbia Sportswear North America, Inc.*, IPR2017-00651, Paper 148, at 10, 12 (PTAB Jan. 24, 2019) (precedential) (finding privity where the two parties "had a specially structured, preexisting, and well-established business relationship with one another, including indemnification and exclusivity arrangements").

A petitioner's "initial identification of the real parties in interest [and privies] should be accepted unless and until disputed by a patent owner." *Worlds Inc. v. Bungie, Inc.*, 903 F.3d 1237, 1244 (Fed. Cir. 2018). In order to raise such a dispute, "a patent owner must produce *some* evidence that tends to show that a particular [time-barred] third party should be named a [privy]." *Id.* The amount of evidence a patent owner must produce does not rise to the level of that required to overcome a burden of production. *Id.* at 1244 n.8. One potential formulation of the amount of evidence required is "evidence that 'reasonably brings into question the accuracy of a petitioner's'" assertion that it is not time-barred. *Id.* (quoting *Atlanta Gas Light v. Bennett Regulator Guards, Inc.*, IPR2013-00453, Paper 88 (PTAB Jan. 6, 2015) (addressing the amount of evidence required from a patent owner to question a petitioner's identification of the real parties in interest)). Although the "burden remains with the petitioner to establish" the timeliness of its petition, it need not respond until the patent owner reasonably brings into question the accuracy of its assertion that it is not time-barred. *Id.* at 1242.

B. Level of Ordinary Skill in the Art

Petitioner asserts that a person of ordinary skill in the art "would have had a Bachelor's degree in electrical engineering, material science, applied physics, or a related field, and four years of experience in semiconductor design and manufacturing or equivalent work experience." Pet. 10 (citing Ex. 1003 ¶¶ 44–47). According to Petitioner, "[a]dditional education might compensate for a deficiency in experience, and vice-versa." *Id.* On the present record, Patent Owner does not contest Petitioner's definition of a person of ordinary skill in the art. *See generally* Prelim. Resp.

In light of the record before us, and for purposes of this Decision, we adopt Petitioner's proposal regarding the level of ordinary skill in the art. Based on our review of the '481 patent and the prior art of record, we determine that the definition offered by Petitioner comports with the qualifications a person would have needed to understand and implement the teachings of the '481 patent and the prior art. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001) (explaining that specific findings regarding ordinary skill level are not required "where the prior art itself reflects an appropriate level and a need for testimony is not shown") (quoting *Litton Indus. Prods., Inc. v. Solid State Sys. Corp.*, 755 F.2d 158, 163 (Fed. Cir. 1985)).

C. Claim Construction

In an *inter partes* review, we construe claim terms according to the standard set forth in *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–17 (Fed. Cir. 2005) (en banc). 37 C.F.R. § 42.100(b). Under *Phillips*, claim terms are afforded "their ordinary and customary meaning." *Phillips*, 415 F.3d at 1312. "[T]he ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention." *Id.* at 1313. "Importantly, the person of ordinary skill in the art is deemed to read the claim term not only in the context of the particular claim in which the disputed term appears, but in the context of the entire patent, including the specification." *Id.*

Neither party proposes any claim terms for construction. Pet. 10–11; *see generally* Prelim. Resp. After considering the arguments and information presented in the Petition and Preliminary Response, we agree that we do not need to construe any terms expressly in order to determine

whether to institute trial. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (citing *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999) ("[O]nly those terms need be construed that are in controversy, and only to the extent necessary to resolve the controversy.")).

D. Timeliness of Petition Under 35 U.S.C. § 315(b)

Patent Owner argues that the Petition should be dismissed because it is untimely. Prelim. Resp. 1–2. Specifically, Patent Owner argues that Petitioner is in privity with [redacted] who Patent Owner asserts are time-barred under 35 U.S.C. § 315(b) and [redacted] *Id.* at 2–3, 6. Patent Owner argues that [redacted] *Id.* at 3 (citing *Applications in Internet Time, LLC v. RPX Corp.*, 897 F.3d 1336, 1360 (Fed. Cir. 2018)). Patent Owner advances several theories, including that [redacted] for custom-made products. *Id.*

1. Legal Standard

"[T]he mere existence of some relationship between a petitioner and another entity is not sufficient" to place that petitioner in privity with that entity. *Google LLC v. DDC Technology, LLC*, IPR2023-00707, Paper 27

at 37 (PTAB Oct. 25, 2023). Instead, "that relationship must be related to [an earlier] lawsuit and be sufficiently close that it can be fairly said the petitioner had a full and fair opportunity to litigate the validity of the patent in that lawsuit." *Id.* In other words, privity concerns "whether the petitioner and the prior litigant's relationship—as it relates to the [earlier] lawsuit—is sufficiently close that it can be fairly said that the petitioner had a full and fair opportunity to litigate the validity of the patent in that lawsuit," or "whether the petitioner is simply serving as a proxy to allow another party to litigate the patent validity question that the other party raised in an earlier filed litigation." *WesternGeco LLC v. ION Geophysical Corp.*, 889 F.3d 1308, 1319 (Fed. Cir. 2018).

A petitioner's "initial identification of the real parties in interest [and privies] should be accepted unless and until disputed by a patent owner." *Worlds Inc. v. Bungie, Inc.*, 903 F.3d 1237, 1242 (Fed. Cir. 2018). In order to raise such a dispute, "a patent owner must produce *some* evidence that tends to show that a particular [time-barred] third party should be named a [privy]." *Id.* at 1244. The amount of evidence a patent owner must produce does not rise to the level of that required to overcome a burden of production. *Id.* at 1244 n.8. Instead, the "burden remains with the petitioner to establish" the timeliness of its petition. *Id.* at 1242.

2. Whether We May Consider Petitioner's Preliminary Reply

As noted above, we authorized Petitioner to file a Preliminary Reply and Patent Owner to file a Preliminary Sur-Reply, both limited to addressing the issue of the timeliness of the Petition. *Supra* § I.A. Patent Owner argues that Petitioner's Preliminary Reply is not appropriate because Petitioner "could have reasonably foreseen" Patent Owner's untimeliness arguments

when filing its petition and because Patent Owner informed Petitioner about these arguments before it filed petitions challenging related patents. Prelim. Resp. 33 (quoting *Sandoz Inc. v. Abbvie Biotechnology Ltd.*, IPR2018-00002, Paper 11 at 3 (PTAB Mar. 6, 2018)) (citing Ex. 2011); Prelim. Sur-Reply 10.

We disagree with this argument raised by Patent Owner. According to the Federal Circuit, a petitioner's "initial identification of the real parties in interest [and privies] should be accepted unless and until disputed by a patent owner." *Worlds*, 903 F.3d at 1242. Thus, there is no requirement that a petitioner preemptively address a disputed issue of privity in its petition. Furthermore, Patent Owner's email to Petitioner about the privity issue (Exhibit 2011) was sent *after* the Petition was filed. *See* Prelim. Resp. 14.

Moreover, Petitioner is not required to address potential arguments that Patent Owner may, but has not yet made, in its Preliminary Response. *See* Ex. 2011. This is especially true where Patent Owner's assertions of privity, for the reasons set forth below, are not sufficient to reasonably call into question Petitioner's assertion that the Petition is timely.

Accordingly, we consider Petitioner's Preliminary Reply, as well as Patent Owner's Preliminary Sur-Reply, in determining whether Petitioner has shown its Petition is timely.

3. The Effect of the Earlier Suit [redacted] on the Timeliness of the Present Petition

Section 315(b) bars institution of *inter partes* review only when "the petition requesting the proceeding is filed more than 1 year after the date on which the petitioner, real party in interest, or privy of the petitioner is served with a complaint alleging infringement of the patent." Patent Owner alleges

that [redacted] are time-barred under § 315(b). Prelim. Resp. 1–3.

As to [redacted] the record does not contain evidence [redacted] was served with a complaint alleging infringement of the '481 patent.

The present record also does not contain any evidence tending to show that [redacted] is time-barred either. On this record, there is no evidence that [redacted] any earlier than January 23, 2023, which is less than one year before the filing of the Petition on October 12, 2023. *Compare* Pet. 106, *with* Ex. 2009, 1 (cited at Prelim. Resp. 5). Accordingly, the service of [redacted] time-barred under § 315(b).

Patent Owner also argues that, because [redacted] was served with an infringement complaint early enough to create a time bar and because [redacted] is time-barred under § 315(b). Prelim. Resp. 4 (arguing that [redacted]), 17. Patent Owner also argues that "[i]t is . . . Petitioners' burden to show that their *specific* customer-manufacturer relationships are the kind that *do not* create privity, as opposed to the kind that do." Prelim. Sur-reply 4. We are presented with no authority, however, for extending the time bar of Section 315(b) to a party that was a real party in interest to a potentially time-barred party. For the foregoing reasons, and at this stage of the proceeding, Patent Owner has produced no evidence that [redacted] is a time-barred entity under § 315(b).[9]

[9] In the next section, we address Patent Owner's argument that [redacted]. Our findings as to [redacted] provide

4. [redacted]

In the subsections below, we address Patent Owner's arguments that [redacted] of Petitioner and Petitioner's real party-in-interest, GlobalFoundries[10] under § 315(b).

a) Agency

Patent Owner argues that "[b]y making custom [redacted], Petitioners step into their shoes, and serve[] as their 'agent,' by [redacted] Prelim. Resp. 3; *see id.* at 22–25. We disagree for three reasons.

First, Patent Owner's agency argument is not based on the applicable legal standard. For purposes of privity under § 315(b), the relevant question is whether Petitioner is acting as an agent for [redacted] in filing a petition for *inter partes* review. The applicable principle is that "preclusion is appropriate when a nonparty later brings suit as an agent for a party who is bound by a judgment." *Taylor*, 553 U.S. at 895. As the Federal Circuit explains, the rationale behind § 315(b)'s time bar is "to prevent successive challenges to a patent by those who previously have had the opportunity to make such challenges in prior litigation." *WesternGeco*, 889 F.3d at 1319. Therefore, the relevant question is "whether the petitioner is simply serving as a proxy to allow another party to litigate the patent validity question that the other party raised in an earlier-filed litigation." *Id.* Here, Patent Owner does not assert that Petitioner is acting as an agent for

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additional support for our determination that service of a complaint against [redacted] does not give rise to a time bar.

[10] Petitioner identifies GlobalFoundries U.S., Inc. ("GlobalFoundries") as a real party-in-interest. Pet. 1.

[redacted] in this proceeding. Any such assertion would be appropriate only based on evidence that [redacted]. *See* *Taylor*, 553 U.S. at 906 (cautioning that "preclusion is appropriate only if the putative agent's conduct of the suit is subject to the control of the party who is bound by the prior adjudication"). No such evidence is in this record.

Second, the case law cited by Patent Owner does not apply.[11] In each case, the alleged privy was the party asserting a defense of res judicata or collateral estoppel, not the party against whom collateral estoppel was asserted, as is the case here.[12] The privity issue was whether the party raising a res judicata or collateral estoppel *defense* was in privity with a defendant in a prior lawsuit brought by the same plaintiff. In *Herrion*, for example, the plaintiff brought successive lawsuits arising out of the same incident, and the defendants in the second suit asserted a res judicata defense. 448 F. App'x at 72. Applicable res judicata law required the court to consider whether the defendants in the second lawsuit were in privity with the defendant in the first lawsuit. *Id.* at 72–73 (finding privity existed for res

[11] Prelim. Resp. 23 (citing *Herrion v. Children's Hosp. Nat. Med. Ctr.*, 786 F. Supp. 2d 359 (D.D.C. 2011), *aff'd*, 448 F. App'x 71 (D.C. Cir. 2011); *John Street Leasehold, LLC v. Cap. Mgmt. Res., L.P.*, 283 F.3d 73, 75 (2d Cir. 2002); *Fiumara v. Fireman's Fund Ins. Companies*, 746 F.2d 87, 87 (1st Cir. 1984)).

[12] By asserting Petitioner is time-barred under § 315(b), Patent Owner is in effect asserting a collateral estoppel bar against Petitioner. *See* *WesternGeco*, 889 F.3d at 1318 ("Privity is essentially a shorthand statement that collateral estoppel is to be applied in a given case." (citing Consolidated Trial Practice Guide ("CTPG"), November 2019 at 15, available at https://www.uspto.gov/TrialPracticeGuideConsolidated)).

judicata purposes). Similarly, in *John Street*, the court held that plaintiff's second lawsuit was barred by res judicata in part because the defendants were in privity with the defendants in the prior action. 283 F.3d at 75. Likewise in *Fiumara*, the court held that "the res judicata defense is unmistakably available" to the defendants "as persons in privity with" the defendants in a prior lawsuit brought by the same plaintiff. 746 F.2d at 92. The privity issue in each of these cases was entirely different from this case, where Patent Owner asserts that Petitioner is *barred* because Petitioner is in privity with the defendants in the prior lawsuit.

Third, even if Patent Owner's argument were on solid legal footing, it lacks factual support in the record. An "essential element[] of agency" is "the principal's 'right to direct or control' the agent's actions." *In re Google LLC*, 949 F.3d 1338, 1345 (Fed. Cir. 2022) (quoting *Meyer v. Holley*, 537 U.S. 280, 286 (2003)). Patent Owner does not argue in the Preliminary Response that [redacted], much less direct us to any evidence that would tend to prove the existence of such a right. *See, e.g.*, Prelim. Resp. 22–25. Patent Owner argues that GlobalFoundries "produc[es] ICs for other companies, rather than those of its own design" and that Cirrus Logic makes "custom" products. *Id.* at 25 (citing Ex. 2033, 12, 35) (alteration in original). Patent Owner does not, however, present any evidence that any Petitioner manufactures products [redacted] *Cf. In re Google*, 949 F.3d at 1346 (contracts to "[a]ssembl[e] equipment based on information and instructions provided by Google" were "suggestive of an agency relationship;" first alteration in original). Patent Owner also does not allege that any particular product

[redacted]. Thus, Patent Owner does not direct us to any evidence that Petitioner [redacted].

b) Preceding and Succeeding Owners of Property

Patent Owner argues that [redacted] Prelim. Resp. 3; *see id.* at 25–29 (citing *Taylor*, 553 U.S. at 894). Entities who are "preceding and succeeding owners of property" can be in privity with one another. *Taylor*, 553 U.S. at 894. But this rule does not extend to the point where all manufacturers of allegedly infringing goods are in privity with the customers who buy those goods. *See, e.g.*, *WesternGeco*, 889 F.3d at 1319–22 (finding that the parties "had a contractual and fairly standard customer-manufacturer relationship regarding the accused product," which "does not necessarily suggest that the relationship is sufficiently close that both" parties should be considered to be in privity); *Wi-Fi One, LLC v. Broadcom Corp.*, 887 F.3d 1329, 1340–41 (Fed. Cir. 2018) (same); *Samsung Electronics Co. Ltd. v. Netlist Inc.*, IPR2022-00615, Paper 64 at 22–26 (PTAB June 30, 2023) (same).

Patent Owner alleges that [redacted] Prelim. Resp. 25. For example, Patent Owner asserts that Cirrus Logic chips are [redacted], and these chips are accused in both the current litigation against Cirrus Logic[13] and the [redacted]. *Id.* at 7–9. Patent Owner

[13] *See* Section I.C. (Related Matters).

makes a similar assertion regarding OmniVision chips. *Id.* at 11. Patent Owner asserts that [redacted], but has not made any infringement allegation against GlobalFoundries and has not identified any accused product or component made by GlobalFoundries.

Under the applicable legal standard, we accept Petitioner's identification of the real parties-in-interest and privies absent *some* evidence that tends to show that a particular time-barred third party is a privy of Petitioner. *Worlds*, 903 F.3d at 1243–44. There is no requirement that a petition identify petitioner's customers as privies, unless the petitioner and the customers have a sufficiently close relationship that "it can be fairly said that the petitioner had a full and fair opportunity to litigate the validity of the patent in that lawsuit" or that or that petitioner is serving as a proxy to allow the customer to challenge the patent. *WesternGeco*, 889 F.3d at 1319.

Patent Owner's evidence that Petitioner's products are [redacted] does not come close to meeting this standard. Patent Owner does not assert that any of Petitioner's products were specifically accused in prior litigation [redacted],[14] or that any

[14] For example, Patent Owner alleges that Cirrus Logic's chips "CS35L41 and CS40L25 are both currently accused, . . . and both are [redacted] Prelim. Resp. 8 (citing Exs. 2018, 2021, 2035). Patent Owner's evidence does not show that Cirrus Logic's chips CS35L41 or CS40L25 were accused during the [redacted]. Although Patent Owner cites a Teardown report (Ex. 2035), Patent Owner does not show that the report was cited or relied upon in the [redacted]. Furthermore, the report shows that the accused [redacted] contains "16 major ICs" (integrated circuits), all but one of which are supplied by manufacturers other than Cirrus Logic. *Id.* at 2.

Petitioner was involved in those cases through third party discovery or otherwise. There is no suggestion that any Petitioner was even aware of the '481 Patent or Patent Owner's infringement claim before being served with a complaint. *See* Ex. 2027, 15 ¶ 47 (May 10, 2023, complaint: "Omnivision has obtained knowledge of Greenthread's patents and its infringement at least through the filing of this Complaint."); Ex. 3005, 12 ¶ 39 (June 16, 2023, amended complaint: "Cirrus Logic has knowledge of the Greenthread patents at least through the service of the Complaint."). Thus, Patent Owner does not present evidence that lends support to a finding that [redacted] renders them privies.

c) [redacted]

Patent Owner argues [redacted]. Prelim. Resp. 28–29 (citing *Ventex Co. v. Columbia Sportswear North America, Inc.*, IPR2017-00651, Paper 148 (PTAB Jan. 24, 2019) (precedential)). We disagree. Unlike the agreements in *Ventex*, Paper 148 at 12, [redacted] Even if Petitioner were considered a [redacted].[15]

[15] In contract law, a third-party beneficiary is not a privy. *See, e.g.*, *Pac. Gas & Elec. Co. v. United States*, 838 F.3d 1341, 1350–51 (Fed. Cir. 2016) ("Limited exceptions to the privity requirement have been recognized when

d) Patent Exhaustion

Patent Owner argues that the doctrine of patent exhaustion [redacted] Prelim. Resp. 29; *see id.* at 30. According to Patent Owner, [redacted] *Id.* at 30. We disagree. Although [redacted] against any claim of infringement by Patent Owner, we do not see how such a defense [redacted].

e) Indemnification

Patent Owner argues that [redacted] Prelim. Resp. 30. As evidence of this alleged indemnification obligation, Patent Owner argues that [redacted] *Id.* (quoting Paper 11, 8; citing Ex. 2033, 24). Patent Owner also directs us to the indemnification

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a 'party standing outside of privity by contractual obligation stands in the shoes of a party within privity,' such as when a party can demonstrate that it was an intended third-party beneficiary under the contract."); *Prime Finish, LLC v. Cameo, LLC*, 487 F. App'x 956, 959 (6th Cir. 2012) ("Ordinarily, the obligations arising out of a contract are due only to those with whom it is made; a contract cannot be enforced by a person who is not a party to it or in privity with it, except . . . under certain circumstances, [such as] by a third-party beneficiary." (alterations in original)).

provisions of Petitioner Cirrus Logic's "standard sales agreement[]." *Id.* at 10, 18 (citing Ex. 2026, 1, 4–5).

An agreement by a petitioner to indemnify a third party in an earlier infringement suit can give rise to a privity relationship between the petitioner and that third party. *Intel Corp. v. U.S. Int'l Trade Comm'n*, 946 F.2d 821, 839 (Fed. Cir. 1991). But not all indemnification agreements create privity between the parties to the agreement. An indemnification agreement does not give rise to privity where the indemnitor has the option either "to pay for any litigation defense expenses or for any damages related to infringement" or, in the alternative, "to modify or replace the equipment if an infringement claim [is] made," as opposed to being required "to defend [the indemnitee] from a patent infringement lawsuit, reimburse or pay for a lawsuit, cover any damages liability for any adverse patent infringement verdict against [the indemnitee], or initiate an invalidity challenge in one or more fora." *WesternGeco*, 889 F.3d at 1321. Patent Owner does not explain why the terms and conditions to which it directs us are of the latter type rather than the former. Prelim. Resp. 30; Ex. 2026, 4–5. Accordingly, on the present record, Patent Owner does not direct us to evidence that the indemnification agreement [redacted].

5. Conclusion as to Timeliness of Petition

As noted above, privity concerns "whether the petitioner and the prior litigant's relationship—as it relates to the [earlier] lawsuit—is sufficiently close that it can be fairly said that the petitioner had a full and fair opportunity to litigate the validity of the patent in that lawsuit," or "whether the petitioner is simply serving as a proxy to allow another party to litigate

the patent validity question that the other party raised in an earlier filed litigation." *WesternGeco*, 889 F.3d at 1319. A petitioner's "initial identification of the real parties in interest [and privies] should be accepted unless and until disputed by a patent owner." *Worlds*, 903 F.3d at 1244. In order to raise such a dispute, "a patent owner must produce *some* evidence that tends to show that a particular [time-barred] third party should be named a [privy]." *Id.* Here, Patent Owner argues that it has produced such evidence in several respects, but, on the present record, none of the evidence in question tends to show either that [redacted].

E. Challenge Based on Kawagoe Alone

Petitioner contends claims 1–9, 12–14, 16–27, 30–36 would have been obvious in view of Kawagoe. Pet. 7, 15–52. On the present record, Patent Owner does not dispute Petitioner's arguments. *See generally* Prelim. Resp.

1. Kawagoe

Kawagoe discloses a process for manufacturing a semiconductor integrated circuit device using an epitaxial wafer, i.e., a semiconductor wafer having a semiconductor single crystal epitaxial layer grown over a polished semiconductor substrate. Ex. 1007, 1:13–27, 2:31–35. According to Kawagoe, "[t]he epitaxial wafer is advantageous in that it is excellent in suppressing the soft errors and resisting to the latchup,"[16] as well as

[16] Petitioner submits Exhibit 1009 (Wang and Agrawal, *Single Event Upset: An Embedded Tutorial*, 21st Int'l Conf on VLSI Design, 429–434, IEEE 2008), which explains that "soft errors" are "random and not related to permanent hardware faults" and "[t]heir causes may be internal (e.g., interconnect coupling) or external (e.g., cosmic radiation)," including "alpha

"drastically reduc[ing] the defect density of the gate insulating film" of a semiconductor integrated device. *Id.* at 1:33–40.

Kawagoe discloses various "representative" processes, including processes in which the single crystal (epitaxial) layer contains an impurity of the same type and in the same concentration as the substrate body. Ex. 1007, 2:55–3:9. According to Kawagoe, the impurity concentration of the substrate body can be made higher than that of epitaxial layer "so that the resistance of the semiconductor substrate body can be relatively lowered to improve the resistance to the latchup." *Id.* at 4:1–8. Kawagoe discloses a process for manufacturing a semiconductor integrated circuit device including a step of forming a semiconductor region (well) extending below the epitaxial layer and having an impurity concentration that decreases with increasing depth below the epitaxial layer. *Id.* at 3:10–25. According to Kawagoe, the well can be used for forming a complementary Metal-Oxide-Semiconductor.Field-Effect-Transistor ("MOS.FET") circuit. *Id.* at 3:32–38.

Kawagoe describes seven embodiments, including Embodiment 1 (Ex. 1007, 6:41–12:40, Figs. 1–8) and Embodiment 4 (*id.* at 14:46–19:64, Figs. 16–25). According to Embodiment 1, a semiconductor integrated circuit device includes semiconductor substrate body 2S, epitaxial layer 2E, and gettering layer 2G. *Id.* at 6:51–56, Fig. 1. Substrate body 2S and epitaxial layer 2E are doped with p-type impurity in equal concentrations.

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particles [that] are emitted when the nucleus of an unstable isotope decays to a lower energy state." Ex. 1009, Abstract, 430. Dr. Banerjee characterizes "latchup" as "a 'short-circuit' failure condition in poorly designed circuits." Ex. 1003 ¶ 75.

Id. at 6:60–7:3, 10:51–55, 11:12–16. Embodiment 1 includes n-channel MOS.FET ("nMOS") 4N and p-channel MOS.FET ("pMOS") 4P, the latter being formed in n-well 6, which is doped with n-type impurity and extends below the epitaxial layer. *Id.* at 8:46–52, 9:32–40, 11:18–24, 11:43–50, Figs. 1, 5, 7.

According to Embodiment 4, substrate body 2S and epitaxial layer 2E are doped with p-type impurity, and the impurity concentration of substrate body 2S is higher than that of epitaxial layer 2E "to improve the resistance to the latchup." Ex. 1007, 14:64–15:6, 15:13–17, 16:16–21, 19:59–63, Fig. 17. Embodiment 4 includes p-well 6*p* formed with nMOS 4N and n-well 6*n* formed with pMOS 4P. *Id.* at 15:26–40, 17:40–18:35, Figs. 16, 21–23. In Embodiment 4, the impurity concentration in p-well 6*p* and n-well 6*n* decreases with increasing depth below the epitaxial layer. *Id.* at 15:62–16:15, 17:55–61, Fig. 17. Kawagoe discloses that the concentration gradient reduces soft errors by attracting carriers (electrons) to the substrate and preventing them from entering the p-well. *Id.* at 16:2–11.

Petitioner relies on Kawagoe Figures 17 and 23, which are reproduced below and illustrate Embodiment 4 and its properties.

FIG. 17

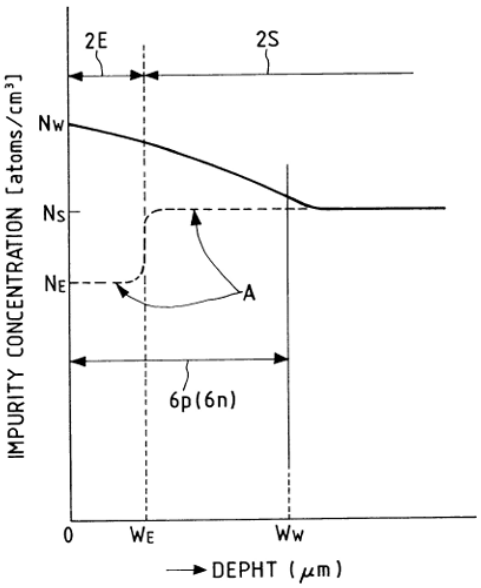

FIG. 23

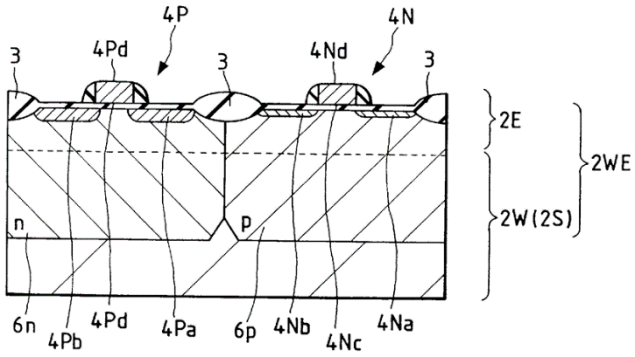

Figure 17 is a plot of impurity concentration as a function of depth in a semiconductor integrated circuit device, which shows "the p-well 6*p* and n-well 6*n* have their impurity concentrations gradually lowered in the depthwise direction from the principal surface (having an impurity concentration N_W) of the epitaxial layer 2E." Ex. 1007, 5:41–45, 15:62–16:40. Figure 23 shows a step in a process for manufacturing a semiconductor integrated circuit device, including p-well 6*p* formed with nMOS 4N and n-well 6*n* formed with pMOS 4P. *Id.* at 6:1–4, 15:26–32, 18:3–35.

2. Analysis

Petitioner argues that Kawagoe would have taught or suggested the limitations of the challenged claims. Pet. 5–45.

a) Claim 1

The preamble of claim 1 recites "[a] semiconductor device." Ex. 1001, 4:50. Petitioner argues that Kawagoe teaches the preamble.

Pet. 16–17. Kawagoe discloses "a semiconductor integrated circuit device." Ex. 1007, 1:15–16, 14:50–51. At this stage of the proceeding, Petitioner has shown sufficiently that Kawagoe teaches the preamble of claim 1.

Claim 1 recites "a substrate of a first doping type at a first doping level having first and second surfaces." Ex. 1001, 4:51–52. Relying on a combination of Kawagoe's Embodiment 1 and Embodiment 4, Petitioner argues that Kawagoe teaches this limitation. Pet. 17–24. Petitioner contends that "a substrate of a first doping type" is taught by Kawagoe's epitaxial substrate, including epitaxial layer 2E and substrate body 2S doped with p-type impurity, and that the recited "surface" corresponds to the top surface of the epitaxial substrate. *Id.* at 17–19 (citing Ex. 1007, 6:50–7:3, 14:61–15:12, 17:10–18:38, Figs. 20, 23). Petitioner contends that the recitation, "at a first doping level," is taught by Kawagoe's Embodiment 1, which has a uniformly-doped epitaxial substrate, with epitaxial layer 2E and substrate body 2S having the same impurity concentration. *Id.* at 19–20 (citing Ex. 1007, code (57), 2:57–3:9, 6:60–7:3). Petitioner contends that a POSITA would have understood that Kawagoe teaches forming a twin-well CMOS device on either a uniformly doped epitaxial substrate, as described in Embodiment 1, or a non-uniformly doped latchup-resistant epitaxial substrate, as described in Embodiment 4. *Id.* at 20 (citing Ex. 1003 ¶ 70). Relying on Dr. Banerjee's testimony and various prior art disclosures, Petitioner contends that a POSITA would have been motivated to use a uniformly-doped epitaxial substrate to form a twin-well CMOS device and would have had a reasonable expectation of success. *Id.* at 20–24 (citing Ex. 1003 ¶¶ 71–76; Ex. 1007, 1:33–40, 2:57–65, 8:40–52, 12:8–40, 14:58–60, 15:7–40, 19:49–63, Fig. 23; Ex. 1008, 381, 387–89, 406, 419, 523, 530;

Ex. 1026, 1). We find that Petitioner's contention for this limitation is sufficiently supported for purposes of institution.

Claim 1 recites "a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed." Ex. 1001, 4:53–56. Petitioner argues that Kawagoe teaches this limitation. Pet. 24–26. Kawagoe discloses "semiconductor regions 4Na and 4Nb . . . for forming the source-drain regions of the nMOS 4N." Ex. 1007, 8:66–67, Fig. 23. Petitioner contends that Kawagoe's semiconductor regions 4Na and 4Nb (corresponding to the "first active region") have a doping type (n-type) opposite to the doping type (p-type) of the substrate. Pet. 25. Kawagoe discloses that these regions "are doped with an n-type impurity such as phosphor[us] (P) or arsenic (As)." Ex. 1007, 8:67–9:3. Petitioner directs us to evidence tending to show that source-drain regions 4Na and 4Nb, as well as the channel region between those regions and below insulating film 4Nc, all would have been considered part of an active region. Ex. 1008B, 299–300 ("The active regions are those in which transistor action occurs; i.e., the channel and the heavily doped source and drain regions."). At this stage of the proceeding, Petitioner has shown sufficiently that Kawagoe teaches this limitation of claim 1.

Claim 1 recites "a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed." Ex. 1001, 4:57–59. Petitioner argues that Kawagoe teaches this limitation. Pet. 16–18. Kawagoe discloses "semiconductor regions 4Pa and 4Pb . . . for forming the source-drain regions of the pMOS 4P." Ex. 1007, 9:47–48, Fig. 23. These regions "are

doped with a[] p-type impurity such as boron." *Id.* at 9:48–50. Petitioner directs us to evidence that source-drain regions 4Pa and 4Pb, as well as the channel region between those regions and below insulating film 4Pc all would have been considered part of an active region. Ex. 1008B, 299–300 ("The active regions are those in which transistor action occurs; i.e., the channel and the heavily doped source and drain regions."). This active region is separate from and disposed adjacent to the first active region. Ex. 1007, Fig. 23. At this stage of the proceeding, Petitioner has shown sufficiently that Kawagoe teaches this limitation of claim 1.

Claim 1 recites "transistors formed in at least one of the first active region or second active region." Ex. 1001, 4:60–61. Petitioner argues that Kawagoe teaches this limitation. Kawagoe discloses forming transistors 4N and 4P, each in an active region, as discussed above. Ex. 1007, 8:66–9:3, 9:47–50, Fig. 23. Petitioner notes that the disclosure of Kawagoe satisfies claim 1's recitation of "transistors" either under Patent Owner's district court construction of "transistors" as requiring one or more transistors, or under an alternative construction requiring multiple transistors in each active region. Pet. 25 ("forming multiple nMOS transistors would have been obvious as a mere duplication of parts lacking unexpected results"), 27–28 ("a POSITA would have understood that forming multiple pMOS transistors in this [second active] region would have been obvious"), 84–85 (citing Ex. 1003 ¶¶ 78, 82; Ex. 1014, 1:52–54, 2:17–21, Fig. 23; Ex. 1020, 31).

Claim 1 recites "at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate." Ex. 1001, 4:62–65. Petitioner argues that Kawagoe teaches this

limitation. Pet. 28–34. Kawagoe discloses its wells "hav[ing] their impurity concentrations gradually lowered in the depthwise direction from the principal surface . . . of the epitaxial layer 2E." Ex. 1007, 15:62–16:2, Figs. 17, 23. Petitioner directs us to evidence that tends to show that these depthwise variations in impurity concentrations include the channel regions of each active region and that such variations in impurity concentrations help to move carriers down into the substrate, away from the top surface and toward the bottom surface. Ex. 1003 ¶ 86; Ex. 1007, 5:41–45, 15:32–36, 16:2–11, Figs. 17, 23; Ex. 1016, 289–90. At this stage of the proceeding, Petitioner has shown sufficiently that Kawagoe teaches this limitation of claim 1.

Claim 1 recites "at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the first surface to the second surface of the substrate." Ex. 1001, 4:66–5:3. Petitioner argues that Kawagoe teaches this limitation. Pet. 34–39. Kawagoe discloses its wells "hav[ing] their impurity concentrations gradually lowered in the depthwise direction from the principal surface . . . of the epitaxial layer 2E." Ex. 1007, 15:62–16:2, Figs. 17, 23. Petitioner directs us to evidence that tends to show that these depthwise variations in impurity concentrations sweep carriers down into the substrate, away from the top surface and toward the bottom surface. *Id.* at 5:41–45, 15:32–36, 16:2–11, Figs. 17, 23; Ex. 1016, 289–90. At this stage of the proceeding, Petitioner has shown sufficiently that Kawagoe teaches this limitation of claim 1.

b) Remaining Claims

In view of our determination that Petitioner establishes a reasonable likelihood for claim 1, and because Petitioner's arguments and evidence for remaining claims 2–9, 12–14, 16–27, 30–36 (Pet. 39–52) are similar to Petitioner's arguments and evidence for claim 1 (*id.* at 15–39) and are unopposed at this stage by Patent Owner, we determine that it is unnecessary to provide an explicit analysis of Petitioner's challenges to the remaining claims in order to provide guidance to the parties for the upcoming trial. Consolidated Trial Practice Guide November 2019 ("CTPG")[17] at 64; *see* 37 C.F.R. § 42.108(a) ("When instituting *inter partes* review, the Board will authorize the review to proceed on all of the challenged claims and on all grounds of unpatentability asserted for each claim."); *see also SAS Institute Inc. v. Iancu*, 138 S. Ct. 1348, 1359–60 (2018) (holding that 35 U.S.C. § 314 forbids the Board's prior "partial institution" practice).

F. Challenges Based on the Combination of Wieczorek and Wolf

Petitioner contends claims 1, 2, 4–9, 12–22, 24–27, 30–36 would have been obvious in view of the combination of Wieczorek and Wolf. Pet. 7, 52–90. On the present record, Patent Owner does not dispute Petitioner's arguments. *See generally* Prelim. Resp.

1. Wieczorek

Wieczorek relates "to a semiconductor device, such as a field-effect transistor, having an improved retrograde dopant profile in a channel region of the transistor element." Ex. 1006 ¶ 2. The Petition relies on Wieczorek's description of the prior art, not its disclosed improvement. Pet. 11, 40.

[17] *Available at* https://www.uspto.gov/TrialPracticeGuideConsolidated.

Wieczorek explains that a retrograde channel dopant profile is one where "the concentration of dopants increases from the gate insulation layer to the areas located deeper down the channel region." Ex. 1006 ¶ 6. According to Wieczorek, a retrograde channel dopant profile is desirable, but "very difficult to obtain." *Id.* Wieczorek states that "the dopant concentration immediately after the implantation process exhibits a desired retrograde dopant profile" (*id.* ¶ 9), but during heat treatment, "the initially retrograde profile in the vicinity of the surface of the semiconductor device . . . may have become substantially uniformly distributed" due to diffusion of the dopant atoms (*id.* ¶ 11).

Petitioner relies on Figures 1b and 2b (reproduced below), which Wieczorek uses to illustrate the prior art.

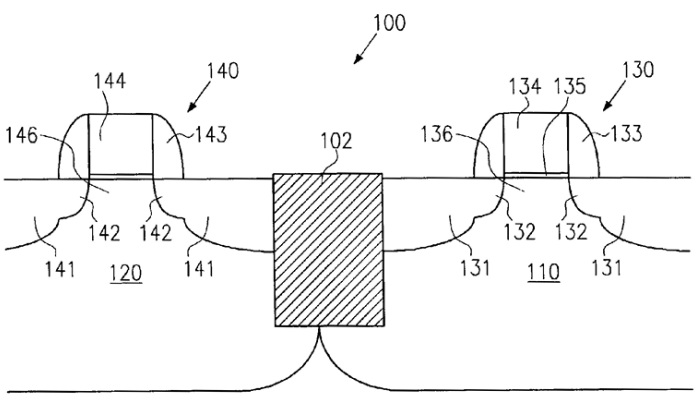

FIG.1b
(Prior Art)

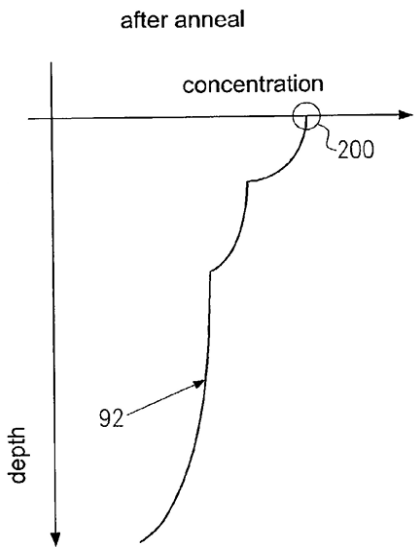

FIG.2b
(Prior Art)

Wieczorek Figure 1b shows a conventional semiconductor device at an intermediate manufacturing stage, including shallow trench isolation 102 separating N-well structure 120 from P-well structure 110. Ex. 1006 ¶¶ 7, 20. The device includes P-channel transistor 140 with source and drain

regions 141 in N-well structure 120 and N-channel transistor 130 with source and drain regions 131 in P-well structure 110. *Id.* ¶ 12. Wieczorek Figure 2b is a graph of dopant concentration versus depth of N-well structure 120 and P-well structure 110 and shows "a typical dopant profile with respect to the depth of the respective well structure" after ion implantation and heat treatment. *Id.* ¶¶ 9–11, 13, 21.

2. Wolf

Wolf is a four-volume textbook titled "Silicon Processing for the VLSI Era." Ex. 1008. A portion of the textbook focuses on CMOS technology. Ex. 1008A, 807–40.

3. Analysis

Petitioner argues that the combination of Wieczorek and would have taught or suggested the limitations of the challenged claims and that a person of ordinary skill in the art would have had reason to combine the teachings of Wieczorek and Wolf. Pet. 7, 52–90. On the present record, Patent Owner does not disagree. *See generally* Prelim. Resp.

a) Reason to Combine Wieczorek and Wolf

Petitioner argues that a person of ordinary skill in the art would have had a reason to combine the teachings of Wieczorek with those of Wolf. Pet. 52–53. On the present record, Patent Owner does not dispute this argument. *See generally* Prelim. Resp. Petitioner argues specifically that Wieczorek discloses "a conventional prior-art CMOS device" and that "Wolf is a well-known textbook that teaches known fundamental features and concepts related to semiconductor manufacturing, with particular emphasis on CMOS devices." Pet. 52–53. Wieczorek discloses "[a] typical process flow for forming the semiconductor device 100" which is "a

complementary MOS transistor pair." Ex. 1006 ¶ 12, Fig. 1b. Petitioner directs us to evidence that a person of ordinary skill in the art would have looked to Wolf for details on how to manufacture the conventional CMOS devices of Wieczorek. Ex. 1003 ¶ 142; Ex. 1008A, 807–40. Accordingly, Petitioner has shown sufficiently, for purposes of this decision, that a person of ordinary skill in the art would have had a reason to combine the teachings of Wieczorek with those of Wolf.

b) Claim 1

The preamble of claim 1 recites "[a] semiconductor device." Ex. 1001, 4:50. Petitioner argues that the combination of Wieczorek and Wolf teaches the preamble. Pet. 54. Wieczorek discloses a "semiconductor device." Ex. 1006 ¶ 12, Fig. 1b. At this stage of the proceeding, Petitioner has shown sufficiently that the combination of Wieczorek and Wolf teaches the preamble of claim 1.

Claim 1 recites "a substrate of a first doping type at a first doping level having first and second surfaces." Ex. 1001, 4:51–52. Petitioner argues that the combination of Wieczorek and Wolf teaches this limitation. Pet. 54–58. Wolf discloses that its twin-well CMOS devices "are formed . . . on a lightly doped substrate . . . of *n* or *p* material. Ex. 1008C, 530, Fig. 8-1(e). The substrates of Wieczorek and Wolf both have surfaces. Ex. 1006, Fig. 1b; Ex. 1008C, 525, Fig. 8-1(e). Relying on Dr. Banerjee's testimony, Petitioner contends that "a POSITA would have found it obvious to use a uniformly doped n- or p-type substrate ('a substrate of a first doping type at a first doping level') as a suitable substrate for Wieczorek's CMOS device in Figure 1b." Pet. 56 (citing Ex. 1003 ¶ 147). At this stage of the proceeding,

Petitioner has shown sufficiently that the combination of Wieczorek and Wolf teaches this limitation of claim 1.

Claim 1 recites "a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed." Ex. 1001, 4:53–56. Petitioner argues that the combination of Wieczorek and Wolf teaches this limitation. Pet. 58–61. Petitioner contends that, "[b]ecause the source-drain regions of the first active region are N-doped, Wieczorek-Wolf's first active region has a second doping type (N-type) opposite in conductivity to the first doping type (P-type) of the substrate." *Id.* at 60 (citing Ex. 1003 ¶ 151; Ex. 1006 ¶ 12). Wieczorek discloses "N-channel transistor 130" that includes "heavily N-doped source and drain regions 131" and "channel region 136." Ex. 1006 ¶ 12; *see id.* ¶ 4 (describing "field effect transistor[s]" generally as having the same parts). Wolf discloses that the source-drain and the channel region between those regions would have been considered part of an active region. Ex. 1008B, 299–300 ("The active regions are those in which transistor action occurs; i.e., the channel and the heavily doped source and drain regions."). At this stage of the proceeding, Petitioner has shown sufficiently that the combination of Wieczorek and Wolf teaches this limitation of claim 1.

Claim 1 recites "a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed." Ex. 1001, 4:57–59. Petitioner argues that the combination of Wieczorek and Wolf teaches this limitation. Pet. 61–62. Wieczorek discloses "P-channel transistor 140" that includes "heavily P-doped source and drain regions 141" and "channel region 146." Ex. 1006

¶¶ 4, 12. Wolf discloses that the source-drain and the channel region between those regions would have been considered part of an active region. Ex. 1008B, 299–300 ("The active regions are those in which transistor action occurs; i.e., the channel and the heavily doped source and drain regions."). This active region is separate from and disposed adjacent to the first active region. Ex. 1006, Fig. 1b. At this stage of the proceeding, Petitioner has shown sufficiently that the combination of Wieczorek and Wolf teaches this limitation of claim 1.

Claim 1 recites "transistors formed in at least one of the first active region or second active region." Ex. 1001, 4:60–61. Petitioner argues that the combination of Wieczorek and Wolf teaches this limitation. Pet. 63. Wieczorek discloses forming transistors N-channel and P-channel transistors, each in an active region, as discussed above. Ex. 1006 ¶¶ 12–13, Fig. 1b. Petitioner notes that the disclosure of Wieczorek and Wolf satisfies claim 1's recitation of "transistors" either under Patent Owner's district court construction of "transistors" as requiring one or more transistors or under an alternative construction requiring multiple transistors in each active region. Pet. 60 ("a POSITA would have understood that Wieczorek teaches forming multiple nMOS transistors in the first active region to minimize chip area, as good layout practice dictates"), 62 ("a POSITA would have understood that Wieczorek teaches forming multiple pMOS transistors in the second active region"), 84 (citing Ex. 1003 ¶¶ 148, 153; Ex. 1006 ¶ 4; Ex. 1014, 1:52–54, 2:17–21; Ex. 1020, 31).

Claim 1 recites "at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the

substrate." Ex. 1001, 4:62–65. Petitioner argues that the combination of Wieczorek and Wolf teaches this limitation. Pet. 63–67. The channel region of Wieczorek's transistors exhibits graded dopant concentration, with the concentration decreasing with increasing depth away from the surface. Ex. 1006 ¶¶ 11, 13, Figs. 1b, 2b. Petitioner directs us to evidence that tends to show that these depthwise variations in impurity concentrations help to move carriers down into the substrate, away from the top surface and toward the bottom surface. Ex. 1003 ¶¶ 161–162; Ex. 1010, 2:27–32, 5:14–22, Figs. 1a, 1b. At this stage of the proceeding, Petitioner has shown sufficiently that the combination of Wieczorek and Wolf teaches this limitation of claim 1.

Claim 1 recites "at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the first surface to the second surface of the substrate." Ex. 1001, 4:66–5:3. Petitioner argues that the combination of Wieczorek and Wolf teaches this limitation. Pet. 67–68. Wieczorek's P-well exhibits gradually decreasing dopant concentration with increasing depth away from the surface. Ex. 1006 ¶¶ 9, 11, 13, Figs. 1b, 2b. Petitioner directs us to evidence that tends to show that these depthwise variations in impurity concentrations help to move carriers down into the substrate, away from the top surface and toward the bottom surface. Ex. 1003 ¶¶ 95, 165; Ex. 1010, 2:27–32, 5:14–22, Figs. 1a, 1b; Ex. 1016, 289–90. At this stage of the proceeding, Petitioner has shown sufficiently that the combination of Wieczorek and Wolf teaches this limitation of claim 1.

c) Remaining Claims

In view of our determination that Petitioner establishes a reasonable likelihood for claim 1, and because Petitioner's arguments and evidence for remaining claims 2, 4–9, 12–22, 24–27, 30–36 (Pet. 69–83) are similar to Petitioner's arguments and evidence for claim 1 (*id.* at 54–68, 84–90) and are unopposed at this stage by Patent Owner, we determine that it is unnecessary to provide an explicit analysis of Petitioner's challenges to the remaining claims in order to provide guidance to the parties for the upcoming trial. CTPG at 64; 37 C.F.R. § 42.108(a); *SAS*, 138 S. Ct. at 1359–60.

III. CONCLUSION

Upon consideration of the Petition, the Preliminary Response, the Preliminary Reply, the Preliminary Sur-Reply, and the evidence presented, we determine that Petitioner has shown a reasonable likelihood that it will prevail in showing that at least one of the challenged claims is unpatentable. In addition, we are persuaded on the present record that the Petition is not time-barred under 35 U.S.C. § 315(b). Accordingly, we institute an *inter partes* review of all challenged claims based on the grounds asserted in the Petition.

IV. ORDER

For the reasons given, it is:

ORDERED that an *inter partes* review is instituted with respect to the challenged claims and each of the grounds asserted in the Petition;

FURTHER ORDERED that, pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial, which shall commence on the entry date of this Decision;

FURTHER ORDERED that, in view of the pending motion to seal, this Decision is being filed "Board and Parties Only"; and

FURTHER ORDERED that after conferring with Petitioner, Patent Owner shall, within one week of this Decision, submit to the Board via email to Trials@uspto.gov, a version of this Decision to be filed on the public record, with any redactions proposed by either party.

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