IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

CIRRUS LOGIC, INC.;
OMNIVISION TECHNOLOGIES, INC.; AND
TEXAS INSTRUMENTS INCORPORATED,
Petitioner,

v.

GREENTHREAD, LLC,
Patent Owner.

Case No. IPR2024-00017[1]
Patent No. 8,421,195

PETITIONER'S UPDATED EXHIBIT LIST

[1] Texas Instruments Incorporated, which filed a petition in IPR2024-00771, has been joined as a party to this proceeding.

UPDATED TABLE OF EXHIBITS

Exhibit	Description
1001	U.S. Patent No. 8,421,195 to Rao (the "'195 Patent")
1002	Prosecution History of the '195 Patent ("the Prosecution History")
1003	Declaration of Sanjay Banerjee, PhD
1004	Curriculum Vitae of Sanjay Banerjee, PhD
1005	U.S. Patent No. 4,684,971 ("Payne")
1006	U.S. Patent No. 4,907,058 to Sakai ("Sakai")
1007	U.S. Patent No. 6,043,114 to Kawagoe, et al., ("Kawagoe")
1008A	Wolf and Tauber, *Silicon Processing For The VLSI Era,* Vol 1, Lattice Press (2000) ("Wolf.1")
1008B	Wolf and Tauber, *Silicon Processing For The VLSI Era,* Vol. 2, Lattice Press (2000) ("Wolf.2")
1008C	Wolf and Tauber, *Silicon Processing For The VLSI Era,* Vol. 3, Lattice Press (2000) ("Wolf.3")
1008D	Wolf and Tauber, *Silicon Processing For The VLSI Era,* Vol. 4, Lattice Press (2000) ("Wolf.4")
1009	U.S. Patent No. 4,160,985 ("Kamins")
1010	U.S. Patent No. 4,481,522 ("Jastrzebski")
1011	U.S. Patent Application Publication No. 2003/0042511 ("Rhodes")
1012	U.S. Patent Application Publication No. 2002/0102783 ("Fujimoto")
1013	Wang and Agrawal, *Single Event Upset: An Embedded Tutorial*, 21st Intl Conf on VLSI Design, IEEE 2008 ("Wang")
1014	Publication Declaration of Alyssa G. Resnick for Wolf.1 and Wolf.2 ("Resnick Decl.")
1015	Publication Declaration of Rachel J. Watters for Wolf.3 and Wolf.4 ("Watters Decl.")
1016	IPR2020-00289, Patent Owner Preliminary Response
1017	U.S. Pat. No. 11,121,222 (the "'222 Patent")
1018	U.S. Pat. No. 11,316,014 (the "'014 Patent")
1019	Civil Action No. 2:19-cv-00147-JRG, Dkt. 67 (E.D. Tex. Apr. 20, 2019)
1020	Prosecution History of U.S. Pat. No. 11,121,222
1021	Prosecution History of U.S. Pat. No. 11,316,014

Exhibit	Description
1022	U.S. Patent Application Publication No. 2004/0063288 ("Kenney")
1023	Jaeger, *Introduction to Microelectronic Fabrication*, Vol. V, Addison-Wesley Modular Series on Solid State Devices (1988) ("Jaeger")
1024	U.S. District Courts – Case Statistics, obtained at https://www.uscourts.gov/statistics-reports/analysis-reports/ federal-court-management-statistics, dated June 30, 2023
1025	U.S. Patent No. 4,435,896 ("Parrillo")
1026	L.C. Parrillo, R.S. Payne et al., *Twin-Tub CMOS - A Technology for VLSI Circuits*, IEEE 1980 ("Parrillo2")
1027	U.S. Patent Application Publication No. 2007/0045682 to Hong *et al*. ("Hong")
1028	The Oxford American Dictionary and Language Guide, Oxford University Press (1996)
1029	Blank
1030	Patent Owner's Responsive Claim Construction Brief
1031	Blank
1032	Patent Owner's Sur-Reply Claim Construction Brief
1033	Proposed Claim Constructions in the District Court Case
1034	Redacted District Court Case Transfer Order
1035	Civil Action No. 2:19-cv-00147-JRG, Dkt. 105 (E.D. Tex. Jul. 9, 2020)
1036	Publication Declaration of Sylvia Hall-Ellis for Wolf
1037	Dec. 21, 2022 Preliminary Claim Constructions in 6:22-CV-00105
1038	U.S. Patent Application Publication No. 2003/0183856 to Wieczorek ("Wieczorek")
1039	Parrillo IEEE Citation List
1040	Dictionary of Scientific and Technical Terms, McGraw Hill (2003)
1041	Rubin et al., *Ranges and Moments of Depth Distributions of Boron and Phosphorus Implanted into Silicon in the Energy Range 1.7 -5.0 MeV with an Eaton NV-GSD/VHE Implanter*, IEEE 1997 ("Rubin")
1042	Certified translation of Japanese Unexamined Patent Application Publication No. H8-279598 ("Onoda")

Exhibit	Description
1043	Japanese Unexamined Patent Application Publication No. H8-279598, published on October 22, 1996
1044	IPR2020-289, Termination Order
1045	Oct. 31, 2022 Giapis Declaration, 6:22-CV-00105
1046	Email dated December 22, 2023
1047	Blank
1048	Blank
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1057	Blank
1058	Blank
1059	Blank
1060	Supplemental Declaration of Sanjay Banerjee, PhD
1061	Sze, Semiconductor Devices: Physics and Technology, Second Edition 1985, excerpted ("Sze")
1062	Streetman and Banerjee, Solid State Electronic Devices, Sixth Edition 2006, excerpted ("Streetman")
1063	Deposition Transcript of Alexander Glew, Ph.D., P.E., taken on Oct. 16, 2024
1064	Declaration of Douglas Holberg in Application No. 17/728,588 (Aug. 1, 2024)
1065	R. C. Baumann, *Soft Errors in Commercial Integrated Circuits*, 14(2) Int'l J. High Speed Elect. & Sys. 299-399 (2004)
1066	Confidential Deposition Transcript of Mohan Rao, Ph.D., taken on Oct. 23, 2024
1067	RPX Rational Patent FAQs
1068	A. S. Grove, *Physics and Technology of Semiconductor Devices*, excerpted (1067)
1069	Deposition Transcript of Alexander Glew, Ph.D., P.E., taken on July 16, 2024
1070	Amendment and Response to Office Action in Application No. 17/728,588 (Aug. 1, 2024)

Exhibit	Description
1071	Wolf Vol. 2 Supplement
1072	Petitioner's Hearing Demonstratives
1073	Telephonic Conference Call Transcript, taken on May 2, 2025 (Confidential)
1074	Telephonic Conference Call Transcript, taken on May 2, 2025 (Redacted – Public Version)
1075	Declaration of Hyun S. Byun in Support of Petitioner's Notice of Intent to Designate Hyun S. Byun as Back-up Counsel under 37 C.F.R. § 42.10

Respectfully submitted,

Dated: September 3, 2025

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CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6, I hereby certify that the foregoing Updated Exhibit List, were served on the Patent Owner by electronic mail to the following counsel of record for Patent Owner:

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