

PUBLIC VERSION

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

CIRRUS LOGIC, INC. and OMNIVISION TECHNOLOGIES, INC.
Petitioner,

v.

GREENTHREAD, LLC,
Patent Owner.

IPR2024-00019
Patent 11,316,014 B2

Before JON B. TORNQUIST, MONICA S. ULLAGADDI, and
JULIA HEANEY, *Administrative Patent Judges*.

TORNQUIST, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Cirrus Logic, Inc., OmniVision Technologies, Inc., and ams Sensors USA, Inc.¹ (collectively “Petitioner”) filed a Petition requesting *inter partes* review of claims 1–9 and 12–28 of U.S. Patent No. 11,316,014 B2 (Ex. 1001, “the ’014 patent”). Paper 1 (“Pet.”). Greenthread, LLC (“Patent Owner”) filed a Preliminary Response to the Petition. Paper 16 (“Prelim. Resp.”). With authorization, Petitioner subsequently filed a Preliminary Reply (Paper 19, “Prelim. Reply”) and Patent Owner filed a Preliminary Sur-reply (Paper 21, “Prelim. Sur-reply”).

An *inter partes* review may not be instituted “unless . . . the information presented in the petition . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a) (2018). Having considered the arguments and evidence set forth by Petitioner and Patent Owner, we determine that the information presented in the Petition demonstrates a reasonable likelihood that Petitioner would prevail on at least one of the challenged claims of the ’014 patent. Accordingly, we institute an *inter partes* review as to all of the challenged claims of the ’014 patent on all of the grounds of unpatentability set forth in the Petition.

¹ After the Petition was filed, original Petitioner ams Sensors USA Inc. merged into ams-OSRAM USA Inc. Paper 23 (Petitioner’s Updated Mandatory Notices). On April 10, 2024, the parties filed a Joint Motion to Terminate the Proceedings as to ams-OSRAM Inc. (Paper 25), which was granted (Paper 27). The caption of this proceeding has been updated accordingly.

II. BACKGROUND

A. Related Matters

The parties indicate that the '014 patent is at issue in the following proceedings:

Greenthread, LLC v. Cirrus Logic, Inc., No. 1:23-cv-00369 (W.D. Tex. filed March 31, 2023);

Greenthread, LLC v. Texas Instruments Inc., No. 2:23-cv-00157 (E.D. Tex. filed April 6, 2023);

Greenthread, LLC v. OSRAM GmbH, No. 2:23-cv-00179 (E.D. Tex. filed April 19, 2023);

Greenthread, LLC v. OmniVision Technologies, Inc., No. 2:23-cv-00212 (E.D. Tex. filed May 10, 2023); and

Greenthread, LLC v. Monolithic Power Systems, Inc., No. 1:23-cv-00579 (D. Del. filed May 26, 2023).

Paper 6, 2–3 (Patent Owner's mandatory notices); Pet. 1–2.

B. Real Parties-in-Interest

Petitioner identifies itself (the two parties identified in the caption), ams-OSRAM USA Inc., OSRAM GmbH, Heptagon Holding CA Inc., ams-OSRAM AG, and GlobalFoundries, U.S., Inc., as the real parties-in-interest. Pet. 1; Paper 23, 1 (Updated Mandatory Notices). Patent Owner identifies itself as the real party-in-interest. Paper 6, 1.

C. The '014 patent

The '014 patent, titled “Semiconductor Devices with Graded Dopant Regions,” issued on April 26, 2022. Ex. 1001, codes (45), (54). The '014 patent “relates to all semiconductor devices and systems,” including Bipolar Junction Transistors (BJT). *Id.* at 1:39–52.

The '014 patent explains that in bipolar junction transistors, minority carriers are the principal device conduction mechanism, but majority carriers also play a small but finite role in modulating the conductivity in such devices. *Id.* at 1:50–54. The '014 patent further explains that “[e]fforts have been made in graded base transistors to create an aiding drift field to enhance the diffusing minority carrier’s speed from emitter to collector” versus the standard “uniformly doped base” bipolar junction transistors. *Id.* at 1:62–64. The '014 patent explains that this improvement has not been implemented in most semiconductor devices, including various power MOSFETs and IGBTs, which “still use a uniformly doped ‘drift epitaxial’ region in the base.” *Id.* at 1:64–2:2. The '014 patent implements a graded dopant concentration in these devices, which results in at least two important performance enhancements: “electrons can be swept from source to drain rapidly, while at the same time holes can be recombined closer to the n+ buffer layer,” thereby improving “ t_{on} and t_{off} in the same device.” *Id.* at 3:42–47.

Figure 1 of the '014 patent is reproduced below.

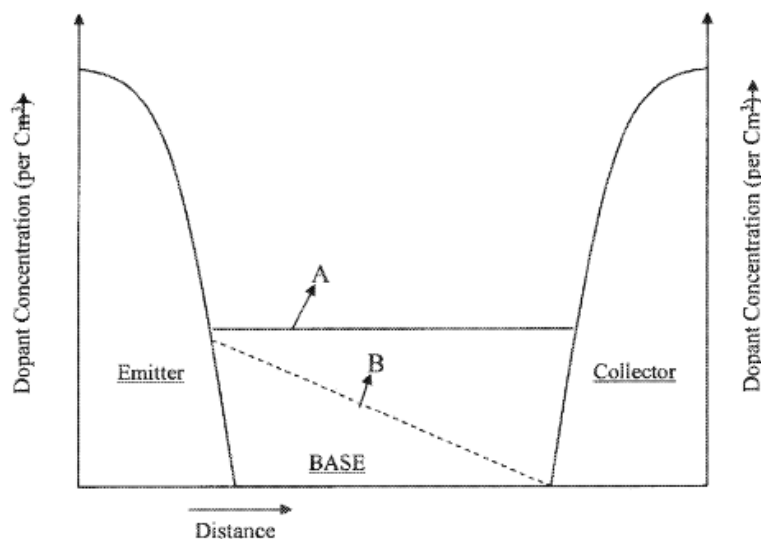


Figure 1 is labeled “Prior Art” and “illustrates the relative doping profiles of emitter, base and collector for the two most popular bipolar junction transistors: namely, uniform base (“A”) and graded base (“B”).” *Id.* at 2:40–43, Fig. 1.

Figure 3A of the '014 patent is reproduced below.

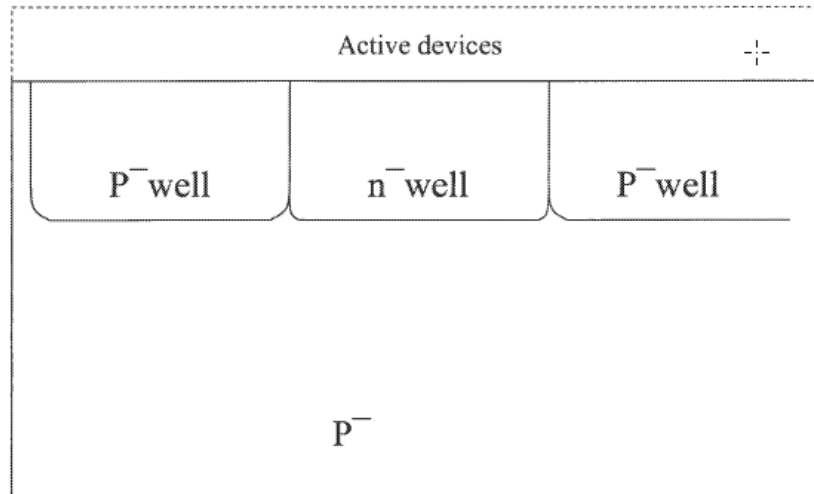


Figure 3A is labeled “Prior art” and shows a cross section of “a typical prior art IC with two wells (one n- well in which p-channel transistors are subsequently fabricated and one p- well in which n-channel transistors are subsequently fabricated).” Ex. 1001, 2:46–51, Fig. 3A.

Figure 5A of the '014 patent is reproduced below.

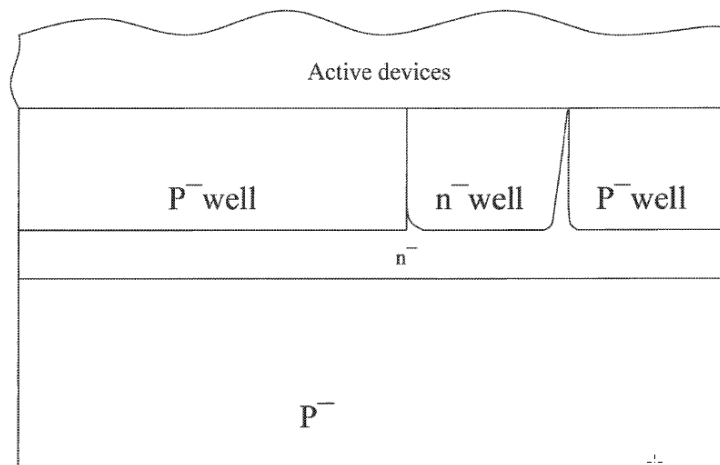


Figure 5A illustrates a cross section of a CMOS silicon substrate with two wells and an underlying layer using embodiments of the invention. *Id.* at 2:58–61. According to the '014 patent, “[s]purious minority carriers can be generated by clock switching in digital VLSI logic and memory ICs.” Ex. 1001, 3:48–52. The '014 patent states that these “unwanted carriers can discharge dynamically-held ‘actively held high’ nodes,” and serve to degrade performance of various types of devices, including digital imaging ICs. *Id.* at 3:51–59. According to the '014 patent, “a novel technique is described” in which “a drift field [is used] to sweep these unwanted minority carriers from the active circuitry at the surface into the substrate in a monolithic die as quickly as possible.” *Id.* at 3:64–4:1. For example, “[i]n a preferred embodiment, the subterranean n^- layer has a graded donor concentration to sweep the minority carriers deep into the substrate.” *Id.* at 4:1–3.

D. Illustrative Claim

Claims 1 and 21 are independent, with challenged claims 2–9 and 12–20 depending from claim 1 and challenged claims 22–28 depending from claim 21. Ex. 1001, 4:49–6:56. Claim 1 is representative of the challenged claims and is reproduced below.

1. An electronic system, the system comprising:

at least one semiconductor device, the at least one semiconductor device including:

a substrate of a first doping type at a first doping level having a surface;

a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;

a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;

transistors formed in at least one of the first active region or second active region;

at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions; and

at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions, wherein at least some of the transistors form digital logic of the semiconductor device.

Ex. 1001, 4:49–5:7 (spacing added to aid readability).

E. Asserted Grounds of Unpatentability

Petitioner asserts the following grounds of unpatentability (Pet. 6–7):²

Claims Challenged	35 U.S.C. §	Reference(s)/Basis
1–9, 12–14, 16–21, 23–28	103(a)	Kawagoe ³

² The Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112–29, took effect on March 16, 2013. The ’014 patent claims priority to an application filed September 3, 2004. Ex. 1001, code (60). Thus, we apply the pre-AIA version of §103. See Pet. 5 n.1.

³ US 6,043,114, issued Mar. 28, 2000 (Ex. 1007).

Claims Challenged	35 U.S.C. §	Reference(s)/Basis
1–2, 4–9, 12–23, 25–28	103(a)	Wieczorek ⁴ , Wolf ⁵
1–9, 12–14, 16–21, 23–28	103(a)	Kawagoe, Gupta ⁶
1–2, 4–9, 12–23, 25–28	103(a)	Wieczorek, Wolf, Gupta
19	103(a)	Kawagoe, Silverbrook ⁷
19	103(a)	Wieczorek, Wolf, Silverbrook

Petitioner also relies upon the declaration testimony of Dr. Sanjay Banerjee, Ph.D. Ex. 1003.

III. ANALYSIS

A. Legal Standard

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and “the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) when in evidence, objective

⁴ US 2003/0183856 A1, published Oct. 2, 2003 (Ex. 1006).

⁵ Stanley Wolf & Richard N. Tauber, *Silicon Processing for the VLSI Era*, Vols. 1–4 (Lattice Press 2000) (Ex. 1008).

⁶ US 6,163,877, issued Dec. 19, 2000 (Ex. 1014).

⁷ US 6,614,560 B1, issued Sept. 2, 2003 (Ex. 1046).

evidence of nonobviousness. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

B. Level of Ordinary Skill in the Art

In order to determine whether an invention would have been obvious at the time the application was filed, we consider the level of ordinary skill in the pertinent art. *Graham*, 383 U.S. at 17. In assessing the level of ordinary skill in the art, various factors may be considered, including the “type of problems encountered in the art; prior art solutions to those problems; rapidity with which innovations are made; sophistication of the technology; and educational level of active workers in the field.” *In re GPAC, Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995) (quotation omitted).

Petitioner contends that one of ordinary skill in the art would have had “a Bachelor’s degree in electrical engineering, material science, applied physics, or a related field, and four years of experience in semiconductor design and manufacturing or equivalent work experience.” Pet. 7 (citing Ex. 1003 ¶ 45). Petitioner further contends that “[a]dditional education might compensate for a deficiency in experience, and vice-versa.” *Id.*

Although Patent Owner does not address the level of ordinary skill in the art, Patent Owner agreed with Petitioner’s characterization of the ordinarily skilled artisan during a previous litigation, as Petitioner points out. *See generally*, Prelim. Resp. 1–37; Pet. 7 (citing Ex. 1045 ¶ 13).

On this record, we adopt Petitioner’s definition of the person of ordinary skill in the art as it appears consistent with the prior art of record. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001) (holding

that the prior art itself can reflect the appropriate level of ordinary skill in the art).

C. Claim Construction

In an *inter partes* review proceeding, a patent claim is construed using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. § 282(b). 37 C.F.R. § 42.100(b) (as amended Oct. 11, 2018). This rule adopts the same claim construction standard used by Article III federal courts, which follow *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc), and its progeny. Under this standard, the words of a claim are generally given their “ordinary and customary meaning,” which is the meaning the term would have to a person of ordinary skill at the time of the invention, in the context of the entire patent including the specification. *See Phillips*, 415 F.3d at 1312–13.

Petitioner contends that no claims terms require express construction to resolve the issues presented in the Petition. Pet. 8–9.

Patent Owner does not assert that any claim terms require express construction. *See generally*, Prelim. Resp.

Upon review of the record, we determine that no claim terms require express construction for purposes of this Decision. *See Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) (“The Board is required to construe ‘only those terms . . . that are in controversy, and only to the extent necessary to resolve the controversy.’”) (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)).

D. Timeliness of the Petition Under 35 U.S.C. § 315(b)

Pursuant to 35 U.S.C. § 315(b), “[a]n *inter partes* review may not be instituted if the petition requesting the proceeding is filed more than 1 year

after the date on which the petitioner, real party in interest, or privy of the petitioner is served with a complaint alleging infringement of the patent.”

Patent Owner argues that the Petition should be dismissed because it is untimely. Prelim. Resp. 2. In particular, Patent Owner argues that Petitioner is in privity with [REDACTED] Intel Corp.

(“Intel”), [REDACTED], who

Patent Owner asserts are time-barred under 35 U.S.C. § 315(b) and [REDACTED]

[REDACTED] *Id.* at 2–3 (citing *Applications in Internet Time, LLC v. RPX Corp.*, 897 F.3d 1336, 1360 (Fed. Cir. 2018)).

Patent Owner advances several theories supporting its privity arguments, including that [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED] for custom-made products. *Id.*

1. *Legal Standard*

Patent Owner does not assert that Petitioner was a party to, or named as a real party-in-interest in, any prior lawsuit involving the ’014 patent. “A person who is not a party to a suit generally has not had a ‘full and fair opportunity to litigate’ the claims and issues settled in that suit.” *Taylor v. Sturgell*, 553 U.S. 880, 892 (2008). Thus, in general, Petitioner should not be precluded from addressing the unpatentability of a patent based on the filing of [REDACTED] Intel, [REDACTED] [REDACTED]. *See id.* (noting that, in general, one is not bound by a judgment “in which he is not designated as a party or to which he has not been made a party by service of process”); *WesternGeco LLC v. ION Geophysical Corp.*,

889 F.3d 1308, 1319 (Fed. Cir. 2018) (noting the “general rule against nonparty preclusion”). This rule is deeply-rooted in the “historic tradition that everyone should have his own day in court.” *Taylor*, 553 U.S. at 892–93 (quoting *Richards v. Jefferson County*, 517 U.S. 793, 798 (1996)).

An exception to this deeply-rooted rule exists for parties that are in privity with a defendant in an earlier litigation. *See WesternGeco*, 889 F.3d at 1319 (noting that “the standards for the privity inquiry must be grounded in due process”). The Supreme Court in *Taylor* identified considerations where nonparty preclusion would be justified, including:

- (1) an agreement to be bound; (2) pre-existing substantive legal relationships between the person to be bound and a party to the judgment (e.g., “preceding and succeeding owners of property”); (3) adequate representation by someone with the same interests who was a party (e.g., “class actions” and “suits brought by trustees, guardians, and other fiduciaries”); (4) assumption of control over the litigation in which the judgment was rendered; (5) where the nonparty to an earlier litigation acts as a proxy for the named party to relitigate the same issues; and (6) a special statutory scheme expressly foreclosing successive litigation by nonlitigants.

Id. (citing *Taylor*, 553 U.S. at 894–95).

As this list of considerations indicates, “the mere existence of some relationship between a petitioner and another entity is not sufficient” to place that petitioner in privity with that entity. *Google LLC v. DDC Technology, LLC*, IPR2023-00707, Paper 27 at 37 (PTAB Oct. 25, 2023). Instead, “that relationship must be related to [an earlier] lawsuit and be sufficiently close that it can be fairly said the petitioner had a full and fair opportunity to litigate the validity of the patent in that lawsuit,” or the evidence must demonstrate “that petitioner is simply serving as a proxy to allow another party to litigate the patent validity question that the other party raised in an

earlier filed litigation.” *Id.*; *WesternGeco*, 889 F.3d at 1319; *see also Ventex Co. v. Columbia Sportswear North America, Inc.*, IPR2017-00651, Paper 148, at 10, 12 (PTAB Jan. 24, 2019) (precedential) (finding privity where the two parties “had a specially structured, preexisting, and well established business relationship with one another, including indemnification and exclusivity arrangements”).

A petitioner’s “initial identification of the real parties in interest [and privies] should be accepted unless and until disputed by a patent owner.” *Worlds Inc. v. Bungie, Inc.*, 903 F.3d 1237, 1244 (Fed. Cir. 2018). In order to raise such a dispute, “a patent owner must produce *some* evidence that tends to show that a particular [time-barred] third party should be named a [privity].” *Id.* The amount of evidence a patent owner must produce does not rise to the level of that required to overcome a burden of production. *Id.* at 1244 n.8. One potential formulation of the amount of evidence required is “evidence that ‘reasonably brings into question the accuracy of a petitioner’s’” assertion that it is not time-barred. *Id.* (quoting *Atlanta Gas Light v. Bennett Regulator Guards, Inc.*, IPR2013-00453, Paper 88 (PTAB Jan. 6, 2015) (addressing the amount of evidence required from a patent owner to question a petitioner’s identification of the real parties-in-interest)). Although the “burden remains with the petitioner to establish” the timeliness of its petition, it need not respond until the patent owner reasonably brings into question the accuracy of its assertion that it is not time-barred. *Id.* at 1242.

2. *Whether we May Consider Petitioner’s Preliminary Reply*

As noted above, we authorized Petitioner to file a Preliminary Reply and Patent Owner to file a Preliminary Sur-reply, both limited to addressing

the issue of the timeliness of the Petition. Patent Owner argues that Petitioner's Preliminary Reply is not appropriate because Petitioner "could have reasonably foreseen" Patent Owner's untimeliness arguments when filing its petition and because Patent Owner informed Petitioner about these arguments before it filed petitions challenging related patents. Prelim. Resp. 2, 34–36 (quoting *Sandoz Inc. v. Abbvie Biotechnology Ltd.*, IPR2018-00002, Paper 11 at 3 (PTAB Mar. 6, 2018); citing Ex. 2011).

We disagree with Patent Owner's argument. According to the Federal Circuit, a petitioner's "initial identification of the real parties in interest [and privies] should be accepted unless and until disputed by a patent owner." *Worlds*, 903 F.3d at 1244. Thus, there is no requirement that a petitioner preemptively address a disputed issue of privity in its petition. Although Patent Owner generally made Petitioner aware that it might raise a timeliness issue under § 315(b) (Ex. 2011), Petitioner is not required to address potential arguments that Patent Owner may, but has not yet made, in its Preliminary Response. This is especially true where Patent Owner's assertions of privity, for the reasons set forth below, are not sufficient to reasonably call into question Petitioner's assertion that the Petition is timely.

Accordingly, we consider Petitioner's Preliminary Reply, as well as Patent Owner's Preliminary Sur-Reply, in determining whether Petitioner has shown its Petition is timely.

3. *The Effect of the Earlier Suits [REDACTED] on the Timeliness of the Present Petition*

Patent Owner alleges that [REDACTED] Intel, [REDACTED] are time-barred under § 315(b). Prelim. Resp. 2–3. As to [REDACTED], the present record does not contain any evidence tending to show that this is the case.

Section 315(b) bars institution of *inter partes* review only when “the petition requesting the proceeding is filed more than 1 year after the date on which the petitioner, real party in interest, or privy of the petitioner is served with a complaint alleging infringement of the patent.” On this record, there is no evidence that [REDACTED] was ever served with a complaint alleging infringement of the ’014 patent. Prelim. Resp. 3–4 (asserting that Patent Owner filed a complaint against [REDACTED] with respect to patents other than the ’014 patent). Thus, on the present record, there is insufficient evidence to suggest that [REDACTED].

There is also no evidence, on the present record, that [REDACTED] any earlier than January 23, 2023, which is less than one year before the filing of the Petition on October 27, 2023. *Compare* Pet. 91, with Ex. 2009 (cited at Prelim. Resp. 5). Accordingly, the service of [REDACTED] time-barred under § 315(b).

Patent Owner argues that, because [REDACTED] [REDACTED] were served with an infringement complaint early enough to create a time bar, and because [REDACTED] [REDACTED] is time-barred under § 315(b). Prelim. Resp. 4–5, 17 (arguing that [REDACTED] [REDACTED]). We are presented with no authority, however, for extending the time bar of Section 315(b) to a party [REDACTED] that was a real party-in-interest to a potentially time barred party [REDACTED]. Thus, Patent Owner has produced no evidence that [REDACTED] is a time-barred entity under § 315(b).

4. [REDACTED] Intel, [REDACTED]

In the subsections below, we address Patent Owner’s arguments that [REDACTED] Intel, [REDACTED] of Petitioner and Petitioner’s real party-in-interest, GlobalFoundries⁸, under § 315(b).

a. *Agency*

Patent Owner argues that “[b]y making custom [REDACTED] [REDACTED], Petitioners step into their shoes, and serve[] as their ‘agent,’ by [REDACTED]. Prelim. Resp. 3, 23–26. We disagree.

First, Patent Owner’s agency argument is not based on the applicable legal standard. For purposes of privity under § 315(b), the relevant question is whether Petitioner is acting as an agent for [REDACTED] Intel [REDACTED] in filing a petition for *inter partes* review. *See Taylor*, 553 U.S. at 895 (“preclusion is appropriate when a nonparty later brings suit as an agent for a party who is bound by a judgment.”). As the Federal Circuit explains, the rationale behind § 315(b)’s time bar is “to prevent successive challenges to a patent by those who previously have had the opportunity to make such challenges in prior litigation.” *WesternGeco*, 889 F.3d at 1319. Here, Patent Owner does not assert that Petitioner is acting as an agent for [REDACTED] Intel, [REDACTED] in this proceeding. Any such assertion would be appropriate only based on evidence suggesting that [REDACTED] Intel, is controlling Petitioner’s conduct in the proceeding. *See Taylor*, 553 U.S. at 906 (cautioning that “preclusion is appropriate only if the

⁸ Petitioner identifies GlobalFoundries U.S., Inc. (“GlobalFoundries”) as a real party-in-interest. Pet. 1.

putative agent's conduct of the suit is subject to the control of the party who is bound by the prior adjudication"). No such evidence is in this record.

Patent Owner argues that to be in [REDACTED], "what matters is not the scope or nature of the agency, but whether "the prior action concerned a matter within the agency." Prelim. Resp. 26 (citing *Herrion v. Children's Hosp. Nat. Med. Ctr.*, 786 F. Supp. 2d 359 (D.D.C.), *aff'd*, 448 F. App'x 71 (D.C. Cir. 2011); *John Street Leasehold, LLC v. Cap. Mgmt. Res., L.P.*, 283 F.3d 73 (2d Cir. 2002); *Fiumara v. Fireman's Fund Ins. Companies*, 746 F.2d 87 (1st Cir. 1984)). This conclusion, however, would significantly expand the analysis set forth in *Taylor*, which noted that preclusion is only appropriate if the putative agent's conduct "is subject to the control of the party who is bound by the prior adjudication." *Taylor*, 553 U.S. at 906 (explaining that "courts should be cautious about finding preclusion" on the basis of agency). Moreover, the privity inquiry must take into account the rationale behind § 315(b)'s preclusion provision, which "is to prevent successive challenges to a patent by those who previously have had the opportunity to make such challenges in prior litigation." *WesternGeco*, 889 F.3d at 1319. Patent Owner's broad interpretation would be inconsistent with this purpose.

Even if Patent Owner's argument that a general agency relationship is sufficient to demonstrate privity for purposes of nonparty preclusion were on solid legal footing, it lacks factual support in the record. An "essential element[] of agency" is "the principal's 'right to direct or control the agent's actions.'" *In re Google LLC*, 949 F.3d 1338, 1345 (Fed. Cir. 2022) (quoting *Meyer v. Holley*, 537 U.S. 280, 286 (2003)). Patent Owner does not argue in the Preliminary Response that [REDACTED] Intel, [REDACTED] [REDACTED], much less direct us to any

evidence that would tend to prove the existence of such a right. Prelim. Resp. 23–26.

Patent Owner argues that GlobalFoundries “produc[es] ICs for other companies, rather than those of its own design,” and that Cirrus Logic makes “custom” products. *Id.* at 25 (citing Ex. 2033, 12, 35); *see In re Google*, 949 F.3d at 1346 (contracts to “[a]ssembl[e] equipment based on information and instructions provided by Google” were “suggestive of an agency relationship;” first alteration in original). Patent Owner does not allege, however, that any particular product [REDACTED] Intel, [REDACTED] Intel, [REDACTED] Intel, [REDACTED] with respect to the patented technology. Prelim. Resp. 26–28. Thus, Patent Owner does not direct us to any evidence that Petitioner [REDACTED] Intel’s [REDACTED] Intel.

b. Preceding and Succeeding Owners of Property

Patent Owner argues that [REDACTED] Intel, [REDACTED]
[REDACTED]

Prelim. Resp. 3, 26–29 (citing *Taylor*, 553 U.S. at 894). It is true that entities who are “preceding and succeeding owners of property” can be in privity with one another. *Taylor*, 553 U.S. at 894. This rule, however, is based on property law and “is extended or denied in an effort to protect conflicting property interests rather than an effort to implement concepts of participation or representation.” 18A C. Wright, A. Miller, & E. Cooper, Federal Practice and Procedure § 4448 (3d. ed. 2023); *see also id.* at § 4462 (“Successive Property Relationships”) (“There is no independent reason to treat the defeated litigant as the representative of his transferee. Preclusion

is limited to the property involved in the judgment.”). As noted above, our relevant analysis is based on the relationships between the parties with respect to the prior proceeding or the Petition (e.g., participation or representation), not on property interests. *See WesternGeco*, 889 F.3d at 1319 (noting that the privity requirement is used “to prevent successive challenges to a patent by those who previously have had the opportunity to make such challenges in prior litigation”).

Moreover, the rule related to preceding and succeeding owners of property does not extend to the point where all manufacturers of allegedly infringing goods are in privity with the customers who buy those goods. *See, e.g., WesternGeco*, 889 F.3d at 1319–22 (the parties “had a contractual and fairly standard customer-manufacturer relationship regarding the accused product,” which “does not necessarily suggest that the relationship is sufficiently close that both” parties should be considered to be in privity); *Wi-Fi One, LLC v. Broadcom Corp.*, 887 F.3d 1329, 1340–41 (Fed. Cir. 2018) (same); *Samsung Electronics Co. Ltd. v. Netlist Inc.*, IPR2022-00615, Paper 64 at 22–26 (PTAB June 30, 2023) (same).

Patent Owner alleges that [REDACTED]

[REDACTED] Prelim. Resp. 26–27. For example, Patent Owner asserts that Cirrus Logic chips are [REDACTED]

[REDACTED] *Id.* at 7–8.

Patent Owner makes a similar assertion regarding OmniVision chips. *Id.* at 11–13. Patent Owner also asserts that [REDACTED] Intel, [REDACTED] [REDACTED] (*id.* at 12–13), but has not made any

⁹ See Section I.B. (Related Matters).

infringement allegation against GlobalFoundries and has not identified any accused product or component made by GlobalFoundries. Thus, Patent Owner does not direct us to any evidence that [REDACTED] Intel's [REDACTED] [REDACTED] Intel.

Patent Owner's evidence that Petitioner's products are [REDACTED] [REDACTED] does not come close to suggesting that "it can be fairly said that the petitioner had a full and fair opportunity to litigate the validity of the patent" [REDACTED] Intel [REDACTED] *WesternGeco*, 889 F.3d at 1319. Indeed, Patent Owner does not assert that any of Petitioner's products were specifically accused in prior litigation against [REDACTED] Intel, [REDACTED],¹⁰ or that any Petitioner was involved in those cases through third party discovery or otherwise. There is no suggestion that any Petitioner was even aware of the '014 patent or Patent Owner's infringement claim before being served with a complaint. Thus, Patent Owner does not present evidence that lends

¹⁰ For example, Patent Owner alleges Cirrus Logic's chips "CS35L41 and CS40L25 are both currently accused, . . . and both are [REDACTED]" Prelim. Resp. 7–8 (citing Exs. 2018, 2021, 2035). Patent Owner's evidence does not show that Cirrus Logic's chips CS35L41 or CS40L25 were accused during the [REDACTED]. Although Patent Owner cites a Teardown report (Ex. 2035), Patent Owner does not show that the report was cited or relied upon in the [REDACTED]. Furthermore, the report shows that the accused [REDACTED] contains "16 major ICs" (integrated circuits), all but one of which are supplied by manufacturers other than Cirrus Logic. *Id.* at 2. Likewise, Patent Owner contends that an OmniVision sensor (OV7261) is a component of [REDACTED] [REDACTED] Prelim. Resp. 11 (citing Ex. 2021, 18). Again, there is no persuasive evidence that OV7261, in particular, was alleged to infringe any patent during the [REDACTED].

support to a finding that [REDACTED]
[REDACTED] renders them privies for
purposes of § 315(b).

c. [REDACTED]

Patent Owner argues [REDACTED] Intel [REDACTED]
[REDACTED] Intel, [REDACTED]
[REDACTED] Prelim.

Resp. 30–31 (citing *Ventex*, Paper 148). We disagree. Unlike the
agreements in *Ventex*, Paper 148 at 12, [REDACTED]
[REDACTED]
[REDACTED] Nor is there any
argument that [REDACTED]

d. *Patent Exhaustion*

Patent Owner argues that the doctrine of patent exhaustion [REDACTED]
[REDACTED]
[REDACTED]
[REDACTED] Prelim. Resp. 31. According to Patent Owner,
[REDACTED]
[REDACTED] *Id.* We disagree. It is true that
downstream purchasers and users of Intel’s products that incorporate
products made by Petitioner [REDACTED] may have a [REDACTED]
(or exhaustion) defense against any claim of infringement by Patent Owner.
The relevant question, however, is ultimately whether the relationship
between Petitioner [REDACTED], and in particular Intel, is sufficiently
close to justify denying Petitioner its day in court. *See Taylor*, 553 U.S. at
892. Patent Owner does not sufficiently explain why a license defense

supports such a privity relationship between Petitioner and Intel.

e. Indemnification

Patent Owner argues that [REDACTED]

[REDACTED]. Prelim. Resp. 31–

32. As evidence of this alleged indemnification obligation, Patent Owner argues that [REDACTED]

[REDACTED]

[REDACTED]” *Id.* (quoting

Paper 11, 8; citing Ex. 2033, 24). Patent Owner also directs us to the indemnification provisions found in Petitioner Cirrus Logic’s “standard sales agreement[.]” *Id.* at 10 (citing Ex. 2026, 1, 4–5).

An agreement by a petitioner to indemnify a third party in an earlier infringement suit can give rise to a privity relationship between the petitioner and that third party. *Intel Corp. v. U.S. Int’l Trade Comm’n*, 946 F.2d 821, 839 (Fed. Cir. 1991). With respect to the ’014 patent, the evidence of record suggests that only [REDACTED]—Intel—is potentially time-barred. Cirrus Logic’s indemnification provisions are directed to specific products sold by Cirrus Logic. Ex. 2026. To the extent that Cirrus Logic’s indemnification provisions could demonstrate a privity relationship sufficient to deny Petitioner its day in court, it must be with respect to a product Cirrus Logic sold to Intel. The present record, however, does not identify any Cirrus Logic device or component that formed the basis for the [REDACTED] Intel. As such, we are not persuaded that the indemnification provisions of Cirrus Logic’s “standard sales agreement” are relevant to [REDACTED] Intel.

Patent Owner contends that Global Foundries' publications suggest it may indemnify customers. Prelim. Resp. 13. Patent Owner also present evidence that Global Foundries [REDACTED] Intel. *Id.* (citing Ex. 2014, 19). We are directed to no persuasive evidence, however, to suggest that Global Foundries [REDACTED] Intel [REDACTED] Nor is there any evidence of record that Global Foundries indemnifies customers for every type of intellectual property infringement claim brought against it, such as for the technology at issue in the '014 patent. As such, there is simply insufficient evidence to suggest that any party had an [REDACTED] Intel that would give rise to a privity relationship relevant to the current Petition.

f. Conclusion as to Timeliness of the Petition

As noted above, privity concerns “whether the petitioner and the prior litigant’s relationship—as it relates to the [earlier] lawsuit—is sufficiently close that it can be fairly said that the petitioner had a full and fair opportunity to litigate the validity of the patent in that lawsuit,” or “whether the petitioner is simply serving as a proxy to allow another party to litigate the patent validity question that the other party raised in an earlier filed litigation.” *WesternGeco*, 889 F.3d at 1319. A petitioner’s “initial identification of the real parties in interest [and privies] should be accepted unless and until disputed by a patent owner.” *Worlds*, 903 F.3d at 1244. In order to raise such a dispute, “a patent owner must produce *some* evidence that tends to show that a particular [time-barred] third party should be named a [privity].” *Id.* Here, Patent Owner argues that it has produced such evidence in several respects, but, on the present record, none of the evidence

in question tends to show that [REDACTED]
[REDACTED] for purposes of § 315(b). As such, we find the evidence of record does not tend to suggest that Petitioner is time-barred under 35 U.S.C. § 315(b), and does not call into question Petitioner's assertion that the Petition is timely-filed.¹¹

E. Claims 1–9, 12–14, 16–21, and 23–28 in View of Kawagoe

Petitioner contends the subject matter of claims 1–9, 12–14, 16–21, and 23–28 would have been obvious over the disclosures of Kawagoe. Pet. 9–46.

1. Kawagoe

Kawagoe discloses a process for manufacturing a semiconductor integrated circuit device using an epitaxial wafer, i.e., a semiconductor wafer having a semiconductor single crystal epitaxial layer grown over a polished semiconductor substrate. Ex. 1007, 1:13–27, 2:31–35. According to Kawagoe, “[t]he epitaxial wafer is advantageous in that it is excellent in suppressing the soft errors and resisting to the latchup,”¹² and also has

¹¹ Pursuant to 37 C.F.R. § 42.51(b)(1)(iii), Petitioner is required to “serve relevant information that is inconsistent with a position” it has advanced during the proceeding. To the extent Petitioner is in possession of information that is inconsistent with its assertion that it is not in privity with Intel, such information should be served upon Patent Owner, subject to the exceptions outlined in § 42.51(b)(1)(iii).

¹² Petitioner submits Exhibit 1009 (Wang and Agrawal, *Single Event Upset: An Embedded Tutorial*, 21st Int’l Conf on VLSI Design, 429–434, IEEE 2008), which explains that “soft errors” are “random and not related to permanent hardware faults” and “[t]heir causes may be internal (e.g., interconnect coupling) or external (e.g., cosmic radiation),” including “alpha particles [that] are emitted when the nucleus of an unstable isotope decays to a lower energy state.” Ex. 1009, Abstract, 430. Dr. Banerjee characterizes

“excellent breakdown characteristics” that “drastically reduce the defect density of the gate insulating film” of a semiconductor integrated device. *Id.* at 1:33–40.

Kawagoe discloses various “representative” processes, including processes in which the single crystal (epitaxial) layer contains an impurity of the same type and in the same concentration as the substrate body.

Ex. 1007, 2:55–3:9. According to Kawagoe, the impurity concentration of the substrate body can be made higher than that of the epitaxial layer “so that the resistance of the semiconductor substrate body can be relatively lowered to improve the resistance to the latchup.” *Id.* at 4:1–8. Kawagoe discloses a process for manufacturing a semiconductor integrated circuit device including a step of forming a semiconductor region (well) extending below the epitaxial layer and having an impurity concentration that decreases with increasing depth below the epitaxial layer. *Id.* at 3:10–25. According to Kawagoe, the well can be used for forming a complementary Metal-Oxide-Semiconductor.Field-Effect-Transistor (“MOS.FET”) circuit. *Id.* at 3:32–38.

Kawagoe describes seven embodiments, including Embodiment 1 (Ex. 1007, 6:41–12:40, Figs. 1–8) and Embodiment 4 (*id.* at 14:46–19:63, Figs. 16–25). Figure 1, reproduced below, depicts the device of Embodiment 1.

“latchup” as “a ‘short-circuit’ failure condition in poorly designed circuits.” Ex. 1003 ¶ 77.

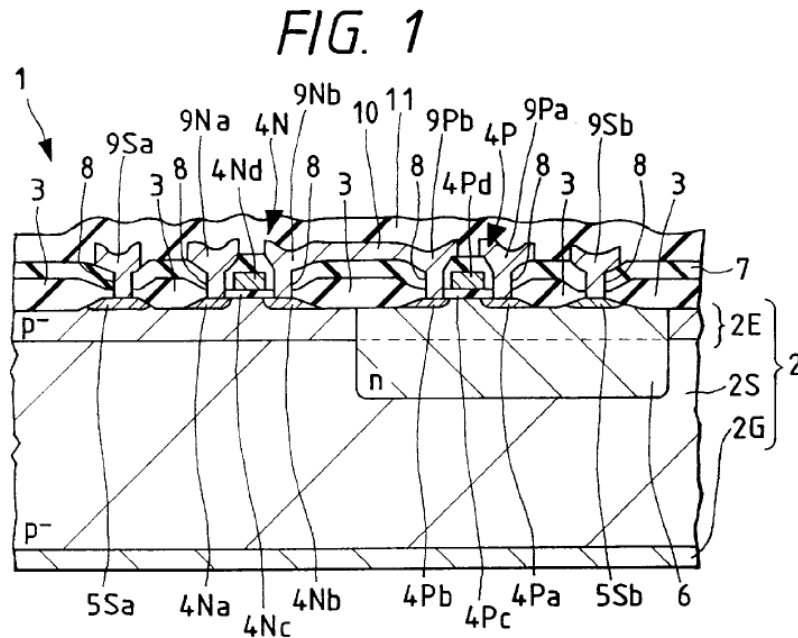


Figure 1 depicts “an essential portion of a semiconductor integrated circuit device” that includes semiconductor substrate body 2S, epitaxial layer 2E, and gettering layer 2G. *Id.* at 6:51–56, Fig. 1. Substrate body 2S and epitaxial layer 2E are doped with a p-type impurity in equal concentrations. *Id.* at 6:60–7:3, 10:51–55, 11:12–16. Embodiment 1 includes n-channel MOS.FET (“nMOS”) 4N and p-channel MOS.FET (“pMOS”) 4P, the latter being formed in n-well 6, which is doped with n-type impurity and extends below the epitaxial layer. *Id.* at 8:46–52, 9:32–40, 11:18–24, 11:43–50, Figs. 1, 5, 7.

Figure 23, reproduced below, depicts a semiconductor device of Embodiment 4 in the process of manufacture. *Id.* at 17:11–13.

FIG. 23

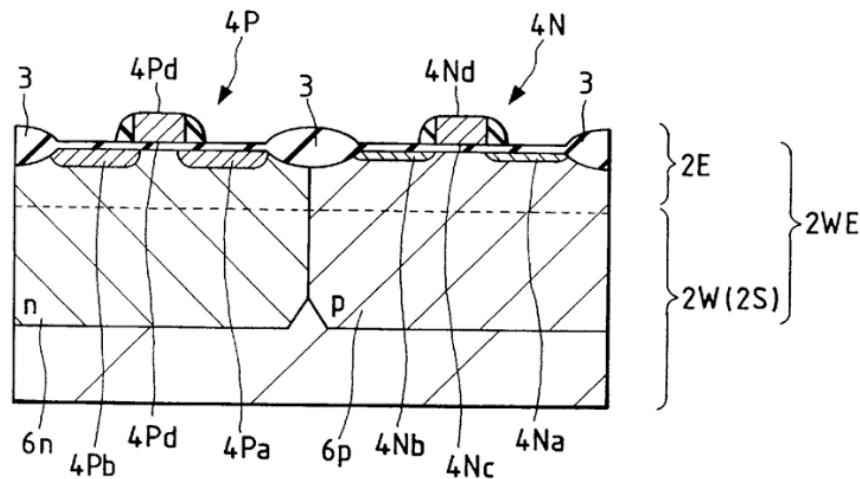


Figure 23 shows a step in a process for manufacturing the semiconductor integrated circuit device of Embodiment 4, including p-well 6p formed with nMOS 4N and n-well 6n formed with pMOS 4P. *Id.* at 6:1–4, 15:26–32, 18:3–35. Substrate body 2S and epitaxial layer 2E are doped with p-type impurity, and the impurity concentration of substrate body 2S is higher than that of epitaxial layer 2E “to improve the resistance to the latchup.” *Id.* at 14:64–15:6, 15:13–17, 16:16–21, 19:59–63, Fig. 17. In Embodiment 4, the impurity concentration in p-well 6p and n-well 6n decreases with increasing depth below the epitaxial layer. *Id.* at 15:62–16:15, 17:55–61, Fig. 17. Kawagoe discloses that the concentration gradient reduces soft errors by attracting carriers (electrons) to the substrate and preventing them from entering the p-well. *Id.* at 16:2–11.

Petitioner relies on Kawagoe Figure 17, which is reproduced below and illustrates properties of the semiconductor device of Embodiment 4.

FIG. 17

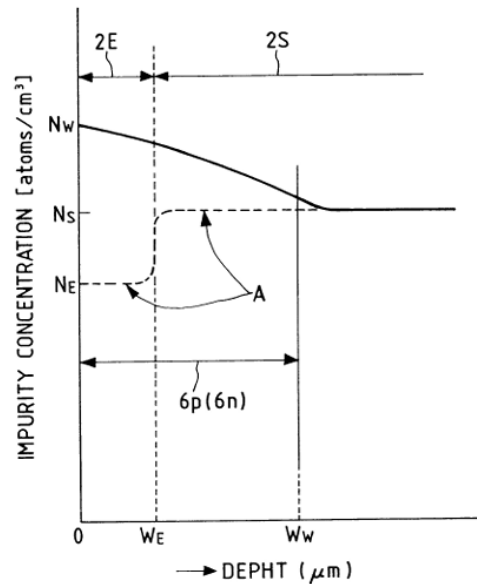


Figure 17 is a plot of impurity concentration as a function of depth in a semiconductor integrated circuit device, which shows “the p-well 6p and n-well 6n have their impurity concentrations gradually lowered in the depthwise direction from the principal surface (having an impurity concentration N_w) of the epitaxial layer 2E.” Ex. 1007, 5:41–45, 15:62–16:40.

2. Analysis—Claims 1 and 21

Petitioner argues that Kawagoe discloses the limitations of independent claims 1 and 21. Pet. 9–46. On the present record, Patent Owner does not disagree. Prelim. Resp. 1–37.

The preamble and first clause of independent claims 1 and 21 recites “An electronic system, [the system] comprising: at least one semiconductor device, the at least one semiconductor device including:”¹³ Ex. 1001, 4:49–

¹³ Petitioner uses bracketed language to show the difference between an

51, 6:4–6. To the extent the preamble is limiting, Petitioner contends that Kawagoe discloses a “semiconductor integrated circuit device,” such as a microcomputer and memories that each constitute an electronic system. Pet. 9 (citing Ex. 1007, 1:13–23, 14:46–67, 24:28–31, 19:15–16, 20:1–33, 22:10–23:14, Figs. 16, 17, 23, 26(A), 28; Ex. 1003 ¶ 64). Petitioner further contends that this evidence demonstrates that Kawagoe discloses at least one semiconductor device. *Id.* at 10–11. We find that, to the extent the preamble is limiting, Petitioner’s contention for these limitations is sufficiently supported for purposes of institution.

Claims 1 and 21 recite “a substrate of a first doping type at a first doping level having a surface.” Ex. 1001, 4:52–53, 6:7–8. Petitioner contends that Kawagoe discloses a “semiconductor substrate 2” having a first doping type (p-type), and that this substrate has a surface. Pet. 11 (citing Ex. 1007, 14:61–15:12, 6:50–7:3, Fig. 23 (annotated in orange)). Petitioner contends one of ordinary skill in the art would have sought to use the uniformly-doped (“a first doping level”) epitaxial substrate of Embodiment 1 of Kawagoe, as opposed to Embodiment 4’s latchup-resistant substrate, to form the twin-well CMOS device of Figure 23 because this would optimize costs over latch-up resistance. *Id.* at 12–17. We find that Petitioner’s contention for this limitation is sufficiently supported for purposes of institution.

Claims 1 and 21 also recite “a first active region disposed adjacent the surface [of the substrate] with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed [in the surface thereof].” Ex. 1001, 4:54–57, 6:9:13. Petitioner contends that

identified pair of claims. Pet. 9, n.3. We use this convention as well.

Kawagoe discloses “semiconductor regions 4Na and 4Nb” that are used “for forming the *source-drain regions* of the nMOS [n-channel transistor] 4N.” Pet. 17 (citing Ex. 1007, 8:66–67; *id.* at 3:35–38, 8:45–52, 14:46–55, 15:26–40) (modifications and emphasis by Petitioner). Petitioner contends that source-drain regions 4Na/4Nb, in conjunction with the channel region between these regions, form part of the claimed first active region. *Id.* at 18. Petitioner further contends that regions 4Na and 4Nb are doped with a n-type impurity and, therefore, have a second doping type (n-type) opposite in conductivity to the first doping type (p-type) of the substrate. *Id.* at 18–19. Petitioner contends that nMOS transistor 4N is formed in the claimed first active region and an “active region . . . within which transistors can be formed” requires only that at least one transistor can be formed. *Id.* at 19; *see also id.* at 19–20 (asserting that Kawagoe satisfies the recited claim elements under either Petitioner’s or Patent Owner’s construction of “active region”). We find that Petitioner’s contention for this limitation is sufficiently supported for purposes of institution.

Claims 1 and 21 also recite “a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed [in the surface thereof]” and “transistors formed in at least one of the first active region or second active region.” Ex. 1001, 4:58–62, 6:14–19. Petitioner contends that semiconductor regions (source-drain regions) 4Pa and 4Pb are part of the claimed second active region, which also includes the channel region that is between them and below gate 4Pd. Pet. 21–22. According to Petitioner, as shown in Figure 23, pMOS transistor 4P is formed in the surface of this second active region, which is separate from and disposed adjacent to the first active region. *Id.* at 22. Petitioner contends that a single pMOS transistor 4P may be formed in

the second active region, or one of ordinary skill in the art would have understood that multiple pMOS transistors could be formed in this region to minimize chip area. *Id.*; *see also id.* at 19 (asserting that forming multiple transistors will minimize chip area, “as good layout practice dictates”). We find Petitioner’s contentions for these limitations are sufficiently supported for purposes of institution.

Claims 1 and 21 also recite “at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the [first and second active regions towards/surface to] an area of the substrate where there are no active regions.” Ex. 1001, 4:63–67, 6:21–25. Petitioner contends that Figure 17 of Kawagoe illustrates the doping concentration from a top surface of the substrate and the channel region, and shows that the dopant concentration is “gradually lowered in the depthwise direction *from the principal surface* (having an impurity concentration NW) of the epitaxial layer 2E.” Pet. 23–24 (quoting Ex. 1007, 15:62–16:40, Fig. 17) (emphasis by Petitioner). According to Petitioner, the dopant concentration is thus graded in the channel region of transistor 4N, which is a portion of the first active region formed at “the principal surface” of epitaxial layer 2E. *Id.* at 24 (citing Ex. 1003 ¶ 90); *see also id.* at 25 (noting the same dopant configuration for pMOS transistor 4P, i.e., the second active region) (citing Ex. 1007, 15:62–16:2). Petitioner contends that Kawagoe explains that the downward-sloping graded dopant concentration aids the movement of carriers from the first and second active regions towards the bottom of the substrate where there are no active regions. *Id.* at 25–26 (citing Ex. 1007, 16:2–11); *see also id.* at 27 (noting that the downward-sloping graded dopant concentration aids the movement of carriers from the surface to deeper parts of the substrate

where there are no active regions). We find that Petitioner’s contentions for this limitation are sufficiently supported for purposes of institution.

Claims 1 and 21 also require “at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface [towards/to] the area of the substrate where there are no active regions.” Ex. 1001, 5:1–5, 6:26–30. Petitioner contends that Kawagoe discloses “p-well 6p” that is adjacent to a first active region and discloses that the dopant concentration in p-well 6p gradually decreases with depth. Pet. 28–29 (citing Ex. 1007, 8:66–67, 14:46–55, 15:26–40, 15:62–16:40; Ex. 1003 ¶ 95). Petitioner further contends that Kawagoe explains that the downward-sloping graded dopant concentration aids carrier movement from the surface of the epitaxial layer towards/to the area of the substrate where there are no active regions. *Id.* at 30 (citing Ex. 1007, 16:2–11). We find that Petitioner’s contention for this limitation is sufficiently supported for purposes of institution.

Claim 1 also requires “wherein at least some of the transistors form digital logic of the semiconductor device.” Ex. 1001, 5:5–7. Petitioner contends that Kawagoe teaches that the transistors in its active regions may form a CMOS circuit or be applied to a logic circuit such as a microcomputer. Pet. 34 (citing Ex. 1007, 8:46–52, 14:46–55, 15:26–40, 20:1–33, 22:10–29, 22:51–23:2, 24:28–31; Ex. 1008A, 810–811; Ex. 1003 ¶ 103). We find that Petitioner’s contention for this limitation is sufficiently supported for purposes of institution.

Claim 21 also requires “wherein the graded dopant concentration is linear, quasilinear, error function, complementary error function, or any combination thereof.” Ex. 1001, 6:30–33. Petitioner contends that, for the reasons discussed above, the graded dopant concentration of Kawagoe is

linear or nearly linear (quasilinear). Pet. 34–35 (citing Ex. 1007, Fig. 17; Ex. 1003 ¶ 104). We find that Petitioner’s contention for this limitation is sufficiently supported for purposes of institution.

In view of the foregoing, and on this record, Petitioner demonstrates sufficiently for purposes of institution that Kawagoe discloses, or teaches or suggests in combination with the knowledge of one of ordinary skill in the art, every limitation of claims 1 and 21. Accordingly, Petitioner demonstrates a reasonable likelihood that claims 1 and 21 would have been obvious over the disclosures of Kawagoe.

3. Analysis—Remaining Claims

Petitioner identifies where it contends the subject matter of claims 2–9, 12–14, 16–20, and 23–28 is taught or suggested in Kawagoe. Pet. 64–77. Patent Owner does not, on this record, dispute Petitioner’s identifications.

Upon review of Petitioner’s arguments and supporting evidence, we determine that Petitioner demonstrates a reasonable likelihood that claims 2–9, 12–14, 16–20, and 23–28 would have been obvious over Kawagoe.

F. Claims 1, 2, 4–9, 12–23, and 25–28 in view of Wieczorek and Wolf

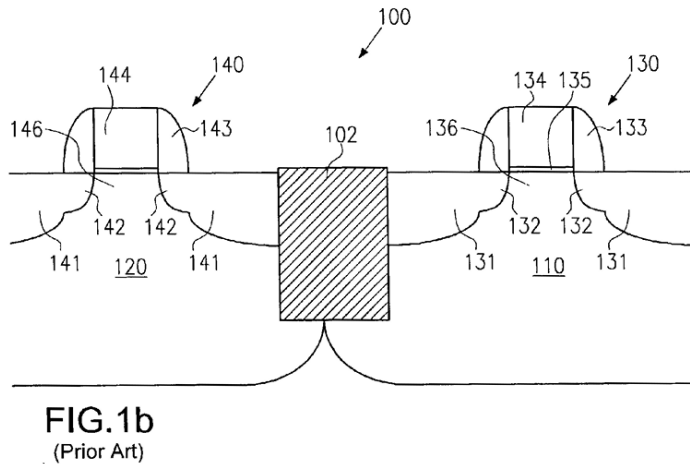
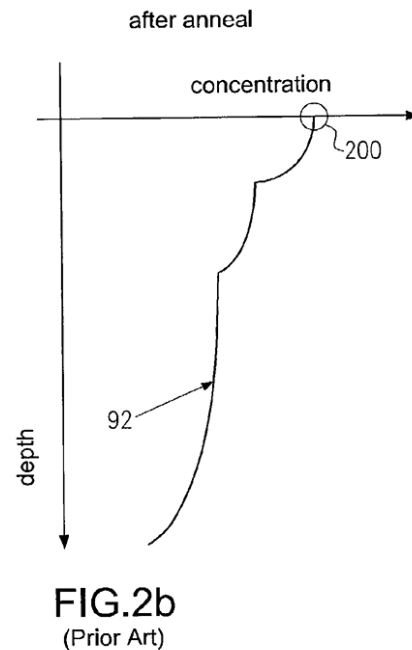
Petitioner contends that the subject matter of claims 1, 2, 4–9, 12–23, and 25–28 would have been obvious in view of the combined disclosures of Wieczorek and Wolf. Pet. 46–77.

1. Wieczorek

Wieczorek relates “to a semiconductor device, such as a field-effect transistor, having an improved retrograde dopant profile in a channel region of the transistor element.” Ex. 1006 ¶ 2. Wieczorek explains that a retrograde channel dopant profile is one where “the concentration of dopants increases from the gate insulation layer to the areas located deeper down the

channel region.” Ex. 1006 ¶ 6. According to Wieczorek, although a retrograde channel dopant profile is desirable, it is “very difficult to obtain.” *Id.* Wieczorek notes that “the dopant concentration immediately after the implantation process exhibits a desired retrograde dopant profile” (*id.* ¶ 9), but during heat treatment, “the initially retrograde profile in the vicinity of the surface of the semiconductor device . . . may have become substantially uniformly distributed” due to diffusion of the dopant atoms (*id.* ¶ 11).

Petitioner relies on Figures 1b and 2b (reproduced below), which Wieczorek uses to illustrate the prior art.



Wieczorek Figure 1b shows a conventional semiconductor device at an advanced manufacturing stage. Ex. 1006 ¶¶ 12, 20. The device includes P-channel transistor 140 with source and drain regions 141 in N-well structure 120 and N-channel transistor 130 with source and drain regions 131 in P-well structure 110. *Id.* ¶ 12. Shallow trench isolation 102 separates N-well structure 120 from P-well structure 110. *Id.* ¶ 7. Wieczorek Figure 2b is a graph of dopant concentration versus depth of N-well

structure 120 and P-well structure 110 and shows “a typical dopant profile with respect to the depth of the respective well structure” after ion implantation and heat treatment. *Id.* ¶¶ 9–11, 13, 21.

2. *Wolf*

Wolf is a four-volume textbook titled “Silicon Processing for the VLSI Era.” Ex. 1008. A portion of the textbook focuses on CMOS technology. Ex. 1008A, 807–40.

3. *Analysis – Claims 1 and 21*

a. *Motivation to Combine*

Wieczorek discloses both prior art devices and different approaches for addressing difficulties in maintaining a retrograde profile in such conventional prior art devices. Pet. 46. Petitioner relies on Wieczorek’s disclosure of the conventional prior art device. *Id.* (“This Petition relies on Wieczorek’s description of a conventional prior-art CMOS device.”).

Petitioner contends *Wolf* is “a well-known textbook,” and relies on *Wolf* for teaching “known fundamental features and concepts related to semiconductor manufacturing, with particular emphasis on CMOS devices.” *Id.* (citing Ex. 1008A, Chapter 16; Ex. 1003 ¶ 129). According to Petitioner, a person of ordinary skill in the art would have understood and expected that the teachings of *Wolf* would apply to Wieczorek’s conventional CMOS device, and would have looked to *Wolf* for additional details related to conventional CMOS devices. *Id.* at 47.

b. *Claims 1 and 21*

Claims 1 and 21 recite “An electronic system, [the system] comprising: at least one semiconductor device, the at least one

semiconductor device including:”¹⁴ Ex. 1001, 4:51, 6:4–6. To the extent the preamble is limiting, Petitioner contends that Wieczorek teaches or renders obvious a “semiconductor device 100” that constitutes an electronic system. Pet. 48 (citing Ex. 1006 ¶ 12, Fig. 1b; Ex. 1003 ¶ 130). On this record, Petitioner has shown sufficiently that Wieczorek teaches the recited subject matter of claims 1 and 21.

Claims 1 and 21 also recite “a substrate of a first doping type at a first doping level having a surface.” Ex. 1001, 4:52–53, 6:7–8. Petitioner contends that Wieczorek in combination with Wolf discloses this limitation. In support, Petitioner provides an annotated version of Figure 1b of Wieczorek, which is reproduced below.

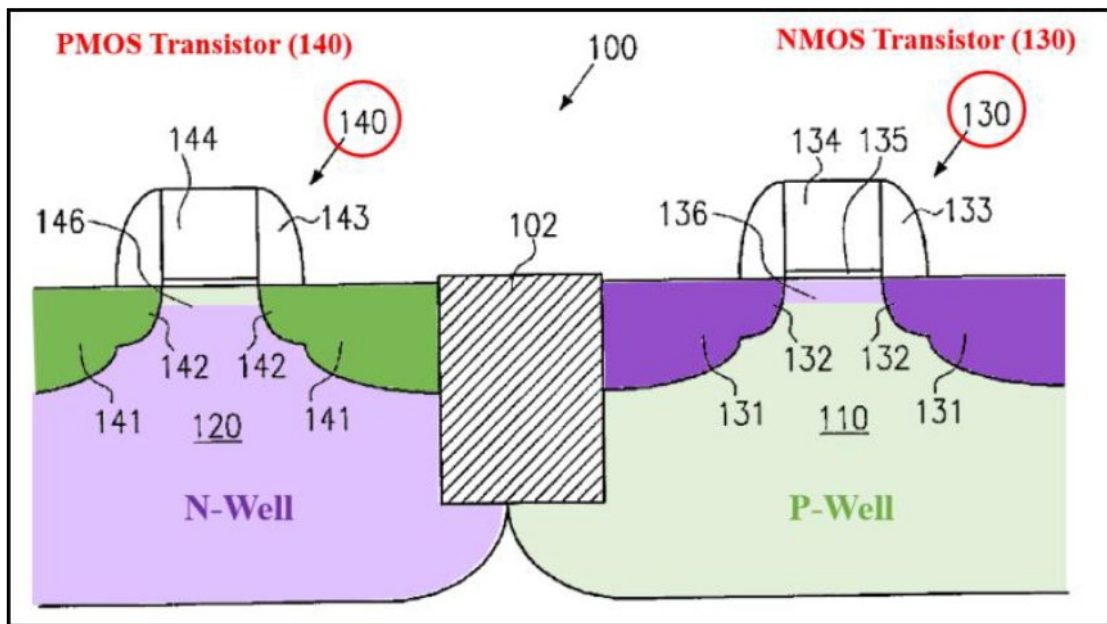


Figure 1b is annotated to show N-channel transistor 130 (nMOS) with source/drain regions 131–132 (purple) and channel region 136 (light purple)

¹⁴ Petitioner uses bracketed language to show the difference between an identified pair of claims. Pet. 9, n.3. We use this convention as well.

formed in P-well 110 (light green). Pet. 48 (citing Ex. 1006 ¶¶ 7, 12, 20–21; Ex. 1008C, 525, Fig. 8-1(e)). Figure 1b is also annotated to show P-channel transistor 140 (pMOS) with source/drain regions 141–142 (green) and channel region 146 (light green) formed in N-well 120 (light purple). *Id.*

Petitioner contends that Wieczorek explains that the P-well and N-well structures may be formed on any appropriate substrate, but does not explicitly specify what that substrate may be. *Id.* at 48–49 (citing Ex. 1006 ¶¶ 4, 7; Ex. 1003 ¶ 132). Petitioner asserts, however, that one of ordinary skill in the art would have understood that a twin well approach is independent of the starting material type for the substrate, and such an ordinarily skilled artisan would have consulted Wolf to confirm that a “***uniform***, lightly doped *p*- or *n*- type substrate” is commonly used in twin-well CMOS devices. *Id.* at 49 (citing Ex. 1008C, 523, 530; Ex. 1008B, 387–389; Ex. 1003 ¶ 134). According to Petitioner, one of ordinary skill in the art would have found it obvious to use a uniformly doped *n*- or *p*- type substrate as “[d]oing so would amount to combining known prior art elements . . . according to known methods . . . to obtain predictable results.” *Id.* at 50; *see also id.* (asserting that the proposed combination would involve “nothing more than choosing one of a finite number of known appropriate substrates that are described by Wolf as suitable for use in forming a twin-well CMOS device”). We find that Petitioner’s contentions for this limitation are sufficiently supported for purposes of institution.

Claims 1 and 21 also recite “a first active region disposed adjacent the surface [of the substrate] with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed [in the surface thereof];” Ex. 1001, 4:54–57, 6:9:13. Petitioner contends that Figure 1b of Wieczorek shows nMOS transistor 130 that includes “heavily

N-doped **source and drain regions** 131, including lightly doped extensions 132” and “**channel region** 136.” Pet. 52 (citing Ex. 1006 ¶¶ 4, 12–13).

Petitioner further contends that nMOS transistor 130 is formed in the surface of the first active region, which is adjacent the surface of the substrate, and because the source-drain regions are N-doped the first active region has a second doping type that is opposite in conductivity to the first doping type (P-type). *Id.* at 53–54. We find that Petitioner’s contentions for this limitation are sufficiently supported for purposes of institution.

Claims 1 and 21 also recite “a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed [in the surface thereof].” Ex. 1001, 4:58–62, 6:14–19. Petitioner contends that P-channel transistor 140 of Wieczorek includes heavily P-doped source and drain regions 141, lightly doped extensions 142, and channel region 146, which are part of the claimed second active region. Pet. 55 (citing Ex. 1006 ¶¶ 4, 7, 12–13; Ex. 1003 ¶ 142). According to Petitioner, this second active region is disposed adjacent the first active region and transistors (one or more), such as P-channel transistor 140, can be formed in the surface of this second active region. *Id.* at 55–56. We find that Petitioner’s contentions for this limitation are sufficiently supported for purposes of institution.

Claims 1 and 21 also recite “at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the [first and second active regions towards/surface to] an area of the substrate where there are no active regions.” Ex. 1001, 4:63–67, 6:21–25. Petitioner contends that the doping concentration of transistor 130 (including the channel region) in Wieczorek is shown in Figure 2b (reproduced above), and shows a dopant concentration

that is highest at the surface of the substrate and decreases with depth. Pet. 57–58 (citing Ex. 1006 ¶¶ 4, 9, 11, 13, Figs. 2a-2b; Ex. 1008B, 298–301, Fig. 5-2; Ex. 1003 ¶ 148). Petitioner further contends that Wieczorek’s downward-sloping graded dopant concentration aids carrier movement from the first and second active regions towards/to an area of the substrate in which there are no active regions. *Id.* at 59–60 (citing Ex. 1003 ¶¶ 149–150; Ex. 1010, 2:27–32, 5:14–22). We find that Petitioner’s contentions for this limitation are sufficiently supported for purposes of institution.

Claims 1 and 21 also require “at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface [towards/to] the area of the substrate where there are no active regions.” Ex. 1001, 5:1–5, 6:26–30. Petitioner contends that P-well structure 110 shown in annotated Figure 1b (light green) is adjacent to the first active region (purple/light purple), and the dopant concentration in P-well 110 is gradually decreasing with depth (Figure 2b). Pet. 61 (citing Ex. 1006 ¶¶ 9, 11–13; Ex. 1003 ¶ 153). According to Petitioner, the downward-sloping gradient of Wieczorek was known to create a “built-in” electric field that moves carriers deep into the substrate, i.e., it aids carrier movement from the surface towards/to the area of the substrate where there are no active regions. *Id.* at 62. We find that Petitioner’s contentions for this limitation are sufficiently supported for purposes of institution.

Claim 1 also requires “wherein at least some of the transistors form digital logic of the semiconductor device.” Ex. 1001, 5:5–7. Petitioner contends that Wieczorek’s “complementary MOS transistor pair” is a “frequently used semiconductor device in modern integrated circuits” and was understood to form digital logical gates. Pet. 63 (Ex. 1006 ¶¶ 7, 26;

Ex. 1008A, 810–811; Ex. 1003 ¶ 157). We find that Petitioner’s contentions for this limitation are sufficiently supported for purposes of institution.

Claim 21 also requires “wherein the graded dopant concentration is linear, quasilinear, error function, complementary error function, or nay combination thereof.” Ex. 1001, 6:30–33. Petitioner contends that, as shown in Figure 2b, the graded dopant concentration is a combination of linear or nearly linear (quasilinear) segments. Pet. 63–64 (citing Ex. 1003 ¶ 158). We find that Petitioner’s contentions for this limitation are sufficiently supported for purposes of institution.

In view of the foregoing, Petitioner sufficiently demonstrates for purposes of institution that Wieczorek and Wolf teach or suggest every limitation of claim 1. Petitioner also provides an explanation, supported by factual underpinning, to support the combination of Wieczorek and Wolf. Accordingly, Petitioner demonstrates a reasonable likelihood that claims 1 and 21 would have been obvious over Wieczorek and Wolf.

4. Analysis—Remaining Claims

Generally relying on the same figures of Wieczorek, and citations to Wolf, Petitioner identifies where it contends every limitation of claims 2, 4–9, 12–20, 22, 23, and 25–28 is disclosed in Wieczorek and Wolf. Pet. 64–77. Patent Owner does not dispute, on this record, any of Petitioner’s arguments and evidence with respect to these claims. Upon review of Petitioner’s arguments and evidence, we find that Petitioner’s contentions with respect to the remaining claims are sufficiently supported for purposes of institution.

G. Grounds Including Gupta

1. Gupta

Gupta “relates to the field of complimentary metal oxide semiconductor (CMOS) circuits, and more particularly to automatically producing layouts for CMOS circuits.” Ex. 1014, 1:7–10. According to Gupta, “[a]s semiconductor chips become ever larger, incorporating ever more devices, it becomes increasingly important to minimize semiconductor area used by a given number of devices.” *Id.* at 1:28–31. Doing so “potentially [saves] millions of dollars.” *Id.* at 1:31–34. To accomplish this goal, Gupta discloses abutting multiple transistors to “form transistor chains.” *Id.* at 2:17–21, Fig. 4.

2. Analysis

As discussed above, several challenged claims require “transistors” or “devices.” Pet. 77 (citing claims 1, 4, 5, 13, 21, 25, 26). Petitioner contends that one transistor is sufficient to show “transistors” or “devices” may be formed in the relevant layers, but to the extent that the claims are interpreted to require multiple transistors or devices be formed, Petitioner contends Gupta discloses such a configuration. *Id.* at 77–83. Patent Owner, on this record, does not contest this assertion.

For the reasons set forth above, we determine that Petitioner demonstrates that the challenged claims would have been obvious over Kawagoe or Wieczorek and Wolf. Thus, we do not address Petitioner’s additional arguments relying on the additional disclosures of Gupta.

H. Challenges Based on Silverbrook

Claim 19 depends from claim 1 and further requires “wherein the at least one semiconductor device is an image sensor.” Ex. 1001, 5:62–63.

Petitioner contends that the subject matter of claim 19 would have been obvious over the combined disclosures of Kawagoe and Silverbrook, or Wieczorek, Wolf, and Silverbrook. Pet. 83–84.

1. *Silverbrook*

Silverbrook “relates substantially to the concept of a disposable camera having instant printing capabilities.” Ex. 1046, 1:8–9. Part of Silverbrook’s camera is an “Image Capture and Processing Chip” that performs “CMOS image sensing.” *Id.* at 6:41–49. The CMOS image sensing is accomplished by “a CMOS active pixel sensor array” manufactured using a “CMOS/DRAM/APS process.” *Id.* at 6:50–55.

2. *Analysis*

Petitioner contends that Silverbrook expressly seeks incorporation of existing CMOS designs into its image sensor device, and asserts that using the CMOS device designs of Kawagoe or Wieczorek/Wolf in Silverbrook’s CMOS image sensor “would have been nothing more than” the combination of familiar elements, according to known methods, to yield predictable results. Pet. 83–84.

Patent Owner does not, on this record, contest Petitioner’s arguments with respect to claim 19.

Upon review of the arguments and prior art of record, we determine that Petitioner demonstrates sufficiently for purposes of institution where every limitation of claim 19 is disclosed or suggested in either Kawagoe and Silverbrook, or Wieczorek, Wolf, and Silverbrook.

IV. CONCLUSION

For the foregoing reasons, we determine that there is a reasonable likelihood that Petitioner would prevail with respect to at least one of the

claims challenged in the Petition. In addition, we are persuaded on the present record that the Petition is not time-barred under 35 U.S.C. § 315(b). Accordingly, we institute an *inter partes* review of all challenged claims based on the grounds asserted in the Petition.

V. ORDER

For the foregoing reasons, it is:

ORDERED that, pursuant to 35 U.S.C. § 314(a), *inter partes* review is instituted with respect to the grounds of unpatentability set forth in the Petition;

FURTHER ORDERED that, pursuant to 35 U.S.C. § 314(a) and 37 C.F.R. § 42.4, notice is given of institution of trial commencing on the entry date of this Decision;

FURTHER ORDERED that, in view of the pending motion to seal, this Decision is being filed “Board and Parties Only”; and

FURTHER ORDERED that after conferring with Petitioner, Patent Owner shall, within one week of this Decision, submit to the Board via email to Trials@uspto.gov, a version of this Decision to be filed on the public record, with any redactions proposed by either party.

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