

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TEXAS INSTRUMENTS INCORPORATED,
Petitioner,

v.

GREENTHREAD, LLC,
Patent Owner.

IPR2024-00774
Patent 11,316,014 B2

Before JON B. TORNQUIST, MONICA S. ULLAGADDI, and
JULIA HEANEY, *Administrative Patent Judges*.

TORNQUIST, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314
Granting Motion for Joinder
35 U.S.C. § 315(c); 37 C.F.R. § 42.122(b)

I. INTRODUCTION

Petitioner filed a petition (Paper 3, “Pet.”) to institute an *inter partes* review of claims 1–9 and 12–28 of U.S. Patent No. 11,316,014 B2 (Ex. 1001, “the ’014 patent”). 35 U.S.C. § 311. Along with the Petition, Petitioner filed a Motion for Joinder seeking to join the previously instituted proceeding in IPR2024-00019, which involves the ’014 patent and Petitioner Cirrus Logic, Inc. and OmniVision Technologies, Inc. (“the Cirrus IPR”). Paper 1 (“Mot.”). Patent Owner filed a Preliminary Response (Paper 15, “Prelim. Resp.”) and an Opposition to the Motion for Joinder (Paper 7, “Opp.”), and Petitioner filed a Preliminary Reply (Paper 18) that addresses privity issues raised in the Preliminary Response.¹ Patent Owner did not file a preliminary sur-reply.

For reasons explained below, we institute an *inter partes* review and grant the Motion for Joinder.

A. *Real Parties-in-Interest*

The parties each identify themselves as the real party-in-interest. Pet. 1; Paper 5, 1.

B. *Related Matters*

The parties identify numerous district court litigations as related matters, including the following parallel litigation: *Greenthread, LLC v. Texas Instruments Incorporated*, No. 2:23-cv-00157 (E.D. Tex., April 6, 2023). Pet. 2; Paper 5, 1.² The parties further note that the ’014 patent is at

¹ The Preliminary Response and the Preliminary Reply were filed under seal. Redacted versions of these papers are in the record as Papers 16 and 19, respectively.

² The Mandatory Notices of Petitioner and Patent Owner identify other pending infringement actions against the ’014 patent, including actions

issue in *Cirrus Logic, Inc., et. al. v. Greenthread, LLC*, IPR2024-00019; *Semiconductor Components Industries, LLC v. Greenthread, LLC*, IPR2024-00263; and *Monolithic Power Systems, Inc. v. Greenthread, LLC*, IPR2024-00553. Pet. 2; Paper 5, 1.

C. The '014 Patent

The '014 patent, titled “Semiconductor Devices with Graded Dopant Regions,” issued on April 26, 2022. Ex. 1001, codes (45), (54). The '014 patent “relates to all semiconductor devices and systems,” including Bipolar Junction Transistors (BJT). *Id.* at 1:39–52.

The '014 patent explains that in bipolar junction transistors, minority carriers are the principal device conduction mechanism, but majority carriers also play a small but finite role in modulating the conductivity in such devices. Ex. 1001, 1:50–54. The '014 patent further explains that “[e]fforts have been made in graded base transistors to create an aiding drift field to enhance the diffusing minority carrier’s speed from emitter to collector.” *Id.* at 1:62–64. The '014 patent explains that this improvement has not been implemented in most semiconductor devices, including various power MOSFETs and IGBTs, which “still use a uniformly doped ‘drift epitaxial’ region in the base.” *Id.* at 1:64–2:2. The '014 patent implements a graded dopant concentration in these devices, which results in at least two important performance enhancements: “electrons can be swept from source to drain rapidly, while at the same time holes can be recombined closer to the n+ buffer layer,” thereby improving “ t_{on} and t_{off} in the same device.” *Id.* at 3:42–47.

against both Cirrus Logic, Inc. and OmniVision Technologies, Inc. Pet. 1–2; Paper 5, 1–2.

Figure 1 of the '014 patent is reproduced below.

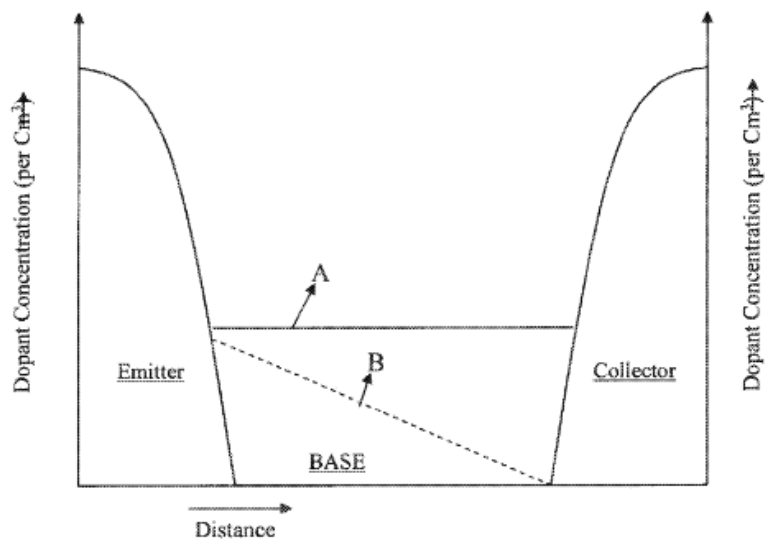


Figure 1 is labeled “Prior Art” and “illustrates the relative doping profiles of emitter, base and collector for the two most popular bipolar junction transistors: namely, uniform base (“A”) and graded base (“B”).” Ex. 1001, 2:40–43, Fig. 1.

Figure 3A of the '014 patent is reproduced below.

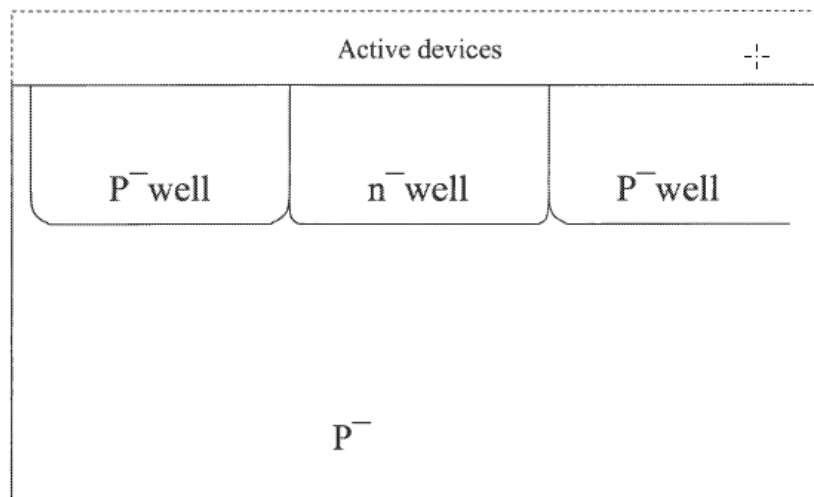


Figure 3A is labeled “Prior art” and shows a cross section of “a typical prior art IC with two wells (one n- well in which p-channel transistors are

subsequently fabricated and one p-well in which n-channel transistors are subsequently fabricated).” Ex. 1001, 2:46–51, Fig. 3A.

Figure 5A of the '014 patent is reproduced below.

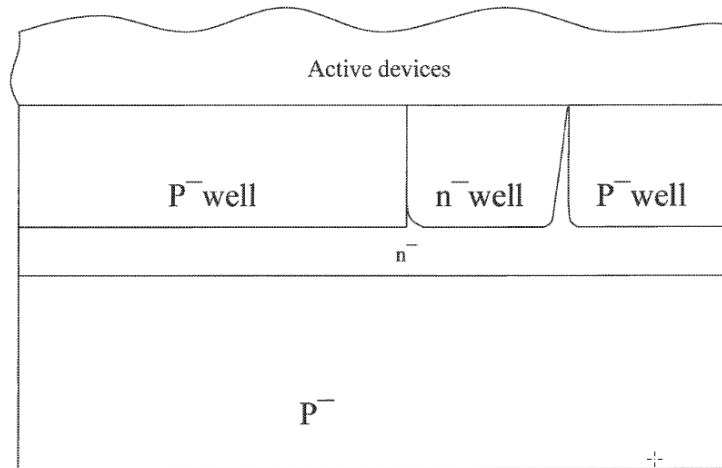


Figure 5A illustrates a cross section of a CMOS silicon substrate with two wells and an underlying layer using embodiments of the invention to improve performance in each application. Ex. 1001, 2:58–61. In this embodiment, “the subterranean n^- layer has a graded donor concentration” as may the n^- and p^- wells. *Id.* at 4:1–9

According to the '014 patent, “[s]purious minority carriers can be generated by clock switching in digital VLSI logic and memory ICs.” Ex. 1001, 3:51–52. The '014 patent states that these “unwanted carriers can discharge dynamically-held ‘actively held high’ nodes,” and serve to degrade performance of various types of devices, including CMOS digital images and DRAMs. *Id.* at 3:51–59. According to the '014 patent, “a novel technique is described” that “creates a drift field to sweep these unwanted minority carriers from the active circuitry at the surface into the substrate in a monolithic die as quickly as possible.” *Id.* at 3:64–4:1. For example, a

graded donor concentration in subterranean n^- layer may be used to “sweep the minority carriers deep into the substrate.” *Id.* at 4:1–3.

D. Illustrative Claim

Claims 1 and 21 are independent, with challenged claims 2–9 and 12–20 depending from claim 1 and challenged claims 22–28 depending from claim 21. Ex. 1001, 4:49–6:56. Claim 1 is representative of the challenged claims and is reproduced below.

1. An electronic system, the system comprising:

at least one semiconductor device, the at least one semiconductor device including:

a substrate of a first doping type at a first doping level having a surface;

a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;

a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;

transistors formed in at least one of the first active region or second active region;

at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions; and

at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the

surface towards the area of the substrate where there are no active regions, wherein at least some of the transistors form digital logic of the semiconductor device.

Ex. 1001, 4:49–5:7 (spacing added to aid readability).

E. The Asserted Grounds of Unpatentability

Petitioner asserts the following grounds of unpatentability (Pet. 5–6)

Claims Challenged	35 U.S.C. §³	Reference(s)/Basis
1–9, 12–14, 16–21, 23–28	103(a)	Kawagoe ⁴
1–2, 4–9, 12–23, 25–28	103(a)	Wieczorek ⁵ , Wolf ⁶
1–9, 12–14, 16–21, 23–28	103(a)	Kawagoe, Gupta ⁷
1–2, 4–9, 12–23, 25–28	103(a)	Wieczorek, Wolf, Gupta
19	103(a)	Kawagoe, Silverbrook ⁸
19	103(a)	Wieczorek, Wolf, Silverbrook

The Petition is supported by the declaration of Dr. Sanjay Banerjee.

Ex. 1003.

³ The Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112–29, took effect on March 16, 2013. The ’014 patent claims priority to an application filed September 3, 2004. Ex. 1001, code (60). Thus, we apply the pre-AIA version of §103. See Pet. 5 n.1.

⁴ US 6,043,114, issued Mar. 28, 2000 (Ex. 1007).

⁵ US 2003/0183856 A1, published Oct. 2, 2003 (Ex. 1006).

⁶ Stanley Wolf & Richard N. Tauber, *Silicon Processing for the VLSI Era*, Vols. 1–4 (Lattice Press 2000) (Ex. 1008).

⁷ US 6,163,877, issued Dec. 19, 2000 (Ex. 1014).

⁸ US 6,614,560 B1, issued Sept. 2, 2003 (Ex. 1046).

II. TIMELINESS OF THE PETITION UNDER 35 U.S.C. § 315(B)

Pursuant to 35 U.S.C. § 315(b), “[a]n inter partes review may not be instituted if the petition requesting the proceeding is filed more than 1 year after the date on which the petitioner, real party in interest, or privy of the petitioner is served with a complaint alleging infringement of the patent.” Patent Owner argues that the Petition is untimely under 35 U.S.C. § 315(b) because Petitioner is in privity with time-barred entities. Prelim. Resp. 15–35. The one-year time bar under § 315(b), however, “shall not apply to a request for joinder under subsection (c).” 35 U.S.C. § 315(b); *see* 37 C.F.R. § 42.122(b). And, because the Petition is accompanied by a timely request for joinder (Paper 1) to the instituted proceeding (IPR2024-00019), which we grant as further discussed below, Patent Owner’s argument that the Petition is time-barred under 35 U.S.C. § 315(b) is moot, irrespective of whether Petitioner is in privity with time-barred entities.

III. MOTION FOR JOINDER

A party in an *inter partes* review may be joined as a party in another *inter partes* review, subject to certain statutory provisions:

(c) JOINDER.—If the Director institutes an inter partes review, the Director, in his or her discretion, may join as a party to that inter partes review any person who properly files a petition under section 311 that the Director, after receiving a preliminary response under section 313 or the expiration of the time for filing such a response, determines warrants the institution of an inter partes review under section 314.

35 U.S.C. § 315(c); *see also* 37 C.F.R. § 42.122 (“Any request for joinder must be filed, as a motion under § 42.22, no later than one month after the institution date of any *inter partes* review for which joinder is requested.”). To join a party to an instituted *inter partes* review, “the plain language of

§ 315(c) requires two different decisions.” *Facebook, Inc. v. Windy City Innovations, LLC*, 973 F.3d 1321, 1332 (Fed. Cir. 2020). “First, the statute requires that the Director (or the Board acting through a delegation of authority) . . . determine whether the joinder applicant’s petition for IPR ‘warrants’ institution under § 314.” *Id.* “Second, to effect joinder, § 315(c) requires the Director to exercise . . . discretion to decide whether to ‘join as a party’ the joinder applicant.” *Id.* (“That is, the statute requires the Director (or the Board on behalf of the Director) to make a “joinder decision.”).

A. Whether the Petition Warrants Institution

Petitioner argues that its Petition challenges the same claims of the same patent on the same grounds and prior art as those before the Board in the Cirrus IPR. Mot. 1 (noting that the present Petition “includes the exact same substantive arguments as the Cirrus IPR”). Petitioner further argues that the “supporting materials” cited in the Petition—including the “supporting expert declaration, exhibits, and exhibit numbering—are identical to those presented in the Cirrus IPR.” *Id.* at 6 (citing IPR2024-00019, Paper 1).

Because the Preliminary Response in the instant case includes arguments pertaining to the sufficiency of the asserted prior art references, which were not raised in the preliminary response in the Cirrus IPR, we briefly address below the patentability of the challenged claims.

1. Overview of the Challenges

The Petition challenges the patentability of claim 1–9 and 12–28 of the ’014 patent. Pet. 5–6. Each challenge identified in the Petition is based

on Kawagoe or Wieczorek, either alone (Kawagoe) or in combination with other references (both the Kawagoe and Wieczorek-based grounds). *Id.*

Patent Owner does not challenge the sufficiency of the evidence asserted in the Petition to support institution of review, except to argue that the prior art does not teach or suggest the “aid carrier movement” limitations of independent claims 1 and 21. Prelim. Resp. 4–14.

2. *Kawagoe*

Kawagoe discloses a process for manufacturing a semiconductor integrated circuit device using an epitaxial wafer, i.e., a semiconductor wafer having a semiconductor single crystal epitaxial layer grown over a polished semiconductor substrate. Ex. 1007, 1:13–27, 2:31–35. According to Kawagoe, “[t]he epitaxial wafer is advantageous in that it is excellent in suppressing the soft errors and resisting to the latchup,”⁹ and also has “excellent breakdown characteristics” that “drastically reduce the defect density of the gate insulating film” of a semiconductor integrated device. *Id.* at 1:33–40.

Kawagoe discloses various “representative” processes, including processes in which the single crystal (epitaxial) layer contains an impurity of the same type and in the same concentration as the substrate body.

⁹ Petitioner submits Exhibit 1009 (Wang and Agrawal, *Single Event Upset: An Embedded Tutorial*, 21st Int’l Conf on VLSI Design, 429–434, IEEE 2008), which explains that “soft errors” are “random and not related to permanent hardware faults” and “[t]heir causes may be internal (e.g., interconnect coupling) or external (e.g., cosmic radiation),” including “alpha particles [that] are emitted when the nucleus of an unstable isotope decays to a lower energy state.” Ex. 1009, Abstract, 430. Dr. Banerjee characterizes “latchup” as “a ‘short-circuit’ failure condition in poorly designed circuits.” Ex. 1003 ¶ 77.

Ex. 1007, 2:55–3:9. According to Kawagoe, the impurity concentration of the substrate body can be made higher than that of the epitaxial layer “so that the resistance of the semiconductor substrate body can be relatively lowered to improve the resistance to the latchup.” *Id.* at 4:1–8. Kawagoe discloses a process for manufacturing a semiconductor integrated circuit device including a step of forming a semiconductor region (well) extending below the epitaxial layer and having an impurity concentration that decreases with increasing depth below the epitaxial layer. *Id.* at 3:10–25. According to Kawagoe, the well can be used for forming a complementary Metal-Oxide-Semiconductor Field-Effect Transistor (“MOS.FET”) circuit. *Id.* at 3:32–38.

Kawagoe describes seven embodiments, including Embodiment 1 (Ex. 1007, 6:41–12:40, Figs. 1–8) and Embodiment 4 (*id.* at 14:46–19:63, Figs. 16–25). Figure 1, reproduced below, depicts the device of Embodiment 1.

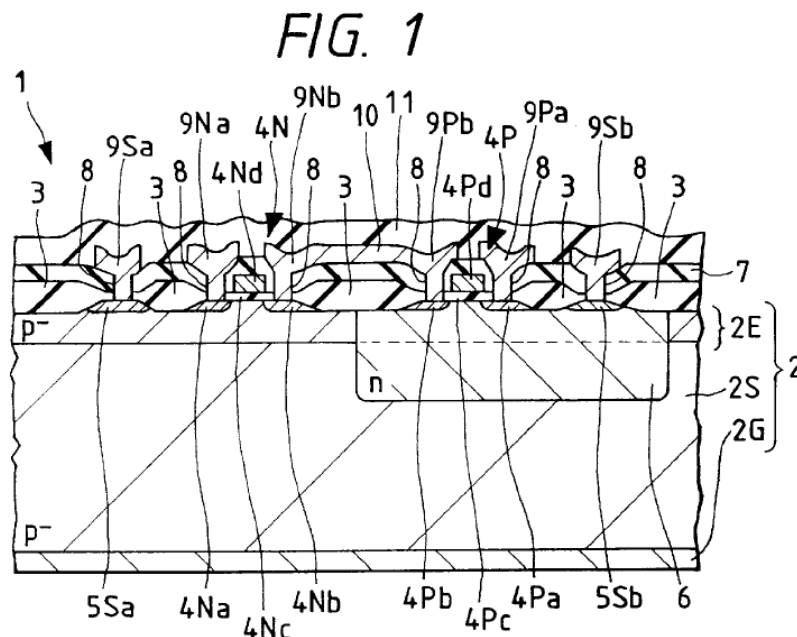


Figure 1 depicts “an essential portion of a semiconductor integrated circuit device” that includes semiconductor substrate body 2S, epitaxial layer 2E, and gettering layer 2G. *Id.* at 6:51–56, Fig. 1. Substrate body 2S and epitaxial layer 2E are doped with a p-type impurity in equal concentrations. *Id.* at 6:60–7:3, 10:51–55, 11:12–16. Embodiment 1 includes n-channel MOS.FET (“nMOS”) 4N and p-channel MOS.FET (“pMOS”) 4P, the latter being formed in n-well 6, which is doped with n-type impurity and extends below the epitaxial layer. *Id.* at 8:46–52, 9:32–40, 11:18–24, 11:43–50, Figs. 1, 5, 7.

Figure 23, reproduced below, depicts a semiconductor device of Embodiment 4 in the process of manufacture. *Id.* at 17:11–13.

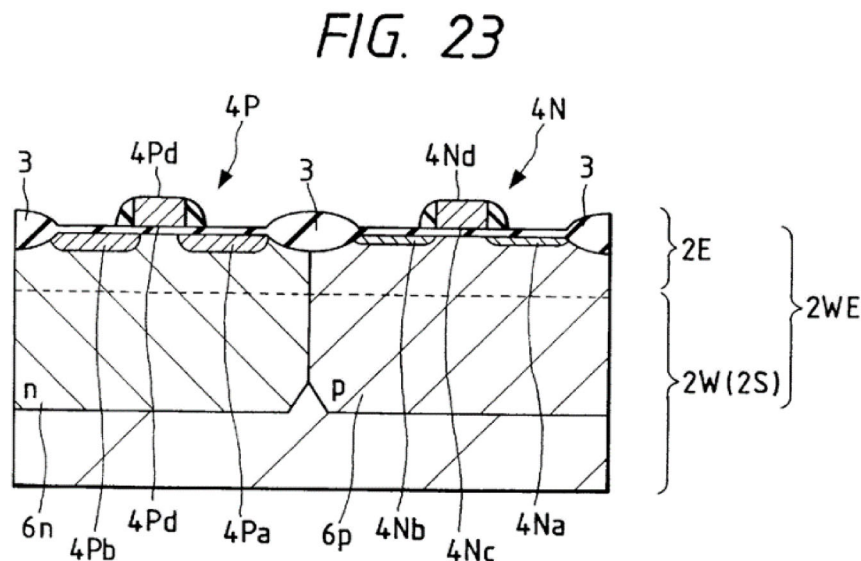


Figure 23 shows a step in a process for manufacturing the semiconductor integrated circuit device of Embodiment 4, including p-well 6p formed with nMOS 4N and n-well 6n formed with pMOS 4P. *Id.* at 6:1–4, 15:26–32, 18:3–35. Substrate body 2S and epitaxial layer 2E are doped with p-type impurity, and the impurity concentration of substrate body 2S is higher than that of epitaxial layer 2E “to improve the resistance to the latchup.” *Id.* at

14:64–15:6, 15:13–17, 16:16–21, 19:59–63, Fig. 17. In Embodiment 4, the impurity concentration in p-well 6p and n-well 6n decreases with increasing depth below the epitaxial layer. *Id.* at 15:62–16:15, 17:55–61, Fig. 17.

Kawagoe discloses that the concentration gradient reduces soft errors by attracting carriers (electrons) to the substrate and preventing them from entering the p-well. *Id.* at 16:2–11.

Petitioner relies on Kawagoe Figure 17, which is reproduced below and illustrates properties of the semiconductor device of Embodiment 4.

FIG. 17

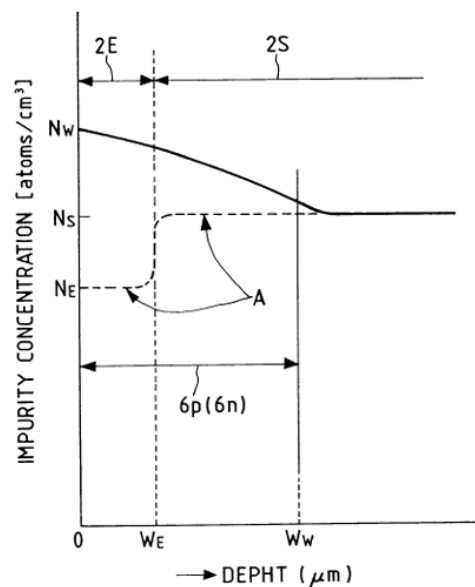
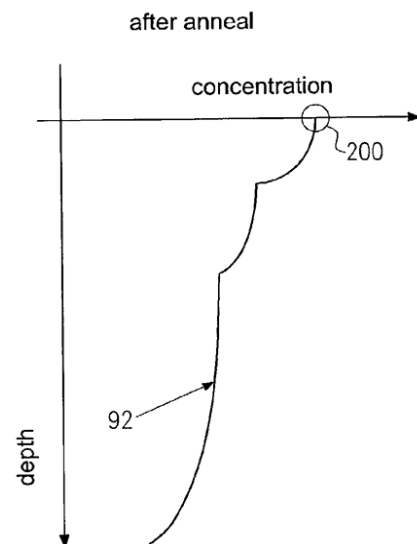
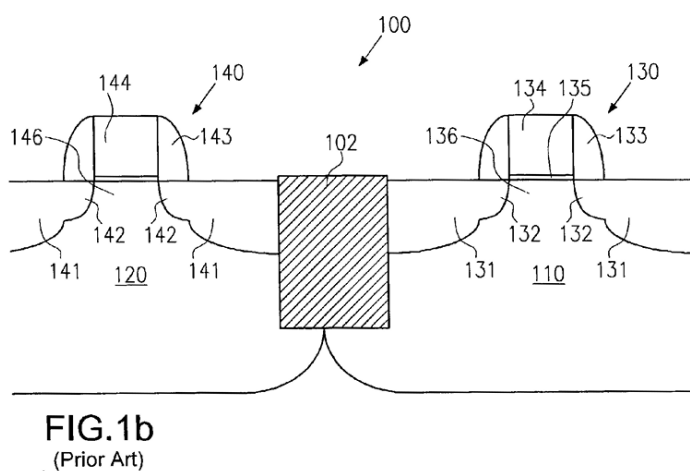


Figure 17 is a plot of impurity concentration as a function of depth in a semiconductor integrated circuit device, which shows “the p-well 6*p* and n-well 6*n* have their impurity concentrations gradually lowered in the depthwise direction from the principal surface (having an impurity concentration N_w) of the epitaxial layer 2E.” Ex. 1007, 5:41–45, 15:62–16:40.

3. *Wieczorek*

Wieczorek relates “to a semiconductor device, such as a field-effect transistor, having an improved retrograde dopant profile in a channel region of the transistor element.” Ex. 1006 ¶ 2. Wieczorek explains that a retrograde channel dopant profile is one where “the concentration of dopants increases from the gate insulation layer to the areas located deeper down the channel region.” *Id.* ¶ 6. According to Wieczorek, although a retrograde channel dopant profile is desirable, it is “very difficult to obtain.” *Id.* Wieczorek notes that “the dopant concentration immediately after the implantation process exhibits a desired retrograde dopant profile” (*id.* ¶ 9), but during heat treatment, “the initially retrograde profile in the vicinity of the surface of the semiconductor device . . . may have become substantially uniformly distributed” due to diffusion of the dopant atoms (*id.* ¶ 11).

Petitioner relies on Figures 1b and 2b (reproduced below), which Wieczorek uses to illustrate the prior art.



Wieczorek Figure 1b shows a conventional semiconductor device at an advanced manufacturing stage. Ex. 1006 ¶¶ 12, 20. The device includes P-channel transistor 140 with source and drain regions 141 in N-well structure 120 and N-channel transistor 130 with source and drain regions 131 in P-well structure 110. *Id.* ¶ 12. Shallow trench isolation 102 separates N-well structure 120 from P-well structure 110. *Id.* ¶ 7. Wieczorek Figure 2b is a graph of dopant concentration versus depth of N-well structure 120 and P-well structure 110 and shows “a typical dopant profile with respect to the depth of the respective well structure” after ion implantation and heat treatment. *Id.* ¶¶ 9–11, 13, 21.

4. *Undisputed Claim Limitations*

Patent Owner does not contest the sufficiency of the evidence to support institution of review, except to argue that Petitioner does not show sufficiently that the asserted prior art teaches or suggests the limitations directed to “aid carrier movement.” Prelim. Resp. 4–14. Accordingly, for the same reasons stated in our decision instituting review in the Cirrus IPR, we find Petitioner shows sufficiently that the prior art teaches or suggests each of the other limitations of claims 1–9 and 12–28.

5. *“aid carrier movement”*

Independent claims 1 and 21 each require a graded dopant concentration “to aid carrier movement” from either active regions or a surface to the substrate “where there are no active areas.” Ex. 1001, 4:63–5, 6:21–30. Patent Owner argues that “the Petition fails to show that any of the primary references disclose any of the claim elements requiring ‘aid carrier movement.’” Prelim. Resp. 8. Patent Owner summarizes this dispute as follows:

The challenged patent discloses and claims a semiconductor device with (among other things) a “graded dopant concentration to *aid carrier movement*.” The Petition should not be instituted, because (among other deficiencies) it fails to show that the prior art discloses the “aid carrier movement” claim limitation.

Rather than pointing to anything in the prior art that would teach this claim limitation, the Petition assumes that *any* “graded dopant concentration” would *necessarily* “aid carrier movement.” The Petition contains no analysis explaining why the “graded dopant concentration[s]” in the prior art meet the “aid carrier movement” limitation, apart from the fact that they *are* “graded dopant concentration[s].” In other words, Petitioner reads the “aid carrier movement” limitation out of the claims completely.

Id. at 1. Patent Owner includes additional details in support of its view that the asserted prior art fails to establish obviousness of the “aid carrier movement” limitation of claim 1. *Id.* at 4–14. Of particular significance, Patent Owner contends Cirrus Logic’s declarant admitted during cross-examination that “the existence of a gradient alone is not enough to determine whether the gradient would ‘aid carrier movement.’” *Id.* at 9 (citing Ex. 2022, 95:2–96:13).

Patent Owner raises similar, if not identical, arguments in the Cirrus IPR. *Compare id.*, with IPR2024-00019, Paper 46 at 1–4, 6–22 (Patent Owner’s response in the Cirrus IPR) (public version). We decline to resolve the material issue of fact surrounding this limitation on this preliminary record, because the trial in the Cirrus IPR is the better proceeding in which to do so. Specifically, as compared to the preliminary phase of this case, the instituted trial in the Cirrus IPR affords the parties a better opportunity to fully and fairly brief, argue, and develop evidence in support of their

positions, and, in particular, to address Cirrus Logic’s alleged admission that the existence of a gradient alone is insufficient to disclose the “aid carrier movement” limitations of independent claims 1 and 21. We observe only that, on this record, the disputed issue of material fact is not sufficient to undermine the sufficiency of Petitioner’s evidence supporting institution of review.

B. Whether to Join Petitioner as a Party to the Cirrus IPR

Joinder may be authorized when warranted, but the decision to grant joinder is discretionary. *See* 35 U.S.C. § 315(c); 37 C.F.R. § 42.122.

A motion for joinder should (1) set forth reasons why joinder is appropriate; (2) identify any new grounds of unpatentability asserted in the petition; (3) explain what impact (if any) joinder would have on the trial schedule for the existing review; and (4) address specifically how briefing and discovery may be simplified. *See, e.g., Kyocera Corp. v. Softview LLC*, IPR2013-00004, Paper 15 (PTAB April 24, 2013). As the moving party, Petitioner bears the burden of proving that it is entitled to the requested relief.

37 C.F.R. § 42.20(c).

As an initial matter, we find the Motion for Joinder meets the timing requirements of 37 C.F.R. § 42.122(b) because Petitioner filed it on April 10, 2024, no later than one month after the Cirrus IPR was instituted on May 3, 2024.

Petitioner asserts that the four *Kyocera* factors favor joinder here. Mot. 3 (addressing the *Kyocera* factors as recited in *Dell, Inc. v. Network-1 Security Sols., Inc.*, IPR2013-00385, Paper 17 at 3 (PTAB July 29, 2013)). In particular, Petitioner explains that joinder will have no impact on the pending schedule because Petitioner will “take an understudy role” in which

it “will not seek additional depositions or deposition time,” Petitioner “agrees to be bound by the scheduling order in the Cirrus IPR proceeding,” and Petitioner “agrees to rely entirely on, and be bound by, the expert declarations and depositions in the Cirrus IPR” unless the current petitioner in that proceeding “ceases to participate.” *Id.* at 4–8.

Petitioner (referring to itself as “TI”) also agrees that:

(a) TI shall not make any substantive filing and shall be bound by the filings of the Cirrus IPR Petitioner, unless a filing concerns termination and settlement, or issues solely involving TI;

(b) TI shall not present any argument or make any presentation at oral hearing unless an issue solely involves TI, or when addressing Board-approved motions that do not affect the Cirrus IPR Petitioner, or its respective position;

(c) TI shall not seek to cross-examine or defend the cross-examination of any witness, unless the topic of cross-examination concerns issues solely involving TI;

(d) TI shall not seek discovery from Patent Owner on issues not solely involving TI; [and]

(e) TI will not rely on expert testimony beyond that submitted by the Cirrus IPR Petitioner unless the Cirrus IPR Petitioner is terminated from the case.

Id. at 7. Petitioner “will also abide by any additional conditions the Board deems appropriate for an ‘understudy’ role.” *Id.* at 8.

Patent Owner argues that the Motion for Joinder should be denied because joinder would be prejudicial to Patent Owner and contrary to public policy favoring settlement, and Patent Owner’s Preliminary Response related to Petitioner might address issues never addressed in IPR2024-00019, including the timeliness of the current Petition or the “*Fintiv*” factors. Opp. 3–5. Patent Owner also argues that joinder is unavailable if Patent

Owner prevails on a request for Director Review of the Decision on Institution in the Cirrus IPR. *Id.* at 5–7.

Patent Owner’s arguments are not persuasive. First, the timeliness of the current Petition is moot, in view of Petitioner’s timely-filed motion for joinder. Second, contrary to Patent Owner’s arguments, the Preliminary Response does not raise “*Fintiv*” issues. Third, Patent Owner’s public policy arguments are not persuasive because they are based on speculation that Petitioner “is trying to block settlement with *any* of these defendants unless [Patent Owner] *also* settles with” Petitioner. Opp. 5. Moreover, even in a situation where the petitioner and patent owner in the proceeding to be joined had settled (*Code200 v. Bright Data Ltd.*, IPR2022-00861, Paper 17 at 5 (PTAB July 25, 2022) (vacated)), the Director nevertheless vacated a decision to deny a motion for joinder. *Code200 v. Bright Data Ltd.*, IPR2022-00861, Paper 18 at 7 (Vidal Aug. 23, 2022) (precedential); *see also eBay, Inc. v. Lexos Media IP, LLC*, IPR2024-00336, Paper 11 at 13–15 (PTAB Feb. 23, 2024). Finally, Patent Owner’s argument based on the request for Director Review of the institution decision in the Cirrus IPR is moot because Patent Owner’s Request for Director Review was denied. *See* IPR2024-00019, Paper 34 (May 30, 2024).

Based on the facts and circumstances discussed above, we determine Petitioner has established good cause for joining the Cirrus IPR. Specifically, we find that joining Petitioner to the Cirrus IPR is unlikely to require any delay or modification to the scheduling order already in place for that proceeding. We also determine that Patent Owner will not be prejudiced unduly by the joinder of this proceeding. Thus, we determine

that granting the Motion for Joinder would help “secure the just, speedy, and inexpensive resolution” of these proceedings. *See* 37 C.F.R. § 42.1(b). Accordingly, we grant Petitioner’s Motion for Joinder and join Petitioner as a party to the Cirrus IPR.

IV. CONCLUSION

For the above reasons, we determine that there is a reasonable likelihood that Petitioner would prevail with respect to at least one of the claims challenged in the Petition. Accordingly, we institute an *inter partes* review of all challenged claims based on the grounds asserted in the Petition. In addition, we grant Petitioner’s Motion for Joinder. Patent Owner’s argument that the Petition is time-barred under 35 U.S.C. § 315(b) is moot because it is accompanied by a request for joinder to an instituted proceeding, which we grant.

V. ORDER

It is

ORDERED that, pursuant to 35 U.S.C. § 314(a), an *inter partes* review of the ’014 patent is hereby instituted, commencing on the entry date of this Order, and pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial;

FURTHER ORDERED that the trial is authorized on all grounds set forth in the Petition;

FURTHER ORDERED that Petitioner’s Motion for Joinder with IPR2024-00019 is granted, and Petitioner is hereby joined as a petitioner in IPR2024-00019;

FURTHER ORDERED that there are no changes to the grounds on which trial in IPR2024-00019 was instituted, and no other grounds are added in IPR2024-00019;

FURTHER ORDERED that the Scheduling Order entered in IPR2024-00019, including any schedule changes agreed to by the parties in that proceeding pursuant to the Scheduling Order, shall govern the trial schedule in IPR2024-00019;

FURTHER ORDERED that Petitioner's role in IPR2024-00019 shall be limited as stated by Petitioner in the Motion for Joinder unless and until Cirrus Logic and OmniVision are terminated from that proceeding;

FURTHER ORDERED that the case caption in IPR2024-00019 shall be changed to reflect joinder of Texas Instruments Incorporated as a petitioner in accordance with the attached example;

FURTHER ORDERED that a copy of this Decision shall be entered into the record of IPR2024-00019; and

FURTHER ORDERED that all further filings shall be made in IPR2024-00019.

IPR2024-00774
Patent 11,316,014 B2

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IPR2024-00774
Patent 11,316,014 B2

[Sample Case Caption]

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

CIRRUS LOGIC, INC.;
OMNIVISION TECHNOLOGIES, INC.; and
TEXAS INSTRUMENTS INCORPORATED,
Petitioner,

v.

GREENTHREAD, LLC,
Patent Owner.

IPR2024-00019*
Patent 11,316,014 B2

* Texas Instruments Inc., which filed a petition in IPR2024-00774, has been joined as a party to this proceeding.