IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

CIRRUS LOGIC, INC.;
OMNIVISION TECHNOLOGIES, INC.; AND
TEXAS INSTRUMENTS INCORPORATED,
Petitioner,

v.

GREENTHREAD, LLC,
Patent Owner.

Case No. IPR2024-00019[1]
Patent No. 11,316,014

PETITIONER'S UPDATED EXHIBIT LIST

[1] Texas Instruments Incorporated, which filed a petition in IPR2024-00774, has been joined as a party to this proceeding.

UPDATED TABLE OF EXHIBITS

Exhibit	Description
1001	U.S. Patent No. 11,316,014 to Rao (the "'014 Patent")
1002	Prosecution History of the '014 Patent
1003	Declaration of Sanjay Banerjee, PhD
1004	Curriculum Vitae of Sanjay Banerjee, PhD
1005	Publication Declaration of Sean O'Bryan for Maziasz ("O'Bryan Decl.")
1006	U.S. Patent Application Publication No. 2003/0183856 to Wieczorek ("Wieczorek")
1007	U.S. Patent No. 6,043,114 to Kawagoe, et al. ("Kawagoe")
1008A	Wolf and Tauber, *Silicon Processing For The VLSI Era*, Vol 1, Lattice Press (2000) ("Wolf.1")
1008B	Wolf and Tauber, *Silicon Processing For The VLSI Era*, Vol. 2, Lattice Press (2000) ("Wolf.2")
1008C	Wolf and Tauber, *Silicon Processing For The VLSI Era*, Vol. 3, Lattice Press (2000) ("Wolf.3")
1008D	Wolf and Tauber, *Silicon Processing For The VLSI Era*, Vol. 4, Lattice Press (2000) ("Wolf.4")
1009	Wang and Agrawal, *Single Event Upset: An Embedded Tutorial*, 21st Intl Conf on VLSI Design, IEEE 2008 ("Wang")
1010	U.S. Patent No. 4,481,522 ("Jastrzebski")
1011	Publication Declaration of Martin L. Knott for Rabaey ("Knott-Rabaey Decl.")
1012	Publication Declaration of Alyssa G. Resnick for Wolf.1 and Wolf.2 ("Resnick Decl.")
1013	Publication Declaration of Rachel J. Watters for Wolf.3 and Wolf.4 ("Watters Decl.")
1014	U.S. Patent No. 6,163,877 ("Gupta")
1015	U.S. Patent No. 6,534,805 ("Jin")
1016	Excerpts from the Prosecution History of U.S. Patent No. 8,421,195 (the "'195 Patent")
1017	Patent Owner's Proposed Constructions
1018	Blank
1019	Blank
1020	Patent Owner's Responsive Claim Construction Brief
1021	Blank

Exhibit	Description
1022	Sze, *Semiconductor Devices Physics and Technology*, 2d Ed., John Wiley & Sons (2002)
1023	Maziasz and Hayes, *Layout Minimization of CMOS Cells*, Kluwer Academic Publishers (1992) ("Maziasz")
1024	U.S. District Courts – Case Statistics, obtained at https://www.uscourts.gov/statistics-reports/analysis- reports/ federal-court-management-statistics, dated June 30, 2023
1025	*Rabaey et al., Digital Integrated Circuits, A Design Perspective*, Prentice Hall Electronics and VLSI Series (2003) ("Rabaey")
1026	Gregory and Shafer, "Latch-Up In CMOS Integrated Circuits," IEEE Transactions on Nuclear Science, Volume 20, Issue 6 (1973)
1027	U.S. Patent Application Publication No. 2007/0045682 to Hong *et al.* ("Hong")
1028	Excerpts from the Prosecution History of U.S. Patent Application Publication No. 10/934,915 (the "'915 App.")
1029	Excerpts from the Prosecution History of U.S. Patent No. 9,190,502 (the "'502 Patent")
1030	Excerpts from the Prosecution History of U.S. Patent Application Publication No. 13/854,319 (the "'319 App.")
1031	U.S. Patent No. 4,160,985 to Kamins *et al*. ("Kamins")
1032	McGraw-Hill Dictionary of Scientific and Technical Terms (2003)
1033	U.S. Patent No. 9,647,070 to Rao (the "'070 Patent")
1034	U.S. Patent Application Publication No. 2003/0030488 to Hueting *et al.* ("Hueting")
1035	Blank
1036	Proposed Claim Constructions in the District Court Case
1037	Howe and Sodini, *Microelectronics, An Integrated Approach*, Prentice Hall Electronics and VLSI Series (1997) ("Howe")
1038	Hodges *et al.*, *Analysis and Design of Digital Integrated Circuits In Deep Submicron Technology,* 3rd Ed., McGraw-Hill (2004) ("Hodges")
1039	Publication Declaration of Martin L. Knott for Hodges ("Knott-Hodges Decl.")
1040	Jaeger, *Microelectronic Circuit Design*, McGraw-Hill (1997) ("Jaeger")

Exhibit	Description
1041	Kang and Leblebici, *CMOS Digital Integrated Circuits Analysis and Design*, McGraw-Hill (2003) ("Kang")
1042	Redacted District Court Case Transfer Order
1043	Publication Declaration of Sylvia Hall-Ellis for Wolf
1044	Dec. 21, 2022 Preliminary Claim Constructions in 6:22-CV-00105
1045	Oct. 31, 2022 Giapis Declaration, 6:22-CV-00105
1046	U.S. Patent No. 6,614,560 to Silverbrook ("Silverbrook")
1047	Wong et al., "*CMOS Active Pixel Image Sensors Fabricated Using a 1.8V, 0.25 um CMOS Technology*."
1048	Email dated December 22, 2023
1049	Blank
1050	Blank
1051	Blank
1052	Blank
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1056	Blank
1057	Blank
1058	Blank
1059	Blank
1060	Supplemental Declaration of Sanjay Banerjee, PhD
1061	Sze, Semiconductor Devices: Physics and Technology, Second Edition 1985, excerpted ("Sze")
1062	Streetman and Banerjee, Solid State Electronic Devices, Sixth Edition 2006, excerpted ("Streetman")
1063	Deposition Transcript of Alexander Glew, Ph.D., P.E., taken on Oct. 16, 2024
1064	Declaration of Douglas Holberg in Application No. 17/728,588 (Aug. 1, 2024)
1065	R. C. Baumann, *Soft Errors in Commercial Integrated Circuits*, 14(2) Int'l J. High Speed Elect. & Sys. 299-399 (2004)
1066	Confidential Deposition Transcript of Mohan Rao, Ph.D., taken on Oct. 23, 2024
1067	RPX Rational Patent FAQs
1068	A. S. Grove, *Physics and Technology of Semiconductor Devices*, excerpted (1067)

Exhibit	Description
1069	Deposition Transcript of Alexander Glew, Ph.D., P.E., taken on July 16, 2024
1070	Amendment and Response to Office Action in Application No. 17/728,588 (Aug. 1, 2024)
1071	Wolf Vol. 2 Supplement
1072	Petitioner's Hearing Demonstratives
1073	Telephonic Conference Call Transcript, taken on May 2, 2025 (Confidential)
1074	Telephonic Conference Call Transcript, taken on May 2, 2025 (Redacted – Public Version)
1075	Declaration of Hyun S. Byun in Support of Petitioner's Notice of Intent to Designate Hyun S. Byun as Back-up Counsel under 37 C.F.R. § 42.10

Respectfully submitted,

Dated: September 3, 2025

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CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6, I hereby certify that the foregoing Updated Exhibit List, were served on the Patent Owner by electronic mail to the following counsel of record for Patent Owner:

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