UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

CIRRUS LOGIC, INC. and
OMNIVISION TECHNOLOGIES, INC.
Petitioners,

v.

GREENTHREAD, LLC,
Patent Owner.

Case IPR2024-00020
U.S. Patent 11,121,222

DECLARATION OF ALEXANDER D. GLEW

TABLE OF CONTENTS

I. INTRODUCTION 1

II. BACKGROUND AND QUALIFICATIONS 3

III. SCOPE OF ASSIGNMENT AND MATERIALS CONSIDERED 7

IV. LEVEL OF ORDINARY SKILL IN THE ART 9

V. RELEVANT LEGAL PRINCIPLES 10

A. Claim Construction 10

B. Anticipation 12

C. Obviousness 12

VI. THE CHALLENGED PATENT 14

A. Background Technology Regarding Dopants 14

B. Overview of Challenged Patent 14

VII. OVERVIEW OF ALLEGED PRIOR ART 19

A. Kawagoe (Ex. 1007) 19

B. Wieczorek (Ex. 1006) 22

VIII. CLAIM CONSTRUCTION 25

IX. THE CITED REFERENCES DO NOT DISCLOSE OR SUGGEST ALL THE FEATURES OF THE CHALLENGED CLAIMS 26

A. Dr. Banerjee's Kawagoe-based analysis is incorrect regarding the "aid carrier movement…" limitations (Elements [1.5], [1.6], [21.5], [21.6], [39.5], [41.5], [42.5]). 26

B. Dr. Banerjee's Wieczorek-based analysis is incorrect regarding the "aid carrier movement…" limitations (Elements [1.5]/[21.5]/[39.5]/[41.5]/[42.5] and [1.6]/[21.6]). 35

C. Dr. Banerjee's Kawagoe-based analysis is incorrect regarding the "first active region … with a second doping type opposite in conductivity to the first doping type" limitation (Elements [1.2]/[21.2]/[39.2]/[41.2]/[42.2]).....36

D. Dr. Banerjee's Kawagoe-based analysis is incorrect regarding the "first active region and second active region are each separated by at least one isolation region" limitation (Dependent claims 6 and 27).....38

X. CONCLUSION.....41

I, Alexander D. Glew, declare as follows:

I. INTRODUCTION

1. My name is Alexander D. Glew. I have been retained on behalf of Greenthread, LLC ("Greenthread"), and its counsel, McKool Smith, P.C., as an expert with regard to this matter. I understand Cirrus Logic, Inc. ("Cirrus"), OmniVision Technologies, Inc. ("OmniVision"), and ams Sensors USA, Inc. ("ams") (collectively, "Petitioner") filed a Petition (Paper No. 1) for *inter partes* review (IPR) of U.S. Patent No. 11,121,222 ("the '222 patent" or "the Challenged Patent") (Ex. 1001).

2. I have been asked to consider, and provide my independent analysis and opinions regarding, whether the alleged prior art references cited in this proceeding disclose or suggest the features recited in claims 1-9, 12-28, and 31-42 ("the Challenged Claims") of the Challenged Patent, which I understand Petitioner has challenged in this IPR. In my view, the alleged prior art references do neither. My opinions and conclusions are fully discussed in later sections of this declaration. This declaration is based on the information currently available to me.

3. I am an independent consultant, and I am not, and have never been, an employee of Greenthread or Petitioner. I am being compensated at my consulting rate of $700 per hour for my work related to this matter. I received no compensation

for this declaration beyond my normal hourly compensation based on my time actually spent analyzing the Challenged Patent, the prosecution history of the Challenged Patent and related applications, the alleged prior art publications relied upon by Petitioner, the declaration of Petitioner's expert Dr. Sanjay Banerjee, and other related materials (discussed below in Section III). My compensation is not dependent on the outcome of this IPR or the testimony or opinions that I give.

4. I understand a copy of my curriculum vitae is submitted as Ex. 2061, and it sets forth my educational experience, employment history, and publications.

II. BACKGROUND AND QUALIFICATIONS

5. I earned a B.S. degree in Mechanical Engineering in 1985 and a M.S. degree in Mechanical Engineering in 1987 from the University of California, Berkeley.

6. I earned a M.S. degree in Materials Science and Engineering in 1995 and a Ph.D. in Materials Science and Engineering in 2003 from Stanford University.

7. I am the Founder and President of Glew Engineering Consulting, Inc., based in Mountain View, California. I have been President of Glew Engineering Consulting, Inc. since I started the company in 1997. In my role as President, I have provided consulting services to clients in the field of semiconductor manufacturing and materials, as well as to clients in other fields. I have reviewed and analyzed semiconductor technologies and products. My consulting work has involved semiconductor process equipment, thin film deposition and characterization, process development, project turnaround/rescue, gas flow and vacuum metrology, design of experiments, corrosive gas applications, finite element analysis, and related market analysis.

8. I have over 30 years of experience in semiconductor manufacturing and materials, including in semiconductor equipment and processing. I have implemented numerous manufacturing processes for the formation of semiconductors, including chemical vapor deposition ("CVD"), plasma enhanced

chemical vapor deposition ("PECVD"), high density plasma chemical vapor deposition ("HDPCVD"), etch processing (including dry plasma and wet processing), reactive-ion etching ("RIE"), chemical-mechanical planarization ("CMP"), spin-on dielectrics ("SOD"), epitaxy ("EPI"), molecular beam epitaxy ("MBE"), rapid thermal processing ("RTP"), and others.

9. In 1987, before receiving my Ph.D., I worked at Applied Materials, Inc. in Santa Clara, California. At Applied Materials, Inc., I served in a number of roles, including Engineering Manager, Core-Technologist Project Manager, CVD Supplier Quality Engineering Manager, Core Technologist, CVD Engineering Manager, and Systems Engineer. In these roles, I provided engineering services and supervised other employees on projects related to technologies used to manufacture semiconductors, including CVD, epitaxy, physical vapor deposition ("PVD"), rapid thermal processing ("RTP"), etch, and thermal. I oversaw gas, vacuum, and chemical component evaluation, testing, and supplier quality management. I successfully proposed and executed a project to develop industry methods to determine the effects of trace chemicals on semiconductor processing and equipment reliability. I worked on the development and release of the Precision 5000 CVD product, the first cluster tool for semiconductor manufacturing.

10. I have used alpha particles to perform hydrogen forward scattering (HFS) and Rutherford Back Scattering (RBS) in materials analysis of thin films on

silicon wafers. I am generally familiar with the effects of alpha particles fired at silicon wafers.

11. I am a licensed professional mechanical engineer in the state of California.

12. I have published articles and presented on topics related to semiconductor manufacturing. My curriculum vitae includes a list of selected publications.

13. I am a co-inventor of five U.S. patents: (a) U.S. Patent No. 6,204,174, directed to a method and apparatus to control the deposition rate of material in a semiconductor fabrication process; (b) U.S. Patent No. 9,224,626 and 10,395,593, directed to a method of forming a heater assembly for use in semiconductor processing; and (c) U.S. Patent Nos. 6,679,476 and 7,118,090, both directed to control valves for use in ultra pure applications such as semiconductor processing. I have another patent application pending.

14. I am a member of the American Society of Mechanical Engineers ("ASME"), International Microelectronics and Packaging Society ("IMAPS"), Materials Research Society ("MRS"), Institute of Electrical and Electronics Engineers ("IEEE"), and Semiconductor Equipment and Materials International ("SEMI").

15. I am qualified to render an opinion regarding the design and development of semiconductor manufacturing devices and semiconductor materials based on my experience. Based on my expertise and qualifications, I am qualified to provide an opinion as to what a person of ordinary skill in the art would have understood, known, or concluded as of 2004.

III. SCOPE OF ASSIGNMENT AND MATERIALS CONSIDERED

16. The opinions contained in this declaration are based on the documents that I reviewed, my professional judgment, as well as my education, experience, and knowledge regarding technologies related to the Challenged Patent. In preparing this Declaration, I am relying on my own knowledge and expertise as well as the following documents:

- The Challenged Patent (Ex. 1001);
- Other patents that I understand are in the same family as the Challenged Patent, including:
    - U.S. Patent No. 8,421,195 to Dr. G.R. Mohan Rao ("the '195 patent) (Ex. 2062)
    - U.S. Patent No. 9,190,502 to Dr. G.R. Mohan Rao ("the '502 patent") (Ex. 2063);
    - U.S. Patent No. 10,510,842 to Dr. G.R. Mohan Rao ("the '842 patent") (Ex. 2064);
    - U.S. Patent No. 10,734,481 to Dr. G.R. Mohan Rao ("the '481 patent") (Ex. 2065);
    - U.S. Patent No. 11,316,014 to Dr. G.R. Mohan Rao ("the '014 patent") (Ex. 2066);

- Prosecution histories for the Challenged Patent and the other patents in the same family (listed above), which I understand constitute the exchange of correspondence between the Patent Office and the applicant (Ex. 1002; Exs. 2067-2071);
- Petitioner's IPR petitions in Nos. IPR2024-00001 (regarding the '481 patent), IPR2024-00016 (regarding the '842 patent), IPR2024-00017 (regarding the '195 patent), IPR2024-00018 (regarding the '502 patent), IPR2024-00019 (regarding the '014 patent), and IPR2024-00020 and -00021 (regarding the '222 patent);
- Declaration Dr. Sanjay Banerjee (Ex. 1003), who I understand is Petitioner's expert in this IPR and the other IPR proceedings listed above (his declaration is Ex. 1003 in each of those IPR proceedings);
- Petitioner's exhibits 1001-1017, 1020, 1022-1023, 1025-1034, 1036-1038, 1040-1041, 1044, and 1046-1047 in this IPR; and
- Any other references/documents cited within this Declaration.

IV. LEVEL OF ORDINARY SKILL IN THE ART

17. Based on my review of the Challenged Patent, the types of problems encountered in the art at and prior to the time of the alleged invention, prior solutions to those problems, the pace with which innovations were made during the relevant time period, the sophistication of the technology, and the educational level of active professionals in the field, I believe that a person of ordinary skill in the art (POSITA), at the time of the alleged invention, would have had at least a Bachelor's of Science degree in electrical or computer engineering, materials science, chemical engineering, applied physics, or a related field, with emphasis on semiconductor manufacturing, or an equivalent degree, and at least four years of experience in semiconductor design and manufacturing. Additional education in a relevant field or industry experience may compensate for a deficit in one of the other aspects of the requirements stated above.

18. All of my opinions in this declaration are from the perspective of a POSITA, as I have defined it above and during the relevant time frame (e.g., late 2004, including the period up to September 3, 2004, which I understand is the earliest claimed priority date of the Challenged Patent). During this time frame, I possessed at least the qualifications of a POSITA, as defined above.

V. RELEVANT LEGAL PRINCIPLES

19. For the purposes of this Declaration, I have been informed about certain aspects of the law that are relevant to my analysis and opinions. I have applied these legal principles in rendering my opinions below.

A. Claim Construction

20. I understand that the ordinary and customary meaning of a claim term is the meaning that the term would have to a POSITA at the time of the effective filing date of the patent application that matured into the patent-at-issue. For the Challenged Patent, this is September 3, 2004. In the absence of an express intent on the part of the inventor to give a special meaning to the claim terms, the words are presumed to take on the ordinary and customary meanings attributed to them by a POSITA.

21. I understand that it is the use of the words in the context of the written description, and as customarily used by those skilled in the relevant art, that accurately reflects both the ordinary and the customary meaning of the terms in the claims.

22. I understand that the basis for a term's ordinary and customary meaning may be derived from a variety of sources, including the words of the claims themselves, the remainder of the specification, the prosecution history, and extrinsic

evidence concerning relevant scientific principles, the meaning of technical terms, and the state of the art at the time of the invention.

23. I have been instructed that dictionary definitions or definitions from technical references can be used to inform or confirm the ordinary and customary meaning of words found in a claim, but that in construing claim terms, the general meanings gleaned from reference sources, such as dictionaries, must always be compared against the use of the terms in the context of the claim itself, and the intrinsic record must always be consulted to identify which of the different possible dictionary meanings is most consistent with the use of the words by the inventor.

24. I understand that a patent applicant is entitled to be his or her own lexicographer (in other words, provide his or her own meaning to a word or phrase) and may rebut the presumption that claim terms are to be given their plain and ordinary meaning. To do so, the applicant must clearly set forth a definition of the term that is different from its ordinary and customary meaning.

25. Where the applicant provides an explicit definition for a term, that definition will control interpretation of the term as it is used in the claim in which it appears. I understand that the specification can also be relied on for more than just explicit lexicography to determine the meaning of a claim term. For example, I understand that the meaning of a particular claim term may also be determined by

implication, that is, according to the usage of the term in the context of the specification.

B. Anticipation

26. I understand that under U.S. Patent Law, 35 U.S.C. § 102, a claim is invalid as anticipated if a single prior art reference discloses each and every limitation of the claimed invention.

27. I am informed that a reference is anticipatory if it contains the claim elements in the same order as claimed, regardless of whether the prior art and the claimed invention are directed to achieving the same purpose.

28. I understand that a prior art reference may anticipate a claim without expressly disclosing a feature of the claimed invention if that missing feature is necessarily present, or inherent, in the single anticipating reference.

29. I am informed that inherency requires more than a probability or possibility that a claimed feature is present in the prior art, but rather that the feature or characteristic is a necessary part of the prior art. I also am informed that recognition of the inherency by a POSITA— at the time— is not required.

C. Obviousness

30. I understand that under U.S. Patent Law, 35 U.S.C. § 103, a claim is invalid as obvious if the differences sought to be patented and the prior art are such

that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

31. I am informed that an obviousness analysis requires an assessment of the scope and content of the prior art, the differences between the art and the claims at issue, and the level of ordinary skill in the art. I am told that it is against this backdrop that obviousness is assessed.

32. I am informed that a person of ordinary skill in the art (POSITA) is a hypothetical person who is presumed to be aware of all the pertinent prior art. I am also informed that an obviousness analysis may take account of the inferences and creative steps that a POSITA would employ.

VI. THE CHALLENGED PATENT

A. Background Technology Regarding Dopants

33. Silicon is an example of a semiconductor. In its pure form, it is typically an insulator, but it can become an electrical conductor when impurities called "dopants" are added into the silicon crystal. These dopants are often phosphorous or boron atoms that have one more or one less valence electron than a silicon atom. If the dopant has one less valence electron, then it creates what is called a "hole" where there was an electron, which can be thought of as a positive unit of charge. The extra electrons or holes disturb the local charge equilibrium in the silicon and can become mobile in response to electric fields. Thus, the electrons and holes are called "charge carriers." These dopants can also change the local net electrical charge distribution in the surrounding silicon, influencing the motion of other charge carriers passing by. When the dopant concentration is graded in a particular direction, other charge carriers will move in the gradient direction (or opposite direction) depending on the charge carrier's polarity. This phenomenon is called "carrier drift."

B. Overview of Challenged Patent

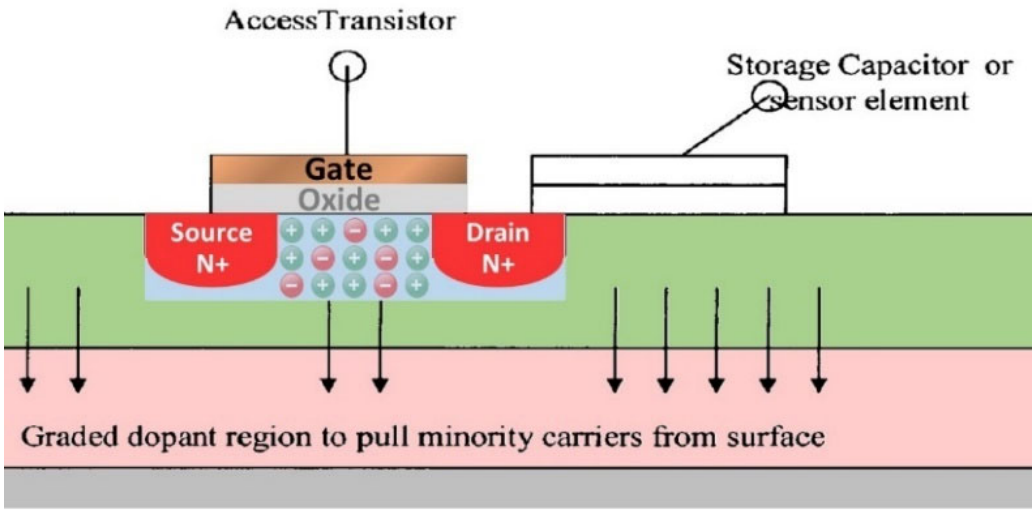
34. At the time of invention of the Challenged Patent, most semiconductor devices relied on spatially uniform concentrations of dopants. Ex. 1001 (Challenged

Patent), Abstract, 1:48-63. Dr. Rao (the inventor named on the Challenged Patent) recognized, however, that graded concentrations of dopants can be used to improve certain aspects of the performance of transistors and other semiconductor devices. *Id.*, Abstract, 3:25-35, 3:56-58. The claimed invention is clearly disclosed in, e.g., Figs. 5B-5C of the Challenged Patent, and the corresponding parts of the specification.

35. A surface-channel MOSFET is a common type of transistor capable of controlling current flow at or along the surface of the semiconductor substrate. Ex. 2059 (Chen textbook), 27 ("carriers propagate at the semiconductor surface"). Figure 5B shows an NMOS[1] transistor that is formed in a p-type surface layer. The transistor comprises (1) a gate; (2) a thin oxide separating the gate from the surface layer; and (3) two doped regions called the source and drain (shaded red). Ex. 1001, 3:31-34 ("electrons can be swept from source to drain"), 3:64-66 ("accelerate majority carriers towards the drain"). In Fig. 5B, which is annotated below, the N+ means these regions are heavily doped with an n-type dopant that creates a surplus

[1] MOS stands for "metal oxide semiconductor."

of negative carriers (i.e., electrons).[2] The specification explains that the NMOS transistor in Fig. 5B can be a surface-channel MOSFET.

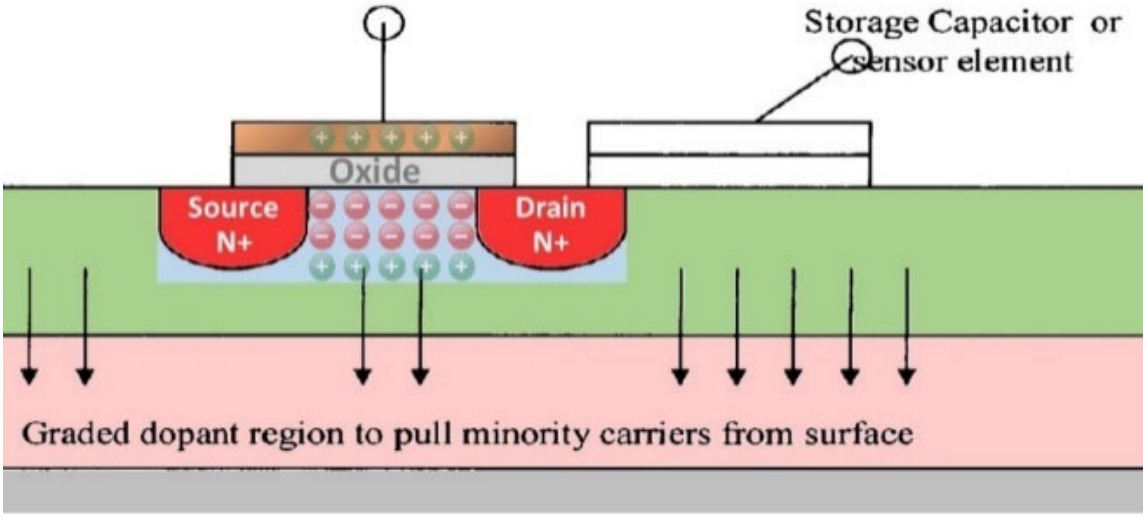


Id., Fig. 5B (annotated); *see also id.*, 3:64-66. Meanwhile, the p-type silicon between the source and drain (shaded blue) has an abundance of positively charged holes (green circles). When the holes separate the source's electrons from the drain's electrons, current cannot flow through the transistor, and the transistor is in an "off" state.

36. When a positive voltage is applied to the gate, an electric field forms in the oxide. This positive electric field repels the "positive" holes downwards, while

[2] An "N" region or layer has more electrons, and thus a "**n**egative charge." A "P" layer has more holes, and a "**p**ositive charge." A "+" or "-" means heavily or lightly doped.

the negative electrons (red circles) are attracted to move into the blue surface layer. When enough electrons have accumulated in the surface layer below the oxide, they form a conductive channel (as annotated in Figure 5B below) of electrons between the source and the drain, and current can begin to flow through the transistor.



Ex. 1001, FIG. 5B (annotated).[3] In order to turn the transistor "off," the positive voltage is removed from the gate and the channel disappears as the holes return to the surface layer.

37. Dr. Rao (the inventor named on the Challenged Patent) recognized that by using graded concentrations of dopants in the well region and a drift layer (shaded pink), it is possible to "pull" carriers from the silicon's surface. Ex. 1001, Fig. 5B

[3] Because the channel is formed by electrons with a **n**egative charge, the MOSFET is referred to as an **n**-channel MOSFET, and the "minority carriers" are holes.

(annotated above). In this example, pulling the holes from the surface layer when a positive voltage is applied to the gate, allows the transistor to turn "on" more quickly. This improves the speed and performance of the transistor. Ex. 1001, 3:30-35.

VII. OVERVIEW OF ALLEGED PRIOR ART

38. Dr. Banerjee's declaration relies on the Kawagoe (Ex. 1007) reference for single-reference obviousness in Ground I; Kawagoe in view of Gupta (Ex. 1014) in Ground III; Kawagoe in view of Silverbrook (Ex. 1042) in Ground V; Wieczorek (Ex. 1006) in view of Wolf (Ex. 1008) in Ground II; Wieczorek in view of Wolf and Gupta in Ground IV; and Wieczorek in view of Wolf and Silverbrook in Ground VI. Ex. 1003, ¶31. Below, I provide overviews of relevant portions of Kawagoe and Wieczorek.

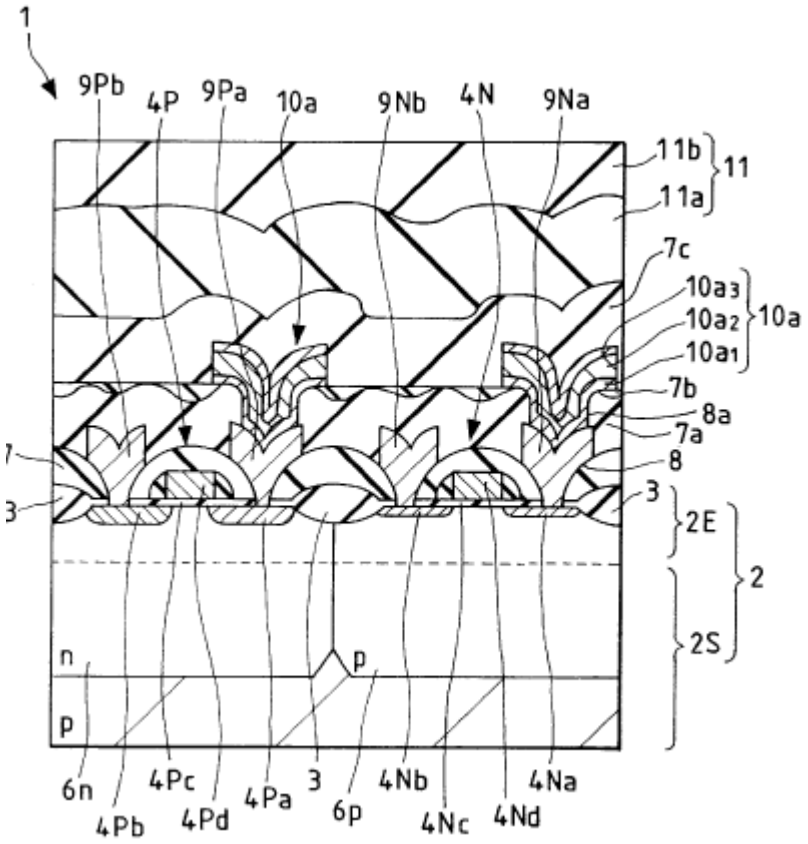
A. Kawagoe (Ex. 1007)

39. Kawagoe is a patent that:

> relates to a process for manufacturing a semiconductor wafer, a semiconductor wafer, a process for manufacturing a semiconductor integrated circuit device, and a semiconductor integrated circuit device and, more particularly, to a technique which is effective if applied to the so-called 'epitaxial wafer manufacturing process' for forming an epitaxial layer over the surface of a semiconductor substrate body, an epitaxial wafer, a process for manufacturing a semiconductor integrated circuit device by using the epitaxial wafer, and a semiconductor integrated circuit device.

Ex. 1007, 1:13-23.

40. Figure 16 of Kawagoe (shown below) is "a section showing an essential portion of a semiconductor integrated circuit device according to" Kawagoe's fourth embodiment. *Id.*, 14:46-49.



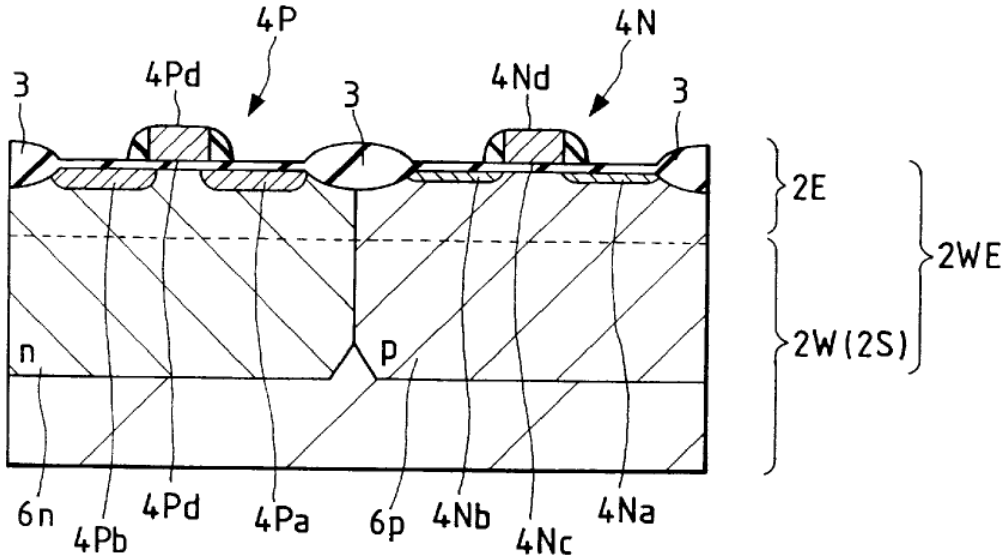
Id., FIG. 16.

41. Figure 16 shows, in part, an n-well 6n and a p-well 6p. Kawagoe discloses that in p-well 6p:

> the impurity concentration of the p-well 6p is given such a gradient that it is gradually lowered in the depthwise direction from the surface of the epitaxial layer 2E, so that the influence to be caused by the carriers (or electrons) due to the α-ray is

> lowered. Specifically, ***the electrons produced by the α-ray are attracted to the substrate body 2S by that concentration gradient and prevented from entering the p-well 6p*** so that the soft errors can be reduced in case the MIS memory of the DRAM or the like is formed in the p-well 6p. The impurity concentration NW in the principal surface of the epitaxial layer 2E of the p-well 6p and the n-well 6n is at about 6×10^{16} atoms/cm^3, so that the impurity concentration of the p-well 6p and the n-well 6n is at 5×10^{15} to 6×10^{16} atoms/cm^3.

Id., 16:2-15 (emphasis added). Figure 23 (shown below) "is a section of the essential portion of the semiconductor substrate at the step … of manufacturing the semiconductor integrated circuit device of FIG. 16":



Id., 6:1-4.

B. Wieczorek (Ex. 1006)

42. Wieczorek is a patent publication that "relates to the field of manufacturing integrated circuits, and, more particularly, to a semiconductor device, such as a field effect transistor, having an improved retrograde dopant profile in a channel region of the transistor element, and a method of manufacturing such a semiconductor device." Ex. 1006, ¶[0002].

43. Much of the Petition's discussion focuses on Figures 1B and 2B (shown below), which are described in a relatively cursory manner in the background section of Wieczorek. The entirety of Wieczorek's description of Figure 1B is:

> FIG. 1b schematically shows the semiconductor device 100 in an advanced manufacturing stage. In FIG. 1b, the semiconductor device 100 comprises within the P-well structure 110 heavily N-doped source and drain regions 131, including lightly doped extensions 132. In the N-well structure 120, similarly, heavily P-doped source and drain regions 141, including lightly doped extensions 142, are provided. A gate insulation layer 135, for example, a gate oxide layer, is provided on the entire surface of the semiconductor device 100 to separate a gate electrode 134 from a corresponding channel region 136 and a gate electrode 144 from the corresponding channel region 146. Spacer elements 133 are provided at the sidewalls of the gate electrode 134 and respective spacer elements 143 are located at the sidewalls of the

> gate electrode 144. Thus, the semiconductor device 100 includes an N-channel transistor 130 and a P-channel transistor 140.

Ex. 1006, ¶[0012]; *see also id.*, ¶[0020] ("FIGS. 1a-1b show schematic cross-sectional views of an exemplary conventional semiconductor device at different manufacturing stages.").

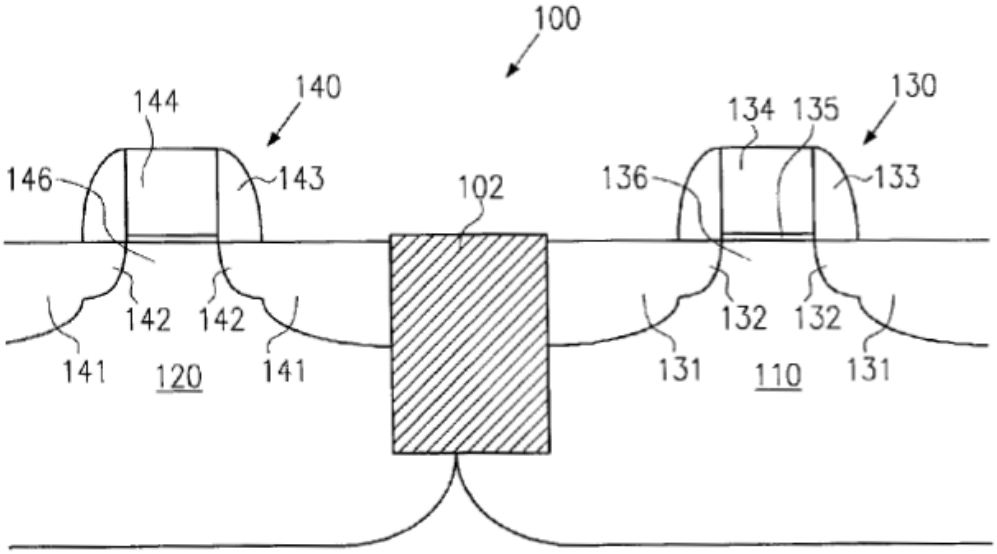


FIG.1b
(Prior Art)

Id., FIG. 1B.

44. Figure 2B (shown below) is described in the background section of Wieczorek:

> FIG. 2b shows a corresponding graph with a typical dopant profile with respect to the depth of the respective well structure. Due to the up-diffusion of the dopant atoms during the heat treatment, the initially retrograde profile in the vicinity of the surface of the semiconductor device 100, as indicated by

> reference number 200, may have become substantially uniformly distributed.

Id., ¶[0011].

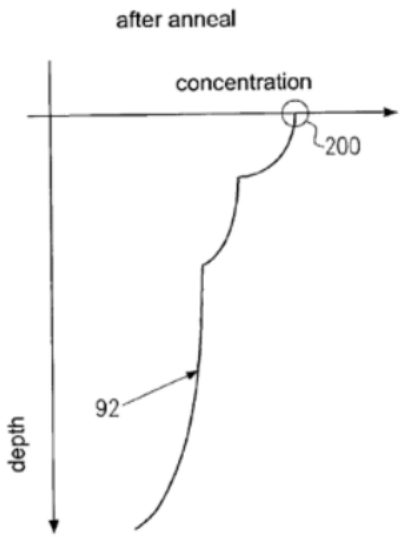


FIG.2b
(Prior Art)

Id., FIG. 2B.

VIII. CLAIM CONSTRUCTION

45. I understand that claim terms are typically given their ordinary and customary meaning, as would have been understood by a person of ordinary skill in the art at the time of the alleged invention. In considering the meaning of the claims, I also understand that one must consider the claim language, specification, prosecution history, and the knowledge of a person of ordinary skill in the art at the relevant time. I understand that Patent Owner is not proposing any claim terms for claim construction. I agree with Patent Owner that none of the terms require construction. I applied the above understanding in my analysis.

IX. THE CITED REFERENCES DO NOT DISCLOSE OR SUGGEST ALL THE FEATURES OF THE CHALLENGED CLAIMS

46. In my opinion, the prior art references relied upon in the Petition and Dr. Banerjee's declaration (Ex. 1003) do not disclose or suggest all the features of the Challenged Claims, as I explain below.

A. Dr. Banerjee's Kawagoe-based analysis is incorrect regarding the "aid carrier movement…" limitations (Elements [1.5], [1.6], [21.5], [21.6], [39.5], [41.5], [42.5]).

47. Dr. Banerjee stated in his declaration that "Kawagoe renders claims 1-9, 12-14, 16-21, 23-28, and 31-42 obvious." Ex. 1003, ¶66. I disagree. For elements [1.5]/[1.6]/[21.5]/[21.6]/[39.5]/[41.5]/[42.5] he states that "Kawagoe discloses or, at a minimum, renders obvious this element" (*id.*, ¶¶89, 97), but he did not identify any portion of Kawagoe that actually discloses the "aid carrier movement…" feature of these claim elements. The "aid carrier movement…" feature appears in the challenged independent claims as follows. Elements [1.5] / [21.5]: "at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to ***aid carrier movement***" "from the first and second active regions towards an area of the substrate where there are no active regions" (claim 1) or "from the surface to an area of the substrate where there are no active regions" (claim 21) (elements [39.5], [41.5], and [42.5] are similar); Elements [1.6] / [21.6]: "at least one well region adjacent to the first or second active region containing at least one graded

dopant region, the graded dopant region to ***aid carrier movement*** from the surface [towards | to] the area of the substrate where there are no active regions" (claims 1/21).

48. In Ground I, for the "aid carrier movement" feature of these claims, it appears that Dr. Banerjee made inferences based on Kawagoe's disclosures, and I disagree with his inferences. Specifically, he pointed to one part of Kawagoe for mapping to the claimed "graded dopant concentration" of the above independent claims, and used that to infer that the "aid carrier movement…" limitation of those claims is disclosed. Ex. 1003, ¶¶89-105. But while Kawagoe does disclose a "concentration gradient," Dr. Banerjee misses the context of Kawagoe. In general, there are three possibilities: a reference disclosing a dopant concentration gradient in a semiconductor device could a) teach that the concentration gradient aids carrier movement; b) teach that the concentration gradient impedes carrier movement; or c) be silent as to the concentration gradient aiding or impeding carrier movement. Kawagoe teaches using a concentration gradient to *impede* carrier movement. Kawagoe is concerned with naturally occurring α-rays striking a semiconductor

device and generating free electrons in the substrate.[4] Kawagoe's free electrons can disrupt the operation of the device during a "single event upset" ("SEU"). Dr. Banerjee fails to appreciate that Kawagoe teaches a "concentration gradient" to "*prevent*[] [the SEU-generated carriers] from entering the p-well." Ex. 1007, 16:7-11. Below, I reproduce the portion of Kawagoe's specification containing the disclosure about preventing carriers from entering the p-well.

16

from the principal surface (having an impurity concentration N_W) of the epitaxial layer **2**E. Thus, the impurity concentration of the p-well **6***p* is given such a gradient that it is gradually lowered in the depthwise direction from the surface of the epitaxial layer **2**E, so that the influence to be caused by the carriers (or electrons) due to the α-ray is lowered. Specifically, the electrons produced by the α-ray are attracted to the substrate body **2**S by that concentration gradient and prevented from entering the p-well **6***p* so that the soft errors can be reduced in case the MIS memory of the DRAM or the like is formed in the p-well **6***p*. The impurity concentration N_W in the principal surface of the epitaxial layer **2**E of the p-well **6***p* and the n-well **6***n* is at about 6×10^{16} atoms/cm^3, so that the impurity concentration of the p-well **6***p* and the n-well **6***n* is at 5×10^{15} to 6×10^{16} atoms/cm^3.

[4] As I explained above in Section II, I am familiar with *α*-rays and have experience with them, including in the time period preceding 2004 (which I understand is the earliest claimed priority date of the Challenged Patent).

Id., 16:1-15.

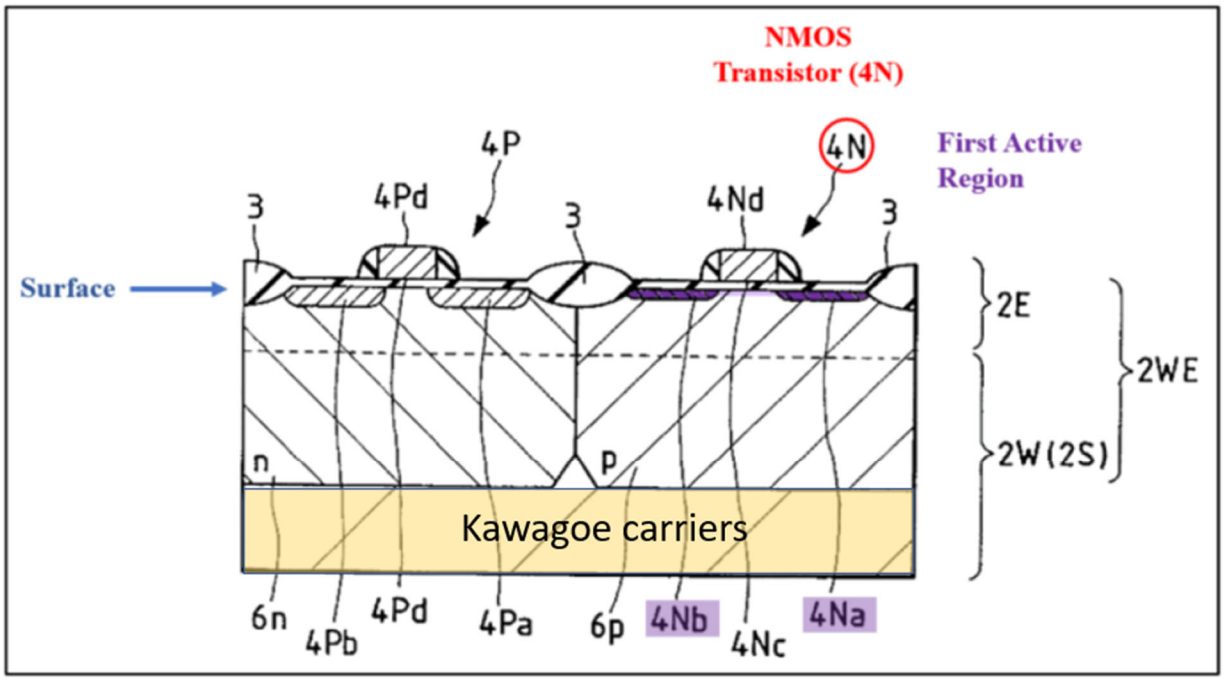
49. In my opinion, a POSITA would have understood that Kawagoe shows that graded dopant concentrations don't *always* aid carrier movement, as Petitioner claims, because sometimes the "concentration gradient" can "prevent" carrier movement.

50. Based on Dr. Banerjee's declaration, it is apparent that for his analysis of the "aid the movement carriers …" limitation he only considered the downward sloping nature of Kawagoe's concentration gradient, and not any other aspect of the gradient (e.g., the magnitude of the force it produces on carriers) or whether there are any external forces (e.g., opposing forces, e.g., due to the intrinsic resistance of silicon) such that the net force might not be aiding carrier movement in the claimed manner. In my opinion, a POSITA would have known that if two forces are acting on an object in opposite directions, both forces cannot aid its movement. Either the opposing forces are equal—and there is no movement—or the two forces are not equal and the object moves in the direction of the force having larger magnitude, albeit diminished by the counter force. The smaller force does not "aid" the movement of the object, because it is pushing *against* the movement. The magnitude of the concentration gradient plays a substantial role, because a small gradient may not be sufficient to overcome the resistance of the material in which the gradient exists. Therefore, a POSITA would need to know other parameters of the relevant

device (e.g., magnitude of concentration gradient, intrinsic resistance of silicon, presence of any other external forces) to know whether a drift field associated with a concentration gradient would aid carrier movement.

51. Dr. Banerjee's declaration does not indicate that he calculated the slope of the concentration gradient that he said Kawagoe discloses. The magnitude of the slope is essential to determine the magnitude of the force the dopant gradient places on the carrier and thus the net force. Since the mere direction of the gradient is *not* sufficient to determine the nature of the net force, the premise of Dr. Banerjee's analysis is incorrect. Therefore, I disagree with his conclusion about the "aid carrier movement…" feature being taught in Kawagoe. As I explained above, since Kawagoe teaches inhibiting carrier movement, it does not teach aiding carrier movement.

52. I see that Dr. Banerjee stated in a footnote that SEUs generate "electrons produced in the large substrate body below the wells"—far below the active regions. *See* Ex. 1003, ¶93 n.6. Dr. Banerjee confirms that alpha ray SEUs produce electrons, not holes. Kawagoe's electrons are initially ***below*** p-well 6p, and prevented from moving ***upward*** into p-well 6p. The annotated figure (which adds an annotation to one found in Dr. Banerjee's declaration) shows, in orange, the location of the carriers in Kawagoe.



Ex. 1003, ¶81 (annotated). Kawagoe does not address carriers in the "active region," and as the annotated image above shows, does not "aid carrier movement *from the [first and second active regions | first or second active region | surface]*" because Kawagoe's carriers are nowhere near what the Petition identifies as the "surface" or first/second "active regions." Recall that the dopant gradient keeps the alpha particle-generated electrons (SEU) from entering the well. Since the well starts at the surface and extends down to the depth 2WE, the generated electrons must originate in the substrate below the wells, in the area highlighted in yellow.

53. Dr. Banerjee stated that "[d]uring a so-called single event upset (SEU), an α-ray generates millions of carriers, some of which are produced in or near the active region at the surface of the substrate." Ex. 1003, ¶94. The only document he

cited in support of that statement is Wang (Ex. 1009). It appears that Wang is a document from 2008. Ex. 1003, ¶94 (citing Ex. 1009); Pet. at Table of Exhibits (listing "2008" for Ex. 1009); Ex. 1009, 429 (listing copyright date of 2008). I do not believe that Wang shows what a POSITA would have known about SEU carriers in the active region at the time of the Challenged Patent. Wang does not give a POSITA a reason to use Kawagoe's technique in the active region. Wang's Figure 2 (cited by Dr. Banerjee, *see* Ex. 1003, ¶93, and shown below)—just like Kawagoe—shows that the SEU carriers are primarily generated deep in the device.

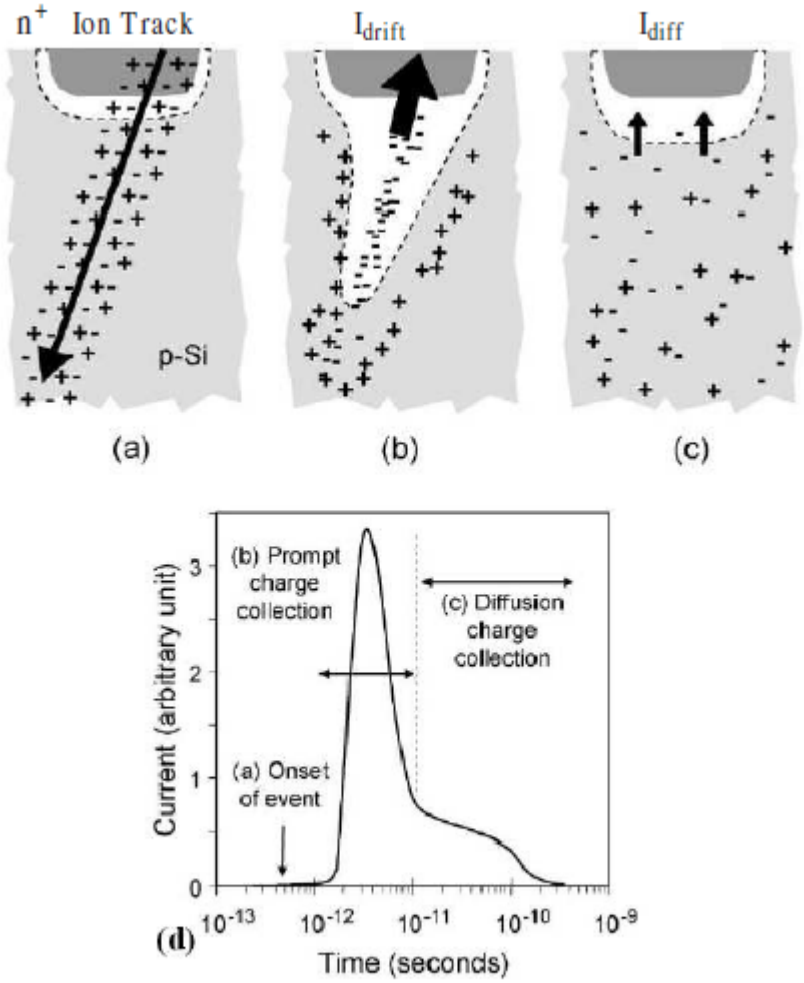


Fig. 2. Schematic representation of charge collection in a silicon junction immediately after (a) an ion strike, (b) prompt (drift) collection , (c) diffusion collection, (d) the junction current induced as a function of time [4].

Ex. 1009, FIG. 2. Wang shows some carriers in the active region, but does not disclose that they are problematic.

54. Dr. Banerjee's analysis of Kawagoe's disclosure regarding electrons generated by alpha-rays is incorrect. A POSITA would have understood that when Kawagoe mentions "electrons produced by the α-ray" (Ex. 1007, 16:7-11), Kawagoe

is *not* describing electrons near the surface. Nishizawa (Ex. 2060), demonstrates the knowledge of a POSITA:

> Accordingly, it will be understood that the alpha-particle immediately after irradiation to the surface of a semiconductor body has an energy of several MeV, for example about 5 MeV, and that, accordingly, ***the probability of creation of electron-hole pairs is extremely low near the surface***. The alpha-particle will begin to create electron-hole pairs after it has entered into the semiconductor substrate to a certain distance.

Ex-2060, 19:26-34; *see also id.*, 20:19-22 ("[T]he amount of electrons created which adversely affect the memory action is no greater than only 10% of the stored electric charge, and thus it can be disregarded."). To the extent that any electrons are created near the surface, they are taught that they are not a problem. Hence, there would be no reason to solve a nonexistent problem.

55. A POSITA would have known that the probability of the alpha-ray strike *creating electrons* (like disclosed in Kawagoe, Ex. 1007, 16:7-11) is *extremely low* near the surface (as demonstrated by Nishizawa). Therefore, the better reading of Kawagoe is that Kawagoe is describing electrons "***created … in the substrate body below the wells***," as Dr. Banerjee conceded. Thus, a POSITA would have understood that Kawagoe's electrons that are prevented from entering the p-well are

not created near the surface. Thus, Kawagoe does not teach aiding carrier movement from the surface (or first surface) to the surface (or to the substrate).

B. Dr. Banerjee's Wieczorek-based analysis is incorrect regarding the "aid carrier movement…" limitations (Elements [1.5]/[21.5]/[39.5]/[41.5]/[42.5] and [1.6]/[21.6]).

56. Dr. Banerjee stated in his declaration that "Wieczorek in combination with Wolf renders claims 1-2, 4-9, 12-23, 25-28, and 31-42 obvious." Ex. 1003, ¶136. I disagree. For elements [1.5]/[1.6]/[21.5]/[39.5]/41.5]/[42.5] he states that "Wieczorek-Wolf renders obvious these elements" (*id.*, ¶¶155, 162), but as he did for the Kawagoe-based ground regarding claim 1, Dr. Banerjee didn't actually identify anything in Wieczorek that discloses the "aid carrier movement…" feature of the above elements. Ex. 1003, ¶¶155-165.

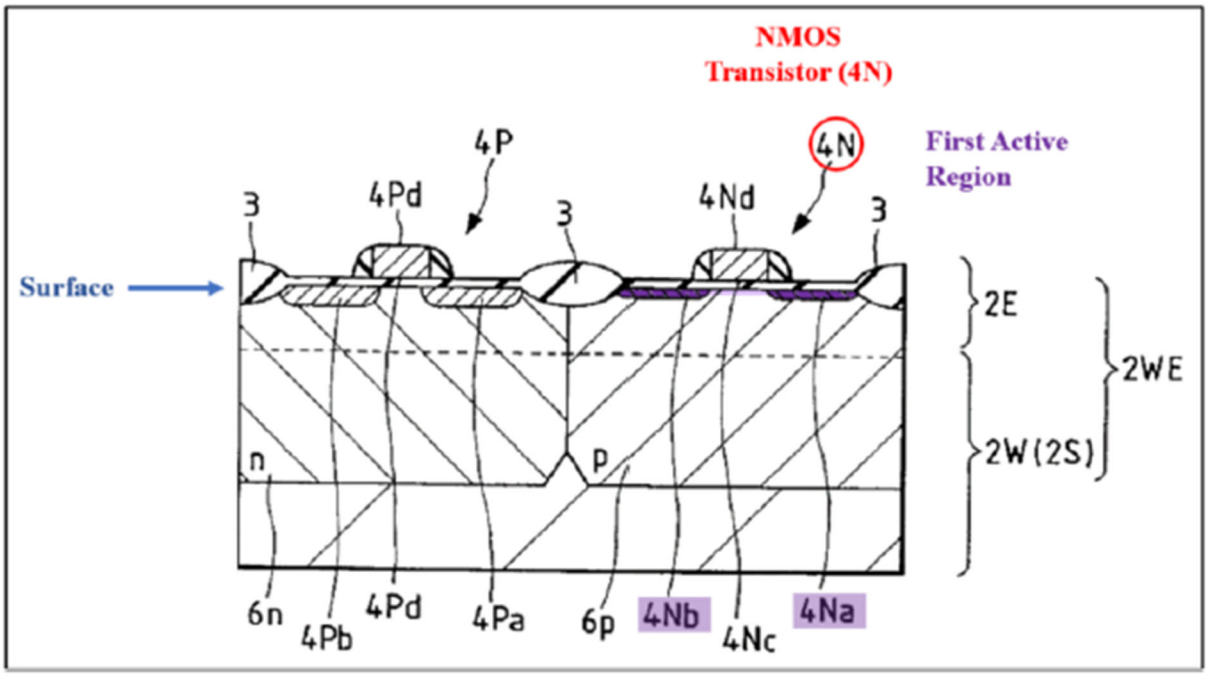
57. Dr. Banerjee's declaration does not indicate that he calculated the slope of the concentration gradient that he said Wieczorek discloses. It would have been impossible for Dr. Banerjee to make such a calculation because the dopant gradient Petitioner points to in Figure 2B (and Wieczorek generally) does not have any values from which one could calculate a slope. In mathematical terms, the slope in each direction (X, Y, and Z) is known formally as the gradient vector. The magnitude of the slope is essential to determine the magnitude of the force the dopant gradient places on the carrier and thus the net force.

C. Dr. Banerjee's Kawagoe-based analysis is incorrect regarding the "first active region … with a second doping type opposite in conductivity to the first doping type" limitation (Elements [1.2]/[21.2]/[39.2]/[41.2]/[42.2]).

58. Regarding elements [1.2], [21.2], [39.2], [41.2], and [42.2], Dr. Banerjee stated that "Kawagoe discloses or, at a minimum, renders obvious this element." Ex. 1003, ¶81. I disagree, because Kawagoe does not disclose or suggest a "first active region … with a second doping type opposite in conductivity to the first doping type" as required by each of these challenged independent claims, as I explain below.

59. For elements [1.1]/[21.1]/[39.1]/[41.1]/[42.1] (where the antecedent basis for "the first doping type" is found), Dr. Banerjee mapped "a first doping type" to p-type doping. Ex. 1003, ¶69. For elements [1.2], [21.2], [39.2], [41.2], and [42.2], Dr. Banerjee stated that Kawagoe's regions 4Na and 4Nb "have a second doping type (n-type) opposite in conductivity to the first doping type (p-type) of the substrate." *Id.*, ¶81. Kawagoe discloses that regions 4Na and 4Nb are doped n-type (Ex. 1007, 8:66-9:3), but Dr. Banerjee also states that the channel of transistor 4N is part of the first active region. Ex. 1003, ¶81 ("Source-drain regions 4Na/4Nb (purple) form part of the claimed first active region, which also includes the channel region…."). And for elements [1.5]/[21.5]/[39.5]/[41.5]/[42.5], which recite "at least a portion of at least one of the first and second active regions having at least

one graded [dopant | dopant acceptor | donor dopant] concentration…," Dr. Banerjee pointed to the concentration profile under the channel. Ex. 1003, ¶¶89-91. But the channel of transistor 4N is doped p-type, because it is the top portion of a p-well (as shown in Figure 23 of Kawagoe):



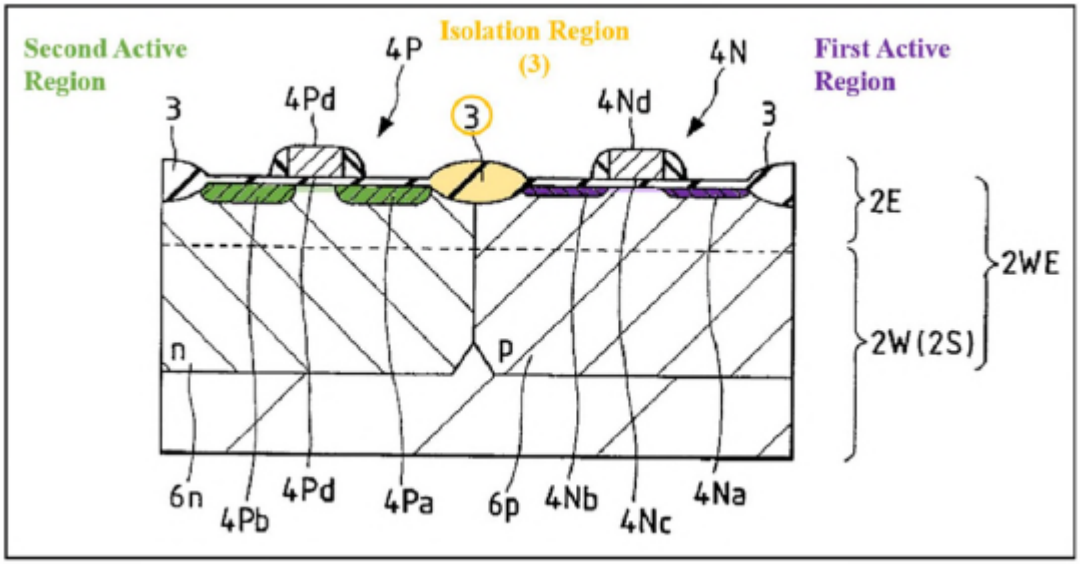
Ex. 1003, ¶81 (citing Ex. 1007, FIG. 23, which shows the channel of transistor 4N at the top of p-well 6p, and stating "the channel region (light purple) in between the source-drain regions 4Na and 4Nb"). A POSITA would have understood that the channel in a CMOS transistor has the same doping type as the well in which the source and drain are formed. All three material sections are p-type without any n-type: (1) the channel of NMOS 4N made from the p-well; (2) the p-well; (3) and the p-type substrate are all doped p-type.

60. Therefore, under Dr. Banerjee's analysis in which the source, drain, and channel are all part of Kawagoe's first active region, he has not established that the active region has n-type doping (which is what he would need to establish for elements [1.2], [21.2], [39.2], [41.2], and [42.2], in light of his analysis for elements [1.1]/[21.1]/[39.1]/[41.1]/[42.1]).

D. Dr. Banerjee's Kawagoe-based analysis is incorrect regarding the "first active region and second active region are each separated by at least one isolation region" limitation (Dependent claims 6 and 27).

61. In Ground I, Dr. Banerjee relied on Kawagoe for the "first active region and second active region are each separated by at least one isolation region" limitation of dependent claims 6 and 27. I disagree with his analysis, as Kawagoe does not disclose or suggest that feature, as I explain below.

62. Dr. Banerjee's declaration provides the following annotated Figure 23 of Kawagoe and maps Kawagoe's source/drain 4Na/4Nb and channel of nMOS 4N to the claimed "first active region," and maps Kawagoe's source/drain 4Pa/4Pb and channel of pMOS 4P to the claimed "second active region." Ex. 1003, ¶114 ("As shown below, the first active region (purple/light purple) and second active region (green/light green) are separated by 'field insulating film 3' (claimed 'isolation region') (yellow).").



Ex. 1003, ¶114 (citing Ex. 1007, FIG. 23). The Petition further maps Kawagoe's field insulating film 3 to the claimed "isolation region." *Id.*

63. But Dr. Banerjee fails to appreciate that regions 4Na and 4Nb, which "are regions for forming the source-drain regions of the nMOS 4N" (Ex. 1007, 8:66-67), "are made as deep as about 0.5 μm and ***formed in the range of the thickness of the epitaxial layer 2E***." Ex. 1007, 9:3-6 (emphasis added). Kawagoe provides similar disclosure regarding regions 4Pa and 4Pb. *Id.*, 9:47-53. Conversely, the oxide layer is described as over the surface. Figures are not to be taken to scale, but the specification as cited describes an accurate description. Thus, a POSITA would have understood that the first and second active regions extend to about the depth of the epitaxial layer 2E and abut each other laterally, and therefore they are not separated by Kawagoe's field insulating film 3, as required by claims 6 and 27. The

field insulating film 3 is formed "[o]ver the principal surface of the epitaxial layer 2E" (Ex. 1007, 8:40-42) and a POSITA would have understood that it does not extend deep enough to separate the two active regions.

X. CONCLUSION

64. I declare that all statements made herein of my knowledge are true, and that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine, imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Respectfully submitted,

Date: August 16, 2024 By: Alexander D. Glew

Alexander D. Glew