

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

CIRRUS LOGIC, INC.;
OMNIVISION TECHNOLOGIES, INC.; AND
AMS SENSORS USA, INC.,
Petitioner,

v.

GREENTHREAD LLC,
Patent Owner.

IPR2024-00001 Patent 10,734,481 B2
IPR2024-00016 Patent 10,510,842 B2
IPR2024-00017 Patent 8,421,195 B2
IPR2024-00018 Patent 9,190,502 B2
IPR2024-00019 Patent 11,316,014 B2
IPR2024-00020 Patent 11,121,222 B2
IPR2024-00021 Patent 11,121,222 B2¹

**SUPPLEMENTAL DECLARATION OF DR. SANJAY BANERJEE
IN SUPPORT OF PETITIONERS' REPLY**

¹ The same declaration is being filed in each of the referenced proceedings.

TABLE OF CONTENTS

I.	Introduction.....	1
II.	Dr. Glew’s Analysis Regarding the Movement of Charge Carriers in a Doped Semiconductor Device is Flawed	1
III.	Summary of Opinions.....	2
IV.	A Graded Dopant Concentration Sloped in a Particular Direction Is Sufficient to Aid Movement of Minority Carriers in that Direction due to Drift.....	4
A.	Majority and Minority Carriers Exist in Conduction and Valence Bands of Doped Silicon and Are In Constant Motion at Room Temperature.....	5
1.	Crystalline Silicon Substrate Has Free Carriers.	5
2.	Silicon Substrate Has Carriers in Conduction Band at Room Temperature.	6
3.	N-Doped Silicon Has Many Free Electrons in the Conduction Band at and a Few Holes in the Valence Band at Room Temperature.	9
B.	A Graded Concentration of Dopants Will Induce a Static Electric Field That, in Turn, Will Cause Carriers to Drift.	12
1.	A Graded Concentration of Dopants Creates a Static Electric Field.	12
2.	Movement of Carriers Due To a Static Electric Field (Drift and Diffusion)	13
3.	The Prior Art Cited During Prosecution Discloses How A Graded Dopant Concentration Causes Carriers to Drift	16
C.	Minority Carrier Drift Occurs Based on the Direction of the Electric Field Regardless of “Magnitude” of the Graded Dopant Concentration	20

1.	An Electric Field Results in Movement of Carriers Via Drift.....	20
2.	Neither Resistivity nor Resistance Imposes a Barrier to Carrier Movement.....	21
3.	Aside From Absolute Zero, Changes in Temperature Do Not Preclude Carrier Movement.....	23
4.	Stress Does Not Preclude Carrier Movement.....	23
D.	Threshold Voltage V_T Facilitates Flow of Current in Field Effect Transistors (FETs) and Does Not Impose a Barrier to Movement of Carriers Due to a Static Electric Field.....	24
E.	Majority and Minority Carriers in a MOSFET In OFF State	28
F.	Majority and Minority Carrier in a MOSFET In ON State	28
G.	Channel Stopper Regions Facilitate Isolation in MOSFETs	29
V.	Dr. Glew’s Opinions and Testimony are Flawed in Multiple Respects.....	32
A.	Dr. Glew’s Analysis Rests on an Incorrect Understanding of the Operation of Doped Semiconductors	32
1.	Neither “Intrinsic Resistance” or Resistance of Silicon Imposes a Barrier That Carrier Must Overcome Before Moving In Response to a Static Electric Field	33
2.	Stress in Silicon Lattice Does Not Impose a Barrier That Carriers Must Overcome Before Drifting.....	34
3.	A Minimum Magnitude of the Dopant Concentration Gradient Is Not Required for Carriers to Drift	35
4.	At Room Temperature, Doped Semiconductors Contain Carriers In Conduction Band That Are Not Bound to the Dopant or Silicon Atoms	36
5.	Threshold Voltage V_T Enables Flow of Current In a MOSFET And Does not “Liberate” Extra Electrons From A Crystal Structure.....	37

6.	At Equilibrium With No External Voltages, There Is No Net Flow of Current, But Carriers Move Via <i>Drift</i> and <i>Diffusion</i> ,.....	40
7.	At Room Temperature, Thermal Effects Will Move Carriers From Valence to Conduction Bands	43
8.	Identity of Majority and Minority Carriers Does Not Change When a MOSFET is Turned ON	44
9.	Neither Inadvertent Diodes nor Capacitance Imposes a Barrier That Carriers Must Overcome When Drifting	47
10.	Channel Stopper Region Facilitates Isolation between MOSFETs	48
B.	Dr. Glew Failed to Analyze Transistors In Their OFF State and Did Not Consider <i>Drift</i> of Carriers	49
C.	Dr. Glew Had Only Glanced at the File History As He Did Not Consider it Relevant, But Greenthread Made Technical Representations During Prosecution That Support My Analysis	52
VI.	Dr. Glew’s Other Analyses of Petitioner’s Grounds are Incorrect	53
A.	Kawagoe’s First Active Region Includes a “Second Doping Type”	53
B.	Kawagoe Includes an “Isolation Region”	55

I. Introduction

1. I have reviewed Patent Owner Greenthread's Response to the Petition, including the declaration of Dr. Glew (Ex. 2057). I have been asked to provide this supplemental declaration to respond to the technical arguments provided by Dr. Grew in his declaration, Ex. 2057, and during his deposition on Oct. 16, 2024 (Ex. 1063).

II. Dr. Glew's Analysis Regarding the Movement of Charge Carriers in a Doped Semiconductor Device is Flawed

2. With respect to my analysis for various grounds in my initial declaration, Dr. Glew disputes my conclusion that the graded dopant concentration shown in the prior art *aids carrier movement* from the surface towards the substrate. Specifically, Dr. Glew asserts that I only considered the downward sloping nature of the concentration gradient disclosed in the prior art and not any other aspect of the gradient. Ex. 2057, ¶50.

3. Dr. Glew also states that "a POSITA would need to know other parameters of the relevant device (e.g., magnitude of the concentration gradient, intrinsic resistance of silicon, presence of any other external forces) to know whether a drift field associated with a concentration gradient will aid carrier movement." Ex. 2057, ¶50. Dr. Glew further states that "[t]he magnitude of the slope is essential to determine the magnitude of the force the dopant gradient places on the carrier and thus the net force. Since the mere direction of the dopant

gradient is *not* sufficient to determine the nature of the net force, the premise of Dr. Banerjee's analysis is incorrect." Ex. 2057, ¶51. Dr. Glew's declaration does not explain why the magnitude of slope must be known, or why it needs to overcome the "intrinsic resistance," nor does he explain what the "other external forces" are. His declaration also lacks citations to any books or papers that describe the structure or operation of semiconductor devices.

4. Dr. Glew provided additional technical bases of his opinions during his deposition. For example, Dr. Glew stated that these "other forces" include the potential stress on the silicon lattice, which he says may reduce the resistance, and any other defects in the silicon structure, due to post-implantation annealing. *See* Section V.A.2.

5. I disagree with Dr. Glew. His opinions are based on an incorrect understanding of the behavior of charge carriers in a semiconductor device, including their motion, and the impact of a graded dopant concentration in a region on the motion of such charge carriers.

III. Summary of Opinions

6. Doped semiconductors contain carriers (electrons and holes) in the conduction and valence band that are not covalently bonded to the atoms (e.g., silicon or impurity atoms). At room temperature, such carriers are constantly moving due to thermal (i.e., Brownian) effects.

7. A graded concentration of dopants in a region of a semiconductor device creates a static electric field. The direction of the electric field depends upon the type of dopants. A graded concentration of p -type impurity that decreases from the surface of the substrate with increasing depth creates a static electric field that points towards the surface. Such a field causes electrons to drift from the surface deep into the substrate, and causes holes to drift from the substrate towards the surface. The direction of the static electric field is reversed when the concentration of the p -type dopant increases with depth into the substrate. A graded concentration of n -type impurity will exhibit the opposite behavior.

8. The *direction of the slope* of the graded dopant concentration is sufficient to determine whether the static electric field created by the graded dopant concentration will aid the movement of carriers in a given direction due to drift. The carriers (holes or electrons) in the conduction band are in constant motion, and the static electric field causes them to drift. At equilibrium (i.e., when the device is off), there cannot be a net movement of carriers. As a result, the movement of carriers due to drift in one direction is compensated by diffusion of those carriers in the opposite direction.

9. Factors such as intrinsic resistance, operating temperature, and stress in lattice, do not impose any barrier that the carriers must overcome before they start to drift in the presence of a static electric field. No threshold voltage or an

electric field is required to free or liberate the carriers that are already in the conduction band at room temperature. Such factors affect only the resistance of the semiconductor, which in turn impacts the drift velocity of the carriers, and does not pose a barrier to the drift of carriers.

IV. A Graded Dopant Concentration Sloped in a Particular Direction Is Sufficient to Aid Movement of Minority Carriers in that Direction due to Drift

10. In order to respond to Dr. Glew's incorrect opinions, I provide some background on charge carriers in a semiconductor device, including an explanation of how they behave at an equilibrium state. I then explain how a graded dopant concentration produces an electric field in such a device, and results in movement of minority and majority carriers based on the direction of the electric field, including drift and diffusion in a semiconductor. In providing this background, I rely upon my education and research experience, and also provide excerpts and figures found in the following widely-used books on semiconductors:

- Sze, Semiconductor Devices: Physics and Technology, Second Edition 1985 ("Sze"), Ex.1061 (excerpted)
- Streetman and Banerjee, Solid State Electronic Devices, Sixth Edition 2006 ("Streetman"), Ex.1062 (excerpted)
- Wolf, Silicon Processing for the VLSI Era, Volume 3 – The Submicron MOSFET 1990 ("Wolf"), Ex.1008C (excerpted)
- Wolf, Silicon Processing for the VLSI Era, Volume 2 – Process Integration ("Wolf Vol. II), Ex. 1071 (excerpted)

11. While my textbook is the 2006 edition, Sze and Wolf were published in 1985 and 1990 respectively. The overview of technology provided below reflects the knowledge of a person of ordinary skill (POSITA) at least as of the filing date of the Greenthread patents, which I understand is in September 2004.

A. Majority and Minority Carriers Exist in Conduction and Valence Bands of Doped Silicon and Are In Constant Motion at Room Temperature.

1. Crystalline Silicon Substrate Has Free Carriers.

12. A single crystalline silicon substrate is made up of a periodic arrangement of silicon atoms. Silicon has four electrons in the outermost valence shell that forms four covalent bonds to the four neighboring silicon atoms. At low temperatures (e.g., near absolute zero or about -273°C), the silicon electrons are tightly bound to the positively charged silicon nucleus and do not move in the crystal. Consequently, they are not available for conduction of current. At higher temperatures (e.g., at room temperature), thermal energy absorbed from the background will break many of the covalent bonds. When a bond is broken, a free electron results that can participate in current conduction. Fig. 12(a) from Sze illustrates a valence electron in silicon becoming a free electron. An electron deficiency is left in the covalent bond, forming a so-called “hole”. Ex. 1061 (Sze), 27, 28. This deficiency may be filled by one of the neighboring electrons, which

results in a shift of the deficiency location, as from location A to location B in Fig.

12(b). *See also* Ex. 1062 (Streetman) at 62-63.

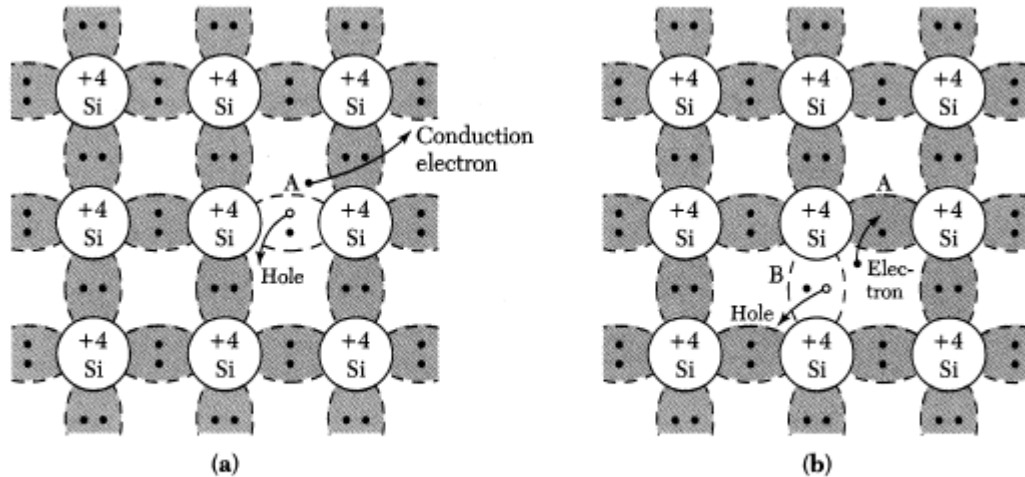


Fig. 12 The basic bond representation of intrinsic silicon. (a) A broken bond at position A, resulting in a conduction electron and a *hole*. (b) A broken bond at position B.

Ex. 1061 (Sze), 28. *See also* Ex. 1062 (Streetman) Fig. 3-1 at 62.

2. Silicon Substrate Has Carriers in Conduction Band at Room Temperature.

13. The electrons associated with silicon atoms in a lattice reside in energy bands. Sze's Figure 15 depicts the energy bands in a diamond lattice formed by bringing isolated silicon atoms together.

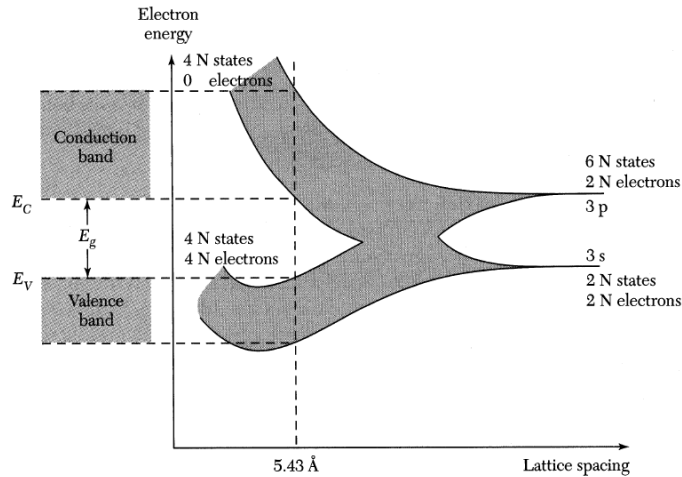


Fig. 15 Formation of energy bands as a diamond lattice crystal is formed by bringing isolated silicon atoms together.

Ex.1061 (Sze), 30. *See also* Ex. 1062 (Streetman) Fig. 3-3 at 66.

14. At very low temperatures (e.g., absolute zero), electrons occupy the lower energy states, so that all the states in the lower band (*the valence band*) will be full and all the states in the upper band (*the conduction band*) will be empty. The bottom of the conduction band is called E_c and the top of the valence band is called E_v . The gap between the bottom of the conduction band and the top of the valence band is the *bandgap energy* E_g and denotes the energy required to break a bond in the semiconductor to free an electron to the conduction band and leave a hole in the valence band. Ex.1061 (Sze), 29. *See also* Ex. 1062 (Streetman) at 66-67.

15. Sze's Figure 19 shows the energy band diagrams for conductors, semiconductors and insulators.

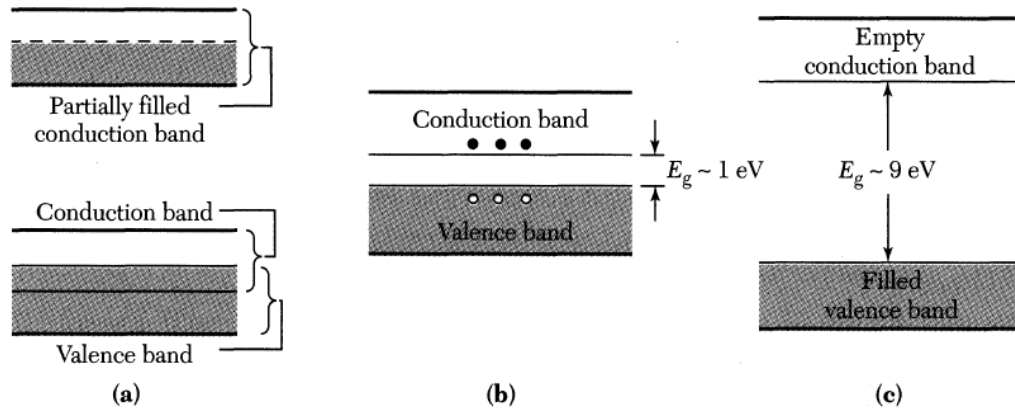


Fig. 19 Schematic energy band representations of (a) a conductor with two possibilities (either the partially filled conduction band shown at the upper portion or the overlapping bands shown at the lower portion), (b) a semiconductor, and (c) an insulator.

Ex. 1061 (Sze), 33. *See also* Ex. 1062 (Streetman) Fig. 3-4 at 68.

16. As shown in Sze's Figure 19(b) above, the energy gap E_g for semiconductors, such as silicon, is on the order of 1 eV. At very low temperatures, all the electrons are in the valence band, and there are no electrons in the conduction band. At room temperature, the value of E_g for silicon is 1.12 eV. The thermal energy at room temperature is a good fraction of E_g . Thus, an appreciable number (about 10^{10} cm^{-3}) of electrons are thermally excited from the valence band to the conduction band. Since there are many available states in the conduction band, a small applied potential and electric field can easily move the electrons in the conduction band and the holes in the valence band in opposite directions. As explained below, impurities are added to silicon used in semiconductor devices to increase the number of electrons in the conduction band or to increase number of holes in the valence band. Ex.1061 (Sze), 33. *See also* Ex. 1062 (Streetman) at 66-68, 73-74 and 86-87.

3. N-Doped Silicon Has Many Free Electrons in the Conduction Band at and a Few Holes in the Valence Band at Room Temperature.

17. When silicon is used in semiconductor devices, small quantities of impurities are added to silicon and the process is referred to as doping. For example, Fig. 23a (below and on left) shows a silicon atom that has been substituted by an arsenic atom with five valence electrons. The arsenic atom forms four covalent bonds with its four neighboring silicon atoms. The extra electron is free to move around and becomes a conduction electron at room temperature.

Ex.1061 (Sze), 37. The silicon substrate becomes *n*-type because of the addition of the electron, which is a negative charge carrier. In the *n*-type silicon, **electrons** are the **majority carriers**, while the **holes** are the **minority carriers**.

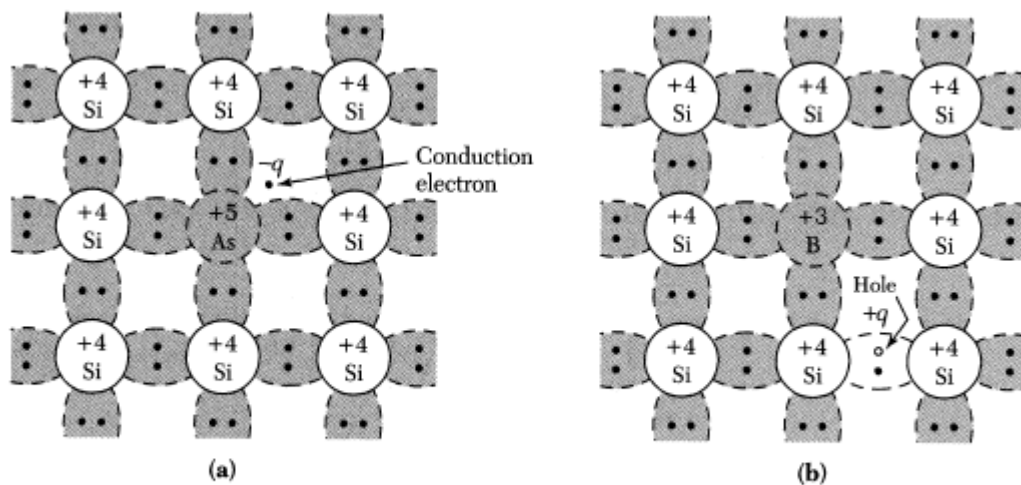


Fig. 23 Schematic bond pictures for (a) *n*-type Si with donor (arsenic) and (b) *p*-type Si with acceptor (boron).

Ex. 1061 (Sze), 38. See also Ex. 1062 (Streetman) Fig. 3-12 at 82.

18. Fig. 23b of Sze shows silicon that has been doped with boron. Because boron has three electrons in its valence shell, it creates a deficit of electrons in the valence shell of the silicon atoms. The deficit creates a positively charged “hole” in the valence band. This results in a *p*-type semiconductor substrate because the holes are positively charged. Like the electron in the *n*-type semiconductor, the *hole* is also free to move around. In the ***p*-type** silicon, **holes** are the **majority carriers** and **electrons** are the **minority carriers**. Undoped silicon has an equal number of electrons and holes. Addition of arsenic increases the total number of electrons making them the majority carriers whereas addition of boron increases the number of holes making them the majority carriers. Thus, what is considered a majority or a minority carrier depends upon the type of dopant (e.g., arsenic or boron) that was added to the substrate. Ex.1061 (Sze), 37. *See also* Ex. 1062 (Streetman) at 66-68, 73-74 and 86-87.

19. In an *n*-type silicon, the conduction electrons are essentially free particles because they are not associated with any particular lattice or donor site. Same is true for holes in a *p*-type semiconductor. Though the carriers are bound to the atoms at low temperature, the bonds are very weak and thermal energy breaks the bonds at room temperature. Importantly, these carriers are not stationary, but are constantly moving in random paths, due to thermal effects, in all directions reaching speeds of about 10^7 cm/second at room temperature. (“*The electrons in*

the semiconductor are therefore moving rapidly in all directions). Ex.1063 (Sze), p. 48. The “motion of an individual electron may be visualized as a succession of random scattering from collisions with [vibrating] lattice atoms, impurity atoms and other scattering centers,” as illustrated in Fig. 1(a) below (the electron is annotated in blue). Ex. 1063 (Sze), p. 48.

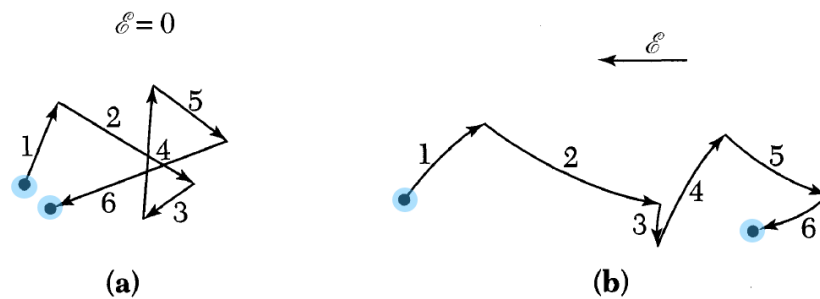


Fig. 1 Schematic path of an electron in a semiconductor. (a) Random thermal motion. (b) Combined motion due to random thermal motion and an applied electric field.

Ex. 1061 (Sze), 48 (annotated). *See also* Ex. 1062 (Streetman) Fig. 3-20 at 98. The random motion of electrons leads to zero net displacement of a group of electrons over a sufficiently long period of time. The average distance between collisions is called *mean free path*, and the average time between collisions is called *mean free time* τ_c . Ex. 1061 (Sze), 48. *See also* Ex. 1062 (Streetman) at 98-99.

20. When an electric field $\mathcal{E}$ (either created due to applied voltages, or self-generated because of doping gradations) is present in an *n*-type silicon (as illustrated in Sze’s Fig. 1(b) above), each electron (which is already in motion) will experience a force from the electric field and will be accelerated in the opposite

direction to the electric field during the time between collisions. Similarly, holes in a p -type silicon would be accelerated in the direction of the electric field. Sze's Fig. 1b above shows the movement of an electron (again annotated in blue) due to the combined effects of random thermal motion and the static electric field. The electrons will *drift* under the influence of the electric field. Same is true when an electric field $\mathcal{E}$ is applied to a p -type silicon except that the holes move in the same direction as the electric field. Ex. 1061 (Sze), 48.

B. A Graded Concentration of Dopants Will Induce a Static Electric Field That, in Turn, Will Cause Carriers to Drift.

1. A Graded Concentration of Dopants Creates a Static Electric Field.

21. In a doped semiconductor device, a graded concentration of dopants that is monotonically increasing or decreasing in a particular direction will induce a static electric drift field. The direction of that field depends upon the type of the dopant and the direction of the grading. For example, if the semiconductor is doped with arsenic, then arsenic becomes a positively charged donor impurity which cannot move in the semiconductor. If the arsenic donor concentration monotonically decreases as a function of depth, it will create a static electric field pointing downwards in the direction of the slope of the graded concentration. The static electric field, in turn, will cause minority charge carriers (holes in n -type)

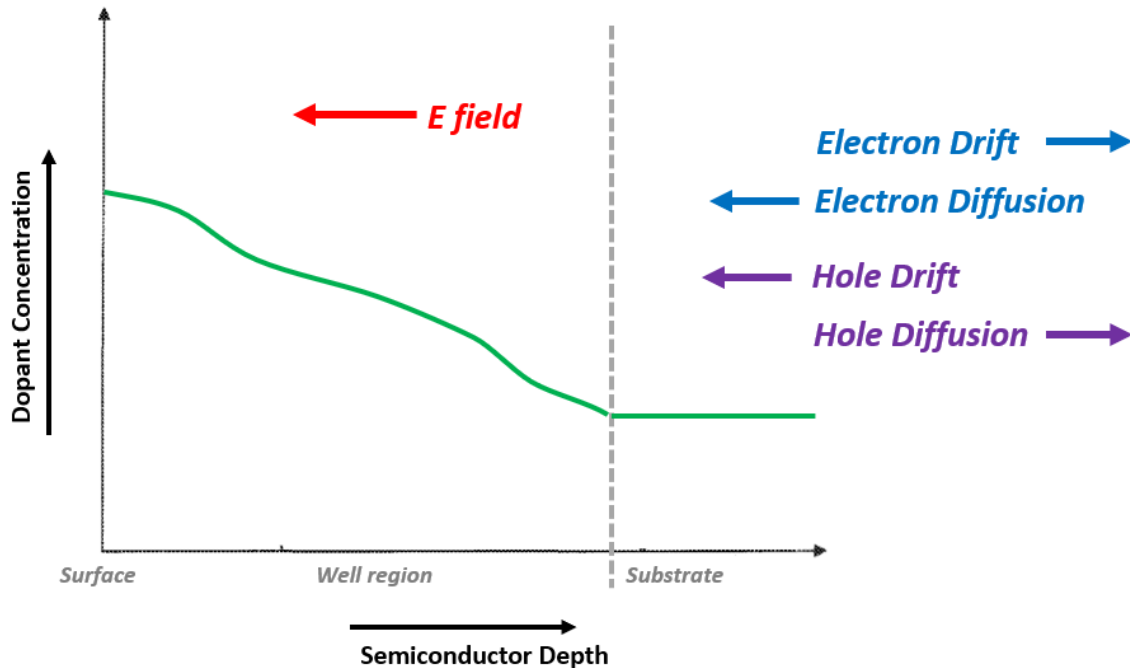
that are already in Brownian motion to move due to drift downwards in the same direction as the electric field.

22. Conversely, if the semiconductor is doped with boron, then boron becomes an immobile negatively charged acceptor ion, unlike the positively charged arsenic donor. If the boron acceptor concentration monotonically decreases as a function of depth, it will create a static electric field pointing towards the surface and opposite to the direction of the slope of the graded concentration. The minority electrons will drift in the direction opposite to the direction of electric field. Note that for both types of doping, if the concentration decreases with depth, static fields are generated which *aid* the movement of the minority carriers via drift away from the surface.

2. Movement of Carriers Due To a Static Electric Field (Drift and Diffusion)

23. Using the graph below of a dopant concentration profile, I will explain how a graded dopant concentration causes carriers to move. I have illustrated a dopant concentration profile as a function of depth through a cross section of a CMOS device—specifically, of the substrate in a semiconductor device with a well region in the substrate. The y-axis denotes dopant concentration and the x-axis denotes the substrate starting with the surface from the left and then moving through the well region deeper into the substrate. The dashed vertical line denotes the position beyond which the dopant concentration is constant in the substrate.

The dopants can be either p -type or n -type. Assume that the dopant profile in the chart below is p -type.



24. Because the concentration of p -type dopants decreases with depth, there will be more p -type dopants near the surface than in the substrate. Holes are the majority carriers and electrons are the minority carriers in p -type silicon. As majority carrier concentrations increase, the minority carrier concentrations correspondingly decrease. In the figure above, the majority carrier hole concentration will decrease to the right, while the minority electron concentration will increase to the right as a function of depth. Since the electrons and holes are in a constant state of motion, there will be a tendency towards movement of the carriers from the high to the low concentration regions by a process known as **diffusion**. The rate of diffusion is proportional to the variation in the concentration

of the carriers. In this case the majority holes will *diffuse* into the substrate, and the minority electrons will *diffuse* towards the surface, as shown by the arrows. *See generally* Ex. 1062 (Streetman) at 98-103 and 134-138.

25. Of course, in the absence of *externally* applied voltages or electric field, there cannot be any *net* movement of either the electrons or holes. Thus, in this case, the diffusion of carriers in one direction *must* be counterbalanced by movement of carriers in the opposite direction. Such a movement is called ***drift***, which occurs due to the static electric field $\mathcal{E}$ shown by the red arrow. The static electric field $\mathcal{E}$ is self-generated due to the decrease in the acceptor impurity concentration from the surface into the substrate. The electric field $\mathcal{E}$ spans the entire length for which the slope is monotonically decreasing and is not *externally* applied. In the figure above, the electric field $\mathcal{E}$ will aid the movement of minority carrier electrons from the surface to the substrate (depicted as Electron Drift in figure above, and—conversely will aid the movement of majority carrier holes from the substrate to the surface (depicted as Hole Drift in figure above). In the above device, ***carrier drift will necessarily occur*** by virtue of the graded (i.e., non-zero sloping) dopant concentration, and the resulting electric field $\mathcal{E}$. Ex. 1061 (Sze), 48, 57. *See generally* Ex. 1062 (Streetman) at 98-103 and 134-138.

26. Carrier *drift* due to electric fields is different than carrier *diffusion*.

Diffusion is governed by concentration gradients of carriers, while drift is dependent on electric fields. Ex. 1061 (Sze), 48, 57.

27. At equilibrium without externally applied voltages, there cannot be any *net movement* of carriers (both electrons or holes). This is because the movement of a given carrier type due to *drift* is counterbalanced by corresponding movement of the same carrier type due to *diffusion*. In equilibrium the product of the majority and minority carrier concentrations is constant.

3. The Prior Art Cited During Prosecution Discloses How A Graded Dopant Concentration Causes Carriers to Drift

28. Prior art patents and textbooks cited during the prosecution of Greenthread patents also confirm that a graded concentration of dopant creates a static electric field, which in turn aids movement of minority carriers due to drift. Figure 3 from Kamins patent (Ex. 1031) “illustrates profiles of doping concentration vs. depth into substrate 19. Curve 24 represents N-type dopants, while curve 26 indicates the P⁺-type doping for photosensors 11, 13 etc. The non-uniform dopant concentration in the substrate creates electric fields in the substrate, indicated by arrows label “E” in . . . Fig. 3.” Ex. 1031 (Kamins) 2:64-9:2.

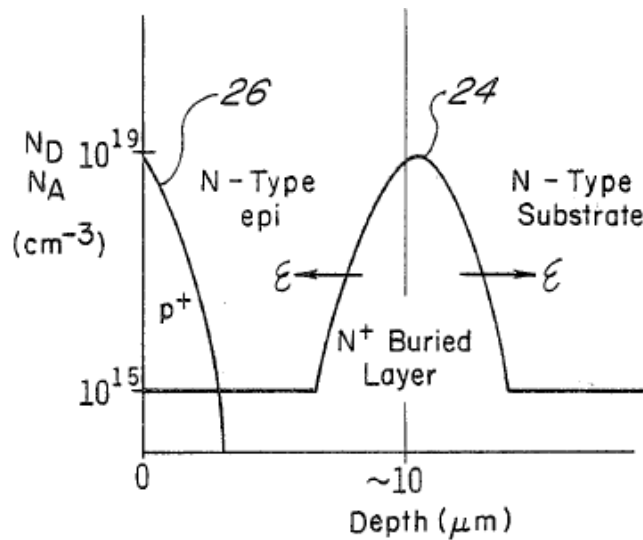


Figure 3

Ex. 1031 (Kamins), Fig. 3. Kamins states that the minority carrier holes created below the maximum dopant concentration are accelerated by the electric field deeper into the substrate (to the right on the graph), while carriers created above the maximum dopant concentration are accelerated towards the surface. *See id.*, 3:8-14. Thus, Kamins confirms that a graded dopant concentration creates a static electric field, which, in turn, moves the majority and minority carriers, opposite to and in the direction of the doping gradient, respectively. Kamins does not mention that a minimum gradient is required to move the carriers or that the carriers need to overcome some opposing force before moving.

29. Likewise, Greenthread cited portions of the book authored by Grove during prosecution. Fig. 7.13 shows the impurity distribution in a *pn*p transistor.

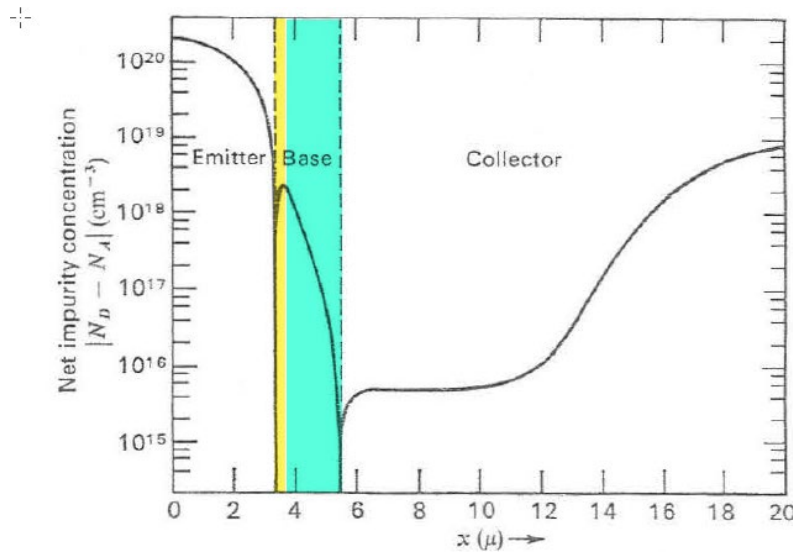
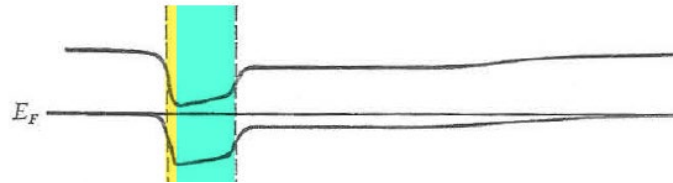


Fig. 7.13 The impurity distribution in the *pnp* transistor. (Estimated on the basis of diffusion conditions.)



Ex. 1068 (Grove), 225 (annotated). When describing the operation of the *pnp* transistor, Grove states as follows:

This same electric field will then be of such direction as to aid the motion of injected holes. Thus *the injected minority carriers will now move not only by diffusion but also by drift* due to the existence of this electric field.

Ex. 1068 (Grove), 225.

30. Grove's diagrams relate to a PNP transistor. Here, the emitter and collector portions are P-type. The downward slope in the emitter region corresponds with a bending downward energy band where the emitter meets the base, as shown in Grove's Figure 7.14 above. The base is N-type and thus the

corresponding energy band bending reflects the emitter-base p-n junction formation. The N-type doping in the base is highest near the emitter-base junction and gradually decreases towards the collector junction. The upward sloping band edge corresponds to an electric field pointing to the right, which causes the holes (minority carriers in the n type base) to drift in the direction of the decreasing donor concentration.

31. Grove's discussion of a gradient that causes an electric field "pushing the electrons toward the emitter-base junction" and the holes in the opposite direction, references the portion that I have highlighted in green above (which is monotonically decreasing as a function of depth).

32. Thus, Grove confirms that a gradient in dopant concentration creates an electric field that causes carriers to move, and that carriers move in the form of both diffusion and drift. Even though Grove refers to bipolar transistors, the disclosure of drift and diffusion of carrier in an electric field is also applicable to movement of carriers in field effect transistors (FET) used to make CMOS devices. Further, while the example shown in Figure 7.13 happens to be described as "quite strongly graded," Grove does not suggest or imply that the drift-related carrier movement hinges on some magnitude of the slope of the graded dopant concentration.

C. Minority Carrier Drift Occurs Based on the Direction of the Electric Field Regardless of “Magnitude” of the Graded Dopant Concentration

33. Carriers drift based on the presence of a static electric field and no minimum magnitude is required to cause the drift. Other factors such as, resistivity, resistance, temperature, and stress, do not impose an opposing force or a barrier that must be overcome before carriers drift under the influence of the static electric field. Though some phenomenon may be described with respect to electrons only in this declaration, similar arguments are true for holes, though the carrier movements will be in opposite directions. *See generally* Ex. 1062 (Streetman) at 98-103 and 134-138.

1. An Electric Field Results in Movement of Carriers Via Drift.

34. For context, when electrons drift under the influence of the static electric field $\mathcal{E}$, the steady-state velocity imparted onto the electrons by the field is called *drift velocity*. As shown in the Sze textbook, the drift velocity of an electron v_n can be expressed as:

$$v_n = -\mu_n * \mathcal{E} \quad [1]$$

where μ_n denotes the mobility of an electron. Ex. 1061 (Sze) at 49. Mobility describes how strongly the motion of a carrier is influenced by a static electric field, or the ease with which carriers can flow through the semiconductor. The mobility of an electron is expressed as:

$$\mu_n = (q\tau_c)/m_n \quad [2]$$

where q denotes the charge on an electron, τ_c is the mean free time and m_n is the mass of the electron. *Id.* Mobility will never be zero at temperatures above absolute zero.

35. The equations for electron drift velocity v_n demonstrate that the movement of an electron is a function of the static electric field and the mobility of the electron. Multiplying a non-zero electric field by the mobility will always yield drift velocity. This confirms that the application of a non-zero static electric field, alone, will aid the movement of the electron opposite to the direction of the field (because of the negative charge of the electron). Put differently, there is no minimum, threshold magnitude of the static electric field required to effect the movement of an electron. The same is true for holes as well.

2. Neither Resistivity nor Resistance Imposes a Barrier to Carrier Movement

36. *Resistivity* is an inherent property of semiconductor materials, including silicon. As shown in the Sze textbook, resistivity ρ of an n -type silicon can be expressed as:

$$\rho = 1/qn\mu_n \quad [3]$$

where q is the charge of an electron, n is the number of electrons per unit volume and μ_n is the mobility of electrons. Ex. 1061 (Sze) at 53-54. Similar expression can be derived for holes too. *Id.*

37. Thus, *resistivity* is function of the number of available carriers and their mobility. If the number of carriers and their mobility goes up, the *resistivity* of the silicon goes down. Thus, the *resistivity* of silicon is analogous to a dynamic friction force, or a drag force, that tends to dampen the drift velocity of carriers in response to an electric field. Importantly, though it imposes a drag, *resistivity* does not bring carriers to a standstill; the carriers will move constantly, as a result of the thermal effects and, if present, the static electric field.

38. Unlike static friction in the mechanical domain (e.g., pushing a stationary box on smooth wood floor vs. pushing the same box on a carpet), *resistivity* does not present a force that the charge carriers would first need to overcome in order to move under the influence of a static electric field (i.e., carrier drift).

39. Further, while *resistivity* is an intrinsic property of a material, which indicates how much it resists current flow per unit length and cross-sectional area, ***resistance R*** refers to the opposition of current flow for a specific piece material with defined physical dimensions. For a semiconductor bar of length L , width w and thickness t , the resistance R of the bar is

$$R = \frac{\rho L}{wt} = \frac{L}{wt} \frac{1}{\sigma} \quad [4]$$

Ex. 1061 (Sze), 51-54.

40. Resistance R , is measured in ohms. Ohm's Law specifies the relationship among resistance R , voltage V , and current I :

$$I = V/R \quad [5]$$

41. As Ohm's Law clarifies, current I is proportional to voltage V ; when a voltage is applied, current flows. Although resistance R opposes or impedes the flow of current, it does not require that a certain *minimum* threshold voltage (V_{th} or V_T) be present (or that the carriers must overcome some sort of barrier) before the current can flow.

3. Aside From Absolute Zero, Changes in Temperature Do Not Preclude Carrier Movement

42. As shown above in Eq. 2, mobility of carriers is related directly to the mean free time between collisions. As temperature increases, the carriers collide more frequently with the vibrating lattice atoms, and thus, mobility decreases (and resistivity increases) with increasing temperature. The increase in temperature, while increasing the drag on the flow of carriers, does not prevent carriers from moving. Again, at room temperatures carriers in the semiconductor are moving rapidly in all directions due to thermal effects, and the built-in electric field caused by a monotonically decreasing graded dopant concentration will result in movement of carriers due to drift.

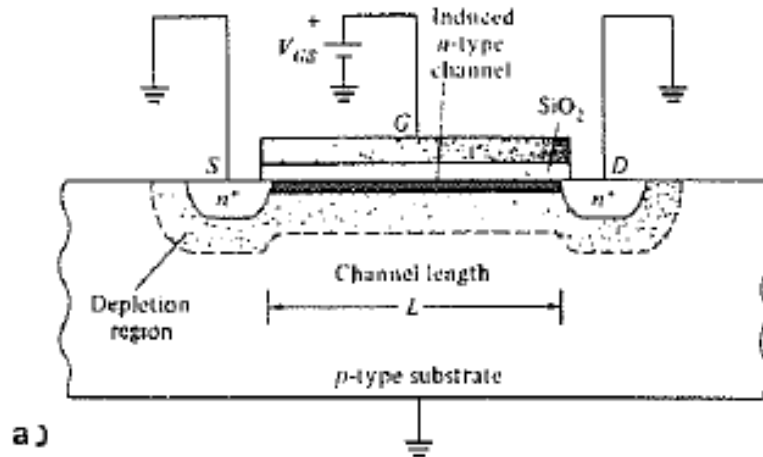
4. Stress Does Not Preclude Carrier Movement

43. Manufacturing steps may induce stress in the silicon lattice. Such stress on the silicon structure can *reduce* resistance of the substrate. Electrons requires tensile stress, while holes require compressive stress. As mentioned above, resistance opposes flow of current but does not impose a barrier that must be overcome in order for carriers to move via drift in response to an electric field. Thus, stress impacts movement of carriers in the same manner as resistance. Implantation may create residual defects which can cause increased scattering and increase resistivity.

D. Threshold Voltage V_T Facilitates Flow of Current in Field Effect Transistors (FETs) and Does Not Impose a Barrier to Movement of Carriers Due to a Static Electric Field

44. Dr. Glew has asserted that a threshold voltage must be applied to a gate to liberate electrons from the silicon atoms and dopant atoms. In order to rebut Dr. Glew's incorrect assertion, I provide how a MOSFET transistor is turned ON by application of threshold voltage at the gate terminal. Figure 4.2(a) below from Wolf depicts an n-type MOSFET formed on a *p*-type substrate. The MOSFET contains an n^+ source region (S), an n^+ drain region (D), and a gate electrode (G) in the middle. The portions between the source (S) and the drain (D) in the substrate is called the channel region. The operation of MOS transistor involves the application of an input voltage to the gate electrode. If no voltage is applied to the

gate electrode, the transistor consists of two back-to-back *pn* junctions and no current flows between the source and the drain.



Ex. 1008C (Wolf Vol. 3) at 137. *See also* Ex. 1062 (Streetman) Fig. 6-10 at 266.

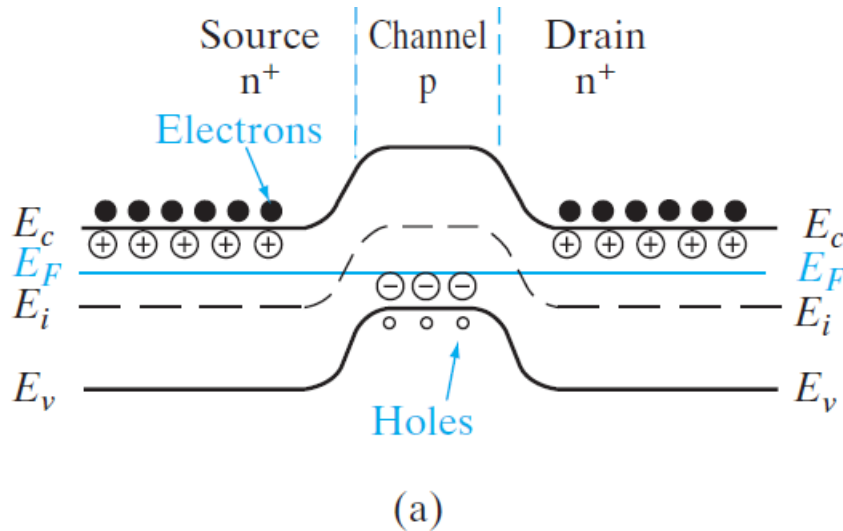
45. Figure 4.2(a) depicts that a positive voltage V_{GS} is applied to the gate. The positive voltage at the gate repels the majority carrier holes in the p-type channel, and attracts electrons to the channel region once the positive voltage at the gate exceeds the so-called threshold voltage so that the applied electric field becomes strong enough to form an *inversion* layer; i.e. an n-type channel is formed in surface of the p-doped channel, that connects the n^+ source and drain regions. In the figure above, “**Depletion region**” depicts the portion of the substrate where the majority carrier holes have been repelled away due to the electric field created by V_{GS} . Due to the voltage V_{GS} at the gate G exceeding V_T , the layer below the gate G now contains an excess of electrons though it has p-type doping. Thus, it is referred to as the *inversion layer* and is depicted as the “**Induced n-type channel**”

in the figure above. A drain current I_D can flow between the source and drain if voltage V_{DS} is applied between the source and the drain. The voltage-induced n -type channel does not form unless the voltage applied to the gate exceeds the threshold voltage V_T . Ex. 1008C (Wolf Vol. 3) at 137. *See also* Ex. 1062 (Streetman) at 265-267.

46. Thus, threshold voltage V_T (also referred to as turn-on voltage) is the minimum gate to source voltage V_{GS} required to create a conducting path between the source and the drain terminals. The charge carriers (electrons and holes) are freely moving in the substrate at room temperature, as described above, and their covalent bonds have been broken due to thermal effects. The threshold voltage V_T does not impact the covalent bonds between carriers in any manner. As explained above, drift of carriers pursuant to a static electric field caused by a graded concentration of dopants will occur even if no external voltage is applied that meets the threshold voltage V_T .

47. Figure 6.10(a) depicts the band diagram at equilibrium along the channel. At equilibrium, no current flows from drain to source and there is no conducting n channel between them. At this stage, Fermi level E_F is flat. Fermi level is the energy level at which there is a fifty per cent chance of finding an electron, and shown in the figure, it is between the conduction band E_c and the valence band E_v . In the source and drain region, the conduction band is close to the

Fermi level, while the valence band is close to the Fermi level in the channel region. This imposes a barrier for an electron to move from the source to the drain, corresponding to the built-in potential of the back-to-back p-n junctions between the source and drain. Ex.1062 (Streetman) at 267.



Ex.1062 (Streetman), Figure 6.10(a), at 266.

48. When a positive voltage is applied to the gate, electrons are attracted to the p -type channel region, and the regions becomes less p -type. As a result, the valence band moves down, farther away from the Fermi level. This reduces the barrier for electrons to move between the source, the drain and the channel. Threshold voltage V_T reduces the barrier sufficiently to enable significant current flow from the source to the drain. The barrier in this context pertains to lateral movement of electrons (or carriers) between the source and the drain through the channel. The carriers are already in the conduction band and are not bonded to the

atoms. This movement of carriers that results in current flow is distinct from the drift movement discussed above. *See also* Ex. 1062 (Streetman) at 265-67.

E. Majority and Minority Carriers in a MOSFET In OFF State

49. In the OFF state in equilibrium without externally applied voltages, there is no current and no *net* movement of carriers between the source and drain regions through the channel. Since the channel, well region and the substrate are *p*-type in the ***n*-type transistor** (NMOS) above, the minority carriers are electrons and the majority carriers are holes. On the other hand, in the n^+ source and drains, electrons are the majority carriers. Once the *p*-type channel is inverted to the *n*-type inversion layer of electrons, it is the electrons that flow from the source, across the inverted channel to the drain. In a ***p*-type transistor** (PMOS), the channel, well region and the substrate are *n*-type, the minority carriers are holes and majority carriers are electron. Such a transistor has a p^+ source and drains, and the holes are majority carriers there.

F. Majority and Minority Carrier in a MOSFET In ON State

50. As mentioned above, to get the ***n*-type transistor** (shown above) in the ON state, a positive voltage is applied to the gate terminal, which repels holes away from the gate, and attracts electrons towards the gate. Movement of carriers leads to excess electrons as compared to the holes in the channel region. In the inverted channel region, the electrons are more numerous than holes. However,

outside the channel region (for example, in the drift layer and in the substrate on Figures 5A-C of Greenthread patents), the minority carriers are still electrons and the majority carriers are still holes because of the *p*-type doping of these regions.

51. To get ***p*-type transistor** in the ON state, a negative voltage is applied to the gate terminal, which repels electrons away from the gate, and attracts holes towards the gate. Movement of carriers leads to excess holes as compared to electrons in the channel region. The inverted channel region will have more holes than electrons. However, because the doping of the channel region is *n*-type, the majority carriers will be electrons and minority carriers will be holes.

G. Channel Stopper Regions Facilitate Isolation in MOSFETs

52. Dr. Glew has stated that the channel stopper regions as disclosed in Kawagoe (Ex.1007) do not facilitate isolation between transistors. In order to respond to Dr. Glew's incorrect statements, below I explain why isolation is needed and how it was achieved before the priority date of the Greenthread patents. MOSFETs need to be isolated to prevent flow of parasitic current between two adjacent transistors. Such current is undesirable as it affects performance of transistors. Figure 2-4 below from Wolf depicts two MOSFET's (MOSFET 1 and MOSFET 2) and the "Field" oxide between the two transistors:

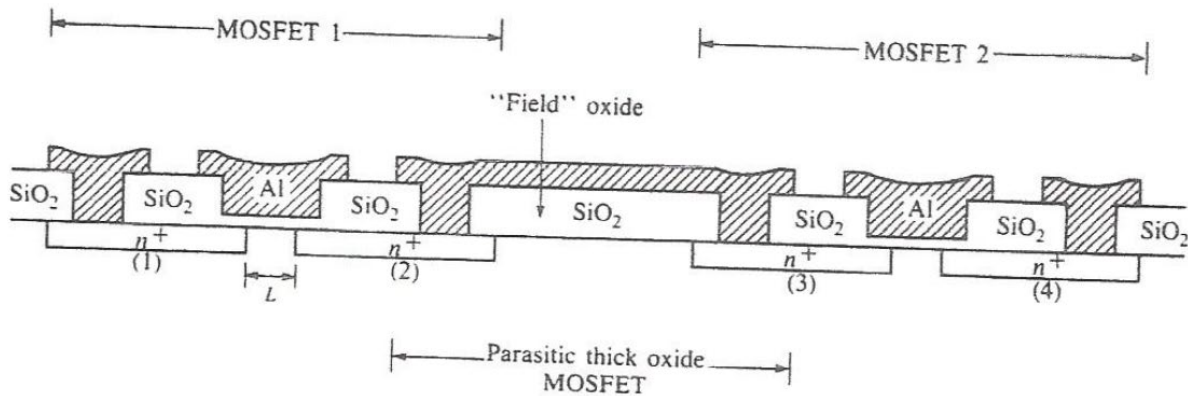


Fig. 2-4 No current should flow between source and drain regions of adjacent MOS transistors. This figure shows the parasitic field transistor with a possible channel under the field oxide if the substrate under this oxide is inverted.¹²⁸ From R. C. Jaeger, *Introduction to Microelectronic Fabrication*. Copyright, 1988, Addison-Wesley. Reprinted with permission.

Ex. 1071 (Wolf Vol. II), Figure 2-4, at 18.

53. The parasitic current can flow between the two MOSFETs through this region. Thus, the field oxide is made several times (e.g., up to seven to ten times) thicker than the gate oxide in the active regions. In addition to the thick field oxide, ion implantation is used to increase the doping under the field oxide. This step is called a **channel-stop implant** and the doped region is referred to as the channel stopper region because it prevents formation of channel between the two MOSFETs. Wolf expressly states that “[t]he **combination of thick oxide and a channel-stop implant can provide adequate isolation for PMOS and NMOS . . . ICs.**” Ex. 1071 (Wolf Vol II) at 18.

54. The thick field oxide can be fabricated in a number of ways. Figure 2-5(a) from Wolf below show two adjacent transistors and the region where the

parasitic transistor can be formed. Figure 2-5(b) and Figure 2-6(c) show two common ways of growing the field oxide. Figure 2-5(b) shows the *grow-oxide-and-etch* approach whereas Figure 2-5(c) depicts the LOCOS approach where the oxide is selectively grown over the desired field regions.

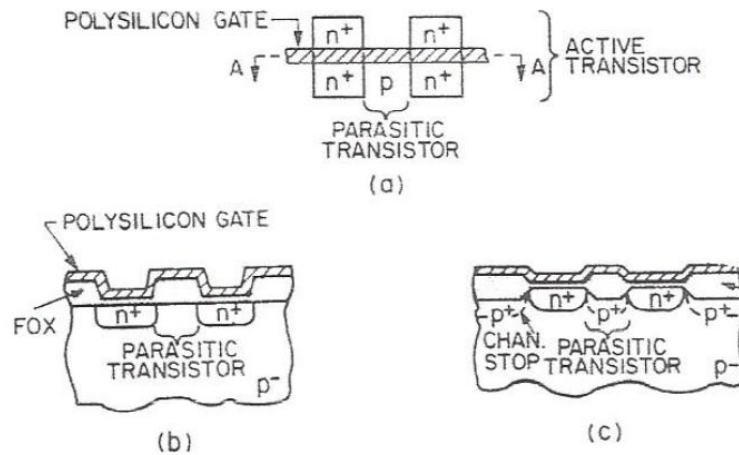


Fig. 2-5 MOSFET isolation. (a) Top view of adjacent MOS transistors with common polysilicon gate illustrating active and parasitic transistor conduction paths. Cross section through A - A for (b) Grow-oxide-and-etch isolation, and (c) LOCOS isolation structures.¹³⁰ From S. M. Sze, Ed., *VLSI Technology*, 2nd Ed., Copyright 1988 McGraw-Hill. Reprinted with permission.

Ex. 1071 (Wolf Vol. II) Figure 2-5 at 19.

55. Figure 6-27 from Wolf depicts isolation of *n*-type and *p*-type transistors in CMOS using channel stop regions below the field oxide regions.

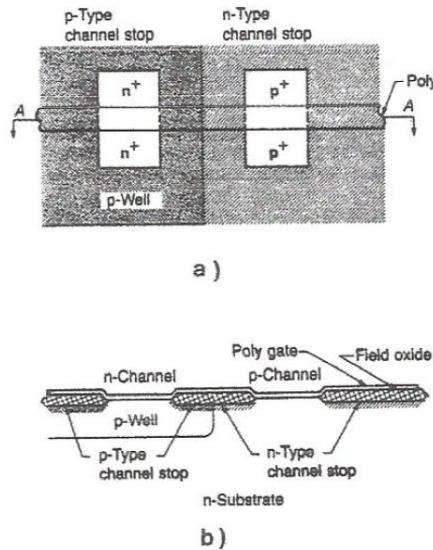


Fig. 6-27 (a) Layout top view of the isolation region between *n*-type and *p*-type transistors in CMOS. (b) Cross sectional view of a CMOS inverter showing the channel stops that are designed to prevent the surface under the field oxide from inverting.⁵³ (© 1986 IEEE).

Ex. 1071 (Wolf Vol II) Figure 6-27, at 420.

56. Kawagoe (Ex.1007) discloses insulating film 3 at least in Figs. 6, 16 and 23 and also mentions, at 8:40-45, that channel stopper regions are formed below the insulating film 3. The disclosure of insulating films and channel stopper regions in Kawagoe (Ex.1007) is consistent with disclosure of techniques for isolating MOS transistors in Wolf discussed above.

V. Dr. Glew's Opinions and Testimony are Flawed in Multiple Respects

A. Dr. Glew's Analysis Rests on an Incorrect Understanding of the Operation of Doped Semiconductors

57. Below I list the opinions and testimony offered by Dr. Glew, and explain by Dr. Glew's opinions are based on an incorrect understanding of how semiconductors operate, and/or why those opinions do not undermine my analysis.

1. Neither "Intrinsic Resistance" or Resistance of Silicon Imposes a Barrier That Carrier Must Overcome Before Moving In Response to a Static Electric Field

58. Dr. Glew has opined that "intrinsic resistance of silicon" creates a barrier to movement of carriers. Ex.2057, ¶50. When asked about intrinsic resistance of silicon during his deposition, he stated that:

Well, you know, silicon has an intrinsic resistance when it's undoped in that -- then as one increases the number of carriers, electrons or holes, based upon a change in temperature, for example, or a -- dopants, then that resistance changes. And one can calculate based upon the number of electrons -- based upon the properties how many electrons are actually free. And that determines -- you know, helps you determine the resistance of the material.

Ex.1063 (Glew-Tr.) at 123:1-13. Elsewhere, he stated that the intrinsic resistance corresponds to resistance R in Ohm's Law ($I = V/R$). Ex.1063 (Glew-Tr.) at 117:4-124:30, 153:18-157:22.

59. Dr. Glew's responses are incorrect. To the extent that he is referring to resistivity of material, that is a property of the material. It does not correspond to resistance R in Ohm's Law. Instead, resistance depends on not only on the type of material, but also its physical dimensions (length, width and thickness) of the

material. As I explained above, neither resistivity nor resistance serves as a barrier that a carrier must overcome in order to drift under the influence of a static electric field. *See supra* Section IV.C.1-2. The resistance of the silicon would affect the *speed* of carrier movement, or the ease of carrier movement in response to an electric field. It would not impose a barrier to the drift of minority carriers caused by the graded dopant concentration.

2. Stress in Silicon Lattice Does Not Impose a Barrier That Carriers Must Overcome Before Drifting

60. Dr. Glew testified during his deposition that mechanical stress may be introduced in the silicon lattice during manufacturing, and may be further affected by ion implantation and annealing, and that such stress creates a force that carriers must overcome in order to drift under the influence of a static electric field. Ex.1063 (Glew Tr.) at 151:10-152:17, 159:1-161:22, 168:14-169:14, 276:6-21.

61. Dr. Glew's reference to stress is incorrect to the extent he implies that stress imposes a barrier that carriers must overcome when drifting in a static electric field. As discussed above, stress affects resistance of the silicon, and resistance does not create a barrier to the movement of carriers. Thus, stress would not impose a barrier that carriers must overcome before they drift. *See supra* Section IV.C.1-2 and 4. Like resistance, stress would impact only the ease of movement. Further, Dr. Glew admitted that "the reality is that usually stress is used to reduce resistance," Ex.1063 (Glew Tr. at 159:17-19, which further undermines Dr. Glew's suggestion that stress could preclude carrier movement.

3. A Minimum Magnitude of the Dopant Concentration Gradient Is Not Required for Carriers to Drift

62. Dr. Glew has opined that “[t]he *magnitude of the concentration gradient* plays a substantial role, because a small gradient may not be sufficient to overcome the resistance of the material in which the gradient exists,” one must compare that magnitude with “any other external forces[] to know whether a drift field would aid the movement of minority carriers.” Ex.2057 (Glew Decl.), ¶50. He testified that charge carriers “can also become mobile under certain circumstances,” Ex.1063 (Glew-Tr. at 102:18-19), and “under certain circumstances electric fields could cause carriers in semiconductors such as silicon to move.” Ex.1063 (Glew-Tr. at 104:18-20). He subsequently clarified what those circumstances are when he testified “*that the mere presence of electric field isn’t sufficient to cause electrons to become charge carriers*. There’s a – essentially a threshold voltage to cause motion as well as resistance to the materials.” Ex.1063 (Glew-Tr. at 105:6-12).

63. Dr. Glew is incorrect. As discussed above, at equilibrium, doped silicon contains free carriers that are constantly in motion, and a graded dopant concentration sloped in a particular direction will—regardless of magnitude—induce an electric field that aids minority carrier movement in that direction. *See supra* Section IV.A, IV.B, and IV.C.1. Dr. Glew’s incorrect opinion may be based on his mistaken belief that all the carriers are bound to atoms even at room

temperature and are not able to drift. He seems to believe incorrectly that a minimum voltage or electric force is required to break the bonds between the carriers (electrons) and the atoms.

4. At Room Temperature, Doped Semiconductors Contain Carriers In Conduction Band That Are Not Bound to the Dopant or Silicon Atoms

64. Dr. Glew testified that the excess carriers (i.e., electrons) in an *n*-type semiconductor are not free but weakly bound to the silicon or dopant atoms. He further testified that a minimum force is needed free the excess electron. For example, Dr. Glew testified that “there’s also *a threshold voltage to liberate an extra electron from a crystal structure.*” Ex.1063 (Glew Tr.) at 107:8-10. He reiterated that “[a] *small enough voltage won’t make an electron free or liberate it from the atom it’s bonded to. A large voltage will.*” Ex.1063 (Glew Tr.) at 108:6-8. Dr. Glew believes that in a semiconductor “*all the electrons are not free to move,*” Ex.1063 (Glew Tr.) at 123:14-15, and that the “inherent resistance in silicon is based on the fact that it’s a semiconductor with a very, very small fraction of its electrons are in the conduction band.” Ex. 1063 (Glew Tr.) at 123:14-19. *See also* Ex.1063 (Glew Tr.) at 102:10-103:20, 103:21-107:10-108:11, 115:17-116:17.

65. Dr. Glew is incorrect. As explained above, at room temperature, the excess electrons in a doped semiconductor are not bound to the silicon or the

dopant nuclei. The bonds between the electrons in the conduction band and the atoms are easily broken by thermal energy at room temperature. *See supra* Section IV.A and IV.B. Thus, the carriers are constantly subjected to thermal motion. Dr. Glew mentioned that a ***threshold voltage*** is needed to liberate the extra carrier electrons. As further discussed below, Dr. Glew is incorrect.

66. Dr. Glew is also incorrect about his statement that the electrons are not free to move, and also mistaken about the relationship between the inherent resistance of silicon and the number of electrons in the conduction band. As discussed above, the carriers are free to move, and resistivity is inversely proportional to the number of electrons per unit volume in the conduction band. *See supra* Section IV.C.1-2.

5. Threshold Voltage V_T Enables Flow of Current In a MOSFET And Does not “Liberate” Extra Electrons From A Crystal Structure

67. Dr. Glew testified that a threshold voltage V_T is needed to free conduction electrons from silicon and dopant atoms. In particular, he stated that “***a threshold voltage [is needed] to liberate an extra electron from a crystal structure.***” Ex.1063 (Glew-Tr.) at 107:8-10. Dr. Glew made several statements about threshold voltage:

- “So there’s a threshold voltage to turn on the transistor so that there is current flow from the source to gate.” Ex.1063 (Glew Tr.) at 128:10-12.

- “There’s also another threshold . . . But there’s *another minimum voltage that would be required to free an extra electron from the crystal structure of silicon.*” Ex.1063 (Glew Tr.) at 107:13-17.
- “I don’t believe that I ever testified or wrote that there was a threshold voltage that would cause the . . . the extra electrons to be liberated.” Ex.1063 (Glew Tr.) at 131:9-15.
- “I spoke of a certain threshold or energy or voltage required to free an electron from – a weakly bound electron from a dopant that’s incorporated into a silicon crystal lattice.” Ex. 1063 (Glew-Tr.) at 133:2-5.
- “There is a voltage required to free electrons, whether they’re weakly bonded or other types, in this case the weakly bonded extra electrons. But I never opined that one necessarily did that.” Ex. 1063 (Glew-Tr.) at 137:10-15.
- “The dopant field that is graded is pulling minority carriers that have been enabled, freed, when the *gate electrode has a voltage applied to it of sufficient magnitude.*” Ex. 1063 (Glew-Tr.) at 145:10-14.
- “I mean, I would put it that the *gate voltage needs to free the electrons and holes from the crystal lattice.* Of course, there’s atoms there, but I think of it more as the properties of the crystal in this sense.” Ex. 1063 (Glew Tr.) at 147:5-9.

68. In short, Dr. Glew seems to have testified that the application of the threshold voltage V_T at the gate releases electrons from the lattice and the released electrons can facilitate current flow. *See also* Ex. 1063 (Glew Tr.) at 147:2-9, 144:20-145:14, 130:2-131:3, 136:13-21, 137:1-15.

69. Dr. Glew is incorrect for several reasons. First, as discussed above, the threshold voltage V_T in MOSFETs refers to the minimum voltage needed to enable current to flow from source to drain. *See supra* Section IV.D. If a positive

voltage is applied at the gate, it repels the holes and attracts electrons. The threshold voltage is not required to free carriers from silicon or dopant atoms to conduct current. Dr. Glew seems to be conflating threshold voltage V_T with “another threshold voltage” that is supposedly needed to liberate the electrons. Dr. Glew initially stated that threshold voltage V_T applied to the **gate** to turn ON the transistor is different than the another threshold voltage needed to liberate the electrons. Later he stated that the voltage to the **gate** liberates the electrons. The two concepts are completely different. Threshold voltage V_T at the gate is needed to turn on the transistor but does not liberate electrons from their atoms. ***There is no such concept of a threshold voltage to liberate electrons.*** If that were to be true, Ohm’s law, one of the most fundamental laws of electric circuits, would need to be rewritten to read $I = (V - V_T)/R$.

70. Second, as discussed above, at room temperatures, doped silicon will have carriers in the conduction band that are not bound to any atom. *See supra* Section IV.A and IV.B. Dr. Glew’s inability to articulate what this “another threshold voltage” is and his inability to distinguish it from V_T which is used to turn on a transistor implies that he does not understand how carriers operate in semiconductors. As discussed above, bandgap energy E_g determines when an electron can move from the valence band to the conduction band. That concept is totally unrelated to threshold voltage needed to turn a transistor ON.

71. Third, I note that Dr. Glew was asked whether any book on semiconductor device physics or a technical paper describe how to determine the “threshold voltage” needed to liberate the extra electron. Ex.1063 (Glew Tr.) at 110:4-115:16. In response, Dr. Glew could not identify any such textbooks or technical papers. He seems to equate such techniques to techniques used to measure resistance when he stated that “[i]t’s *essentially a resistance measurement*. At some point there’s a resistance of a certain value, and at a higher voltage that resistance will break down because current starts flowing.” Ex. 1063 (Glew Tr.) at 111:20-112:2. Dr. Glew also referred to “TCAD programs” but again as examples of how to measure “resistance values at different doping concentrations.” Ex. 1063 (Glew Tr.) at 113:6-7.

72. Dr. Glew is again incorrect. His inability to identify a textbook or a technical paper that describes the “threshold voltage” to liberate the extra electron in this context simply underscores that no such threshold exists. By equating this concept to techniques that measure resistance, Dr. Glew seems to simply obfuscate the issue.

6. At Equilibrium With No External Voltages, There Is No Net Flow of Current, But Carriers Move Via *Drift* and *Diffusion*,

73. During his deposition, Dr. Glew testified that in a semiconductor device, even in the presence of a graded dopant concentration, *carriers will not*

move unless an external voltage is applied (i.e., in order to turn the device ON).

“When it is off, there is no motion of carriers. Again, I've made this point a number of times.” Ex. 1063 (Glew Tr.) at 52:3-22. He further testified:

Q. There may not be any net movement of carriers or there may not be any net flow of current, but the carriers are in motion even though the transistors is not operating; is that correct?

A. To me, the question makes no sense. It's nonsensical. The movement of carriers is current. So I just can't fathom what you're asking.

Q. Okay. So if the transistor's sitting there and it is not operating but there is a dopant electric field, is your testimony that the electrons would not be in motion?

A. It's my testimony that when the current -- excuse me -- when the transistor is off, there should be ***no net current flow*** in the transistor and that the channel region should not become electron rich and hole poor.

Ex.1063 (Glew Deposition Tr.) at 50:10-51:3. *See also id.* at 55:7-20.

74. Dr. Glew testified that it is his “understanding that there’s no movement until the voltage is applied to the gate electrode. Once the gate electrode is **on**, then there is movement. Meanwhile, the gradient that exists when the transistor’s in the ‘**off**’ state merely provides a force but not enough force to move the charges.” Ex. 1063 (Glew Tr.) at 41:4-9; *see also id.* at 49:22-51:6.

75. Dr. Glew also testified that in an *n*-type semiconductor, “[e]lectrons oscillate at very high frequencies with their neighbors,” Ex.1063 (Glew Tr.) at

82:14-15, and “electrons trade places with their nearest neighbor periodically.” *Id.*, at 84:11-12. *See also id.*, at 84:15-87:17.

76. Thus, Dr. Glew testified that absent an external electric field, there will be no net movement of carriers even if a static electric field is present. He testified that the carriers are not moving but oscillating about their position resulting in no net movement. To clarify, to a person of ordinary skill in the art, an external voltage in this context refers to voltage that may be applied to a transistor (e.g., at the source, the drain, the gate, or to the substrate) from an external power source. It does not refer to the electric field created by a graded dopant concentration, which is a “*built-in*” field.

77. In my opinion, Dr. Glew’s assessment is fundamentally incorrect. While Dr. Glew is correct that there will be no net movement of carriers absent an external force, he is incorrect about the movement of carriers. As explained above, doped silicon contains free carriers. If a static electric field is present due to a gradient of doped concentration, the carriers will *drift* due to the electric field but will also *diffuse* in the opposite direction to ensure there is no net movement of carriers. *See supra* Section IV.A, IV.B, and IV.C.1.

78. Because Dr. Glew believes that a “threshold voltage” is required to “liberate” the carriers from the lattice, it appears he is forced to argue that there will not be any movement of carriers due to drift or diffusion if the “threshold

voltage” is absent. He incorrectly believes that in such a situation, the carriers will simply oscillate in place and not drift and diffuse. Though Dr. Glew seems to be aware of drift and diffusion, Ex. 1063 (Glew-Tr.) at 58:3-20, it seems that he is forced to ignore them because of this belief that a “threshold voltage” is needed to free the carriers. Because Dr. Glew has taken the untenable position that carriers must overcome opposing forces before they can drift under the influence of a static electric field, he is forced to take other incorrect positions. For example, Dr. Glew testified that carriers will not drift occur under the influence of a static electric field, and that a static electric field by itself cannot induce movement, and if it did, it would result in a non-functioning device. Ex.1063 (Glew Tr.) at 50:10-51:16, 55:7-57:17, 108:6-8. It appears that Dr. Glew is forced to take this position because he incorrectly believes that carriers do not drift and diffuse, and that an external voltage needs to be applied to dislodge the carriers.

7. At Room Temperature, Thermal Effects Will Move Carriers From Valence to Conduction Bands

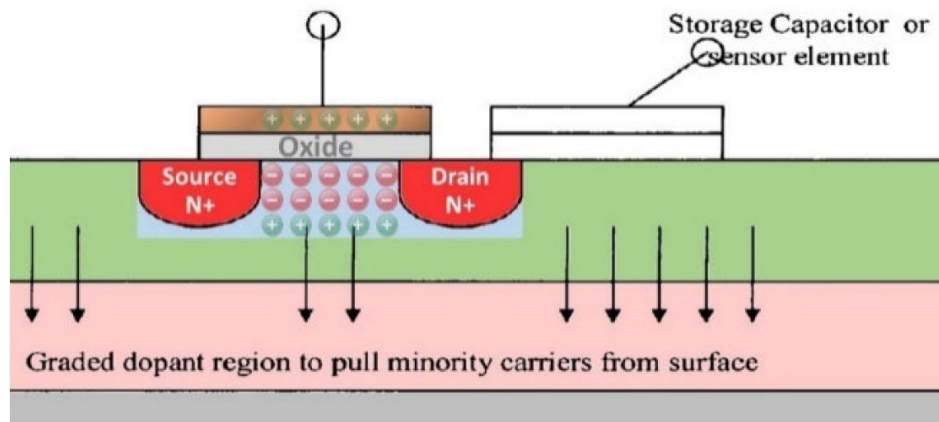
79. When asked about “other forces” that act on carriers, Dr. Glew states that “solid-state devices are complicated, so there’s potentially things like thermal effects. Chips get warm when they operate. So there are thermoelectric effects” Ex.1063 (Glew-Tr.) at 73:1-4.

80. Dr. Glew is incorrect to the extent he considered thermal effects as increasing the temperature of chips. He did not elaborate the impact of thermal

effects beyond increasing the temperature. As described above, thermal effects cause carriers to move from valence to conduction bands, and the become free. *See supra* Section IV.C.2-3. The carriers are then free to move in response to a static electric field. Dr. Glew’s mention of thermal effects undermines his statement that a minimum threshold voltage is needed to “liberate” the carriers.

8. Identity of Majority and Minority Carriers Does Not Change When a MOSFET is Turned ON

81. Dr. Glew provided the annotated Fig. 5B in his declaration and described its operation. Ex. 2057, ¶¶36, 37. Dr. Glew explained that when a positive voltage is applied at the gate, electrons are attracted to the surface whereas the holes are repelled away from the surface. *Id.* He further explained that the graded concentration of dopants pulls the carriers from silicon’s surface, and with reference to the annotated Fig. 5b below, Dr. Glew stated that figure depicts pulling holes from the surface layer. *Id.* at ¶37.



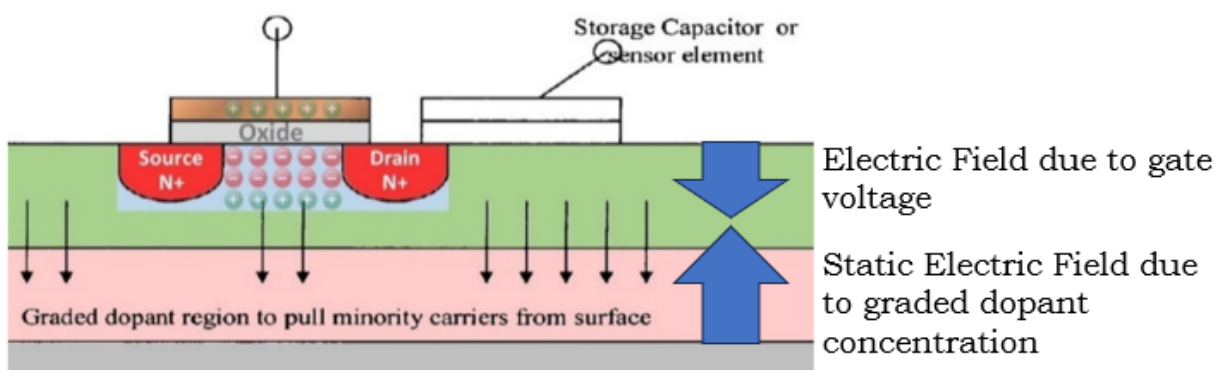
Ex. 2057, p. 17.

82. When testifying about annotated Fig. 5B from his declaration (excerpted above), consistent with his report, Dr. Glew testified that “*The arrows and the text refers to pulling minority carriers from the surface, meaning the holes.*” Ex. 1063 (Glew Tr.) at 142:13-15. My review of his declaration and testimony indicates that he believes that what are majority carriers and minority carriers depends upon the operation of the transistor. In the above example, when a positive gate voltage is applied, the channel region can have more electrons and less holes. Dr. Glew believes that the majority carriers in this situation are electron and minority carriers are holes. Thus, he asserts that the arrows depict movement of holes.

83. Dr. Glew is incorrect in believing that the holes are minority carriers in the channel of the transistor depicted in Fig. 5B. As explained above, when a gate voltage in excess of V_T is applied to an *n*-type FET, the inversion layer will have more electrons than holes. *See supra* Section IV.D. However, the term “majority carrier” refers to the carrier type that is provided by the dopants; the other type is the “minority carrier.” In the *p*-type channel, well, and substrate, the minority carriers are electrons and majority carriers are holes. Regardless of the fact that once the channel is inverted, there is an excess of electrons compared to holes in the inversion region. In a *n*-type channel, well and substrate, the minority

carriers are holes and the majority carriers are electrons. *See* Ex. 1061 (Sze) at 37 (discussing donors and acceptors). *See supra* Section IV.E and IV.F.

84. Further, it is clear that Dr. Glew has not fully considered the consequences of limiting his analysis to only the ON state of the transistor. If a positive voltage is applied at the gate, it creates an electric field pointing towards the substrate. As Dr. Glew noted, the field pulls the electrons towards the surface. However, deeper in the substrate, the effect of gate voltage is no longer felt. The graded dopant concentration in the p -type substrate creates a field pointing towards the surface, which pulls the minority carriers (electrons) towards the substrate. I have depicted the field created by the gate voltage at the right side of the figure for clarity instead of its true location. This electric field will be present in the channel below the gate.



85. Dr. Glew's fundamental misunderstanding of how carriers operate in a doped semiconductor leads to a cascade of erroneous statements. For example, he has to define majority and minority carriers based on the operation of a transistor

in defiance of the conventional usage of such terms. *See supra* Section IV.B, IV.E and IV.F.

9. Neither Inadvertent Diodes nor Capacitance Imposes a Barrier That Carriers Must Overcome When Drifting

86. When asked about other factors that affect carrier movement, Dr. Glew testified that “[f]urthermore, there may be *internal diode* – you know, *inadvertent diodes*. There may be resistance in capacitance form that causes a slowing of motion. So there are a number of things that can cause degradation of the motion of charged particles associated with the desired benefits of this invention.” Ex.1063 (Glew-Tr. at 277:5-12). As for capacitance, when questioned about the impact of resistance on the movement of carriers, Dr. Glew mentioned that “if there were resistance, of a given value in the channel region would diminish the source-drain current. It would have some other effects, capacitance formation but – as well. Well, not capacitance formation but R – capacitance time resistance time delay issues.” Ex.1063 (Glew Tr.) at 157:21-158:5.

87. In my opinion, Dr. Glew’s testimony regarding capacitance and inadvertent diodes is irrelevant. He discussed capacitance in the context of RC time constant. The RC time constant is a measure of how long it takes for a voltage or current to rise or fall. It does not have any bearing on the issue whether the carriers are drifting in response to a static electric field created by a graded dopant concentration.

88. Dr. Glew's statements about inadvertent diodes are irrelevant too. To begin with the term is not a commonly used term in the art. Dr. Glew is most likely referring to an inadvertent diode that can form between a source/drain to the channel/well region because such regions have opposite doping types. All diodes in equilibrium have minority carriers on either side of the junction that drift across the depletion region where the doping is graded from p to n type or vice versa. This drift is counterbalanced by diffusion of majority carriers; i.e. holes from *p* to *n* side, and electrons from *n* to *p* side. Again, such diodes are routine in all semiconductors (including in Greenthread patents and in prior art) and they have no bearing on whether the carriers are drifting in response to a static electric field created by a graded dopant concentration.

10. Channel Stopper Region Facilitates Isolation between MOSFETs

89. When questioned about the disclosure of channel stopper region in Kawagoe during his deposition, Dr. Glew testified that though the channel stopper region is to stop the spread of the channel, it would not achieve isolation between FET devices. Ex.1063 (Glew Tr.) at 232:6-237:2.

90. Dr. Glew is incorrect. As discussed above, Wolf states channel stopper regions have been used in the industry along with field oxide (usually grown by LOCOS method) to achieve isolation between adjacent transistors. *See supra* Section IV.G. Kawagoe's (Ex.1007) disclosure of using a channel stopper

region below the insulating film 3 is consistent with the disclosure of Wolf. Thus, a POSITA would understand that the insulating film along with the channel stopper region provides isolation.

B. Dr. Glew Failed to Analyze Transistors In Their OFF State and Did Not Consider *Drift* of Carriers

91. Dr. Glew testified that he had “*not performed an analysis of . . . counterbalances of drift or of drift itself.*” Ex.1063 (Glew Tr. at 63:13-15). He reiterated that “I don’t believe I’ve addressed ‘off’ state diffusion and balance in my report while I was rebutting the positions I was asked to rebut. That goes beyond anything I’ve thought and considered for the purposes of this report.” Ex.1063 (Glew Tr. at 65:10-15).

92. Dr. Glew testified that he has not considered the **OFF** state activity of the devices disclosed in the prior art references in formulating his opinions.

Q So maybe I should state that you don't have a position or you have not analyzed whether the electrons will drift from the surface towards the substrate when a dopant electric field is present but the transistor is not operating? Is that a fair statement?

A I think it's a fair statement to say it's my opinion that there will be no net drift in that this is a functional transistor intended to store memory bits or image bits.

Beyond that, *I haven't performed an additional analysis of the balance of any stat- --any “off” state activity.*

Ex.1063 (Glew Tr). at 62:10-22:

93. Dr. Glew also confirmed that the challenged claims are apparatus claims. Ex.1063 (Glew Tr.) at 209:9-14 (“It’s not a process patent claim. It’s an apparatus. So the limitations – the requirements do not require a specific process. The realities of manufacturing are that one must make it, but’s not – how one makes it isn’t claimed in the elements of the apparatus claims”); Ex.1063 (Glew Tr. at 209:17-22 “I would say generally how a CMOS apparatus or CMOS device operates isn’t exactly a claim element. There are aspects of these claims that describe what some of these structures do. But I wouldn’t characterize that as the general operation of a CMOS”); Ex.1063 (Glew Tr. at 210:7-6 “***Claim 1 is not a process or method claims. It’s really an apparatus claim. It’s describing structures here.***”).

94. In view of the testimony cited above, it is clear that Dr. Glew did not consider transistors in the OFF state, i.e., when no gate voltage is applied, and the transistor is OFF. Because Dr. Glew believes that electrons cannot move in an OFF state and a threshold voltage V_T is needed to liberate the electrons, he concludes that the carriers will drift only when the transistor is ON and when threshold voltage has been applied. Thus, he seems to be only considering the ON state of the transistor, i.e., when a threshold voltage V_T has been applied to the gate terminal to facilitate flow of current between the source and the drain terminals. As described above, if an *n*-type device (NMOS) is ON and a gate voltage has been

applied, a channel inversion layer forms to allow current to flow from the source to drain. The external gate voltage creates an additional, stronger, electric field in channel region, but pointing in the *opposite direction* (i.e., from the surface into the substrate). That additional electric field in the channel induces electron carrier drift *toward the surface*, that—within that layer—will overwhelm the electron carrier drift due to built-in electric field. *See supra* Section IV.A and IV.B.

95. Based on the portions of the deposition transcript I have cited above, it appears that Dr. Glew is misreading the claims to specifically require a ***net movement*** of carriers, or a “net current.” However, the claims do not speak to the ***net movement*** of carriers. Rather, the claims require structural features of the device — here, a “graded dopant concentration” that is capable of aiding the movement of carriers. While I do not dispute Dr. Glew’s assessment that an external voltage must be applied in order to cause ***net movement*** of carriers, or ***net current*** to flow, that is beside the point, because even at equilibrium (i.e., where no external voltages are applied to the device) ***minority carriers will move via drift*** by virtue of the static electric field alone. Further, while all of the challenged claims are to a “device,” an externally applied voltage is, by definition, outside of the device. That also indicates that the claims are not concerned with the effects of external forces or fields on the device. Dr. Glew seems to require “net movement”

of carriers because he believes that the movement only occurs when a gate voltage liberates the carriers and thus, the claims cover only the ON state of the transistor.

C. Dr. Glew Had Only Glanced at the File History As He Did Not Consider it Relevant, But Greenthread Made Technical Representations During Prosecution That Support My Analysis

96. I reviewed the prosecution history of the Greenthread patents when preparing my initial declaration. I believe that Greenthread's statement made to the USPTO during prosecution are consistent with my explanation above, and how a POSITA would interpret those statements.

97. For example, Greenthread itself cited pages 224-225 of the Grove textbook during prosecution of the Greenthread patents. The cited portion of the book mirrors the description above regarding the effect of static electric field on the carriers. Greenthread also expressed to the USPTO that "the graded dopant concentration itself creates a "built-in" electrical field that forces the movement of carriers into a particular direction," and that "a unidirectional drift (electric) field necessarily affects all the present minority carriers in the same way - moving all minority carriers in the same direction because of the unidirectional drift due to the existence of the electric field." Ex.1016 ('195 File History) at 289-90. These representations are consistent with my above discussion that minority carrier movement via drift occurs solely due to the built-in field induced by a monotonically decreasing graded dopant concentration.

98. During the deposition, Dr. Glew admitted that he had only “glanced” at the prosecution history, because—according to him—“**[i]t didn’t seem relevant** to ... any of the issues I was rebutting at the time.” Ex.1063-Glew-Tr. 179:18-180:6. In my opinion, this is a glaring omission from his analysis, because the above statements of the file history are technical representations that speak to what level of disclosure in the prior art is sufficient to demonstrate the “aid carrier movement” term.

VI. Dr. Glew’s Other Analyses of Petitioner’s Grounds are Incorrect

A. Kawagoe’s First Active Region Includes a “Second Doping Type”

99. Dr. Glew argues that “Kawagoe does not disclose or suggest ‘a first active region . . . with a second doping type opposite in conductivity to the first doping type.’” Glew-Decl., ¶58. Specifically, he argues that “[t]he channel of transistor 4N is doped N-type, because it is the top portion of a p-well (as shown in Figure 23 of Kawagoe)....A POSITA would have understood that the channel in a CMOS transistor has the same doping type as the well in which the source and drain are formed. All three material sections are p-type without any n-type: (1) the channel of NMOS 4N made from the p-well; (2) the p-well; (3) and the p-type substrate are all doped p-type.” *Id.*, ¶59. I disagree with Dr. Glew’s analysis for multiple reasons.

100. First, Dr. Glew assumes that the claim term at issue requires that the “second doping type” must span the through the entirety of the claimed “first active region.” However, the plain and ordinary meaning of “first active region...with a second doping type” does not mandate this. As to Kawagoe’s transistor 4N, as I explained in my opening declaration, IPR2024-00016 (’842 Patent), Ex. 1003, ¶79, n-type dopants, which are a “second doping type” relative to the p-type, are included in Kawagoe’s source and drain regions 4Na and 4Nb. Dr. Glew does not appear to dispute this. That satisfied the disputed term under its plain and ordinary meaning. Whether or not the “second doping type” is included in the channel region of transistor 4N specifically, is beyond the scope of the claim.

101. Second, even assuming that Dr. Glew’s construction were correct (i.e., assuming that the “second doping type” must be included in all regions of the identified “first active region”), his argument completely ignores Kawagoe’s transistor 4P that is also shown and described in Figure 23. As a POSITA would have recognized, that transistor 4P is constructed within n-well 6n. Subsequently, the source and drain regions of transistor 4P (4Pa and 4Pb) are formed by doping p-type dopants. Nonetheless, n-type dopants remain present in those source and drain regions (4Pa and 4Pb). Accordingly, *all three regions* of transistor 4P (the source, drain, and channel) will include n-type dopants. Accordingly, even under

Dr. Glew's construction (which is incorrect), in my opinion Kawagoe's transistor 4P qualifies as the claimed "first active region...with a second doping type opposite in conductivity to the first doping type."

B. Kawagoe Includes an "Isolation Region"

102. I have seen that Dr. Glew argues that my "Kawagoe-based analysis is incorrect regarding the 'first active region and second active region are each separated by at least one isolation region' limitation (Dependent claims 7 and 15)." Glew-Decl., §IX.D. Specifically, he argues that "a POSITA would have understood that the first and second active regions extend to about the depth of the epitaxial layer 2E and abut each other laterally, and therefore they are not separated by Kawagoe's field insulating film 3, as required by claims 7 and 15. The field insulating film 3 is formed '[o]ver principal surface of the epitaxial layer 2E' (Ex. 1007, 8:40-42) and a POSITA would have understood that it does not extend deep enough to separate the two active regions." IPR2024-00016 ('842 Patent), Ex. 2057, Glew-Decl., ¶63. I disagree with Dr. Glew's analysis for multiple reasons.

103. First, Dr. Glew assumes that "isolation region" must "extend deep enough" to achieve complete physical "separat[ion]" of the identified active regions. However, there is nothing in the claim to suggest that such complete physical separation is required. Kawagoe clearly shows field insulating region 3 as separating the first and second active regions in Figure 23. Kawagoe further

teaches that the region is “made of SiO₂ or the like,” which was well understood at the time of the alleged invention as used for electrically isolating components. Under the plain and ordinary meaning, a POSITA would have understood Figure 23 as including a “first and second active region...separated by at least one isolation region,” as required. I further note that while Kawagoe contemplates examples where active regions are “formed in the range of the thickness of the epitaxial layer 2E,” Kawagoe also teaches such active regions having a depth significantly less than that of epitaxial layer 2E—for example, active regions that are 0.5 μm deep, versus epitaxial layer 2E that are 5 μm deep. Ex.1007 (Kawagoe), 8:36-40, 9:3-6, 9:47-53, 17:22-25.

104. Second, Dr. Glew’s critique completely neglects Kawagoe’s disclosure that “a channel stopper region is formed below the field insulating film 3, although not shown” in Figure 23. Ex. 1007 (Kawagoe), 8:43-45. I referenced that feature as well, in my analysis for the “isolation region” requirement of claims 7 and 15. *See* IPR2024-00016 (’842 Patent), Ex.1003, ¶103. Kawagoe illustrates the “channel stopper region” later, as elements 16a and 16b in Figure 26(A). Ex. 1007 (Kawagoe), 20:54-56; Fig. 26(A). Importantly, the channel stopper regions 16a and 16b are shown as extending below the active regions on either side of field insulating film 3. Accordingly, even assuming that the claimed “isolation region” must achieve complete physical separation of the first and second active regions,

Kawagoe's collective disclosure of the field insulating film 3 and channel stopper regions in Figure 23 would satisfy that requirement. I have provided above a short description of what a channel stopper region is, how it is formed, and how a POSITA would understand that the insulating region and channel stopper region disclosed in Kawagoe collectively provide isolation between the active regions. *See supra* Section IV.G.

Executed on November 8, 2024

Respectfully submitted,

A handwritten signature in blue ink that reads "Sanjay Banerjee". The signature is written in a cursive, flowing style.

Sanjay Banerjee