

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

CIRRUS LOGIC, INC. and
OMNIVISION TECHNOLOGIES, INC.
Petitioners,

v.

GREENTHREAD, LLC,
Patent Owner.

Case IPR2024-00021
U.S. Patent 11,121,222

DECLARATION OF ALEXANDER D. GLEW

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I, Alexander D. Glew, declare as follows:

I. INTRODUCTION

1. My name is Alexander D. Glew. I have been retained on behalf of Greenthread, LLC (“Greenthread”), and its counsel, McKool Smith, P.C., as an expert with regard to this matter. I understand Cirrus Logic, Inc. (“Cirrus”), OmniVision Technologies, Inc. (“OmniVision”), and ams Sensors USA, Inc. (“ams”) (collectively, “Petitioner”) filed a Petition (Paper No. 1) for *inter partes* review (IPR) of U.S. Patent No. 11,121,222 (“the ’222 patent” or “the Challenged Patent”) (Ex. 1001).

2. I have been asked to consider, and provide my independent analysis and opinions regarding, whether the alleged prior art references cited in this proceeding disclose or suggest the features recited in claim 44 (“the Challenged Claim”) of the ’222 patent, which I understand Petitioner has challenged in this IPR. In my view, the alleged prior art references do neither. My opinions and conclusions are fully discussed in later sections of this declaration. This declaration is based on the information currently available to me.

3. I am an independent consultant, and I am not, and have never been, an employee of Greenthread or Petitioner. I am being compensated at my consulting rate of \$700 per hour for my work related to this matter. I received no compensation

for this declaration beyond my normal hourly compensation based on my time actually spent analyzing the Challenged Patent, the prosecution history of the Challenged Patent and related applications, the alleged prior art publications relied upon by Petitioner, the declaration of Petitioner's expert Dr. Sanjay Banerjee, and other related materials (discussed below in Section III). My compensation is not dependent on the outcome of this IPR or the testimony or opinions that I give.

4. I understand a copy of my curriculum vitae is submitted as Ex. 2061, and it sets forth my educational experience, employment history, and publications.

II. BACKGROUND AND QUALIFICATIONS

5. I earned a B.S. degree in Mechanical Engineering in 1985 and a M.S. degree in Mechanical Engineering in 1987 from the University of California, Berkeley.

6. I earned a M.S. degree in Materials Science and Engineering in 1995 and a Ph.D. in Materials Science and Engineering in 2003 from Stanford University.

7. I am the Founder and President of Glew Engineering Consulting, Inc., based in Mountain View, California. I have been President of Glew Engineering Consulting, Inc. since I started the company in 1997. In my role as President, I have provided consulting services to clients in the field of semiconductor manufacturing and materials, as well as to clients in other fields. I have reviewed and analyzed semiconductor technologies and products. My consulting work has involved semiconductor process equipment, thin film deposition and characterization, process development, project turnaround/rescue, gas flow and vacuum metrology, design of experiments, corrosive gas applications, finite element analysis, and related market analysis.

8. I have over 30 years of experience in semiconductor manufacturing and materials, including in semiconductor equipment and processing. I have implemented numerous manufacturing processes for the formation of semiconductors, including chemical vapor deposition (“CVD”), plasma enhanced

chemical vapor deposition (“PECVD”), high density plasma chemical vapor deposition (“HDPCVD”), etch processing (including dry plasma and wet processing), reactive-ion etching (“RIE”), chemical-mechanical planarization (“CMP”), spin-on dielectrics (“SOD”), epitaxy (“EPI”), molecular beam epitaxy (“MBE”), rapid thermal processing (“RTP”), and others.

9. In 1987, before receiving my Ph.D., I worked at Applied Materials, Inc. in Santa Clara, California. At Applied Materials, Inc., I served in a number of roles, including Engineering Manager, Core-Technologist Project Manager, CVD Supplier Quality Engineering Manager, Core Technologist, CVD Engineering Manager, and Systems Engineer. In these roles, I provided engineering services and supervised other employees on projects related to technologies used to manufacture semiconductors, including CVD, epitaxy, physical vapor deposition (“PVD”), rapid thermal processing (“RTP”), etch, and thermal. I oversaw gas, vacuum, and chemical component evaluation, testing, and supplier quality management. I successfully proposed and executed a project to develop industry methods to determine the effects of trace chemicals on semiconductor processing and equipment reliability. I worked on the development and release of the Precision 5000 CVD product, the first cluster tool for semiconductor manufacturing.

10. I have used alpha particles to perform hydrogen forward scattering (HFS) and Rutherford Back Scattering (RBS) in materials analysis of thin films on

silicon wafers. I am generally familiar with the effects of alpha particles fired at silicon wafers.

11. I am a licensed professional mechanical engineer in the state of California.

12. I have published articles and presented on topics related to semiconductor manufacturing. My curriculum vitae includes a list of selected publications.

13. I am a co-inventor of five U.S. patents: (a) U.S. Patent No. 6,204,174, directed to a method and apparatus to control the deposition rate of material in a semiconductor fabrication process; (b) U.S. Patent No. 9,224,626 and 10,395,593, directed to a method of forming a heater assembly for use in semiconductor processing; and (c) U.S. Patent Nos. 6,679,476 and 7,118,090, both directed to control valves for use in ultra pure applications such as semiconductor processing. I have another patent application pending.

14. I am a member of the American Society of Mechanical Engineers (“ASME”), International Microelectronics and Packaging Society (“IMAPS”), Materials Research Society (“MRS”), Institute of Electrical and Electronics Engineers (“IEEE”), and Semiconductor Equipment and Materials International (“SEMI”).

15. I am qualified to render an opinion regarding the design and development of semiconductor manufacturing devices and semiconductor materials based on my experience. Based on my expertise and qualifications, I am qualified to provide an opinion as to what a person of ordinary skill in the art would have understood, known, or concluded as of 2004.

III. SCOPE OF ASSIGNMENT AND MATERIALS CONSIDERED

16. The opinions contained in this declaration are based on the documents that I reviewed, my professional judgment, as well as my education, experience, and knowledge regarding technologies related to the Challenged Patent. In preparing this Declaration, I am relying on my own knowledge and expertise as well as the following documents:

- The Challenged Patent (Ex. 1001);
- Other patents that I understand are in the same family as the Challenged Patent, including:
 - U.S. Patent No. 8,421,195 to Dr. G.R. Mohan Rao (“the ’195 patent”) (Ex. 2062);
 - U.S. Patent No. 10,510,842 to Dr. G.R. Mohan Rao (“the ’842 patent”) (Ex. 2063);
 - U.S. Patent No. 9,190,502 to Dr. G.R. Mohan Rao (“the ’502 patent”) (Ex. 2064);

- U.S. Patent No. 10,734,481 to Dr. G.R. Mohan Rao (“the ’481 patent”) (Ex. 2065);
 - U.S. Patent No. 11,316,014 to Dr. G.R. Mohan Rao (“the ’014 patent”) (Ex. 2066);
- Prosecution histories for the Challenged Patent and the other patents in the same family (listed above), which I understand constitute the exchange of correspondence between the Patent Office and the applicant (Ex. 1002; Exs. 2067-2071);
- Petitioner’s IPR petitions in Nos. IPR2024-00001 (regarding the ’481 patent), IPR2024-00016 (regarding the ’842 patent), IPR2024-00017 (regarding the ’195 patent), IPR2024-00018 (regarding the ’502 patent), IPR2024-00019 (regarding the ’014 patent), and IPR2024-00020 and -00021 (regarding the ’222 patent);
- Declaration of Dr. Sanjay Banerjee (Ex. 1003), who I understand is Petitioner’s expert in this IPR and the other IPR proceedings listed above (his declaration is Ex. 1003 in each of those IPR proceedings);
- Petitioner’s exhibits 1001-1022, 1027, 1030, 1032-1033, 1037-1038, and 1042-1043 in this IPR; and
- Any other references/documents cited within this Declaration.

IV. LEVEL OF ORDINARY SKILL IN THE ART

17. Based on my review of the Challenged Patent, the types of problems encountered in the art at and prior to the time of the alleged invention, prior solutions to those problems, the pace with which innovations were made during the relevant time period, the sophistication of the technology, and the educational level of active professionals in the field, I believe that a person of ordinary skill in the art (POSITA), at the time of the alleged invention, would have had at least a Bachelor's of Science degree in electrical or computer engineering, materials science, chemical engineering, applied physics, or a related field, with emphasis on semiconductor manufacturing, or an equivalent degree, and at least four years of experience in semiconductor design and manufacturing. Additional education in a relevant field or industry experience may compensate for a deficit in one of the other aspects of the requirements stated above.

18. All of my opinions in this declaration are from the perspective of a POSITA, as I have defined it above and during the relevant time frame (e.g., late 2004, including the period up to September 3, 2004, which I understand is the earliest claimed priority date of the Challenged Patent). During this time frame, I possessed at least the qualifications of a POSITA, as defined above.

V. RELEVANT LEGAL PRINCIPLES

19. For the purposes of this Declaration, I have been informed about certain aspects of the law that are relevant to my analysis and opinions. I have applied these legal principles in rendering my opinions below.

A. Claim Construction

20. I understand that the ordinary and customary meaning of a claim term is the meaning that the term would have to a POSITA at the time of the effective filing date of the patent application that matured into the patent-at-issue. For the Challenged Patent, this is September 3, 2004. In the absence of an express intent on the part of the inventor to give a special meaning to the claim terms, the words are presumed to take on the ordinary and customary meanings attributed to them by a POSITA.

21. I understand that it is the use of the words in the context of the written description, and as customarily used by those skilled in the relevant art, that accurately reflects both the ordinary and the customary meaning of the terms in the claims.

22. I understand that the basis for a term's ordinary and customary meaning may be derived from a variety of sources, including the words of the claims themselves, the remainder of the specification, the prosecution history, and extrinsic

evidence concerning relevant scientific principles, the meaning of technical terms, and the state of the art at the time of the invention.

23. I have been instructed that dictionary definitions or definitions from technical references can be used to inform or confirm the ordinary and customary meaning of words found in a claim, but that in construing claim terms, the general meanings gleaned from reference sources, such as dictionaries, must always be compared against the use of the terms in the context of the claim itself, and the intrinsic record must always be consulted to identify which of the different possible dictionary meanings is most consistent with the use of the words by the inventor.

24. I understand that a patent applicant is entitled to be his or her own lexicographer (in other words, provide his or her own meaning to a word or phrase) and may rebut the presumption that claim terms are to be given their plain and ordinary meaning. To do so, the applicant must clearly set forth a definition of the term that is different from its ordinary and customary meaning.

25. Where the applicant provides an explicit definition for a term, that definition will control interpretation of the term as it is used in the claim in which it appears. I understand that the specification can also be relied on for more than just explicit lexicography to determine the meaning of a claim term. For example, I understand that the meaning of a particular claim term may also be determined by

implication, that is, according to the usage of the term in the context of the specification.

B. Anticipation

26. I understand that under U.S. Patent Law, 35 U.S.C. § 102, a claim is invalid as anticipated if a single prior art reference discloses each and every limitation of the claimed invention.

27. I am informed that a reference is anticipatory if it contains the claim elements in the same order as claimed, regardless of whether the prior art and the claimed invention are directed to achieving the same purpose.

28. I understand that a prior art reference may anticipate a claim without expressly disclosing a feature of the claimed invention if that missing feature is necessarily present, or inherent, in the single anticipating reference.

29. I am informed that inherency requires more than a probability or possibility that a claimed feature is present in the prior art, but rather that the feature or characteristic is a necessary part of the prior art. I also am informed that recognition of the inherency by a POSITA— at the time— is not required.

C. Obviousness

30. I understand that under U.S. Patent Law, 35 U.S.C. § 103, a claim is invalid as obvious if the differences sought to be patented and the prior art are such

that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

31. I am informed that an obviousness analysis requires an assessment of the scope and content of the prior art, the differences between the art and the claims at issue, and the level of ordinary skill in the art. I am told that it is against this backdrop that obviousness is assessed.

32. I am informed that a person of ordinary skill in the art (POSITA) is a hypothetical person who is presumed to be aware of all the pertinent prior art. I am also informed that an obviousness analysis may take account of the inferences and creative steps that a POSITA would employ.

VI. THE CHALLENGED PATENT

A. Background Technology Regarding Dopants

33. Silicon is an example of a semiconductor. In its pure form, it is typically an insulator, but it can become an electrical conductor when impurities called “dopants” are added into the silicon crystal. These dopants are often phosphorous or boron atoms that have one more or one less valence electron than a silicon atom. If the dopant has one less valence electron, then it creates what is called a “hole” where there was an electron, which can be thought of as a positive unit of charge. The extra electrons or holes disturb the local charge equilibrium in the silicon and can become mobile in response to electric fields. Thus, the electrons and holes are called “charge carriers.” These dopants can also change the local net electrical charge distribution in the surrounding silicon, influencing the motion of other charge carriers passing by. When the dopant concentration is graded in a particular direction, other charge carriers will move in the gradient direction (or opposite direction) depending on the charge carrier’s polarity. This phenomenon is called “carrier drift.”

B. Overview of Challenged Patent

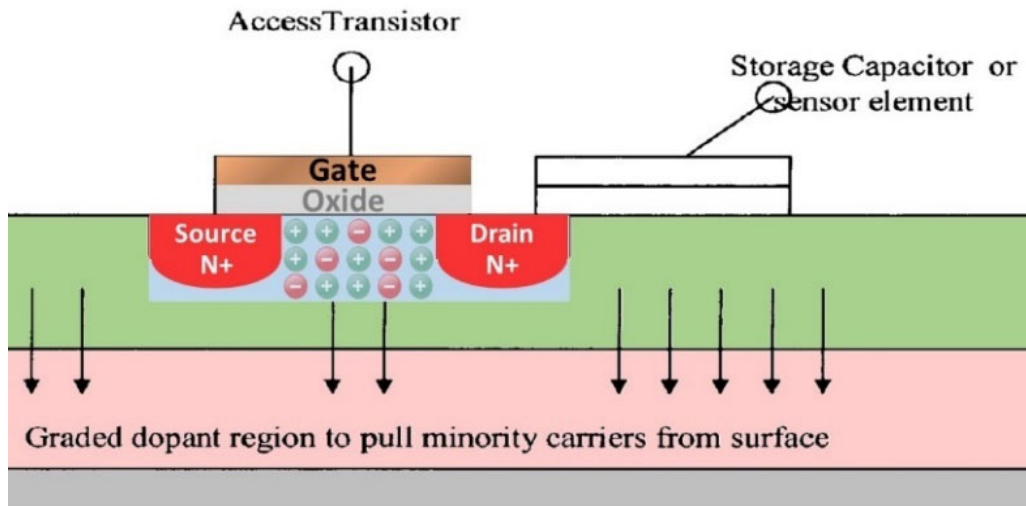
34. At the time of invention of the Challenged Patent, most semiconductor devices relied on spatially uniform concentrations of dopants. Ex. 1001 (Challenged Patent), Abstract, 1:48-63. Dr. Rao (the inventor named on the Challenged Patent)

recognized, however, that graded concentrations of dopants can be used to improve certain aspects of the performance of transistors and other semiconductor devices. *Id.*, Abstract, 3:25-35, 3:56-58. The claimed invention is clearly disclosed in, e.g., Figs. 5B-5C of the Challenged Patent, and the corresponding parts of the specification.

35. A surface-channel MOSFET is a common type of transistor capable of controlling current flow at or along the surface of the semiconductor substrate. Ex. 2059 (Chen textbook), 27 (“carriers propagate at the semiconductor surface”). Figure 5B shows an NMOS¹ transistor that is formed in a p-type surface layer. The transistor comprises (1) a gate; (2) a thin oxide separating the gate from the surface layer; and (3) two doped regions called the source and drain (shaded red). Ex. 1001, 3:31-34 (“electrons can be swept from source to drain”), 3:64-66 (“accelerate majority carriers towards the drain”). In Fig. 5B, which is annotated below, the N⁺ means these regions are heavily doped with an n-type dopant that creates a surplus

¹ MOS stands for “metal oxide semiconductor.”

of negative carriers (i.e., electrons).² The specification explains that the NMOS transistor in Fig. 5B can be a surface-channel MOSFET.

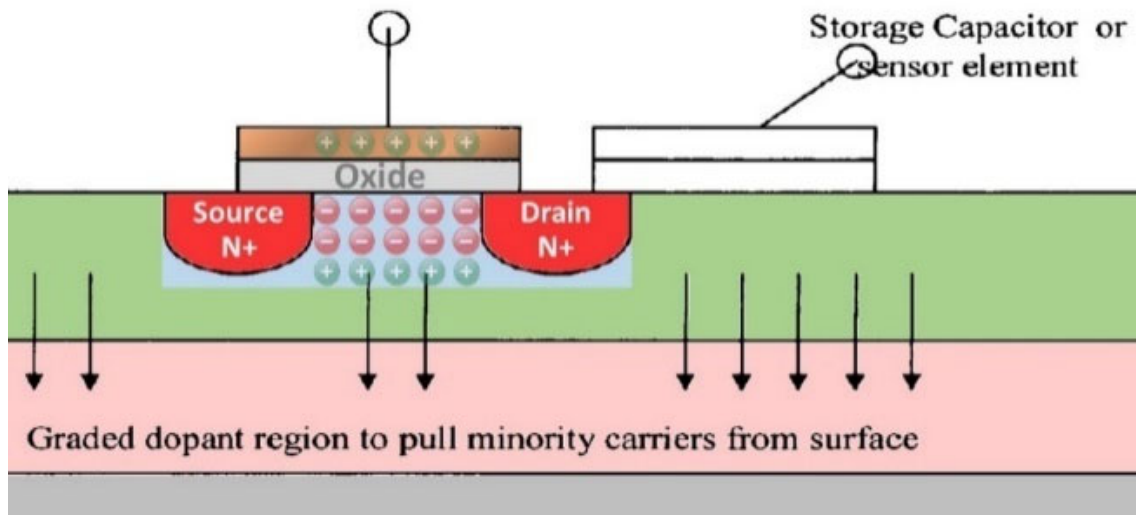


Id., Fig. 5B (annotated); *see also id.*, 3:64-66. Meanwhile, the p-type silicon between the source and drain (shaded blue) has an abundance of positively charged holes (green circles). When the holes separate the source’s electrons from the drain’s electrons, current cannot flow through the transistor, and the transistor is in an “off” state.

36. When a positive voltage is applied to the gate, an electric field forms in the oxide. This positive electric field repels the “positive” holes downwards, while

² An “N” region or layer has more electrons, and thus a “negative charge.” A “P” layer has more holes, and a “positive charge.” A “+” or “-” means heavily or lightly doped.

the negative electrons (red circles) are attracted to move into the blue surface layer. When enough electrons have accumulated in the surface layer below the oxide, they form a conductive channel (as annotated in Figure 5B below) of electrons between the source and the drain, and current can begin to flow through the transistor.



Ex. 1001, FIG. 5B (annotated).³ In order to turn the transistor “off,” the positive voltage is removed from the gate and the channel disappears as the holes return to the surface layer.

37. Dr. Rao (the inventor named on the Challenged Patent) recognized that by using graded concentrations of dopants in the well region and a drift layer (shaded pink), it is possible to “pull” carriers from the silicon’s surface. Ex. 1001, Fig. 5B

³ Because the channel is formed by electrons with a negative charge, the MOSFET is referred to as an n-channel MOSFET, and the “minority carriers” are holes.

(annotated above). In this example, pulling the holes from the surface layer when a positive voltage is applied to the gate, allows the transistor to turn “on” more quickly.

This improves the speed and performance of the transistor. Ex. 1001, 3:30-35.

VII. OVERVIEW OF ALLEGED PRIOR ART

38. Dr. Banerjee's declaration relies on the Payne (Ex. 1005) reference for single-reference obviousness in Ground I, anticipation by Onoda (Ex. 1042 is an English-language translation of the Japanese patent application Ex. 1043) in Ground II, and obviousness over Onoda in view of Wolf (Exs. 1008A-1008D) in Ground III. Ex. 1003, ¶¶32-34. Below, I provide overviews of relevant portions of Payne and Onoda.

A. Payne (Ex. 1005)

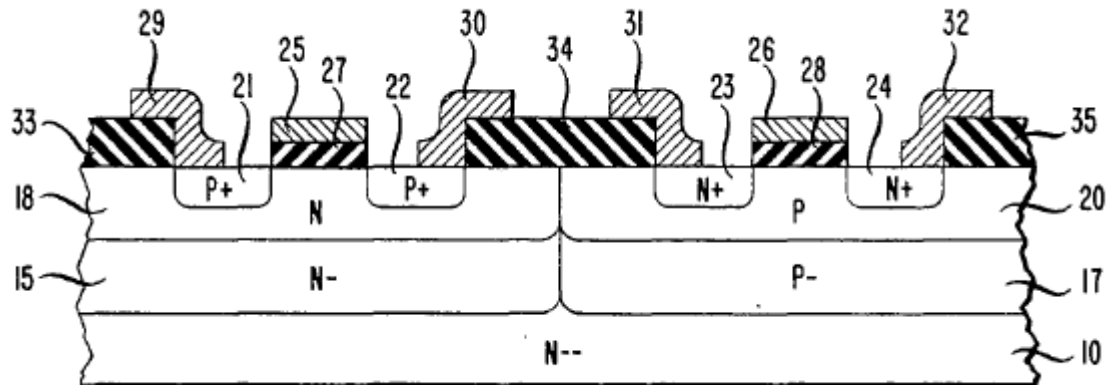
39. The Petition's first ground is single-reference obviousness over Payne (Ex. 1005). Pet., 7. Below is an overview of pertinent portions of Payne relevant to the present dispute.

40. Payne is a patent that "relates to complementary field effect transistors formed by ion implantation, and in particular to a structure and method of fabrication which permit high packing density." Ex. 1005, 1:5-8. Much of the Petition's discussion focuses on Figures 10 and 11 of Payne. Payne describes a CMOS device shown in Figure 10 (shown below):

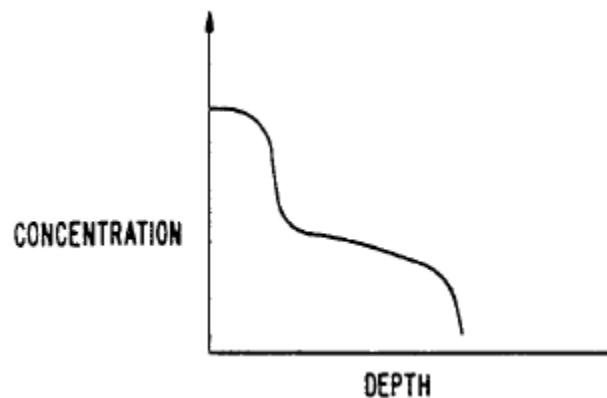
The oxide layer can then be stripped off, for example, with a solution of dilute HF, and fabrication may proceed in accordance with standard techniques to produce the CMOS device depicted in FIG. 10. The p-channel device includes source and drain regions, 21 and 22, respectively, of P⁺ conductivity type formed

with the N surface region, 18. Similarly, the n-channel device includes source and drain regions, 23 and 24, of N + conductivity type formed within the P surface region 20.

Id., 5:18-27.



Id., FIG. 10. Figure 10 shows an N- tub 15 and a P- tub 17. *Id.*, 3:35-39 (describing N- tub 15), 4:12-14, 5:3-5 (describing P- tub 17). Payne discloses that after a heating step, “[t]he resulting impurity profile in both tubs thereby has the general shape illustrated in FIG. 11, where the abscissa is depth and the ordinate is impurity concentration.” *Id.*, 5:14-17.



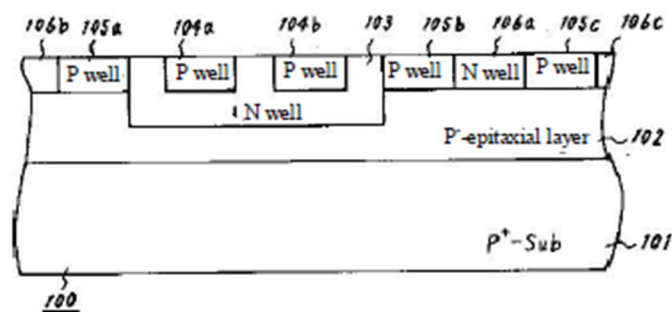
Id., FIG. 11; *see also id.*, 2:38-41 (“FIG. 11 is an illustration of the approximate concentration of implanted impurities as a function of depth in the semiconductor for a device in accordance with one embodiment of [Payne].”).

B. Onoda (Ex. 1042)

41. The Petition's second ground relies on Onoda (Ex. 1042) for anticipation, and the third ground relies on Onoda as the primary reference for an obviousness combination. Pet., 7. Below is an overview of pertinent portions of Onoda relevant to the present dispute.

42. Onoda discloses a nonvolatile semiconductor storage device with a cross-section as shown below in Figure 2.

[FIG. 2]



Ex. 1042, FIG. 2.

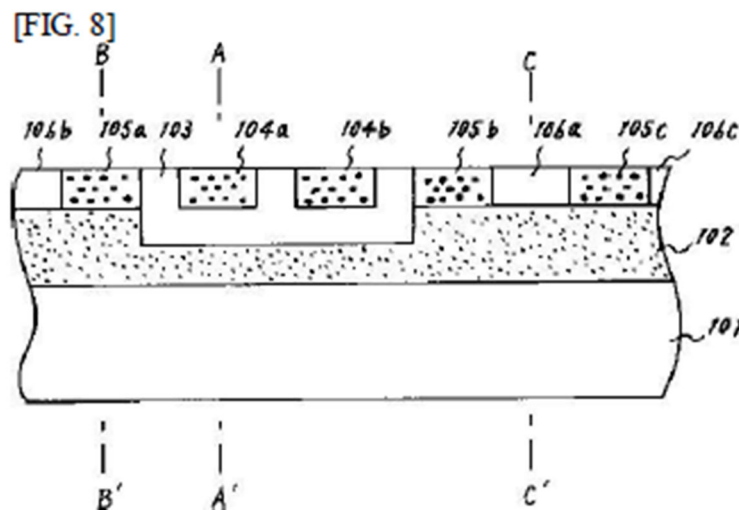
43. Onoda discloses that:

A lightly-doped P-type epitaxial layer 102a is formed on the surface of a first semiconductor layer 101 that is made from a heavily-doped P-type silicon substrate. Boron [B] is implanted into the surface of this epitaxial layer 102a and a heat treatment is carried out to produce a lightly-doped P-type second semiconductor layer 102. Regions other than a desire region are masked, phosphorus is implanted, and a heat treatment is carried

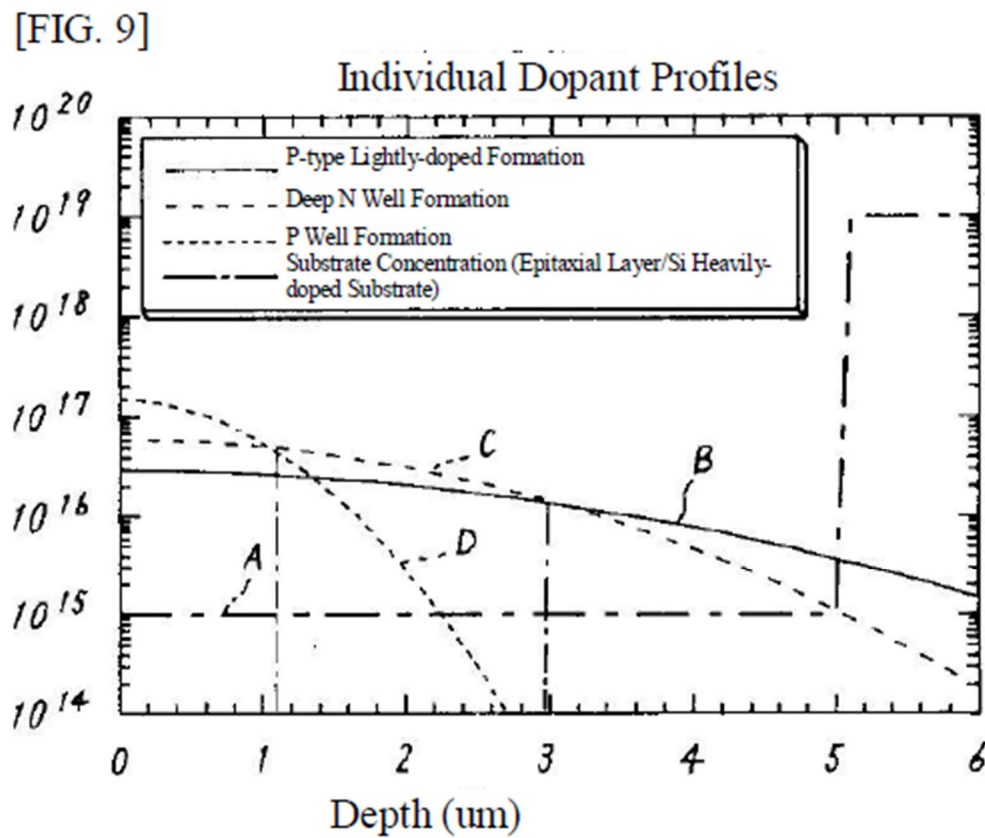
out to form an N-type first well region 103. Regions other than the desired region are masked, boron [B] is implanted, and the boron implantation layer is then masked and phosphorus is implanted, and a heat treatment is carried out to form P-type second well regions 104a and 104b, P-type third well regions 105a through 105c, and N-type fourth well regions 106a through 106c.

Id., Abstract.

44. Onoda discloses performing carrying out a heat treatment to thermally diffuse the boron and phosphorus of the boron implantation layers 104A, 104B, 105A, 105B, and 105C to form, as illustrated below in FIG. 8, P-type second well regions 104a and 140b and P-type third well regions 106a through 106c, and N-type fourth well regions 106a through 106c, in the surface of the second semiconductor layer 102. The dopant concentration due to the boron at this time is depicted by the dotted line D shown in FIG. 9 (below). *Id.*, ¶[0050].

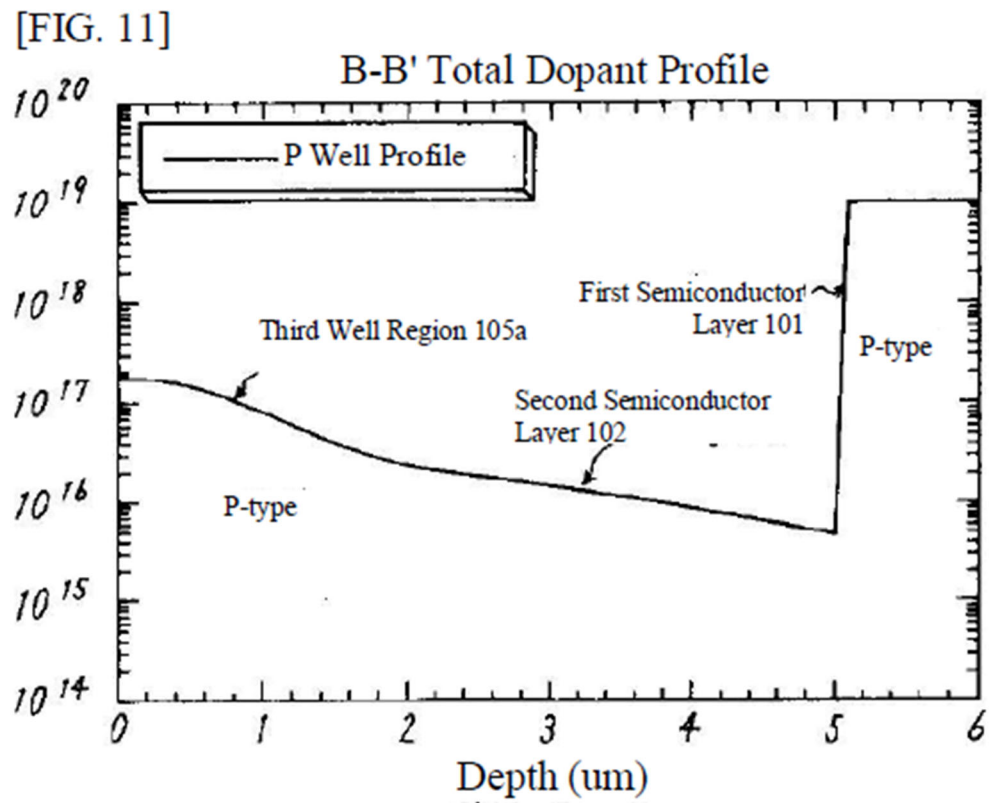


Ex. 1042, FIG. 8.



Ex. 1042, FIG. 9.

45. Onoda discloses that the dopant profile appearing in the B-B' cross-section in FIG. 8 is shown in FIG. 11 (below). Id., ¶[0052].



Ex. 1042, FIG. 11.

VIII. CLAIM CONSTRUCTION

46. I understand that claim terms are typically given their ordinary and customary meaning, as would have been understood by a person of ordinary skill in the art at the time of the alleged invention. In considering the meaning of the claims, I also understand that one must consider the claim language, specification, prosecution history, and the knowledge of a person of ordinary skill in the art at the relevant time. I understand that Patent Owner is not proposing any claim terms for claim construction. I agree with Patent Owner that none of the terms require construction. I applied the above understanding in my analysis.

IX. THE CITED REFERENCES DO NOT DISCLOSE OR SUGGEST ALL THE FEATURES OF THE CHALLENGED CLAIM

47. In my opinion, the prior art references relied upon in the Petition and Dr. Banerjee's declaration (Ex. 1003) do not disclose or suggest all the features of the Challenged Claim, as I explain below.

A. Dr. Banerjee's Payne-based analysis is incorrect regarding the "aid the movement of carriers" limitations (Elements [44.5]/[44.6]).

48. Dr. Banerjee stated in his declaration that "Payne renders claim 44 obvious." Ex. 1003, ¶67. I disagree. For elements [44.5] and [44.6], Dr. Banerjee stated in his declaration that "Payne discloses or, at a minimum, renders obvious this element." Ex. 1003, ¶¶89, 107. I disagree. He did not identify any portion of Payne that actually discloses the "aid the movement of carriers..." feature of these claim elements. The "aid the movement of carriers" feature appears in the Challenged Claim as follows. Element [44.5]: "the drift layer further having a first static unidirectional electric drift field to *aid the movement of carriers* from the surface layer to an area of the substrate where there are no active regions" and (B) Element [44.6]: "the well region having a graded concentration of dopants and a second static unidirectional electric drift field to *aid the movement of carriers* from the surface layer to the area of the substrate where there are no active regions."

49. In Ground I, for the “aid the movement of carriers” feature of these claims, it appears that Dr. Banerjee made inferences based on Payne’s disclosures, and I disagree with his inferences. Specifically, he cited to Payne in his element [44.4] analysis for mapping to the claimed “graded concentration of dopants” (Ex. 1003, ¶¶83-88), and used that to infer that the “aid the movement of carriers ...” feature of element [44.5] is disclosed. Ex. 1003, ¶¶164-167. Specifically, Dr. Banerjee points to Figures 10-11 of Payne for the claimed “graded concentration of dopants” recited in element [44.4]. Ex. 1003, ¶¶84-88. But for the claimed “aid the movement of carriers” feature of elements [44.5]/[44.6], Dr. Banerjee relies entirely on Greenthread’s supposed admissions:

Payne’s downward-sloping graded-dopant concentration aids the movement of minority carriers from the surface layer to the substrate *to the same extent* to which Applicant relied on the prior art and admitted to the Patent Office that such carrier movement would occur under the same scenario.

Ex. 1003, ¶94 (emphasis added) (regarding element [44.5]); *see also id.*, ¶¶114, 117 (regarding element [44.6]. Dr. Banerjee did not analyze anything actually disclosed in Payne for the “aid the movement of carriers...” feature. Ex. 1003, ¶¶89-117.

50. Based on Dr. Banerjee’s declaration, it is apparent that for his analysis of the “aid the movement of carriers ...” limitation he only considered the downward sloping nature of Payne’s concentration gradient, and not any other aspect of the

gradient (e.g., the magnitude of the force it produces on carriers) or whether there are any external forces (e.g., opposing forces e.g., due to the intrinsic resistance of silicon) such that the net force might not be aiding carrier movement in the claimed manner. In my opinion, a POSITA would have known that if two forces are acting on an object in opposite directions, both forces cannot aid its movement. Either the opposing forces are equal—and there is no movement—or the two forces are not equal and the object moves in the direction of the force having larger magnitude, albeit diminished by the counter force. The smaller force does not “aid” the movement of the object, because it is pushing *against* the movement. The magnitude of the concentration gradient plays a substantial role, because a small gradient may not be sufficient to overcome the resistance of the material in which the gradient exists. Therefore, a POSITA would need to know other parameters of the relevant device (e.g., magnitude of concentration gradient, intrinsic resistance of silicon, presence of any other external forces) to know whether a drift field associated with a concentration gradient would aid the movement of carriers.

51. Dr. Banerjee’s declaration does not indicate that he calculated the slope of the concentration gradient that he said Payne discloses. The magnitude of the slope is essential to determine the magnitude of the force the dopant gradient places on the carrier and thus the net force. Since the mere direction of the gradient is *not* sufficient to determine the nature of the net force, the premise of Dr. Banerjee’s

analysis is incorrect. Therefore, I disagree with his conclusion about the “aid carrier movement...” feature being taught in Payne.

B. Dr. Banerjee’s Onoda-based analysis is incorrect regarding the “aid the movement of carriers” limitations (Elements [44.5]/[44.6]).

52. Dr. Banerjee stated in his declaration that “Onoda anticipates claim 44 (Ground II), or Onoda in combination with Wolf (hereinafter, “Onoda-Wolf”) renders claim 44 obvious (Ground III).” Ex. 1003, ¶118. And for elements [44.5] and [44.6], Dr. Banerjee stated that “Onoda discloses or, at a minimum, renders obvious this element” (*id.*, ¶155 regarding element [44.5]) and “Onoda discloses this element” (*id.*, ¶166 regarding element [44.6]). I disagree with each of those statements that he made. As an initial comment, it is not clear why Dr. Banerjee mentioned “at a minimum, renders obvious” for element [44.5] but not for [44.6] when he presented basically the same analysis regarding “aid the movement of carriers” for both of those claim elements. At any rate, I disagree that Onoda discloses (or renders obvious) this claim. The “aid the movement of carriers” feature appears in the Challenged Claim as follows. Element [44.5]: “the drift layer further having a first static unidirectional electric drift field to ***aid the movement of carriers*** from the surface layer to an area of the substrate where there are no active regions” and (B) Element [44.6]: “the well region having a graded concentration of dopants and a second static unidirectional electric drift field to ***aid the movement of carriers*** from the surface layer to the area of the substrate where there are no active regions.” As he did for the Payne-based ground, Dr. Banerjee did not identify any portion of

Onoda that actually discloses the “aid the movement of carriers...” feature of these claim elements. *Id.*, ¶¶155-177.

53. Similar to his Payne-based analysis, Dr. Banerjee’s analysis for the Onoda-based grounds relies entirely on Greenthread’s supposed admissions. *Id.*, ¶162 (“Onoda’s graded-dopant concentration is downward-sloping over the entire single drift layer (tan) ... and thus, according to Patent Owner (and also in light of Applicant’s representations to the Patent Office discussed above), has a static unidirectional electric drift field that aids the movement of minority carriers from the surface layer to the substrate (specifically to an area of the substrate where there are no active regions).”); *see also id.*, ¶160.

54. But as I explained above, the existence of a downward-sloping graded-dopant concentration alone is not sufficient to establish the “aid the movement of carriers” claim limitation. *See* above at Section IX.A. As I explained above, Dr. Banerjee’s premise is flawed because did not take into account anything besides the existence of a downward-sloping concentration gradient in concluding that Onoda teaches the “aid the movement of carriers” aspect of limitations [44.5] and [44.6]. *Id.* His analysis is based on an incorrect premise.

X. CONCLUSION

55. I declare that all statements made herein of my knowledge are true, and that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine, imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Respectfully submitted,

Date: August 16, 2024

By: _____


Alexander D. Glew