

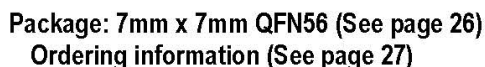


Description

- The IDTP9020 is a highly-integrated single-chip WPC-compliant wireless power receiver IC. The device receives an AC power signal from a compatible wireless transmitter and converts it into a regulated 5V output voltage which can be used to power devices or supply the charger input in mobile applications. The IDTP9020 integrates a high-efficiency synchronous full-bridge rectifier, high-efficiency synchronous buck converter, and control circuits used to modulate the load to transmit WPC-compliant message packets to the transmitter station to optimize power delivery. Power delivery is limited to 5W in accordance with the Qi specification.

Applications

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- The diagram illustrates the typical application circuit for the I2T95020. It is divided into two main sections: the internal circuitry of the I2T95020 (shaded green) and the external components (white background).
- Internal Circuitry (I2T95020):**
- EN:** Connected to a 10K pull-up resistor.
 - 330V_P:** Connected to a 330nF capacitor.
 - 22V_P:** Connected to a 22nF capacitor.
 - 100V_P:** Connected to a 100nF capacitor.
 - 11.4uH:** Connected to a 11.4uH inductor.
 - 2nF:** Connected to a 2nF capacitor.
 - 330V_M:** Connected to a 330nF capacitor.
 - 28K_M:** Connected to a 28K resistor.
 - 10uF:** Connected to a 10uF capacitor.
 - 1uF:** Connected to a 1uF capacitor.
 - 47nF:** Connected to a 47nF capacitor.
 - 10uF:** Connected to a 10uF capacitor.
 - 100K:** Connected to a 100K resistor.
 - 2.7K:** Connected to a 2.7K resistor.
 - 100nF:** Connected to a 100nF capacitor.
 - 5K:** Connected to a 5K resistor.
- External Components:**
- EN:** Connected to a 10K pull-up resistor.
 - 330V_P:** Connected to a 330nF capacitor.
 - 22V_P:** Connected to a 22nF capacitor.
 - 100V_P:** Connected to a 100nF capacitor.
 - 11.4uH:** Connected to a 11.4uH inductor.
 - 2nF:** Connected to a 2nF capacitor.
 - 330V_M:** Connected to a 330nF capacitor.
 - 28K_M:** Connected to a 28K resistor.
 - 10uF:** Connected to a 10uF capacitor.
 - 1uF:** Connected to a 1uF capacitor.
 - 47nF:** Connected to a 47nF capacitor.
 - 10uF:** Connected to a 10uF capacitor.
 - 100K:** Connected to a 100K resistor.
 - 2.7K:** Connected to a 2.7K resistor.
 - 100nF:** Connected to a 100nF capacitor.
 - 5K:** Connected to a 5K resistor.



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ABSOLUTE MAXIMUM RATINGS

These absolute maximum ratings are stress ratings only. Stresses greater than those listed below (Table 1 and Table 2) may cause permanent damage to the device. Functional operation of the IDTP9020 at absolute maximum ratings is not implied. Application of the absolute maximum rating conditions affects device reliability.

Table 1. Absolute Maximum Ratings Summary. All voltages are referred to ground, unless otherwise noted.

PINS	MAXIMUM RATING	UNITS
INP, INM	-1 to 24	V
REG_IN, EN, BUCK5VR_IN, REC_OUT, LX, Z _{REFP} , Z _{REFM} , A _{COMP} , A _{COMM}	-0.3 to 24	V
BST	-0.3 to BUCK5VR_IN+5	V
LDO2P5V, XTAL/CLK_IN, XTAL/CLK_OUT	-0.3 to 2.75	V
AGND, DGND, PGND, REF_GND	-0.3 to +0.3	V
All Other Pins	-0.3 to 6.0	V
Maximum Current from REC_OUT	1.5	A
Maximum Current from INP, INM	1	A _{RMS}
Maximum Current from LX	2	A

Table 2. Package Thermal Information

SYMBOL	DESCRIPTION	MAXIMUM RATING NTG56-TQFN	UNITS
θ_{JA}	Thermal Resistance Junction to Ambient ²	28.5	°C/W
θ_{JC}	Thermal Resistance Junction to Case	11.2	°C/W
θ_{JB}^2	Thermal Resistance Junction to Board	0.56	°C/W
T _J	Junction Temperature	0 to +150	°C
T _A	Ambient Operating Temperature	0 to +85	°C
T _{STG}	Storage Temperature	-55 to +150	°C
T _{LEAD}	Lead Temperature (soldering, 10s)	+300	°C

Note 1: The maximum power dissipation is $P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$ where $T_{J(MAX)}$ is 125°C. Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the device will enter thermal shutdown.

Note 2: This thermal rating was calculated on a JEDEC 51 standard 4-layer board with dimensions 3" x 4.5" in still air conditions. Actual thermal resistance is affected by PCB size, solder joint quality, layer count, copper thickness, air flow, altitude, and other unlisted variables. For the NTG56 package, connecting the 5.7mm X 5.7mm EP to internal/external ground planes with a 5x5 matrix of PCB plated-through-hole (PTH) vias, from top to bottom sides of the PCB, is recommended for improving the overall thermal performance.

SPECIFICATION TABLE
Table 3. Device Characteristics

$V_{REC_OUT} = 12V$; $EN=RESET=0V$; Synchronous Rectifier, LDO2P5, LDO5V, and DC/DC Converter blocks must be operated together. $T_A = 0$ to $+85^{\circ}C$, unless otherwise noted. Typical values are at $25^{\circ}C$, unless otherwise noted.

Symbol	Description	Conditions	Min	Typ	Max	Units
Full-Bridge Synchronous Rectifier						
$I_{RECT_STANDBY}$	Standby Current	$V_{REC_OUT}=V_{BUCK5VR_IN}=V_{REG_IN}=7.5V$, no load on REC_OUT, BUCK5VR, LDO5V, and LDO2P5V		8		mA
I_{RECT_DIS}	Disabled Current	$V_{REC_OUT}=V_{BUCK5VR_IN}=V_{REG_IN}=19V$, no load on REC_OUT, BUCK5VR, LDO5V, and LDO2P5V, $V_{EN}=5V$		250		μA
$R_{DSON_SFBR_HI}$	SFBR High-side switch on-resistance			150		m Ω
$R_{DSON_SFBR_LO}$	SFBR Low-side switch on-resistance			120		m Ω
Modulation						
$R_{DS-ON_CMOD_AC}$	MOSFET on resistance driving C_{MOD}		1	2	3	Ω
AC Clamp						
$R_{DS-ON_AC_CLAMP}$	MOSFET on resistance driving C_{ZREF}			450		m Ω
OVPIUVLO						
V_{RECT_OVP}	Over-voltage clamp protection for rectified voltage	$I_{RECT}=0$ to 1.5A	19		23.6	V
$V_{RECT_OVP_HYST}$	Over-voltage clamp protection hysteresis	$I_{RECT}=0$ to 1.5A		2		V
V_{RECT_UVLO}	Rising		3.1		4.3	V
	Falling		2.9		4.1	V
$V_{RECT_UVLO_HYST}$	Under-voltage lock-out hysteresis			0.2		V
DC/DC Converter						
V_{OUT}	Output voltage	$6V \leq V_{BUCK5VR_IN} \leq 19V$, $50mA \leq I_{OUT} \leq 1A$	4.75	5	5.25	V
I_{OUT_MAX}	Maximum output current capability		1			A
F_{sw}	Switching frequency			3		MHz
R_{DSON_HI}	High-side switch on-resistance			220		m Ω
R_{DSON_LO}	Low-side switch on-resistance			130		m Ω
Low-Drop-Out Regulators						
LDO2P5V²						
V_{OUT}	Output voltage	$I_{OUT} = 2mA$	2.375	2.5	2.625	V
I_{OUT}	Output current				5	mA
LDO5V²						
V_{OUT}	Output voltage	$6V \leq V_{IN} \leq 19V$, $I_{OUT} = 2mA$	4.75	5	5.25	V
I_{OUT}	Output current				2	mA
Thermal Shutdown						
T_{SD}	Thermal shutdown	Threshold Rising		140		$^{\circ}C$
		Threshold Falling		110		$^{\circ}C$

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SPECIFICATION TABLE (CONTINUED)

Table 3. Device Characteristics Continued

$V_{REG_OUT} = 12$; $EN=RESET=0V$; Synchronous Rectifier, LDO2P5, LDO5V, and DC/DC Converter must be operated together for correct operation. $T_A = 0$ to $+85^\circ C$, unless otherwise noted. Typical values are at $25^\circ C$, unless otherwise noted.

Symbol	Description	Conditions	Min	Typ	Max	Units
USB/ADP Switch						
$R_{DS(on)}^1$	USB switch on-resistance	$0\mu A \leq I_{OUT} \leq 500mA$		500		mΩ
EN						
V_{IH}				900		mV
V_{IL}				550		mV
I_{EN}	EN input current	$V_{EN} = 5V$		7.5		μA
		$V_{EN} = 20V$		56		μA
General Purpose Inputs / Outputs (GPIO)						
V_{IH}	Input Threshold High		3.5			V
V_{IL}	Input Threshold Low				1.5	V
I_{LKG}	Input Leakage		-1		+1	μA
V_{OH}	Output Logic High	$I_{OH} = -8mA$	4			V
V_{OL}	Output Logic Low	$I_{OL} = 8mA$			0.5	V
RESET						
V_{IH}	Input Threshold High		3.5			V
V_{IL}	Input Threshold Low				1.5	V
I_{LKG}	Input Leakage		-1		+1	μA
SCL, SDA (I²C Interface)						
f_{SCL}	Clock Frequency	EEPROM loading, Step 1, IDTP9020 as Master		100		kHz
f_{SCL}	Clock Frequency	EEPROM loading, Step 2, IDTP9020 as Master		300		kHz
f_{SCL}	Clock Frequency	IDTP9020 as Slave	0		400	kHz
t_{LOW}	Clock Low Period		1.3			μS
t_{HIGH}	Clock High Period		0.6			μS
$t_{HD,STA}$	Hold Time (Repeated) for START Condition		0.6			μS
$t_{SU,STA}$	Set-up Time for Repeated START Condition		0.6			μs
$t_{HD,DAT}$	Data Hold Time		10			ns
t_{BUF}	Bus Free Time Between STOP and START Condition		1.3			μs
C_B	Capacitive Load for Each Bus Line				100	pF
C_{BIN}	SCL, SDA Input Capacitance			5		pF
V_{IL}	Input Threshold Low				1.5	V
V_{IH}	Input Threshold High		3.5			V
I_{LKG}	Input Leakage Current		-1.0		1.0	μA
V_{OL}	Output Logic Low (SDA)	$I_{PD} = 2mA$			0.5	V

SPECIFICATION TABLE (CONTINUED)
Table 3. Device Characteristics Continued

$V_{REC_OUT} = 12$; $\overline{EN} = \text{RESET} = 0V$; Synchronous Rectifier, LDO2P5, LDO5V, and DC/DC Converter must be operated together for correct operation. $T_A = 0$ to $+85^\circ\text{C}$, unless otherwise noted. Typical values are at 25°C , unless otherwise noted.

Symbol	Description	Conditions	Min	Typ	Max	Units
Analog to Digital Converter						
N	Resolution			12		Bit
f_{SAMPLE}	Sampling Rate			62.5		kSPS
Channel	# of Channels at ADC MUX input			8		
ADC_{CLK}	ADC Clock Frequency			1		MHz
V_{INFS}	Full scale Input voltage			2.4		V
Microcontroller						
F_{CLOCK}	Clock frequency			40		MHz
V_{MCU}	MCU Supply Voltage from internal 2.5V LDO			2.5		V

Note 1: The load on the USB/Adaptor switch must not exceed 500mA.

Note 2: LDO2P5V and LDO5V are intended only as internal device supplies and must not be loaded externally except for the EEPROM, LEDs, and resistor loads (up to an absolute maximum of 25mA), as recommended in Figure 7 WPC "Qi" Compliance Schematic and Table 5 WPC "Qi" Compliance Bill of Materials.

PIN CONFIGURATION & DESCRIPTION

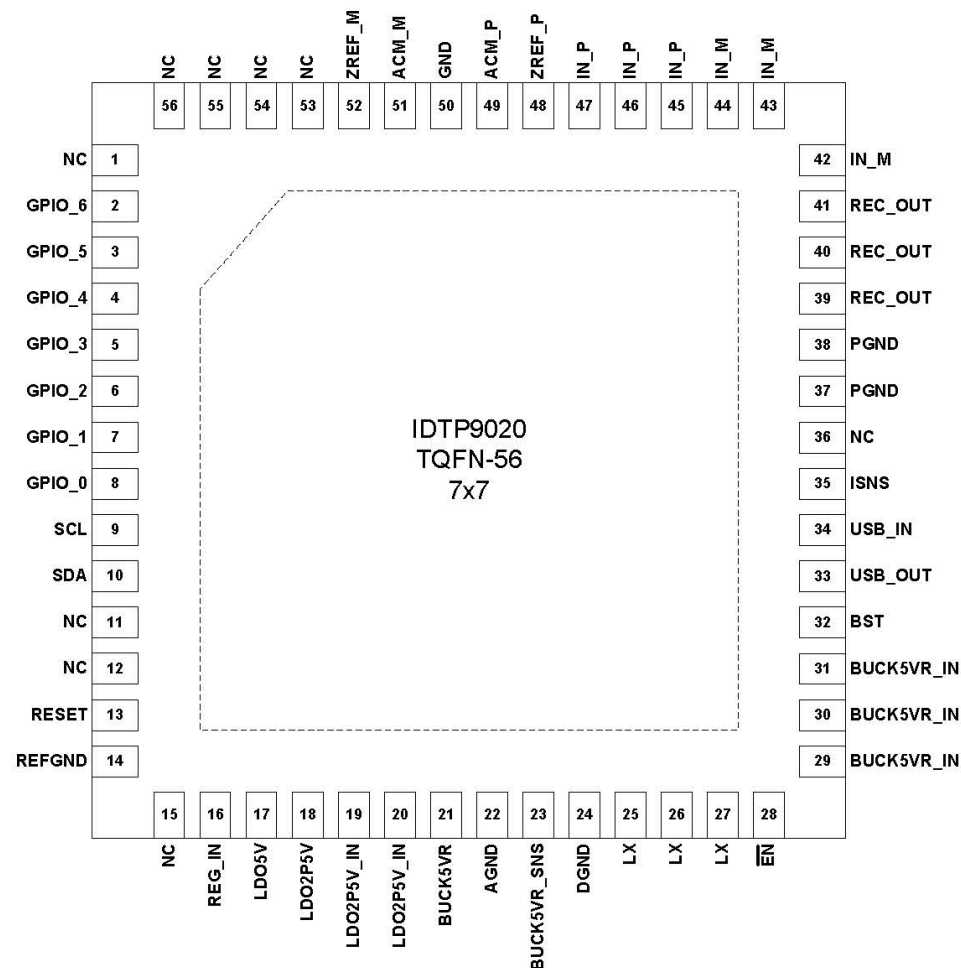


Figure 1. IDTP9020 QFN (NDG56 7x7x1mm 56-ld) Pin Configuration

PIN DESCRIPTION

Table 4 – QFN NDG56 Pin Functions by Pin Number (See Figure 1)

Pin # (TQFN)	Name	Type	Description
1	NC	-	Must be left unconnected.
2	GPIO_6	I/O	General input/output 6
3	GPIO_5	I/O	General input/output 5
4	GPIO_4	I/O	General input/output 4
5	GPIO_3	I/O	General input/output 3
6	GPIO_2	I/O	General input/output 2
7	GPIO_1	I/O	General input/output 1
8	GPIO_0	I/O	General input/output 0
9	SCL	I	I ² C clock
10	SDA	I/O	I ² C data
11	NC	NC	Must be connected to GND.
12	NC	NC	Must be left unconnected.
13	RESET	I	Active-high chip reset pin. Connect a 100kΩ resistor to GND.
14	REFGND	-	Signal ground connection. Must be connected to AGND.
15	NC	-	Must be connected to GND.
16	REG_IN	I	Regulator power supply input. Connect a 1μF capacitor between this pin and GND.
17	LDO5V	O	5V LDO output. A 1μF ceramic capacitor must be connected between this pin and GND.
18	LDO2P5V	O	2.5V LDO output. A 1μF ceramic capacitor must be connected between this pin and GND.
19	LDO2P5V_IN	I	2.5V LDO regulator power supply input. A 1μF ceramic capacitor must be connected between this pin and GND.
20	LDO2P5V_IN	I	2.5V LDO regulator power supply input. Connect to pin 19.
21	BUCK5VR	I	Power and digital supply input.
22	AGND	-	Analog ground connection. Must be connected to REFGND and GND.
23	BUCK5VR_SNS	I	Buck regulator feedback. Connect to the high side of the buck converter output capacitor.
24	DGND	-	Digital ground connection. Must be connected to GND.
25	LX	O	Switch node of buck converter. Connects to one of the inductor's terminals.
26	LX	O	Switch node of buck converter. Connects to one of the inductor's terminals.
27	LX	O	Switch node of buck converter. Connects to one of the inductor's terminals.
28	$\overline{\text{EN}}$	I	Active-low enable pin. The chip is suspended and placed in low-current (sleep) mode when pulled high. Tie to GND for stand-alone operation.

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Pin # (TQFN)	Name	Type	Description
29	BUCK5VR_IN	I	Buck converter power supply input. Connect a 10µF ceramic capacitor between pins 29, 30, and 31 and GND, and connect these pins to REC_OUT. A 0.1µF ceramic capacitor in parallel with the 10µF is also recommended.
30	BUCK5VR_IN	I	Connect to pins 29 and 31.
31	BUCK5VR_IN	I	Connect to pins 29 and 30.
32	BST	I	Bootstrap pin for buck converter top switch gate drive supply. Connect a 47nF/35V ceramic capacitor between this pin and LX.
33	USB_OUT	O	USB or 5V adaptor output.
34	USB_IN	I	USB or 5V adaptor input.
35	ISNS	O	ISNS output signal. Connect a 47nF ceramic capacitor between this pin and GND.
36	NC	—	Must be connected to GND.
37	PGND	-	Power ground.
38	PGND	-	Power ground.
39	REC_OUT	O	Rectified output. Connect four 10µF ceramic capacitors between these pins and GND.
40	REC_OUT	O	Rectified output. Connect four 10µF ceramic capacitors between these pins and GND.
41	REC_OUT	O	Rectified output. Connect four 10µF ceramic capacitors between these pins and GND.
42	IN_M	I	Negative bridge input.
43	IN_M	I	Negative bridge input.
44	IN_M	I	Negative bridge input.
45	IN_P	I	Positive bridge input.
46	IN_P	I	Positive bridge input.
47	IN_P	I	Positive bridge input.
48	ZREF_P	I	AC clamp, positive end.
49	ACM_P	I	AC modulation input, positive end.
50	GND	-	Ground.
51	ACM_M	I	AC modulation input, negative end.
52	ZREF_M	I	AC clamp, negative end.
53	NC	NC	Internal connection, do not connect.
54	NC	NC	Internal connection, do not connect.
55	NC	NC	Internal connection, do not connect.
56	NC	NC	Internal connection, do not connect.

SIMPLIFIED BLOCK DIAGRAM

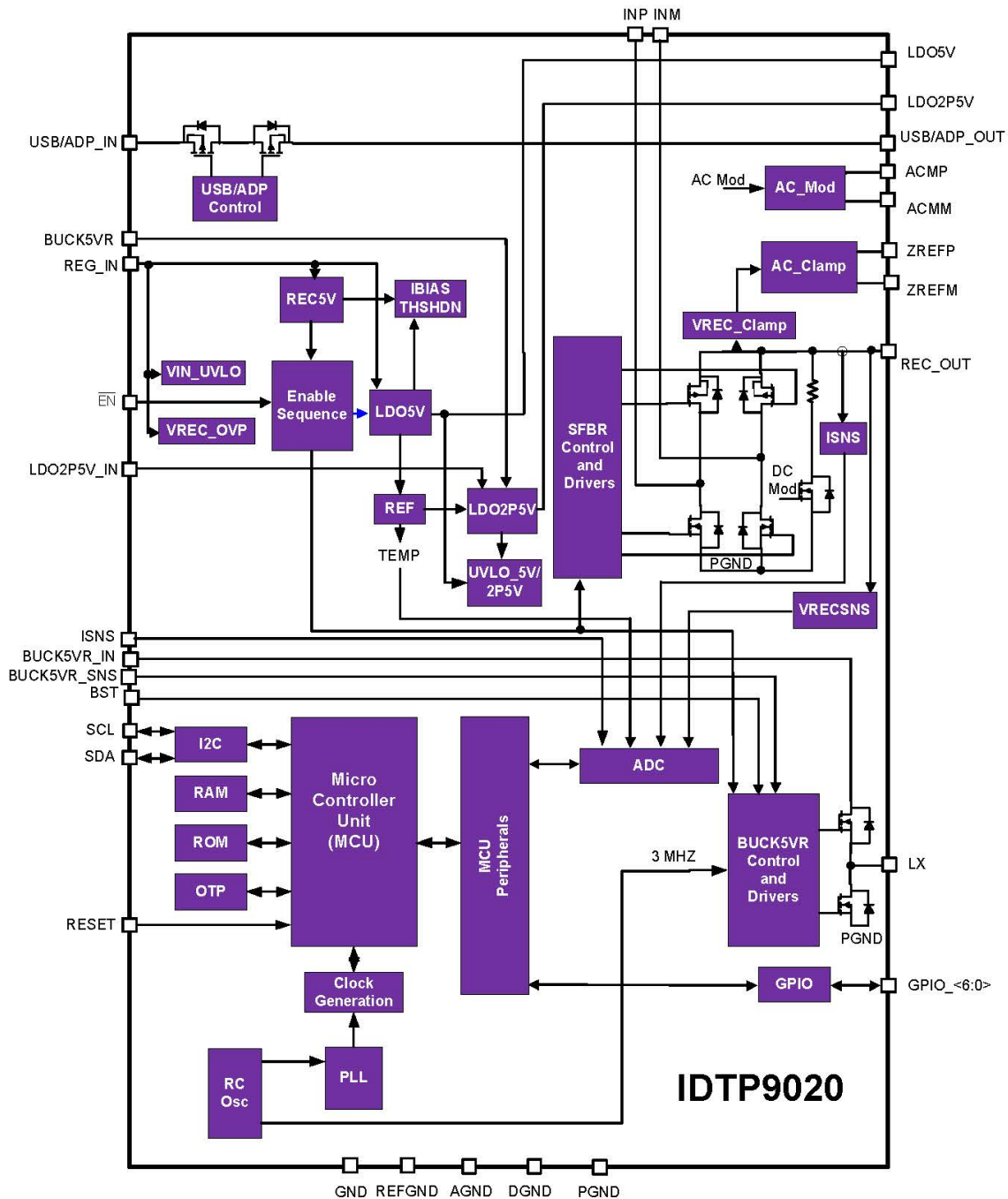


Figure 2. IDTP9020 Internal Functional Block Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

Typical Performance Characteristics: System Efficiency versus RX Output Power
= RESET = 0, TA = 25°C

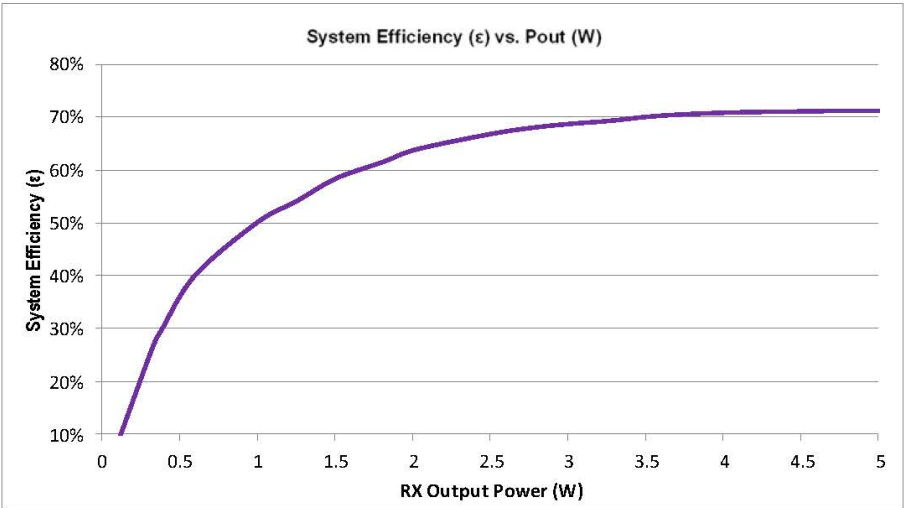


Figure 3. Efficiency vs. RX Output Power with IDTP9030 Transmitter

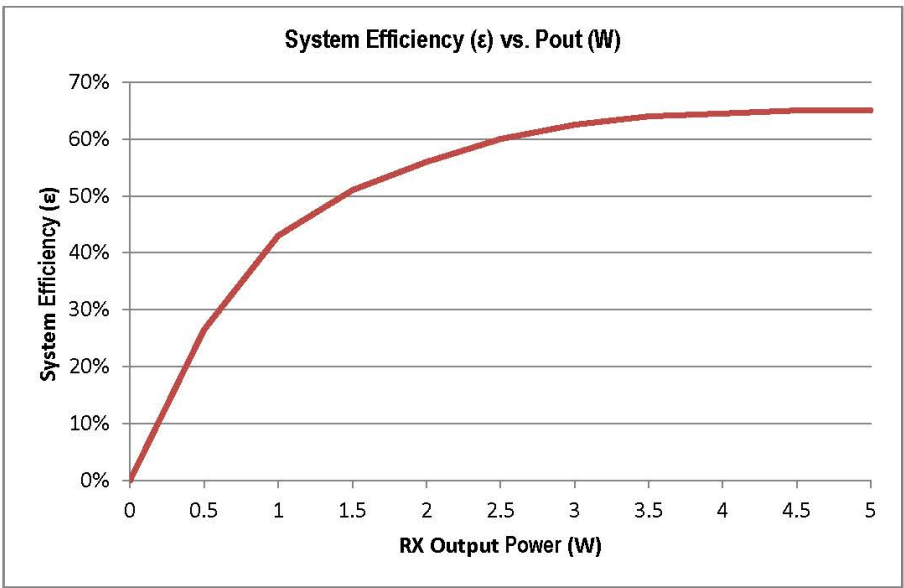


Figure 4. Efficiency vs. RX Output Power with IDTP9035 Transmitter

Description of the Wireless Power Charging System

A wireless power charging system has a base station that has one or more transmitters that make power available via DC-to-AC inverter(s) and transmit the power over a strongly-coupled inductor pair. The transmitter may be a *free-positioning* or *magnetically-guided* type. A *free-positioning* type of transmitter has an array of coils that gives limited spatial freedom to the end-user, whereas a *magnetically-guided* type of transmitter helps the end-user align the receiver to the transmitter with a magnetic attraction.

The amount of power transferred to the mobile device is controlled by the receiver. The receiver sends communication packets to the transmitter to increase power, decrease power, or maintain the power level. The bit rate for RX-to-TX communication link is 2-kbps. The communication is purely digital and communication 1's and 0's ride on top of the power link that exists between the two coils.

A large part of the efficiency of the wireless charging system arises from the fact that when it's not actually charging a mobile device, the transmitter is in a very-low-power sleep mode. The transmitter occasionally awakens and scans the environment to see if a receiver is present. If no receiver is detected, the transmitter goes back to sleep.

Theory of Operation

The IDTP9020 is a highly-integrated WPC¹ (Wireless Power Consortium)-compliant wireless power receiver IC solution for mobile devices. It can transfer more than 5W of power from a wireless transmitter to a load (e.g., a battery charger) when paired with one of IDT's family of wireless transmitters, or 5W in WPC "Qi" mode using near-field magnetic induction. It is the industry's first single-chip WPC-compliant wireless power receiver solution.

Note 1 - Refer to the WPC specification at <http://www.wirelesspowerconsortium.com/> for the most current information

OVERVIEW

The simplified block diagram of the IDTP9020 is shown in Figure 3. An external inductor and two capacitors transfer energy from the transmitter's coil through the IDTP9020's INM and INP pins to be full-wave-rectified and stored on a capacitor connected to REC_OUT. Until the voltage across the capacitor exceeds the threshold of the VIN_UVLO block, the rectification is performed by the body diodes of the Synchronous Full Bridge Rectifier FETs. After the internal biasing circuit is enabled, the SFBR Control and Drivers block operates the MOSFET switches in the rectifier for increased efficiency. An internal ADC monitors the voltage at REC_OUT and the load current, and the IDTP9020 sends instructions to the wireless power transmitter to increase or decrease the amount of power transferred or to terminate power transmission. The voltages at the outputs of the voltage regulators and the internal temperature are also monitored to ensure proper operation.

STARTUP

When the voltage at REC_OUT reaches about four volts, REC5V provides an internal regulated supply voltage to the ENABLE and IBIAS/THSHDN blocks. If the voltage on EN is at a logic low when the Under-Voltage Lock-Out is released, the ENABLE block turns on the 5V LDO, which then turns on the bandgap voltage reference in the REF block and provides a more highly-regulated supply voltage for the IBIAS/THSHDN block. When the reference voltage is ready, the 2.5V LDO is enabled and power is supplied to the Micro-Controller Unit, the Analog-to-Digital Converter, the Synchronous Full-Bridge Rectifier, and related circuitry.

RECTIFIER and VREC_CLAMP

When the 5V and 2.5V UVLOs have been released, the full-bridge rectifier switches to synchronous mode to more efficiently transfer energy from the transmitter to the load at REC_OUT. VREC_OVP monitors the REC_OUT voltage. If the voltage at REC_OUT exceeds about 20V, the VREC_CLAMP turns on two internal FETs to connect INP and INM to ground through external capacitors, shunting AC current from the secondary coil away from the IDTP9020. The clamp is released when the voltage at REC_OUT falls to about 18V.

DC/DC CONVERTER

The 5V buck switching regulator is turned on shortly after the 2.5V LDO is activated, operating at 3MHz with internal power FETs. When the buck switcher reaches regulation, in addition to the external load, it also provides power to the IDTP9020's internal circuitry.

POWER CONTROL

The voltage at REC_OUT and the current through the rectifier are sampled periodically by the VRECSNS and ISNS blocks, and digitized by the ADC. The digital equivalents of the voltage and current are supplied to the MCU, which decides whether the loading conditions on REC_OUT indicate that a change in the operating point is required. If the load is heavy enough to bring the voltage at REC_OUT below its target, the transmitter is instructed to move its frequency lower, closer to resonance. If the voltage at REC_OUT is higher than its target, the transmitter is instructed to increase its frequency.

MODULATION/COMMUNICATION

Receiver-to-transmitter communication is accomplished by modulating the load seen by the receiver's coil. To the transmitter, this appears as an impedance change which results in measurable variations of the transmitter's output waveform. Modulation can be done with either AC Modulation, using internal switches to connect external capacitors from INM and INP to ground, or DC Modulation, which connects an internal resistor from REC_OUT to ground. The communication protocol is covered in the COMMUNICATION section of this datasheet.

Communication between the MCU and an external EEPROM is carried out through the I²C interface. The firmware that controls the operation of the IDTP9020 is held in RAM, and parameter value trimming and some operation-mode adjustments are performed through One-Time-Programming (OTP) at the factory.

OSCILLATOR

An internal RC oscillator generates the frequencies at which the MCU and buck switching regulator operate.

USB SWITCH

Whether or not the mobile device in which the IDTP9020 resides is involved in wireless power transfer, connecting a USB adaptor to the USB_IN input deactivates the IDTP9020. An internal switch connects the USB power to the USB_OUT pin. The switch is sized for a maximum of 500mA. Exceeding this current will cause the voltage at the USB_OUT pin to drop out of regulation. Unplugging the adaptor will cause wireless power transfer to resume if the IDTP9020's coil is aligned with a transmitter's coil. Note that if the mobile device remains aligned with the transmitter's coil while the USB cable is plugged in, charge will continue to pass through the body diodes of the rectifier and accumulate on the capacitor at REC_OUT during periodic pings. If the IDTP9020's REC_OUT pin is unloaded, the voltage on the external capacitor could rise to a high voltage. The AC clamp will protect the IDTP9020 and the external capacitor, but any device connected to REC_OUT that can't tolerate 20V will probably be damaged.

SIMPLIFIED APPLICATION DIAGRAM

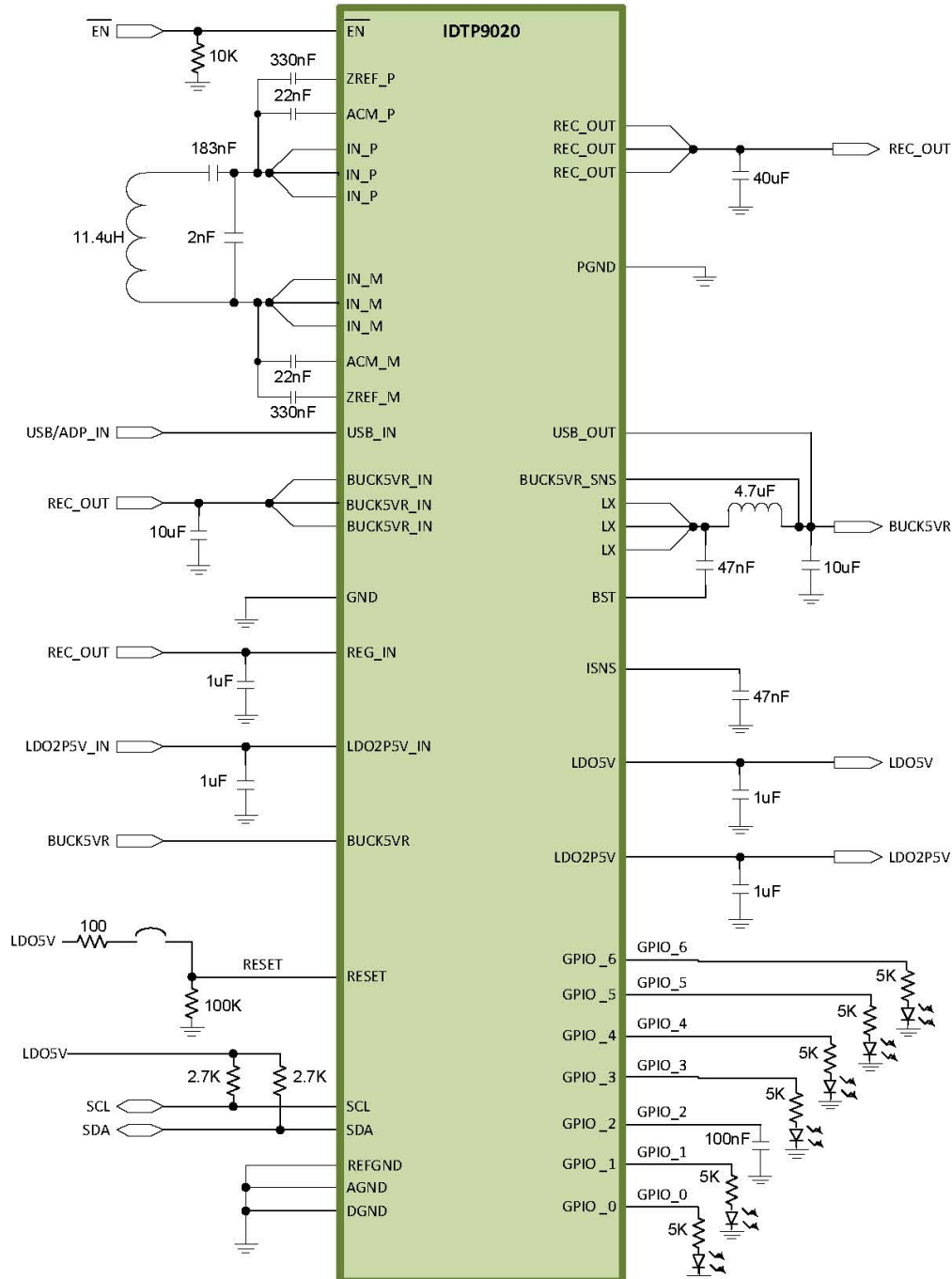
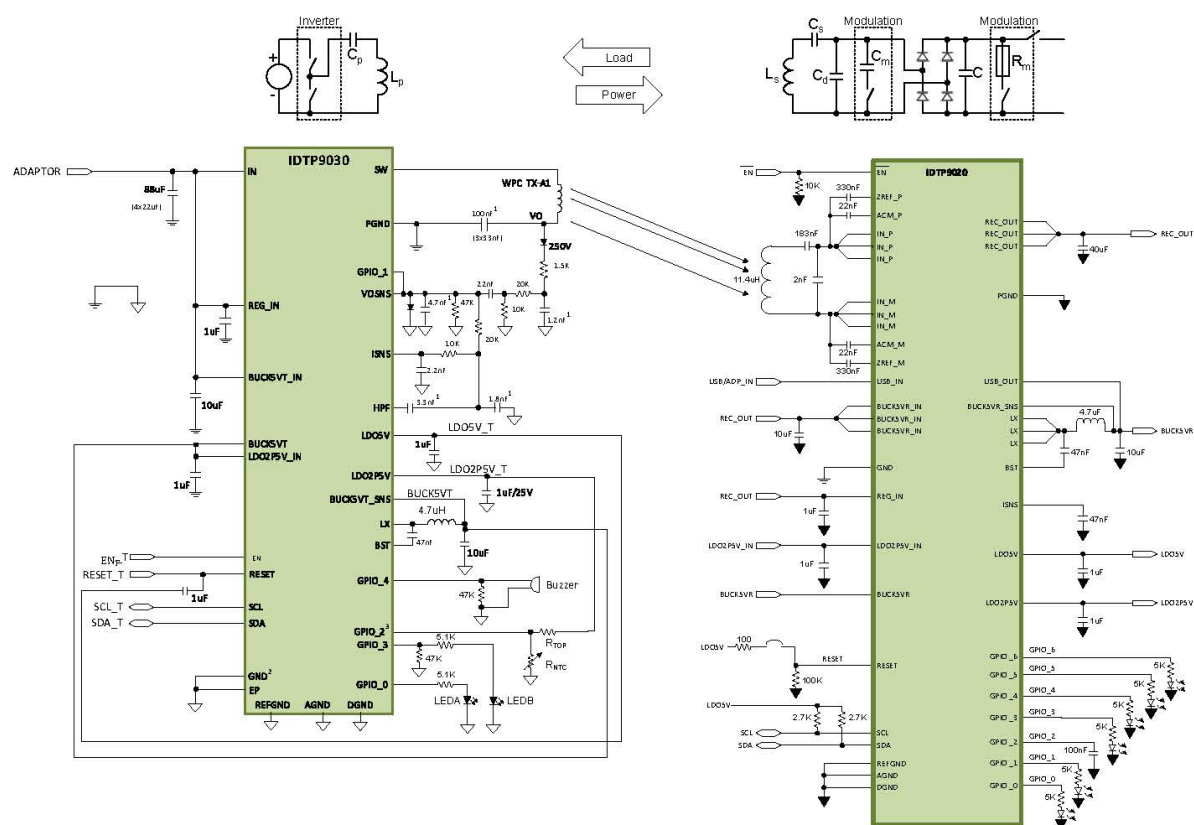


Figure 5. IDTP9020 Simplified Applications Diagram.



DETAILED SYSTEM DIAGRAM

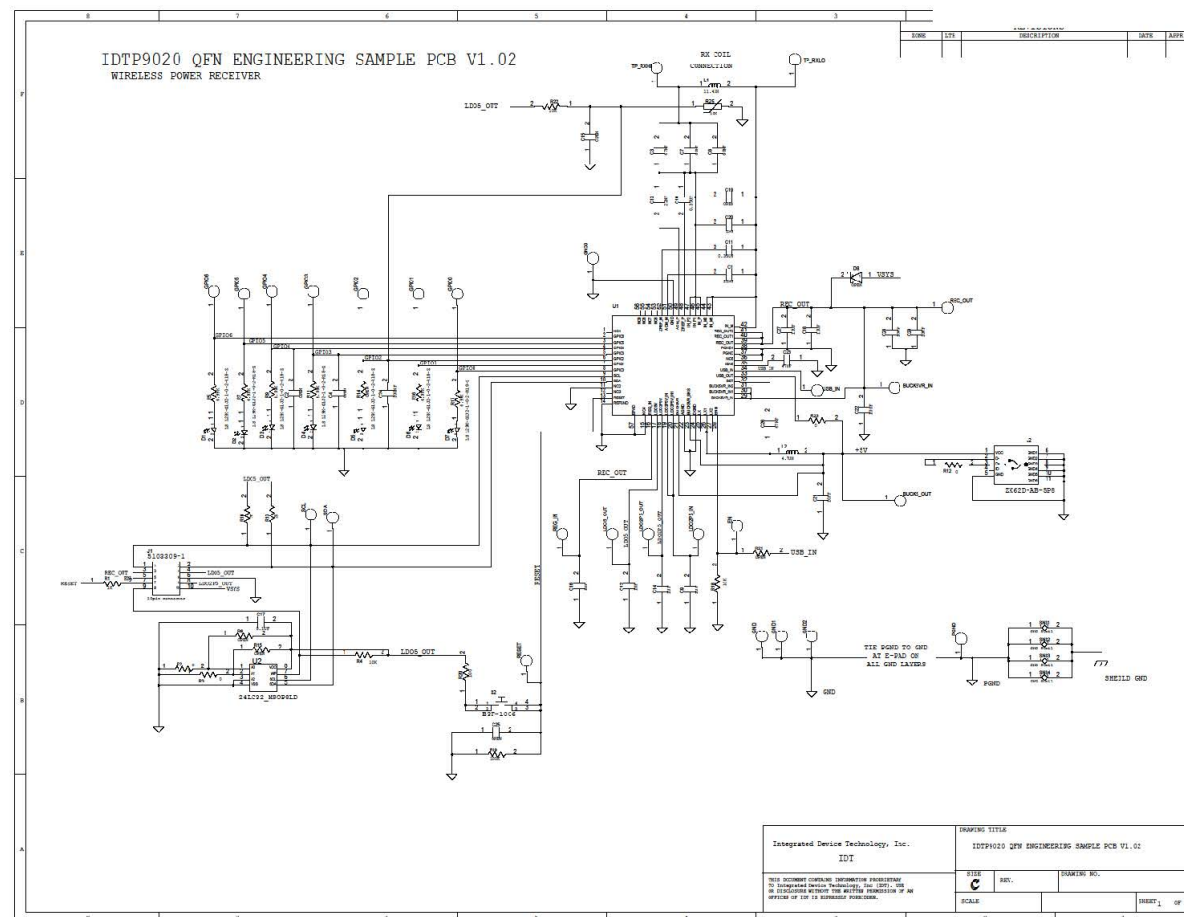


Figure 7. IDTP9020 Evaluation Kit Schematic diagram.

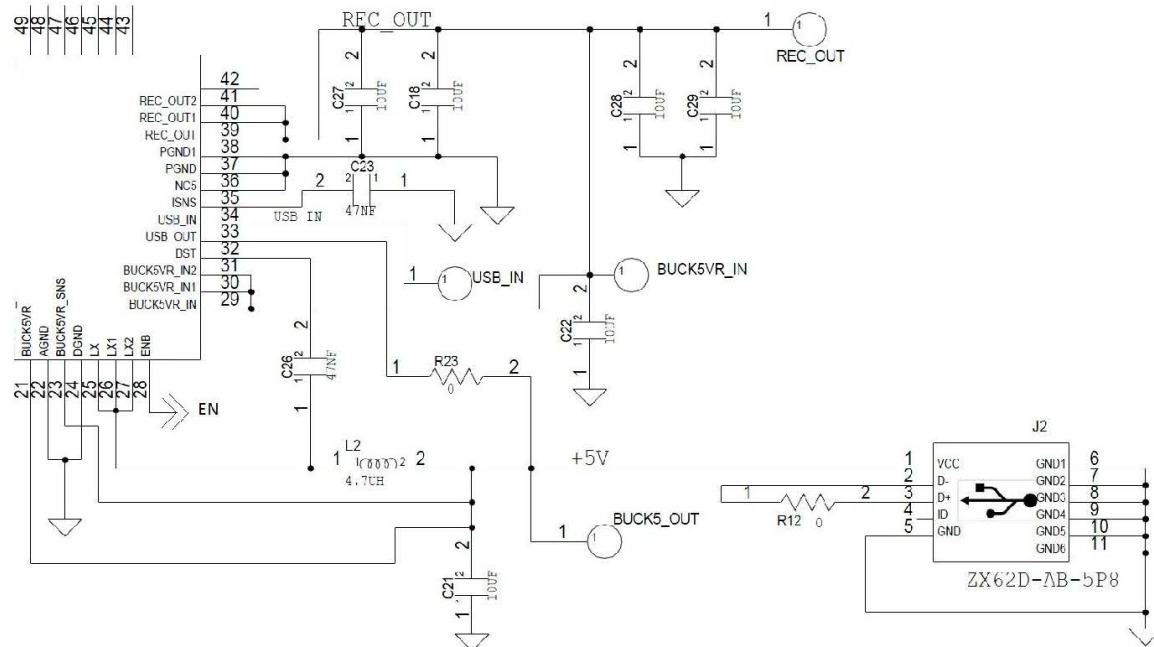


Figure 7a. Detail of REC_OUT and BUCK5VT connections.

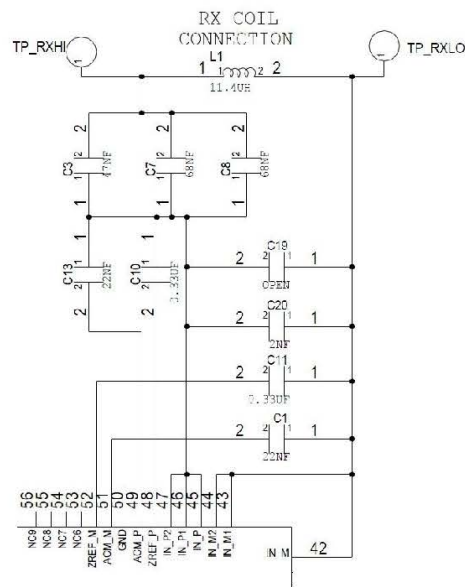


Figure 7b. Detail of Rx Power connections. C3, C7, C8, C19, and C20 values vary with RX-A coil value. See Table 5 BOM and Note 2 for details.

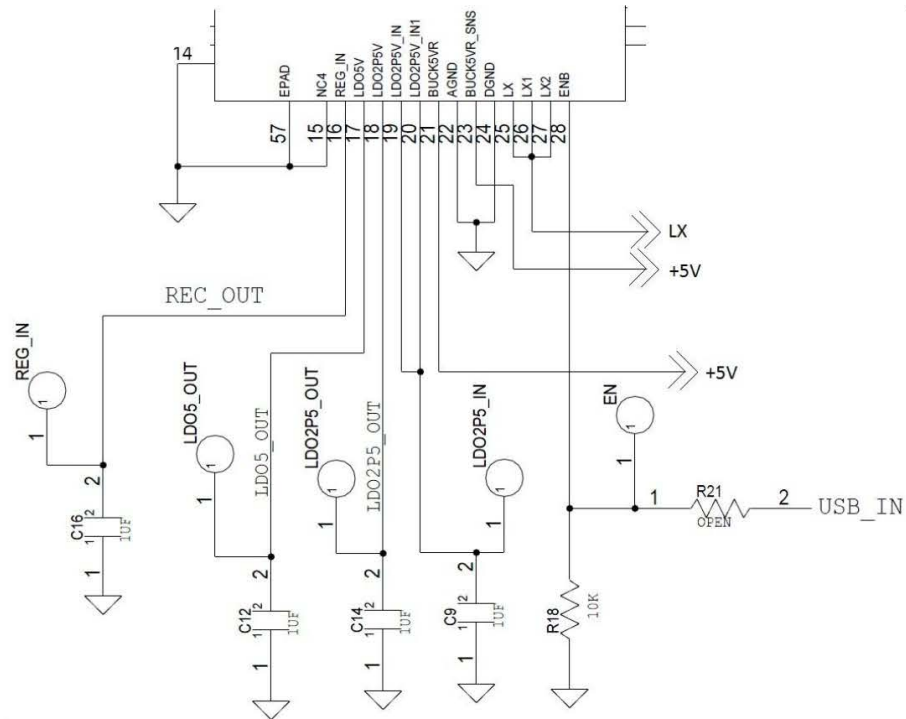


Figure 7c. Detail of LDO5V and LDO2P5V connections.

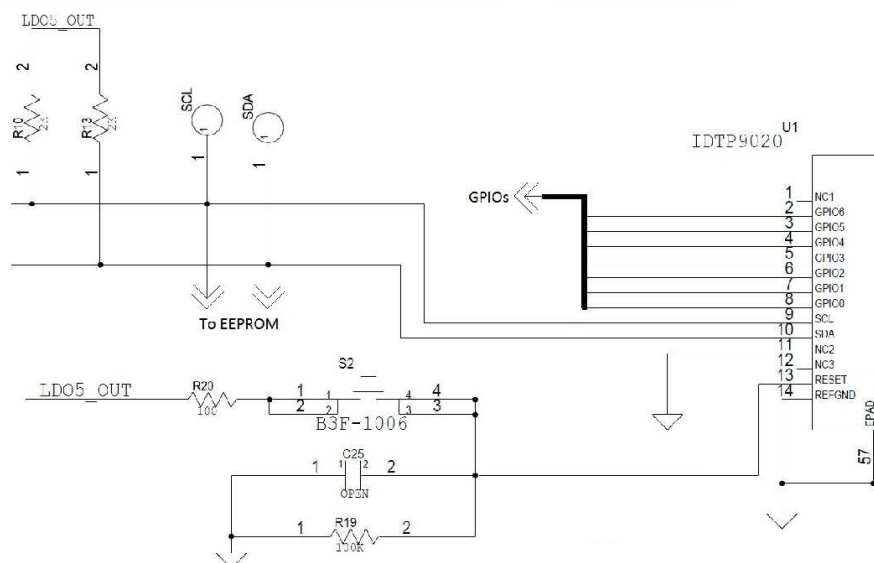


Figure 7d. Detail of RESET and I²C connections.

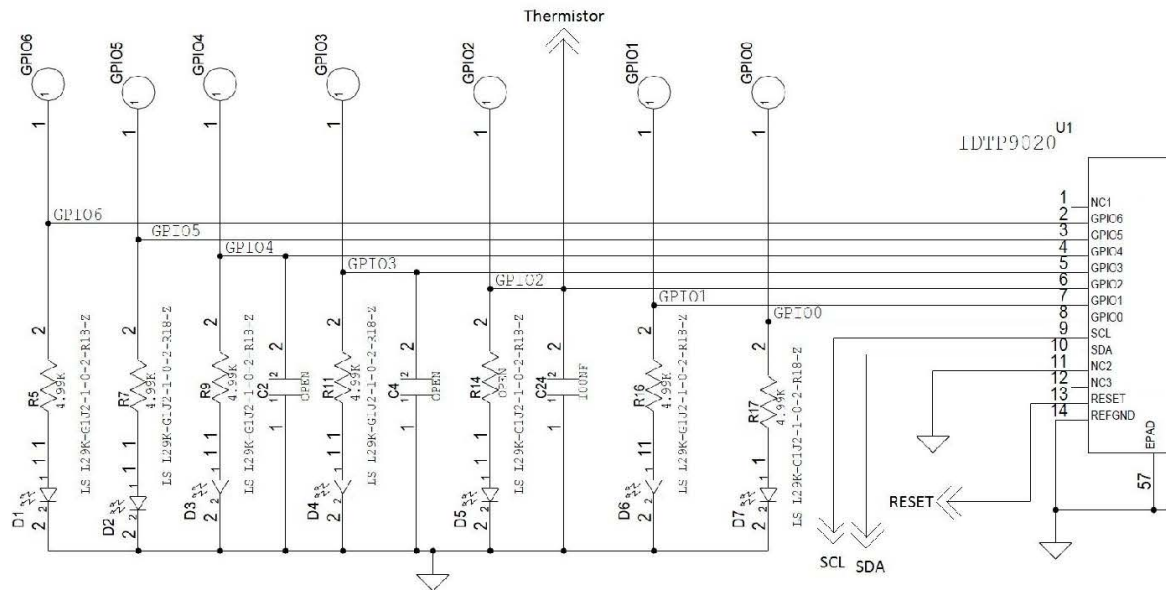


Figure 7e. Detail of GPIO connections.

COMPONENT SELECTION

Table 5. IDTP9020 Minimum Required Bill of Materials, Based on RX-A 1mm type receiver coil:

S.No.	Qty	Part Name	Manufacturer	PART_NUMBER	VALUE	Ref Des	JEDEC_TYPE
1	2	CAP-22NF,0805,5%,NPO,50V ¹	TDK	C2012C0G1H223J	22NF	C1,C13	805
2	2	CAP-0.33UF,1206,10%,X7R,50V ¹	TDK	C3216X7R1H334K	0.33UF	C10,C11	1206
3	3	CAP-1UF,0603,10%,X7R,25V	Murata	GRM188R71E105KA12D	1UF	C9,C12,C14	603
4	1	CAP-47NF,0402,10%,X7R,35V	TDK	C1005X7R1V473K	47NF	C26	402
5	1	CAP-0.1UF,0402,10%,X7R,16V	Taiyo Yuden	EMK105B7104KV-F	0.1UF	C17	402
6	5	CAP-10UF,1210,10%,X7S,50V ¹	Taiyo Yuden	UMK325C7106MMT	10UF	C18,C22,C27-C29	1210
7	1	CAP-2NF,1206,5%,NPO,50V ^{1,2}	AVX	12065A202JAT2A	2NF	C20	1206
		CAP-2.2NF,1206,5%,NPO,50V ^{1,2}	Kemet	C1206C222K5GACTU	2.2NF		
8	1	CAP-10UF,1206,10%,X7R,25V	Taiyo Yuden	TMK316B7106KL-TD	10UF	C21	1206
9	1	CAP-47NF,0402,10%,X7R,25V	TDK	C1005X7R1E473K	47NF	C23	402
10	1	CAP-100NF,0402,10%,X7R,16V	Murata	GRM155R71C104KA88D	100NF	C24	402
11	1	CAP-470PF,1206,5%,NPO,50V ^{1,2}	TDK	C3216C0G1H471J	470PF	C19	1206
		CAP-180PF,1206,5%,NPO,50V ^{1,2}	AVX	12065A181JAT2A	180PF		
		CAP-1UF,0805,10%,X7R,50V ¹	Murata	GRM21BR71H105KA12L	1UF	C16	805
13	3	CAP-82NF,1206,5%,NPO,50V ^{1,2}	Murata	GRM31C5C1H823JA01L	82NF	C3,C7,C8	1206
		CAP-68NF,1206,5%,NPO,50V ^{1,2}	TDK	C3216C0G1H683J	68NF		
		CAP-100NF,1206,5%,NPO,50V ^{1,2}	TDK	C3216C0G1H104J	100NF		
		CAP-47NF,1206,5%,NPO,50V ^{1,2}	TDK	C3216C0G1H473J	47NF		
14	1	INDUCTOR ²	Vishay	IWAS4832FFEB9R7J50	9.7UH	L1	48X32X1MM
			TDK	WR-483250-15M2-xx	10.5UH		48X32X1MM
15	1	INDUCTOR-4.7UH,4X4X1.8MM,2.2(A),20%	Würth	744 373 240 47	4.7UH	L2	IND_25Q_TO_6P9SQ
16	2	RES-2.7K,0603,1%,1/10W,100	Vishay	CRCW06032K70FKEA	2.7K	R10,R13	603
17	1	RES-10K,0402,1%,1/10W,100	Yageo	RC0402FR-0710KL	10K	R18	0402_1
18	1	RES-100K,0402,1%,1/10W,100	Yageo	RC0402FR-07100KL	100K	R19	402
19	1	IDTP9020 QFN	IDT	P9020NDG	QFN56	U1	QFN-56 7x7x1mm
20	1	IC EEPROM 64KBIT 400KHZ 8TDFN	Microchip	24AA64T-1/MNY	8kX8	U2	DFN_8LD_2X3MM

Note 1 - Recommended capacitor temperature/dielectric and voltage ratings. 50V capacitors are recommended for C1, C3, C5, C7, C8, C13, C10, C11, C18, C19, C20, C22, C23, C26-C28. Furthermore, C0G/NPO-type capacitor values stay constant with voltage while X7R and X5R capacitor values derate over the working voltage range at 40% to over 80%. The decision to use lower voltage lower voltage rated capacitors or other type temperature/dielectric capacitors is left to the end user.

Note 2 – RX coil L1. When the TDK RX coil is used (WR-483250-15M2-xx), the resonant capacitors for C3, C7 and C8 is populated with two 68nF and one 82nF. C20 is populated with one 2nF and C19 is populated with one 470pF. For the Vishay coil (IWAS4832FFEB9R7J50), C3, C7 and C8 is populated with one 100nF and two 47nF capacitors. C20 is populated with one 2.2nF and C19 is populated with one 180pF.

FUNCTIONAL DESCRIPTION

The IDTP9020 is a highly-integrated single-chip receiver-side 'Qi' compliant solution. It can deliver up to 5W to the external load through a high-efficiency synchronous buck converter. Incoming AC power from the resonant tank is conditioned and rectified through a full-wave synchronous rectifier and regulated down to 5V for delivery to the system as shown below.

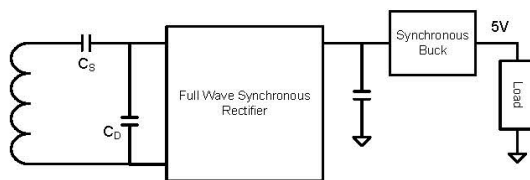


Figure 8: Wireless power delivery to the load

Integrated USB Switch

In addition to the Wireless Power Path, the IDTP9020 has an alternative USB power path integrated on-chip to offer the highest level of system integration in a wireless receiver design. In the absence of USB power, if wireless power is available, then the wireless path is enabled as shown below:

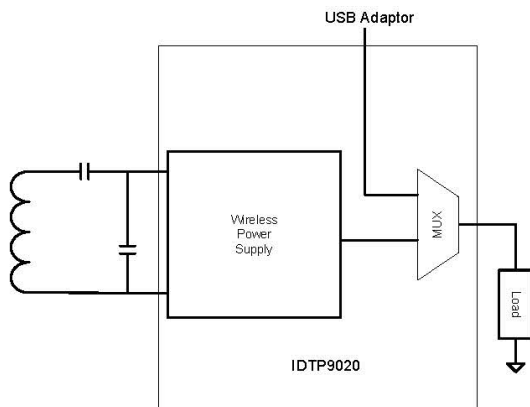


Figure 9: Integrated USB power path option

However, if USB power is available, then it powers the downstream load regardless of wireless power availability.

Modulation

The IDTP9020 is compatible with all WPC-recommended coils: RX-A,B,C,D. Each receiver coil type has a unique inductance value. As such, a unique resonant capacitor is used for a given type of receiver coil. Additionally, each receiver type has a unique modulation capacitor, C_{MOD} , as shown below:

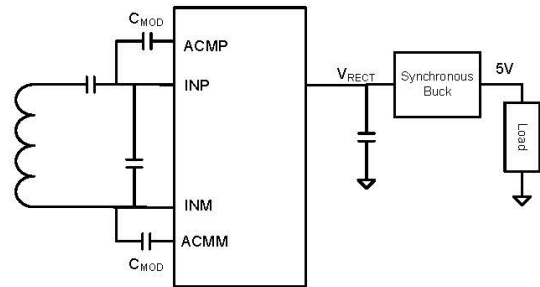


Figure 10: Modulation components

Consult the factory for assistance with configuring a system with a specific coil type.

Communication

The IDTP9020 communicates with the base via communication packets. Each communication packet has the following structure:

Preamble	Header	Message	Checksum
----------	--------	---------	----------

Figure 11: Communication packet structure

According to the WPC specification, the power receiver communicates with the power transmitter using backscatter modulation. The load seen by the inductor is modulated on the receiver side to send packets. The power transmitter detects this as a modulation of coil current/voltage to receive packets.

Bit Encoding Scheme

As required by the WPC, the IDTP9020 uses a differential bi-phase encoding scheme to modulate data bits onto the Power Signal. A clock frequency of 2kHz is used for this purpose. A logic ONE bit is encoded using two narrow

transitions, whereas a logic ZERO bit is encoded using two wider transitions as shown below:

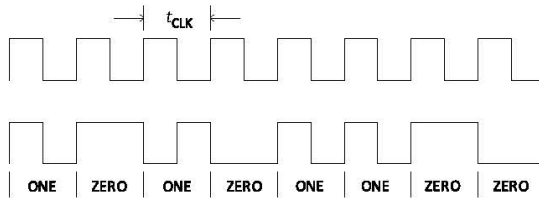


Figure 12: Bit encoding scheme

Byte Encoding Scheme

Each byte in the communication packet comprises 11bits in an asynchronous serial format, as shown below:

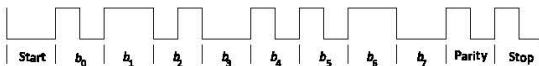


Figure 13: Byte encoding scheme

Each byte has a start bit, 8 data bits, a parity bit, and a single stop bit.

System Feedback Control

The IDTP9020 is fully compatible with WPC specification Rev. 1.1 and has all necessary circuitry to communicate with the base station via WPC-compliant communication packets.

The overall WPC-compliant system behavior between the transmitter and receiver follows the state machine below:

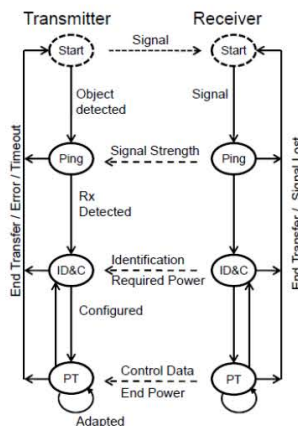


Figure 14: WPC System Feedback control

The IDTP9020 goes through four phases: Selection, Ping, Identification & Configuration, and Power Transfer.

SELECTION

In this phase, the IDTP9020 looks at the incoming power from the base and proceeds to the *PING* state. It monitors the rectified voltage, and when the voltage is above the $V_{RECT,UVLO}$ threshold, the IDTP9020 wakes up its digital electronics and prepares to communicate with the base station. If the IDTP9020 does not proceed to *PING*, then it does not transmit any communication packets.

PING

In this phase, the IDTP9020 transmits a Signal Strength Packet as the first communication packet to instruct the base to keep the power signal ON. After sending the Signal Strength Packet, the IDTP9020 proceeds to the *Identification and Configuration* phase. If, instead, the IDTP9020 sends End of Power Packets, then it remains in the *PING* phase.

In this phase, the IDTP9020 sends the following packets:

- Signal Strength Packet

IDENTIFICATION AND CONFIGURATION (ID & Config)

In this phase, the IDTP9020 may send the following packets:

- Identification Packet
- Configuration Packet
- Extended Identification Packet (Optional)
- Up to 7 optional configuration packets

After sending the Configuration Packet, the IDTP9020 proceeds to the *power transfer* phase.

POWER TRANSFER

In this phase, the IDTP9020 controls the power transfer from the Power Transmitter by means of the following Control Data Packets:

- Control Error Packets
- Rectified Power Packet
- Charge Status Packet
- End Power Transfer Packet
- Any Proprietary Packets

OVER-VOLTAGE/TEMPERATURE PROTECTION

If the voltage at REC_OUT exceeds about 20V, most of the AC current from the inductor is shunted to ground through external capacitors and internal FET switches, rather than conducted through the rectifier to the output capacitor. The AC clamp that performs this function turns off when the voltage at REC_OUT decreases to about 18V.

The internal temperature is monitored, and the IDTP9020 is temporarily deactivated if the temperature exceeds 140°C and reactivated when the temperature falls below 110°C.

External Components

The IDTP9020 requires a minimum number of external components for proper operation (see the BOM in Table 5). A complete design schematic compliant to the WPC "Qi" standard is given in Figure 7. It includes LED signaling and an EEPROM for loading IDTP9020 firmware.

I²C Communication

The IDTP9020 includes an I²C block which can support either I²C Master or I²C Slave operation. After power-on-reset (POR), the IDTP9020 will initially become I²C Master for the purpose of uploading firmware from an external memory device, such as an EEPROM. The I²C Master mode on the IDTP9020 does not support multi-master mode, and it is important for system designers to avoid any bus master conflict until the IDTP9020 has finished any firmware uploading and has released control of the bus as I²C Master.

After any firmware uploading from external memory is complete, and when the IDTP9020 begins normal operation, the IDTP9020 is normally configured by the firmware to be exclusively in I²C Slave mode.

For maximum flexibility, the IDTP9020 uses a two-step approach to communicate with the EEPROM: step one attempts to access the first EEPROM address at 100kHz. If no ACK is received, communication is attempted at the other addresses at 300kHz.

EEPROM

The IDTP9020 could use an external EEPROM which contains either standard or custom TX firmware. The external EEPROM memory chip is pre-programmed with a standard start-up program that is automatically loaded when the voltage on REC_OUT is high enough to enable the IDTP9020's MCU. The IDTP9020 uses I²C slave address 0x50 to access the EEPROM. The IDTP9020 slave address is 0x39. The EEPROM can be reprogrammed to suit the needs of a specific application using the IDTP9020 software tool (see the IDTP9020-Qi Demo Board User Manual for complete details). The IC will look initially for an external EEPROM and use the firmware built into the IC ROM only if no external memory device is found. A serial 8Kbyte (8Kx8 64Kbits) external EEPROM is sufficient.

If the standard default/built-in firmware is not suitable for the application, custom ROM options are possible. Please contact IDT sales for more information. IDT will provide the appropriate image in the format best suited to the application.

APPLICATIONS INFORMATION

External Components

The IDTP9020 requires a minimum number of external components for proper operation, as indicated in Figures 5 and 7 and Table 5.

ADC Considerations

The GPIO pins are connected internally to a successive-approximation 12-bit ADC with a multiplexed input.

The GPIO pins that are connected to the ADC have limited input range, so attention should be paid to the maximum input voltages (2.4V). Decoupling capacitors can be added to minimize noise.

Buck Converter

- The input capacitors (C_{IN}) should be connected as close to the BUCK5VR_IN and PGND pins as practical.
- The output capacitor (C_{OUT}) should be connected as close to the PGND pin as possible to minimize switching ripple caused by ground potential differences.
- The high-side gate bootstrap pin requires a small capacitor to pull the DC-DC regulator's HS gate voltage higher than the input voltage level. Connect a 47nF bootstrap capacitor rated above 35V between the BST pin and the LX pin.
- The output-sense connection to the feedback pins should be separated from any power trace. Connect the output-sense trace as close as possible to the load point to avoid additional load regulation errors.
- The power traces, including GND traces, the LX or BUCK5VR traces, should be kept short, direct and wide to reduce parasitic that could affect performance. The inductor connection to the LX and BUCK5VR pins should be as short as possible to reduce the magnetic loop. Use several via pads when routing between layers.

LDOs

Input Capacitor

The input capacitors should be located as close as possible to the power pins, LDO2P5V_IN and REG_IN, and ground (GND). Ceramic capacitors are recommended for their lower ESR and small profile. See Table 5 for voltage ratings.

Output Capacitor

For proper load voltage regulation and operational stability, a capacitor is required on the output of each LDO (LDO2P5V and LDO5V). The output capacitor connection to the ground pin (GND) should be made as short as practical for maximum device performance. Since the LDOs have been designed to function with very low ESR capacitors, a ceramic capacitor is recommended for best performance.

PCB Layout Considerations

- For optimum device performance and lowest output phase noise, the following guidelines should be observed. Please contact IDT Inc. for Gerber files that contain the recommended board layout.
- As with all switching power supplies, especially those providing high current at high switching frequencies, layout is an important design step. If layout is not carefully done, the regulator could show instability as well as generate EMI problems. Therefore, use wide and short traces for high-current paths.
- An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers. Other signal traces should be routed away from the IDTP9020. This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.
- Layout and PCB design have a significant influence on the power dissipation capabilities of power management ICs because the surface mount packages used with these devices rely heavily on thermally conductive traces or pads to transfer heat away from the package. Appropriate PC layout techniques should be used to remove the heat due to device power dissipation.

Product Datasheet

- The following general guidelines will be helpful in designing a board layout for lowest thermal resistance:
 1. PC board traces with large cross sectional areas remove more heat. For optimum results, use large-area PCB patterns with wide copper traces, placed on the uppermost side of the PCB.
 2. In cases where maximum heat dissipation is required, use double-sided copper planes connected with multiple vias.
 3. Thermal vias are needed to provide a thermal path to inner and/or bottom layers of the PCB to remove the heat generated by device power dissipation.

Power Dissipation and Thermal Requirements

The IDTP9020 is offered in a QFN56 package which has a maximum power dissipation capability of about 1.4W, defined by the die's specified maximum operating junction temperature, T_J , of 125°C. The junction temperature rises when the heat generated by the device power dissipation goes through the package thermal resistance. The QFN56 package offers a typical thermal resistance, junction to ambient (θ_{JA}), of 28.5°C/W when the PCB layout and surrounding devices are optimized as described in the PCB Layout Considerations section. The techniques as noted in the PCB layout section must be followed when designing the printed circuit board layout, as well as the placement of the IDTP9020 IC package in proximity to other heat-generating devices in a given application design. The ambient temperature around the power IC will also have an effect on the thermal limits of an application. The main factors influencing θ_{JA} (in the order of decreasing influence) are PCB characteristics, die/package attach thermal pad size, and internal package construction. Board designers should keep in mind that the package thermal parameter θ_{JA} is influenced by the characteristics of the PCB upon which the QFN is mounted. For example, in a still-air environment, as is often the case, a significant amount of the heat generated (~85%) sinks into the PCB. Changing the design or configuration of the PCB changes the overall thermal resistivity and, thus, the board's heat-sinking efficiency.

The use of integrated circuits in low-profile and fine-pitch surface-mount packages requires special attention to

power dissipation. Many system-dependant issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components, affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below:

1. Improving the power dissipation capability of the PCB design
2. Improving the thermal coupling of the component to the PCB
3. Introducing airflow into the system

First, the maximum power dissipation for a given situation should be calculated:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

In which

$P_{D(MAX)}$ = Maximum Power Dissipation (W)

θ_{JA} = Device Junction-to-Ambient Thermal Resistance (°C/W)

$T_{J(MAX)}$ = Maximum Device Junction Temperature (°C)

T_A = Ambient Temperature (°C)

The maximum recommended junction temperature ($T_{J(MAX)}$) for the IDTP9020 device is 125°C. The thermal resistance of the 56-pin NQG package (NGQ56) is optimally $\theta_{JA}=28.5^\circ\text{C/W}$. Operation is specified to a maximum steady-state ambient temperature (T_A) of 85°C. Therefore, the maximum recommended power dissipation is:

$$P_{D(Max)} = (125^\circ\text{C} - 85^\circ\text{C}) / 28.5^\circ\text{C/W} \cong 1.4 \text{ Watt}$$

Thermal Overload Protection

The IDTP9020 integrates thermal overload shutdown circuitry to prevent damage resulting from excessive thermal stress that may be encountered under fault conditions. This circuitry will shut down or reset the device if the die temperature exceeds 140°C. To allow the maximum load current on each regulator and resonant transmitter, and to prevent thermal overload, it is important to ensure that the heat generated by the IDTP9020 is dissipated into the PCB. The package exposed paddle must be soldered to the PCB, with multiple vias evenly distributed under the exposed paddle and exiting the bottom side of the PCB. This improves heat flow away from the package and minimizes package thermal gradients.

Special Notes**NQG TQFN-56 Package Assembly**

Note 1: Unopened Dry Packaged Parts have a one year shelf life.

Note 2: The HIC indicator card for newly-opened Dry Packaged Parts should be checked. If there is any moisture content, the parts must be baked for a minimum of 8 hours at 125°C within 24 hours of the assembly reflow process.

PACKAGE OUTLINE DRAWING

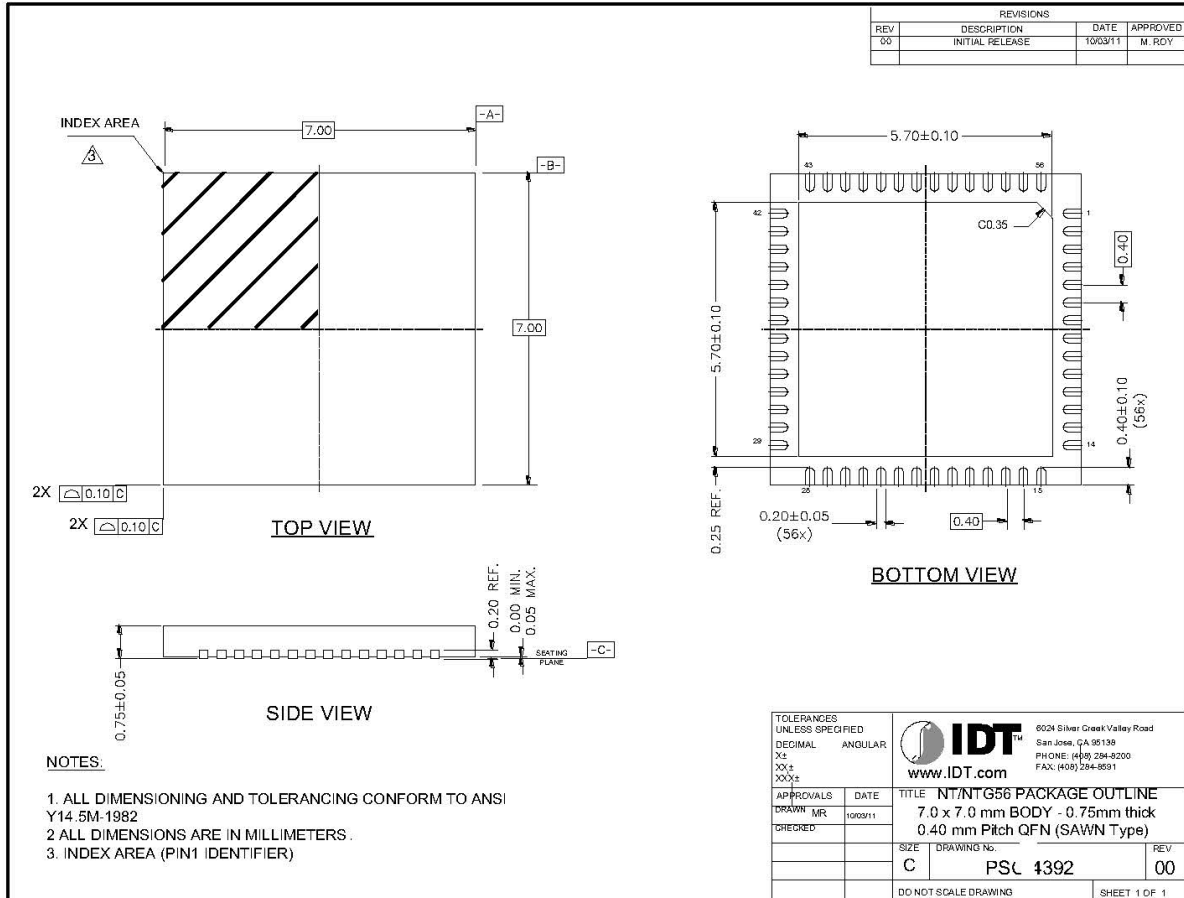


Figure 15. Package Outline Drawing (QFN NDG56 7x7x1mm 56-Ild)

ORDERING GUIDE

Table 6. Ordering Summary

PART NUMBER	MARKING	PACKAGE	AMBIENT TEMP. RANGE	SHIPPING CARRIER	QUANTITY
P9020NDG	P9020NDG	QFN-56 7x7x1mm	0°C to +85°C	Tape or Canister	25
P9020NDG8	P9020NDG	QFN-56 7x7x1mm	0°C to +85°C	Tape and Reel	2,500



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