

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO. LTD.
Petitioner,

v.

WIPQTUS INC.
Patent Owner.

U.S. Patent No. 10,038,339

Inter Partes Review No. IPR2024-00023

DECLARATION OF DR. RANDAL H. DIREEN IN FURTHER SUPPORT
OF PATENT OWNER'S REVISED MOTION TO AMEND AND IN
REBUTTAL TO SECOND SUPPLEMENTAL
DECLARATION OF JOSHUA PHINNEY

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I, Randal H. Direen, hereby declare as follows:

I. INTRODUCTION

1. I have previously provided my *Declaration of Dr. Randal H Direen in Support of Patent Owner's Preliminary Response* executed on January 17, 2024 and filed as Exhibit 2001 (the "Direen Preliminary Declaration"). I have also provided my *Declaration of Dr. Randal H. Direen in Support of Patent Owner's Response* executed June 5, 2024 and filed as Exhibit 2003 (the "Direen Declaration"). In addition, I provided testimony in my deposition taken on August 6, 2024, the transcript of which I have reviewed, which transcript I understand has been filed by Petitioner/Samsung as Exhibit 1019 ("Direen Deposition"). I have also previously provided the *Declaration of Dr. Randal H. Direen in Support of Patent Owner's Revised Motion to Amend* ("Direen III Declaration") dated October 9, 2024 submitted as Exhibit 2008. I also provided testimony in my deposition taken on November 14, 2024, the transcript of which I have reviewed, which transcript I understand has been filed by Petitioner/Samsung as Exhibit 1020 ("Direen II Deposition").

2. I have been asked to review (1) the *Second Supplemental Expert Declaration of Joshua Phinney, in Support of Petitioner's Opposition to Revised Motion to Amend U.S. Patent No. 10,038,339* dated November 20, 2024, filed as Exhibit 1021 ("Phinney Second Supp. Decl.") and (2) *Petitioner's Opposition to*

Patent Owner's Revised Motion to Amend filed as Paper No. 20. These Materials are in addition to those identified in my prior declarations noted above.

3. I have been asked by counsel for WiPQTUS Inc. (“WiPQTUS”) in the above-captioned matter as an independent consultant to offer opinions in rebuttal to positions taken by Petitioner Samsung Electronics Co. Ltd. (“Samsung”) and/or Mr. Phinney in the above-referenced Materials, and particularly the Phinney Second Supplemental Declaration (Ex. 1021).

II. QUALIFICATIONS AND COMPENSATION

4. My qualifications and compensation were previously stated in my Preliminary Declaration, which I incorporate herein.

5. My opinions are based in part on a review and analysis of the above-mentioned documents and materials as well as those materials that I have previously identified. I have also drawn on my education, experience, and knowledge of basic engineering and circuit design principles in forming my opinions.

III. UNDERSTANDING OF THE LAW

6. I am not an attorney. However, I understand and have been informed of several legal principles, which I have employed in forming my opinions in this declaration. I set forth my understanding of the legal principles in my Preliminary

Declaration, my Declaration, and my Direen III Declaration, which I incorporate herein by reference. *See* Exhibit 2001, Section V; Exhibit 2003, Section V. In addition, I am familiar with these legal principles as a result of my experience as an expert in other matters involving infringement/non-infringement and/or validity/invalidity.

7. I have not previously addressed enablement. I understand that the Patent Statute 35 U.S.C. §112 requires that the inventor set forth in the specification "a written description of the invention, and of the manner and process of making and using it [the invention of a claim], in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains... ." I also understand and have been instructed that to prove that a claim is invalid for lack of enablement, a challenger must show by clear and convincing evidence that a person of ordinary skill in the art would not be able to practice the claimed invention without "undue experimentation." In analyzing undue experimentation, at least the following factors must be considered: (1) the quantity of experimentation necessary, (2) the amount of direction or guidance presented, (3) the presence or absence of working examples, (4) the nature of the invention, (5) the state of the prior art, (6) the relative skill of those in the art, (7) the predictability or unpredictability of the art, and (8) the breadth of the claims.

8. I understand and have been instructed that a claim of a patent is indefinite if it fails to inform, with reasonable certainty, those skilled in the art about the scope of the invention.

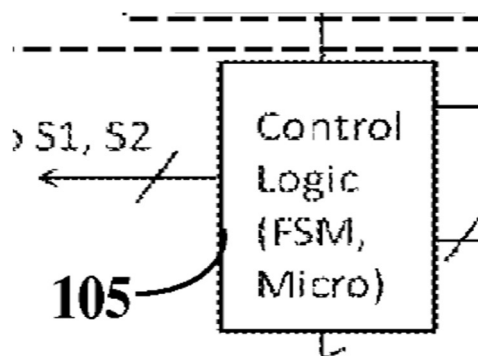
IV. ANALYSIS REGARDING ENABLEMENT

9. I understand from reviewing the Response and Dr. Phinney's Second Supplemental Declaration that Dr. Phinney contends that Substitute Claims 21 and 22 are invalid for indefiniteness and enablement. *See* Ex. 1021, ¶ 16. In reviewing Dr. Phinney's Declaration, I understand that he is basing his opinion on a statement I made in my prior Declaration in distinguishing the Lee and Cook references. *See* Ex. 1021, ¶ 18 (referencing ¶¶ 73 - 77 in my Declaration (Ex. 2008)). I note that Dr. Phinney and Petitioner no longer rely on the Lee reference. Dr. Phinney relies apparently on the following sentence (from Ex. 2008, ¶ 75): "Cook does not contain any control logic to monitor the power delivered to a system battery for the purpose of managing responsive topological changes to the rectifier." In making this statement, I was relying on the language of Substitute Claim 21 as written.

10. Claim 21 specifically states that the "first circuitry" must be capable of being "configured to change, while configured to receive said power, the impedance of said impedance network and topology of said switch network." Critically, these changes are made for a reason -- "to obtain a modified form of said received power, and apply said modified form of said power to said load

device." In addition, the "control logic" of the "first circuitry" is responsible for making the changes for this claimed purpose. I as well as a POSA would understand in the context of the claim as well as the specification ('929/'339 Patent) that the "control logic" provides the ability to monitor, meaning to receive one or more inputs in order to provide the output that causes the claimed changes to accomplish the claimed purpose. Without input, there would be no meaningful reason to change the output.

11. For example, the "control logic circuit 105" is described as making two adjustments, one to impedance and one to the "topology of the switch network 102" based on two different inputs, (1) the type of wireless transmitter that is sending the power and (2) "the level of wireless power being received." '929 Patent, Col. 8, ll. 55 - 61. The '929 Patent discloses that the control logic is implemented by a finite state machine ("FSM"), a microprocessor, or the like. This is shown in Figure 1:



Ex. 2002, Figure 1; see also Ex. 1001, Figure 1. Element 105 is further described:

"[t]he control logic 105 is, for example, a state machine, a microcontroller, etc."

Ex. 2002, '929 Patent, Col. 7, ll. 8 - 9. A state machine, inter alia, provides an output based on one or more inputs. IBM Dictionary of Computing, p. 273

(McGraw-Hill, Inc. 1994). Exhibit 2010. As explained above, the '929 Patent describes two inputs. Ex. 2002, '929 Patent, Col. 8, ll. 55 - 61. The output is a control signal that causes the impedance and topology to change. It would be well within the ordinary skill of a POSA to design control logic based on the description given to meet limitations Claim 21 without undue experimentation.

12. As Claim 21 is written, the control logic is not required to "identify the wireless transmitter." However, Claim 21 as written requires that the control logic have some ability to "monitor" the power being applied to the load device to make the requisite changes to obtain a "modified form of said received power. This understanding is consistent with portions of the specification described above. Hence, my answer to the last question directed to "control logic" in my last deposition is entirely accurate:

Q: Do you consider that limitation as meeting what you describe as a control logic to monitor the power delivered to the system battery?

A: I believe that's what it's discussing on the next page, in Fig. 5 where it says, "said first circuit based on input from said control

logic circuit, configured to change, while configured to receive said power -- said power, the impedance of said impedance network and topology of said switch network to obtain a modified form of said received power, and apply modified form of power to said load device."

Ex. 1020, p. 118, l. 21 - p. 119, l. 10.

13. I note that Dr. Phinney provided little analysis and did not discuss the provisions of the specification noted above. Dr. Phinney did not discuss his understanding of control logic nor the degree of "experimentation" that would be required of a POSA to design "control logic" meeting the limitations for the claim. In my opinion, designing circuitry that includes control logic (such as state machines, microcontrollers and the like) is one of the more common tasks that a POSA would perform. A POSA would have no trouble implementing the first circuitry as claimed and described with little experimentation if any. In my opinion, "control logic" and limitation 21[e] ("said first circuitry, based on input from control logic, configured to change, ... topology of the switch network") is disclosed in sufficient detail in the '310 Application for the '929 Patent to meet the enablement requirement of Section 112.

V. ANALYSIS REGARDING INDEFINITENESS

14. I understand from reviewing the Response and Dr. Phinney's Second Supplemental Declaration that Dr. Phinney contends that Substitute Claims 21 and 22 are invalid for indefiniteness. *See* Ex. 1021, ¶ 16.

15. In my last Declaration in support of WiPQTUS' Revised Motion to Amend (Ex. 2008), I provided a construction of "topology" and "change ... topology" as found in supplemental Claim 21. *See* Direen II Declaration, Ex. 2008, ¶¶ 22 - 41. I further note that Claim 21 expressly states "said first circuitry, based on an input from said control logic circuit, configured to change, while configured to receive said power, the impedance of said impedance network and topology of said switch network to obtain a modified form of said received power, and apply said modified form of said power to said load device." In the context of this limitation, the relevant "topologies" are rectifiers not inverters since rectifiers are used to convert AC to DC current to charge a load device such as a battery.

16. In light of the express language of Claim 21, I am puzzled as to why Dr. Phinney discusses two well-known types of inverters, Class D and Class E, as opposed to focusing on the types of rectifiers disclosed in the specification. *See* Ex. 1021, ¶¶ 22 - 23. As I previously explained in connection with my constructions, the '929 Patent discloses at least three types of rectifiers, non-synchronous, half-

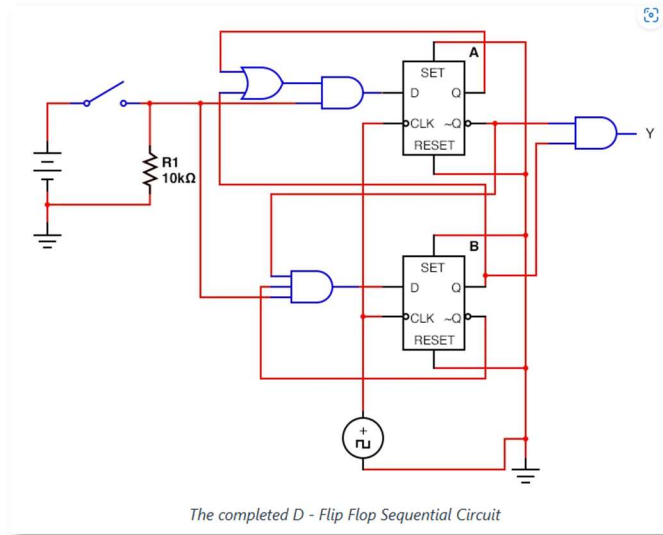
synchronous, and full synchronous. Ex. 2008, ¶¶ 22 - 23; *e.g.*, Ex. 2002, '929 Patent, 3:67-4:3, 4:9-18, 14:41-58, Figs. 6A-B, Figs. 7A-B.

17. The three types of rectifiers are simply examples among others. The types of inverters, Class D and E, are just two well-known types of inverters. As I previously explained, taking just the language "configured to change ... topology," ignoring the express language, "configured to receive power," a change in topology would include changing from one type of rectifier to another, changing from a rectifier to an inverter or vice versa, or changing from one type of inverter to another. Ex. 2008, ¶ 42. The phrase "while configured to receive power" further limits the requisite "change ... topology of said switch network" to a change from one type of rectifier to another. I further note that the "topology" in the limitation that follows, "said first circuitry ... configured to change said topology ... to transmit..." pertains to the change from a rectifier to an inverter. I further note that Claim 21 is silent as to any changes between types of inverters. Therefore, Dr. Phinney's comments regarding Type D and E inverters are not relevant to understanding Claim 21. In conclusion, in my opinion Claim 21 provides reasonable notice to a POSA as to claim scope and is not indefinite.

VI. ADDRESSING DR. PHINNEY'S ANALYSIS OF THE COMBINATION OF CHATTERJEE, CORBRIDGE, COOK, AND KNOWLEDGE OF POSA

18. I understand from reviewing the Response and Dr. Phinney's Second Supplemental Declaration that Dr. Phinney contends that the proposed substitute Claims 21 and 22 are invalid on two grounds, each of which is based on the combination of Chatterjee, Corbridge, Cook, and some ill-defined "Knowledge of a POSA." *See* Ex. 1021, Phinney II Supp. Decl., ¶ 24.

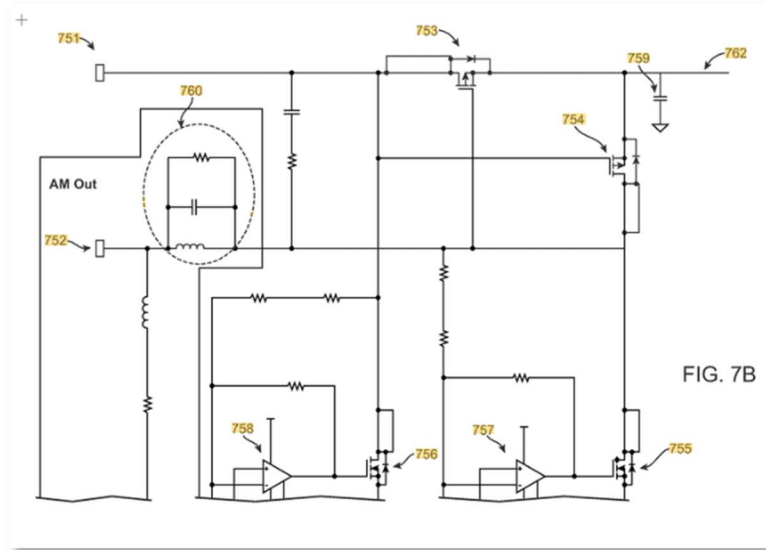
19. Dr. Phinney asserts that Corbridge discloses a control logic circuit that controls the switch network and points to Figure 7B. I do not see any control logic circuit in Figure 7B. There are clearly diodes, MOSFETS, resistors capacitors, inductors and op amps, but I do not see circuitry that includes a control logic circuit. In the art, control logic is usually shown as a microcontroller, an FPGA (field programable gate array), etc. At the very least, control logic would need to be something that could implement a state machine (such as logic gates and flip flops shown in the example figure below).



Exemplar D – Flip Flop Sequential Circuit¹

20. In fact, as discussed above, the '929 Patent (at Col. 7, ll. 8 - 9; Col. 8, ll. 55 - 61; Fig. 1; *see also* '339 Patent (*e.g.*, Fig. 1; Col 9, l. 15) provides examples such as state machines and microcontrollers which a POSA would use to confirm his or her understanding of the term “control logic circuit” as used in the claims. The circuitry shown in Figure 7B of the Corbridge (Ex. 1004, U.S. Publication No. 2010/0083012) does not show any control logic circuit:

¹ Example from All About Circuits website:
<https://www.allaboutcircuits.com/textbook/digital/chpt-11/finite-state-machines/>



Ex. 1004, Corbridge, Fig. 7B

21. Further, Figure 7B of the Corbridge (Ex. 1004) does not show any interface that would connect to control logic circuit. Based on Paragraphs 85 and 86 of Corbridge (Ex. 1004), power and data come into ports 751 and 752. Power is rectified through the transistor diode pairs 753, 754, 755, and 756, and sent out on line 762. Data is sent out through the data signal line 761. I do not see any additional input and output locations that control logic circuit would interface. Since the figure is labeled “Synchronous Bridge,” there would be no reason for additional inputs and outputs because it does what it says it does, it is a synchronous bridge rectifier. In the art, the drawing labeled Synchronous Bridge of Figure 7B is a classic example of an analog circuit that contains no control logic circuit. Engineers are taught this in undergraduate school. A POSA would not identify anything within this circuit as control logic circuit.

22. In paragraph 84 of Phinney's declaration he states that the transistors diode pairs of Figure 7B can "selectively" operate as different configurations of a rectifier. He then references Corbridge Paragraph 85. I see nowhere within Paragraph 85 where Corbridge states or indicates that different rectifier configurations can be "selected." It appears that Corbridge merely provides alternative configurations of a rectifier:

The power component of the received AC signal is converted to a DC power signal using a synchronous bridge or rectifier formed by diodes 753, 754, 755, and 756. The synchronous bridge corresponds to the synchronous bridge 730 of FIG. 7A. A half-synchronous bridge *may alternatively* be used.

Ex. 1004, Corbridge, Paragraph 85 (emphasis added). Corbridge (Ex. 1004) simply does not describe selecting between different rectifier configurations (topologies).

23. Corbridge does indicate in Paragraph 85 that the diodes paired with the MOSFETs in Figure 7B can be used for the purpose of rectification. However, for that to work with this particular circuit, certain modifications would be necessary to keep the MOSFETs off. For example, the op amp 758 (when properly powered with a voltage source as I will explain later) turns the 758 transistor on when the voltage at 751 drops below the ground reference (or 0 volts). To keep the 758 transistor from turning on, the op amp would need to be disconnected from it and the gate of the 756 would perhaps need to be tied to ground. Other

modifications to the circuit would be required to ensure that all transistors do not turn on.

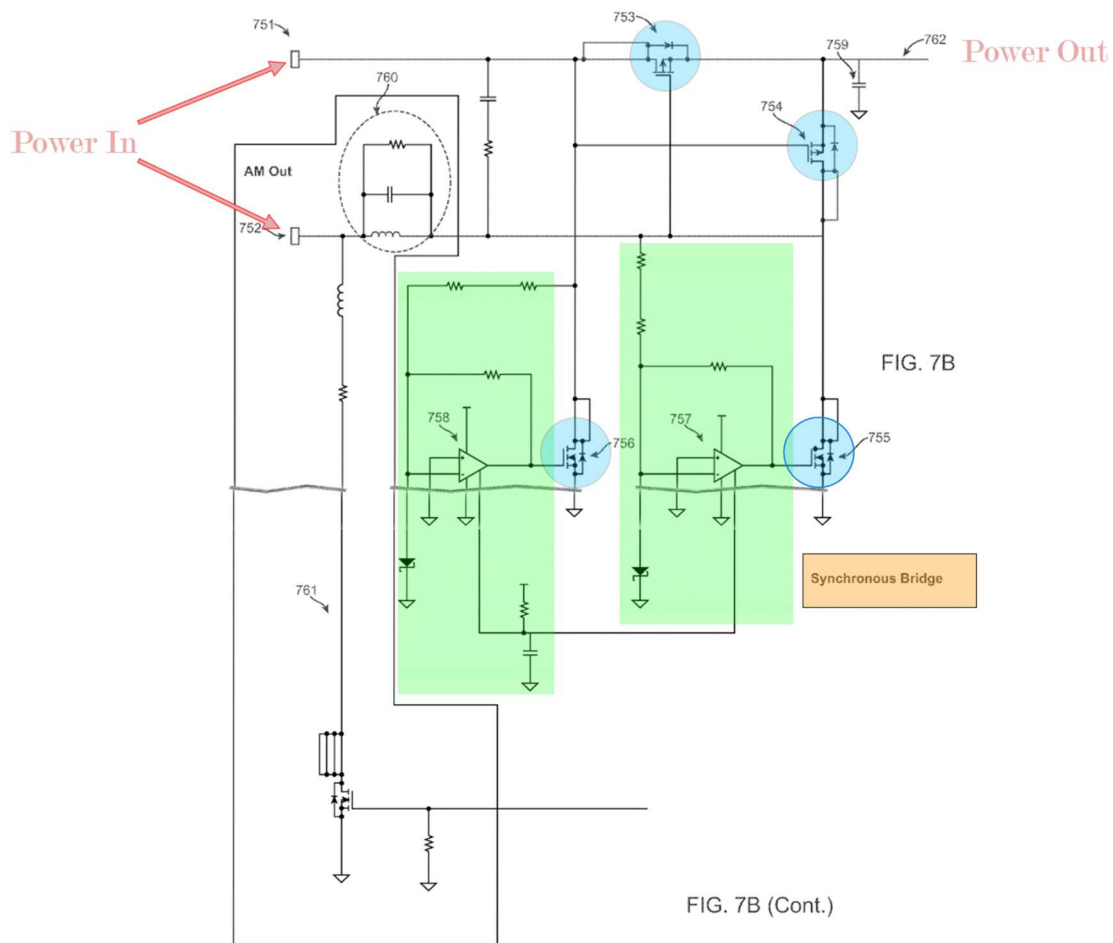
24. Certain details of the particular circuit, labeled Synchronous Bridge, and shown in Figure 7B are described by Corbridge in Paragraph 86 of the Corbridge (Ex. 1004). Corbridge does not describe in any way how the circuit can be used as a non-synchronous rectifier. There are no provisions for disabling transistors 753, 754, 755, and 756. The circuit as it is drawn cannot be used as a non-synchronous rectifier.

25. Dr. Phinney attempts to provide an explanation for how the circuit of Figure 7B can be used as a non-synchronous rectifier in Paragraph 85 of his Declaration, (Ex. 1021). However, his explanation is misguided. To begin with, Corbridge does not disclose anywhere that the circuit first operates in a non-synchronous mode and then transfers to a synchronous mode when the voltage gets to a certain level. In Paragraph 85 of his Declaration (Ex. 1021), without explanation, Dr. Phinney makes the claim that a POSA would understand that the term “becomes forward-biased” indicates that current flows through the diode. However, forward biased simply means that a positive voltage is applied to the terminals. To be specific in the case of a diode, forward biased means a positive voltage is applied across the anode to the cathode. For example, an ideal diode can also be reversed biased, and under this condition no current will flow. Further, Dr.

Phinney indicates in middle of Paragraph 85 (Ex. 1021), that a POSA would understand that diodes 755 and 756 of Figure 7B conduct current before the transistors get “turned[ed] on.” It is well known in the art that there is a small voltage across a diode when current flows through it, and this voltage is called “voltage drop.” With respect to the circuit of Figure 7B, Corbridge states “In each of the transistor diode pairs, 753, 754, 755, and 756, a transistor (typically MOSFET) is connected in series with a diode *to eliminate voltage drop* across the diode when the diode is forward biased” Paragraph 86 of Corbridge (Ex. 1004), emphasis added. To “eliminate” the voltage drop across a diode is to ensure that no current flows through the diodes. Dr. Phinney goes on to say that “transistors 755 and 756 would only actively switch on and off when the incoming voltage is above a certain threshold,” but Corbridge says nothing about a threshold. Conversely, and for example with respect to one of the transistor diode pairs, Corbridge states “Op Amp 757 is configured and coupled to output a voltage level to *turn on the transistor* of transistor diode pair 755 *when the diode of transistor diode pair 755 becomes forward biased*” Paragraph 86 of Corbridge (Ex. 1004) (emphasis added). Thus, Corbridge’s description of the circuit indicates that the transistor is turned on “when” the diode is forward biased, or as soon as a positive voltage is applied to the diode. The description provided by Dr. Phinney in Paragraph 85 (Ex, 1021) is

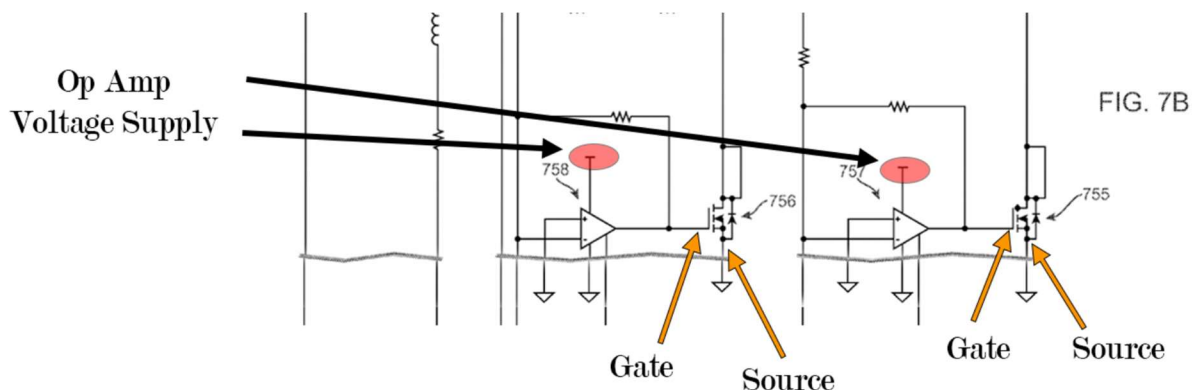
incorrect. I will now provide the correct explanation of the circuit described in Paragraphs 85 - 86 of Corbridge (Ex. 1004).

26. As the text within Figure 7B of Corbridge (Ex. 1004) indicates, the circuit is a Synchronous Bridge rectifier, which means the circuit will turn transistors 753, 754, 755, and 756 on and off synchronously with the incoming signal at 751 and 752 to rectify the output at 761:



Ex. 1004, Corbridge, Figure 7B (with my notations).

27. The op amps 758 and 757 are used to detect when to turn transistors 756 and 755 on and off (see Paragraph 86 of the Corbridge). For example, when the voltage at 751 goes above ground potential (or when diode 756 becomes reverse biased), the op amp 758 will turn transistor 756 off. Conversely, op amp 757 will detect that the voltage at 752 is less than ground potential and turn transistor 755 on (when diode 755 becomes forward biased). This is supported by the first four sentences in Paragraph 86 of Corbridge (Ex. 1004). The figure indicates that transistors 756 and 755 are Enhancement-mode N Channel MOSFETs, which implies that they can be turned on by applying a voltage from their gate to source (see image below). Power is sourced from the voltage supply that connects to the op amp (labeled Voltage Supply below). (Operational amplifiers require an external voltage supply to power them.)



Ex. 1004, Corbridge, Fig. 7B (with my annotations). Essentially, the op amps are configured as “comparators” to compare voltages at the inputs labeled “+” and “-“. For example, when the voltage at “+” is higher than the voltage at “-“ on the 758

op amp, a voltage derived from the Voltage Supply is applied to the gate of the 756 transistor, and the voltage is such the transistor is fully turned on (Paragraph 86 of Corbridge). This design is beneficial because it bypasses the diodes attached to 756 and 755 as soon as there is a forward bias on the diodes, the transistors turn on to ensure no current goes through the diodes. If current starts flowing through the diodes, there will be a voltage drop, power will be lost to them in the form of heat (meaning the circuit becomes less efficient).

28. In Paragraph 86 of Phinney's Declaration (Ex. 1021) he claims that a POSA would have had the insight to take the op amp circuit from Corbridge and insert it into Chatterjee's circuit of Figure 6D in the '356 patent to make a circuit that could switch between a non-synchronous and synchronous rectifier. Based on the discussion above, this circuit would not switch between configurations without modification or some additional design work. Additionally, the op amps would require external power supplies to work. Additionally, simply adding op amps to the circuitry from the Corbridge does not satisfy any form of control logic. There is a lot more work that a POSA would need to put into the circuit of Corbridge (e.g., shown in Fig. 7B) to enable it to change between rectifier topologies. I note that Dr. Phinney did not explain how this could be done.

29. In conclusion, for reasons previously stated and as stated above, my opinion remains that a POSA would **not** find the inventions of Substitute Claims

21 and 22 obvious in view of the differences between the claimed inventions and each of the combination of Chatterjee, Corbridge, Cook, and Dr. Phinney's ill-defined knowledge of a POSA. *See, e.g.*, Ex. 2008, ¶ 79. For example, among other reasons provided, neither Chatterjee, Corbridge, or Cook disclose anything meeting the limitation "said first circuitry, based on an input from said control logic circuit, configured to change, while configured to receive said power, said topology of said switch network to obtain a modified form of said received power, and apply said modified form of said power to said load device." Furthermore, Dr. Phinney has not identified any particular knowledge of a POSA that would "fill-in" or substitute for this missing limitation. Therefore, in my opinion substitute Claims 21 and 22 are patentable.

I declare under penalty of perjury that the foregoing is true and correct.

Executed this 12th day of December, 2024.

/s/ Dr. Randal H. Direen

DR. RANDAL H. DIREEN