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**UNITED STATES DISTRICT COURT
NORTHERN DISTRICT OF CALIFORNIA
SAN FRANCISCO DIVISION**

SEMICONDUCTOR DESIGN
TECHNOLOGIES, LLC,

Plaintiff,

v.

CADENCE DESIGN SYSTEMS, INC.,

Defendant.

Case No. 3:23-cv-01001-AMO

**PLAINTIFF'S OPPOSITION
TO MOTION TO DISMISS FIRST
AMENDED COMPLAINT**

Date: October 12, 2023
Time: 2:00 p.m.
Courtroom: 10, 19th Floor
Judge: Hon. Araceli Martínez-Olguín

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I. INTRODUCTION

Plaintiff and patent owner Semiconductor Design Technologies, LLC (“SDT”) opposes Defendant Cadence Design Systems, Inc.’s (“Cadence”) Motion to Dismiss (“Motion”, Dkt. 42) in its entirety. Nothing Cadence argues comes close to overcoming the strong presumption that U.S. Patent Nos. 7,603,636 (“the ’636 patent”) and 7,971,167 (“the ’167 patent”) (collectively the “Asserted Patents”) are valid. The record evidence in the First Amended Complaint and this Opposition demonstrates that the Asserted Patents readily satisfy the requirements of 35 U.S.C. § 101. Moreover, before the merits of Cadence’s invalidity argument can even be addressed, the disputed claim construction issues and disputed issues of material fact must be resolved, neither of which should be done in a Rule 12(b)(6) motion. Cadence’s motion also asks the Court to consider a 244-page patent file history, to which Cadence selectively refers, something Cadence is not allowed to do at the 12(b)(6) stage. These issues each independently and collectively preclude the granting of Cadence’s motion to dismiss, where it must be assumed that all of the non-conclusory allegations of the complaint are true, even before Cadence’s unsupported invalidity arguments are addressed. Simply put, Cadence’s motion is not an appropriate 12(b)(6) motion and should be denied.

SDT filed a First Amended Complaint (“FAC”, Dkt. 41) containing well-substantiated allegations that the ’636 and ’167 patents are not abstract (*i.e.*, directed to specific technological improvements to their respective areas of technology), and contain inventive concepts (*e.g.*, an ordered combination consisting of a technological improvement upon and that overcomes problems associated with prior art approaches). The FAC incorporates an expert declaration from MIT-trained physicist and experienced chip designer John Berg that further supports the allegations made in the FAC. These allegations, including Mr. Berg’s statements, must be accepted as true in deciding Cadence’s motion as they are well-pleaded and not conclusory.

Moreover, before any patent eligibility analysis can even be undertaken, Cadence’s arguments reveal significant claim construction disputes germane to the eligibility analysis, for example as to the meaning of claim terms “property generating step” and “latency analyzer.” Such claim construction disputes preclude the granting of Cadence’s motion at the 12(b)(6) stage. *Nalco*

1 *Co. v. Chem-Mod, LLC*, 883 F.3d 1337, 1350 (Fed. Cir. 2018) (not appropriate to resolve claim
2 construction disputes on a Rule 12(b)(6) motion, without the benefit of claim construction).

3 Further, in contravention of the requirements for a 12(b)(6) motion, Cadence’s motion relies
4 on unsupported allegations and unsupported attorney argument improperly presented as expert
5 opinions. Such disputed and unsupported statements should not be accepted as true. In overruling
6 the granting of a 12(b)(6) motion on § 101 grounds, the Federal Circuit has explained how disputed
7 fact issues, as is the situation here, preclude granting such a motion:

8 We have held that patent eligibility can be determined at the Rule 12(b)(6) stage.
9 ***This is true only when there are no factual allegations that, taken as true, prevent***
10 ***resolving the eligibility question as a matter of law. Indeed, we have explained***
11 ***that plausible factual allegations may preclude dismissing a case under § 101***
where, for example, nothing on the record refutes those allegations as a matter of
law or justifies dismissal under Rule 12(b)(6).

12 *Aatrix Software, Inc. v. Green Shades Software, Inc.*, 882 F.3d 1121, 1125 (Fed. Cir. 2018)
13 (emphasis added) (citations and quotations omitted).

14 Here, there are various unsupported factual allegations by Cadence including, for example,
15 the following:

- 16 • Cadence states: “The ’636 patent admits that it seeks to automate a step that
17 engineers typically performed by hand when designing an Integrated Circuit
18 (“IC”).” Mot. at 2-3.
- 19 • Cadence states: “the ’636 patent admits that its alleged invention automates a
20 verification methodology that had been performed manually by engineers using
21 pen and paper (or finger and keyboard).” Mot. at 11.

22 Likewise, there are various attorney arguments presented by Cadence as though they were
23 substantiated expert opinions, but that are unsupported by the pleading record and not agreed to:

- 24 • Cadence states: “When designing an IC, managers and engineers write a design
25 specification, for example using Microsoft Office to create figures or charts, to
26 provide a vision for what the circuit is supposed to do.” Mot. at 4.
- 27 • Cadence states: “A state machine is a conceptual model that moves from one
28 state to the next, e.g., a stop light moving between its three states (green, yellow,
and red).” Mot. at 7.

29 Technical tutorial like this should not be accepted as true for purposes of Cadence’s motion.
30 Rather, this material should be seen as what it is – attorney argument in lieu of properly submitted
31 expert testimony. *See, e.g., Invitrogen Corp. v. Clontech Lab ’ys, Inc.*, 429 F.3d 1052, 1068 (Fed.
32 Cir. 2005) (“Unsubstantiated attorney argument regarding the meaning of technical evidence is no

substitute for competent, substantiated expert testimony.”) These statements should be given the least possible weight because they are no more than attorney argument.

Such unsupported “technical tutorial” material is then used to formulate unsupported inferences in Cadence’s favor, such as the following:

- Cadence states: “Determining the portions of behavioral code that corresponded to particular (high latency) portions of the RTL description was a simple matter of referring to the correspondence table—a simple mental task of reading a table, which humans have done for centuries before computers.” Mot. at 22.

With respect to the merits of Cadence’s § 101 argument, Cadence relies heavily on *Synopsys, Inc. v. Mentor Graphics Corp.*, 839 F.3d 1138, 1150 (Fed. Cir. 2016) to suggest that the ’636 and ’167 claims should be doomed to suffer the same fate. However, *Synopsys* is not applicable. The claims of the patents in *Synopsys* were quite different than the claims of Plaintiff’s patents. Unlike the claims at issue in this case, which are directed to a technological improvement to existing technology performed on a computer and specifically include computer functionality, the claims at issue in *Synopsys* did not call for any form of computer implementation: “Because the Asserted Claims make no mention of employing a computer or any other physical device, they are so broad as to read on an individual performing the claimed steps mentally or with pencil and paper.” *Synopsys*, 839 F.3d at 1149. *Synopsys* declined to consider whether a “computer-implemented version of the invention would not be ‘directed to’ an abstract idea.” *Id.* Given the claim construction issues and disputed issues of fact raised by Cadence’s motion, as well as Cadence’s attempt to inject materials from outside the pleadings into the 12(b)(6) record and its substantively deficient arguments, Cadence’s 12(b)(6) motion should be denied.

II. BACKGROUND

The ’636 patent relates to semiconductor technology that involves generating and verifying design data of a semiconductor integrated circuit. The ’636 patent discloses graphically editing a specification of an integrated circuit and generating a property that verifies the specification of the semiconductor integrated circuit based on design data. The property is in turn converted into an “assertion description language” if the property is to be verified, or checked, during a process called “asset verification.” The ’636 patent explains that the “conventional technologies,” *i.e.*, the prior

art, have a specific technical problem: “matching the circuit specifications with the assertion description cannot be assured.” ’636 patent, 4:29-31. The invention of the ’636 patent “solve[s] the problems in the conventional technologies, for example, to enable high reliability and high efficiency in assertion verification for an LSI,” or large-scale integration. *Id.*, 4:35-38. To accomplish this goal, a property to be verified is automatically converted into an assertion description language based on the circuit specification. *Id.*, 4:35-44.

The other Asserted Patent, the ’167 patent, relates to a semiconductor design support device for designing a semiconductor integrated circuit. A “behavioral description” describes an algorithm of processing performed by hardware at a motion (*e.g.*, operation) level. A tool, such as a behavioral synthesis tool, generates what is known as an “RTL description” from the behavioral description, and specifies in the “RTL description” registers and clock synchronisms particular to the hardware. Conventionally, the RTL can be analyzed using a simulator to check for latency, but the ’167 patent states that there is no effective way to determine which portions of the corresponding behavioral description is associated with the latency measurement. ’167 patent, 1:56-62. The claimed invention of the ’167 patent provides a novel solution to this problem by providing a “latency analyzer” that “calculate[s] a latency in each block representing an operation in a predetermined unit in the behavioral description,” (*id.*, 2:9-12), in combination with a “correspondence table generator” that generates a “correspondence table in which each block in the behavioral description corresponds to a state in the RTL description.” *Id.*, Claim 1.

III. LEGAL STANDARD

A complaint will survive a 12(b)(6) motion to dismiss if it contains “enough facts to state a claim to relief that is plausible on its face.” *Bell Atl. Corp. v. Twombly*, 550 U.S. 544, 570 (2007). “Generally, a district court may not consider any material beyond the pleadings in ruling on a Rule 12(b)(6) motion.” *Hal Roach Studios, Inc. v. Richard Feiner & Co.*, 896 F.2d 1542, 1555 n. 19 (9th Cir. 1990). “However, material which is properly submitted as part of the complaint may be considered” on a motion to dismiss. *Id.*

IV. ARGUMENT

A. Cadence’s Flawed Approach to § 101 Reveals Claim Construction Issues that Prevent the Court from Deciding Defendant’s 12(b)(6) Challenge

1 Cadence improperly analyzes the claims at both Step 1 and Step 2 using a flawed approach
 2 that reveals claim construction issues, the presence of which dooms its motion. *MyMail, Ltd. v.*
 3 *ooVoo, LLC*, 934 F.3d 1373, 1380 (Fed. Cir. 2019) (“[T]he district court’s failure to address the
 4 parties’ claim construction dispute is error under *Aatrix*.”); *Nalco*, 883 F.3d at 1350. At Step 1,
 5 rather than consider the character of the claim as a whole (*Enfish, LLC v. Microsoft Corp.*, 822 F.3d
 6 1327, 1335 (Fed. Cir. 2016)), Cadence reduces each claim to a single element. At Step 2, Cadence
 7 declares that the remaining elements are known in the prior art and “cannot provide an inventive
 8 concept.” Mot. at 15. Cadence improperly “conflates patent eligibility with novelty, which are
 9 inquiries that ... are separate.” *Fitbit, Inc. v. AliphCom*, 233 F. Supp. 3d 799, 812 (N.D. Cal. 2017).
 10 Claim construction will reveal that two claim elements that Cadence seeks to ignore as prior art,
 11 should be considered as part of a proper §101 analysis. This claim construction in turn is fatal to
 12 Cadence’s motion.

13 First, Cadence’s arguments surrounding “property generating step” raise a claim
 14 construction dispute. Mot. at 10-12 (stating that claim 8 “emphasizes [] automatic generation in
 15 limitation 8[c]” and dismissing other limitations including the “property generating step” as
 16 “known in the art”). Claim construction would reveal that the “property generating step,” recited in
 17 claim 8 of the ’636 patent, excludes manually generating properties mentally conceived by a circuit
 18 designer to produce assertions. A cursory review of the ’636 patent shows that such a manual
 19 approach is specifically and repeatedly disparaged in the ’636 patent. *See, e.g.*, ’636 patent, 3:43-
 20 60, 4:4-11. The Federal Circuit has stated that “[t]o find disavowal of claim scope through
 21 disparagement of a particular feature, we ask whether the specification goes well beyond expressing
 22 the patentee’s preference... such that its repeated derogatory statements about a particular
 23 embodiment reasonably may be viewed as a disavowal.” *Openwave Sys., Inc. v. Apple Inc.*, 808
 24 F.3d 509, 513 (Fed. Cir. 2015) (internal quotation marks and brackets omitted). That is precisely
 25 the case here. The ’636 specification repeatedly makes derogatory statements about manual input
 26 of assertions, or alternatively emphasizing the benefits of the non-manual approach. *See, e.g.*, ’636
 27 patent, 3:43-60, 4:4-11, 4:35-38, 12:50-13:10. When “property generating step” is properly
 28 construed, it requires that a computer identify the properties to be identified from a circuit

1 specification and converted into assertions. Cadence’s Step 2 *Alice* arguments cannot be sustained
 2 because the “property generating step” cannot simply be set aside – it works in conjunction with
 3 the other steps to establish a non-conventional framework that allows computers to perform non-
 4 conventional functions that it otherwise could not.

5 Second, Cadence inadvertently reveals another claim construction dispute by characterizing
 6 “latency analyzer” as prior art. Mot. at 18-19 (alleging that “the other elements of claim 1 were
 7 prior art, including ... latency analysis). Claim construction would reveal that “latency analyzer”
 8 as recited in claim 1 of the ’167 patent does not recite a generic “latency analyzer” that calculates
 9 latency based on the simulation result of an RTL description. ’167 patent, 1:48-62; Berg at ¶81.
 10 Claim construction would also reveal that “latency analyzer” should be construed to exclude
 11 latency analysis that does not provide any insight as to latency associated with a behavioral
 12 description. Plainly, the language of claim 1 requires the “latency analyzer” to calculate “a latency
 13 in each block representing an operation in a predetermined unit in the behavioral description.” ’167
 14 patent, 2:9-12, 7:8-11. The ’167 patent specifically states that this is not known or possible in the
 15 prior art because the behavioral description does not recognize the concept of clock cycles: “known
 16 methods may not check the behavioral description effectively.” ’167 patent, 1:40-43, 1:61-62; FAC
 17 at ¶35; Berg at ¶82. As such, claim 1 does not encompass, nor does the specification acknowledge
 18 any prior latency analyzer that can “calculate a latency in each block representing an operation in
 19 a predetermined unit in the behavioral description.” FAC at ¶84, Berg at ¶¶80-83, ’167 patent, 2:9-
 20 12.

21 Such claim construction disputes preclude the Court from granting Cadence’s motion. *See*
 22 *Fortinet, Inc. v. Forescout Techs., Inc.*, No. 20-CV-03343-EMC, 2020 WL 6415321, at *7 (N.D.
 23 Cal. Nov. 2, 2020) (determining that “forbearing early adjudication is further warranted by the
 24 potential informative value of claim construction”). The Court must either conduct a claim
 25 construction hearing or decide the claim construction issues in SDT’s favor. In the latter case,
 26 Cadence cannot prevail because it has advanced a theory under Step 2 predicated on the dismissal
 27 of any claim element that it improperly deems “prior art.”
 28

B. The Claims of the Asserted Patents Are Patent Eligible

1. The Court Should Consider the Declaration of Mr. Berg and Should Not Consider the 244-Page File History of which Cadence Seeks Judicial Notice

Despite asserting without support that “the declaration is contradicted by the patents that it attempts to save” (Mot. at 3-4), Cadence fails to address the substance of Mr. Berg’s expert declaration anywhere in its 25-page brief, beyond urging the Court to strike it. In this same context, a Delaware court analyzed Federal Circuit case law and relied upon an expert declaration incorporated into the complaint to deny a motion to dismiss:

Defendants argue that the allegations in the [] Declaration are simply “legal conclusions” that are “completely untethered” from the [] patent, and thus need not be accepted as true. But an expert’s declaration asserting that certain features of a patent claim are “unconventional” in the prior art, combined with an explanation of why this is so and how the features provide certain benefits over the prior art, are factual assertions—not legal conclusions. Thus, they must be accepted as true at the pleading stage.

Sapphire Crossing LLC v. Quotient Tech. Inc., No. CV 18-1717-MN-CJB, 2020 WL 1550786, at *4 (D. Del. Apr. 1, 2020) (citations omitted). On page 4 of its Motion, in attempting to convince this Court to strike the declaration of Mr. Berg, Cadence states the standard for what materials are considered in a 12(b)(6) motion: “Generally, a district court may not consider any material beyond the pleadings in ruling on a Rule 12(b)(6) motion.” *Branch v. Tunnell*, 14 F.3d 449, 453 (9th Cir. 1994). This standard is undisputed; it is the application of this case that is disputed:

[A] document is not “outside” the complaint if the complaint specifically refers to the document and if its authenticity is not questioned. As it makes sense and comports with existing practice, we hold that documents whose contents are alleged in a complaint and whose authenticity no party questions, but which are not physically attached to the pleading, may be considered in ruling on a Rule 12(b)(6) motion to dismiss. Such consideration does “not convert the motion to dismiss into a motion for summary judgment.”

Branch, 14 F.3d at 453-454 (citations omitted). Here, Mr. Berg’s declaration is specifically referred to throughout the complaint (*see, e.g.*, ¶¶16-22, 25, and 27-28), and provides expert support for many of the statements in the complaint. Cadence has not questioned its authenticity, although Cadence disputes the substance, without providing any elaboration. Cadence’s other cases, often in the securities context or dealing with a different set of facts (*e.g.*, a declaration attached to an opposition, not incorporated into a complaint) do not affect this conclusion under Ninth Circuit

1 law.

2 Ironically, while urging the Court to exclude the Berg declaration, Cadence also urges the
3 Court to take “judicial notice” of a 244-page file history that is indisputably not part of the pleadings
4 and was not integral to or explicitly relied upon in the complaint. This argument has been rejected
5 by other district courts. *See Par Pharm., Inc. v. Hospira, Inc.*, No. CV 17-944-JFB-SRF, 2018 WL
6 3343238, at *2 (D. Del. May 11, 2018) (a patent’s file history should not be considered at the
7 12(b)(6) stage of proceedings).

8 **2. The FAC Includes Plausible Allegations that the ’636 Claims Are Patent
Eligible**

9 **a) At Step 1, the ’636 Claims Are Not Abstract**

10 The ’636 patent describes and claims a specific improvement over prior processes. Before
11 the ’636 patent, a computer could not read a circuit specification and produce assertions against
12 which synthesized RTL could be tested. For example, the ’636 patent describes a prior art manual
13 approach in which a designer thinks of properties and writes assertions in PSL. The ’636 patent
14 also describes another prior art approach in which assertions are generated from the RTL
15 description, which is the intended target of verification. The known and/or conventional approaches
16 to implement assertions to verify circuit designs were tedious and prone to mistakes, *e.g.*, failing to
17 accurately check the behavior of the circuit specification. FAC at ¶19; Berg at ¶¶49-52. The ’636
18 patent improves verification technology by establishing a new framework for automated and
19 efficient generation of accurate assertions. ’636 patent, 2:31; Berg at ¶57. The framework, which
20 is also recited in the claims, includes: (1) specification input, which includes graphical editing of
21 the specification; (2) property generation that reads the design data from the specification input and
22 generates a property to be verified; and (3) assertion generation that reads and converts the property
23 into an assertion description. Berg at ¶59. Importantly, the ’636 patent enables a circuit designer to
24 graphically edit the design data to generate properties and assertions in an automated and accurate
25 manner, *i.e.*, on-the-fly, in a way that no designer could do manually. *Id.* ¶68.

26 The specification inputting step includes two important components, *i.e.*, inputting circuit
27 specifications and using a graphical editor. Berg at ¶60. This step improves upon the background
28 prior art to improve both accuracy and efficiency in generating assertions. Berg at ¶60 (enumerating

eight separate improvements over manual input of assertions). An invention that automates tasks previously performed by humans is patent eligible if directed to a specific improvement over the prior process. *McRO, Inc. v. Bandai Namco Games Am. Inc.*, 837 F.3d 1299, 1314 (Fed. Cir. 2016) (reversing the district court's finding of invalidity). The '636 patent does exactly that by claiming improvements over both a manual process for generating assertions and a computer-implemented process for generating assertions. Specifically, claim 1 is directed to a physical system that, among other things, generates design data of a circuit specification and generates a property to verify the specification by reading the design data:

a specification inputting unit that generates design data or specifications and a document for confirming a specification of the semiconductor integrated circuit by graphically editing the specification of the semiconductor integrated circuit based on user operations ... [and] a property generating unit that generates a property which verifies the specification of the semiconductor integrated circuit by reading the design data generated by the specification inputting unit from the first storing unit and using the read design data;

The claimed system can subsequently convert the properties into assertions that will verify the properties. '636 patent, 4:48-59, 13:32-44.

By reading the design data to generate properties that verify the specification, the invention results in a double-improvement over conventional techniques for creating assertions, which could not assure that the assertions would match the circuit specification. '636 patent, 4:29-31. With the conventional technique of manually writing assertions directly from the circuit specification, the '636 patent observes that a designer has no way of confirming that the assertion description matches the circuit specification prior to performing simulation testing. *Id.* at 3:54-60. And while conventional automated techniques sought to improve upon manual creation of assertions, they too fail to ensure that the assertion descriptions match the design specification because they generate assertions from the RTL representation of the circuit, not the design specification. *Id.* at 4:4-31. Thus, the '636 patent describes and claims a specific computer-implemented improvement over those prior techniques for creating assertions, namely, a property generating unit that ensures that the assertions are created from properties generated from the circuit design specification data. As such, the system of claim 1 satisfies the test set forth in *McRO* for determining if the automation of a human process (creating assertions) is patent-eligible. Claims such as those at issue here that are

1 directed to the improvement of computing technology are routinely found to be concrete inventions,
 2 and not abstract ideas. *See, e.g., Enfish*, 822 F.3d at 1338. Like the invention in *Enfish*, and as
 3 discussed above, the '636 claims are directed to “a specific improvement to the way computers
 4 operate” and “improv[ing] an existing technological process,” which is not an abstract idea. *Enfish*,
 5 822 F.3d at 1335-36 (quoting *Alice Corp. Pty. v. CLS Bank Int'l*, 134 S. Ct. 2347, 2358-59 (2014)).

6 In *CardioNet*, yet another case with a similar holding, the Federal Circuit examined claims
 7 directed to a device for detecting and reporting the presence of atrial fibrillation or atrial flutter in
 8 a patient, in which the device can “more accurately distinguish atrial fibrillation and atrial flutter
 9 from other types of arrhythmias and has ‘improved positive predictability’ of atrial fibrillation and
 10 atrial flutter.” *CardioNet, LLC v. InfoBionic, Inc.*, 955 F.3d 1358, 1366 (Fed. Cir. 2020). The
 11 Federal Circuit explained that “[n]othing in the record in this case suggests that the claims merely
 12 computerize pre-existing techniques for diagnosing atrial fibrillation and atrial flutter.” *Id.* at 1370.
 13 Furthermore, “the written description [] confirm[ed] that the asserted claims [were] directed to a
 14 specific technological improvement – an improved medical device that achieves speedier, more
 15 accurate, and clinically significant detection of two specific medical conditions out of a host of
 16 possible heart conditions.” Similarly, here, the asserted claims are directed to a “specific
 17 technological improvement” – an improved design tool that “relates to a technology that executes
 18 circuit verification of an LSI (large scale integration)” in which the system “solve[s] the problems
 19 in the conventional technologies, for example, to enable high reliability and high efficiency in
 20 assertion verification for an LSI.” '636 patent, 1:8-9, 4:35-38, claim 8.

21 Cadence incorrectly suggests that the “assertion generating step” is the only point of novelty
 22 in claim 8, and that the '636 patent “admit[s] the other limitations of claim 8 were known in the
 23 art.” Mot. at 10. First, Cadence improperly conflates the *Alice* inquiry under § 101 with an
 24 anticipation/obviousness inquiry under § 102 or § 103. *Fitbit*, 233 F. Supp. 3d at 812. At step 1, the
 25 proper question is not whether individual elements were known in the art. It is whether the claimed
 26 invention, when considered as a whole, is directed to an abstract idea, or whether it is directed to
 27 something else (*e.g.*, a specific improvement to technology). *Enfish*, 822 F.3d at 1335 (“the
 28 ‘directed to’ inquiry applies a stage-one filter to claims, considered in light of the specification,

1 based on whether ‘their character as a whole is directed to excluded subject matter.’”). Instead,
 2 Cadence dissects the claim into individual elements, then declares all but a single element to be
 3 known in the prior art. But the reason the ’636 patent discusses the prior art is to explain why their
 4 approaches are ineffective, and how the ’636 invention improves LSI circuit verification
 5 technology to enable more efficient and accurate design of semiconductor circuits. The
 6 improvement is not simply automating what could be done by hand, but rather establishing a new
 7 framework to enable the efficient generation of accurate assertions for LSI circuit designs. ’636
 8 patent, 2:31, Berg at ¶57. The specification inputting and property generating steps are also distinct
 9 from the background prior art. ’636 patent, 1:46-54; Berg at ¶¶60-65.

10 Cadence argues that “[t]his is nothing more than using a computer to perform a translation
 11 that the patent specification admits was performed manually in the prior art” and “[u]sing a
 12 computer to automate a manual process is abstract”. Mot. at 10-11. As previously explained, the
 13 ’636 patent provides a new technological framework that enables a computer to generate properties
 14 for assertion, then convert them into assertion descriptions. Using this framework, chip designers
 15 can create high level designs and later rely on assertion verification to ensure that the synthesized
 16 RTL accurately captures the desired behavior of the chip design. Berg at ¶60. This is a technological
 17 improvement over what was once done manually. The claim does not simply use computers to
 18 make a manual process faster. *Id.* ¶61. For example, claim 8 recites a computer program that
 19 performs a number of steps, including (1) “a specification inputting step that generates design data
 20 of the semiconductor integrated circuit by graphically editing a specification of the semiconductor
 21 integrated circuit based on user operations...,” (2) “a property generating step that reads the design
 22 data generated at the specification inputting step from the storage and generates a property which
 23 verifies the specification of the semiconductor integrated circuit using the read design data...,” and
 24 (3) “an assertion generating step that reads the property generated at the property generating step
 25 from the storage and automatically converts the property into an assertion description if the property
 26 is to be verified during assertion verification...” Performed as a sequence, claim 8 enables a circuit
 27 designer to graphically edit the design data to generate properties and assertions on the fly, which
 28 provides a technological benefit to a circuit designer. *Id.* ¶53. Moreover, the ’636 patent enables

1 the computer program to accurately determine properties for verification, something that the '636
 2 patent states was not previously possible. *Id.* ¶63. A computer would not know what to do with a
 3 circuit specification, nor would an RTL simulator be able to derive properties or assertions from
 4 the specification. *Id.*

5 Cadence cites to *Int'l Bus. Machines Corp. v. Zillow Grp., Inc.*, 50 F.4th 1371, 1381-82
 6 (Fed. Cir. 2022) for the proposition that “automat[ing] ‘pen and paper methodologies’ to conserve
 7 human resources and minimize errors” is abstract. But in *Zillow*, the claims were directed to
 8 distinguishing between the various displayed layers [which] “could be accomplished using colored
 9 pencils and translucent paper.” *Id.* With the '636 patent, the claimed improvement breaks barriers
 10 to allow computers to generate assertions for verification of LSI designs. Berg at ¶57. *See SRI Int'l,*
 11 *Inc. v. Cisco Sys., Inc.*, 930 F.3d 1295, 1304 (Fed. Cir. 2019) (“the claims here are not directed to
 12 ... automating a conventional idea on a computer [but] [r]ather [] the technical functioning of the
 13 computer and computer networks by reciting a specific technique for improving computer network
 14 security”). This is an improvement to technology, not simply automating a manual process. '636
 15 patent, 2:31; Berg at ¶57.

16 Cadence further cites to *Synopsys*, 839 F.3d at 1147, where “the method can be performed
 17 mentally or with pencil and paper.” But claim 8 cannot be performed mentally or with pencil and
 18 paper. It is directed to a computer-readable medium upon which a program is stored that performs
 19 several steps. Claim 8 recites the framework from which the computer program can generate
 20 properties from a circuit specification, and automatically convert those properties to assertion
 21 descriptions. This is a fundamentally technological approach that is not comparable to either the
 22 manual process claimed in *Synopsys*, or the manual process to write assertions distinguished in the
 23 '636 patent. Notably, in *Synopsys*, the court declined to “decide whether a computer-implemented
 24 version of the invention would not be ‘directed to’ an abstract idea.” *Id.* at 1149. Cadence also cites
 25 to *Univ. of Fla. Rsch. Found., Inc. v. Gen. Elec. Co.*, 916 F.3d 1363, 1367 (Fed. Cir. 2019) for the
 26 proposition that automating “pen and paper methodologies” to conserve human resources and
 27 minimize errors is abstract. But the '636 patent claims a framework by which a computer program
 28 can determine which properties of a circuit design should be verified, and automatically converts

those properties into assertions. Without this technological framework, a computer could not even begin to replicate the manual process of writing assertions. Berg at ¶63. Nor is the '636 patent simply taking an abstract idea and “limiting the invention to a particular field of use or technological environment.” Mot. at 14. The '636 patent specifically improves circuit verification technology to allow computers to generate the assertions from circuit specifications. Cadence is dismissive of the claim language “computer readable medium encoded with a program” as a “generic use of computers.” *Id.* But all inferences must be drawn in favor of Plaintiff. Plaintiff has stated that this language gives life and meaning to the subsequent claim steps and enables assertion verification technology to be carried out by computers, instead of having to resort to an error-prone manual process. Berg at ¶¶59-69. Cadence argues that “[f]unctional claiming that attempts to cover an end goal has long been held invalid under §101 ...” Mot. at 14. But as described above, claim 8 sets forth a technological framework by which computers can generate assertions to verify a circuit design.

Regarding Cadence’s next argument, claim 8 does not preempt all manners of assertion-based verification of circuit designs. Mot. at 14. First, claim 8 improves upon several prior art approaches, which would not be covered by the claim. '636 patent, 3:43-50, 3:55-60, 3:61-4:31; Berg at ¶¶49-52. The claim includes narrowing limitations that require a computer program to perform the assertion verification; limitation 8[a] which requires graphical editing of a specification of a semiconductor integrated circuit; limitation 8[b] which requires the program to read the design data and generate a property for verification; limitation 8[c] which requires the program to automatically convert the property into an assertion description; and limitation 8[d] which further limits the nature of the property to “a selection condition with respect to a state transition, a logic value of at least one or more signals, or at least one or more signals in the design data.” *Id.* ¶59. Claim 8 is narrowly tailored and avoids concerns about preclusion.

b) At Step 2, the '636 Claims Plausibly Include Inventive Concepts

The '636 specification explains the problems associated with existing approaches for verification of LSI circuit designs, such as manual input of assertions and generating assertions from RTL and proffers a new technological solution to avoid such problems. '636 patent, 3:43-50,

3:55-60, 3:61-4:31; Berg at ¶¶49-52. The ordered combination of elements recited in claim 8, as described above, enables a computer program to perform assertion verification of an LSI circuit design. This avoids an inefficient and error-prone manual process, and avoids issues associated with RTL (as opposed to circuit specification) derived assertions. *Id.* ¶69. The claimed invention is nonconventional based on the pleading record because the '636 specification enables functionality that was not previously available. *Id.* ¶¶63, 68-69. *See Cellspin Soft, Inc. v. Fitbit, Inc.*, 927 F.3d 1306, 1317-18 (Fed. Cir. 2019) (overruling granting of motions to dismiss where “Cellspin made specific, plausible factual allegations about why aspects of its claimed inventions were not conventional,” and “[t]he district court erred by not accepting those allegations as true”).

In *Aatrix*, the Federal Circuit found that an amended complaint contained sufficient allegations that a claim directed to a data file that “allow[s] data to be imported into the viewable electronic form from outside applications” contained an inventive concept. *Aatrix*, 882 F.3d at 1127. The complaint alleged that the invention was an improvement over the prior art because it “allowed data to be imported from an end user application without needing to know proprietary database schemas and without having to custom program the form files to work with each outside application.” *Id.* It also alleged that the invention “eliminat[ed] the need for hand typing in the values and eliminating the risk of transcription error.” *Id.* The amended complaint also described “the development and success of the claimed data file despite the difficulty in obtaining data from other software vendors given proprietary data structures.” *Id.* “These allegations about the claimed data file claim that the data file is directed to an improvement in importing data from third-party software applications.” *Id.*

As in *Aatrix*, the FAC includes similar allegations with respect to the '636 patent. The '636 patent defines a framework with which a circuit designer can automatically and efficiently derive assertions from a circuit specification that are later used by an EDA tool to verify an RTL description. FAC at ¶¶23-32. The FAC includes descriptions about why the '636 patent improves upon prior art, such as the inefficient and error-prone manual process, to generate assertions. The '636 patent recites similar benefits as found in *Aatrix*. '636 patent, 12:50-13:10 (*e.g.*, asserting that (1) automatically generating properties from the circuit specification (2) ensures the specification

1 matches the assertions, (3) reduces the amount of work to debug the assertion, (4) prevents missing
 2 a test of a corner case); *see also* Berg at ¶¶60-69. The circuit specification can also be dynamically
 3 modified, resulting in the ability to update properties and assertions on-the-fly. *Id.* ¶68. As such,
 4 the FAC and the '636 patent plausibly show that claim 8 is directed to an unconventional approach
 5 for generating assertions, which constitutes an inventive concept.

6 Rather than accept the statements in the FAC and the '636 patent about improving upon
 7 existing LSI verification approaches using a new technological framework for generating
 8 assertions, Cadence argues that “beyond the abstract idea, its other limitations were routine,
 9 conventional, and admitted by the patent specification as being known in the art.” Mot. at 15.
 10 Cadence again conflates patent eligibility with novelty. *Fitbit*, 233 F. Supp. 3d at 812.

11 Cadence fails to give credit to the fact that claim 8 is directed to a “computer readable
 12 medium encoded with a program for causing a computer provided in an assertion generating
 13 system, that is capable of generating an assertion description for assertion verification of a
 14 semiconductor integrated circuit” that performs each of the steps recited in the claim. Mot. at 5.
 15 Claim 8 recites the framework that enables a computer to generate assertions quickly and efficiently
 16 from a circuit specification.

17 Importantly, Cadence errs in arguing that Limitation 8[b] was known in the prior art (“a
 18 property generating step that reads the design data generated at the specification inputting step from
 19 the storage and generates a property which verifies the specification of the semiconductor
 20 integrated circuit using the read design data and inputs the property in the storage”). Mot. at 6.
 21 Cadence’s reliance on the '636 patent at 1:46-54 is misplaced - it only describes a “property with
 22 respect to circuit specifications” at a high level in the context of manual input of assertions.
 23 *CosmoKey Sols. GmbH & Co. KG v. Duo Sec. LLC*, 15 F.4th 1091, 1098 (Fed. Cir. 2021) (“The
 24 district court’s reliance on column 1, lines 15-53 as allegedly admitting that these steps were routine
 25 or conventional is misplaced. While column 1, lines 30-46 describes three prior art references, none
 26 teach the recited claim steps.”). At 2:31-36, the '636 patent describes a set of exemplary properties
 27 that the circuit designer would have had to derive from the circuit specification based on knowledge
 28 of how the circuit was supposed to work. At 2:37-52, the '636 patent describes the assertions that

1 the circuit designer would manually input based on the properties to verify that the circuit behaves
 2 as intended. At 3:43-53, the '636 patent explains why such a manual approach to writing assertions
 3 is disadvantageous. The '636 patent *does not disclose or even suggest that in the prior art such*
 4 *properties existed separate and apart from the circuit specification or assertions*, nor does it
 5 suggest that a prior art computer program could perform the step in 8[b]. Berg at ¶63. The '636
 6 patent never states that the prior art incorporated any properties separate from what a circuit
 7 designer thought of based on design intent. *Id.* ¶62. As such, the ability to read properties from a
 8 circuit specification for purposes of automatically generating assertions was not known or
 9 conventional, especially when it was performed by a computer program stored on a computer-
 10 readable medium. *Id.* ¶63.

11 Limitation 8[c] is directed toward the “assertion generating step” that reads the property
 12 from Limitation 8[b] and automatically converts it to an assertion description. When considered
 13 together with Limitations 8[a] and 8[b], Limitation 8[c] provides an improvement to the
 14 conventional manual process where a designer considers a circuit design, thinks of test cases, and
 15 writes assertions to ensure those test cases perform as expected. Instead, claim 8 provides a
 16 technological process by which assertions can be automatically generated from properties extracted
 17 from a circuit specification. In doing so, the computerized process of claim 8 avoids mistakes and
 18 reduces the inefficiency of prior art approaches. Berg at ¶69. It enables computers to intelligently
 19 perform the bulk of the work in generating assertions for circuit design verification. *Id.*

20 Cadence argues that “[t]he ordering of those steps also fails to provide any inventive concept
 21 because they are in the natural and logical order for carrying out the abstract idea ...” Mot. at 16.
 22 Cadence’s argument relies on unsupported inferences it makes in its own favor, which violates the
 23 Rule 12(b) standard. Claim 8 recites the same steps discussed in the '636 specification, and the
 24 specification explains how the performance of these steps avoids problems associated with the prior
 25 art. *See, e.g.,* '636 patent, 3:43-60, 4:3-19, 4:35-44, 5:30-56; 12:50-13:10. Cadence’s dismissal of
 26 the claim steps as “natural and logical” simply cannot be true given the numerous benefits of the
 27 claimed approach over the prior art. Berg at ¶69. Cadence also argues that “claim 8 is not directed
 28 to any novel component or improvement in the way computers operate” and the “claims neither

1 seek to solve any technological problems arising in the realm of computers or computer networks
 2 nor offer any unconventional technological solutions.” Mot. at 16. This is untrue because as
 3 described above, claim 8 improves LSI semiconductor verification technology by providing a
 4 framework for generating assertions from a circuit specification. There is nothing in the record to
 5 show that such a framework is well-understood or routine. *Aatrix*, 882 F.3d at 1129.

6 Cadence also argues that the “alleged advantages are not found in the claim language.” Mot.
 7 at 17. But this is not required. *Cellspin*, 927 F.3d at 1317 (“[a]s long as what makes the claims
 8 inventive is recited by the claims, the specification need not expressly list all the reasons why this
 9 claimed structure is unconventional”); *Berkheimer v. HP Inc.*, 881 F.3d 1360, 1370 (Fed. Cir. 2018)
 10 (“These claims recite a specific method of archiving that, according to the specification, provides
 11 benefits that improve computer functionality”). Cadence argues “[r]eliability’ and ‘efficiency’ due
 12 to performing a process on a computer do not elevate an abstract idea to an inventive concept.”
 13 Mot. at 17. The benefits of claim 8 are not limited to “reliability and efficiency,” because claim 8
 14 introduces a technological framework that enables computers to produce accurate assertions and
 15 overcomes inefficiencies and errors in the prior art. FAC at ¶¶27-32.

16 3. The FAC Includes Plausible Allegations that the ’167 Claims Are Patent 17 Eligible

18 a) At Step 1, the ’167 Claims Are Not Abstract

19 As discussed above, an invention that automates tasks previously performed by humans is
 20 patent eligible if directed to a specific improvement over the prior process. Claim 1 of the ’167
 21 patent is directed to a specific technological improvement to a large-scale integration (LSI)
 22 semiconductor design support device. At the time of the ’167 patent, LSI circuits included
 23 thousands, and sometimes millions, of transistors. ’167 patent, 1:26-27; Berg at ¶12. Rather than
 24 design circuits at the transistor level, digital circuit designers use computer tools to design circuits
 25 at higher levels of abstraction, *e.g.*, a behavioral level. FAC at ¶35; ’167 patent, 1:33-35; Berg at
 26 ¶¶16-17.

27 A behavioral synthesis tool can later be used to generate a register transfer level (RTL)
 28 description. FAC at ¶35; ’167 patent, 1:34-39; Berg at ¶18. The RTL can be analyzed using a

1 simulator to check for latency, but the '167 patent states that there is no effective way to determine
 2 which portions of the corresponding behavioral description is associated with the latency
 3 measurement. FAC at ¶36; '167 patent, 1:56-62; Berg at ¶72. As such, the '167 patent proposes a
 4 specific improvement that allows a circuit designer to determine the latency associated with specific
 5 portions of a behavioral description. At the heart of claim 1 is a “latency analyzer” to check the
 6 latency based on an RTL simulation and a “correspondence table generator” that maps blocks in
 7 the behavioral description to states in the RTL description. FAC at ¶37; Berg at ¶77. Together, the
 8 latency analyzer can determine the latency of behavioral blocks that are associated with states in
 9 the RTL description. FAC at ¶37; Berg at ¶78. As a result, circuit designers have greater insight
 10 into the delays caused by their behavioral designs, and they can easily focus their efforts on
 11 improving the high-latency portions of their designs. *Id.* Cadence asserts without any support that
 12 “[b]eyond the correspondence table limitations, the '167 patent admits the other limitations of claim
 13 1 were known in the art” (Mot. at 8), but the '167 patent does not state this anywhere. This specific
 14 improvement over the prior art described in the '167 patent is patentable under Federal Circuit law.
 15 In *Packet Intel. LLC v. NetScout Sys., Inc.*, 965 F.3d 1299, 1308 (Fed. Cir. 2020), the Federal Circuit
 16 found claims directed to network monitors to be non-abstract improvements to technology by
 17 looking at how the claimed invention improved upon prior art network monitors:

18 According to the district court, prior art monitors could not identify disjointed
 19 connection flows as belonging to the same conversational flow, but ***the claimed***
 20 ***invention could provide a granular, nuanced, and useful classification of network***
 21 ***traffic***. The court found that the metrics made possible by the recited invention
 22 improved quality and performance of traffic flows. Specifically, ***the monitors had***
 23 ***an improved ability to classify and diagnose network congestion*** while providing
 24 increased network visibility to identify intrusions and malicious attacks.

25 (emphasis added). The Federal Circuit ultimately found that such benefits over the prior art
 26 demonstrated that the focus of the claims is a specific improvement in computer technology:

27 The specifications explain that known network monitors were unable to identify
 28 disjointed connection flows to each other, and ***the focus of the claims is a specific***
 29 ***improvement in computer technology: a more granular, nuanced, and useful***
 30 ***classification of network traffic***.

31 *Id.* at 1309-10 (emphasis added).

The ability to provide “a granular, nuanced, and useful classification of network traffic” in
 the *Packet Intelligence* claims is analogous to the improvement recited in the '167 claims. Prior art

1 latency analyzers could not determine latency with respect to any blocks of a behavioral
2 description, *i.e.*, a designer would have to manually review the behavioral description to locate
3 blocks associated with high latency. But the '167 invention now provides “granular, nuanced, and
4 useful” latency information such that the designer can pinpoint the specific blocks of the behavioral
5 description associated with high latency. The '167 patent claims an improvement to semiconductor
6 design support tools in the same way that the *Packet Intelligence* claims are directed to
7 improvements to computer technology.

8 In *Enfish*, the Federal Circuit found claims directed to a “self-referential table for a
9 computer database” to be non-abstract as “a specific implementation of a solution to a problem in
10 the software arts.” *Enfish*, 822 F.3d at 1337, 1339. The court gave significant weight to the fact that
11 “[t]he specification also teaches that the self-referential table functions differently than
12 conventional database structures.” *Id.* at 1337. As discussed above, the '167 patent provides a
13 specific implementation for a semiconductor design support device to allow a circuit designer to
14 pinpoint specific blocks in the behavioral description that are associated with high latency.

15 Cadence argues that “claim 1 is directed to the abstract idea of saving a cross-reference
16 table” and that “[s]aving this table of cross-references [] is the alleged point of novelty in the '167
17 patent.” Mot. at 18-19. Cadence’s analysis is flawed. At step 1, “the ‘directed to’ inquiry applies a
18 stage-one filter to claims, considered in light of the specification, ***based on whether ‘their
19 character as a whole is directed to excluded subject matter’.***” *Enfish*, 822 F.3d at 1335 (emphasis
20 added). Cadence improperly eliminates elements it claims were known in the prior art and then says
21 the claim must be directed to what is left over. Moreover, the purpose of the correspondence table
22 is not simply to save information, but rather to overcome limitations with prior art latency analysis
23 that could not determine the latency associated with specific blocks in the behavioral description.
24 See *id.* at 1337, 1339 (rejecting characterization of claims as “storing, organizing, and retrieving
25 memory in a logical table” and instead finding them directed to “a specific implementation of a
26 solution to a problem in the software arts”).

27 On page 19, Cadence improperly relies on statements made by the Examiner (*i.e.*, the
28 Examiner’s mental impressions) during the prosecution of the application leading to the '167 patent

1 as true, accepted facts as to what was known in the prior art. “The inquiry in a motion to dismiss is
 2 typically confined to the contents of the complaint and the plain words of the patent that is
 3 incorporated by reference.” *Broadcom Corp. v. Netflix Inc.*, 598 F. Supp. 3d 800, 805 (N.D. Cal.
 4 2022); *see also Contour IP Holding, LLC v. GoPro, Inc.*, No. 3:17-CV-04738-WHO, 2021 WL
 5 4148651, at *8-9 (N.D. Cal. Sept. 13, 2021) (“At this posture, I may only look at the pleadings,
 6 things incorporated into the pleadings, and matters subject to judicial notice” and “GoPro’s
 7 argument that it can slap the label ‘judicial notice’ on extra-pleadings positions is incorrect.”).

8 Cadence then dismisses the “correspondence table” as “no different than an engineer writing
 9 a table in a notebook for later reference” or “the table of contents in this brief.” Mot. at 19. But
 10 Cadence divorces this claim element from the claim. The correspondence table generator works in
 11 conjunction with the latency analyzer to calculate the latency associated with individual blocks in
 12 the behavioral description. Together, these elements improve the semiconductor design support
 13 device by allowing it to provide more granular latency calculations for blocks in the behavioral
 14 description. Berg at ¶84. Regardless of Cadence’s unsupported attorney argument, this process
 15 cannot be performed by hand, but rather requires using specialized EDA software. Berg at ¶¶21-
 16 25. Cadence cites three cases – *CyberSource*, *Twilio*, and *OpenTV* – but they are distinguishable
 17 because the claims at issue here are directed to specific improvements to technology.

18 The ’167 patent is directed to a specific technological improvement of a large-scale
 19 integration (LSI) semiconductor design support device. Prior to the ’167 patent, LSI circuits
 20 contained thousands, sometimes even millions, of transistors. ’167 patent, 1:26-27; Berg at ¶12.
 21 The ’167 patent offers an improvement that allows a circuit designer to determine the latency
 22 associated with portions of a behavioral description. The ’167 patent claims a “latency analyzer”
 23 that checks the latency based on an RTL simulation and a “correspondence table generator” that
 24 maps blocks in the behavioral description to parts in the RTL description. FAC at ¶37; Berg at ¶77.
 25 In tandem, the latency analyzer can determine the latency of behavioral blocks that are associated
 26 with states in the RTL description. FAC at ¶37; Berg at ¶78. The practical effect of this specific
 27 improvement is that circuit designers now have greater insight into the delays caused by the
 28

1 behavioral designs. In turn, these circuit designers can efficiently direct their attention and efforts
2 to improving the high-latency portions of the designs. *Id.*

3 Cadence also cites *Synopsys* for the proposition that “the Federal Circuit found claims
4 directed to logic (RTL) synthesis to be unpatentable under § 101.” Mot. at 19-20. The ’167 patent
5 does not purport to invent logic synthesis. ’167 patent, 1:36-40. Instead, it solves a related problem
6 because RTL simulation cannot ascertain latency for particular blocks in the behavioral description.
7 Berg at ¶72. Claim 1 sets forth an improved semiconductor design support device that allows circuit
8 designers to have greater insight into the hardware implementation of their designs and how it
9 performs relative to the corresponding behavioral description. Berg at ¶79. Cadence cites to *Intell.*
10 *Ventures I LLC v. Erie Indem. Co.*, for the proposition that “creating an index and using that index
11 to search for and retrieve data” is an abstract idea. 850 F.3d 1315, 1327 (Fed. Cir. 2017), Mot. at
12 20. Cadence ignores the unconventional combination of the latency analyzer and correspondence
13 table generator, the technological improvement offered by the combination where latency can be
14 calculated at the level of individual blocks in the behavioral description. The same distinction
15 applies to the other cases cited by Cadence relating to “collecting data” (*Content Extraction &*
16 *Trans. v. Wells Fargo Bank*, 776 F.3d 1343, 1347 (Fed. Cir. 2014)), “gathering and analyzing
17 information” (*Electric Power Grp. LLC v. Alstom SA*, 830 F.3d 1350, 1354 (Fed. Cir. 2016)), and
18 “track[ing] ... user identity” (*Intell. Ventures I LLC v. Capital One Bank (USA), N.A.*, 792 F.3d
19 1363, 1367 (Fed. Cir. 2015)).

20 Cadence asserts that “alleged efficiency gains cannot save claim 1.” Mot. at 20. But claim
21 1 does not realize efficiency gains by simply using a computer, as in *Zillow*. Instead, Claim 1
22 provides a specific solution in the form of a latency analyzer that works with the correspondence
23 table generator to determine latency of specific blocks in the behavioral description. This is a new
24 technological construct that improves semiconductor design support devices.

25 **b) At Step 2, the ’167 Claims Plausibly Include Inventive Concepts**

26 Specific, plausible factual allegations about why aspects of the claimed inventions were not
27 conventional can satisfy step 2 of *Alice*. The ’167 patent describes problems with the prior approach
28 to identifying behavioral blocks associated with high latency in an RTL description. The latency of

the RTL description can be determined via a logic simulation, but the designer describes the circuit at the behavioral level, which is not aware of clock cycles. As such, the designer cannot effectively pinpoint the portions of the behavioral description that cause high latency in the synthesized RTL description. FAC at ¶36; Berg at ¶72. The ordered combination of elements in claim 1 provides an unconventional approach by “calculat[ing] a latency in each block representing an operation in a predetermined unit in the behavioral description,” and this ability is enabled by a “correspondence table generator” that generates a “correspondence table in which each block in the behavioral description corresponds to a state in the RTL description.” FAC at ¶¶37, 40, 84, 88; Berg at ¶¶72-75, 84. *See Cellspin*, 927 F.3d at 1317-18 (overruling grant of motions to dismiss where “Cellspin made specific, plausible factual allegations about why aspects of its claimed inventions were not conventional,” and “[t]he district court erred by not accepting those allegations as true”). As such, claim 1 overcomes problems associated with known approaches in an unconventional manner.

In *Amdocs (Israel) Ltd. v. Openet Telecom, Inc.*, 841 F.3d 1288, 1300 (Fed. Cir. 2016), the Federal Circuit found that a claim that “entails an unconventional technological solution (enhancing data in a distributed fashion) to a technological problem (massive record flows which previously required massive databases)” contained an inventive concept. “The solution requires arguably generic components, including network devices and ‘gatherers’ which ‘gather’ information. However, the claim’s enhancing limitation necessarily requires that these generic components operate in an unconventional manner to achieve an improvement in computer functionality.” *Id.* at 1300-01. The ’167 patent recites a “latency analyzer” and a “correspondence table generator.” Even assuming *arguendo* that these elements are “generic components,” the FAC plausibly alleges that they work together in an unconventional way to provide a circuit designer with greater insight into the latency associated with blocks in the behavioral description. FAC at ¶40. This is like *Amdocs* where “the network devices and gatherers ... [are] working together in a distributed manner”. 841 F.3d at 1301. The benefits from the inventions are also similar, *i.e.*, in *Amdocs*, the data is enhanced by combining data from different sources, and in the ’167 patent, the circuit designer is provided greater insight into the latency performance of a circuit design at the behavioral level. *Id.*; FAC at ¶40.

For Step 2, Cadence again focuses on the “correspondence table,” arguing that “claim 1 does not mention any particular way of generating the correspondence table.” Mot. at 21. Cadence ignores the ordered combination of elements that overcome issues in debugging behavioral descriptions of circuit designs. In dismissing the “latency analyzer” as known in the prior art, Cadence fails to address the combination of the “latency analyzer” and “correspondence table generator” in its Step 2 analysis, and this failure should be fatal to its motion. *Fitbit*, 233 F. Supp. 3d at 813 (“the fact that tapping appears in the prior art does not prevent it from supplying an inventive concept here”). A “particular way of generating the correspondence table” (Mot. at 21) is not required to satisfy Step 2 as the combination of the “latency analyzer” and “correspondence table generator” enables a new functionality, *i.e.*, granular calculations of latency that correspond to specific blocks in a behavioral description, and thereby supplies an inventive concept. *Bascom Glob. Internet Servs., Inc. v. AT&T Mobility LLC*, 827 F.3d 1341, 1350 (Fed. Cir. 2016) (“an inventive concept can be found in the non-conventional and non-generic arrangement of known, conventional pieces”). Still, the ’167 patent explains how the correspondence table is generated (*e.g.*, 4:1-38), and describes how the latency analyzer refers to the correspondence table to obtain latency calculations associated with individual blocks of the behavioral description (*e.g.*, 4:39-5:3, 5:54-64.)

Cadence cites *Rearden*, but here, the ’167 claims are not merely directed to the result (*i.e.*, the capability of calculating latency pertaining to specific blocks of a behavioral description), and specifically claims the mechanism that enables the result (*i.e.*, the combination of the latency analyzer and the correspondence table generator). See *Rearden LLC v. TWDC Enter. 18 Corp.*, No. 22-cv-02464, 2023 WL 3579324 at *8 (N.D. Cal. Feb. 21, 2023), Mot. at 21.

Cadence then alleges that “[c]laim 1 does not recite a specific, much less novel or technical, way for generating or saving the correspondence table.” Mot. at 21. Cadence’s unnatural focus on the correspondence table results from its flawed analysis at Step 1 (failing to consider the character of the claims as a whole). The specific, novel, and technical approach in the claims, *i.e.*, the combination of the latency analyzer and correspondence table generator, enables the circuit designer to check the latency performance of specific blocks in the behavioral description.

1 Cadence then accuses SDT of “attempt[ing] to save the ’167 patent by rewriting it” and
 2 alleges that ¶36 of the FAC is contradicted by statements in the specification. Mot. at 22. This is
 3 untrue. The Background of the Invention section at col. 1, lines 48-62 clearly states the deficiencies
 4 in the prior art, including that the prior art latency analysis was performed on the RTL and “known
 5 methods may not check the behavioral description effectively.” Cadence then declares in its own
 6 favor that “[d]etermining the portions of behavioral code that corresponded to particular (high
 7 latency) portions of the RTL description was a simple matter of referring to the correspondence
 8 table—a simple mental task of reading a table ...” Mot. at 22. Even assuming a table was made
 9 available to a circuit designer along with the overall latency of the RTL, the designer would not be
 10 able to determine which portions of the behavioral description are associated with high latency.
 11 There is no evidence that a designer could do so, and finding as such requires much more than self-
 12 serving attorney argument from Cadence’s own attorneys.

13 Cadence argues that “[s]aving a table so that it can be referred to later is a conventional
 14 human activity that predates computers.” Mot. at 22. Cadence misses the mark for two reasons.
 15 First, its reliance on “human activity” at Step 2 is misplaced. *California Inst. of Tech. v. Hughes*
 16 *Comm’ns Inc.*, 59 F. Supp. 3d 974, 995 (C.D. Cal. 2014) (“The Court should not ask whether a
 17 human can calculate parity bit values using pencil and paper. Instead, the Court must ask whether
 18 the formula in claim 1 constitutes an inventive concept that sufficiently limits the claim’s
 19 preemptive effect.”). Cadence argues “linking an abstract idea to a particular technological
 20 environment [] does not provide an inventive concept.” Mot. at 22. Again, Cadence focuses on the
 21 “correspondence table” element and disregards the ordered combination of elements that improves
 22 upon prior art approaches to analyzing the latency in circuits. Cadence next argues “[e]ven in
 23 combination, the elements of claim 1 amount to no more than a routine and conventional use of a
 24 cross-reference table in a conventional IC design methodology...” Mot. at 23. The ordered
 25 combination enables a designer to gain unprecedented insight into the latency caused by individual
 26 blocks of a behavioral description, which otherwise does not recognize the concept of clock cycles
 27 and time. FAC at ¶¶35-37; Berg at ¶¶72, 78. The FAC explains how the combination overcomes
 28 problems in the prior art, and as such cannot be considered conventional when all facts are

1 construed in SDT’s favor. Cadence incorrectly argues that “[c]laim 1 is not directed to any novel
2 component or improvement in the way computers operate” and “[t]here is no mention of
3 improvements to computer components or EDA tools in the patent specification or claims.” Mot.
4 at 23. As discussed above, claim 1 is directed to an improved semiconductor design support tool,
5 which is an EDA tool that enables designers to have greater insight into latency performance
6 associated with blocks in the behavioral description. FAC at ¶¶35-37; Berg at ¶¶72, 78.

7 Cadence cites to *Elec. Power* to argue that “[c]laim 1 is not directed to any novel component
8 or improvement in the way computers operate.” Mot. at 23. Cadence improperly draws inferences
9 in its own favor. The claimed “latency analyzer” is novel because it can provide latency information
10 pertaining to particular blocks of a behavioral description by working in conjunction with a
11 correspondence table generator. This was not possible in the prior art. *See* ’167 patent, 1:48-62.

12 Cadence attempts to distinguish the “self-referential table” of *Enfish*. But *Enfish* only
13 addressed Step 1. *Enfish*, 822 F.3d at 1339 (“Because the claims are not directed to an abstract idea
14 under step one of the *Alice* analysis, we do not need to proceed to step two of that analysis.”). That
15 said, the “latency analyzer” and “correspondence table generator” of claim 1 of the ’167 patent are
16 analogous to the self-referential table of *Enfish* in that they improve the way latency information
17 for individual blocks in a behavioral description can be ascertained. The latency analyzer is
18 improved such that it can reference the correspondence table to generate latency calculations at the
19 block level, whereas before it could not. *Id.* at 1337 (“our conclusion that the claims are directed to
20 an improvement of an existing technology is bolstered by the specification’s teachings that the
21 claimed invention achieves other benefits over conventional databases, such as increased
22 flexibility, faster search times, and smaller memory requirements”). The latency analyzer coupled
23 with the correspondence table improves upon conventional latency analysis that could not calculate
24 latency associated with individual blocks of a behavioral description. FAC at ¶40.

25 **V. CONCLUSION**

26 In view of the foregoing, the Court should deny Cadence’s motion.
27
28

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