

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

CADENCE DESIGN SYSTEMS, INC.,

Petitioner,

v.

SEMICONDUCTOR DESIGN TECHNOLOGIES, LLC,

Patent Owner.

IPR2024-00024

U.S. Patent No. 7,971,167

**PETITIONER’S REPLY TO PATENT OWNER’S PRELIMINARY
RESPONSE**

Exhibit 1006 (“Shin”) was publicly available.

Acceleration Bay did not categorically exclude all technical reports (“TR”) as prior art. Rather, *Acceleration Bay* analyzed different facts from those presented here. “Whether a reference is publicly accessible is determined on a case-by-case basis based on the facts and circumstances surrounding the reference[.]....”

VidStream LLC v. Twitter, Inc., 981 F.3d 1060, 1065 (Fed. Cir. 2020) (cleaned up).

In *Acceleration Bay*, the declarant was a system administrator for a general website that hosted TRs for the entire UC San Diego computer science/engineering department. 908 F.3d at 772-73. In contrast, this Petition relied on a declaration by one of Shin’s authors, Dr. Dömer, who explained he was part of a prominent research group at a different school, UC Irvine. The group was “well-known across the academic field and EDA industry” and was led by a pioneer in behavioral synthesis, Dr. Gajski. Pet. 17; Ex-1010, ¶¶3-4, 17. Shin was published on that research group’s website and the professors’ webpages. Ex-1010, ¶¶8, 10, 13-14, 17. Dr. Dömer explained how “[i]t is common for professors to include their publications on their webpages, so that others in the field can locate publications of interest” and how the interested public “would have been able to locate TR 03-42 [Shin] with ease.” *Id.*, ¶¶17, 11, 16; Pet. 17.

Indeed, Courts frequently find public accessibility based on the prominence of the authors or publication forum. For example, art was publicly accessible in *M*

& K Holdings v. Samsung Elecs. Co., where interested users were drawn to an expert group’s website “given its prominence.” 985 F.3d 1376, 1381 (Fed. Cir. 2021). Art was publicly accessible in *Voter Verified, Inc. v. Premier Election Sols., Inc.*, where a POSITA “would have been independently aware of the [website] as a prominent forum for discussing such technologies[.]” 698 F.3d 1374, 1380-1381 (Fed. Cir. 2012). In *Du Pont*, the court relied on the author’s “reputation” “as a pioneer in the field” to conclude a research grant proposal qualified as a printed publication. *E.I. Du Pont de Nemours & Co. v. Cetus Corp.*, 1990 WL 305551, *10 n.7 (N.D. Cal. Dec. 3, 1990). SDT never addressed this testimony from Dr. Dömer, which stands as un rebutted evidence that a POSITA would have sought and found Shin as a Gajski lab publication. Ex-1011, 00005-6. As Dr. Lin explained, “[a]ny person interested in behavioral synthesis would have looked to publications from Dr. Gajski’s lab because of its prominent role in the field.” Ex-1003, ¶51; Pet. 17.

As the Federal Circuit held, “a website’s landing page is not required to have search functionality.” *M & K Holdings*, 935 F.3d at 1381. Search was central in *Acceleration Bay* because the TR was among “potentially hundreds of titles in the same year, with most containing unrelated subject matter...*when the authors were not particularly well known.*” 908 F.3d at 773 (emphasis added). Because the authors were not well known, a POSITA would have had to rely on the search function to discover the reference—therefore, it mattered that the search

“functionality was not reliable.” *Id.* That is not the case here, where Shin was from prominent authors and was but one of 44 papers—the very first publication listed on that research group’s webpage for 2003. Ex-1011, 00005-6. A POSITA could have readily located Shin, exercising reasonable diligence; no more is required.

Shin was, in fact, accessed by the public: the Internet Archive found and archived both the CECS TR page and Shin. Pet. 17; Ex-1003, ¶51 n.3; Ex-1011.

SDT’s implied construction of “RTL” is contrary to the ’167 patent.

SDT argues that “RTL” should include the structures from a background reference D’angelo. POPR, 30. Not so. The ’167 patent states that RTL description means “*RTL (register transfer level)* description.” Ex-1001, 1:36-39 (emphasis added). It describes hardware at the *level* of “register and clock” operations (*id.*, 1:43-45, 2:3-31; Pet. 35 n.4, 10-11) and the “data flow” between registers in a “state machine” (Ex-1001, 4:32-38, 5:11-17). As Dr. Lin explained, “‘RTL’ ... mean[s] it describe[s] the transfer of signals between hardware registers, synchronized to the IC’s clock signal.” Ex-1003, ¶4; Ex-1021; Ex-1018; Pet. 6.

Harada teaches a description of hardware at the register-transfer level. Pet. 34-35. Harada’s simulation model describes hardware, including the data flow between registers in a logic circuit design. Pet. 34; Ex-1004, Fig. 7 (“Reg_A,” “Reg_B,” “Reg_C,” “Reg_o1”), ¶2, ¶99 (describing “the state transition of multiple register resources” and “data path control”). Harada teaches that its

“simulation model generation unit”

includes “the HDL (Hardware Description Language) generation function.” *Id.*, ¶¶99. Figure 5 shows the circuit design described by

FIG. 5

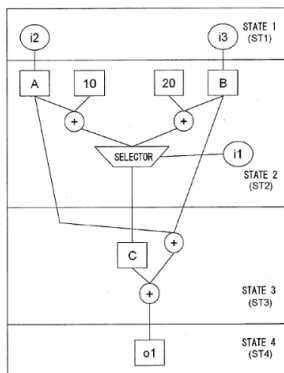


FIG. 7

```
1: #define CM_CHANGE_APPEND(pos)
2: {CysimChangeList[CysimChangeTableMax++] = pos;}
3: in ter(0:1) i1, i2, i3;
4: out reg(0:1) o1;
5: switch (STATE){
6: case ST1:
7:   Reg_A = i1; Reg_B = i3;
8:   CM_CHANGE_APPEND(0);
9:   STATE = ST2;
10:  break;
11: case ST2:
12:   if (i1 != 0){
13:     CM_CHANGE_APPEND(1);
14:     Reg_C = Reg_A + 10;
15:   }
16:   else {
17:     CM_CHANGE_APPEND(2);
18:     Reg_C = Reg_B + 20;
19:   }
20:   STATE = ST3;
21:  break;
22: case ST3:
23:   Reg_o1 = Reg_A + Reg_B + Reg_C;
24:   CM_CHANGE_APPEND(3);
25:   STATE = ST4;
26:  break;
27: case ST4:
28:   o1 = Reg_o1;
29:   CM_CHANGE_APPEND(4);
30:   STATE = ST1;
31:  break;
32: } end switch;
```

Figure 7, including the connections and data flow between hardware registers, adders, and selectors in

RTL states 1-4 which correspond to clock cycles 1-4. Pet. 34; Ex-1004, ¶102. SDT concedes that Harada generates HDL but attempts to sidestep this teaching with the incredulous assertion that “the HDL is an output that is produced, and not used further...” POPR, 31.

As the '167 patent admits, the output of behavioral synthesis was RTL, which was used for logic simulation. *Id.*, 1:36-55; Pet. 11. Harada starts with a “hardware description” at the behavioral level (Pet. 30-31; Ex-1004, ¶2, ¶97); the simulation model is the output of behavioral synthesis: it is “generated from the behavior level description...through behavioral synthesis” and used for clock cycle accurate logic simulation. Ex-1004, ¶¶104, 1-2, 98, 117; Pet. 34-35, 37-38. RTL was known in the art for clock cycle simulations. Ex-1003, ¶¶15-18; Pet. 9-10.

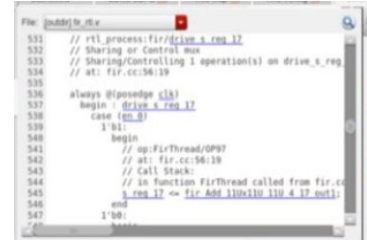
SDT’s implied construction also excludes RTL “expressed in software” code. POPR, 30-32. SDT asserts that Harada’s simulation model is “written in the

C language” and therefore “includes no hardware.”

POPR, 30. However, register-transfer level specifies a

level of description, not any particular language. While a

hardware description may superficially resemble software



Ex-1017, 00013 (excerpt).

code, it is RTL if it describes hardware at the register-transfer level. Moreover,

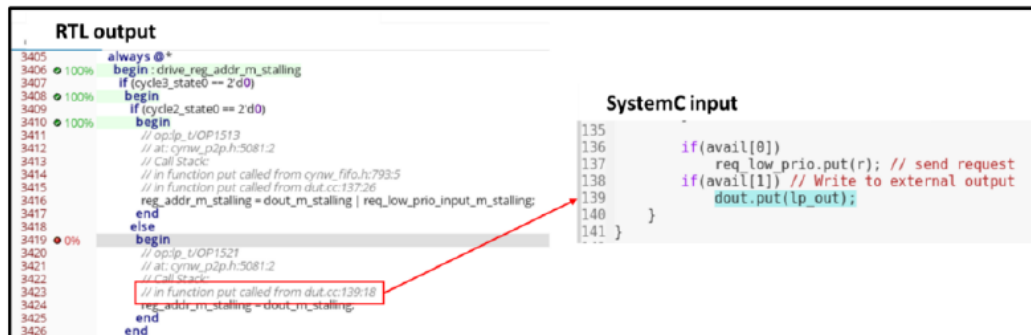
SDT argues that Harada’s simulation model is software because it “includes a

‘switch’ statement.” POPR, 30. But in district court, SDT alleged that RTL was

satisfied by code that includes a case statement and labeled switches. Ex-1017,

00013. SDT further alleged that RTL was satisfied by code that, like Harada,

include if-else statements and assignments of values to registers. Ex-1017, 00015:



Moreover, Grounds 1-2 combined Harada with Gutberlet and Shin, which

SDT did not dispute teaches RTL output from behavioral synthesis. Pet. 35-37; Ex-

1003, ¶¶131-142. The *combination* teaches “using logic simulation on RTL code”

to calculate latency in clock cycles. Ex-1003, ¶¶163, 92, 96; Pet. 48-49, 25-28.

In summary, “RTL” simply means “register transfer level,” and Harada, Gutberlet, and Shin all teach this.

Respectfully submitted,

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CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. § 42.24(d), the undersigned certifies that the foregoing **PETITIONER'S REPLY TO PATENT OWNER'S PRELIMINARY REPLY**, exclusive of the exempted portions as provided in 37 C.F.R. § 42.24(a), contains no more than 1105 words and 5 pages and therefore complies with the Board's order granting briefing by e-mail on February 21, 2024.

February 29, 2024

/s/ Harper Batts
Harper Batts

CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6(e), the undersigned certifies that on February 29, 2024, a complete and entire copy of the foregoing **PETITIONER’S REPLY TO PATENT OWNER’S PRELIMINARY RESPONSE**, including exhibits and testimony relied upon, was filed with the PTAB through its E2E system and served via email on attorneys of record for Semiconductor Design Technologies, LLC at the following address:

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