

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

CADENCE DESIGN SYSTEMS, INC.,
Petitioner,

v.

SEMICONDUCTOR DESIGN TECHNOLOGIES, LLC,
Patent Owner.

IPR2024-00024
Patent 7,791,167 B2

Before ST. JOHN COURTENAY, III, GREGG I. ANDERSON, and
NATHAN A. ENGELS, *Administrative Patent Judges*.

ENGELS, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. §314

I. INTRODUCTION

Cadence Design Systems, Inc. (“Petitioner”) filed a Petition (Paper 2 (“Pet.”)), seeking *inter partes* review of claims 1–4 (the “challenged claims”) of U.S. Patent No. 7,971,167 B2 (Ex. 1001 (“the ’167 patent”)). See Pet. 1. Semiconductor Design Technologies, Inc. (“Patent Owner”) filed a Preliminary Response (Paper 6 (“Prelim. Resp.”)). With authorization from the Board, Petitioner filed a Reply to Patent Owner’s Preliminary Response (Paper 7 (“Prelim. Reply”)), and Patent Owner filed a Sur-Reply in Support of Patent Owner’s Preliminary Response (Paper 8 (“Prelim. Sur-Reply”)).

Institution of an *inter partes* review is authorized by statute when “the information presented in the petition . . . and any response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a); see 37 C.F.R. § 42.108. Upon consideration of the evidence currently of record, we conclude that the information presented shows that there is a reasonable likelihood that Petitioner would prevail in establishing the unpatentability of at least one challenged claim of the ’167 patent.

A. Related Matters

The parties indicate that the ’167 patent is the subject of Civil Action *Semiconductor Design Technologies, LLC v. Cadence Design Systems, Inc.*, No. 3:23-cv-01001 (N.D. Cal.), filed March 6, 2023. Pet. 92; Paper 4, 1.

B. Real Parties in Interest

Petitioner identifies Cadence Design Systems, Inc. as the real party-in-interest. Pet. 92. Patent Owner identifies Semiconductor Design Technologies, LLC as the real party-in-interest. Paper 4, 1.

C. The '167 Patent (Ex. 1001)

The '167 patent, titled “Semiconductor Design Support Device, Semiconductor Design Support Method, and Manufacturing Method for Semiconductor Integrated Circuit,” relates to systems and methods for designing a semiconductor integrated circuit. Ex. 1001, codes [54], [57]. Among other things, the '167 patent states that a behavioral synthesis tool is an example of electronic design automation (“EDA”) and a “behavioral synthesis tool generates an RTL (register transfer level) description from a behavioral description for describing an operation of hardware.” Ex. 1001, 1:37–39. “The behavioral description describes an algorithm of processing to be executed by the hardware directly in a motion level, and does not recognize a concept of clock cycles.” Ex. 1001, 1:40–43. “When the behavioral synthesis tool generates the RTL description, a latency in the RTL description needs to be checked. The latency denotes a total number of clock cycles needed to complete processing for total input data.” Ex. 1001, 1:48–51. Further, “the behavioral description is checked to determine which part of the behavioral description consumes a great number of clock cycles (e.g., which part of the behavioral description has a great latency)” (Ex. 1001, 1:58–62), and “[t]he latency analyzer is configured to analyze a result of a logic simulation performed on the RTL description to calculate a latency in each block representing an operation in a predetermined unit in the behavioral description.” Ex. 1001, 2:9-12.

D. Challenged Claims

Petitioner challenges claims 1–4 of the '167 patent. Pet. 14–15. Claims 1 and 3 are independent claims. Independent claim 1 is illustrative of the challenged claims and is reproduced below with Petitioner's labeling added.

1[pre]. A semiconductor design support device for designing a semiconductor integrated circuit, the device comprising:

[1a] a behavioral description configured to describe an algorithm of processing performed by hardware in a motion level;

[1b] an RTL description generated by reading the behavioral description, the RTL description configured to recognize a concept including register and clock synchronism particular to the hardware;

[1c] a latency analyzer configured to analyze a result of a logic simulation performed on the RTL description to calculate a latency in each block representing an operation in a predetermined unit in the behavioral description;

[1d] a correspondence table in which each block in the behavioral description corresponds to a state in the RTL description; and

[1e] a correspondence table generator configured to generate the correspondence table.

E. The Alleged Grounds of Unpatentability

Petitioner asserts the following grounds of unpatentability (Pet. 2):

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1, 2	103	Harada, ¹ Gutberlet ²
1, 2	103	Harada, Gutberlet, Shin ³
1, 2	103	Ezaki, ⁴ Gutberlet, Shin
3, 4	103	Harada, Gutberlet, Rittman ⁵
3, 4	103	Harada, Gutberlet, Shin, Rittman
3, 4	103	Ezaki, Gutberlet, Shin, Rittman

In addition, Petitioner relies on the Declaration of Bill Lin, Ph.D.
Ex. 1003.

II. ANALYSIS

A. Legal Standards

Petitioner bears the burden to demonstrate unpatentability, and that burden never shifts to Patent Owner. *Dynamic Drinkware, LLC v. Nat’l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015).

A claim is unpatentable for obviousness if “the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.” 35 U.S.C. § 103; *see also KSR Int’l Co. v. Teleflex Inc.*,

¹ US 2006/0069538 A1; published March 30, 2006. Ex. 1004.

² WO 2005/119528 A2; published Dec. 15, 2005. Ex. 1005.

³ Dongwan Shin et al., C-based Interactive RTL Design Methodology, Tech. Report CECS-03-42, Center for Embedded Comp. Sci., U. of Cal., Irvine (Dec. 2003). Ex. 1006.

⁴ US 2006/0225022 A1; published Oct. 5, 2006. Ex. 1007.

⁵ US 2002/0152453 A1; Oct. 17, 2002. Ex. 1008.

550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) when in evidence, objective evidence of nonobviousness.⁶ *Graham v. John Deere Co. of Kan. City*, 383 U.S. 1, 17–18 (1966).

B. Level of Ordinary Skill in the Art

Petitioner asserts that a person of ordinary skill in the art “would have had a bachelor’s degree in electrical engineering or a similar field with at least two years of experience in the field; or a master’s degree with specialization in the field,” and “[a] person with less education but more relevant practical experience may also meet this standard.” Pet. 21 (citing Ex. 1003 ¶¶ 63–64). Petitioner also states that the relevant field is “IC design and manufacturing, including EDA tools and behavioral synthesis.” Pet. 21 (citing Ex. 1001, 1:17–2:37; Ex. 1003 ¶ 62).

At this stage, Patent Owner does not address the level of ordinary skill. For the purposes of this Decision, we apply Petitioner’s articulation of the level of ordinary skill, which is supported by the testimony of Dr. Lin and is consistent with the level reflected by the ’167 patent and the asserted prior art.

⁶ The parties have not directed our attention to any objective evidence of obviousness or non-obviousness.

C. Claim Construction

We apply the same claim construction standard used in district court actions under 35 U.S.C. § 282(b), namely that articulated in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). See 37 C.F.R. § 42.100(b) (2021). In applying that standard, claim terms generally are given their ordinary and customary meaning as would have been understood by a person of ordinary skill in the art at the time of the invention and in the context of the entire patent disclosure. *Phillips*, 415 F.3d at 1312–13. “In determining the meaning of the disputed claim limitation, we look principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the prosecution history, if in evidence.” *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1014 (Fed. Cir. 2006) (citing *Phillips*, 415 F.3d at 1312–17).

Petitioner proposes constructions of the claim terms “block,” “motion level,” and “latency analyzer.” Pet. 22–23. Patent Owner contends the Petition fails even under Petitioner’s proposed constructions and that no constructions are necessary. Prelim. Resp. 16.

For purposes of this Decision, we determine that no aspects of the challenged claims require explicit construction. See, e.g., *Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) (“The Board is required to construe ‘only those terms . . . that are in controversy, and only to the extent necessary to resolve the controversy.’” (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

D. Alleged Obviousness of Claims 1 and 2 View of Harada and Gutberlet

Petitioner provides a limitation-by-limitation comparison of each of

claims 1 and 2 to the teachings of Harada and Gutberlet. Pet. 13–50. We address Petitioner’s contentions regarding claim 1 as illustrative.

1. *Independent Claim 1*

- a. *1[pre]. A semiconductor design support device for designing a semiconductor integrated circuit, the device comprising:*

Petitioner does not address whether the preamble is a limitation, but Petitioner contends Harada and Gutberlet teach a semiconductor design support device. Pet. 29–30.

At this stage, Petitioner’s showings are unrebutted and are adequate for the preamble.

- b. *[1a] a behavioral description configured to describe an algorithm of processing performed by hardware in a motion level;*

Petitioner contends that Harada teaches “a behavioral description configured to describe an algorithm of processing performed by hardware (e.g., logic circuit) in a motion (behavioral) level.” Pet. 30. Petitioner contends Harada’s source file is a “behavioral level description (algorithm description) as the hardware description.” Pet. 30–31 (quoting Ex. 1004 ¶¶ 2, 14 (emphasis omitted)).

Petitioner also contends that Gutberlet’s source code is a behavioral description of an integrated circuit. Pet. 32–33. Further, Petitioner contends “[t]he ‘behavior or functionality’ is described with high-level behavioral languages and is configured to describe IC algorithms in a motion (behavior) level.” Pet. 32 (citing Ex. 1005, 1:16–27, 5:33–6:17; Ex. 1003 ¶¶ 122–123). Petitioner also contends Gutberlet’s source code examples describe behavior using C language and “do not have to account for physical hardware details such as registers and clock cycles.” Pet. 32–33 (citing Ex. 1003 ¶¶ 124,

125).

To the extent that Patent Owner’s arguments address this limitation, we address those arguments below.

- c. [1b] an RTL description generated by reading the behavioral description, the RTL description configured to recognize a concept including register and clock synchronism particular to the hardware;*

Petitioner contends Haranda teaches an RTL “simulation model” that is “generated through behavioral synthesis of a behavior model description composed of a plurality of lines, the simulation model including a finite state machine structure.” Pet. 34 (citing Ex. 1004 ¶¶ 21, 14–19, 40–43).

According to Petitioner, “Haranda’s simulation model is an RTL description because it is the output of the behavioral synthesis process and it describes the design at the register transfer level, including descriptions of registers of RTL states.” Pet. 34 (citing Ex. 1004 ¶¶ 14, 28, 97, 99, Figs. 5–7).

Petitioner also contends that Haranda’s RTL simulation models in Figures 7 and 11 show code at the register-transfer level, “including the flow of data to and from the particular registers for the hardware (‘Reg_A’-‘Reg_D’) and other particular hardware features such as input ports (‘in ter(0:1) i1, i2, i3, i4’) and output ports (‘out reg(o:1) o1’).” Pet. 34 (citing Ex. 1004, Figs. 7, 11; Ex. 1003 ¶ 130). Petitioner additionally cites Haranda’s teachings that “the ‘cycle-based simulator . . . executes clock-based simulation’” of the hardware using Haranda’s RTL description. Pet. 34–35 (quoting Ex. 1004 ¶ 117; citing Ex. 1004 ¶¶ 2, 98; Ex. 1003 ¶ 131).

Next, Petitioner contends Gutberlet teaches RTL code generated from source code describing behavior of an integrated circuit. Pet. 35 (citing

Ex. 1005 1:16–27, Fig. 1). According to Petitioner, “[t]o ‘generate RTL code’, Gutberlet’s ‘behavioral synthesis tool 104 reads in the source code file 102’ which contains the behavioral description.” Pet. 35 (citing Ex. 1005 5:33–6:17, 38:26–27, Fig. 3; Ex. 1003 ¶¶ 133–134) (internal quotation omitted).

To the extent that Patent Owner’s arguments address this limitation, we address those arguments below.

d. [1c] a latency analyzer configured to analyze a result of a logic simulation performed on the RTL description to calculate a latency in each block representing an operation in a predetermined unit in the behavioral description;

Petitioner contends Harada’s simulation monitor is a latency analyzer that is configured to analyze RTL logic simulation results to calculate latency in each block on a cycle basis. Pet. 37 (citing Ex. 1004 ¶ 98). Among other things, Petitioner states Harada teaches clock-based simulation on a simulation model generated through behavioral synthesis of a behavior model description composed of a plurality of lines and including a finite state machine structure. Pet. 37 (citing Ex. 1004 ¶¶ 21, 35; Ex. 1003 ¶ 142). Petitioner states that Harada teaches a latency analyzer that is configured to look at the results of a clock-cycle-based logic simulation and calculate latency by analyzing the number of executions for each block of behavioral code and that the calculation refers to the results of the logic simulation and the correspondence table. Pet. 38–40 (citing Ex. 1004 ¶¶ 26, 39, 76, 132, Figs. 10, 15–17; Ex. 1003 ¶¶ 145, 146).

According to Petitioner, the number of executions is a measure of latency indicative of the amount of time required during Harada’s clock-cycle simulation, which is one known way for calculating latency in clock

cycles over multiple iterations. Pet. 41–44 (citing Ex. 1004 ¶ 136, Figs. 4, 8, 10, 12, 16; Ex. 1014, 3; Ex. 1003 ¶ 149–151). Petitioner argues that converting to another metric, such as the clock cycles needed for each block to complete processing for the simulation’s input data (which Petitioner contends Gutberlet teaches) “would have been obvious because Harada already simulates each component for every clock cycle, for every circuit path. Thus, Harada’s simulation provides the necessary information and converting from one metric to another would have been a matter of simple arithmetic, e.g., by multiplying ratios.” Pet. 41 (citing Ex. 1003 ¶ 148).

Petitioner further contends Gutberlet provides complimentary teachings that reinforce Harada’s teachings “while expanding on the types of latency reported.” Pet. 46. Among other things, Petitioner contends Gutberlet simulates RTL code and verifies and analyzes the synthesis results. Pet. 46 (citing Ex. 1005, 6:3–7, 7:3–6, Fig. 3). According to Petitioner, Gutberlet teaches a framework that includes conventional RTL methodologies to simulate and design hardware and to analyze the performance of a circuit, including the latency of the circuit. Pet. 47–48.

Petitioner also contends a person of ordinary skill in the art would have found it obvious to combine the teachings by using clock-based logic simulation on RTL code to calculate latency for each block of behavioral code as Harada and Gutberlet teach and using that data to create a timing report with latency information in terms of clock cycles and delay, as taught by Gutberlet. Pet. 51.

Among other arguments, Patent Owner contends “Harada does not disclose generating an RTL description and thus it cannot disclose performing a logic simulation on RTL, or analyzing a result of such a

simulation to calculate latency.” Prelim. Resp. 29. Patent Owner states that “Harada’s simulation model does not include anything similar to Dr. Lin’s representative RTL description from Dangelo” and “Harada’s simulation model includes no hardware – it defines in software the states and the steps that occur in each state necessary to carry out the defined behavior.” Prelim. Resp. 30. Patent Owner argues: “Harada’s simulation model is not an RTL description based on the knowledge of one of ordinary skill in the art, as evidenced by statements from Petitioner’s own expert.” Prelim. Resp. 31. According to Patent Owner, “[a]t best, [Harada’s Hardware Description Language] HDL is an output that is produced, and not used further in the context of Harada.” Prelim. Resp. 31. Further, Patent Owner states that “[w]hile Harada appears to disclose counting the number of executions in each conditional branch of source code, this disclosure is different from the claimed latency analyzer that requires analyzing a result of a logic simulation performed on an RTL description.” Prelim. Resp. 32. Patent Owner also argues that “Harada does not disclose what input data is used for the simulation model, and according to the ’167 patent the latency cannot be ascertained before the RTL simulation” and “Harada discloses that each state is assumed to take one clock cycle. Prelim. Resp. 32–33 (citing Ex. 1004 ¶ 102.

Patent Owner also argues, *inter alia*, that “[w]hile Gutberlet purports to disclose in Tables 38 and 39 latency calculations associated with various loops in source code, these purported latency calculations are not determined by ‘analyzing a result of a logic simulation performed on the RTL description to calculate a latency,’ as required by the independent claims.” Prelim. Resp. 33. Patent Owner contends that as illustrated in Figure 3 of

Gutberlet, the RTL code is not generated until after the user has decided how to handle loops. Prelim. Resp. 33–34. Patent Owner states that “the ’167 patent notes that simply determining the number of clock cycles needed for processing in a block is insufficient to determine latency.” Prelim. Resp. 34–35 (citing Ex. 1001, 3:43–50, 3:52–62). According to Patent Owner, “[t]herefore, Latency and Duration shown in Tables 38 and 39 of Gutberlet are different than the claimed latency obtained from analyzing a result of logic simulations of an RTL description.” Prelim. Resp. 35. Patent Owner also argues “Gutberlet disparages the approach of first generating RTL code, and assessing latency and going back to modify the source code as ‘time consuming and inefficient.’” Prelim. Resp. 35–36 (quoting Ex. 1005, 2:17–18).

We note that Patent Owner’s arguments are not currently supported by declaration testimony and amount to attorney argument at this stage in the proceeding. Petitioner’s showings, on the other hand, include the testimony of Dr. Lin in addition to the cited portions of the references, and we thus preliminarily find Petitioner’s showings teach or suggest limitations 1[a], 1[b], and 1[c] for the purpose of deciding institution.

- e. [1d] a correspondence table in which each block in the behavioral description corresponds to a state in the RTL description; and*
- f. [1e] a correspondence table generator configured to generate the correspondence table.*

Petitioner contends that Harada’s simulation model generation unit generates a behavior level description source line branch ID correspondence table in which correspondence between branch IDs and source line numbers in the behavior level description is stored. Pet. 56, 62–63 (citing Ex. 1004

¶¶ 16–19, 32, 33, 42–43, 97, 99, Fig. 2; Ex. 1003 ¶¶ 190). Petitioner states that Harada includes exemplary correspondence tables in Figures 8 and 12 with each table including information on correspondences between a state number, state ID in the RTL description and a source line in the behavioral code. Pet. 56–57 (citing Ex. 1004 ¶¶ 99, 112, 181, Figs. 8, 12). According to Petitioner, each block of behavioral code in Harada’s Figure 4 is cited by line number in the correspondence table of Figure 8 aligned with a state in the RTL description. Pet. 57–58 (citing Ex. 1004 ¶ 113, Figs. 8, 10, 12).

Petitioner also contends that Gutberlet further teaches or suggests including information for each block of the behavioral description, suggesting a data structure for mapping back to behavioral code. Pet. 59 (citing Ex. 1005, 6:30–32; Ex. 1003 ¶ 184). Petitioner argues a person of ordinary skill in the art would have been motivated to apply Gutberlet’s teachings and include each block of the behavioral description in Harada’s correspondence table because Gutberlet teaches the advantages to allow a circuit designer to exercise complete or enhanced control over how a design is synthesized in hardware. Pet. 59 (citing Ex. 1005, 3:7–13). According to Petitioner, Gutberlet reinforces Harada’s teachings and would result in easier identification of information and facilitate the collection and presentation of other useful analysis results corresponding to each block. Pet. 59–60.

Patent Owner argues that “Harada does not disclose an RTL description either used to generate its simulation model or referenced by any of its correspondence tables” and “therefore does not disclose the claimed correspondence table that requires identification of ‘a state in the RTL description.’” Prelim. Resp. 38. Patent Owner also argues that Gutberlet’s reports identify process and loop information from the behavioral

description, not any portion of an RTL description. Prelim. Resp. 38–39 (citing Ex. 1005, Tables 38, 39). Patent Owner contends Gutberlet’s Figure 3 shows that its reports are generated prior to finalizing the circuit design and generating an RTL description and, “[a]s such, the reports do not reference any portion of an RTL description because the RTL description would not yet be generated at that time.” Prelim. Resp. 39.

We again note that Patent Owner’s arguments are not currently supported by declaration testimony and amount to attorney argument at this stage in the proceeding. Petitioner’s showings, on the other hand, include the testimony of Dr. Lin in addition to the cited portions of the references, and we thus preliminarily find Petitioner’s showings teach or suggest limitations 1[d] and 1[e] for the purpose of deciding institution.

g. Reasons to Combine

Petitioner argues a person of ordinary skill would have been motivated to combine the teachings of Harada and Gutberlet for several reasons, in addition to the reasons discussed above with the claim limitations. Pet. 24–29. Among other things, Petitioner contends Harada and Gutberlet share a similar purpose and architecture, “both teach behavioral synthesis of C code to RTL; both simulate RTL; and both report latency metrics for each behavioral block.” Pet. 24 (citing Ex. 1004 ¶¶ 1–2, 72–73, 98, Figs. 16, 17; Ex. 1005, 1:10–27, 2:11–19, 7:3–6, 34:13–20, Table 38). Further, Petitioner contends combining the references’ teachings would have amounted to combining prior art elements according to known methods to yield predictable results, with Harada teaching “a process including steps for synthesizing behavioral code into RTL; performing RTL logic simulation; and analyzing the results, along with a table showing

correspondence between RTL and behavioral code, to calculate latency for each behavioral block,” and Gutberlet teaching “using logic simulation to calculate latency for each behavioral block, measured in clock cycles/ns, and reported in a table.” Pet. 24–25 (citing Ex. 1004 ¶¶ 98, 117, 118, 132–134; Ex. 1005, 2:11–19, Table 38).

Patent Owner argues a person of ordinary skill in the art would not have combined Harada and Gutberlet as suggested in the Petition because, according to Patent Owner, among other things, “Harada does not disclose using RTL in the context of its disclosure” and “Gutberlet discloses loop handling techniques on behavioral code, and any performance assessment occurs prior to generating RTL.” Prelim. Resp. 40. Further, Patent Owner argues Gutberlet explicitly teaches away from generating RTL code, analyzing the latency, and re-editing the source code if there is a latency issue and “[t]herefore, a [person of ordinary skill in the art] would not combine Gutberlet with any reference to satisfy the latency analysis elements of the ’167 claims. Prelim. Resp. 41 (citing Ex. 1005, 2:11–19).

We again note that Patent Owner’s arguments are not currently supported by declaration testimony and amount to attorney argument at this stage in the proceeding. Petitioner’s arguments, on the other hand, are supported by the testimony of Dr. Lin in addition to the cited portions of the references, and we thus preliminarily find Petitioner has adequately articulated reasons for combining the references for the purposes of institution.

h. Conclusion For Claim 1

On the record before us for the reasons discussed above, we determine that Petitioner has demonstrated a reasonable likelihood of prevailing in its

challenge to claim 1 as being unpatentable in view of Harada and Gutberlet, and we institute *inter partes* review on all claims and all grounds asserted in the Petition. *See SAS Inst., Inc. v. Iancu*, 138 S. Ct. 1348, 1359–60 (2018); Consolidated Trial Practice Guide (Nov. 2019), 64.⁷

E. Shin's Status as Prior Art

The parties dispute whether Shin qualifies as a publicly accessible publication. According to Petitioner, prior to the critical date, Shin was published on the Internet by professors at the University of California at Irvine on both the University's website and on the professors' webpages. Pet. 17; Prelim. Reply 1–3. According to Petitioner, the authors were prominent and well-known in the industry, Shin was the very first publication listed on the relevant page of the University's website in 2003, and Shin was one of only 44 papers on that page. Prelim. Reply 1–3.

Patent Owner argues that Shin was not indexed or searchable in a meaningful way and that there is insufficient evidence that an interested person of ordinary skill exercising reasonable diligence would have located Shin. Prelim. Resp. 17–18, 21; Prelim. Sur-Reply 1–3. Patent Owner further argues the facts of Shin's alleged availability are similar to the facts of *Acceleration Bay, LLC v. Activision Blizzard Inc.*, 908 F.3d 765, 772–74 (Fed. Cir. 2018). Prelim. Resp. 19–21; Prelim. Sur-Reply 1–3.

At this preliminary stage, we question whether Petitioner has sufficiently shown that Shin qualifies as a publicly available publication.

III. CONCLUSION

Based on the current record, we determine Petitioner has shown a

⁷ Available at www.uspto.gov/sites/default/files/documents/tpgnov.pdf.

reasonable likelihood of prevailing with respect to at least one claim of the '167 patent. Accordingly, we institute *inter partes* review of all claims challenged on all of the grounds in the Petition.

IV. ORDER

Accordingly, it is:

ORDERED that pursuant to 35 U.S.C. § 314, an *inter partes* review is hereby instituted as to claims 1–4 of the '167 patent based on the unpatentability challenges presented in the Petition; and

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial commencing on the entry date of this decision.

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