

DRIVING MULTIPLE PARALLEL LEDS WITH REDUCED POWER SUPPLY RIPPLE

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5

FIELD OF THE INVENTION

This invention relates to a light emitting diode (LED) driver that drives LEDs in parallel.

BACKGROUND

10 LEDs are rapidly replacing incandescent bulbs, fluorescent bulbs, and other types of light sources due to their efficiency, small size, high reliability, and selectable color emission. A typical forward voltage drop for a high power LED is about 3-4 volts. The brightness of an LED is controlled by the current through the LED, which ranges from a few milliamps to an amp or more, depending on the type of LED. For this reason, LED drivers typically
15 include some means to control the LED current.

In applications where high brightness is needed, multiple LEDs are used. It is common to connect LEDs in series, since the current through all the LEDs in series will be the same. However, driving many LEDs in series requires relatively high voltages, since the driving voltage must be greater than the combined voltage drops of the series LEDs.
20 Additionally, when different types of LEDs are driven, such as different colors of LEDs, it may be desired to drive each type of LED with a different current. Therefore, in some applications, LEDs are connected in parallel, with the current through each parallel path being separately controlled. There may be only one LED in each parallel path, a few LEDs connected in series in each parallel path, or another configuration of LEDs in each parallel
25 path. In some cases, one parallel path may drive a single red LED, another parallel path may drive two or more green LEDs connected in series, and another parallel path may drive one or more blue LEDs, in order to achieve a target overall brightness and color. Parallel LEDs may also be used for redundancy in case one LED fails and becomes an open circuit.

Fig. 1A is a typical prior art LED driver 10 that drives multiple LEDs 12 in parallel.

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Some parallel paths show multiple LEDs connected in series. Most components of the driver 10 are formed on an integrated circuit chip. The LEDs are typically connected to pins extending from the chip package.

5 A DC voltage regulator controller 14 up converts or down converts an input voltage (Vin), depending on the required voltage to drive the LEDs 12. Typically, the voltage regulator is a switching regulator operating at a high frequency, such as 100KHz-5MHz, to keep component sizes small. The controller 14 switches a switching transistor at a certain pulse-width modulation (PWM) duty cycle to maintain an output voltage (Vout) at the desired level. The switching transistor and an output circuit are represented by block 16.
10 The output circuit comprises an inductor and diode (or synchronous rectifier) connected to the switching transistor to supply pulses of current to a smoothing capacitor 18. The topology of the output circuit determines whether the voltage regulator is a step up or step down regulator. Such regulators are well known and need not be described in detail.

The anodes of the “top” LEDs in each parallel path are connected to Vout, as shown
15 in Fig. 1A, and the cathodes of the “bottom” LEDs in each path are connected to designated pins of the driver 10. The current through each path is individually set, such as by the user connecting a current set resistor to corresponding pins of the driver 10. Other types of current setting circuits may be used. A current setting circuit 20-22 for each parallel path is shown, where each circuit 20-22 may comprise a current set resistor or a current regulator. It
20 is important to individually set the currents, since each parallel path may drive a different type (e.g., color) of LED that requires a different current to achieve the desired light output.

An LED’s color is slightly dependent on the magnitude of the forward current. Once the current is fixed, it should be not changed in order to avoid color shift. Therefore, to adjust the perceived brightness of the LEDs 12, a PWM brightness control unit 24 outputs a
25 PWM signal at a relatively low frequency (e.g., 100Hz-1000Hz) and effectively turns all the LEDs on and off at the LF PWM duty cycle. An externally generated dimming control signal sets the LF PWM duty cycle. For example, if the duty cycle were 50%, the average current would be half of the peak current when the LEDs are on. Thus, the perceived brightness of the LEDs would be about half the brightness of the LEDs when fully on.

30 Fig. 1B illustrates one type of brightness control unit 24. An N-Bit counter 26

cyclically counts, such as a repeating 5-bit count from 0-31, at a rate set by a clock. The binary count is applied to preset count detectors 28 and 30. Detector 28 detects a count that begins the high state of the PWM cycle, such as the count 00000. Upon count 00000 being detected, the detector 28 outputs a pulse. Detector 30 detects a count that begins the low state of the PWM cycle, such as 01010. Upon count 01010 being detected, the detector 30 outputs a pulse. The outputs of the detectors 28 and 30 are connected to the set and reset inputs, respectively, of an RS flip flop 32. The output of the flip flop 32 is the PWM brightness control signal, where the duty cycle in the example is approximately 30%.

The frequency of the LF PWM signal must be high enough to prevent noticeable flicker of the LEDs. There may be thousands of HF PWM pulses generated by the voltage regulator during each pulse (on-time) of the LF PWM signal. In this way, the current through the LEDs is either a “fixed” peak current or zero current. This keeps the emitted color of the LEDs constant, but enables the perceived brightness to be adjusted by the LF PWM duty cycle.

Since there are multiple parallel sets of LEDs, the combined currents of the paths can be high. For example, some LEDs may be driven at 1 Amp. When the brightness control PWM signal goes high, the voltage regulator must instantaneously supply driving current to all the LEDs at the same time. The large instantaneous change in the current causes a voltage ripple in the battery or other power supply. Greatly increasing the value of the smoothing capacitor 18 to smooth out the current drain on the power supply is not desirable, since such high value capacitors are relatively large and expensive. The ripple in the power supply due to the high currents being switched on and off causes noise that affects other circuits connected to the power supply. Since the PWM brightness control signal is at audio frequencies, the noise may even be audible.

What is needed is an LED driver that produces less ripple and noise compared to the conventional LED drivers.

SUMMARY

An LED driver is disclosed that drives LEDs connected in parallel paths. Each parallel path may include one LED, or LEDs connected in series, or LEDs connected in parallel, or LEDs connected in a combination of series and parallel.

Instead of applying current to all the parallel-paths at the same time, under control of a PWM brightness control signal, the application of current to each parallel path is staggered. This reduces ripple in the power supply, since the current provided by the power supply when the PWM signal goes high is not the sum of all the LED peak currents. In fact, at medium and low duty cycles, the currents can be staggered such that all the LEDs are never on at the same time.

One way of doing this is to circulate a binary representation of the PWM duty cycle, such as 11111000 (duty cycle=62.5%), in an 8-bit shift register. Any number of bits (e.g., 128) can be used to more finely control the duty cycle. The bits (11111000) are initially loaded into the shift register, such as by a parallel loading process, and the bits are shifted through the shift register by a clock. The bit shifted out of the last position in the shift register is fed back into the first position, so the bit pattern recirculates through the shift register. The PWM brightness control signals for each parallel path of LEDs are tapped from different positions along the shift register so that the PWM brightness control signals are identical but staggered. The spacing of the taps may be equal, random or shaped, depending on the number of parallel paths and the current drawn by each path. The spacing should be that required to minimize ripple in the power supply. In one example, if the duty cycle is low enough, no high state PWM signal overlaps another high state PWM signal.

In another embodiment, the PWM brightness control signal is continuously and serially read into the shift register at one end, and the bits are shifted through the shift register. The PWM brightness control signals for each parallel path of LEDs are tapped from different positions along the shift register so that the PWM brightness control signals are identical but staggered. In this embodiment, there is no feeding back of any bits in the shift register, and the shift register acts as a clocked tapped delay line.

Other circuits may be used to create the staggered PWM signals.

Although embodiments of the invention have been summarized above, the scope of the invention is defined by the claims.

BRIEF DESCRIPTION OF THE DRAWINGS

5 Fig. 1A illustrates a prior art LED driver, driving LEDs connected in different parallel paths.

Fig. 1B illustrates a prior art PWM brightness control signal generator.

Fig. 2A illustrates a tapped recirculating shift register used to stagger PWM brightness control signals to the LEDs in the different parallel paths, in accordance with one
10 embodiment of the invention.

Fig. 2B illustrates the staggering of the PWM brightness control signals.

Fig. 3 illustrates a tapped non-recirculating shift register used to stagger PWM brightness control signals to the LEDs in the different parallel paths, in accordance with another embodiment of the invention.

15 Fig. 4 illustrates an LED driver, driving LEDs connected in different parallel paths, using the staggered PWM brightness control signals, in accordance with one embodiment of the present invention.

Fig. 5 illustrates one type of current regulator for a single parallel path receiving a staggered PWM brightness control signal.

20 Fig. 6 illustrates one type of current set circuit for a single parallel path receiving a staggered PWM brightness control signal.

Elements that are the same or equivalent in the figures are identified with the same numeral.

DETAILED DESCRIPTION

The present invention is an LED driver that staggers PWM brightness control signals to different parallel paths. The LEDs in each path are switched on and off in accordance with the PWM duty cycle to create a certain perceived brightness level, but the paths are energized at different times. This results in the current sinks being spread out so that there is less ripple produced by the power supply. This reduces noise, eases the constraints on the power supply, improves the color output of the LEDs, reduces artifacts caused by lights flickering, and provides other benefits.

Fig. 2A illustrates an N-Bit shift register 40. The number of bits determines the fineness in selecting PWM brightness control signal duty cycles. In one embodiment, the duty cycle of the LEDs is set by a 7-bit word, which represents 128 possible duty cycles (approximately 0.8% change in brightness per step). This would require a 128 bit shift register. Any size bit word may be used in the invention, such as 2-12 bits. For simplicity, only a 3-bit duty cycle word will be used in the examples, corresponding to 8 possible duty cycles (including 0%), or a 12.5% brightness change per step.

A simple digital converter (not shown) may be used to convert the 3-bit word into a pattern of 1's and 0's corresponding to the high and low states of the PWM signal. In the example used in the figures, a duty cycle of 62.5% is set by the 3-bit word (011), and the converter converts this code into the bit pattern 11111000, representing that the PWM brightness control signal is high for five bit-clock cycles and low for three bit-clock cycles.

In Fig. 2A, the 8-bit shift register 40 is loaded with the 11111000 bit pattern in parallel. In another embodiment, the bit pattern is shifted into the shift register 40 as a serial stream. A shift clock is applied to the shift clock terminal of the register 40 to shift the bit pattern to the right for every shift clock cycle. The shift clock has a frequency of 8x the PWM frequency. The PWM frequency should be above 100Hz to avoid noticeable flicker in the LEDs. The bit shifted out of the last position in the shift register 40 is fed back into the first position, so the 8-bit pattern recirculates through the shift register 40.

The PWM brightness control signals for each parallel path of LEDs are tapped from different positions along the shift register 40 so that the PWM brightness control signals are

identical but staggered. The spacing of the taps may be equal, random, or shaped, depending on the number of parallel paths and the current drawn by each path. The spacing and order of the taps should be that required to minimize ripple in the power supply. In the example shown, there are three taps outputting the staggered PWM signals: PWM1, PWM2, and
5 PWM3. Each PWM signal will have the pattern 1111000, representing a 62.5% duty cycle. The taps may be in a different order, such as PWM1, PWM3, and PWM2.

Fig. 2B shows the staggering of the three PWM signals, where the pattern is repeated as long as the bit clock continues to shift the bits in the register 40. In other words, the PWM signals are out of phase with each other. In one example, if the duty cycle is low
10 enough, no high state PWM signal overlaps another high state PWM signal, so the maximum current supplied by the power supply is the highest current in any one LED path.

If the driver drives many parallel paths, some paths may be driven in phase and other paths driven out of phase.

As shown by the LED driver of Fig. 4, described in greater detail later, the staggered
15 PWM signals are applied to their corresponding current set circuit for each parallel path.

In another embodiment, shown in Fig. 3, the bits of the PWM brightness control signal bit pattern 1111000 are continuously and serially loaded into the first bit position of the shift register 46 and then shifted by the load/shift clock. In this embodiment, there is no feeding back of any bits in the shift register, and the shift register acts as a clocked tapped
20 delay line. The PWM brightness control signals (PWM1, PWM2, PWM3) for each parallel path of LEDs are tapped from different positions along the shift register 46 so that the PWM brightness control signals are identical but staggered, as shown in Fig. 2B.

Fig. 4 illustrates an LED driver 50. All circuitry, except for inductors, large capacitors, and the LEDs may be formed on the same integrated circuit. All elements shown
25 in Fig. 4, except the LEDs, may be within the same package, with pins for connection to the LEDs, power, and an external dimming control circuit.

One or more LEDs 12 may be connected in each parallel current path. If more than one LED is to be driven by a single parallel path, such LEDs may be connected in series, parallel, or a combination to achieve the desired brightness and forward voltage drop for the

path. There may be any number of parallel paths for driving LEDs, such as 2-10. Three paths are advantageous for controlling red, green, and blue LEDs to create a variety of colors.

The DC voltage regulator controller 52 may be a boost regulator controller, a buck regulator controller, or any other type of regulator controller needed to generate an output voltage (Vout) that exceeds the forward voltage drop for each parallel path of LEDs to turn the LEDs on. A conventional switching transistor and output circuit block 54 is shown. The voltage regulator controller 52 generates high frequency (e.g., 1 MHz) PWM signals that turn the switching transistor on and off, where the duty cycle controls the level of Vout. An inductor and diode (in block 54) connected to the switching transistor apply ramping currents to the smoothing capacitor 18, which supplies a relatively constant output voltage (Vout). The topology of the switching transistor, inductor, and diode contained in the block 54 determines whether the regulator is a step up or step down regulator. A step up regulator will typically be needed if many LEDs are connected in series. Examples of topologies for step up and step down regulators are found in Micrel's published data sheets for LED drivers and other products, and in US patent 7,307,614, assigned to Micrel, all incorporated herein by reference. The regulator portion may also use isolated components, such as in a flyback or forward converter.

All LED paths are energized with the same voltage but may draw different currents, set by the current set circuits 56, 57, and 58. The current set circuits 56-58 are effectively enabled and disabled by their associated staggered PWM brightness control signal PWM1, PWM2, or PWM3. There may be any number of current set circuits, each driven by a staggered PWM signal. The PWM brightness control unit 40/46 may be either of the shift registers 40 or 46 in Figs. 2A and 2B, or may be any other circuit that operates to stagger a PWM signal, such as a delay line.

Fig. 5 illustrates one current controller circuit 62 that may serve as each of the current set circuits 56-58 in Fig. 4. A low value sense resistor (Rsense) and MOSFET 64 are connected in series with the one or more LEDs 12 in a single parallel path of the driver 50. A feedback voltage (Vfb), proportional to the current through the LEDs, is applied to an inverting input of an op amp 66. The non-inverting input is coupled to a reference voltage (Vref). The op amp 66 controls the gate voltage of the MOSFET 64 to cause Vfb to equal Vref. The value of Rsense is selected to establish the peak current through the LEDs 12

when the MOSFET 64 is on. There may be a different Rsense value for each of the current set circuits 56-58 in Fig. 4. A pass transistor 68 is controlled to be on or off by the PWM brightness control signal. This turns the MOSFET 64 on at the PWM duty cycle. The transistors may be any type of suitable transistor.

5 Fig. 6 illustrates another type of current set circuit 70 that may serve as each of the current set circuits 56-58 in Fig. 4. A current set resistor Rset and MOSFET 72 are connected in series with the one or more LEDs 12 in a single parallel path of the driver 50. Since Vout is substantially constant, the value of Rset is selected to establish the peak current through the LEDs 12. There may be a different Rset value for each of the current set
10 circuits 56-58 in Fig. 4. The MOSFET 72 is controlled to be on or off by the PWM brightness control signal.

 In addition to there being less power supply output voltage ripple by staggering the on-times of the different parallel paths of LEDs, there is less overall flickering of the light, since there is a shorter time (or even no time) that all the LEDs are off at the same time,
15 compared to the prior art techniques. This is advantageous in certain situations and reduces eye fatigue.

 The various components may be coupled together by direct wiring, or via resistors, or via buffers, or via level shifters, or via inverters, or via other components in order to properly operate.

20 Having described the invention in detail, those skilled in the art will appreciate that, given the present disclosure, modifications may be made to the invention without departing from the spirit and inventive concepts described herein. Therefore, it is not intended that the scope of the invention be limited to the specific embodiments illustrated and described.

CLAIMS

What is claimed is:

1. A light emitting diode (LED) driver for driving LEDs connected to different
5 parallel paths, the driver comprising:

a voltage source for connection to first ends of LEDs in a plurality of parallel paths;

a plurality of current set circuits, one current set circuit per parallel path, each current set circuit controlling a peak current through one or more LEDs connected in
10 each parallel path; and

a pulse-width modulated (PWM) brightness control signal generator connected to the plurality of current set circuits, the brightness control signal generator being configured to generate staggered PWM brightness control signals to the plurality of current set circuits,

15 each current set circuit being configured to draw the peak current through its associated one or more LEDs at a duty cycle substantially corresponding to a duty cycle of a PWM brightness control signal applied to it, such that the plurality of current set circuits conduct current through their associated one or more LEDs at the same duty cycle but out of phase with each other.
- 20 2. The driver of Claim 1 wherein the voltage source is a step up voltage regulator.
3. The driver of Claim 1 wherein each current set circuit is a current regulator.
4. The driver of Claim 1 wherein each current set circuit is a current regulator
25 comprising:

a current control transistor in series with one or more LEDs in an associated parallel path; and

a feedback circuit connected to detect a current through the parallel path and connected to the current control transistor to control a conductivity of the current control transistor to cause the current through the parallel path to match a reference level.

5 5. The driver of Claim 4 wherein each current set circuit further comprises a PWM brightness control transistor connected between an output of the feedback circuit and a control terminal of the current control transistor, the PWM brightness control transistor being connected to the PWM brightness control signal generator for receiving a staggered PWM brightness control signal to couple the output of the feedback circuit to the control terminal
10 of the current control transistor at a duty cycle of the staggered PWM brightness control signal.

6. The driver of Claim 1 wherein each current set circuit comprises:

a current set resistor in series with one or more LEDs in an associated parallel path; and

15 a PWM brightness control transistor connected in series between the current set resistor and the one or more LEDs in an associated parallel path, the PWM brightness control transistor being connected to the PWM brightness control signal generator for receiving a staggered PWM brightness control signal.

7. The driver of Claim 1 wherein the PWM brightness control signal generator
20 comprises:

a shift register storing bits corresponding to a PWM duty cycle of a brightness control signal, the shift register having bit positions;

a clock connected to the shift register for shifting the bits along the shift register; and

25 taps off the shift register coupled to different bit positions of the shift register, each tap providing a different staggered PWM brightness control signal connected to an associated current set circuit.

8. The driver of Claim 7 wherein the shift register has a connection that connects an end bit position to a first bit position so that bits in the shift register are recirculated in the shift register.

5 9. The driver of Claim 7 wherein the bits corresponding to a PWM duty cycle of a brightness control signal are serially and continuously loaded into a first bit position of the shift register, then shifted by the clock.

10. The driver of Claim 7 wherein the clock shifts the bits at a rate equal to N times a frequency of the PWM brightness control signal, where N equals the number of bits representing a single PWM duty cycle.

10 11. The driver of Claim 1 wherein the plurality of parallel paths comprises at least three paths.

12. The driver of Claim 1 further comprising the LEDs connected to the driver.

14. The driver of Claim 1 wherein the driver is formed as an integrated circuit.

15 15. A method for driving light emitting diodes (LEDs) connected to different parallel paths, the method comprising:

supplying a voltage to first ends of LEDs in a plurality of parallel paths;

setting a peak current through one or more LEDs connected in each of the parallel paths, the peak current being set by a current set circuit for each parallel path;

20 generating staggered pulse width modulated (PWM) brightness control signals;

applying a different staggered PWM brightness control signals to each current set circuit; and

25 drawing the peak current through the one or more LEDs in each parallel path, set by its associated current set circuit, at a duty cycle corresponding to a duty cycle of an associated PWM brightness control signal, such that the parallel paths of LEDs conduct current at substantially the same duty cycle but out of phase with each other.

16. The method of Claim 15 further comprising varying the duty cycle of the staggered PWM brightness control signals to change an average current through the parallel paths of LEDs to change a perceived brightness of the LEDs.

17. The method of Claim 15 wherein setting a peak current through one or more LEDs connected in each of the parallel paths comprises setting the peak current by controlling conductivity of a current control transistor in series with each parallel path, and wherein applying a different staggered PWM brightness control signal to each current set circuit comprises:

coupling each staggered PWM brightness control signal to a control terminal of an associated pass transistor, each pass transistor being connected between a control terminal of a respective current control transistor and a regulating control voltage, such that the current control transistor is turned on and off corresponding to a duty cycle of the associated pass transistor.

18. The method of Claim 15 wherein applying a different staggered PWM brightness control signal to each current set circuit comprises applying each staggered PWM brightness control signals to an associated transistor connected in series with the one or more LEDs in an associated parallel path, such that the transistor is turned on and off corresponding to the duty cycle of the staggered PWM brightness control signal applied to it.

19. The method of Claim 15 wherein generating staggered PWM brightness control signals comprises:

storing bits corresponding to a PWM duty cycle of a brightness control signal in a shift register, the shift register having bit positions;

shifting the bits along the shift register under control of a clock; and

receiving bits tapped off the shift register at different bit positions of the shift register to generate a different staggered PWM brightness control signal from the bits at each of the different bit positions.

20. The method of Claim 19 further comprising recirculating bits in the shift register by feeding a bit at an output bit position to an input bit position along the shift register.

21. The method of Claim 19 further comprising serially and continuously loading
5 bits corresponding to a PWM duty cycle of a brightness control signal into a first bit position of the shift register, then shifting the bits by the clock.

22. The method of Claim 19 wherein the clock shifts the bits at a rate equal to N times a frequency of the PWM brightness control signal, where N equals the number of bits representing a single PWM duty cycle.

10 23. The method of Claim 15 wherein the plurality of parallel paths comprises at least three paths.

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5 ABSTRACT OF THE DISCLOSURE

An LED driver is disclosed that drives LEDs connected in parallel. Instead of applying current to all the parallel-connected LEDs at the same time, under control of a common PWM brightness control signal, the application of current to each parallel path is staggered by using staggered brightness control signals. The turning on of the LEDs in the
10 different parallel paths will have the same duty cycle but will be out of phase. This reduces ripple in the power supply by reducing the magnitude of the instantaneous current sink. In one embodiment, a shift register contains a binary representation of the PWM duty cycle, and a clock shifts the bits along the shift register. The PWM brightness control signals for each parallel path of LEDs are tapped from different positions along the shift register so that
15 the PWM brightness control signals are identical but staggered.

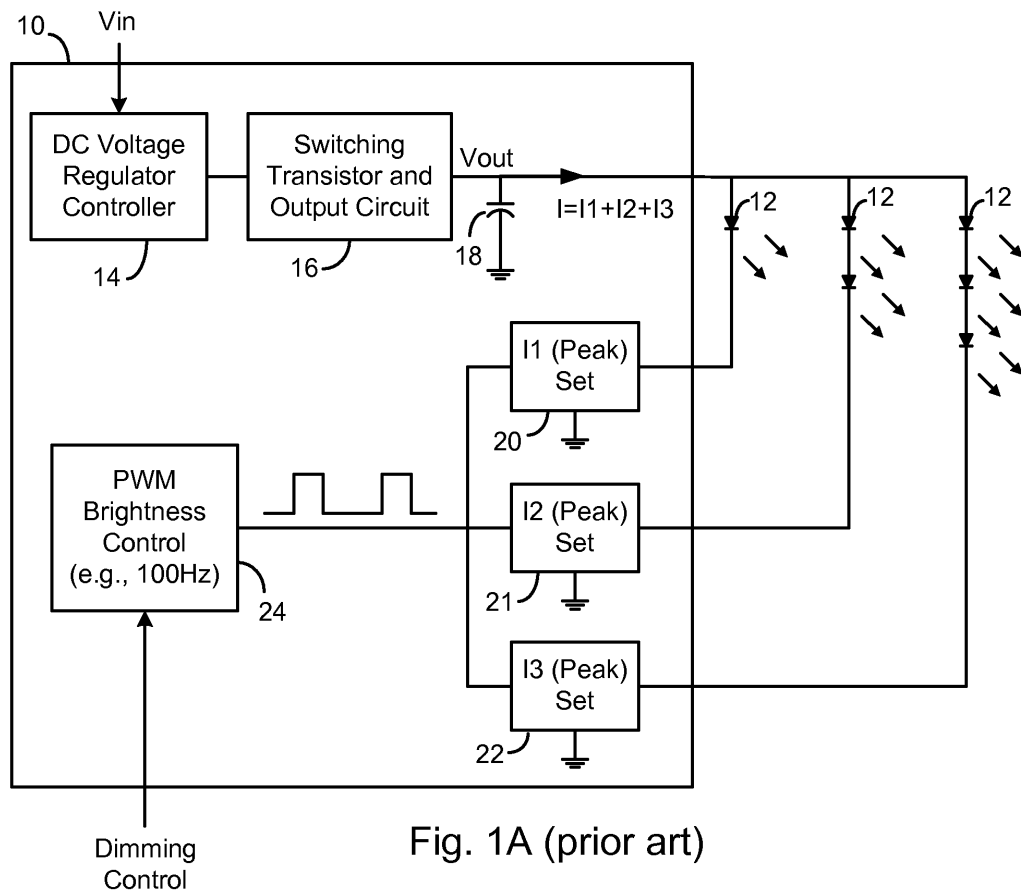


Fig. 1A (prior art)

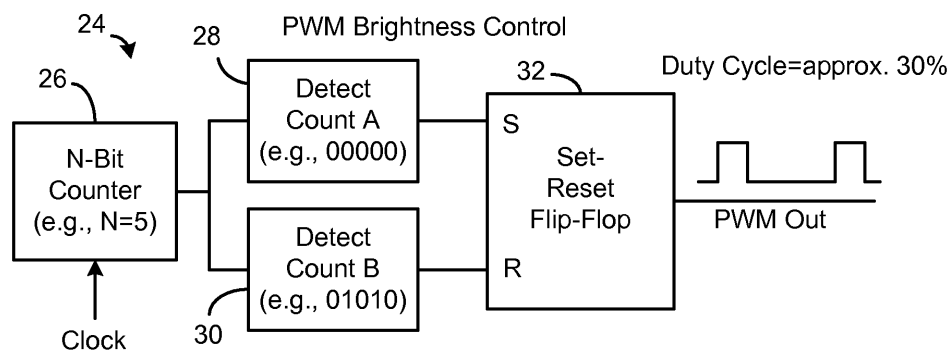


Fig. 1B (prior art)

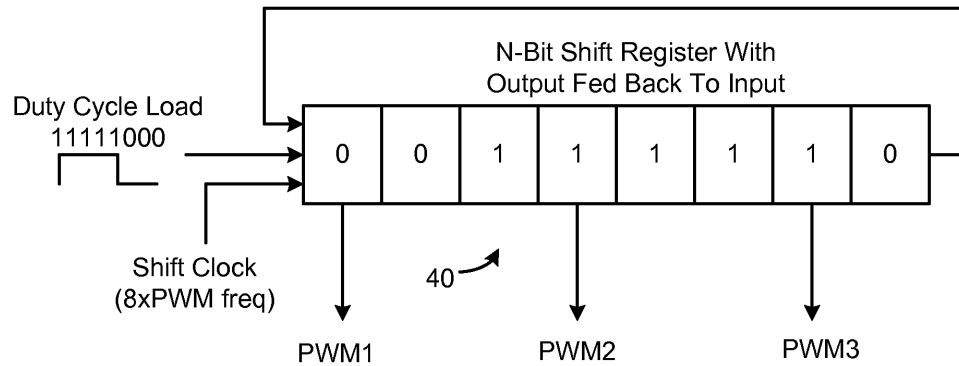


Fig. 2A

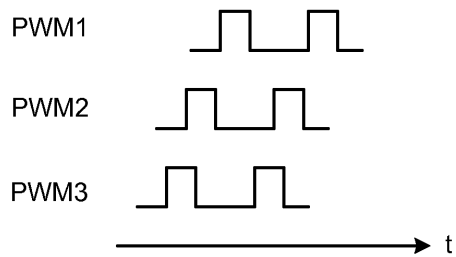


Fig. 2B

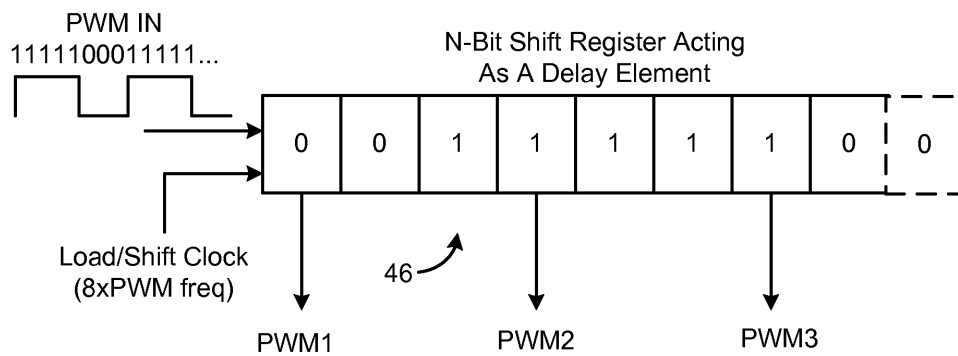


Fig. 3

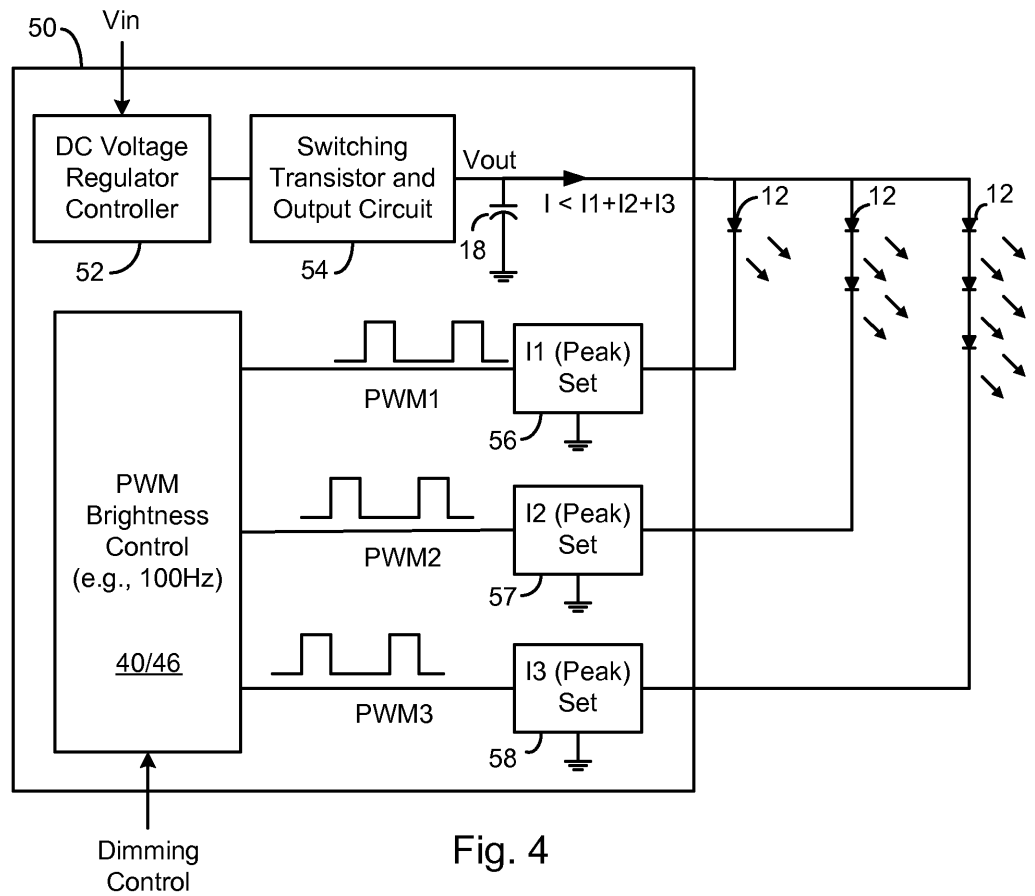


Fig. 4

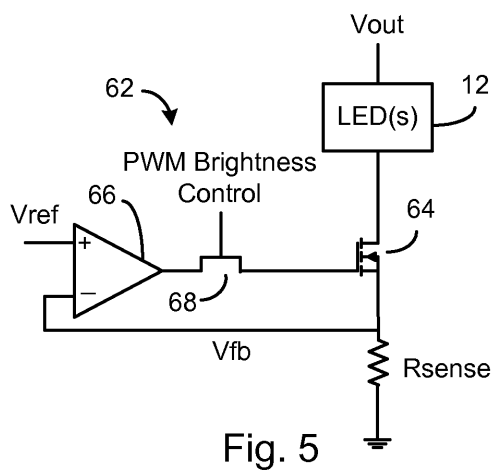


Fig. 5

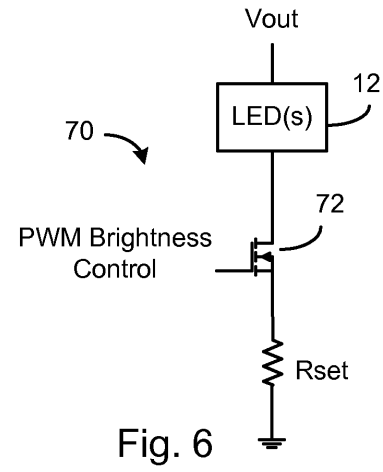


Fig. 6

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As a below named inventor, I hereby declare that:

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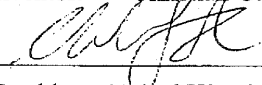
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Full name of first joint inventor: Christian Gater

Inventor's Signature: 

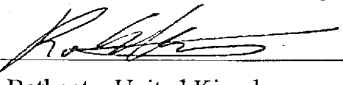
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Mailing Address of Applicant:					
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Applicant Authority ☒ Inventor		☐ Legal Representative under 35 U.S.C. 117		☐ Party of Interest under 35 U.S.C. 118	
Prefix	Given Name	Middle Name	Family Name	Suffix	
	Roel	Van	Ettinger		
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service					
City	Bathgate		Country Of Residenceⁱ	UK	
Citizenship under 37 CFR 1.41(b)ⁱ		NL			
Mailing Address of Applicant:					
Address 1		110 Inch Wood Avenue			
Address 2					
City	Bathgate		State/Province		
Postal Code			Countryⁱ	UK	
All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the Add button.					
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Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below. For further information see 37 CFR 1.33(a).
☐ An Address is being provided for the correspondence Information of this application.

EFS Web 2.2.1

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	MIC-M261	
		Application Number		
Title of Invention	Driving Multiple Parallel LEDs with Reduced Power Supply Ripple			
Customer Number	32566			
Email Address	brian@patentlawgroup.com		Add Email	Remove Email

Application Information:

Title of the Invention	Driving Multiple Parallel LEDs with Reduced Power Supply Ripple		
Attorney Docket Number	MIC-M261	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Suggested Class (if any)		Sub Class (if any)	
Suggested Technology Center (if any)			
Total Number of Drawing Sheets (if any)	3	Suggested Figure for Publication (if any)	4

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)
☐ Request Not to Publish. I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application has not and will not be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

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Please Select One:	☒ Customer Number	☐ US Patent Practitioner	☐ Limited Recognition (37 CFR 11.9)
Customer Number	32566		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78(a)(2) or CFR 1.78(a)(4), and need not otherwise be made part of the specification.			
Prior Application Status		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the Add button.			Add

Foreign Priority Information:

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	MIC-M261
	Application Number	
Title of Invention	Driving Multiple Parallel LEDs with Reduced Power Supply Ripple	

This section allows for the applicant to claim benefit of foreign priority and to identify any prior foreign application for which priority is not claimed. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(a).

Remove			
Application Number	Country ⁱ	Parent Filing Date (YYYY-MM-DD)	Priority Claimed
			☒ Yes ☐ No
Additional Foreign Priority Data may be generated within this form by selecting the Add button.			Add

Assignee Information:

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Assignee 1			
If the Assignee is an Organization check here. ☒			
Organization Name	Micrel, Inc.		
Mailing Address Information:			
Address 1	2180 Fortune Drive		
Address 2			
City	San Jose	State/Province	CA
Country ⁱ	US	Postal Code	95131
Phone Number		Fax Number	
Email Address			
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Signature:

A signature of the applicant or representative is required in accordance with 37 CFR 1.33 and 10.18. Please see 37 CFR 1.4(d) for the form of the signature.

Signature	/Brian D Ogonowsky/	Date (YYYY-MM-DD)	2008-04-08
First Name	Brian	Last Name	Ogonowsky
		Registration Number	31988

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Electronic Patent Application Fee Transmittal				
Application Number:				
Filing Date:				
Title of Invention:		Driving Multiple Parallel LEDs with Reduced Power Supply Ripple		
First Named Inventor/Applicant Name:		Christian Gater		
Filer:		Brian D. Ogonowsky/Edith Fuentes		
Attorney Docket Number:		MIC-M261		
Filed as Large Entity				
Utility Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Utility application filing	1011	1	310	310
Utility Search Fee	1111	1	510	510
Utility Examination Fee	1311	1	210	210
Pages:				
Claims:				
Claims in excess of 20	1202	3	50	150
Miscellaneous-Filing:				
Petition:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1180

Electronic Acknowledgement Receipt	
EFS ID:	3119739
Application Number:	12099729
International Application Number:	
Confirmation Number:	4705
Title of Invention:	Driving Multiple Parallel LEDs with Reduced Power Supply Ripple
First Named Inventor/Applicant Name:	Christian Gater
Customer Number:	32566
Filer:	Brian D. Ogonowsky/Edith Fuentes
Filer Authorized By:	Brian D. Ogonowsky
Attorney Docket Number:	MIC-M261
Receipt Date:	08-APR-2008
Filing Date:	
Time Stamp:	19:33:04
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$ 1180
RAM confirmation Number	3571
Deposit Account	502226
Authorized User	OGONOWSKY,BRIAN D
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)					
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Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)					
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)
1		MIC-M261_App.pdf	78564	yes	15
			cde23a6e88d96a00de90cdceb348e9e dd85181fa		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Specification		1	9	
	Claims		10	14	
	Abstract		15	15	
Warnings:					
Information:					
2	Drawings-only black and white line drawings	MIC-M261_Dwgs.pdf	46931	no	3
			74213864c39185f335125546cd617d23 1f41d64d		
Warnings:					
Information:					
3	Oath or Declaration filed	MIC-M261_Declaration.pdf	256210	no	2
			ae614ea7dfad63d6124e93871cb14c53 33bdf536		
Warnings:					
Information:					
4	Application Data Sheet	MIC-M261_sb0014-ADS.pdf	700154	no	3
			ed614f48962e38bd19c38c1a4122193b b2c961cf		
Warnings:					
Information:					
5	Fee Worksheet (PTO-06)	fee-info.pdf	8485	no	2
			c1438b3ec13c369ab3bd0d1f8ce9f8798 a8b0025		
Warnings:					
Information:					
Total Files Size (in bytes):			1090344		

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National Stage of an International Application under 35 U.S.C. 371

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New International Application Filed with the USPTO as a Receiving Office

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Filing Date: 04/08/08

PTO/SB/06 (12-04)

Approved for use through 7/31/2006. OMB 0651-0032

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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PATENT APPLICATION FEE DETERMINATION RECORD						Application or Docket Number 12/099,729	
APPLICATION AS FILED – PART I							
(Column 1)		(Column 2)		(Column 3)			
FOR	NUMBER FILED	NUMBER EXTRA					
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A					
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A					
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A					
TOTAL CLAIMS (37 CFR 1.16(i))	22	minus 20 =	2				
INDEPENDENT CLAIMS (37 CFR 1.16(h))	2	minus 3 =	0				
APPLICATION SIZE FEE (37 CFR 1.16(s))	3						
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.							
APPLICATION AS AMENDED – PART II							
(Column 1)		(Column 2)		(Column 3)			
AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA				
	Total (37 CFR 1.16(i))	Minus **	=				
	Independent (37 CFR 1.16(h))	Minus ***	=				
	Application Size Fee (37 CFR 1.16(s))						
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
(Column 1)		(Column 2)		(Column 3)			
AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA				
	Total (37 CFR 1.16(i))	Minus **	=				
	Independent (37 CFR 1.16(h))	Minus ***	=				
	Application Size Fee (37 CFR 1.16(s))						
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
(Column 1)		(Column 2)		(Column 3)			
SMALL ENTITY		OTHER THAN SMALL ENTITY		OR			
RATE (\$)	FEE (\$)	RATE (\$)	FEE (\$)				
N/A		N/A	310				
N/A		N/A	510				
N/A		N/A	210				
X\$ 25		X\$50	100				
X\$100		X\$210	0				
185		370					
TOTAL	0	TOTAL	1130				
SMALL ENTITY		OTHER THAN SMALL ENTITY		OR			
RATE (\$)	ADDITIONAL FEE (\$)	RATE (\$)	ADDITIONAL FEE (\$)				
X =		X =					
X =		X =					
N/A		N/A					
TOTAL ADD'T FEE		TOTAL ADD'T FEE					
SMALL ENTITY		OTHER THAN SMALL ENTITY		OR			
RATE (\$)	ADDITIONAL FEE (\$)	RATE (\$)	ADDITIONAL FEE (\$)				
X =		X =					
X =		X =					
N/A		N/A					
TOTAL ADD'T FEE		TOTAL ADD'T FEE					
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.							

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If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Patent Application Fee Transmittal				
Application Number:				
Filing Date:				
Adjustment date: 04/25/2008 HMOHAMM1 04/09/2008 INTEFSW 00003571 12099729 04 FC:1202 -150.00 OP 04/25/2008 HMOHAMM1 00000021 12099729 01 FC:1202 100.00 OP		Driving Multiple Parallel LEDs with Reduced Power Supply Ripple		
Title of Invention:				
Refund Ref: 0030054685 04/25/2008				
Credit Card Refund Total: \$50.00				
Discover: XXXXXXXXXXXX2963				
First Named Inventor/Applicant Name:		Christian Gater		
Filer:		Brian D. Ogonowsky/Edith Fuentes		
Attorney Docket Number:		MIC-M261		
Filed as Large Entity				
Utility Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Utility application filing	1011	1	310	310
Utility Search Fee	1111	1	510	510
Utility Examination Fee	1311	1	210	210
Pages:				
Claims:				
Claims in excess of 20	1202	3	50	150
Miscellaneous-Filing:				
Petition:				



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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
12/099,729	04/08/2008	2821	1130	MIC-M261	22	2

CONFIRMATION NO. 4705

FILING RECEIPT



32566
PATENT LAW GROUP LLP
2635 NORTH FIRST STREET
SUITE 223
SAN JOSE, CA 95134

Date Mailed: 04/29/2008

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Filing Receipt Corrections. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Christian Gater, Dunblane, UNITED KINGDOM;
Roel Van Ettinger, Bathgate, UNITED KINGDOM;

Assignment For Published Patent Application

MICREL, INC., San Jose, CA

Power of Attorney: The patent practitioners associated with Customer Number 32566

Domestic Priority data as claimed by applicant

Foreign Applications

If Required, Foreign Filing License Granted: 04/25/2008

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 12/099,729**

Projected Publication Date: 10/08/2009

Non-Publication Request: No

Early Publication Request: No

Title

Driving Multiple Parallel LEDs with Reduced Power Supply Ripple

Preliminary Class

315

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page 2 of 3

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CLAIMS

What is claimed is:

1. A light emitting diode (LED) driver for driving LEDs connected to different
5 parallel paths, the driver comprising:
 - a voltage source for connection to first ends of LEDs in a plurality of parallel paths;
 - a plurality of current set circuits, one current set circuit per parallel path, each current set circuit controlling a peak current through one or more LEDs connected in
10 each parallel path; and
 - a pulse-width modulated (PWM) brightness control signal generator connected to the plurality of current set circuits, the brightness control signal generator being configured to generate staggered PWM brightness control signals to the plurality of current set circuits,
 - 15 each current set circuit being configured to draw the peak current through its associated one or more LEDs at a duty cycle substantially corresponding to a duty cycle of a PWM brightness control signal applied to it, such that the plurality of current set circuits conduct current through their associated one or more LEDs at the same duty cycle but out of phase with each other.
- 20 2. The driver of Claim 1 wherein the voltage source is a step up voltage regulator.
3. The driver of Claim 1 wherein each current set circuit is a current regulator.
4. The driver of Claim 1 wherein each current set circuit is a current regulator
comprising:
 - 25 a current control transistor in series with one or more LEDs in an associated parallel path; and

a feedback circuit connected to detect a current through the parallel path and connected to the current control transistor to control a conductivity of the current control transistor to cause the current through the parallel path to match a reference level.

5 5. The driver of Claim 4 wherein each current set circuit further comprises a PWM brightness control transistor connected between an output of the feedback circuit and a control terminal of the current control transistor, the PWM brightness control transistor being connected to the PWM brightness control signal generator for receiving a staggered PWM brightness control signal to couple the output of the feedback circuit to the control terminal
10 of the current control transistor at a duty cycle of the staggered PWM brightness control signal.

6. The driver of Claim 1 wherein each current set circuit comprises:

a current set resistor in series with one or more LEDs in an associated parallel path; and

15 a PWM brightness control transistor connected in series between the current set resistor and the one or more LEDs in an associated parallel path, the PWM brightness control transistor being connected to the PWM brightness control signal generator for receiving a staggered PWM brightness control signal.

7. The driver of Claim 1 wherein the PWM brightness control signal generator
20 comprises:

a shift register storing bits corresponding to a PWM duty cycle of a brightness control signal, the shift register having bit positions;

a clock connected to the shift register for shifting the bits along the shift register; and

25 taps off the shift register coupled to different bit positions of the shift register, each tap providing a different staggered PWM brightness control signal connected to an associated current set circuit.

8. The driver of Claim 7 wherein the shift register has a connection that connects an end bit position to a first bit position so that bits in the shift register are recirculated in the shift register.

5 9. The driver of Claim 7 wherein the bits corresponding to a PWM duty cycle of a brightness control signal are serially and continuously loaded into a first bit position of the shift register, then shifted by the clock.

10. The driver of Claim 7 wherein the clock shifts the bits at a rate equal to N times a frequency of the PWM brightness control signal, where N equals the number of bits representing a single PWM duty cycle.

10 11. The driver of Claim 1 wherein the plurality of parallel paths comprises at least three paths.

12. The driver of Claim 1 further comprising the LEDs connected to the driver.

Rule 1.126 ~~13~~ 14. The driver of Claim 1 wherein the driver is formed as an integrated circuit.

14 15 15. A method for driving light emitting diodes (LEDs) connected to different parallel paths, the method comprising:

supplying a voltage to first ends of LEDs in a plurality of parallel paths;

setting a peak current through one or more LEDs connected in each of the parallel paths, the peak current being set by a current set circuit for each parallel path;

20 generating staggered pulse width modulated (PWM) brightness control signals;

applying a different staggered PWM brightness control signals to each current set circuit; and

25 drawing the peak current through the one or more LEDs in each parallel path, set by its associated current set circuit, at a duty cycle corresponding to a duty cycle of an associated PWM brightness control signal, such that the parallel paths of LEDs conduct current at substantially the same duty cycle but out of phase with each other.

¹⁵
16. The method of Claim 15 further comprising varying the duty cycle of the staggered PWM brightness control signals to change an average current through the parallel paths of LEDs to change a perceived brightness of the LEDs.

¹⁶
17. The method of Claim 15 wherein setting a peak current through one or more
5 LEDs connected in each of the parallel paths comprises setting the peak current by controlling conductivity of a current control transistor in series with each parallel path, and wherein applying a different staggered PWM brightness control signal to each current set circuit comprises:

Rule 1.126
10 coupling each staggered PWM brightness control signal to a control terminal of an associated pass transistor, each pass transistor being connected between a control terminal of a respective current control transistor and a regulating control voltage, such that the current control transistor is turned on and off corresponding to a duty cycle of the associated pass transistor.

¹⁷
18. The method of Claim 15 wherein applying a different staggered PWM
15 brightness control signal to each current set circuit comprises applying each staggered PWM brightness control signals to an associated transistor connected in series with the one or more LEDs in an associated parallel path, such that the transistor is turned on and off corresponding to the duty cycle of the staggered PWM brightness control signal applied to it.

¹⁸
19. The method of Claim 15 wherein generating staggered PWM brightness
20 control signals comprises:

storing bits corresponding to a PWM duty cycle of a brightness control signal in a shift register, the shift register having bit positions;

shifting the bits along the shift register under control of a clock; and

receiving bits tapped off the shift register at different bit positions of the shift
25 register to generate a different staggered PWM brightness control signal from the bits at each of the different bit positions.

¹⁹
~~20.~~ The method of Claim 19 further comprising recirculating bits in the shift register by feeding a bit at an output bit position to an input bit position along the shift register.

²⁰
~~21.~~ The method of Claim 19 further comprising serially and continuously loading
5 bits corresponding to a PWM duty cycle of a brightness control signal into a first bit position of the shift register, then shifting the bits by the clock.

²¹
~~22.~~ The method of Claim 19 wherein the clock shifts the bits at a rate equal to N times a frequency of the PWM brightness control signal, where N equals the number of bits representing a single PWM duty cycle.

²²
~~23.~~ The method of Claim 15 wherein the plurality of parallel paths comprises at
10 least three paths.

Doc Code: PD.TO.AUTH

Document Description: Authorization to access Appl. by Trilateral Office

PTO/SB/39 (11-08)
Approved for use through 12/31/2008. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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COMPLETE IF KNOWN	
Application Number	12099729
Filing Date	April 8, 2008
First Named Inventor	Christian Gater
Attorney Docket Number	MIC-M261
Title (Required)	DRIVING MULTIPLE PARALLEL LEDS WIT

Send completed form to: Commissioner for Patents
P.O. Box 1450, Alexandria, VA 22313-1450

The undersigned hereby grants the USPTO authority to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), and any other intellectual property offices in which a foreign application claiming priority to the above-identified application is filed access to the above-identified patent application. See 37 CFR 1.14(c) and (h).

In accordance with 37 CFR 1.14(h)(3), access will be provided to a copy of the application-as-filed with respect to: 1) the above-identified application, 2) any foreign application to which the above-identified application claims priority under 35 USC 119(a)-(d) if a copy of the foreign application that satisfies the certified copy requirement of 37 CFR 1.55 has been filed in the above-identified US application, and 3) any U.S. application from which benefit is sought in the above-identified application.

In accordance with 37 CFR 1.14(c), access may be provided to information concerning the date of filing the Authorization to Permit Access to Application by Participating Offices.

This written authorization should be submitted prior to the filing of a subsequent foreign application, in which priority is claimed to the above-identified patent application, with any intellectual property office (e.g., the EPO, JPO, or KIPO). However, if applicant does not wish the EPO, JPO, KIPO, or other intellectual property office in which a foreign application claiming priority to the above-identified application is filed to have access to the application, this written authorization should not be filed.

No fee will be charged under 37 CFR 1.19(b)(1) for providing a participating intellectual property office with an electronic copy of the above-identified application.

This form must be signed by an authorized party in accordance with 37 CFR 1.14(c).

/Brian D Ogonowsky/

March 24, 2009

Signature

Date

Brian D. Ogonowsky

408-382-0480 x202

Printed or Typed Name

Telephone Number

Attorney for Applicant

31988

Title

Registration Number, if applicable

This collection of information is required by 37 CFR 1.14(h). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process an application). Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 6 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt	
EFS ID:	5025679
Application Number:	12099729
International Application Number:	
Confirmation Number:	4705
Title of Invention:	Driving Multiple Parallel LEDs with Reduced Power Supply Ripple
First Named Inventor/Applicant Name:	Christian Gater
Customer Number:	32566
Filer:	Brian D. Ogonowsky/Linda Richardson
Filer Authorized By:	Brian D. Ogonowsky
Attorney Docket Number:	MIC-M261
Receipt Date:	24-MAR-2009
Filing Date:	08-APR-2008
Time Stamp:	16:17:26
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment		no			
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Authorization to access Appl. by Trilateral Office	MIC-M261-Author-to-permit-access.pdf	221127 5efe20c10c658bfe7e9c531e983e10101e5fbb7f	no	2
Warnings:					
Information:					

Total Files Size (in bytes):	221127
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.	



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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
12/099,729	04/08/2008	2821	1130	MIC-M261	22	2

32566
PATENT LAW GROUP LLP
2635 NORTH FIRST STREET
SUITE 223
SAN JOSE, CA 95134

**CONFIRMATION NO. 4705
REPLACEMENT FILING RECEIPT**



Date Mailed: 03/30/2009

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Christian Gater, Dunblane, UNITED KINGDOM;
Roel Van Ettinger, Bathgate, UNITED KINGDOM;

Assignment For Published Patent Application

MICREL, INC., San Jose, CA

Power of Attorney: The patent practitioners associated with Customer Number 32566

Domestic Priority data as claimed by applicant

Foreign Applications

Permission to Access - A proper **Authorization to Permit Access to Application by Participating Offices** (PTO/SB/39 or its equivalent) has been received by the USPTO.

If Required, Foreign Filing License Granted: 04/25/2008

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 12/099,729**

Projected Publication Date: 10/08/2009

Non-Publication Request: No

Early Publication Request: No

Title

Driving Multiple Parallel LEDs with Reduced Power Supply Ripple

Preliminary Class

315

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

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The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as

page 2 of 3

set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign Assets Control, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).



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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/099,729	04/08/2008	Christian Gater	MIC-M261

32566
PATENT LAW GROUP LLP
2635 NORTH FIRST STREET
SUITE 223
SAN JOSE, CA 95134

CONFIRMATION NO. 4705
PUBLICATION NOTICE



OC00000038186089

Title:Driving Multiple Parallel LEDs with Reduced Power Supply Ripple

Publication No.US-2009-0251071-A1

Publication Date:10/08/2009

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publicly available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently <http://www.uspto.gov/patft/>.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently <http://pair.uspto.gov/>. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101



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NOTICE OF ALLOWANCE AND FEE(S) DUE

32566 7590 08/05/2010

PATENT LAW GROUP LLP
2635 NORTH FIRST STREET
SUITE 223
SAN JOSE, CA 95134

EXAMINER

VU, JIMMY T

ART UNIT

PAPER NUMBER

2821

DATE MAILED: 08/05/2010

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/099,729	04/08/2008	Christian Gater	MIC-M261	4705

TITLE OF INVENTION: DRIVING MULTIPLE PARALLEL LEDS WITH REDUCED POWER SUPPLY RIPPLE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1510	\$300	\$0	\$1810	11/05/2010

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

Page 1 of 3

PTOL-85 (Rev. 08/07) Approved for use through 08/31/2010.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

32566 7590 08/05/2010

PATENT LAW GROUP LLP
2635 NORTH FIRST STREET
SUITE 223
SAN JOSE, CA 95134

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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12/099,729 04/08/2008 Christian Gater MIC-M261 4705

TITLE OF INVENTION: DRIVING MULTIPLE PARALLEL LEDS WITH REDUCED POWER SUPPLY RIPPLE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1510	\$300	\$0	\$1810	11/05/2010

EXAMINER	ART UNIT	CLASS-SUBCLASS
VU, JIMMY T	2821	315-291000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/099,729	04/08/2008	Christian Gater	MIC-M261	4705
32566	7590	08/05/2010	EXAMINER	
PATENT LAW GROUP LLP 2635 NORTH FIRST STREET SUITE 223 SAN JOSE, CA 95134			VU, JIMMY T	
			ART UNIT	PAPER NUMBER
			2821	
DATE MAILED: 08/05/2010				

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)

(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 423 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 423 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Notice of Allowability	Application No.		Applicant(s)	
	12/099,729		GATER ET AL.	
	Examiner		Art Unit	
	JIMMY T. VU		2821	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 04/08/08 and 07/31/08.

2. ☒ The allowed claim(s) is/are 1-22.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) ☐ All b) ☐ Some* c) ☐ None of the:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).
 * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
 (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
 1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
 (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892) 2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948) 3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____ 4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material	5. ☐ Notice of Informal Patent Application 6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ 7. ☒ Examiner's Amendment/Comment 8. ☒ Examiner's Statement of Reasons for Allowance 9. ☐ Other _____.
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	/Douglas W Owens/ Supervisory Patent Examiner, Art Unit 2821
--	---

DETAILED ACTION

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it **MUST** be submitted no later than the payment of the issue fee.

The application has been amended as follows:

In claim 1, line 8, change "with" to --width--.

In renumbered claims 15-18 and 22, line 1 of each claim, change "The method of Claim 15" to --The method of claim 14-- (because original claim 15 has been corrected to claim 14).

In renumbered claims 19-21, line 1 of each claim, change "The method of Claim 19" to --The method of claim 18-- (because original claim 19 has been corrected to claim 18).

Allowable Subject Matter

2. Claims 1-22 are allowed.

3. The following is an examiner's statement of reasons for allowance:

None of the prior art teaches or fairly suggests a light emitting diode (LED) driver and method comprising "each current set circuit being configured to draw the peak current through its associated one or more LEDs at a duty cycle substantially corresponding to a duty cycle of a PWM brightness control signal applied to it, such that

the plurality of current set circuits conduct current through their associated one or more LEDs at the same duty cycle but out of phase with each other” (claims 1 and 14).

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled “Comments on Statement of Reasons for Allowance.”

4. The prior art made of record and relied upon is considered pertinent to applicant’s disclosure. The best consider with this application can be filed in Henry (U.S. Patent 6,812,776 B2), Robinson (U.S. Patent 7,358,681 B2) and Ragonesi (U.S. Patent 7,609,237 B2).

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jimmy T Vu whose telephone number is (571) 272-1832. The examiner can normally be reached on M - F: 9 - 6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner’s supervisor, Douglas W. Owens can be reached on (571) 272-1662. The fax phone numbers for the organization where this application or proceeding is assigned are (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-2800.

Application/Control Number: 12/099,729
Art Unit: 2821

Page 4

/Jimmy Vu/

July 31, 2010

/Douglas W Owens/
Supervisory Patent Examiner, Art Unit 2821
August 2, 2010

Notice of References Cited	Application/Control No. 12/099,729	Applicant(s)/Patent Under Reexamination GATER ET AL.	
	Examiner JIMMY T. VU	Art Unit 2821	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-7,358,681	04-2008	Robinson et al.	315/224
*	B	US-6,812,776	11-2004	Henry, George C.	327/536
*	C	US-7,609,237	10-2009	Ragonesi et al.	345/82
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

U.S. Patent and Trademark Office
PTO-892 (Rev. 01-2001)

Notice of References Cited

Part of Paper No. 20100731

<i>Index of Claims</i> 	Application/Control No. 12099729	Applicant(s)/Patent Under Reexamination GATER ET AL.
	Examiner JIMMY T VU	Art Unit 2821

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47										
CLAIM			DATE							
Final	Original		07/31/2010							
1	1	=								
2	2	=								
3	3	=								
4	4	=								
5	5	=								
6	6	=								
7	7	=								
8	8	=								
9	9	=								
10	10	=								
11	11	=								
12	12	=								
13	13	=								
14	14	=								
15	15	=								
16	16	=								
17	17	=								
18	18	=								
19	19	=								
20	20	=								
21	21	=								
22	22	=								

Search Notes 	Application/Control No. 12099729	Applicant(s)/Patent Under Reexamination GATER ET AL.
	Examiner JIMMY T VU	Art Unit 2821

SEARCHED			
Class	Subclass	Date	Examiner
315	185R,186-195,209R,225,226,291,307,312,361,362	7/31/10	JV

SEARCH NOTES		
Search Notes	Date	Examiner
EAST search	7/31/10	JV

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner
315	291,307	7/31/10	JV

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Issue Classification 	Application/Control No. 12099729	Applicant(s)/Patent Under Reexamination GATER ET AL.
	Examiner JIMMY T VU	Art Unit 2821

ORIGINAL						INTERNATIONAL CLASSIFICATION												
CLASS		SUBCLASS				CLAIMED					NON-CLAIMED							
315		291				H	0	5	B	37 / 02 (2006.01.01)								
CROSS REFERENCE(S)																		
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)																	
315	307																	

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	17	17												
2	2	18	18												
3	3	19	19												
4	4	20	20												
5	5	21	21												
6	6	22	22												
7	7														
8	8														
9	9														
10	10														
11	11														
12	12														
13	13														
14	14														
15	15														
16	16														

/JIMMY T VU/ Examiner.Art Unit 2821 (Assistant Examiner)	07/31/10 (Date)	Total Claims Allowed: 22	
/DOUGLAS W OWENS/ Supervisory Patent Examiner.Art Unit 2821 (Primary Examiner)	08/02/2010 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 4

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	19223	((light\$3 near5 emit\$4) LED\$1) with driv\$3) and ((current peak) with set\$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/31 10:28
S2	10	S1 and (((pulse adj width adj modulat\$4) PWM) with (brightness intensity) with signal with phase)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/31 10:30
S3	6852	((light\$3 near5 emit\$4) LED\$1) with (string parallel)) and ((current peak) with set\$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/31 10:32
S4	41	S3 and (((pulse adj width adj modulat\$4) PWM) with signal with phase)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/31 10:32

S5	4	S4 and 315/185R,186-195,225,226,291,307,312,361,362.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/31 10:33
S6	10	S4 and "315"/\$.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/31 10:33
S7	10	S3 and (((pulse adj width adj modulat\$4) PWM) with phase with differen\$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/31 10:34
S8	20412	((((light\$3 near5 emit\$4) LED\$1) with resist\$4 with connect\$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/31 10:37
S9	16	S8 and (((pulse adj width adj modulat\$4) PWM) with phase with differen\$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/31 10:38
S10	14	S8 and (((pulse adj width adj modulat\$4) PWM) with phase with cycle)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/31 10:38

S11	52	S8 and (((pulse adj width adj modulat\$4) PWM) with signal with phase)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/31 10:39
S12	8	S11 and 315/185R,186-195,209R,225,226,291,307,312,361,362.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/31 10:39
S13	17	S11 and "363"\$.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/31 10:41
S14	0	S11 and "362"\$.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/31 10:42
S15	9	S11 and "323"\$.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/31 10:42
S16	7815	(((light\$3 near5 emit\$4) LED\$1) with resist\$4 with connect\$3 with (parallel series))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/31 10:45

S17	34	S16 and (((pulse adj width adj modulat\$4) PWM) with signal with phase)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/31 10:46
S18	1	S17 and 315/185R,186-195,209R,225,226,291,307,312,361,362.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/31 10:46
S19	68	S16 and (((pulse adj width adj modulat\$4) PWM) with phase)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/31 10:46
S20	17	S19 and 315/185R,186-195,209R,225,226,291,307,312,361,362.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/31 10:47
S21	150	(((light\$3 near5 emit\$4) LED\$1) with parallel) and (current with peak with set\$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/31 10:50
S22	38	S21 and 315/185R,186-195,209R,225,226,291,307,312,361,362.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/31 10:50

S23	1	("7276861").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/07/31 10:53
S24	8	2002/0047642	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/31 11:04
S25	20	"20020047642" "20030117088" "20030169097" "20030227265" "20030234621" "20040041620" "20040164685" "20040183482" "20040190291" "20040195978" "20050128168" "6351079" "6515434" "6522558" "6525488" "6556067" "6628252" "6636104" "6812776" "6822403").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/07/31 11:06
S26	0	S25 and (((pulse adj width adj modulat\$4) PWM) with phase)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/31 11:14
S27	9	((CHRISTIAN) near2 (GATER)).INV.	US-PGPUB; USPAT; USOCR	OR	ON	2010/07/31 11:15
S28	6	((ROEL) near2 (ETTINGER)).INV.	US-PGPUB; USPAT; USOCR	OR	ON	2010/07/31 11:16

7/31/10 11:47:15 AM

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EAST Search History**EAST Search History (Interference)**

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	3465	((light\$3 near5 emit \$4) LED\$1) and ((current peak) with set \$4)).clm.	US-PGPUB; USPAT; UPAD	OR	ON	2010/08/02 09:32
L2	2	((light\$3 near5 emit \$4) LED\$1) and ((current peak) with set \$4) and (((pulse adj width adj modulat\$4) PWM) with signal with phase)).clm.	US-PGPUB; USPAT; UPAD	OR	ON	2010/08/02 09:32

8/ 2/ 10 9:33:03 AM**C:\ Documents and Settings\ jvu\ My Documents\ EAST\ Workspaces\ 2099729. wsp**



UNITED STATES PATENT AND TRADEMARK OFFICE

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 P.O. Box 1450
 Alexandria, Virginia 22313-1450
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BIB DATA SHEET

CONFIRMATION NO. 4705

SERIAL NUMBER 12/099,729	FILING or 371(c) DATE 04/08/2008 RULE	CLASS 315	GROUP ART UNIT 2821	ATTORNEY DOCKET NO. MIC-M261		
APPLICANTS Christian Gater, Dunblane, UNITED KINGDOM; Roel Van Ettinger, Bathgate, UNITED KINGDOM; ** CONTINUING DATA ***** None JV ** FOREIGN APPLICATIONS ***** None JV ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 04/25/2008						
Foreign Priority claimed ☐ Yes ☒ No 35 USC 119(a-d) conditions met ☐ Yes ☒ No Verified and Acknowledged <u>/JIMMY T VU/</u> Examiner's Signature		☐ Met after Allowance <u>/JV/</u> Initials	STATE OR COUNTRY UNITED KINGDOM	SHEETS DRAWINGS 3	TOTAL CLAIMS 22	INDEPENDENT CLAIMS 2
ADDRESS PATENT LAW GROUP LLP 2635 NORTH FIRST STREET SUITE 223 SAN JOSE, CA 95134 UNITED STATES						
TITLE Driving Multiple Parallel LEDs with Reduced Power Supply Ripple						
FILING FEE RECEIVED 1130	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:			☐ All Fees		
				☐ 1.16 Fees (Filing)		
				☐ 1.17 Fees (Processing Ext. of time)		
				☐ 1.18 Fees (Issue)		
				☐ Other _____		
☐ Credit						

BIB (Rev. 05/07).

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
 or **Fax** (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

32566 7590 08/05/2010

PATENT LAW GROUP LLP
 2635 NORTH FIRST STREET
 SUITE 223
 SAN JOSE, CA 95134

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
Electronic Filing (Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/099,729	04/08/2008	Christian Gater	MIC-M261	4705

TITLE OF INVENTION: DRIVING MULTIPLE PARALLEL LEDS WITH REDUCED POWER SUPPLY RIPPLE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1510	\$300	\$0	\$1810	11/05/2010
EXAMINER	ART UNIT	CLASS-SUBCLASS				
VU, JIMMY T	2821	315-291000				

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Patent Law Group LLP

2 Brian D. Ogonowsky

3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

Micrel, Inc.

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

San Jose, California

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

☒ Issue Fee

☒ Publication Fee (No small entity discount permitted)

☐ Advance Order - # of Copies None

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

☐ A check is enclosed.

☒ Payment by credit card. ~~For MICROSIS, use MICROSIS~~

☒ The Director is hereby authorized to charge ~~any deficiency~~ any deficiency, or credit any overpayment, to Deposit Account Number 502226 (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature /Brian D Ogonowsky/

Date 2010-10-21

Typed or printed name Brian D. Ogonowsky

Registration No. 31988

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Electronic Patent Application Fee Transmittal				
Application Number:		12099729		
Filing Date:		08-Apr-2008		
Title of Invention:		DRIVING MULTIPLE PARALLEL LEDS WITH REDUCED POWER SUPPLY RIPPLE		
First Named Inventor/Applicant Name:		Christian Gater		
Filer:		Brian D. Ogonowsky/Edith Fuentes		
Attorney Docket Number:		MIC-M261		
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl issue fee	1501	1	1510	1510
Publ. Fee- early, voluntary, or normal	1504	1	300	300

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1810

Electronic Acknowledgement Receipt	
EFS ID:	8671924
Application Number:	12099729
International Application Number:	
Confirmation Number:	4705
Title of Invention:	DRIVING MULTIPLE PARALLEL LEDS WITH REDUCED POWER SUPPLY RIPPLE
First Named Inventor/Applicant Name:	Christian Gater
Customer Number:	32566
Filer:	Brian D. Ogonowsky/Edith Fuentes
Filer Authorized By:	Brian D. Ogonowsky
Attorney Docket Number:	MIC-M261
Receipt Date:	21-OCT-2010
Filing Date:	08-APR-2008
Time Stamp:	15:08:49
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$ 1810
RAM confirmation Number	1487
Deposit Account	502226
Authorized User	OGONOWSKY,BRIAN D
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)					
Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)					
Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)					
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	MIC-M261_Issue-Fee-Trans-PartB.pdf	180859 0cfec480e17e39090e54e13ef4bc127960fb d90	no	1
Warnings:					
Information:					
2	Fee Worksheet (PTO-875)	fee-info.pdf	32371 e3a632eac0914f25537282c2133b59a8f62e 7ea8	no	2
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12/099,729	11/30/2010	7843148	MIC-M261	4705

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ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 423 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

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