

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

VIZIO, INC.

Petitioner,

v.

POLARIS POWERLED TECHNOLOGIES, LLC

Patent Owner.

IPR2024-00073

U.S. Patent No. US 7,843,148

**DECLARATION OF REGAN ZANE, PH.D. IN SUPPORT OF PETITION
FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 7,843,148**

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I, Regan Zane, declare as follows:

I. INTRODUCTION

1. I am submitting this declaration at the request of VIZIO, Inc.
2. I am being compensated for my work in this matter at my standard hourly rate for consulting services. My compensation in no way depends on the outcome of this proceeding.
3. This declaration provides my independent opinions and analyses as to why Claims 1-22 of U.S. Patent No. 7,843,148 (“the ’148 Patent”) are anticipated and/or would have been obvious to a person of ordinary skill in the art (“POSITA”) at the time of the invention of the claimed subject matter. This declaration is provided after my review and analysis of the ’148 Patent, the prior art, relevant background technology, and is also based on my education and experience, as well as additional materials identified herein.

II. QUALIFICATIONS AND BACKGROUND

4. I am the David G. and Diann L. Sant Endowed Professor of Electrical and Computer Engineering at Utah State University (USU), and I have over 25 years of experience in industry and research with power electronics and lighting technologies, including light-emitting diodes (LEDs) and driver circuits for arrays of LEDs as backlights in LCD-TV applications.

5. I received my Bachelor of Science degree in Electrical Engineering (BSEE) from the University of Colorado at Boulder in 1996. In 1998, I received a Master of Science degree in Electrical Engineering (MSEE) from the University of Colorado at Boulder. In 1999, I received a Doctor of Philosophy (Ph.D.) degree in electrical engineering from the University of Colorado at Boulder. My Ph.D. dissertation research focused on the design of low-cost, high performance custom integrated circuit (IC) controllers and gate drives for isolated AC/DC power converters.

6. In 1999, I joined the Corporate Research and Development Center at General Electric (GE) as a Senior Research Scientist. At GE, I developed and commercialized electronic ballasts and driver circuits using custom integrated circuits (IC) for a wide range of applications, including multiple generations of controllers for compact fluorescent lamps (e.g., residential lighting), high intensity discharge lamps (e.g., commercial lighting), and light emitting diodes (LEDs). In my experience at GE I had custom power ICs fabricated at the Taiwan Semiconductor Manufacturing Corporation (TSCM), led laboratory system testing and evaluation, and transitioned the circuits to GE Lighting for pre-production testing. The success of this work led to my Six Sigma Green Belt certification at GE.

7. In 2001, I joined the Department of Electrical, Computer, and Energy Engineering at the University of Colorado at Boulder (CU Boulder) as an Assistant Professor, and I received tenure and was promoted to Associate Professor in 2008. While at CU Boulder, I was one of three faculty members at the Colorado Power Electronics Center (CoPEC), where we developed power solutions in close partnership with industry sponsors. I led numerous research and development (R&D) projects with industry partners on topics including LED drivers, power IC design, analog and digital control of power converters, magnetics design, solar power systems, voltage regulation modules for processors, and power distribution in data centers.

8. In 2004 I received the National Science Foundation (NSF) CAREER award, the highest honor provided by NSF to early career faculty, for my R&D and commercialization work on electronic circuits and drivers for LED lighting. My work at CU Boulder on drivers for LEDs and gas discharge lamps led to numerous publications, patents, and graduated students who have become prominent leaders in the industry. In 2006 I received the Inventor of the Year and Provost Faculty achievement awards for continued advancements to state-of-the-art in the areas of power electronics and energy efficient lighting. In 2008, I received national recognition through the IEEE Power Electronics Society Richard M. Bass Award for outstanding achievement in the field of power electronics based on my work in

the lighting and control areas. At CU Boulder I also taught courses and provided industry seminars and training on electronic circuit design, the fundamentals of power electronics, and advanced courses in modeling and control of power converters, and I received the Holland Teaching Award and the John and Mercedes Peebles Innovation in Teaching Award.

9. In 2012, I became a Full Professor with a USTAR endowment in the Department of Electrical and Computer Engineering at Utah State University (USU). There, I founded and continue to direct the Electric Vehicle & Roadway (EVR) Research Facility and Test Track, the USU Power Electronics Lab (UPEL), and the Battery Limits and Survivability Test (BLAST) lab. In 2016, I formed and launched the multi-university industry sponsored Center for Sustainable Electrified Transportation (SELECT) focused on advanced technologies for electric drive and battery systems for EVs. In 2018, I received and continue to hold the David G. and Diann L. Sant Endowed Professorship at Utah State University.

10. In 2020, I became the founding Director of the NSF Engineering Research Center for Advancing Sustainability through Powered Infrastructure for Roadway Electrification (ASPIRE ERC), the highest award offered by NSF for multi-university, industry-partnered research centers. The ASPIRE ERC includes 10 universities, 4 national labs, more than 85 faculty and staff, more than 300 students, and more than 60 industry and innovation partners. The partners include

representation from automotive original equipment manufacturers (OEMs), Tier 1 component suppliers, utilities, battery manufacturers, national laboratories, and a wide range of state, government, and non-profit agencies.

11. While at USU I have led numerous large-scale R&D and commercialization programs on technologies for lighting systems, battery systems, electric vehicles (EVs), and battery charging infrastructure. As one example, I was the lead principal investigator (PI) for a multi-million dollar, multi-year project in partnership with key industry and national lab partners where we developed new concepts for advanced active battery management systems that were conceived, modeled, and simulated, then developed into hardware prototypes, integrated into commercial battery packs for a leading automotive OEM plug-in hybrid electric vehicle, evaluated for over one year of testing, and finally transitioned for commercialization at a leading automotive OEM.

12. Multiple additional projects on advanced lighting systems, battery management systems, and power converters for a wide range of applications have stemmed from this early work and continue in my research laboratory today. These include development, testing and delivery of plug-and-play portable lithium ion battery packs for vehicles and DC microgrids in military applications, robust battery solutions for electric aircraft, high power fast charging battery packs for electric vehicles, and battery management systems for second life application of batteries

that provide support to the electric utility grid. This work has received numerous awards, including the Utah Innovation Award in Clean Technology and Energy for "Robust and Efficient Battery Management Systems" and the USU Campus Research of the Year Award.

13. Since 2006, I have served as an Associate Editor with IEEE Transactions on Power Electronics. In addition, since 2013 I have served as an Associate Editor for the IEEE Journal of Emerging and Selected Topics in Power Electronics. I have served as conference chairman, co-chair, session chair, and committee member for numerous professional conferences in power electronics over the past 20 years and maintained active participation as a journal article reviewer and elected professional society leader. I have also served on IEEE and SAE committees for development of standards.

14. I am a named inventor on 37 issued United States patents with many pending in the field of power electronics, including multiple in the areas of lighting systems and power electronic technologies. I have authored or co-authored over 200 peer-reviewed journal and top-rated conference papers and articles and have received 3 best journal paper awards. I am co-author of the book titled "Digital control of high-frequency switched-mode power converters," and have provided more than 60 invited seminars and talks. In my more than 20 years as a faculty member, I have trained, advised, and supervised hundreds of students in laboratory

work and I have led multi-million-dollar industry-partnered projects that include hardware prototype development and evaluation, systems demonstration, and pilot deployment in commercial settings. In all, I have been a lead or co-lead on competitive R&D and commercialization projects in partnership with industry totaling over \$85 million leading to well over 100 hardware systems that have been developed and tested in my labs.

15. My publications include co-authorship of *Digital Architecture for Driving Large LED Arrays with Dynamic Bus Voltage Regulation and Phase Shifted PWM*, which I presented at the Twenty-Second Annual IEEE Applied Power Electronics Conference and Exposition in Anaheim, California during February 2007. Both this article and the '148 Patent concern implementation of staggered pulse width modulation (PWM) signals to control the dimming of parallelly connected LEDs. I am a co-inventor on U.S. Patent No. 7,948,468, which is also directed towards systems and methods utilizing staggered PWM signals for dimming control of parallelly connected LEDs.

16. I am qualified to render an opinion regarding the design and development of devices for driving LEDs. Based on my expertise and qualifications, I am qualified to provide an opinion as to what a person of ordinary skill in the art would have understood, known, or concluded as of April 8, 2008, which I have been informed is the earliest priority date for the claims of the '148 Patent.

17. A copy of my *curriculum vitae*, attached as Exhibit 1004, contains further details concerning my education, experience, publications, patents, and other qualifications to render an expert opinion in this matter.

III. INFORMATION AND MATERIALS CONSIDERED

18. I have considered the following list of materials in formulating my opinions in this matter:

Exhibit No.	Description
1001	U.S. Patent No. 7,843,148 (“the ’148 Patent”)
1002	File history of the ’148 Patent
1004	Regan Zane Curriculum Vitae
1005	U.S. Patent No. 5,317,307 to Thomas, Jr. (“Thomas”)
1006	Montu Doshi & Regan Zane, “Digital Architecture for Driving Large LED Arrays with Dynamic Bus Voltage Regulation and Phase Shifted PWM,” APEC 07 (“Zane”)
1007	U.S. Patent No. 6,402,354 to Tatewaki et al. (“Tatewaki”)
1008	Excerpts from Paul Horowitz & Winfield Hill, <i>The Art of Electronics</i> (2nd ed. 1989)
1009	Declaration of Rachel J. Watters re <i>The Art of Electronics</i>

IPR Petition – U.S. Patent No. 7,843,148
VIZIO, Inc. v. Polaris PowerLED Technologies, LLC

Exhibit No.	Description
1010	U.S. Patent No. 3,972,031 to Riemenschneider et al.
1011	Excerpt from Noel M. Morris, <i>Digital Electronic Circuits and Systems</i> (The Macmillan Press Ltd. 1974)
1012	UK Patent Application Publication GB 2459009A to Gater et al.
1013	PDF Printout dated October 6, 2023 of Case Details for GB2459009 from UK Intellectual Property Office website, available at https://www.ipo.gov.uk/p-ipsu/Case/PublicationNumber/GB2459009
1014	Excerpt from <i>Comprehensive Dictionary of Electrical Engineering</i> (2nd ed. 2005)
1015	Plaintiff's Disclosure of Asserted Claims and Infringement Contentions Against Vizio Pursuant to Northern District of California Patent Local Rules 3-1 and 3-2, in <i>Polaris PowerLED Technologies, LLC v. VIZIO, Inc. et al.</i> , No. 2:23-cv-03478-GW-PDx
1016	Montu Doshi & Regan Zane, "Digital Architecture for Driving Large LED Arrays with Dynamic Bus Voltage Regulation and Phase Shifted PWM," APEC 07 Digest
1017	Table of Contents for APEC 07
1018	Montu Doshi & Regan Zane, "Digital Architecture for Driving Large LED Arrays with Dynamic Bus Voltage Regulation and Phase Shifted PWM," APEC 07 Presentation
1019	List of APEC 2007 Exhibitors

Exhibit No.	Description
1020	Declaration of Gordon MacPherson from IEEE re <i>Zane</i>
1021	U.S. Patent Application Publication No. US 2007/0257869A1 to Huang et al. (“Huang”)
1026	Linear Technology, <i>LTC3783 Specification Sheet</i> , 2005
1027	U.S. Patent No. 6,621,235 to Chang (“Chang”)

19. In addition to the materials referenced above, I have also reviewed all other documents and exhibits cited in my declaration, to the extent they are not listed above.

IV. RELEVANT LEGAL STANDARDS

20. I am not a lawyer. Therefore, in formulating my opinions and conclusions in this proceeding, I have been provided with an understanding of the relevant aspects of U.S. patent law that govern the issues of patent validity.

A. Prior Art

21. I understand that, in this IPR proceeding, the prior art to the ’148 Patent includes patents and printed publications. I understand that the priority date for the ’148 Patent is the April 8, 2008 filing date of nonprovisional patent application No.

12/099,729, from which the '148 Patent issued. I have been informed and understand that because the '148 Patent issued from an application filed before March 16, 2013, that whether a reference qualifies as prior art is based on the patent laws before the America Invents Act (“AIA”). I understand that in pre-AIA, a reference may be prior art under 35 U.S.C. § 102(b) if “the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of the application for patent in the United States,” and that a reference may be prior art under 35 U.S.C. § 102(a) if “the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the application for a patent.”

B. Anticipation

22. I understand that 35 U.S.C. § 102 is the statute that governs the determination of anticipation. I understand that under 35 U.S.C. § 102, a prior art reference anticipates a claim if each and every element of a claim is found, either expressly or inherently, within the single prior art reference. I understand that a reference anticipates a claim if all elements of the claim are disclosed within the four corners of the reference in the same arrangement as in the claim.

23. I understand that something is “inherent in,” and therefore taught by the prior art, if it necessarily flows from the explicit disclosure of the prior art. I

understand that the fact that a certain result or characteristic *may* be present in the prior art is not sufficient to establish inherency. However, if the result or characteristic is *necessarily present* based on the explicit disclosure in the prior art, it is inherent in the prior art and is therefore disclosed.

C. Obviousness

24. I understand that a claim of a patent may be unpatentable as obvious under 35 U.S.C. § 103 if the differences between the subject matter set forth in the patent claim and the prior art are such that the claimed subject matter as a whole would have been obvious to a person of ordinary skill in the art at the time of the invention.

25. I understand that obviousness is a determination of law based on various underlying determinations of fact. In particular, these underlying factual determinations include (1) the scope and content of the prior art; (2) the level of ordinary skill in the art at the time the claimed invention was made; (3) the differences between the claimed invention and the prior art; and (4) the extent of any proffered objective “indicia” of non-obviousness. I understand that the objective indicia, also known as secondary considerations, which may be considered in such an analysis include, among other factors: the commercial success of the patented invention (including evidence of industry recognition or awards), the existence of a long-felt but unmet need in the field satisfied by the invention, the failure of others

to arrive at the invention, unexpected results, industry acquiescence and recognition of the invention, initial skepticism of the invention by others in the field, the extent to which the inventors proceeded in a direction contrary to the accepted wisdom of those of ordinary skill in the art, and licensing of the patent.

26. In determining the scope and content of the prior art, I understand a reference is considered prior art for the obviousness analysis if it falls within the inventors' field of endeavor. Additionally, a reference is prior art for the obviousness analysis, even if from a different field of endeavor, if it is reasonably pertinent to the particular problem for which the invention was made. A reference is reasonably pertinent if it is something a person of ordinary skill in the art would have looked to when attempting to solve the problem.

27. While multiple prior art references or elements may be combined to render a patent claim obvious, I understand that a patent claim composed of several elements is not proven obvious merely by demonstrating that each of its elements was, independently, known in the prior art. I understand that I should consider whether there is an "apparent reason" or motivation to combine the prior art references or elements in the way the patent claims. It is my further understanding that the law recognizes several rationales for combining references or modifying a reference to show obviousness of claimed subject matter. Some of these rationales include: combining prior art elements according to known methods to yield

predictable results; simple substitution of one known element for another to obtain predictable results; a predictable use of prior art elements according to their established functions; applying a known technique to a known method or product ready for improvement; and choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success.

28. I also understand that a reference that anticipates a claim would also render that claim obvious.

D. Claim Construction

29. I have been informed the first step of a validity analysis is to construe the claims. I have been informed that the Patent Trial and Appeal Board construes the claims by giving the claim terms their ordinary and customary meaning, as they would have been understood by a person of ordinary skill in the art (“POSITA”) at the time of the invention in view of the intrinsic record (patent specification and file history). For the purposes of this review, and to the extent necessary, I have interpreted each claim term in accordance with its plain and ordinary meaning as it would have been understood by a POSITA at the time of the invention, in view of the intrinsic record.

30. It is my understanding that an inventor may expressly define certain terms used in a patent, and therefore may give a term a meaning that differs from the term’s plain and ordinary meaning. However, I do not believe that the inventors

defined any claim terms whose construction is necessary for my analysis in a manner inconsistent with their plain and ordinary meanings in view of the intrinsic record.

E. Perspective of a Person of Ordinary Skill in the Art at the Time of the Claimed Invention

31. I have been informed that claim construction and patent validity is generally analyzed from the perspective of a POSITA at the time of the invention. I have assumed for purposes of my analysis that the time of the invention, also referred to herein as the “relevant time,” is no later than April 8, 2008. I have based that assumption in part, on the April 8, 2008 filing date of the ’148 Patent, and I am not aware of any effort by Patent Owner to identify a priority date earlier than April 8, 2008 for the claims of the ’148 Patent.

32. I have performed my analyses, and expressed my opinions, from the perspective of the POSITA (as further described below) at the relevant time. In addition, while my declaration analyzes and presents opinions about *Zane*, which is a paper that I co-authored, my analysis of that paper is from the perspective of a POSITA reviewing that paper at the relevant time.

F. Prior-Art Status of References

33. I have been informed and understand that the patent statute defines the requirements for a reference to be considered prior art to the ’148 Patent. As

discussed below, I understand that the prior art references that I have analyzed and discussed in this declaration are prior art to the '148 Patent.

V. LEVEL OF ORDINARY SKILL IN THE ART

34. I understand that validity must be assessed from the perspective of a person of ordinary skill in the art at the time of the invention of the '148 Patent. As set forth above, the '148 Patent issued from an application that was filed on April 8, 2008, and I am not aware of any effort by Patent Owner to identify any priority date earlier than April 8, 2008 for the claims of the '148 Patent. As a result, I understand April 8, 2008 to be the time of the invention for my analysis. I have been informed that the level of ordinary skill in the art may be determined by various factors including: (a) the type of problems encountered in the art, (b) prior art solutions to those problems, (c) the rapidity with which innovations are made, (d) the sophistication of the technology, and (e) the educational level of active workers in the field.

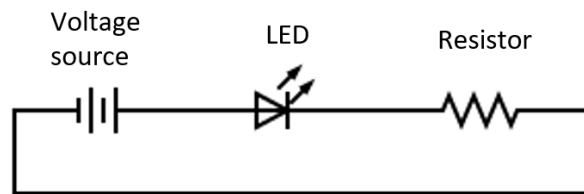
35. In my opinion, a POSITA at the time of the invention of the '148 Patent would have had at least a bachelor's degree in physics, electrical engineering, or a related field, and approximately two years of experience in the fields of LED technology, backlights, LED devices and control thereof, or other related fields. Alternatively, advanced education in the fields of physics, electrical engineering, or a related field can compensate for lesser work experience in the relevant fields. My

opinions concerning the unpatentability of the '148 Patent claims, as set forth herein, are from the perspective of a person of ordinary skill in the art at the time of the invention of the '148 Patent, as set forth above.

VI. THE '148 PATENT

A. Light-Emitting Diodes (LEDs)

36. LEDs are semiconductor circuit elements that emit light when current flows through them. The following circuit diagram illustrates a simple exemplary circuit for driving an LED, consisting of an LED connected in series with a voltage source and a resistor.



The current (I) flowing through the LED is determined by Ohm's Law, $V=IR$. Specifically, the current flowing through the LED in the above diagram is $I=(V-V_{LED})/R$, where V is the voltage provided by the voltage source, V_{LED} is the voltage drop across the LED, and R is the resistance of the resistor. The brightness of an LED is determined by the magnitude of the current flowing through the LED. *See, e.g., EX1001, 1:15-19.* Thus, in the above exemplary circuit, the brightness of the

LED can be varied by varying the resistance of the resistor, R , which in turns varies the current, I .

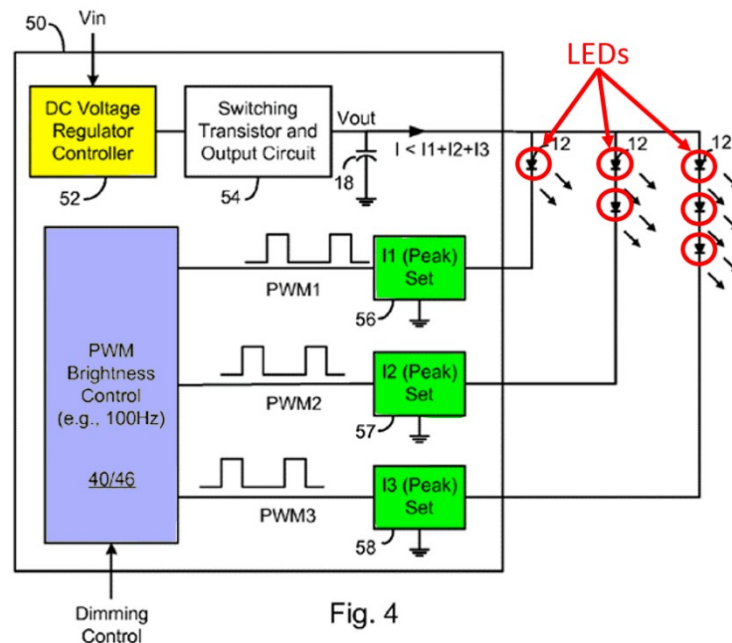
37. LEDs yield significant advantages over prior lighting technologies (such as incandescent bulbs), including low power consumption, high energy efficiency, compact size, and the ability to emit light in specific spectra that make them desirable for a wide range of light purposes. LEDs have been commonly and widely used in the lighting industry. For example, LEDs are used to provide backlighting for displays, such as on TVs, computer monitors, and smartphones.

38. In practice, a control technology well known in the industry as pulse-width modulation (PWM) has been commonly used to achieve the brightness control of LEDs. PWM control of an LED allows one to vary the brightness of an LED by using a fixed current through the LED but turning the LED on and off at frequencies that would be imperceptible to human vision. *See* EX1001, 2:9-18. In effect, rather than changing the actual magnitude of the current through the LED, PWM control changes the average current over time flowing through the LED by turning the LED on and off for various amounts of time. *See id.* The percentage of time that the PWM signal is “on” in a period is referred to as a “duty cycle.” As an example, during a period, T , the LED may be turned on 60% of the time and off for the remaining 40%, and the duty cycle is 60%. The average current flowing through the LED is 60% of the fixed current, and the human eye would perceive the LED to be

at about 60% of the peak brightness. One benefit of PWM control of an LED to vary the brightness is that this method provides better color control. This is due to a color shift that is exhibited in many LEDs when the actual magnitude of the current through the LED is varied.

B. Overview of the '148 Patent

39. The '148 Patent is directed to an LED driver for driving LEDs connected in parallel, using staggered PWM brightness control signals. EX1001, Abstract. Fig. 4 (reproduced below with annotations) depicts an LED driver 50 for controlling three strings of parallelly connected LEDs. EX1001, Fig 4 (annotated).

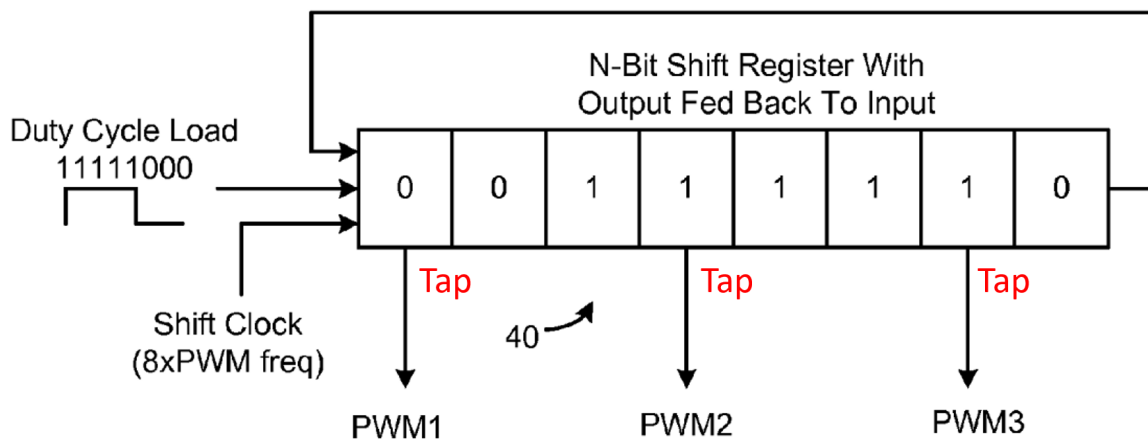


The LED driver 50 comprises a voltage source (highlighted yellow) connecting to the strings of LEDs at the anode end of the LEDs; three current set circuits 56-58

(highlighted green), each connected to one string of LEDs at the cathode end of the LEDs; and a PWM brightness control unit 40/46 (highlighted blue) outputting three associated staggered PWM signals, PWM1, PWM2, PWM3, fed to current set circuits 56-58, respectively. *Id.* at 5:12-58. All three strings of LEDs are energized by the same voltage provided by the voltage source, which includes a DC voltage regulator controller 52 and switching transistor and output circuit 54 for increasing or decreasing the voltage added to the anode end of the LEDs. *Id.* at 5:26-47. The PWM brightness control unit 40/46 and the current set circuits 56-58 together determine how much current each string of LEDs can draw at a certain moment, thereby achieving the dimming control of each string of LEDs. *Id.* By providing staggered PWM signals, PWM1-PWM3, to the current set circuits 56-58, different strings of LEDs are switched on and off at different times. *Id.*

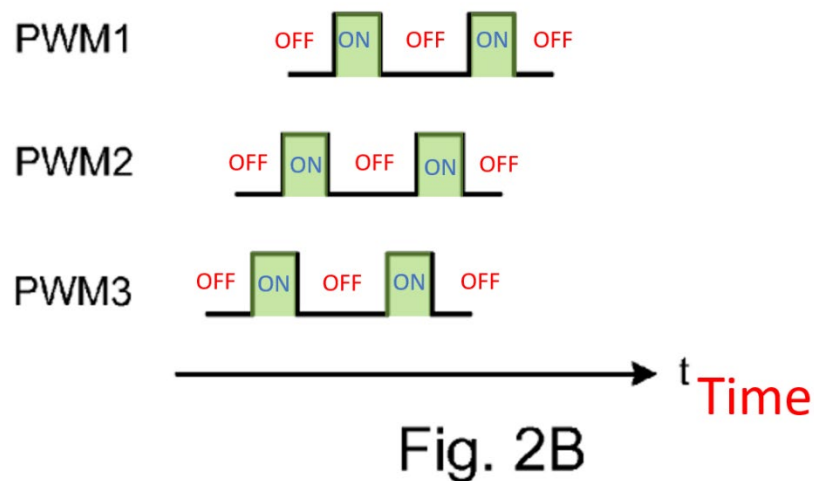
40. The '148 Patent discloses using a shift register to generate the staggered signals PWM1-PWM3. *Id.* at Figs. 2A and 2B; 3:45-51, 4:3-64. A shift register is circuit with an array of flip-flops for holding a pattern of bits (0's and 1's) and connected such that when they are driven by a clock, the pattern of bits is shifted over by one bit location. *See* EX1008, 525; EX1011, 114; EX1010, 1:12-35. While a shift register, by circuit design, can shift bits in an input pattern from left to right or right to left, most commonly, a shift register will be designed to shift bits from left to right so that its output is the value of its right-most-bit. EX1011. In the '148

Patent, a PWM signal is generated by converting the output of the shift register into a signal with high- and low-states corresponding to the 1's and 0's. EX1001, 4:13-30. Fig. 2A shows an 8-bit shift register 40 capable of shifting a bit from left to right. *Id.* at 4:13-30, Fig. 2A (annotated below). When a shift clock signal is applied, it causes the shift register 40 to shift each bit in a Duty Cycle Load input (for example, “11111000”) to the next location to its right. *Id.* As such, the shift register 40 writes in, stores, and shifts a sequence of input in time in its eight positions. *Id.* The '148 Patent further connects the eighth bit to the first bit of the shift register 40 so that the eighth bit is shifted out of the last position to its first position for recirculation. *Id.*

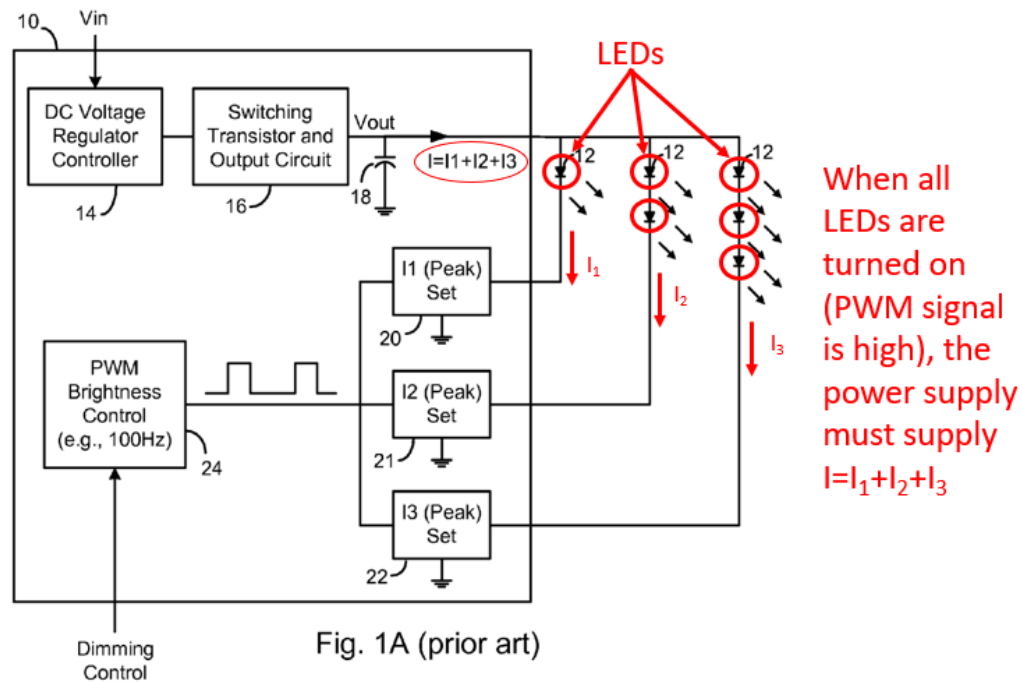


The '148 Patent discloses the use of taps at different positions of the shift register 40 to generate output PWM signals, PWM1, PWM2, PWM3. *Id.* at 4:43-54. Tapping different locations along the shift register produces output signals that have the same

overall shape as the input signal, but are shifted in time as the bits are shifted through the shift register, as shown in the example below. *See id.* at Fig. 2B (annotated).



41. The '148 Patent purports to solve a problem of “voltage ripple(s)” in the power supply caused by instantaneous large current changes produced when changing the brightness of LEDs using prior art LED drivers. *See* EX1001, 2:41-55. The '148 Patent illustrates the problem with the admitted prior art in Figure 1.



EX1001, Fig. 1 (annotated). In the prior art LED driver, when all the LEDs are driven in parallel simultaneously with the same PWM signals, the combined currents through all of the LEDs when they are turned “on” can be high. See EX1001, 2:43-47.

42. The '148 Patent explains that by using staggered PWM signals, not all of the LEDs would be turned on at the same time. EX1001, 2:65-67. Figure 2B, annotated below, shows an example of three PWM signals that are staggered such that the high states of the PWM signal (labeled as “ON,” below) occur at different times relative to each other. In fact, the '148 Patent explains that Figure 2B is a special case where the duty cycle is “low enough” such that “no high state PWM signal overlaps with another high state PWM signal, so the maximum current

supplied by the power supply is the highest current in any one LED path.” *Id.* at 4:58-62. However, the patent also explains that “[i]f the driver drives many parallel paths, some paths may be driven in phase and other paths driven out of phase.” *Id.* at 4:63-64. In other words, some of the high (ON) states of staggered PWM signals may overlap while others do not. The ’148 Patent touts the reduction in noise and artifacts, improvement in the color output of the LEDs, and the ease of constraints on the power supply as advantages associated with an LED driver that staggers PWM brightness control signals provided to different parallel LED strings. *Id.* at 4:1-13.

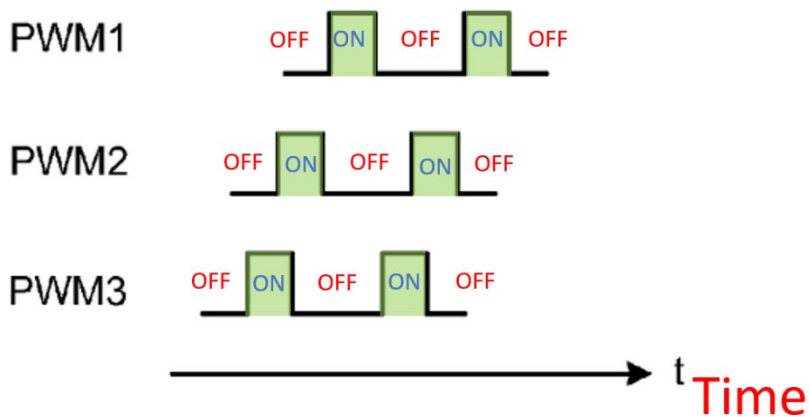


Fig. 2B

EX1001, Fig. 2B (annotated).

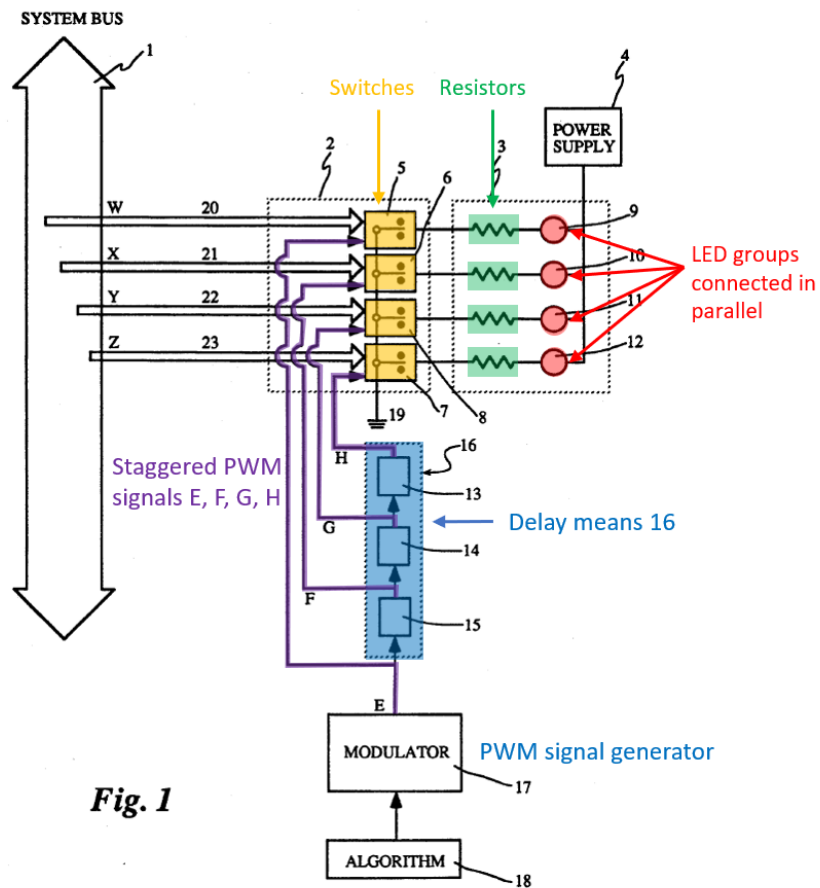
C. Prosecution History of the '148 Patent

43. The '148 Patent issued from a patent application, No. 12/099,729, filed on April 8, 2008. The USPTO allowed the claims with an amendment addressing a typo and claim renumbering. EX1002, 48, 52.

VII. OVERVIEW OF THE PRIOR ART

A. U.S. Patent No 5,317,307 to Thomas, Jr. (“Thomas”) (EX1005)

44. Thomas is a U.S. patent issued in 1994. I understand that Thomas is prior art because it issued more than one year prior to the application filing date of the '148 Patent. Thomas discloses a “method and apparatus for power demand load leveling of a power supply driving a plurality of LED’s through the use of pulse width modulation.” EX1005, Abstract. As shown in Fig. 1 of Thomas, a power supply 4 is added to LED groups 9-12 connected in parallel, each of which is then coupled through a resistance to an activation switch (5-7) that is controlled by modulator 17. *Id.* at 3:24-45. The modulator 17 is a PWM signal generator whose output *E* is determined by an algorithm 18. *Id.* at 3:46-63. The output *E* is then fed to a delay means 16 to generate staggered PWM signals *F*, *G*, *H*. *Id.* at 3:64-4:17.



EX1005 at Fig. 1 (annotated).

45. Fig. 3 of Thomas shows that *F*, *G*, and *H* are time-shifted based on *E*. Accordingly, *E*, *F*, *G*, *H* are staggered in time or out-of-phase with each other. See EX1005 at Fig. 3.

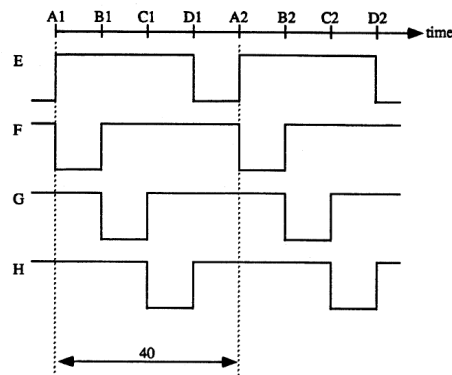


Fig. 3

B. Montu Doshi & Regan Zane, “Digital Architecture for Driving Large LED Arrays with Dynamic Bus Voltage Regulation and Phase Shifted PWM” (“Zane”) (EX1006)

46. *Zane* is a paper that I co-authored with my then-graduate student, Montu Doshi. Dr. Doshi received his Ph.D. a few years later. We presented *Zane* at the 22nd Annual IEEE Applied Power Electronics Conference and Exposition, which was held between February 25, 2007 to March 1, 2007 in Anaheim, California (“APEC 07”). APEC is the premier annual IEEE conference and industry exposition attended by power electronics professionals, including engineers who design LED drivers, power supplies, DC-DC converters, electrical motors, and other power electronic circuits. This conference is held yearly, and I have helped to organize several of these conferences. Based on my personal knowledge, I know that each conference has at least one thousand registered attendees. It is my understanding from discussions with the program chair that over 2,500 people registered and attended APEC 07. I recall from the large industry exhibit at the 2007 conference

and the conference sessions that major players in the industry were in attendance at APEC 07, including for example, Analog Devices, Delta Electronics, Fairchild Semiconductor, International Rectifier, National Semiconductor, NXP (Philips), STMicroelectronics, and Texas Instruments. EX1019 is a true and correct copy of the exhibitor list from APEC 07.

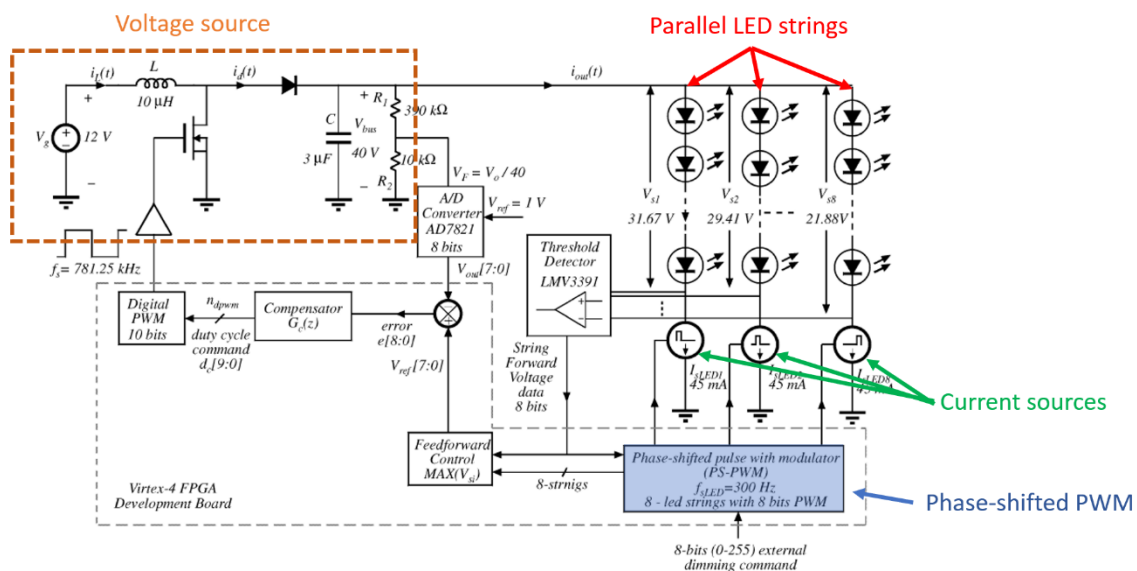
47. We submitted a digest summarizing the *Zane* paper to APEC 07 in August 2006, and we submitted the full paper in its final published form to APEC 07 in December 2006. EX1016 is a true and correct copy of the digest that we submitted in August 2006. The *Zane* paper was then published in the conference proceedings and distributed in electronic form to all registered attendees on the first day of the conference on February 25, 2007. As a result, over 2,500 registered attendees of APEC 07 (including myself) would have received a compact disk (CD) that stored the electronic form of all conference papers (including the *Zane* paper) between February 25, 2007 to March 1, 2007. In addition to distribution of the *Zane* paper in electronic form to all registered attendees, it would have been my typical practice to bring hard copy prints of my paper with me to the conference to distribute to attendees. Our presentation on *Zane* was presented on February 27, 2007 in a session titled “Lighting” that was well-attended by around a few dozen conference attendees. EX1017 is a true and correct copy of the Table of Contents from the APEC 07 conference proceedings, which were available to attendees during the

conference, showing that Dr. Doshi and I presented the *Zane* paper during the February 27, 2007 session. *See* EX1017. EX1018 is a true and correct copy of the presentation slide deck that we presented at APEC 07 when we presented the *Zane* paper. The footer in EX1018 shows that it corresponds to *Zane* based on overlapping language with the title of *Zane*. The session was chaired by Jim Templeton from Zilker Labs, a startup company developing digital power IC solutions that was acquired in 2008 by Intercil, a Renesas company that provides power solutions to a wide range of applications, including LED drivers, lighting and control. The session was dedicated to power electronic solutions in lighting applications and included papers co-authored by power electronics professionals from major companies in the field including International Rectifier and Delta Power Electronics. The conference included another session dedicated to lighting with papers on LED drivers co-authored by International Rectifier and Philips Research Europe.

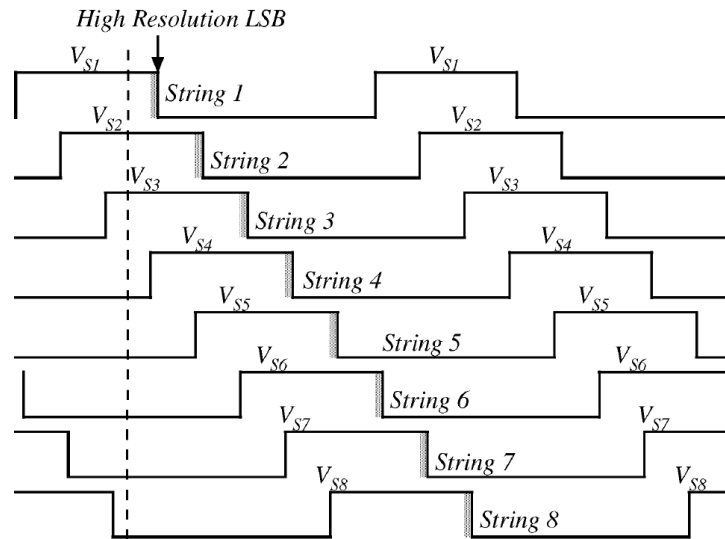
48. Accordingly, I understand that *Zane* is prior art to the '148 Patent because it was published and made available to conference attendees at APEC 07 more than one year before the date of application for the '148 Patent. I also understand that *Zane* is prior art to the '148 Patent because it was published before the inventions claimed in the '148 Patent.

49. *Zane* discloses a “Digital Architecture for Driving Large LED Arrays with Dynamic Bus Voltage Regulation and Phase Shifted PWM.” EX1006, Title.

As shown in Fig. 3 of *Zane*, a voltage source comprising a boost converter is applied to power the arrays of parallel high-brightness LED strings. EX1006, 290-291. The brightness of the LED strings is controlled by regulating the current flowing through the LED strings using linear current sinks with phase-shifted PWM control. *Id.* at 287-289.



EX1006, Fig. 3 (annotated). The phase-shifted PWM signals disclosed by *Zane* are staggered. As illustrated in Fig. 2A of *Zane*, in an example of the phase shifted PWM signals for eight strings of LEDs at a 40% dimming command, only three out of the eight LED strings are on at a given time.



EX1006, Fig. 2A.

C. U.S. Patent No. 6,402,354 (“Tatewaki”) (EX1007)

50. U.S. Patent No. 6,402,354 is titled “Indirect Lighting System for Vehicle Interior” and was issued to Tatewaki et al. on June 11, 2002. I understand that Tatewaki is prior art because it issued more than one year before the April 8, 2008 filing date of the ’148 Patent. Tatewaki describes an LED roof lamp for a car and discloses that the LED is driven by a PWM control circuit. *See, e.g.*, EX1007, Abstract, 11:52-13:47, 12:11-31. Tatewaki also explains that the PWM control circuit uses a ring counter which controls the brightness of the LED. *See id.* at 13:26-47.

D. Applicant Admitted Prior Art (“AAPA”) (EX1001)

51. I understand that a patent applicant may admit that certain features were known in the prior art and that such admissions may be considered in an obviousness

analysis, for example, to disclose a claim limitation or to explain the knowledge of a POSITA at the time of the invention. The '148 Patent describes Figures 1A and 1B as “prior art.” *See, e.g.*, EX1001, 3:41-44 (“FIG. 1A illustrates a prior art LED driver, driving LEDs connected in different parallel paths. FIG. 1B illustrates a prior art PWM brightness control signal generator.”). Thus, I understand that Figures 1A and 1B and the related description about those figures in the '148 Patent are applicant admitted prior art. The '148 Patent admits, for example, that step-up or step-down voltage regulators were “well known and need not be described in detail,” among other admissions. *See* EX1001, 1:46-60 (describing step-up and step-down voltage regulators), *see also id.* at 1:11-2:55 (describing the prior art). The '148 Patent also explains that the duty cycle of a PWM signal used to control LEDs determines the average current through the LEDs. *See id.* at 2:7-18.

E. Paul Horowitz & Winfield Hill, *The Art of Electronics* (2nd ed. 1989) (EX1008)

52. *The Art of Electronics* is a textbook on electronic circuit design that has a publication date of 1989. EX1008 is a scanned excerpt of a copy of this textbook from the University of Wisconsin-Madison Library, and I understand this textbook was available to library patrons at least as early as September 27, 1989. *See* EX1009. Based on this information, I understand that *The Art of Electronics* is a publicly available printed publication and prior art to the '148 Patent.

F. Noel Morris, *Digital Electronic Circuits and Systems* (1974) (“Morris”) (EX1011)

53. *Digital Electronic Circuits and Systems* is a textbook on electronic circuit design that has a publication date of 1974. EX1011 is a scanned excerpt of a copy of this textbook from the Idaho State University Library. The library check-out slip inside this copy of the textbook shows that it was checked out by library patrons as far back as January 1977. See EX1011, 2. Based on this information, I understand that *Digital Electronic Circuits and Systems* is a publicly available printed publication and prior art to the '148 Patent.

VIII. GROUND FOR UNPATENTABILITY

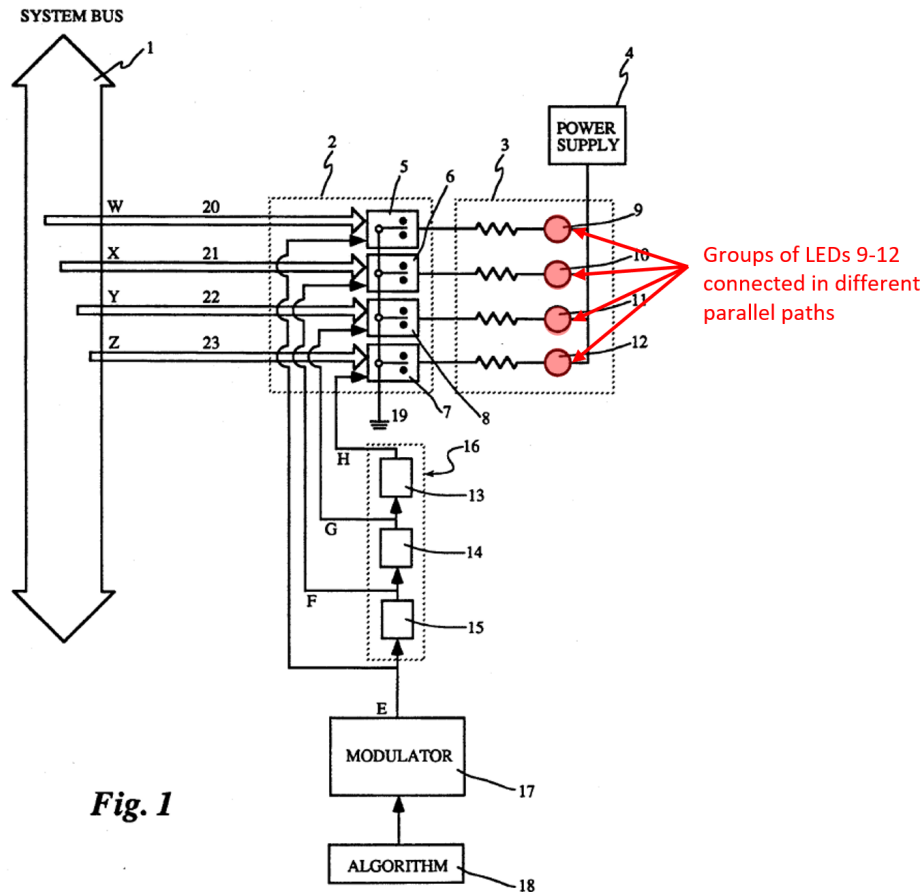
A. Ground 1: Claims 1, 3, 7, 9, 10-12, 14, 17, 18, and 20-22 Are Anticipated By Thomas

1. Claim 1 Preamble: “A light emitting diode (LED) driver for driving LEDs connected to different parallel paths,”

54. It is my opinion Thomas discloses the preamble. Thomas teaches “a method and an apparatus for power demand load leveling of a power supply driving a plurality of LED’s through the use of pulse width modulation.” EX1005, Abstract.

55. As shown below in Fig. 1, Thomas discloses four groups of LEDs (9-12), each group connected to a power supply 4 at one end and ground 19 at the other end through a resistance and a PWM controlled activation switch (5-8). EX1005,

Fig. 1, 3:24-32. Also, as shown in Figure 1, the LED groups 9-12 are connected in parallel paths.



EX1005, Fig. 1 (annotated).

56. As further shown in Figure 2, Thomas discloses that each of the four parallel paths shown in Figure 1 further consists of four parallel sub-paths. See EX1005, Fig. 2; 3:32-45. Specifically, Figure 2 shows an expanded view of the parallel path for LED group 9, showing that the LED group 9 consists of four individual LEDs, 34-37, which are connected in parallel.

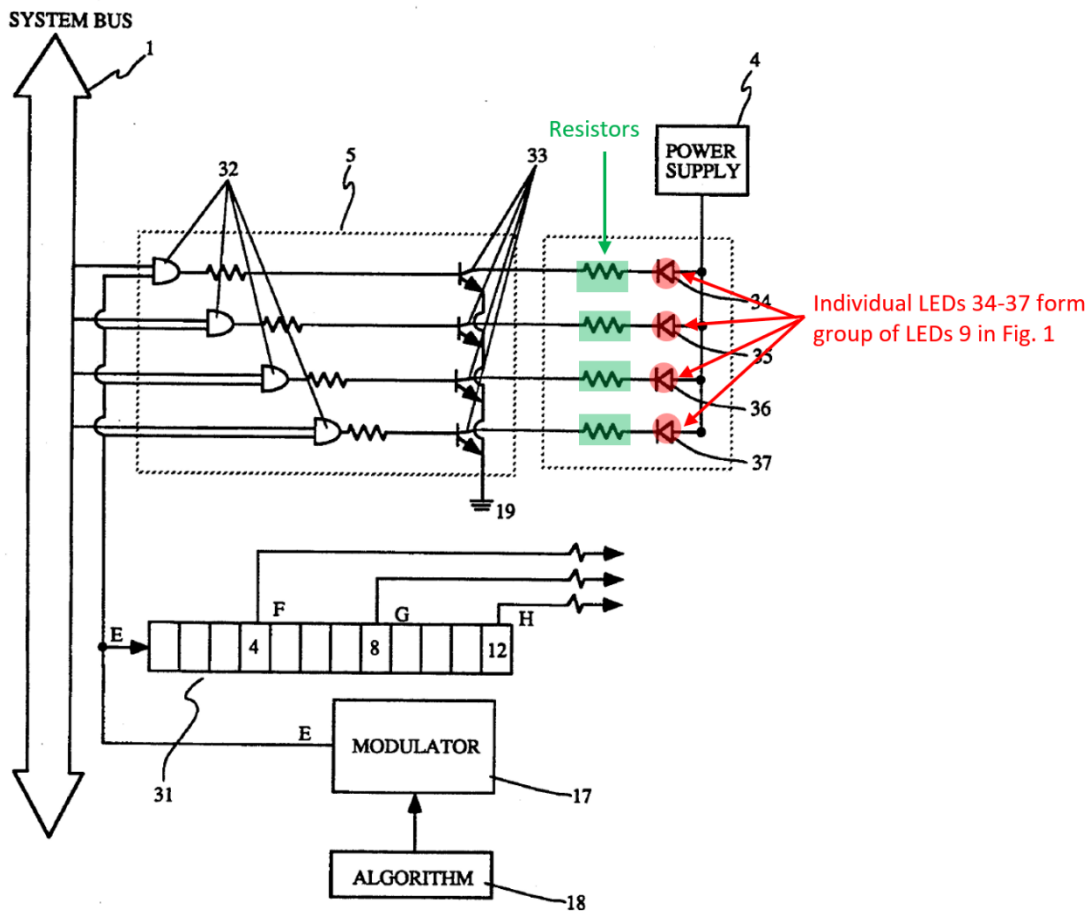
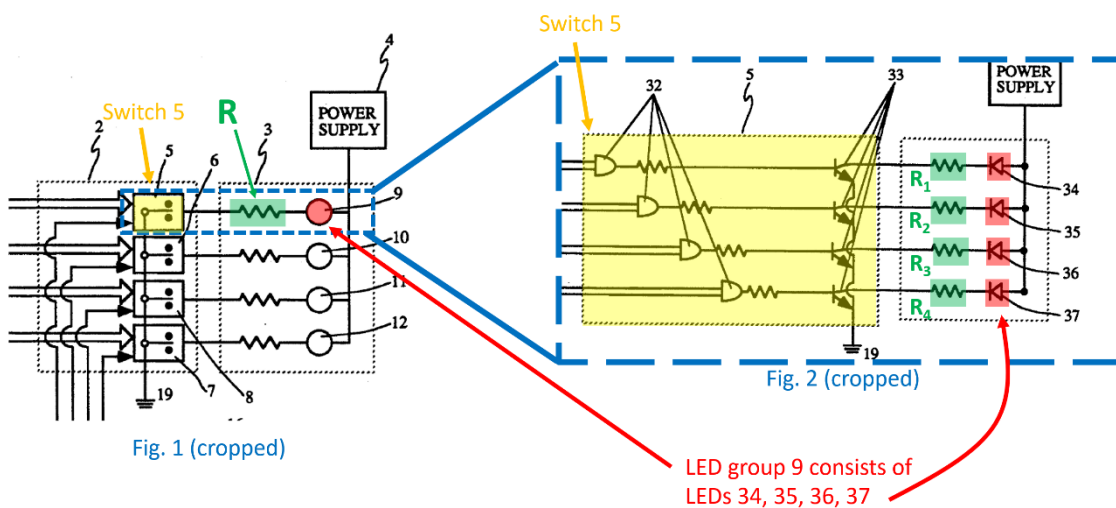


Fig. 2

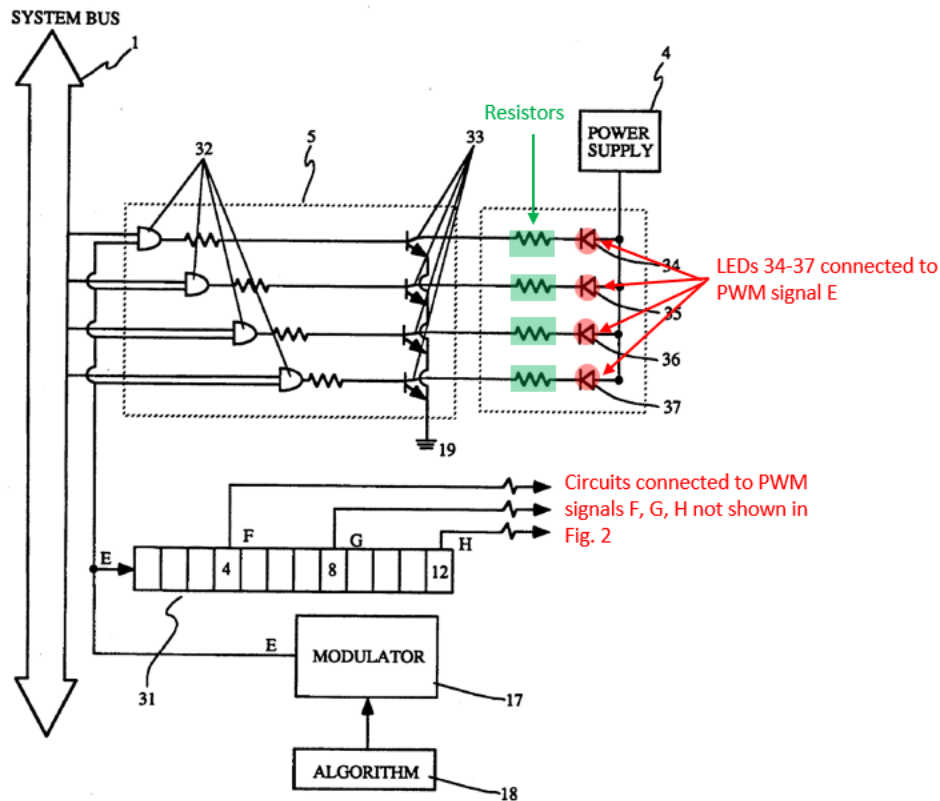
EX1005, Fig. 2 (annotated); *see also id.* at 3:3-5 (“FIG. 2 is a partial circuit diagram of the present invention showing one group of four LED’s with their respective control lines and control devices.”); 3:42-45 (explaining that “group of LED’s (9)” consists of “associated LED’s (34-37)”). Thomas further describes Figures 1 and 2 together, explaining for example that the switch 5 shown in Figure 1 “is comprised of gating control logic (32) forming AND gates and transistors (33) for activating one group of LED’s (9).” EX1005, 4:32-35. Thus, a POSITA would have

understood that Figure 2 is an expanded circuit diagram illustrating how the higher-level circuit diagram shown in Figure 1 is implemented.

57. The annotated figures below further clarify how Figure 2 expands on the details of the implementation of the circuit in Figure 1. As shown below, the LED group 9 (red) in Figure 1 actually consists of the four LEDs 34-37 connected in parallel in Figure 2, and the resistor (labeled R and highlighted green) in Figure 1 actually consists of four resistors R_1 - R_4 , each of which is connected to one of the four individual LEDs 34-37. The four sub-paths shown in Figure 2 are all connected via AND gates to the PWM signal E . Additionally, Thomas explains that the activation switch 5 (highlighted yellow in Figure 1, below) “is comprised of gating control logic (32) forming AND gates and transistors (33)” (also highlighted yellow in Figure 2, below).



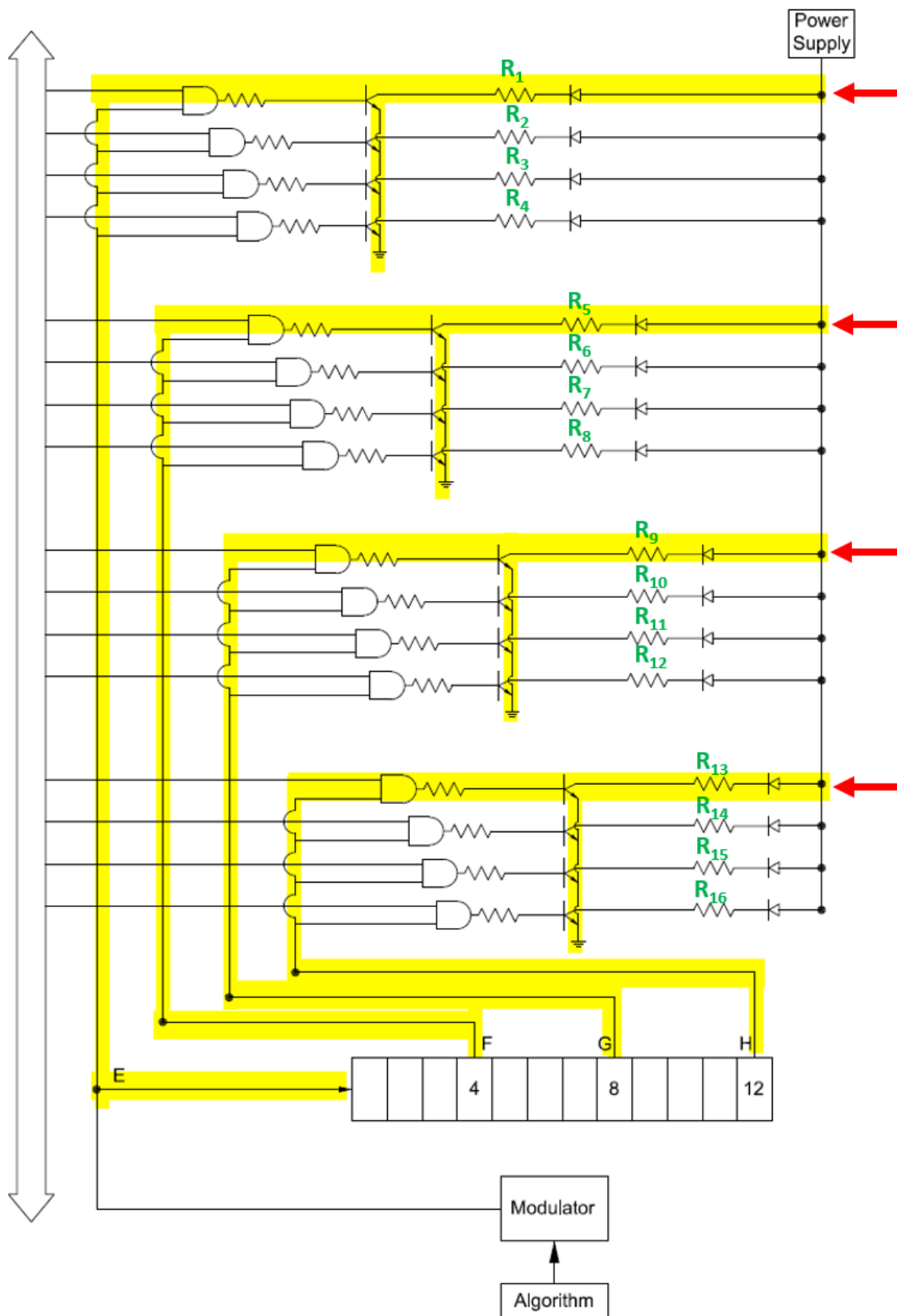
EX1005, Figs. 1 and 2 (cropped and annotated). The sub-paths that are connected to the other staggered PWM signals *F*, *G*, and *H* are not shown in Figure 2.



EX1005, Fig. 2 (annotated).

58. While not shown in Figure 2, Thomas explains that “[i]n the preferred embodiment of the present invention, each group of LED’s (9-12) consists of twenty five percent of the total LED’s in the array.” EX1005, 5:11-13. Thus, Thomas discloses an LED driver where there are $4 \times 4 = 16$ parallel sub-paths with 16 resistors and 16 LEDs. Thus, four LEDs are connected in parallel and connected to PWM

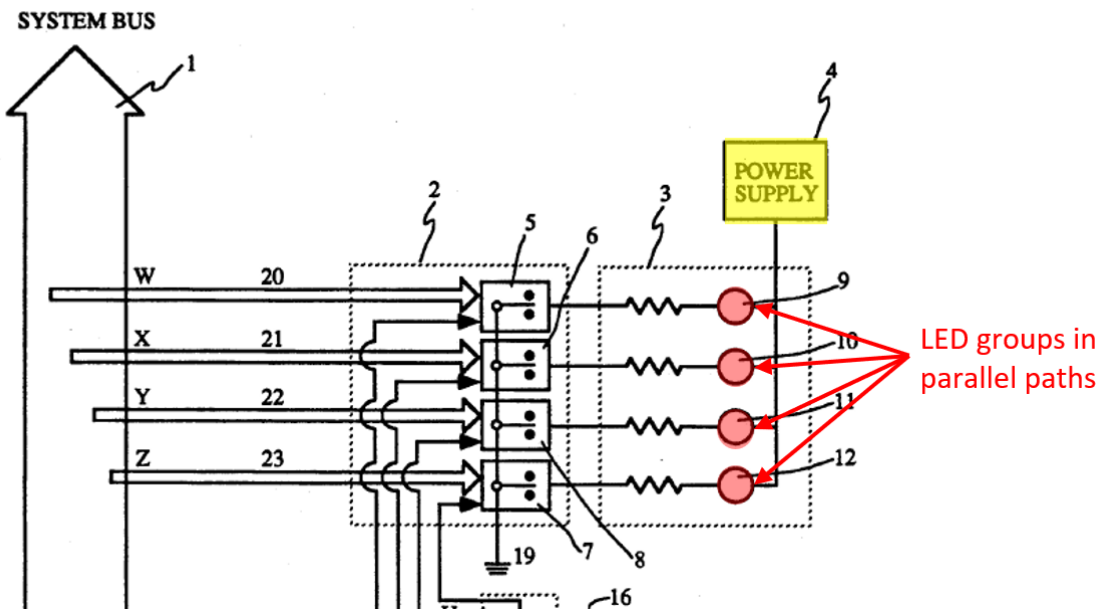
signal *E*, another four LEDs are connected in parallel and connected to PWM signal *F*, and so on and so forth for PWM signals *G* and *H*. The drawing below illustrates how a POSITA would have understood Thomas' Figure 2 circuit if all of the parallel paths connected to *F*, *G*, and *H* were drawn.



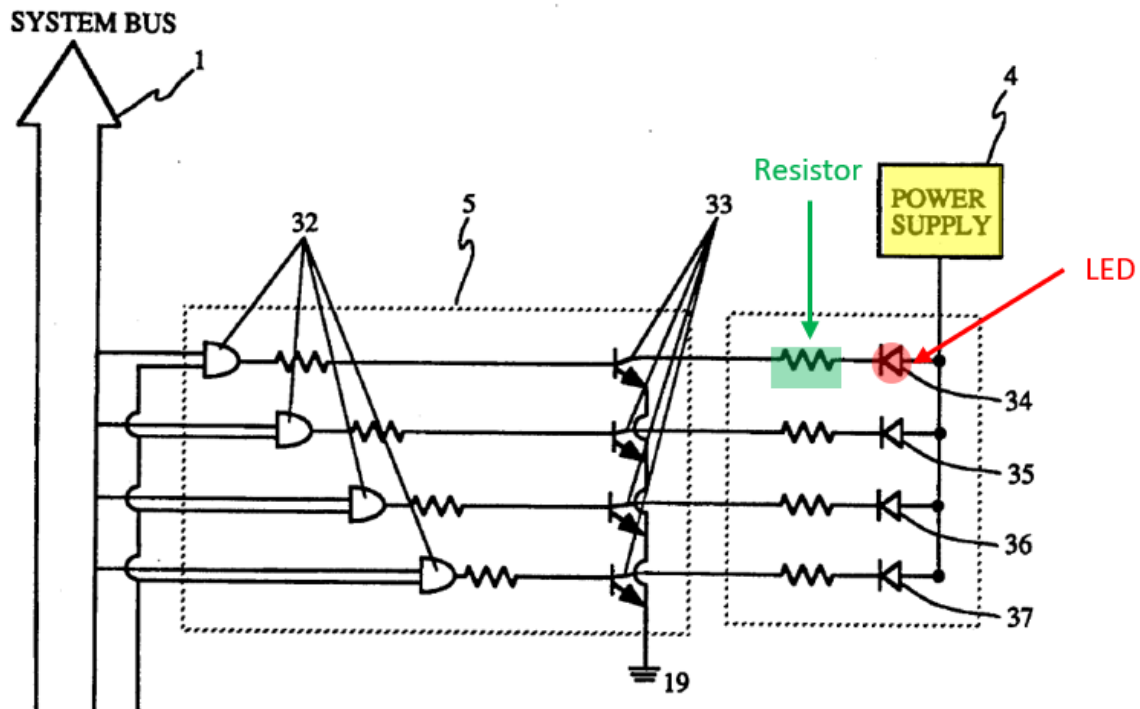
59. For purposes of my analyses, I have focused on four of the sixteen total sub-paths. Specifically, I have focused on one sub-path connected to each of the PWM signals *E*, *F*, *G*, and *H*. For example, I have labeled the resistors in the 16 parallel sub-paths as R_1 - R_{16} , where R_1 - R_4 are connected to the PWM signal *E*, R_5 - R_8 are connected to PWM signal *F*, R_9 - R_{12} are connected to PWM signal *G*, and R_{13} - R_{16} are connected to PWM signal *H*. My analyses are focused on the sub-paths with resistors R_1 , R_5 , R_9 , and R_{13} as the parallel paths recited in the '148 Patent claims. Those paths are highlighted yellow and identified with a red arrow in the figure above. The '148 Patent claims do not exclude the possibility of additional parallel paths of LEDs that are controlled by each of the PWM signals. Additionally, in my analyses, I may refer to the parallel paths shown in Thomas' Figure 1. It should be understood that when I am referring to one of the parallel paths in Figure 1, I am referring to one of the four parallel sub-paths that comprise that parallel path.

a. Limitation 1[a]: “the driver comprising: a voltage source for connection to first ends of LEDs in a plurality of parallel paths”

60. As shown below in Figs. 1 and 2, Thomas discloses a power supply 4 (highlighted yellow below) connected to the anodes of the LEDs in the parallel paths to add a voltage to power the LEDs.



EX1005, Fig. 1 (cropped and annotated).



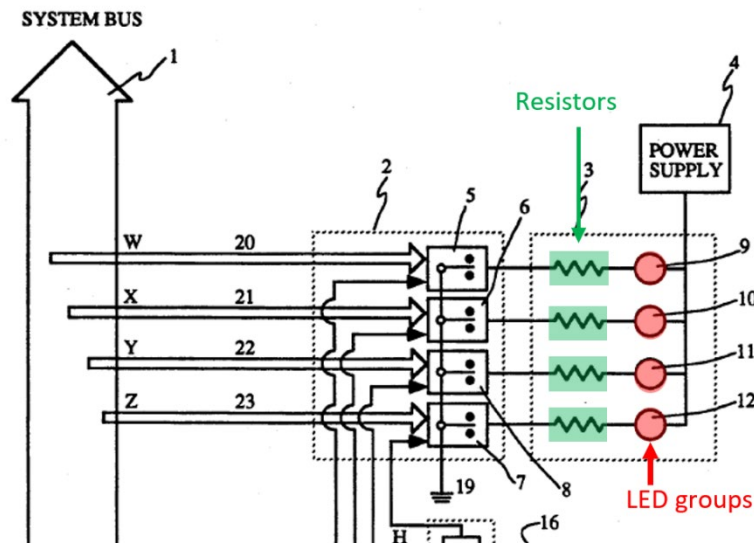
EX1005, Fig. 2 (cropped and annotated).

61. A POSITA would have understood, and Thomas confirms, that a power supply is a voltage source.¹ See EX1005, 1:66-2:10 (explaining one problem with prior art LED drivers is that a power supply “may have severe difficulty in maintaining a regulated voltage” when rapidly activating a large number of LEDs at the same time and that Thomas’ invention “reduces the magnitude of the instantaneous change in the current demand on the power supply such that a more stable output voltage can be maintained”). It is my opinion that Thomas discloses this limitation.

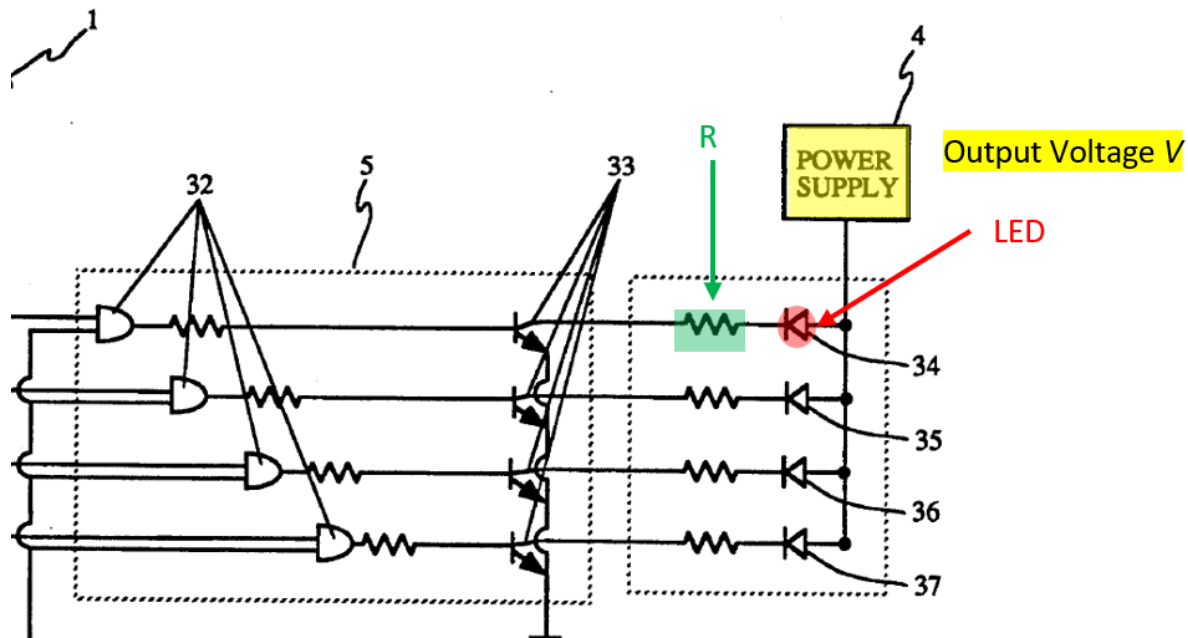
- b. Limitation 1[b]: “a plurality of current set circuits, one current set circuit per parallel path, each current set circuit controlling a peak current through one or more LEDs connected in each parallel path”; and**

62. Thomas discloses a resistor in series with the LEDs in each of the parallel paths, as shown below in Figures 1 and 2.

¹ Based on my review of Patent Owner’s infringement contentions, I also understand that Patent Owner contends that a power supply satisfies the voltage source limitation. See EX1015.



EX1005, Fig. 1 (cropped and annotated).



Id. at Fig. 2 (cropped and annotated).

63. A POSITA would have understood that the function of the resistors, highlighted green above, is to set the current flowing through the LEDs to a peak value when the transistor switch in their path is turned on. This is because the power

supply provides a voltage, the LEDs when they are turned on create a relatively constant voltage drop across them, and the transistors when operated as described in Thomas act as on/off switches with approximately zero voltage across them. Thus, only the resistor in the LED current path acts to set the current. Specifically, if the power supply outputs a voltage V , the LED has a voltage drop of V_{LED} , and the resistor has resistance R , and the voltage on the transistor switch when it is turned on is neglected, then the current flowing through the LED that is connected to the resistor has a maximum current of $I=(V-V_{LED})/R$. Note, however, in practice the actual current flowing through the LED may be smaller due to the additional voltage drop on the transistor switch or other parasitic resistances in the circuit. Regardless, a POSITA would have understood that the resistor is limiting the current through the LED to a peak current. Accordingly, Thomas discloses resistors connected in series with the LEDs in each parallel path which are current set circuits configured to control a peak current through the LEDs in each parallel path. It is my opinion that Thomas discloses this limitation.

- c. **Limitation [1.c]: “a pulse-width modulated (PWM) brightness control signal generator connected to the plurality of current set circuits, the brightness control signal generator being configured to generate staggered PWM**

brightness control signals to the plurality of current set circuits”,

64. Thomas discloses a pulse width modulator 17 which generates a PWM signal *E* and outputs *E* to control the on and off status of one of the switches (5) in one of the paths controlling one LED group (9). EX1005, 3:46-63. “The precise wave form of the modulating signal output from the modulator may be determined by the use of an algorithm (18) implemented in either software or hardware as is well-known in the art.” *Id.* at 3:47-51. The PWM signal *E* is also fed to a delay means 16 to generate three signals *F*, *G*, *H*, which are time-delayed versions of the signal *E*. *See id.* at 3:64-4:47. The three time-delayed signals *F*, *G*, *H* are then each outputted to control the on and off status of the switch in the other three paths (6, 8, 7) controlling LED groups (10, 11, 12). *Id.* Thus, the pulse width modulator 17, the algorithm 18, and the delay means 16 together comprise a “pulse-width modulated (PWM) brightness control signal generator connected to the plurality of current set circuits,” as recited in Limitation [1.c]. *See* EX1005, Fig. 1 (annotated).



65. Thomas teaches two ways to implement the delay means 16: (1) configuring a predetermined number of delay elements (13-15), or (2) using a “shift register (31) having taps.” EX1005, 3:68-4:5. Thomas explains that the shift register implementation is the “preferred embodiment” of his invention. *Id.* at 4:17-23. However, both implementations of the delay means 16 disclose Limitation [1.c] because both result in staggered PWM brightness control signals, as discussed below. Thomas explains that the shift register is a 12-bit shift register which generates PWM signals *F*, *G*, and *H*, which are time-delayed versions of the signal *E*. The shift register works by “sequentially storing twelve binary values

corresponding to the pulses or lack of pulses in the first modulating signal (E).” *Id.* Then, the signals *F*, *G*, and *H* are “generated by tapping the values stored within the fourth, eighth, and twelfth cells of the shift register (31) as the values are sequentially shifted through the twelve cells of the shift register (31).” *Id.* at 4:23-28.

66. Additionally, as shown in Figure 3, Thomas discloses that *F*, *G*, and *H* are time-delayed versions of *E*. See EX1005, Fig. 3. As annotated below, the signals *E*, *F*, *G*, and *H* have alternating high and low states. During the high states, the PWM signal would activate, or turn on, the LEDs, while during the low states, the PWM signal would turn off the LEDs. And as shown in Figure 3, the four signals are staggered in time so that the “on” and “off” cycles do not line up exactly in time. Therefore, *E*, *F*, *G*, and *H* are “staggered PWM brightness control signals” which are applied to the plurality of current set circuits.

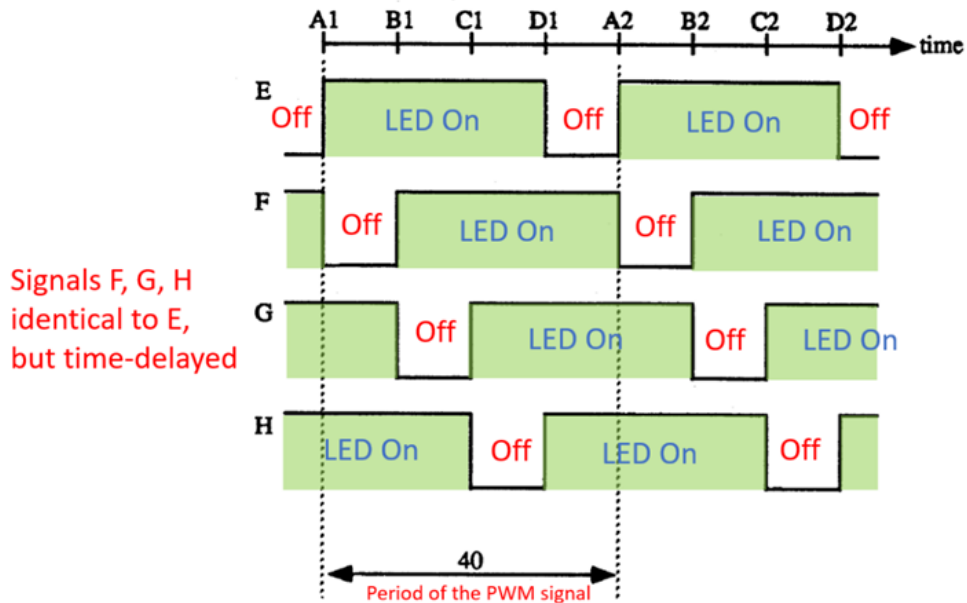


Fig. 3

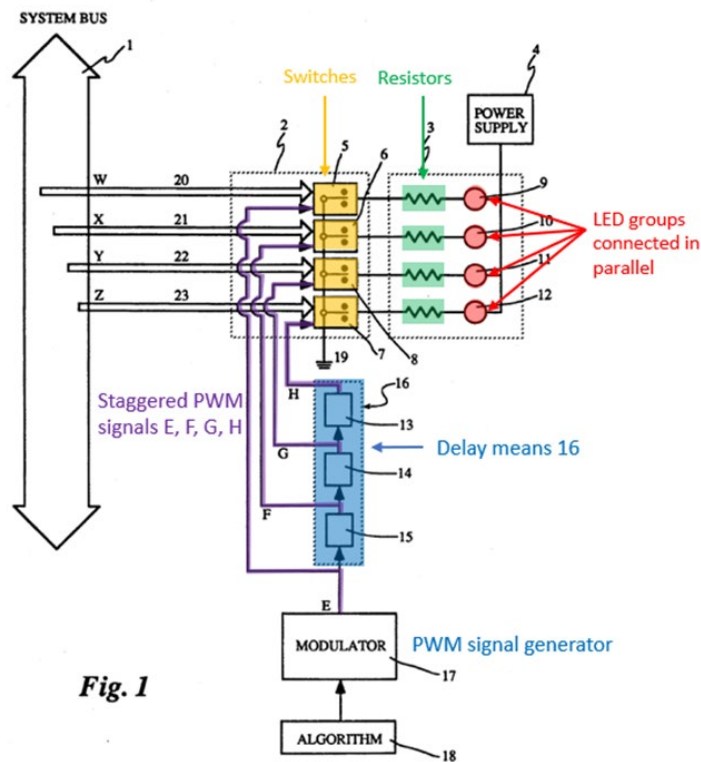
EX1005, Fig. 3 (annotated). And as shown in Figure 1, above, a different one of the staggered PWM signals *E*, *F*, *G*, and *H* are applied to each of the current set circuits corresponding to the LED groups 9, 10, 11, and 12. *See* EX1005, Fig. 1. It is my opinion that Thomas discloses this limitation.

- d. **Limitation [1.d]: “each current set circuit being configured to draw the peak current through its associated one or more LEDs at a duty cycle substantially corresponding to a duty cycle of a PWM brightness control signal applied to it, such that the plurality of current set circuits conduct current through their associated one or more LEDs at the same duty cycle but out of phase with each other.”**

67. As discussed with respect to Limitation [1.b] above, the resistors in parallel with the LEDs in each parallel path in Thomas set the peak current that flows

through the LEDs in their associated path. Additionally, as discussed below, the current set circuits are configured to draw that peak current at the duty cycle of the PWM brightness control signal (*E*, *F*, *G*, or *H*) that is applied to it.

68. As annotated in Figure 1 below, the staggered PWM signals *E*, *F*, *G*, *H* are fed into activation switches 5, 6, 8, and 7, respectively. A set of control signals *W*, *X*, *Y*, *Z* from system bus 1 are also fed to the activation switches 5-8. EX1005, 3:46-63, 4:66-5:10. A high control signal from *W*, *X*, *Y*, or *Z* in combination with a high pulse from a PWM signal *E*, *F*, *G*, or *H* will turn the LED(s) in the associated path on. *Id.*

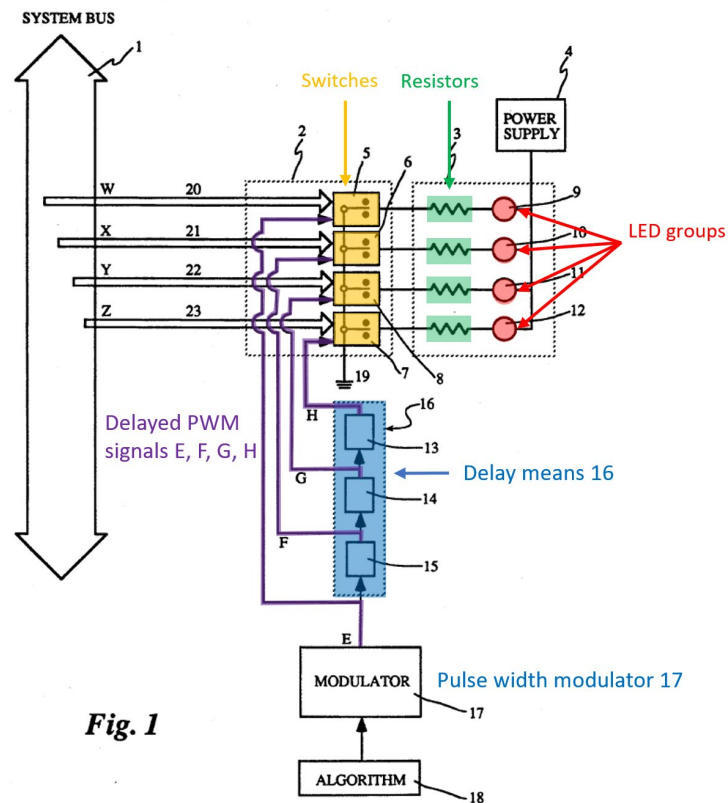


EX1005, Fig. 1 (annotated).

69. A POSITA would have understood that the control signals *W*, *X*, *Y*, and *Z* control whether the LEDs are turned “on” or “off” from the user’s perspective, while the PWM signals *E*, *F*, *G*, and *H* control the perceived brightness of those LEDs. Thomas describes the LED driver in the context of an array of indicator lights on the front panel of a computer. *See* EX1005, 1:12-22. “To light the LED’s in the array, control lines from different processing sections of the computer are carried via a system bus to the LED panel and are connected to the LED’s through transistor switches used for enabling the LEDs.” *Id.* at 1:15-19. Thomas then explains that “[t]o control the intensity of the LED’s within the array, pulse width modulating of the control signals transmitted by the control lines has been used to produce a series of rapid activations of the enabled LED’s.” *Id.* at 1:22-26.

70. Referring back to Thomas’ Figure 1 as annotated above, when the activation switch is turned on and the LED is on, the peak current flows through the path from the power supply 4 to the LED (red), to the resistor (green), and then to the ground (19). When the activation switch is turned off, no current passes through the path, and the LED is turned off. As explained for Limitation [1.c] above, the activation switch is turned on and off by the PWM modulator 17. *See supra* Section VIII.A.1.c. During a duty cycle of the PWM signal, the activation switch is turned on when the PWM signal is at high and turned off when the PWM signal is at low. Thomas explains that “[t]he width of a given pulse in the period of the modulating

signal determines the length of time that the enabled LED's will be activated during the period.” EX1005, 1:36-38. This description refers to the duty cycle of the PWM, which is an expression of how long the PWM cycle is at its high state (or “on” state) in its period.



EX1005, Fig. 1 (annotated). Accordingly, a POSITA would have understood that the resistance in Thomas “draw[s] the peak current through its associated LEDs at a duty cycle substantially corresponding to a duty cycle of a PWM brightness control signal applied to it.” Limitation [1.d].

71. Further, as discussed for [1.c] above, the PWM signals applied to each parallel path, *E, F, G, H*, are identical but staggered. *See supra* Section VIII.A.1.c. As Thomas explained, “[b]ecause the modulating signals (*E, F, G, H*) **vary in phase with respect to each other**, each set of activation switches (5-8) is sequentially turned on by their respective modulating signals (*E, F, G, H*) so that no more than one group of LED’s, comprising twenty five percent of the total LED’s, is activated (or switched on) at any one time.” EX1005, 5:13-20 (emphasis added). Therefore, the activation switches in each path “conduct current through their associated [LEDs] at the same duty cycle but out of phase with each other.” Limitation [1.d]. It is my opinion that Thomas discloses this limitation.

72. For the reasons set forth above, it is my opinion that Thomas discloses every limitation of Claim 1 of the ’148 Patent and therefore anticipates Claim 1.

2. Claim 3: “The driver of claim 1 wherein each current set circuit is a current regulator.”

73. It is my opinion that Thomas anticipates Claim 1, as discussed above. As discussed for Limitation [1.b], Thomas discloses resistors in each parallel path which limit the maximum current flowing through the LED to $(V - V_{LED})/R$. *See supra* Section VIII.A.1.b. A resistor connected in series with the load such as an LED is a basic type of a current regulator because it limits the maximum current flowing

through the load. Accordingly, it is my opinion that Thomas discloses every limitation of Claim 3 and anticipates Claim 3.

3. Claim 7: “The driver of claim 1 wherein the PWM brightness control signal generator comprises:”

74. It is my opinion that Thomas anticipates Claim 1, as discussed above.

See supra Section VIII.A.

a. Limitation [7.a]: “a shift register storing bits corresponding to a PWM duty cycle of a brightness control signal, the shift register having bit positions;”

75. As mentioned in my discussion for Limitation [1.c] above, Thomas discloses using a shift register 31 as the delay means 16 for generating staggered PWM signals. *See supra* Section VIII.A.1.c.; EX1005, Fig. 2, 3:68-4:4:5, 4:17-32.

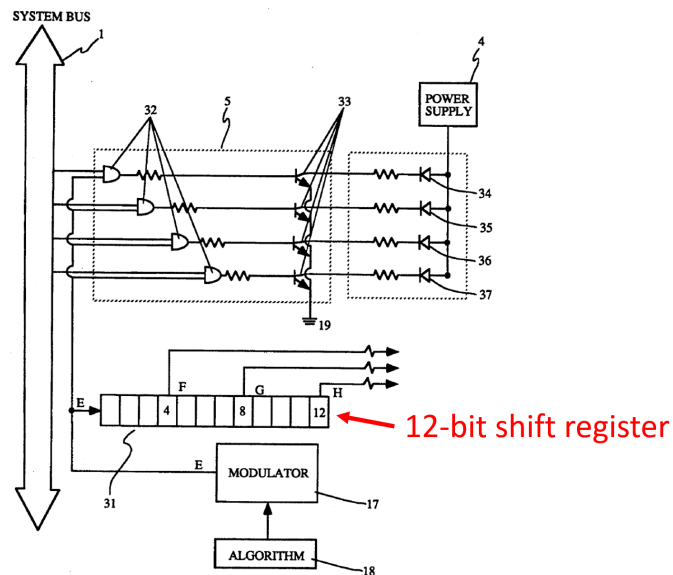


Fig. 2

EX1005, Fig. 2 (annotated). Specifically, Thomas’s shift register 31 has 12 bit positions. EX1005, Fig. 2, 4:17-32. Thomas discloses that the shift register stores bits corresponding to the PWM duty cycle of the brightness control signal, *E*. See EX1005, 3:46-63, 4:17-23 (“[A] twelve bit shift register (31) is used to generate the delayed modulating signals (F, G, H) by sequentially storing twelve binary values corresponding to the pulses or lack of pulses in the first modulating signal (E).”). It is my opinion that Thomas discloses this limitation.

b. Limitation [7.b]: “a clock connected to the shift register for shifting the bits along the shift register”; and

76. Thomas discloses a clock through its disclosure of a “time delay” for the staggered PWM signals *E*, *F*, *G*, and *H*. See EX1005, 4:33-39. Thomas explains that a shift register is used to generate the delayed modulating signals *F*, *G*, and *H*. The reference to a time delay means there is a clock connected to the shift register. Additionally, Thomas’ disclosure of a shift register inherently discloses a clock that is connected to the shift register for shifting the bits along the shift register. Note, in this context, a “clock” is not an analog or digital clock for telling time, but rather an electronic circuit that can output a current or voltage pulse at predictable times. By definition, all shift registers must receive a clock signal to shift the bits. This is necessary to sequentially shift binary values through the cells of a shift register, as described in Thomas. See EX1005, 3:46-63, 4:17-23 (“[A] twelve bit shift register

(31) is used to generate the delayed modulating signals (F, G, H) by sequentially storing twelve binary values corresponding to the pulses or lack of pulses in the first modulating signal (E).”).

77. This understanding is confirmed by textbooks in the field of electronics. For example, *The Art of Electronics* (2d ed.) explains:

If you connect a series of flip-flops so that each *Q* output drives the next *D* input, and all clock inputs are driven simultaneously, you get what’s called a “shift register.” At each clock pulse the pattern of 0’s and 1’s in the register shifts to the right, with the data at the first *D* input entering from the left.

EX1008, 525. As also discussed in another electronics textbook, *Digital Electronic Circuits and Systems*: “A register is simply an array of flip-flops used for the storage of binary data, and a shift register is one which is designed so that the data may be ‘shifted’ along the register in either direction, that is, either to the right or to the left.” See also EX1011, 114-116 (explaining how the bits in a shift register are shifted by a clock pulse). Without a clock, a shift register would not be considered a shift register because it cannot shift the bits. Instead, it would merely be a “register” for storing bits. *Id.*

78. Therefore, Thomas' disclosure of a shift register means that a clock is necessarily present to shift the bits along the shift register. It is my opinion that Thomas discloses this limitation.

c. Limitation [7.c]: “taps off the shift register coupled to different bit positions of the shift register, each tap providing a different staggered PWM brightness control signal connected to an associated current set circuit.”

79. Thomas discloses “taps off the shift register coupled to different bit positions of the shift register.” Limitation [7.c]. As described in Thomas and shown in Figure 2, Thomas discloses taps off the shift register coupled to the fourth, eighth, and twelfth-bit positions to generate modulating signals *F*, *G*, *H*:

[A] twelve bit shift register (31) is used to generate the delayed modulating signals (*F*, *G*, *H*) by sequentially storing twelve binary values corresponding to the pulses or lack of pulses in the first modulating signal (*E*). *The second, third and fourth modulating signals (F, G, H) are then generated by tapping the values stored within the fourth, eighth and twelfth cells of the shift register (31) as the values are sequentially shifted through the twelve cells of the shift register (31).*

EX1005, 4:17-28 (emphasis added).

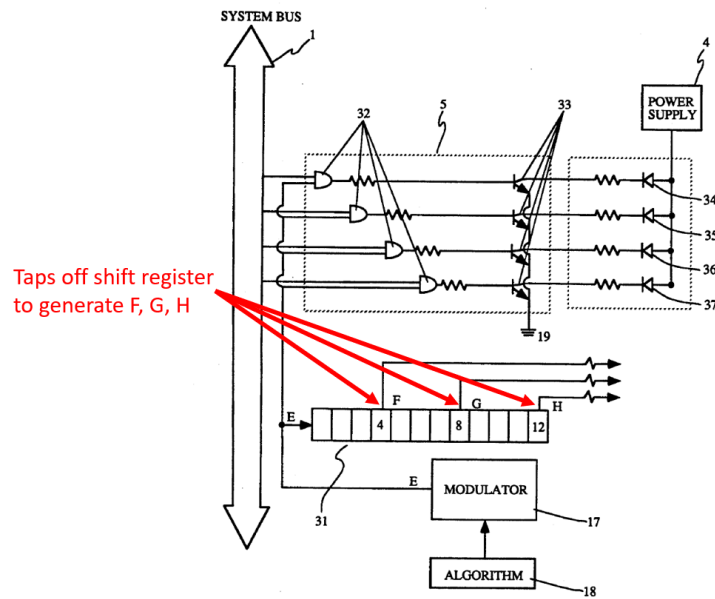
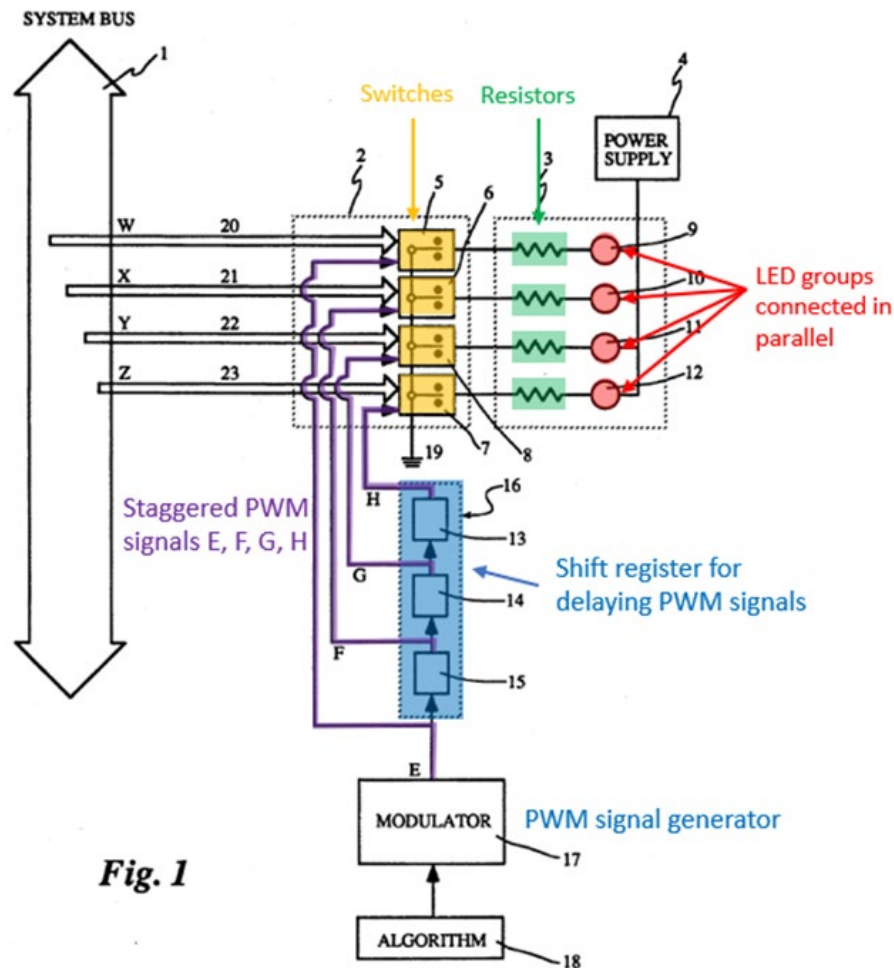


Fig. 2

EX1005, Fig. 2 (annotated).

80. As further shown in Figure 1, the time-delayed PWM signals *F*, *G*, *H* are inputted to the switches and then connected to the current set resistors in their associated parallel LED paths.²

² Figure 1 is drawn with delay elements 13-15, but Thomas' specification expressly states that the delay means 16 may be implemented as a shift register with taps, as illustrated in Figure 2. *See* EX1005, 3:68-4:5.



EX1005, Fig. 1 (annotated). It is my opinion that Thomas discloses this limitation.

Accordingly, Thomas anticipates Claim 7.

4. **Claim 9: “The driver of claim 7 wherein the bits corresponding to a PWM duty cycle of a brightness control signal are serially and continuously loaded into a first bit position of the shift register, then shifted by the clock.”**

81. As set forth above, Thomas discloses all of the limitations in Claim 7.

See supra Section VIII.A.3. Further to the above discussion for Claim 7, Thomas discloses that the shift register “generate[s] the delayed modulating signals (F, G, H)

by ***sequentially*** storing twelve binary values corresponding to the pulses or lack of pulses in the first modulating signal (E).” EX1005, 4:17-23 (emphasis added). As shown in Figure 2, the shift register 31 loads each bit of the modulating signal E into the storing bit positions and then shifts each bit to the right. *Id.* at Fig. 2; 4:23-28 (explaining that “the values are sequentially shifted through the twelve cells of the shift register”). Accordingly, Thomas discloses that the bits corresponding to the duty cycle *E* are serially loaded into the first bit position and then shifted by the clock, which as discussed above, is necessarily present in the shift register.

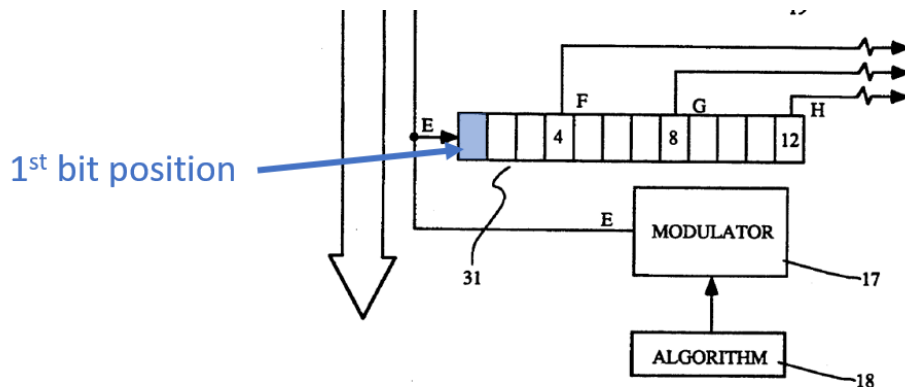


Fig. 2

EX1005, Fig. 2 (cropped, annotated).

82. Further, Thomas discloses that the bits are continuously loaded into the shift register. As shown in Figure 3, the first PWM signal *E* has a period 40 spanning from time A1 to time A2, and the time-delayed PWM signals *F*, *G*, *H* have a period spanning from B1 to B2, C1 to C2, and D1 to D2, respectively.

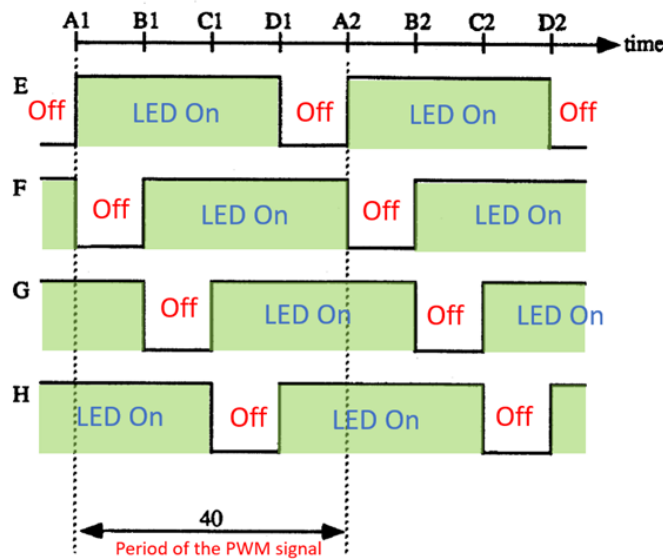


Fig. 3

EX1005, Fig. 3 (annotated), 4:33-65. Figure 3 shows that the signal *E* repeats itself after its period, as do the time-delayed signals *F*, *G*, and *H*. Thomas thus discloses that the shift register is serially *and* continuously loading the bits corresponding to the signal *E* in order to generate the time-delayed signals *F*, *G*, and *H* because the signal is repeating itself. It is my opinion that Thomas discloses this limitation. Accordingly, it is my opinion that Thomas anticipates Claim 9.

5. **Claim 10: “ The driver of claim 7 wherein the clock shifts the bits at a rate equal to N times a frequency of the PWM brightness control signal, where N equals the number of bits representing a single PWM duty cycle.”**

83. As set forth above, Thomas discloses all of the limitations in Claim 7.

See supra Section VIII.A.3. Thomas discloses the additional limitation of Claim 10.

Further to the discussion above for Claim 7, the shift register 31 in Thomas has twelve bits, and “sequentially stor[es] twelve binary values corresponding to the pulses or lack of pulses in the first modulating signal (E).” EX1005, 4:17-23, Fig. 2. Therefore, the duty cycle of the PWM signal E is represented by $N=12$ bits.

84. The frequency of a PWM signal, f (units in Hertz), is defined as $1/T$, where T is the period of the signal (units in seconds). Thomas explains that the period of the signal E is the time from A1 to A2 in Figure 3. EX1005, 4:51-53. As illustrated below in annotated Figure 3, this period corresponds to the time it takes for the shift register to output the 12 bits that correspond to the duty cycle of the signal E . In other words, the clock shifts the stored bits every $T/12$ seconds. Thus, the frequency of the clock signal is $f_{clock} = 1/(T/12) = 12/T = 12f = Nf$. The clock shifts the bits at a rate equal to N times the PWM frequency.

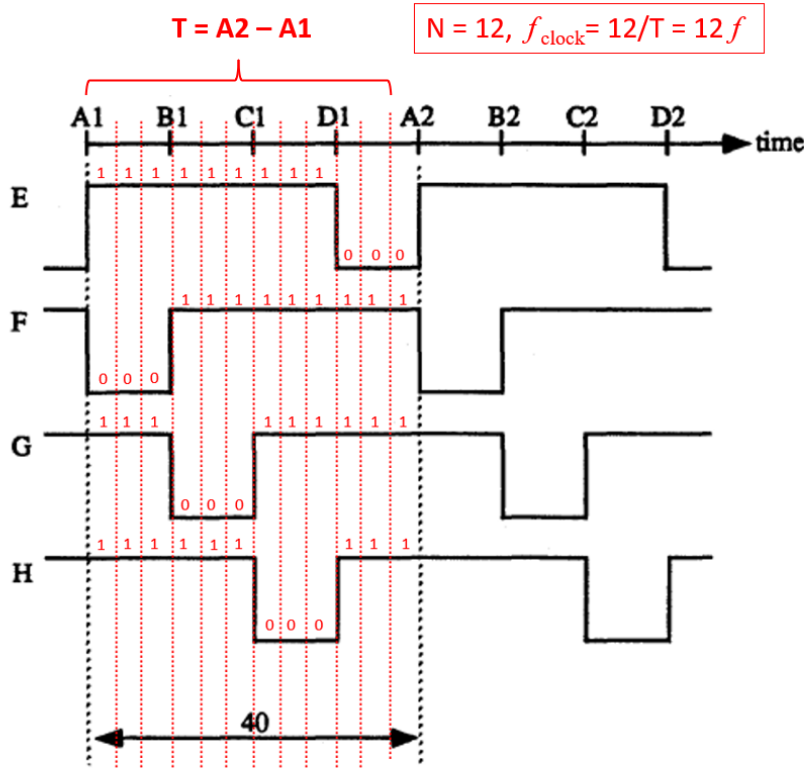


Fig. 3

EX1005, Fig. 3 (annotated), *see also id.* at 4:33-65. It is my opinion Thomas discloses this limitation. Accordingly, Thomas anticipates Claim 10.

6. Claim 11: “The driver of claim 1 wherein the plurality of parallel paths comprises at least three paths.”

85. As set forth above, Thomas discloses all of the limitations of Claim 1. *See supra* Section VIII.A. As discussed for the preamble [1.pre], Thomas discloses more than three parallel paths. *See supra* VIII.A.1 (preamble). And as I explained above, my opinions are based on four parallel paths that are controlled by the signals *E*, *F*, *G*, and *H*. *Id.* It is my opinion Thomas discloses this limitation. Accordingly, Thomas anticipates Claim 11.

7. Claim 12: “The driver of claim 1 further comprising the LEDs connected to the driver.”

86. As set forth above, Thomas discloses all of the limitations of Claim 1. *See supra* Section VIII.A. As discussed for the preamble [1.pre], Thomas discloses LEDs connected to the driver. *See supra* VIII.A.1 (preamble). It is my opinion Thomas discloses this limitation. Thus, Thomas anticipates Claim 12.

8. Claim 14

87. Claim 14 is a method claim with limitations that correspond to the limitations of Claim 1. For the reasons explained with respect to Claim 1, and as cross-referenced below, Thomas anticipates Claim 14.

a. Preamble [14.pre] – “A method for driving light emitting diodes (LEDs) connected to different parallel paths, the method comprising:”

88. Thomas discloses [14.pre] for the same reasons discussed for Preamble [1.pre]. *See supra* Section VIII.A.1.

b. Limitation [14.a] – “supplying a voltage to first ends of LEDs in a plurality of parallel paths;”

89. Thomas discloses Limitation [14.a] for the same reasons discussed for Limitation [1.a]. *See supra* Section VIII.A.1.a.

c. Limitation [14.b] – “setting a peak current through one or more LEDs connected in each of the parallel paths, the peak

current being set by a current set circuit for each parallel path;”

90. Thomas discloses Limitation [14.b] for the same reasons discussed for Limitation [1.b]. *See supra* Section VIII.A.1.b.

d. Limitation [14.c] – “generating staggered pulse width modulated (PWM) brightness control signals;”

91. Thomas discloses Limitation [14.c] for the same reasons discussed for Limitation [1.c]. *See supra* Section VIII.A.1.c.

e. Limitation [14.d] – “applying a different staggered PWM brightness control signals to each current set circuit; and”

92. As explained above for Limitations [1.c] and [1.d], Thomas discloses generating staggered PWM signals *E*, *F*, *G*, and *H* and applying a different one of those staggered PWM signals to each parallel LED path with its corresponding current set circuit (*i.e.*, R1, R5, R9, R13). *See supra* Section VIII.A.1.c.-d; *see also supra* Section VIII.A.1 (preamble). Thus, Thomas discloses applying different staggered PWM brightness control signals to each current set circuit.

f. Limitation [14.e] – “drawing the peak current through the one or more LEDs in each parallel path, set by its associated current set circuit, at a duty cycle corresponding to a duty cycle of an associated PWM brightness control signal, such that the parallel paths of LEDs conduct current at

substantially the same duty cycle but out of phase with each other.”

93. Limitation [14.e] corresponds to Limitation [1.d]: “each current set circuit being configured to draw the peak current through its associated one or more LEDs at a duty cycle substantially corresponding to a duty cycle of a PWM brightness control signal applied to it, such that the plurality of current set circuits conduct current through their associated one or more LEDs at the same duty cycle but out of phase with each other.” Thomas discloses Limitation [14.e] for the same reasons discussed for Limitation [1.d]. *See supra* Section VIII.A.1.d. It is my opinion that Thomas discloses every limitation of Claim 14 and anticipates Claim 14.

9. **Claim 17 – “The method of claim 14 wherein applying a different staggered PWM brightness control signal to each current set circuit comprises applying each staggered PWM brightness control signals to an associated transistor connected in series with the one or more LEDs in an associated parallel path, such that the transistor is turned on and off corresponding to the duty cycle of the staggered PWM brightness control signal applied to it.”**

94. Thomas anticipates Claim 14, as discussed above. *See supra* Section VIII.A.8.

95. As annotated in Figure 2 below, Thomas discloses transistors 33 which are connected in series with the current set resistors and the LED in each parallel path.

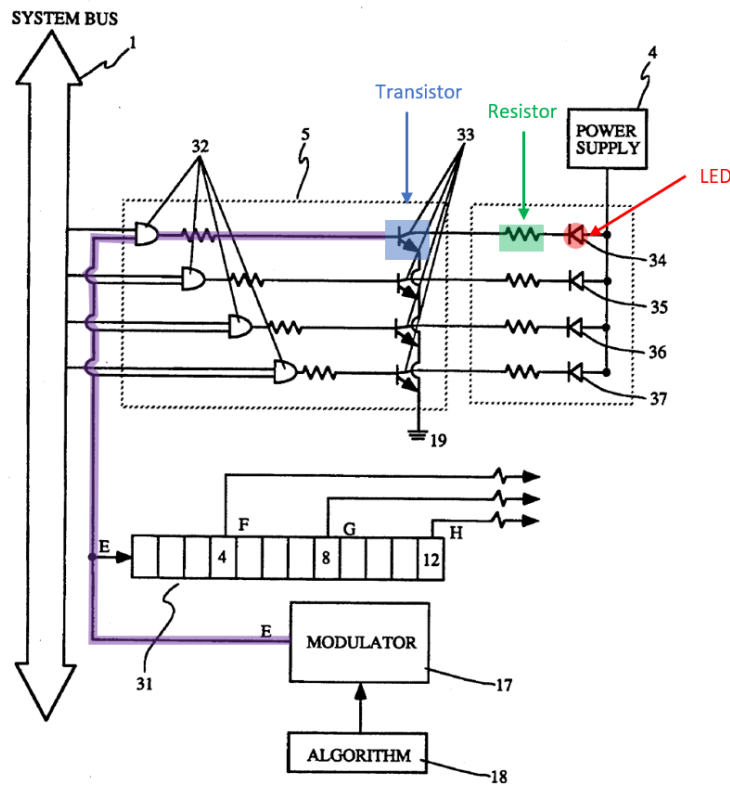


Fig. 2

EX1005, Fig. 2 (annotated). And as highlighted in purple, the transistor is connected to the PWM brightness control signal generator for receiving one of the staggered PWM brightness control signals. Specifically, the transistor highlighted blue above in Figure 2 receives the signal E , whereas other transistors in the other parallel paths, which are not shown in Figure 2, receive the other staggered signals F , G , and H . The transistors 33 are also connected to the PWM brightness control generator (the modulator 17, algorithm 18, and delay means 16, implemented in Figure 2 as a shift register) via AND gates 32. *See* EX1005, Fig. 2, 3:24-42.

96. It is my opinion that the transistors 33 are the “associated transistor connected in series with the one or more LEDs in an associated parallel path,” as recited in Claim 17. Thomas explains that when the transistors 33 are turned on, they “provide current from the power supply (4) for activating the associated LED’s (34-37) in the group of LED’s (9).” EX1005, 3:42-45. As shown in Figure 2 above, each transistor 33 is coupled to its respective LED and to the PWM modulator via the AND gate 32. EX1005, Fig. 2. The AND gate outputs a high control pulse to the transistor 33 when it receives both a high control signal (*W, X, Y, Z*) and a high PWM signal (*E, F, G, H*). *See* EX1005, 3:24-45, Fig. 2. Thus, when that the control signal (*W, X, Y, Z*) is high or “on,” the transistor 33 is activated at the duty cycle of the PWM signal (*E, F, G, H*), thereby controlling the brightness of the LED. It is thus my opinion that Thomas discloses this claim limitation.

97. Accordingly, Thomas anticipates Claim 17.

10. Claim 18

a. Preamble [18.pre] – “The method of claim 14 wherein generating staggered PWM brightness control signals comprises:”

98. Thomas discloses the method of Claim 14 as discussed above. *See supra* Section VIII.A.8.

- b. Limitation [18.a] – “storing bits corresponding to a PWM duty cycle of a brightness control signal in a shift register, the shift register having bit positions;”**

99. Thomas discloses Limitation [18.a] for the same reasons discussed for Limitation [7.a]. *See supra* Section VIII.A.3.a.

- c. Limitation [18.b] – “shifting the bits along the shift register under control of a clock; and”**

100. Thomas discloses Limitation [18.b] for the same reasons discussed for Limitation [7.b]. *See supra* Section VIII.A.3.b.

- d. Limitation [18.c] – “receiving bits tapped off the shift register at different bit positions of the shift register to generate a different staggered PWM brightness control signal from the bits at each of the different bit positions.”**

101. Thomas discloses Limitation [18.c] for the same reasons discussed for Limitation [7.c]. *See supra* Section VIII.A.3.c. Accordingly, it is my opinion that Thomas anticipates Claim 18.

- 11. Claim 20 – “The method of claim 18 further comprising serially and continuously loading bits corresponding to a PWM duty cycle of a brightness control signal into a first bit position the shift register, then shifting the bits by the clock.”**

102. Thomas anticipates Claim 18, as discussed above. *See supra* Section VIII.A.10. Thomas discloses Claim 20 for the same reasons discussed for Claim 9. *See supra* Section VIII.A.4. Accordingly, it is my opinion that Thomas anticipates Claim 20.

- 12. Claim 21 – “The method of claim 18 wherein the clock shifts the bits at a rate equal to N times a frequency of the PWM brightness control signal, where N equals the number of bits representing single PWM duty cycle.”**

103. Thomas anticipates Claim 18, as discussed above. *See supra* Section VIII.A.10. Thomas discloses Claim 21 for the same reasons discussed for Claim 10. *See supra* Section VIII.A.5. Accordingly, it is my opinion that Thomas anticipates Claim 21.

- 13. Claim 22 – “The method of claim 14 wherein the plurality of parallel paths comprises at least three paths.”**

104. Thomas anticipates Claim 14, as discussed above. *See supra* Section VIII.A.8. Thomas discloses Claim 22 for the same reasons as Claim 11. *See supra* Section VIII.A.6. Accordingly, it is my opinion that Thomas anticipates Claim 22.

B. Ground 2A: Claims 1, 3, 6, 7, 9, 10-12, 14, 17, 18, and 20-22 Would Have Been Obvious Over Thomas

105. My discussion of Thomas from Ground 1 (Section VIII.A.) is incorporated by reference here.

1. Claim 1

106. As discussed above, Thomas anticipates Claim 1. *See supra* Section VIII.A.1. To the extent that Thomas does not anticipate Claim 1, any differences between Thomas and Claim 1 are such that Claim 1 as a whole would have been obvious to a POSITA as of the time of the invention of Claim 1.

107. For example, to the extent that Thomas does not expressly state the function of the resistors that are connected in series with the LEDs, a POSITA would have understood that their function is to limit the current, as I explained above in discussing Limitation [1.b], based on the well-understood functionality of resistors. *See supra* Section VIII.A.1.b. No modification of Thomas would be required for the resistors to operate as a current set circuit, and a POSITA would have had a reasonable expectation of success that the disclosed resistors functioned as a current set circuit in view of their well-understood functionality. Accordingly, Thomas anticipates Claim 1, and to the extent an express disclosure of functionality is required, it is my opinion that Claim 1 would have been obvious in view of Thomas in view of the knowledge of a POSITA.

2. Claims 3, 7, 9-12, 14, 17, 18, and 20-22

108. Claim 14 is a method claim that corresponds to the limitations of Claim 1. For the reasons explained for Claim 1 above, to the extent that Thomas does not anticipate Claim 14, it is my opinion that Claim 14 would have been obvious in view of Thomas. *See supra* Section VIII.B.1.

109. Claims 3, 7, and 9-12 each depends directly or indirectly from Claim 1, while Claims 17, 18, and 20-22 each depends directly or indirectly from Claim 14. As set forth above in my discussion of these dependent claims, the additional limitations recited by these claims are disclosed in Thomas. Therefore, to the extent

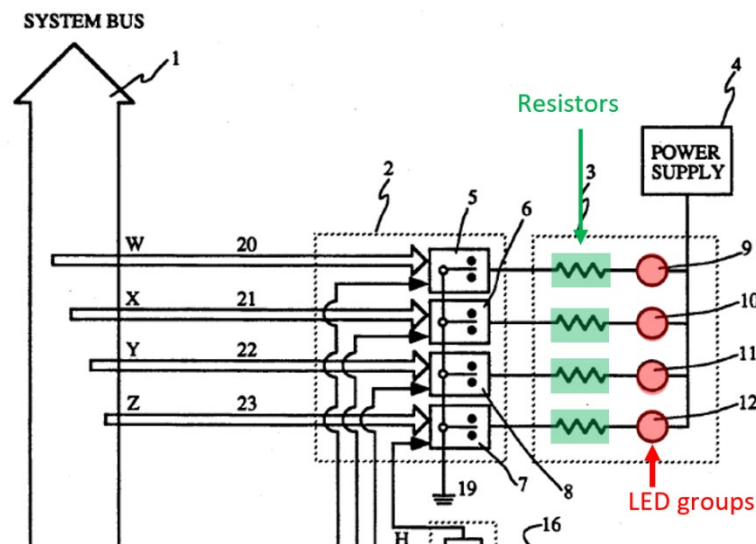
that Claim 1 or 14 would have been obvious in view of Thomas, rather than anticipated by Thomas, it is my opinion that claims 3, 7, 9-12, 17, 18, and 20-22 would have been obvious in view of Thomas.

3. Claim 6 Preamble: “The driver of claim 1 wherein each current set circuit comprises:”

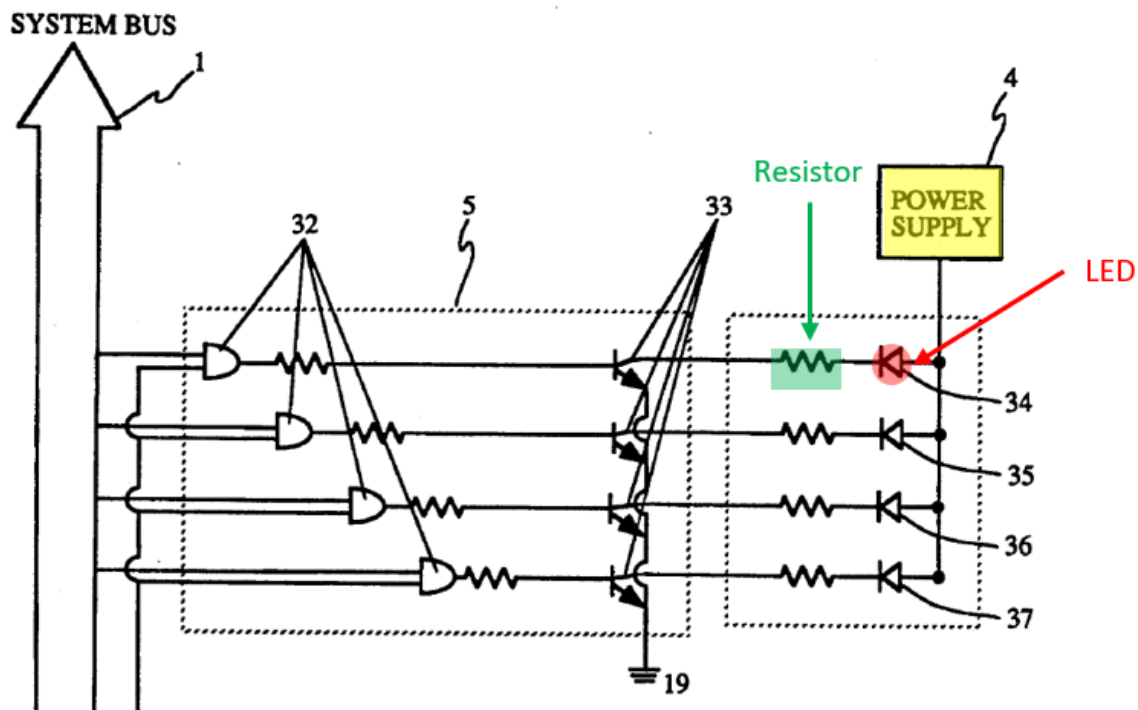
110. It is my opinion that Thomas anticipates and/or renders Claim 1 obvious, as discussed above in Section VIII.A.1 and VIII.B.1.

a. Limitation [6.a] – “a current set resistor in series with one or more LEDs in an associated parallel path; and”

111. As discussed for Limitation [1.b] above, Thomas discloses a resistor in series with an LED in each parallel path. *See supra* Section VIII.A.1.b. These resistors are current set resistors because, as discussed for Limitation [1.b] above, they limit the current that flows through the LEDs to $I=(V-V_{LED})/R$, where R is the resistance of the resistor, V is the voltage outputted from the power source, and V_{LED} is the voltage drop on the LED. Figures 1 and 2, annotated below, show the resistors (highlighted green) that are connected in series with the LEDs (highlighted red).



EX1005, Fig. 1 (cropped and annotated).



Id. at Fig. 2 (cropped and annotated). It is my opinion that Thomas discloses this limitation. Alternatively, to the extent an express disclosure of functionality is required, it would have been obvious to a POSITA based on the well-understood

functionality of resistors that the resistors of Thomas operate as current set resistors, for the same reasons discussed in my analysis of Claim 1.

- b. Limitation [6.b] – “a PWM brightness control transistor connected in series between the current set resistor and the one or more LEDs in an associated parallel path, the PWM brightness control transistor being connected to the PWM brightness control signal generator for receiving a staggered PWM brightness control signal.”**

112. As discussed with relation to Claim 17 above, Thomas discloses transistors 33 which are connected in series with the current set resistors (also discussed in Limitation [6.a]) and the transistor (and hence also the LED) in each parallel path and is turned on and off corresponding to the duty cycle of the staggered PWM brightness control signal applied to it. *See supra* Section VIII.A.9.; *see also supra* Section VIII.B.3.a.

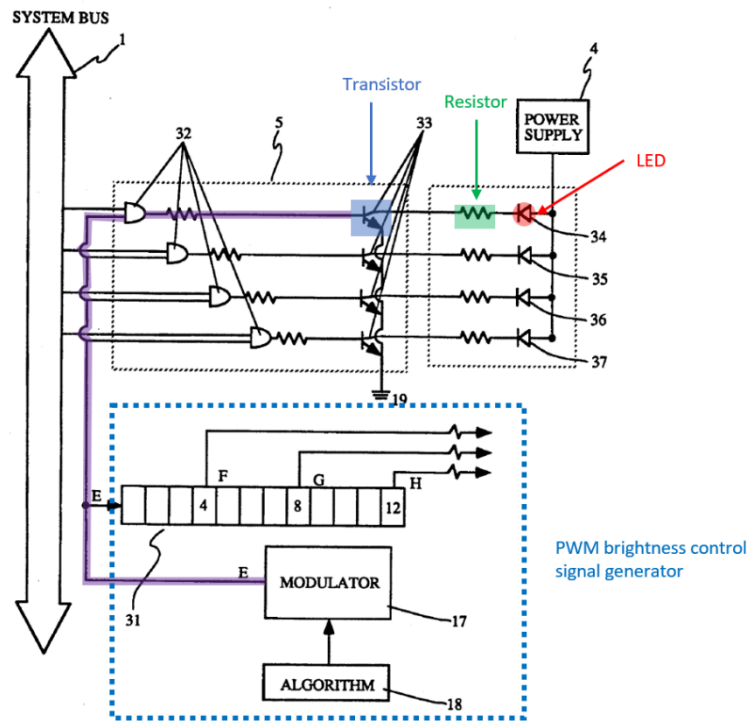


Fig. 2

EX1005, Fig. 2 (annotated). A POSITA would have understood that the transistors 33 are “PWM brightness control transistors,” as recited in Claim 6.

113. Thomas, however, does not expressly disclose that the PWM brightness control transistor is “connected in series *between* the current set resistor and the one or more LEDs.” Limitation [6.b] (emphasis added). Instead, Thomas discloses that the transistor 33 is connected in series after the LED and current set resistor. *See* EX1005, Fig. 2. However, this difference between Thomas and the language of Claim 6 is minor and Claim 6 as a whole would have been obvious to a POSITA over Thomas. In particular, the relative placement of the LED, current set resistor,

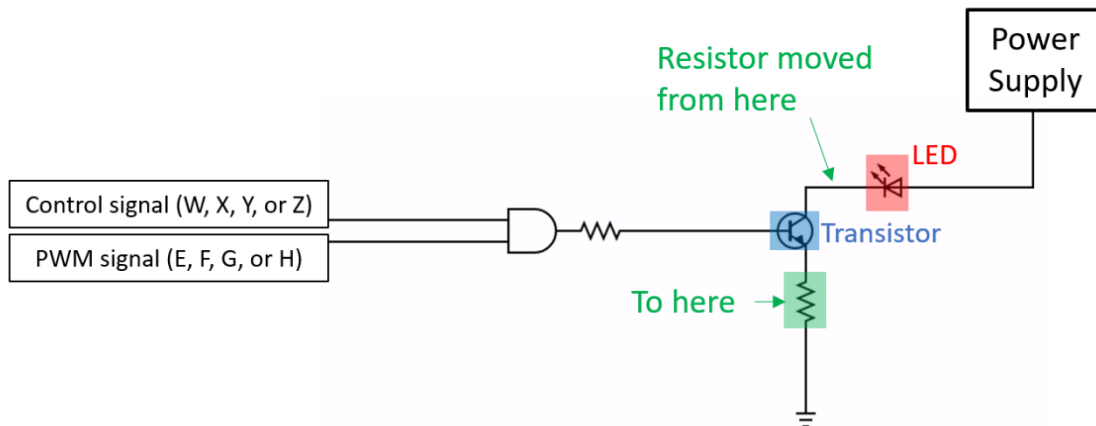
and the transistor was a matter of a simple design choice. There are only six possible ways in which the three circuit elements could be arranged in series with each other:

- LED, resistor, transistor
- LED, transistor, resistor³
- Resistor, LED, transistor
- Resistor, transistor, LED
- Transistor, resistor, LED
- Transistor, LED, resistor

Each of these arrangements would have operated the same way, as the functionality of the circuit disclosed in Thomas' Figure 2 does not depend on the precise order of these three elements. In all cases, the resistor limits the current, the LED emits light, and the transistor turns the current through the LED "on" or "off." Accordingly, it would have been a simple design choice to modify Thomas' Figure 2 circuit by

³ For instance, the LTC 3783 Specification Sheet discloses this arrangement. *See* EX1026. The LTC3783 is a current mode LED driver utilizing PWM control. *See id.* at 1. As shown in the figure on the bottom of page 1 of EX1026 titled "350mA PWM LED Boost Application," the LED string on the right hand side is in order connected to a transistor, a resistor, and then ground. *Id.*

moving the resistor to after the transistor. This modification is illustrated in the image below, which shows the modification in a single parallel path in Figure 2 of Thomas:



114. Further, A POSITA would have been motivated to make this particular modification to move the resistor after the transistor because in this configuration, the resistor can more easily act as a sense resistor. A “sense resistor” is a resistor that is placed in a circuit so that the current flowing through the circuit can be easily measured. Engineers commonly want to be able to detect the current flowing through the load (in this case, the LEDs) for monitoring and control purposes. Having the resistor connected to ground, as reflected in the proposed modification, allows the engineer to simply measure the voltage before the resistor to determine the current (V_R/R), where V_R is the measured voltage across the resistor. This current (V_R/R) corresponds to the current through the LED, plus a negligible current from

the base of the transistor. Without this configuration, one would need to perform a differential voltage measurement at both ends of the resistor in order to determine the current, and the voltage sensor would have to withstand the power supply voltage V when the transistor is off.

115. A POSITA would have had a reasonable expectation of success with this proposed modification, as it mainly comprises rearranging the order of existing components when the functionality of the circuit does not depend on the order, and a POSITA would have known how to carry out this modification, including any additional minor adjustments or modifications necessary to carry out the modification, using well-known techniques.

116. Accordingly, it is my opinion that Claim 6 would have been obvious to a POSITA in view of Thomas.

C. Ground 2B: Claims 2, 13, and 15 Would Have Been Obvious Over Thomas in View of the Knowledge of a POSITA and/or the Applicant Admitted Prior Art

1. Claim 2 – “The driver of claim 1 wherein the voltage source is a step up voltage regulator.”

117. It is my opinion that Thomas anticipates and/or renders Claim 1 obvious, as discussed above. *See supra* Sections VIII.A.1. and VIII.B.1. As discussed above for Limitation [1.a], Thomas discloses a power supply 4 for energizing the parallelly connected LEDs, which is a “voltage source.” *See*

EX1005, Fig. 1; *see also supra* Section VIII.A.1.a. In view of Thomas’ disclosure regarding its power supply, it would have been obvious to a POSITA to implement the power supply with a step-up voltage regulator, as confirmed by the AAPA.

118. Thomas discloses that the primary purpose of staggering the turning on and off of sets of LEDs is to reduce the “sudden change in current demand” that “may overload the power supply and trigger the power supply over current detection.” EX1005, 1:68-2:4. Thomas also emphasizes that without staggered control of the turning on and off of the sets of LEDs, “the power supply may have severe difficulty in maintaining a regulated voltage during these high current switching transitions.” EX1005, 1:62-68. Thomas further explains that sudden changes in current demand cause the output voltage of the power supply to “change in the inverse direction of the current demand, especially with switching power supplies.” EX1005, 1:68-2:4. Thus, the purpose of Thomas is to reduce “the magnitude of the instantaneous change in the current demand on the power supply such that a more stable output voltage can be maintained.” EX1005, 2:1-10.

119. “[S]witching power supplies” as described by Thomas would have been immediately recognized by a POSITA on or before April 2008 as a very well-known class of power supplies that use active switches together with reactive elements such as inductors and capacitors to repeatedly switch between two or more states in order to process power between input and output terminals. *See* EX1008, 355-360. This

class of power supplies can be used to regulate an output such as an output voltage. They are classified as step-up or step-down voltage regulators based on whether they “step” the voltage up (meaning increase the voltage relative to their input voltage, known in the art as a “boost” regulators) or step the voltage down (meaning decrease the voltage relative to their input voltage, known in the art as a “buck” regulators). These two types can also be combined so the voltage regulator can both step the voltage up and down (known in the art as a “buck-boost” regulators).

120. This class of switching power supplies was well-known on or before April 2008 to behave as described in Thomas with limitations in maintaining a stable output voltage with sudden changes in output current demand due to its switching nature and limited energy storage in its inductors and capacitors. Such switching power supplies were well-known to a POSITA as desirable for providing power to LEDs due to high efficiency, small size, and the ability to set the output voltage relatively independent of the input voltage according to the needs of the LED load.

121. As I noted above, Thomas expressly discloses that the invention is especially useful for “switching power supplies,” and a step-up voltage regulator is one of two very well-known options for a switching power supply (step up or step down). The only decision to be made by a POSITA in implementing the switching power supply is whether the output voltage needs to be increased or decreased relative to the input voltage to provide sufficient voltage to the LEDs. This is a very

common consideration that is easily calculated based on the type of input (e.g., a battery) and the voltage of the LEDs relative to the input. Thus, a POSITA would have been motivated and have had a reasonable expectation of success in implementing a step up converter as the power supply 4 in Thomas.

122. The '148 Patent admits that step-up voltage regulators were well-known in the prior art. Specifically, the '148 Patent describes “a typical prior art LED driver 10” in Figure 1A and explains that it contains a “DC voltage regulator controller 14 [which] up converts or down converts an input voltage (V_{in}), depending on the required voltage to drive the LEDs 12.” EX1001, 1:40-48. The '148 Patent further explains that “[t]he topology of the output circuit determines whether the voltage regulator is a step up or step down regulator” and that “*such regulators are well known and need not be described in detail.*” EX1001, 1:57-60 (emphasis added).

123. In addition, a POSITA would have been motivated to implement a step-up voltage regulator to boost the voltage source in Thomas, if the input voltage is lower than the required voltage to energize the LEDs. This would occur, for example, if the input voltage is from a battery or from a low-voltage system bus that is too low for energizing the LEDs. A POSITA would have had a reasonable expectation of success in including a step-up voltage regulator as part of the power

source because such circuitry, as acknowledged in the '148 Patent, was well-known in the art and their operation was well-understood.

124. For the reasons set forth above, it is my opinion that Claim 2 would have been obvious to a POSITA over Thomas in view of the knowledge of a POSITA or the Applicant Admitted Prior Art regarding step-up voltage regulators.

2. Claim 13 –“The driver of claim 1 wherein the driver is formed as an integrated circuit.”

125. Thomas anticipates and/or renders obvious Claim 1, as discussed above. *See supra* Sections VIII.A.1. and VIII.B.1. Thomas does not expressly state that the driver is formed as an integrated circuit or that the majority of the circuitry is part of an integrated circuit. However, it would have been obvious to a POSITA that the driver in Thomas would be formed as an integrated circuit, as this was a common practice in the industry at the time of the invention.

126. An integrated circuit is simply a circuit that is fabricated in a package, often on a semiconductor substrate. *See* EX1014 (“(1) an assembly of miniature electronic components simultaneously produced in batch processing, on or within a single substrate, that performs an electronic circuit function. (2) many transistors, resistors, capacitors, etc., fabricated and connected together to make a circuit on one monolithic slab of semiconductor material.”). In evaluating the claim language reciting that the “driver is formed as an integrated circuit,” a POSITA would be

aware that similar language is commonly used to describe a driver that may include one or more integrated circuits that integrate most of the circuitry into integrated packages, and that some large components of the driver, such as inductors or capacitors, may be external to the integrated circuits.⁴

127. Long before the '148 Patent, it was industry standard practice to fabricate electronic circuits for commercial products as integrated circuits. In practice, an engineer would design an electrical circuit, either on paper or in specialized computer software, test that design either on a breadboard or with computer simulation software, and then provide that circuit design to a contract manufacturer for fabrication into an integrated circuit. The reasons for fabricating electrical circuits as integrated circuits are legion. Integrated circuits are easy to manufacture and scalable for mass production, unlike circuits that are prototyped on a breadboard, for example. They are also smaller and more reliable because they are

⁴ Based on my review of Patent Owner's infringement contentions, I understand that Patent Owner contends that the accused televisions each have a driver in which the majority of the circuitry is part of an LED driver IC (i.e., NT5011S or AS3824) and therefore meet the limitation of Claim 13. EX1015, EXHIBIT A at pp.53-56. Accordingly, it is my understanding that Patent Owner is asserting that this claim is satisfied if the majority of the circuitry is part of the integrated circuit.

fabricated with miniature components and printed wire traces instead of the larger off-the-shelf components and loose wires that one would typically use for prototyping a circuit. Thus, it was industry standard well prior to April 2008 to manufacture circuits for commercial products as integrated circuits, and LED drivers were no exception.

128. This is also confirmed by the AAPA. Specifically, the '148 Patent explains that Figure 1A shows “a typical prior art LED driver 10 that drives multiple LEDs 12 in parallel,” that “[m]ost components of the driver 10 are formed on an integrated circuit chip” and “[t]he LEDs are typically connected to pins extending from the chip package.” EX1001, Fig. 1A, 1:43-45. Accordingly, the '148 Patent admits that LED drivers were formed as integrated circuits in the prior art.

129. In addition, a POSITA would have expected that Thomas' LED driver would be formed as an integrated circuit. Thomas describes that an LED driver can be used for controlling indicator lights on the front panel of a computer. *See* EX1005, 1:11-2:4. Because this would have been a use case in a commercial device, where essentially all the components of a computer are already made of integrated circuits, a POSITA would naturally expect that the LED driver is also formed as an integrated circuit. EX1005, 1:12-22. It would be extremely unusual for an LED driver in a commercial product to *not* be formed as an integrated circuit. Accordingly, it would have been obvious to a POSITA to implement Thomas' LED

driver as an integrated circuit, and a POSITA would have had a reasonable expectation of success in doing so because this technology was well-understood at the time of the '148 Patent.

130. For the reasons set forth above, it is my opinion that Thomas in combination with the knowledge of a POSITA, and as confirmed by the AAPA, renders Claim 13 obvious.

3. Claim 15 – “The method of claim 14 further comprising varying the duty cycle of the staggered PWM brightness control signals to change an average current through the parallel paths of LEDs to change a perceived brightness of the LEDs.”

131. Thomas anticipates and/or renders obvious Claim 14 as discussed above. *See supra* Sections VIII.A.8. and VIII.B.2. Thomas explains and a POSITA would have understood how to vary the duty cycle of PWM brightness control signals to change the average current through the parallel paths of LEDs to change the perceived brightness of the LEDs.

132. Thomas explains that PWM is used “[t]o control the *intensity* of the LED’s within the array” by “produc[ing] a series of rapid activations of the enabled LED’s.” EX1005, 1:23-42 (emphasis added). A POSITA would have understood Thomas to be describing the duty cycle of a PWM. Specifically, Thomas explains that “[t]he width of a given pulse in the period of the modulating signal determines the length of time that the enabled LED’s will be activated during the period.”

EX1005, 1:36-38. A POSITA would have understood that description to be referring to the duty cycle of the PWM, which is an expression of how long the PWM cycle is at its high state (or “on” state) in its period. A duty cycle of 60%, for example, means that the PWM signal is high for 60% of its period. Thomas also explains that the period of a modulating signal “is in the order of microseconds so that the series of activations of the LED’s produce an appearance that the LED’s are being dimmed rather than being turned on and off.” *Id.*

133. Thomas further describes varying the duty cycle. As described above, the purpose of “pulse width modulation of the control signals” is to “control the intensity of the LED’s within the array.” EX1005, 1:23-25. In describing the implementation of the pulse width modulation of the four time-shifted signals in Figure 3, Thomas explains that the timing of the positive edges are “fixed to occur at the designated times,” and that “the falling edges can occur at any subsequent time.

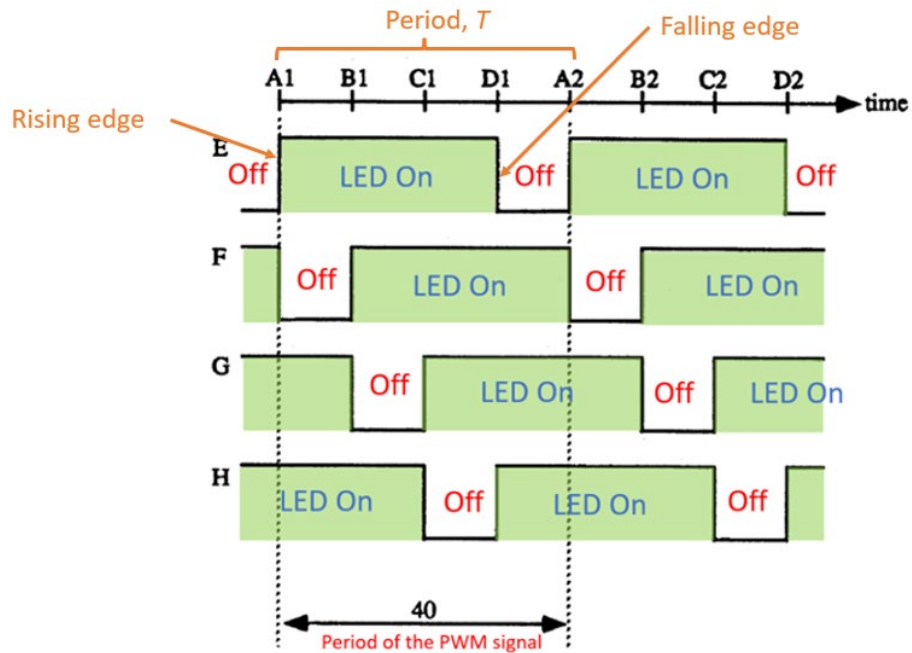


Fig. 3

EX1005, Fig. 3 (annotated), 4:60-62. “In other words, if a particular modulating signal goes high within the period (40), it can stay high for either a fraction of or for the entirety of the period (40).” EX1005, 4:62-65. A POSITA would have understood this explanation in Thomas is stating that the rising edge of the modulating signal is fixed in time, but the falling edge that determines the duty cycle, or the percentage of time that a modulating signal is high within a period, can vary. The variation can be anywhere from a fraction of a period to a full period as required to control the intensity of the LED’s.

134. Thomas further explains that the PWM waveform “may be determined by the use of an algorithm (18) implemented in either software or hardware as is

well-known in the art.” EX1005, 3:47-51. A POSITA would therefore have understood that the algorithm 18 can vary the PWM waveform, which leads to changes in the PWM duty cycle, and a proportional change in the percentage of time in a period that the LED’s are turned on to emit light. Accordingly, Thomas discloses varying the duty cycle of PWM brightness control signals to change the perceived brightness of the LEDs. In addition, a POSITA would also have understood varying the duty cycle of the PWM signal as a conventional way to control the brightness of the LED’s. *See* EX1021, ¶[0010]. Thus, a POSITA would have understood Thomas to describe varying the duty cycle of the PWM signals to change the perceived brightness of the LEDs.

135. While Thomas does not expressly discuss how the duty cycle of a PWM signal relates to the average current through the LEDs, a POSITA would have understood that is how pulse width modulation works to decrease the brightness of an LED. In my opinion, the limitation of Claim 15 of varying the duty cycle to change the average current is not adding an additional feature, but rather it is simply describing what happens when a duty cycle is changed. As explained above, in a PWM cycle, the duty cycle refers to how long in its period the signal is at its high state. When applied to an LED current, the PWM signal dictates how long during a period of the signal that the LED current is “on” at its maximum current and “off” for the rest of the period. Thus, a duty cycle of X% means that the LED current is

at its maximum value X% of the time, which also means that the average current through the LED is X% of the maximum current. In other words, changing the duty cycle of a PWM signal necessarily changes the average current through the LED(s) that are controlled by that PWM signal.

136. Indeed, the '148 Patent admits that this was known. The '148 Patent describes a “typical prior art LED driver 10 that drives multiple LEDs 12 in parallel” and explains that “if the duty cycle were 50%, the average current would be half of the peak current when the LEDs are on,” and therefore “the perceived brightness of the LEDs would be about half the brightness of the LEDs when fully on.” EX1001, 1:40-41, 2:15-18.

137. Therefore, it is my opinion that Claim 15 would have been obvious to a POSITA over Thomas in view of the knowledge of a POSITA, as confirmed by the AAPA.

D. Ground 2C: Claims 8 and 19 Would Have Been Obvious Over Thomas in view of Tatewaki and the Knowledge of a POSITA

- 1. Claim 8 – “The driver of claim 7 wherein the shift register has a connection that connects an end bit position to a first bit position so that bits in the shift register are recirculated in the shift register.”**

138. Thomas anticipates and/or renders obvious Claim 7, as discussed above. *See supra* Sections VIII.A.3. and VIII.B.2. Although Thomas does not expressly teach connecting the shift register 31's end bit position to its first bit

position to recirculate the stored bits, it would have been obvious to a POSITA to modify Thomas's shift register 31 in view of the knowledge of a POSITA and Tatewaki to do so.

139. First, the concept of connecting the output of a shift register to its input to recirculate the bits through the shift register was well known. For example, a 1976 patent about shift registers explains:

Shift registers have been used for some time to record information, such as a transient signal, and thereafter continuously recirculate the stored information such that it can be repetitively reproduced at the output of the shift register for display purposes or the like. A shift register is nothing more than a plurality of individual storage elements connected in a series or chain such that data entered at the input thereof propagates [sic], or shifts, from one storage element in the chain to the next. The entry of data at the input to the chain can either be from an external source of data, such as a pressure transducer, or alternatively can be stored data leaving the output of the chain. In the former case, the shift register is considered to be operating in a "storage" mode, whereas in the latter case the shift register operates in what is termed a "recirculating" mode.

EX1010, 1:12-27. Another textbook, *Digital Electronic Circuits and Systems*, published in 1974, also describes recirculating shift registers and also explains that they are also known by the name, "ring counter":

A register is simply an array of flip-flops used for the storage of binary data, and a **shift register** is one which is designed so that the data may be ‘shifted’ along the register in either direction, that is, either to the right or to the left. A **ring counter** is a shift register which is connected in the form of a continuous ring, the input to the ‘beginning’ of the ring being a logical function of the signals at one or more points in the register.

EX1011, 114 (emphasis in original); *see also id.* at 119 (“A ring counter is simply a shift register whose input is derived directly from its output, in the manner shown in figure 12.6”), Fig. 12.6 (reproduced below).

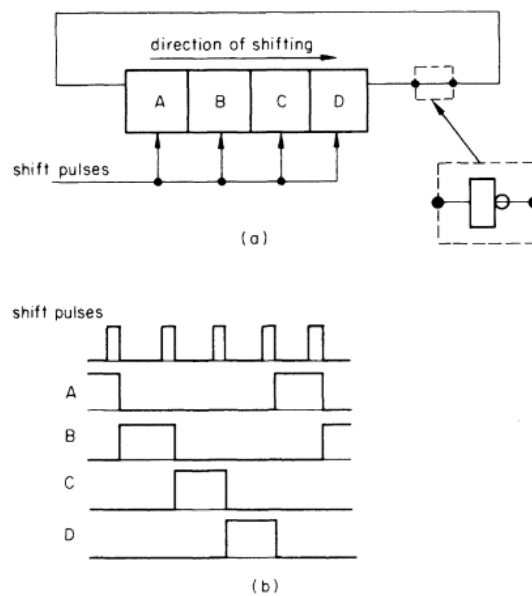


Fig. 12.6 A ring counter

EX1011, 119 (Fig. 12.6).

140. Second, it was also known to use ring counters in LED drivers. For example, Tatewaki discloses a PWM control scheme with a ring counter for

dimming LED lamps for a car interior. *See* EX1007, 12:11-30, 13:25-47.

Specifically, Tatewaki explains:

[E]ach time the on-off switch 163 is activated, a *ring counter* installed in the PWM control circuit 162 operates so that a duration of the on and off of the LED chip 132, 142 is changed, thereby controlling the brightness. Moreover, each time the mode switch 164 is activated when the LED chip 132, 142 is turned on, the ring counter operates so that the light color of the LED chip 132, 142 is switched in a sequence of changing colors determined in advance.

EX1007, 13:35-42; *see also id.* at 12:20-26 (“on-off switch 163” turns on and off the light and sets its brightness, “mode switch 164” changes the color of the light).

141. Accordingly, a POSITA would have understood from his or her general knowledge regarding ring counters and the use of ring counters in LED drivers as exemplified by Tatewaki that a ring counter would be able to receive a particular bit sequence corresponding to a PWM duty cycle, hold that bit sequence in the shift register, and recycle it indefinitely for driving the LEDs at a constant brightness until there is a command to change the brightness of the LEDs.

142. Thomas teaches using an “algorithm (18) implemented in either software or hardware as is well-known in the art.” EX1005, 3:46-51. A POSITA would have been familiar with many options for realizing the algorithm and would

have been motivated to modify the shift register 31 in the LED driver in Thomas to include a ring counter so that once a desired brightness is set with a particular PWM signal generated by algorithm (18), the shift register 31 would be able to constantly output that PWM signal until there is another command to change the brightness. A POSITA would have recognized that this would be beneficial because it reduces the load on the algorithm to constantly generate a PWM signal to be fed into Thomas' shift register. In particular, once the brightness of the LEDs has been set with a particular duty cycle and corresponding PWM waveform, the algorithm 18 would not need to constantly regenerate that PWM signal and feed it into the shift register. Rather, the algorithm 18 could simply generate the bit sequence for a PWM duty cycle one time when desired, input that bit sequence to the ring counter, and have the ring counter repeat that bit sequence indefinitely until the next change in brightness. A POSITA would have recognized that this is particularly useful in applications where the brightness of the LEDs does not need to change frequently.

143. For example, Thomas describes that an LED driver may be used to control the brightness of indicator lights on a computer front panel. EX1005, 1:12-42. A POSITA would have understood that use case as one in which the brightness of the LEDs is unlikely to be changed frequently, and so a ring counter that can constantly output the same PWM signal would be beneficial. Other examples would be the use of an LED driver to drive the backlight of a computer monitor, where

again, a user is likely to set the brightness of the screen at a certain level and leave it at that setting indefinitely.

144. A POSITA would have reasonably expected success of such modification. The circuitry for ring counters and their uses in LED drivers are well-known to a POSITA. The modification would require connecting the last bit position of the shift register 31 in Thomas to its first bit position, which is a straightforward electrical modification of the existing circuit well-known to the POSITA. *See, e.g.,* EX1011, 119 (showing a high-level diagram of a shift register having its output fed into its input). A POSITA would have also added a gate or a switch to the input of the shift register such that when the algorithm 18 generates a new bit sequence, the switch can activate such that the new bit sequence is loaded into the ring counter, and then deactivate so that the bit sequence begins recirculating around the ring counter. A POSITA would have known how to perform such a modification because these are basic circuits and connections as taught in early circuits courses and it would have been well within the skill of a POSITA to design that modified circuit.

145. Accordingly, it is my opinion that Claim 8 would have been obvious to a POSITA over Thomas in combination with Tatewaki and the knowledge of a POSITA.

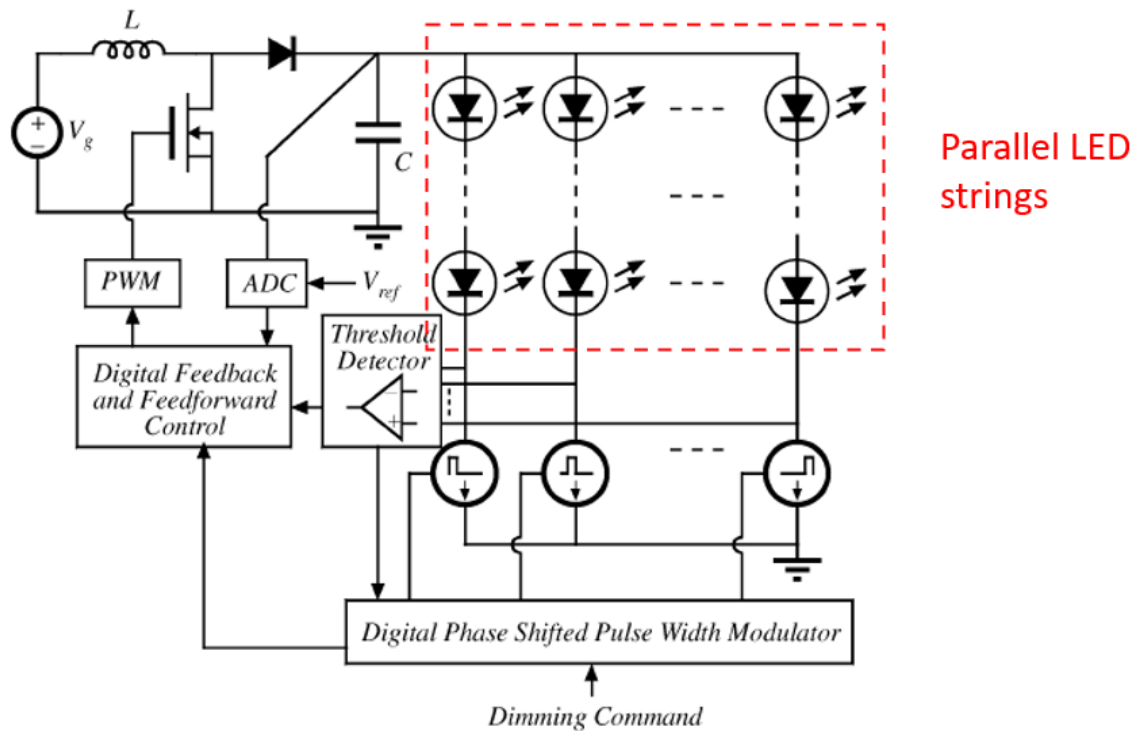
2. **Claim 19: “The method of claim 18 further comprising recirculating bits in the shift register by feeding a bit at an output bit position to an input bit position along the shift register.”**

146. Thomas anticipates and/or discloses Claim 18, as discussed above. *See supra* Sections VIII.A.10. and VIII.B.2. Claim 19 would have been obvious over Thomas in view of Tatewaki and the knowledge of a POSITA, for the same reasons discussed for Claim 8 above. *See supra* Section VIII.D.1.

E. Ground 3: Claims 1-4, 11, 12, 14, 17, and 22 Are Anticipated by *Zane*.

1. **Claim 1: “A light emitting diode (LED) driver for driving LEDs connected to different parallel paths,”**

147. *Zane* discloses an LED driver and “strings” of LEDs in at least three parallel paths. *See* EX1006, 287 (“This paper introduces a digital architecture suitable for driving a large number of High Brightness Light Emitting Diodes....”). As annotated below, Figure 1 shows a “[p]roposed digital architecture for driving a scalable number of parallel LED strings.”

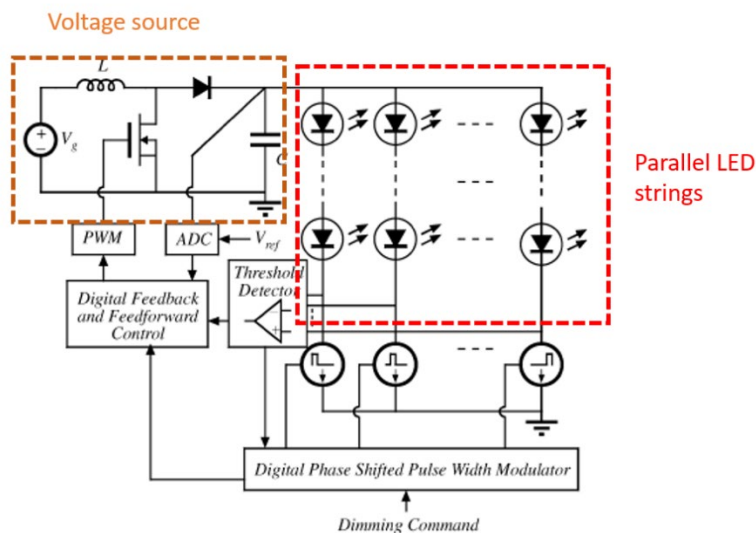


EX1006, Fig. 1 (annotated); 287. Note, Figure 1 is a high-level diagram of the LED driver. Figures 3 and 4 provide further details on the implementation of the LED driver. *See id.* at Figs. 3 and 4, 290-291. It is my opinion that *Zane* discloses the preamble.

- a. **Limitation [1.a]: “the driver comprising: “a voltage source for connection to first ends of LEDs in a plurality of parallel paths”**

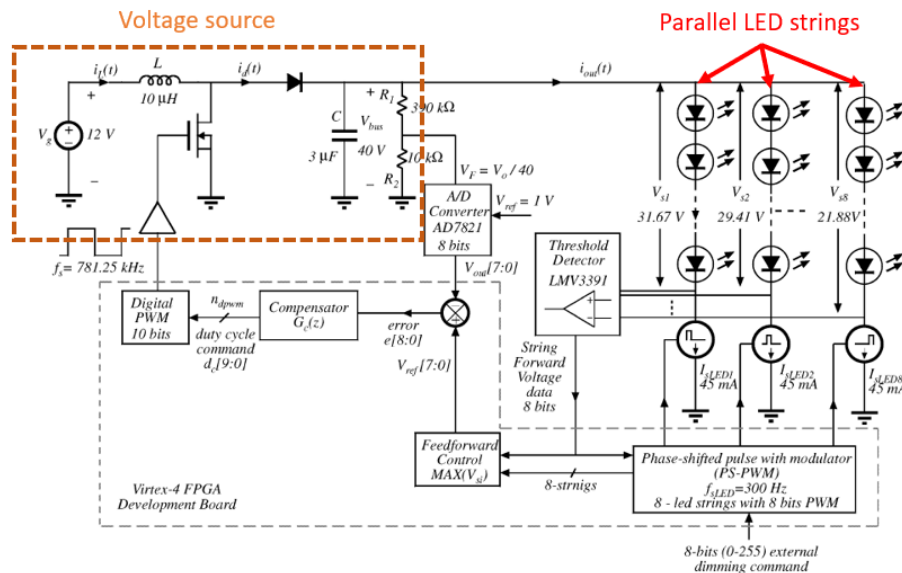
148. *Zane* discloses a voltage source for connection to first ends of LEDs in a plurality of parallel paths. *Zane* discloses, “The proposed architecture, shown in Fig. 1, consists of a power converter driving multiple strings of LEDs” EX1006, 288. Figure 1 from *Zane* is annotated below showing the voltage source (enclosed

in the orange dashed lines) and the parallel LED strings (enclosed in the red dashed lines). See EX1006, Fig. 1. The voltage source includes a voltage, V_g , and also a power converter circuit. Note, the output voltage to the LEDs is not necessarily V_g , because there is a power converter circuit which may either boost or buck the output voltage. In this case, the power converter is a boost converter (also known as a step-up voltage converter) which increases the voltage. See EX1006, 290 (“A boost topology is shown in Fig. 1 as appropriate for operating from a battery voltage or standardized low voltage bus.”). As shown in Figure 1, the voltage source, which includes a voltage source V_g , is connected to the parallel LED arrays via one end of the LEDs. See EX1006, Fig. 1 (annotated).



149. Figure 3 shows additional details on the implementation of Zane’s LED driver with the proposed circuit shown in Figure 1, including more details on the voltage source, “Digital Feedback and Feedforward Control” and the “Digital Phase

Shifted Pulse Width Modulator.” See EX1006, Figs. 1, 3. Again, as shown in the more detailed Figure 3 circuit, the voltage source is connected to the first ends (anodes) of the LEDs in a plurality of parallel LED strings, or “paths” as recited in the claim.



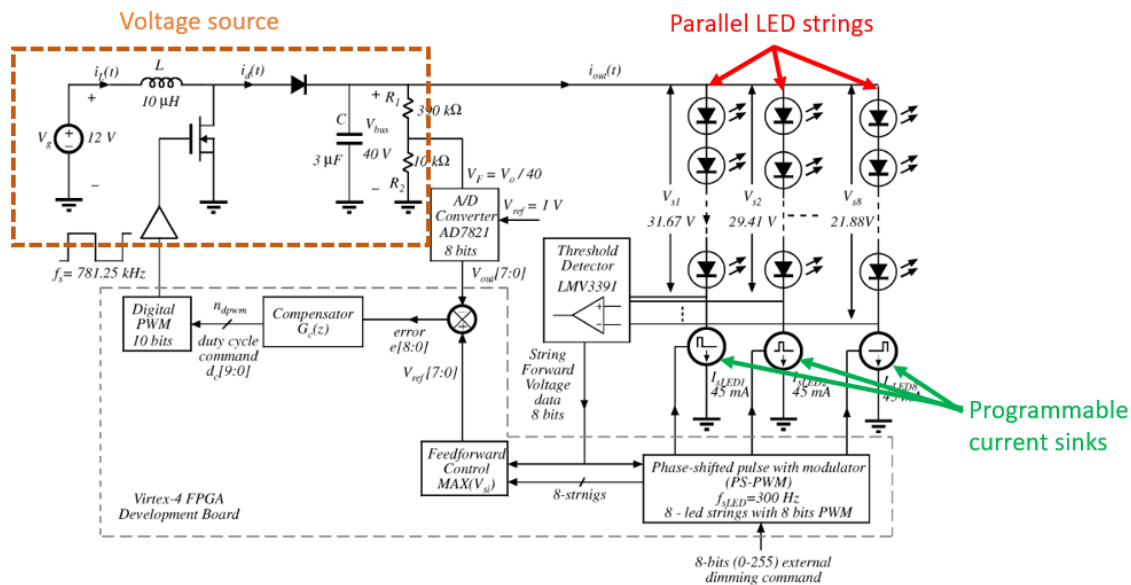
EX1006, Fig. 3 (annotated). It is my opinion *Zane* discloses this limitation.

- b. Limitation [1.b]: “a plurality of current set circuits, one current set circuit per parallel path, each current set circuit controlling a peak current through one or more LEDs connected in each parallel path”; and**

150. *Zane* discloses current set circuits in each parallel string of LEDs, which control the peak currents through each of the LEDs in each of the parallel LED strings. Specifically, *Zane* discloses the use of linear programmable current sinks that are connected to each of the LED strings. See EX1006, 290 (“In this architecture a linear programmable current sink is used to regulate the LED forward

current to a desired level.”), Figs. 3, 4. As annotated in Figure 3 below, the LED

driver has a plurality of these current sinks, indicated by the symbol , and there is one current sink per parallel LED string.



EX1006, Fig. 3 (annotated).

151. Figure 4 is a circuit diagram that provides details on the linear

programmable current sinks  in Figure 3.

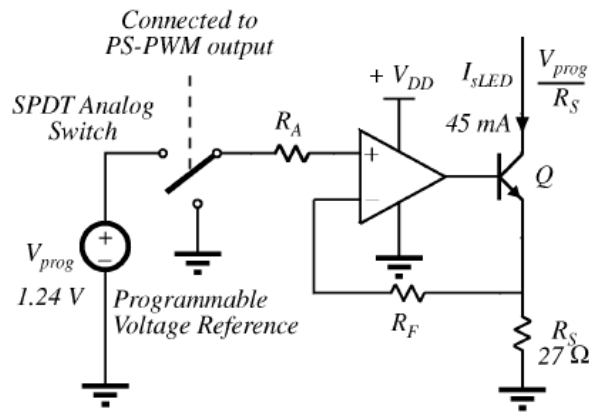


Figure. 4. An op-amp based precision programmable current sink with AM and PWM control options

EX1006, Fig. 4; *see also id.* at 290-291 (“The forward current through the LEDs is regulated by a discrete precision programmable current sink, as shown in Fig. 4.”).

152. This linear programmable current sink is a current set circuit controlling the peak current through the LEDs. *Zane* explains:

In this architecture a linear programmable current sink is used to regulate the LED forward current to a desired level. Amplitude modulation (AM) is achieved by programming the reference current level at which the sink regulates while pulse width modulation is implemented by enabling or disabling the current regulation device. ... Combination of AM and PWM schemes can be then used to achieve a wide dynamic dimming ratio, a feature key to many LED lighting applications.

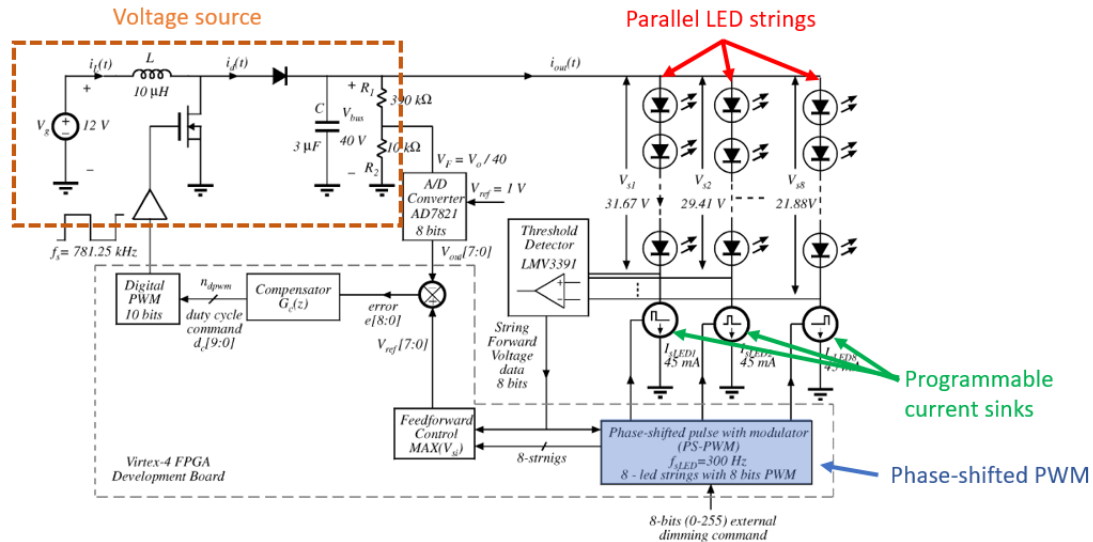
EX1006, 290. The reference to amplitude modulation via programming the reference current level means that the programmable current sink is setting the peak current that will flow through the LEDs in each parallel LED string. Indeed, *Zane*

further describes “the LED string current is regulated to a value of 45 mA by the choice of appropriate resistor, R_s .” EX1006, 290-291; *see also id.* at 291 (“[T]he peak-to-peak load current amplitude is limited by the PS-PWM block to just one LED string regulation current (45 Ma).”). Accordingly, *Zane*’s linear programmable current sink controls the peak current flowing through the one or more LEDs connected in the corresponding string. It is my opinion *Zane* discloses this limitation.

- c. **Limitation [1.c]: “a pulse-width modulated (PWM) brightness control signal generator connected to the plurality of current set circuits, the brightness control signal generator being configured to generate staggered PWM brightness control signals to the plurality of current set circuits”,**

153. As highlighted in blue in Figure 3 below, *Zane*’s LED driver comprises a digital phase-shifted pulse width modulator (PS-PWM) which is connected to the plurality of linear programmable current sinks (which as I discussed above, are current set circuits). *See* EX1006, Fig. 3 (annotated below), 291 (“An 8-bit (256

steps) 300 Hz PS-PWM is implemented on FPGA to control the operation of individual current sinks.”).⁵

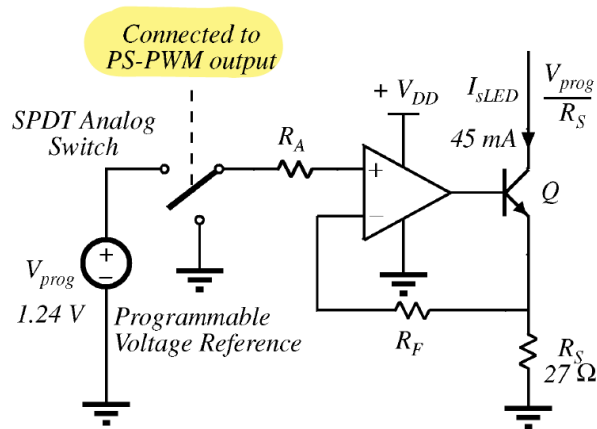


EX1006, Fig. 3 (annotated).

154. The PS-PWM generates staggered PWM brightness control signals to the plurality of current set circuits. *Zane* explains that “[t]he PS-PWM block controls the switching sequence and duty cycle of individual current sources based on the digital command (d bits) received from microcontroller or color control ASIC. ... The modulator rotates which strings are active, resulting in a natural phase shifting of the LED string drive signals that respond immediately to command

⁵ “FPGA” refers to a “Field Programmable Gate Array,” which is an off-the-shelf integrated circuit that circuit designers can reconfigure after manufacturing for specific purposes.

inputs.” EX1006, 288; *see also id.* at 291 (“An external dimming command, received by the PS-PWM module, is used to determine the appropriate phase-shift and duty cycle of individual control output signals.”). Further, as shown in Figure 4, the linear programmable current sink is “Connected to PS-PWM output.”



EX1006, Fig. 4 (annotated).

155. The phase-shifted PWM signals in *Zane* are “staggered.” As shown in Figure 2(a), “the individual outputs of PWM signals of the PS-PWM are phase shifted.” EX1006, 289. Figure 2(a) shows that each of the PWM signals are the same waveform, but that they do not line up in time. Thus, they are staggered. Moreover, Figure 2(a) shows that a different one of the staggered PWM signals is applied to each of the strings of LEDs.

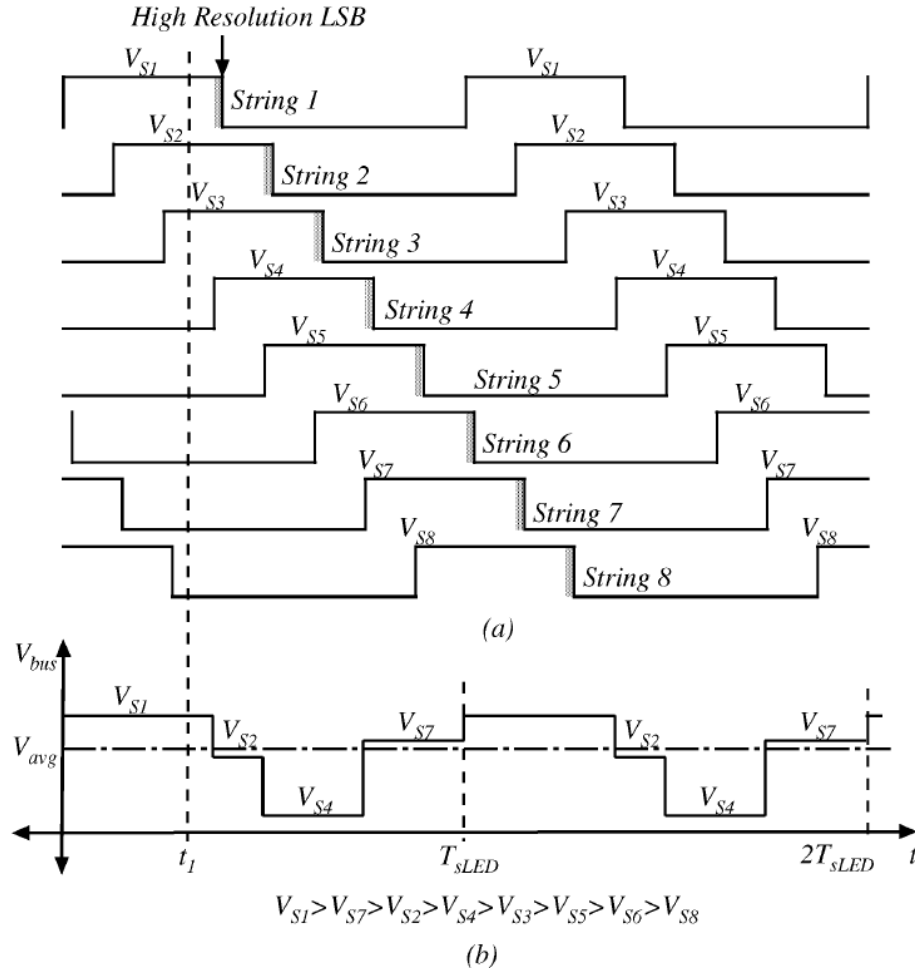


Figure 2(a). PS-PWM operating waveforms at 40% dimming command ($Dim=0110_0110 \{102\}$, $MSB = 011 \{3\}$, $LSB = 0_0110 \{6\}$) illustrating the phase rotation, with three LED strings ‘on’ at a given time and the LSB output (shaded area) added to end of each MSB to generate required resolution.

EX1006, Fig. 2(a). It is my opinion *Zane* discloses this limitation.

- d. **Limitation [1.d]:** “each current set circuit being configured to draw the peak current through its associated one or more LEDs at a duty cycle substantially corresponding to a duty cycle of a PWM brightness control signal applied to it, such that the plurality of current set circuits conduct current

through their associated one or more LEDs at the same duty cycle but out of phase with each other.”

156. *Zane* discloses that each of the current set circuits are controlled by the phase shifted pulse width modulator to conduct current according to the PWM signal output to the respective LED strings. EX1006, 290 (“Amplitude modulation (AM) is achieved by programming the reference current level at which the sink regulates while pulse width modulation is implemented by enabling or disabling the current regulation device. ... Combination of AM and PWM schemes can be then used to achieve a wide dynamic dimming ratio ...”), 291 (“An 8-bit (256 steps) 300 Hz PS-PWM is implemented on FPGA to control the operation of individual current sinks.”). *Zane* further discloses that the linear programmable current sinks are configured to draw the peak current through the LEDs in their associated parallel string at a duty cycle of the PWM brightness control applied to the current set circuits. EX1006, 290-291 (“[T]he LED string current is regulated to a value of 45 mA by the choice of appropriate resistor, R_S .”), 291 (“An external dimming command, received by the PS-PWM module, is used to determine the appropriate phase-shift and duty cycle of individual control output signals. ... [T]he peak-to-peak load current amplitude is limited by the PS-PWM block to just one LED string regulation current (45 mA).”). *Zane* also explains that “it is best suited to drive LEDs with a constant current, with minimum or no ripple.” EX1006, 290. These

disclosures reflect that the linear programmable current sinks in *Zane* draw the peak current (which is programmed with the amplitude modulation) through the LEDs in its associated parallel LED string at the duty cycle of the PWM signal that is applied to that current sink from the PS-PWM.

157. Further, *Zane* discloses that each of the current sinks are conducting current at the same duty cycle, but out of phase with each other. Figure 6 illustrates the currents flowing through three parallel strings of LEDs when the PS-PWM operates with a dimming command of 50%. EX1006, 291, Fig. 6. As shown below, the three PWM signals have the same waveform, and therefore the same duty cycle, but they do not line up in time. Thus, the PWM waveforms are out of phase with each other. Accordingly, the current sinks for the parallel LED strings conduct current through their associated LEDs at the same duty cycle but out of phase with each other.

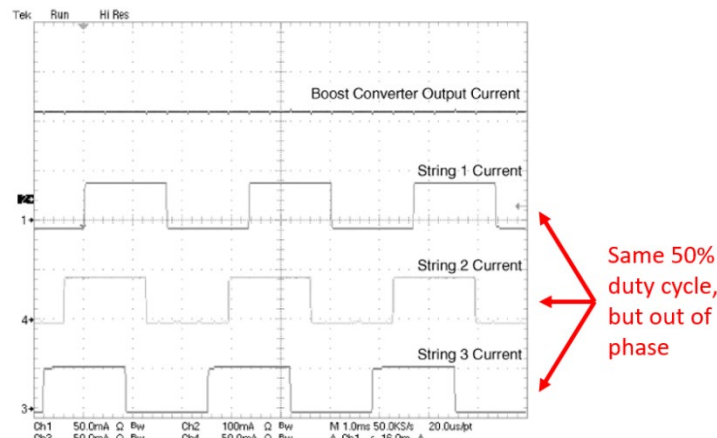


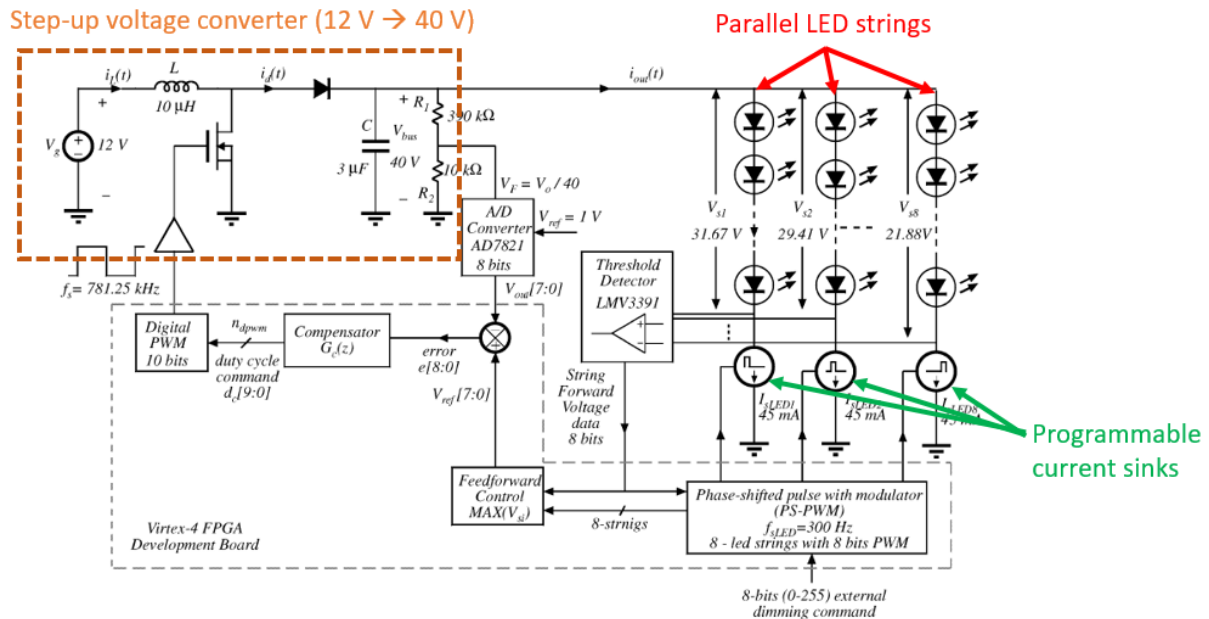
Figure. 6. Experimental system waveforms demonstrating operation of the PS-PWM block at an input command *Dim* = 50%. Current waveforms are shown for the boost converter output and 3 of the 8 LED string currents.

EX1006, Fig. 6 (annotated). It is my opinion *Zane* discloses this limitation.

158. Accordingly, it is my opinion that *Zane* anticipates Claim 1.

2. Claim 2: “The driver of claim 1 wherein the voltage source is a step up voltage regulator.”

159. *Zane* anticipates Claim 1 as discussed above. *See supra* Section VIII.E.1. As shown in Figure 3, *Zane* discloses that the voltage source is a boost converter, which is another name for a “step-up voltage regulator.” *See* EX1008, 355-260. *Zane*’s boost converter comprises a 12V voltage supply (V_g) as input and a circuitry for boosting the input voltage to 40V and outputting the boosted voltage. EX1006, 290 (“The boost converter is designed to output a 40 V signal from 12 V input supply The output is fed to an LED board, with an array of 64 LEDs split into 8 parallel strings of 8 LEDs each.”).



EX1006, Fig. 3 (annotated). It is my opinion *Zane* discloses this limitation.

Accordingly, it is my opinion that *Zane* anticipates Claim 2.

3. Claim 3: “The driver of claim 1 wherein each current set circuit is a current regulator.”

160. *Zane* anticipates Claim 1, as I discussed above. *See supra* Section VIII.E.1. As also discussed above with relation to claim limitation [1.b], *Zane*’s linear current sinks are current regulators. *See supra* Section VIII.E.1.b. Specifically, *Zane* identifies the linear current sinks as “current regulator[s]” in the description of Fig. 3 highlighted below.

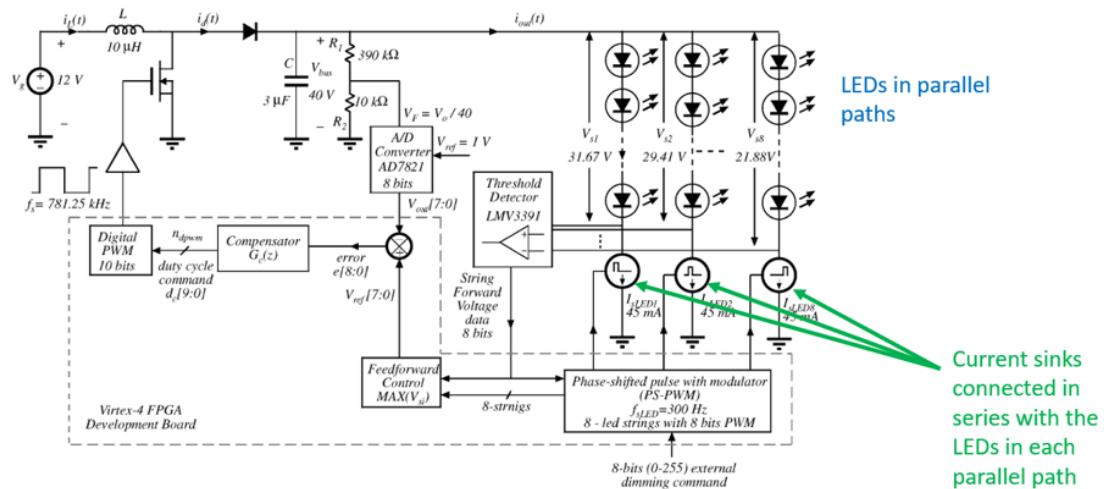


Figure 3. Experimental setup, consisting of a 15 W boost converter, 64 Osram MULTILEDs, linear programmable current regulator, 8-bit half-flash ADC, comparator based threshold detector circuit and digital PS-PWM and control logic implemented on Virtex-4 FPGA

EX1006, 291, Fig. 3 (annotated). *Zane* also discloses that the current sinks' main function includes regulating the current passing through the LEDs. *See* EX1006, 290 (“In this architecture a linear programmable current sink is used to regulate the LED forward current to a desired level.”), *id.* (“The forward current through the LEDs is regulated by a discrete precision programmable current sink, as shown in Fig. 4.”), Fig. 4 (circuit diagram for the current regulator). It is my opinion *Zane* discloses this limitation. Accordingly, it is my opinion that *Zane* anticipates Claim 3.

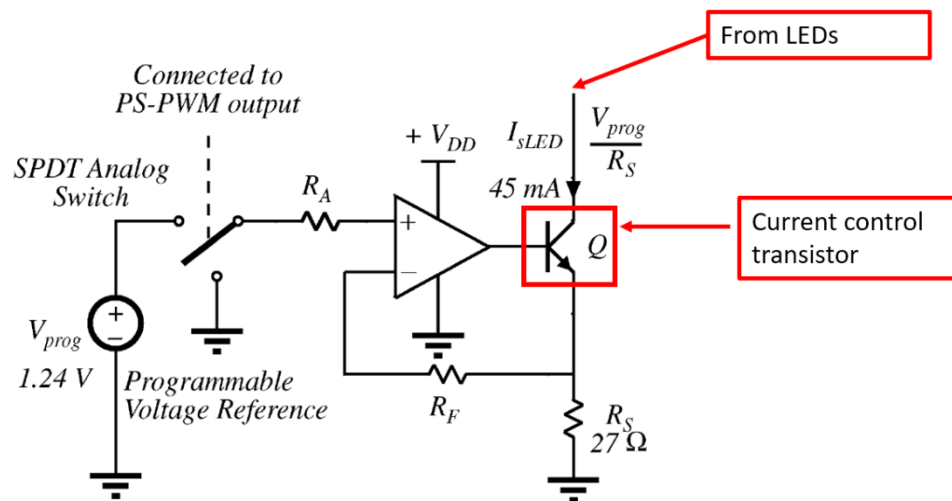
4. Claim 4: “The driver of claim 1 wherein each current set circuit is a current regulator comprising:”

161. *Zane* anticipates Claim 1, as I discussed above. *See supra* Section VIII.E.1. As discussed for Claim 3, *Zane* discloses that the programmable current

sinks are current regulators in each parallel string of LEDs. *See supra* Section VIII.E.3.

a. Limitation [4.a]: “a current control transistor in series with one or more LEDs in an associated parallel path;” and

162. Figure 4 of *Zane* shows the configuration of one of the programmable current sinks of Figure 3 that is connected to a parallel LED path.

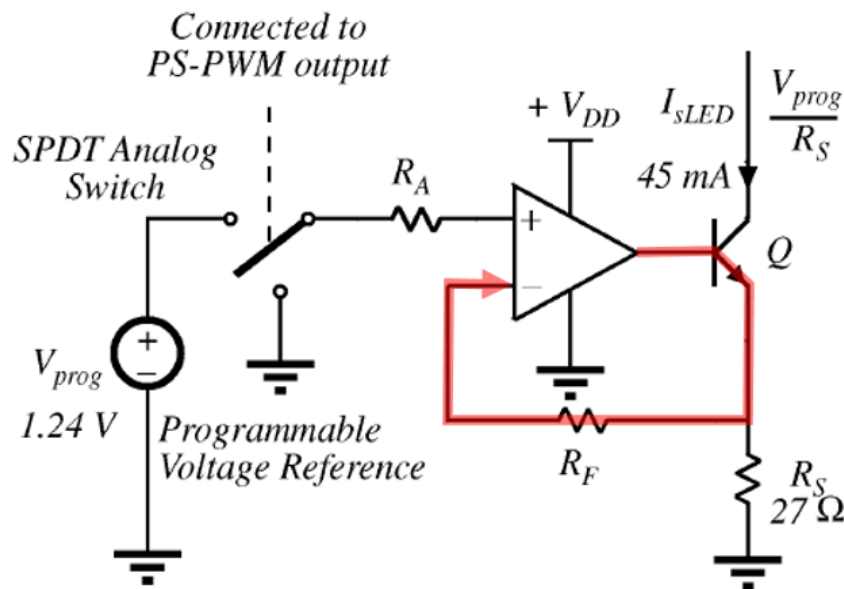


EX1006, Fig. 4 (annotated). *Zane*’s programmable current sink comprises a current control transistor Q , which is connected in series to the LEDs in that parallel string, as illustrated in Figure 3. If the transistor Q is on, the current flowing from the LEDs continues to flow into the transistor Q and then through the resistor R_S . *See* EX1006, Fig. 3 (showing current sinks in each parallel path), Fig. 4 (current sink circuit diagram). It is my opinion *Zane* discloses this limitation.

b. Limitation [4.b]: “a feedback circuit connected to detect a current through the parallel path and connected to the

current control transistor to control a conductivity of the current control transistor to cause the current through the parallel path to match a reference level.”

163. As further shown in Figure 4, *Zane* discloses that each current sink comprises an operational amplifier (“op amp”) forming a feedback circuit connected to the transistor *Q* that connects to the LED in series in the associated parallel path. The op amp receives voltage input from two different sources and outputs a single voltage.

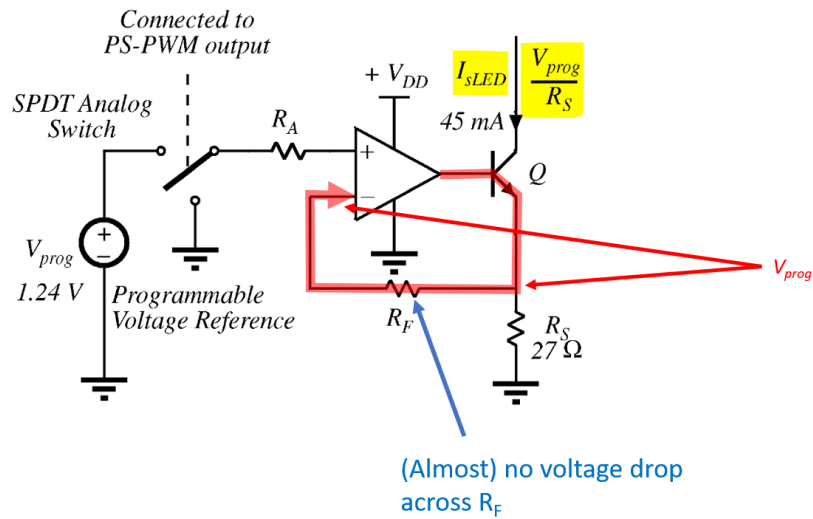


EX1006, Fig. 4 (annotated). Specifically, the output end of the op amp is first connected to the current control transistor Q and then fed back into its inverting (-) input, as shown in the path highlighted red above. *Id.*

164. The output of the op amp is a voltage, and as the output voltage is added to the current transistor Q , it controls the conductivity of the current transistor Q .

Zane explains that the current through the parallel path is $I_{sLED} = \frac{V_{prog}}{R_s}$, where V_{prog} is a programmable voltage reference. See EX1006, 290-291, Fig. 4. Since the resistance of the resistor R_s is a fixed value, the feedback circuit detects a current, which is I_{sLED} , through the parallel path.⁶ The negative feedback op amp circuit shown in *Zane*'s Figure 4 functions to cause the inverting (-) input voltage to match the noninverting (+) input of the op amp. In other words, the voltage at the inverting input (-) is the same as the voltage before R_s , which is V_{prog} , as annotated below.

⁶ Additionally, I note that resistors were and still are very commonly placed in electrical circuits next to ground as shown in Figure 4. These resistors were (and still are) commonly known in the art at the time of the *Zane* publication as “sense resistors” because they allow for easy measurement of the current through the load. That is because the current can be measured by measuring the voltage right before the resistor and applying the simple formula $I=V/R$.



EX1006, Fig. 4 (annotated).⁷ As a result, Zane's current sink causes the current through the parallel path to match a reference level, defined as V_{prog}/R_S . It is my opinion Zane discloses this limitation.

165. Accordingly, it is my opinion that Zane anticipates Claim 4.

⁷ As I also indicated in this figure, there is almost no voltage drop across R_F . A POSITA would have understood that an op amp has an extremely high input impedance (an ideal op amp has infinite input impedance, whereas an actual op amp typically has an input impedance on the order of millions of ohms), which means that almost no current will flow across R_F . Therefore, the voltage at R_S would be the same voltage at the inverting input (-).

5. Claim 11: “The driver of claim 1 wherein the plurality of parallel paths comprises at least three paths.”

166. *Zane* anticipates Claim 1, as discussed above. *See supra* Section VIII.E.1. As shown in Figure 1 and discussed with relation to the preamble [1.pre] above, *Zane*’s system comprises at least three parallel strings of LEDs. *See* Section VIII.E.1. (preamble); EX1006, Figure 1. Thus, it is my opinion that *Zane* anticipates Claim 11.

6. Claim 12: “The driver of claim 1, further comprising the LEDs connected to the driver.”

167. *Zane* anticipates Claim 1, as discussed above. *See supra* Section VIII.E.1. As shown in *Zane*’s Figures 1 and 3, and as discussed with relation to the preamble [1.pre] above, *Zane*’s system comprises LEDs connected to the driver. *See* Section VIII.E.1. (preamble); EX1006, Figs. 1, 3. It is thus my opinion that *Zane* anticipates Claim 12.

7. Claim 14

168. Claim 14 is a method claim with limitations that correspond to the limitations of Claim 1. For the reasons explained with respect to Claim 1, and as cross-referenced below, it is my opinion that *Zane* anticipates Claim 14.

a. Preamble [14.pre]

169. *Zane* discloses Limitation [14.pre] for the same reasons discussed for Limitation [1.pre]. *See supra* Section VIII.E.1. (preamble).

b. Limitation [14.a]

170. *Zane* discloses Limitation [14.a] for the same reasons discussed for Limitation [1.a]. *See supra* Section VIII.E.1.a.

c. Limitation [14.b]

171. *Zane* discloses Limitation [14.b] for the same reasons discussed for Limitation [1.b]. *See supra* Section VIII.E.1.b.

d. Limitation [14.c]

172. *Zane* discloses Limitation [14.c] for the same reasons discussed for Limitation [1.c]. *See supra* Section VIII.E.1.c.

e. Limitation [14.d]

173. As explained with respect to Limitations [1.c] and [1.d], *Zane*'s PS-PWM generates staggered PWM brightness control signals and applies a different staggered PWM brightness control signal to each of the current set circuits in each string of LEDs. *See supra* Section VIII.E.1.c-d. *Zane* discloses this limitation.

f. Limitation [14.e]

174. *Zane* discloses Limitation [14.e] for the same reasons discussed for Limitation [1.d]. *See supra* Section VIII.E.1.d.

8. Claim 17

175. *Zane* anticipates Claim 14, as discussed above. *See supra* Section VIII.E.7. *Zane* discloses the additional limitation of Claim 17 for the same reasons

discussed above for Limitations [4.a] and [4.b]. *See supra* Sections VIII.E.4.a.-b. It is thus my opinion that *Zane* anticipates Claim 17.

9. Claim 22

176. *Zane* anticipates Claim 14, as discussed above. *See supra* Section VIII.E.7. *Zane* discloses more than three parallel paths. *See supra* Section VIII.E.1. It is thus my opinion that *Zane* anticipates Claim 22.

F. Ground 4: Claims 1-4, 5, 11-17, and 22 Would Have Been Obvious Over *Zane*

177. My discussion of *Zane* from Ground 3 (Section VIII.E.) is incorporated by reference here.

1. Claims 1-4, 11, 12, 14, 17, and 22

178. As discussed above, it is my opinion that *Zane* anticipates Claim 1-4, 11, 12, 14, 17, and 22. To the extent that *Zane* does not anticipate Claim 1, any differences between *Zane* and Claim 1 are such that Claim 1 as a whole would have been obvious to a POSITA as of the time of the invention of Claim 1.

179. Claim 14 is a method claim that corresponds to the limitations of Claim 1. For the reasons explained for Claim 1 above, to the extent that *Zane* does not anticipate Claim 14, Claim 14 would have been obvious in view of *Zane*.

180. Claims 2, 3, 4, 11, and 12, each depends directly or indirectly from Claim 1, and Claims 17 and 22 each depends directly or indirectly from Claim 14.

As set forth above, the additional limitations recited by these claims are disclosed in *Zane*. Therefore, to the extent that Claim 1 or 14 would have been obvious in view of *Zane*, rather than anticipated by *Zane*, then Claims 2, 3, 4, 11, 12, 17, and 22 would have been obvious in view of *Zane*.

2. Claim 5: “The driver of claim 4”

181. *Zane* anticipates and/or renders obvious Claim 4, as discussed above.

See supra Sections VIII.E.4. and VIII.F.1.

a. Limitation [5.a]: “wherein each current set circuit further comprises a PWM brightness control transistor connected between an output of the feedback circuit and a control terminal of the current control transistor,”

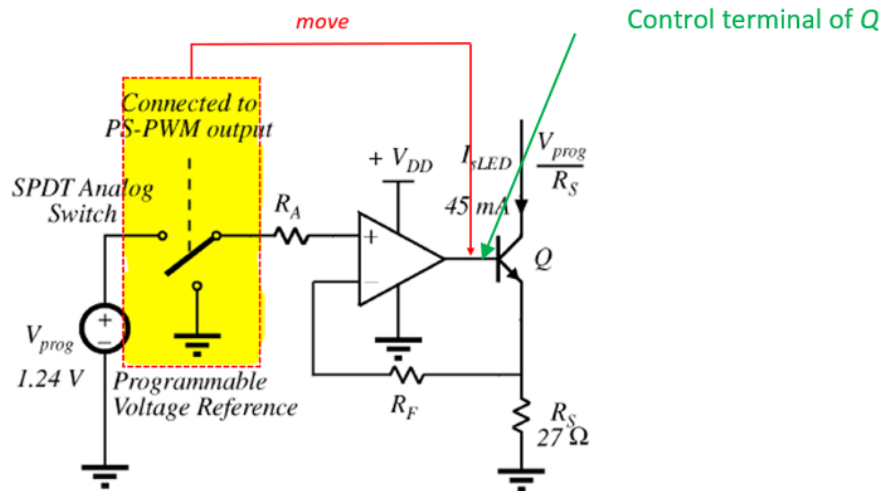
182. As shown in Figure 4, *Zane*’s programmable current sink further comprises a SPDT (single-pole double-throw) analog switch that connects to the PS-PWM output. *See* EX1006, Fig. 4. A POSITA would have understood that the SPDT analog switch in Figure 4 that is capable of responding to the PS-PWM output would include at least one transistor because in this type of electronic circuit, a switch that is controlled by another circuit (*i.e.*, not a physical light switch for a user) would need to involve a transistor. A POSITA would have had many options readily at hand to implement a SPDT analog switch, including for example a single pass transistor with a pull down resistor, two transistors, or one of many commercially

available integrated circuits acting as analog switches, all of which comprise one or more transistors.

183. Alternatively, a POSITA would have readily implemented the SPDT analog switch with at least one transistor because the switch is controlled by the PS-PWM output and therefore a POSITA would naturally use a transistor as a switch. As discussed with relation to claim limitation [1.c] above, *Zane*'s PS-PWM generates the staggered PWM brightness control signals. *See supra* Section VIII.E.1.c. Accordingly, a POSITA would have understood that *Zane*'s SPDT analog switch is or would have been implemented as a PWM brightness control transistor.

184. *Zane* does not disclose that the PWM brightness control transistor is “connected *between* an output of the feedback circuit and a control terminal of the current control transistor.” Limitation [5.a] (emphasis added). As shown in Figure 4, *Zane*'s SPDT analog switch, which corresponds to the PWM brightness control transistor, is connected before the noninverting (+) input of the op amp, rather than between the output end of the op amp (the output of the feedback circuit) and the current control transistor *Q*. *See* EX1006, Fig. 4. However, it would have been obvious to a POSITA to move the SPDT analog switch in *Zane* from the noninverting (+) input of the op amp to between the output of the op amp and the

current control transistor Q . The below annotation to Figure 4 in *Zane* illustrates the modification:



EX1006, Figure 4 (annotated). In the modified system of *Zane*, the switch would connect to the base terminal of the current transistor Q . A POSITA would have understood the base terminal of Q , identified in the annotated Figure 4 above, is a control terminal because applying an appropriate voltage to the base terminal turns on the transistor to conduct current through the collector to the emitter terminals (from the LED to the resistor R_S and to ground).

185. I understand that a POSITA may be motivated to make a particular modification as obvious to try when choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success. I believe in this case, a POSITA would have been motivated to make this modification to *Zane* as to where the switch is located as a design choice among only a few equally valid locations. A

POSITA would have understood that the switch (the PWM brightness control transistor) may be placed in several locations in this circuit without changing the overall operation of the circuit, because the purpose of the switch is to turn the programmable current sink “on” or “off”, and hence, to control the passing of current through the LEDs in the associated path.⁸ Whether the switch is placed at the noninverting (+) input, or at the output of the op amp, or even elsewhere such as between Q and R_S , the switch would perform the same function. When the PWM brightness control transistor is located before the noninverting input, the transistor would switch the reference voltage between V_{prog} (current flows through LEDs) and ground (no current flows through LEDs). When the PWM brightness control transistor is located between the output of the op amp and the control terminal of Q , the transistor would either open (no current through LEDs) or close (current flows

⁸ For instance, Chang discloses an electrical circuit for a LED driver where a brightness control transistor is positioned between the output of the feedback circuit and the current control transistor. *See* EX1027, Fig. 1 and 1:21-2:31. In Fig. 1, Chang discloses a transistor (QA2) for receiving the PWM brightness control signal that is connected between the output of an op-amp (U2) and another transistor (Q1) for controlling the current flowing through the LED string. *Id.*

through LEDs) the feedback loop. The switch turns the linear programmable current sink on or off by opening or closing the circuit.

186. Thus, a POSITA would have understood that there are a finite number of ways in which the PWM brightness control transistor could be connected to *Zane*'s programmable current sink, and it would have been obvious for the POSITA to try any of those solutions as a design choice. In my opinion, if ten engineers were given the task of implementing the circuit design from *Zane*, I would expect some of them to place the switch at the noninverting input as I did, but I would also expect some to place the switch between the output of the op amp and the transistor *Q*, and some might even place the switch elsewhere, and that any such placement would have been an obvious design choice that could have been implemented with a reasonable expectation of success because it involves the use of well-known techniques in circuit design.

- b. Limitation [5.b]: “the PWM brightness control transistor being connected to the PWM brightness control signal generator for receiving a staggered PWM brightness control signal to couple the output of the feedback circuit to the control terminal of the current control transistor at a duty cycle of the staggered PWM brightness control signal.”**

187. As shown in Figures 3 and 4 of *Zane*, the SPDT analog switch, which is the PWM brightness control transistor, is connected to the PS-PWM output for

receiving a phase-shifted, *i.e.*, staggered, PWM brightness control signal. *See supra* Section VIII.F.2.a.; EX1006, Figs. 3-4.

188. After a POSITA has modified the SPDT analog switch to connect between the output of the feedback circuit and the control terminal of the current control transistor Q as discussed above in Section VIII.F.2.a. for claim limitation [5.a], the modified SPDT analog switch would automatically couple the output of the feedback circuit (the voltage outputted from the op amp) to the control terminal of the current control transistor (the base terminal of Q), according to the duty cycle of the staggered PWM brightness control signal.

189. Accordingly, it is my opinion that Claim 5 would have been obvious over *Zane*.

3. Claim 13: “The driver of claim 1 wherein the driver is formed as an integrated circuit.”

190. *Zane* anticipates and/or renders obvious Claim 1, as discussed above. Claim 13 also would have been obvious over *Zane*. *See supra* Sections VIII.E.1. and VIII.F.1. As discussed above for Claim 13 in Ground 2B, a POSITA would have been aware that similar language is commonly used to describe a driver that

may have many but not all components integrated as packages.⁹ See Section VIII.C.2. Zane discloses that its “digital architectures for driving large LED arrays” is FPGA-based. EX1006, Abstract, 293 (“Experimental results are presented for a 15 W boost converter with ***FPGA based digital control driving a 64 LED array with 8 LED strings.***”), 291 (“Experimental setup, consisting of ... digital PS-PWM and control logic ***implemented on Virtex-4 FGPA***”) (emphasis added). A POSITA would have understood an FPGA (field-programmable gate array) is an off-the-shelf integrated circuit that an engineer can reconfigure through programming after manufacturing. An FPGA is essentially a large array of transistors organized as blocks of logic gates, latches, and related functional blocks with reprogrammable connections. The reprogrammable connections allow an engineer to quickly and easily implement complex digital circuits with hundreds to thousands and tens of thousands of logic gates all within a single integrated circuit. The programming is typically realized using advanced software design tools that convert desired functional digital circuit behavior into synthesized designs of logic gates and

⁹ As also discussed above for Claim 13 in Ground 2B, based on my review of Patent Owner’s infringement contentions, it is my understanding that Patent Owner has asserted that the claim is satisfied if the majority of the circuitry is part of the integrated circuit. See Section VIII.C.2.

automated routing to reprogram the array of gates on the FPGA. Thus, *Zane* discloses use of an FPGA as an integrated circuit for the digital control functions of the driver.

191. In addition to the FPGA-based digital control, *Zane* also discloses an operational amplifier (op-amp) integrated circuit for the precision programmable current sink, and additional integrated circuits for additional functions such as voltage protection (with a commercial integrated circuit, the LMV3391 comparator). EX1006, 291. It would have been obvious to a POSITA to combine the various integrated circuits and current control transistors of the driver disclosed in *Zane* as one integrated circuit. *Zane* discloses that integrated solutions for LED drivers “with multiple current sinks for driving parallel LED strings” were already well-known and commercially available by major suppliers such as Maxim (e.g., MAX6974, MAX6975) and Texas Instruments (TLC5940). EX1006, Section I. Introduction, 287 (“An integrated solution with multiple current sinks for driving parallel LED strings is described in [9,10].”). *Zane* further discloses that the “programmable linear current sink [used in *Zane*] can be constructed using discrete components, as described in section IV, or can be easily integrated on chip using precision programmable current mirrors [9,10].” EX1006, Section III.E. Programmable Current Reference and LED Array, 290. Thus, *Zane* expressly discloses that LED drivers are typically realized as integrated circuits, and that the additional hardware

provided by *Zane* for digital control and LED current regulation can be easily added to existing commercially available LED drivers.

192. As discussed above for Claim 13 in Ground 2B, it was standard practice in the electronics industry to fabricate circuits as integrated circuits, and a POSITA would have been motivated to do so for many reasons such as cost, efficiency, scalability, reliability, and manufacturability, and for a wide variety of applications, such as for driving the LED backlighting on displays. *See supra* Section VIII.C.2. Accordingly, it would have been obvious to a POSITA to form the LED driver in *Zane* as an integrated circuit. Indeed, while *Zane* discussed a prototype circuit, a POSITA would have known that if integrated into a commercial product, the driver would have been fabricated as an integrated circuit for the reasons identified above. It would have been routine for a POSITA to have fabricated the LED driver as an integrated circuit when it came to production, as referenced in *Zane* for the Maxim and Texas Instruments LED driver integrated circuit solutions.

193. This is also confirmed by the AAPA. Specifically, the '148 Patent explains that Figure 1A shows “a typical prior art LED driver 10 that drives multiple LEDs 12 in parallel,” that “[m]ost components of the driver 10 are formed on an integrated circuit chip” and “[t]he LEDs are typically connected to pins extending from the chip package.” EX1001, 1:43-45. Accordingly, the '148 Patent admits that

LED drivers were formed as integrated circuits in the prior art, consistent with the disclosures in *Zane*.

194. Accordingly, it is my opinion that Claim 13 would have been obvious over *Zane*.

4. **Claim 15: “The method of claim 14 further comprising varying the duty cycle of the staggered PWM brightness control signals to change an average current through the parallel paths of LEDs to change a perceived brightness of the LEDs.”**

195. *Zane* anticipates and/or renders obvious Claim 14, as discussed above. *Zane* discloses varying the duty cycle of the PS-PWM to change the perceived brightness of the LEDs by tailoring an external dimming command input to the PS-PWM module, for example. *See, e.g.*, EX1006, Figs. 5-6, 8a-8b (showing PWM waveforms at various duty cycles), 291 (“An external dimming command, received by the PS-PWM module, is used to determine the appropriate phase-shift and duty cycle of individual control output signals.”).

196. While *Zane* does not expressly discuss how the duty cycle of a PWM signal relates to the average current through the LEDs, a POSITA would have understood that varying the duty cycle of the signal is how pulse width modulation works to decrease the brightness of an LED. *See, e.g.*, EX1021, ¶[0010]. As discussed for Claim 13 in Ground 2B, it is my opinion that the limitation of Claim 15 of varying the duty cycle to change the average current is not adding an additional

feature, but rather it is simply describing what happens when a duty cycle is changed. *See* Section VIII.C.3. Specifically, the purpose of driving LEDs using PWM is to be able to dim the brightness of the LEDs by applying a fixed current and rapidly turning the LEDs on and off according to a duty cycle, rather than by changing the magnitude of the current actually flowing through the LEDs. A duty cycle of X% means that the LEDs are on X% of the time, meaning that the average current through the LEDs is X% of the fixed current. *See id.* Thus, a POSITA would have understood that varying the duty cycle of a PWM signal changes the average current through the parallel paths of LEDs. *See also* EX1001, 2:7-18 (Applicant admitting that in a prior art LED driver, PWM is used to change the average current flowing through the LEDs).

197. Accordingly, it would have been obvious to a POSITA based on *Zane* and his or her knowledge that *Zane*'s disclosure of dimming LEDs by PWM is effectively changing the average current through the LEDs. Accordingly, Claim 15 would have been obvious over *Zane*.

5. Claim 16 Preamble: “The method of claim 14”

198. *Zane* anticipates and/or renders obvious Claim 14, as discussed above. *See supra* Section VIII.E.7.

- a. Limitation [16.a]: “wherein setting a peak current through one or more LEDs connected in each of the parallel paths comprises setting the peak current by controlling**

conductivity of a current control transistor in series with each parallel path,” and

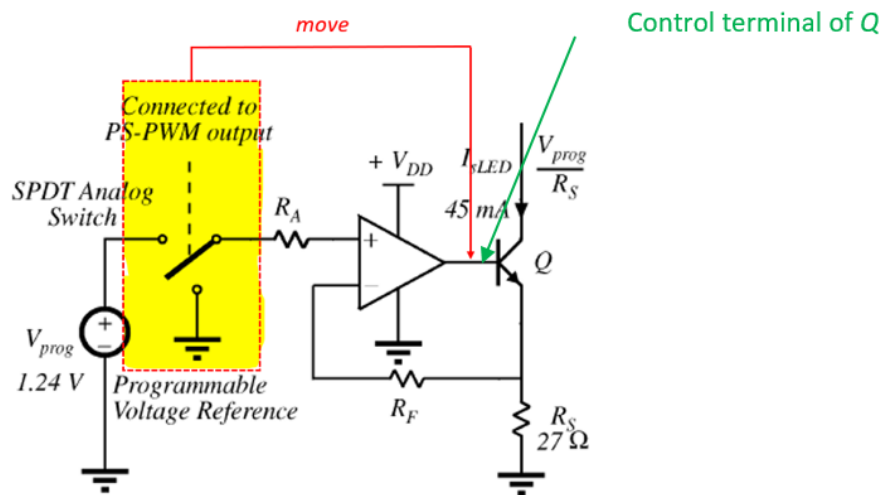
199. As discussed above with relation to Limitations [1.b] and [1.d] above, *Zane* discloses a plurality of current set circuits each setting a peak current flowing through their respective string of LEDs. *See supra* Section VIII.E.1.b.-d. As also discussed above with relation to Limitations [4.a] and [4.b] above, *Zane* discloses that each current set circuit further comprises a current control transistor *Q* in series with the LEDs in the respective string and a feedback circuit controlling the conductivity of the transistor *Q* to regulate the current through the LEDs. *See supra* Section VIII.E.4.a.-b. It is my opinion that *Zane* discloses this limitation, or it would have been obvious for the reasons set forth above for Claims 1 and 4.

- b. Limitation [16.b]: “wherein applying a different staggered PWM brightness control signal to each current set circuit comprises: coupling each staggered PWM brightness control signal to a control terminal of an associated pass transistor, each pass transistor being connected between a control terminal of a respective current control transistor and a regulating control voltage, such that the current control transistor is turned on and off corresponding to a duty cycle of the associated pass transistor.”**

200. As discussed with respect to Limitations [5.a] and [5.b], *Zane* discloses a SPDT analog switch which a POSITA would have implemented with a transistor and which is connected to the output of the PS-PWM. *See supra* Sections VIII.F.a.-b. A POSITA would have understood that the SPDT analog switch is the “pass

transistor” for Claim 16 for the same reasons that a POSITA would have understood that the SPDT analog switch is the “PWM brightness control transistor” for Claim 5. *Id.*

201. As also discussed for Limitation [5.a], it would have been obvious to a POSITA as a design choice among few possibilities to move the SPDT switch from the noninverting input of the op amp to a location between the output of the op amp and the control terminal of the current control transistor Q , as shown below:



EX1006, Fig. 4 (annotated). For the reasons discussed for Limitation [5.a], a POSITA would have had a reasonable expectation of success with this proposed modification. *See supra* Section VIII.F.2.a. In the modified *Zane* system as shown above, a POSITA would have understood V_{prog} is the “regulating control voltage” as it sets the current passing through the current control transistor Q and the LEDs in the associated path as $I_{sLED} = V_{prog}/R_S$. *See supra* Section VIII.E.4.b. Thus, when the

SBPT analog switch is moved to that location, it is between the “regulating control voltage” and the control terminal of *Q*.

202. Finally, in the modified *Zane* system, the staggered PWM signal is applied to the SPDT analog switch. Thus, a POSITA would have understood that the SPDT analog switch will turn the current control transistor *Q* on and off at the same duty cycle of the staggered PWM signal that is applied to the SPDT switch. In other words, the pass transistor is connected such that the current control transistor is turned on and off according to the duty cycle of the associated pass transistor.

203. Accordingly, Claim 16 would have been obvious over *Zane*.

IX. SECONDARY CONSIDERATIONS

204. I understand that secondary considerations of non-obviousness, such as commercial success, unexpected results, industry praise, skepticism of others, long-felt-but-unmet need, etc., should be considered with respect to obviousness when evidence of such factors has been introduced. I am not aware of any evidence of secondary considerations. I reserve the right to respond to any evidence of secondary considerations introduced by Patent Owner. Additionally, as explained above, it is my opinion that many of the '148 Patent claims are anticipated by Thomas and *Zane*. I understand that secondary considerations of non-obviousness are not relevant when a claim is anticipated by the prior art.

X. CONCLUSION

205. For the foregoing reasons, it is my opinion that claims 1-22 of the '148 Patent are anticipated by or would have been obvious to a POSITA at the relevant time in view of the prior art referenced above.

206. I declare that all statements made herein on my own knowledge are true and that all statements made on information and belief are believed to be true, and further, that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Dated: October 19, 2023

By: 

Regan Zane