

Digital Architecture for Driving Large LED Arrays with Dynamic Bus Voltage Regulation and Phase Shifted PWM

I. INTRODUCTION

High brightness light emitting diodes (HB LEDs) have evolved as an alternative lighting solution to conventional technologies, with efficacy greater than that of incandescent lamps and becoming comparable to fluorescent lamps [1, 2]. Applications for large arrays of LEDs (series-parallel connection) include general lighting and LCD TV backlighting. Typical drive solutions for large LED arrays include use of a dedicated power converter with output current regulation for each series string [3,4,5] or use of an integrated circuit to regulate the currents of parallel strings driven from a single constant voltage power supply [5]. The first approach results in a large number of dedicated power converters for large systems that may require many tens of parallel LED strings. The second approach may result in poor efficiency due to a fixed power supply voltage despite wide manufacturing tolerances [6] and temperature variations in LED forward voltage. Both approaches also result in large pulsed currents from the power supply due to the common use of pulse width modulation (PWM) for dimming control in the LED system.

This paper presents an approach that integrates the control of a single power stage to drive a scalable number of parallel LED strings with individual current regulation, coordinated phase shifted PWM dimming to eliminate pulsed currents from the converter output and dynamic bus voltage regulation for improved efficiency. A hardware efficient multi-phase modulator (MPM) is adopted from [7] for natural phase shifting of the PWM drive signals to each parallel LED string. Dynamic bus voltage regulation is achieved through feed-forward of load changes from the MPM, active sensing of the required drive voltage for each LED string and optimal sequencing of LED strings. The proposed architecture is presented in Section II, followed by an experimental test system and experimental results in Section III.

II. LED DRIVE ARCHITECTURE

The proposed architecture, shown in Fig. 1, consists of a power converter driving multiple strings of LEDs, controlled current sources, digital multiphase modulator block, comparator based ADC to sense voltage drop across each strings and feed-forward control logic. A conventional boost power stage is selected as it is the most common topology employed to drive LEDs. Closed-loop output voltage control is achieved through a digital control loop consisting of an A/D converter, a digital PID look-up table based compensator and a digital PWM (DPWM).

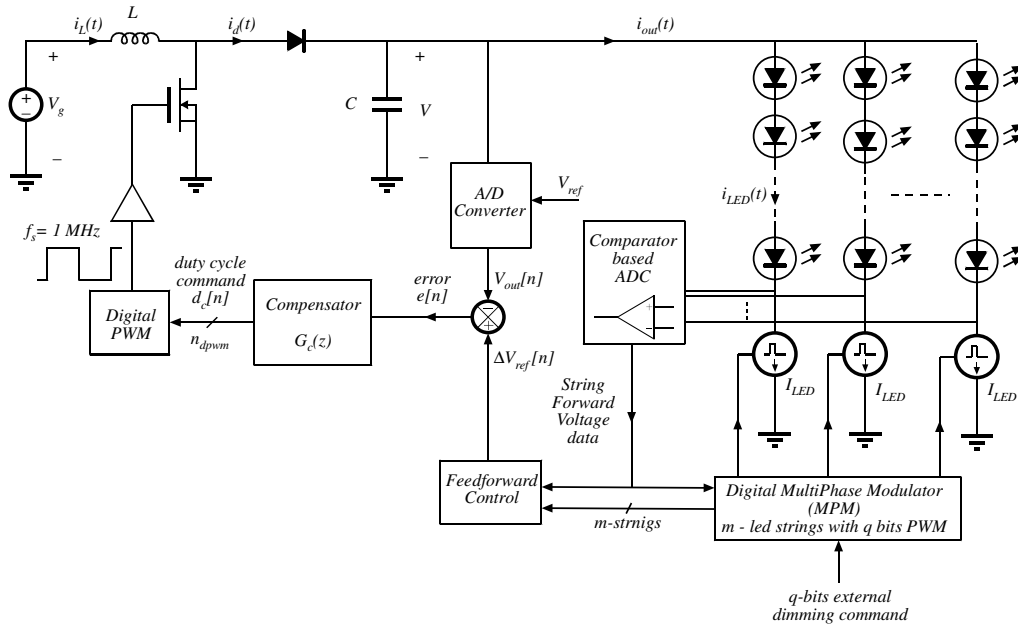


Fig. 1: Digitally controlled parallel LED drive architecture with current regulation and comparator ADC

The key to improving LED drive efficiency is to sense the voltage drop across each individual string, which can vary significantly over manufacturing process and temperature (Table 1), and coordinate with the boost controller for bus voltage regulation. A hardware efficient approach is shown in Fig. 1, where only a single comparator is used for each LED string to detect whether current regulation is active or not. This detection is used for both setting the optimal drive voltage and detecting an LED failure (open or short).

	Min	Typical	Max	Temp Coeff
Red	1.9V	2.1V	2.5V	-2 mV/°C
Green	2.9V	3.2V	3.7V	-2 mV/°C
Blue	2.9V	3.2V	3.7V	-2 mV/°C
8 LED Red	15.2V	16.8V	20V	-
8 LED Green	23.2V	25.6V	29.6V	-

Table 1: Osram MULTILED forward voltage variations

The optimal drive voltage is determined by sweeping the bus voltage to find the point where each LED string current source is on the boundary of regulation. This can be performed at startup or periodically due to the slow nature of changes in the diode forward voltages. Sudden changes in the current source voltage indicate a failure in the LED string and can be used to report a failure and/or actuate control circuitry to mitigate the failure.

The MPM block controls the switching sequence and duty cycle of individual current sources based on the dimming command received. The MPM hardware architecture uses the most significant bits of the dimming level command (duty cycle) to determine the *number* of strings that are active at any point in time [7]. The modulator then rotates *which* strings are active, resulting in a natural phase shifting of the LED string drive signals that

responds immediately to command inputs. The operation of the MPM for 8 phases with two different duty cycles, 80% and 12.5%, is shown in Fig. 2 and Fig. 3. It can be seen that the individual outputs of the MPM are phase shifted in order to avoid large current transients and further, the duty cycle input is directly related to the number of phases that are on simultaneously. For 80% command it can be seen that at any given time 7 out of the eight outputs are on while for 12.5% command only a single output is on.

The ability to control MPM output sequence along with the knowledge of individual string voltages enables the rearrangement of switching sequence of individual outputs to create a suitable voltage profile (Fig. 2 and 3). At low duty cycles this provides an opportunity to reduce the bus voltage to a value less than the maximum, as soon as the string with maximum voltage switches off. This reduces the voltage drop across the current sources, which reduces the power dissipation and hence improves the light load efficiency. As the loading of the converter is predetermined by the MPM sequence, duty cycle command and the current source, the bus voltage can be changed by simple feed-forward control. This is done by adjusting the V_{ref} after the switching of each LED string. In table 2, calculations based on the current experimental setup are made to show the possible improvement in efficiency. The system promises much greater improvement for HB LEDs with a forward current greater than or equal to 350 mA and having a wide manufacturing and temperature variations for dimming commands less than 50 %.

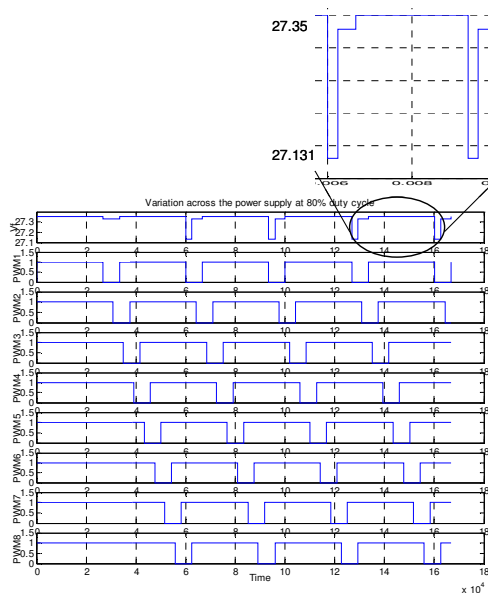


Fig. 2: MPM operating at 80% duty cycle

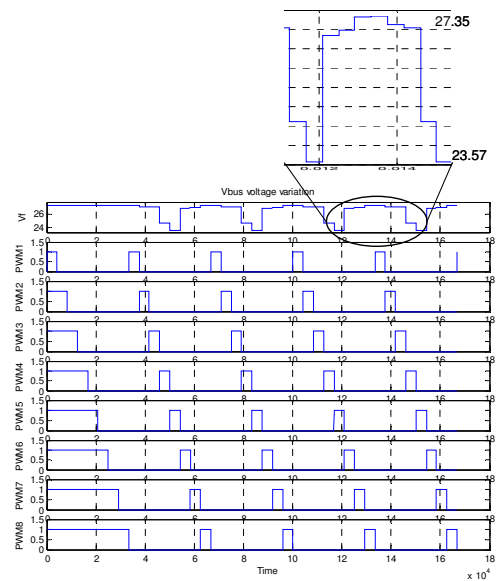


Fig. 3: MPM operating at 12.5% duty cycle

III. EXPERIMENTAL SETUP

A board with 64 Osram MULTILEDs configured in 8 x 8 matrix fashion is built to test the LED drive architecture. The LED board is powered through a power supply and the current through each LED string is regulated to 22 mA through a circuit consisting of controlled current sources built using op-amps and small signal MOSFETs. The digital multi-phase modulation, with a switching frequency of 300 Hz (well above the critical flicker frequency) and 8 bit resolution (256 dimming levels), is implemented through a Virtex-4 FPGA board. The voltage drop across individual LED strings along with the output from the comparator based ADC is given in Fig. 5. In Fig. 6 basic MPM waveforms of 4 phases out of 8 LED strings at a duty cycle of 60 % are shown. It can be inferred from the waveform at any given time all the 4 phases are on. Based on these results and the simulations

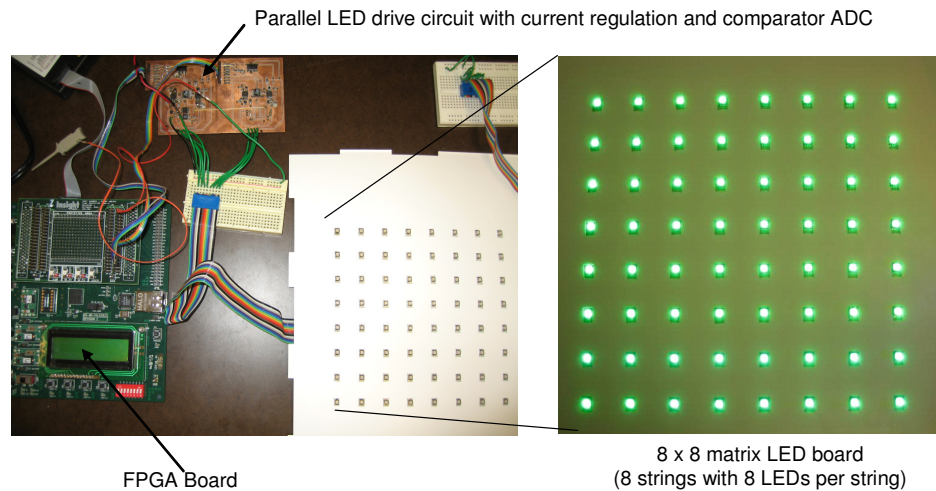


Fig. 4: Experimental setup showing an FPGA control board connected to an LED current source circuit and 8 x 8 matrix LED board with Osram MULTILED running at 22 mA drive current.

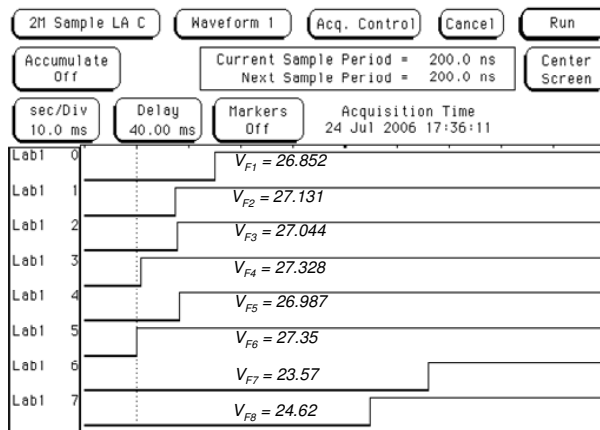


Fig. 5: Comparator based ADC output voltage when input voltage is swept from 30 V to 22 V (low – in regulation, high – out of regulation).

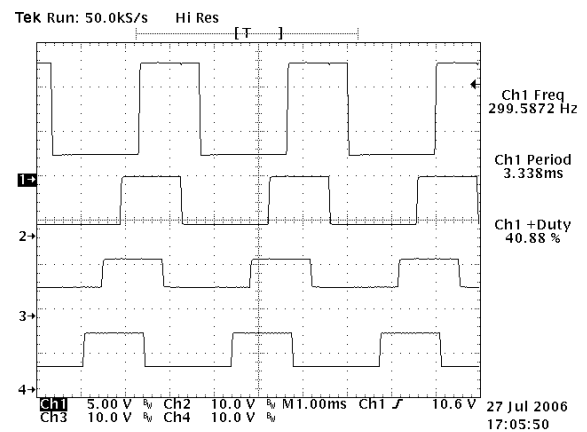


Fig. 6: Voltage across the current sources (low – LED on, high – LED off)

shown in Fig. 2 and Fig. 3 it is possible to calculate the efficiency improvements by calculating the percentage reduction in the average output bus voltage from that of a drive circuit running from a fixed 30 V power supply (Table 2). The comparison at 30 V is based the worst case datasheet tolerance.. Figure 7 shows the output current of the power supply at 5 different dimming levels. Note that the output current has an average value with a small ripple current (max 23 mA), whereas a typical drive approach without phase shifting would result in a pulsed load current of up to n times the single LED string current (8×22 mA in the experimental setup), where n is the number of parallel strings. Ratio of peak current measured for MPM scheme to the peak current (8×22 mA) required to drive the led board using conventional PWM (pulsed current) is used to illustrate factor of improvement

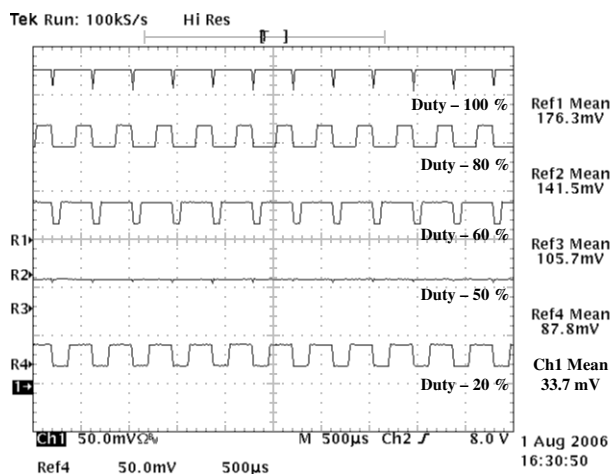


Fig. 7: Average converter output load current with pk-pk ripple of 23 mA (one LED string current)

Duty	Avg. o/p voltage	Efficiency Improvement	$\frac{\text{pk. } I \text{ (mpm)}}{\text{pk. } I \text{ (pulse)}}$
100%	27.35 V	8.834 %	1
80%	27.33 V	8.9 %	0.87
60%	26.99 V	10.034 %	0.666
20%	26.64 V	11.2 %	0.257
12.5%	26.36 V	12.127 %	0.125

Table 2: Efficiency improvements and relative peak current (normalized to peak without phase shifting) at various duty cycles.

IV. CONCLUSION

A complete digital architecture for driving large LED arrays has been presented, which provides the flexibility for a single converter to drive parallel LED strings with high efficiency and relatively continuous output current for reduced EMI and required bus capacitance. The approach utilizes a hardware efficient multi-phase modulator that provides natural phase shifting of the PWM signals to each LED string. A single comparator is used for each LED string to determine the optimal drive voltage and to detect LED failures. This information is used in the modulator to optimize sequencing of the LED strings and to feed-forward load conditions and LED string sequencing to the power converter for dynamic control of the bus voltage. Demonstrated improvements over a traditional approach with constant drive voltage and no phase shifting include reduction of average drive voltage by more than 10% (for same light output) and more than 5 times reduction in converter peak output current