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Document Sections

I. Introduction

II. Forward Voltage Variations and LED Binning

III. Digital Architecture for Driving Large LED Arrays

IV. Experimental Setup

V. Conclusion

Authors

Figures

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Contents

I. Introduction

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Authors

Figures

References

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Digital Architecture for Driving Large LED Arrays with Dynamic Bus Voltage Regulation and Phase Shifted PWM

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***Abstract* – This paper introduces a digital architecture suitable for driving a large number of High Brightness Light Emitting Diodes (HB-LEDs) with improved system efficiency and reduced EMI. Key advantages are achieved by combining and coordinating control of the power converter and LED strings, resulting in a system with deterministic load behavior. Uniform phase shifting of LED strings is performed to minimize load current variations, resulting in reduced output capacitance, improved converter efficiency and reduced system EMI. LED string voltages are detected online and used in a feedforward path for dynamic bus voltage scaling, resulting in improved system efficiency at low dimming levels. Experimental results are presented for a 15 W boost converter with FPGA based digital control driving a 64 LED array with 8 LED strings.**

I. INTRODUCTION

The emergence of HB-LEDs has ushered a new era of solid state lighting solutions that provide distinct performance advantage over conventional lighting technology. Higher optical efficiency, long operating lifetimes, wide operating temperature range and environmentally friendly implementation are some of the key advantages sited in favor of LED technology over incandescent or gas discharge solutions [1, 2]. However, manufacturing variations in forward voltage drop, luminous flux output and peak wavelength necessitate binning strategies resulting in low yield and increased cost [3, 4]. Further, a large number of such LEDs, with matched characteristics arranged in a suitable optical housing, are required to meet the desired optical and luminance performance requirements. Dimming requirements along with the need for circuit compensation techniques to regulate light output over a range of temperature and life time render the simple resistor biased drive solution obsolete for modern LED [5].

Various circuit techniques based on switching and linear regulating devices have been described for driving a single "string" of series LEDs with precise forward current regulation and pulse modulation based dimming techniques [6-8]. Such architectures require a dedicated drive circuit for each LED string, and hence do not scale well with a large number of strings. An integrated solution with multiple current sinks for driving parallel LED strings is described in [9, 10]. The design assumes a separate independent power supply for delivering a shared voltage bus to the parallel LED string.

This work is co-sponsored by the National Science Foundation (under Grant No. 0348772) and industry sponsors of the Colorado Power Electronics Center.

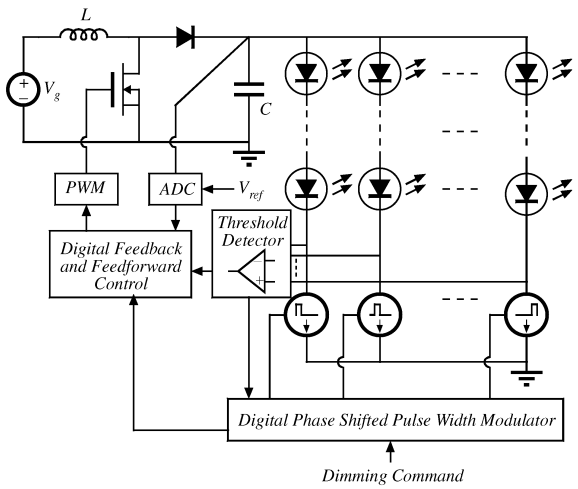


Figure 1. Proposed digital architecture for driving a scalable number of parallel LED strings. The approach integrates both converter control and current regulation of each LED string to facilitate system level optimization.

This paper presents an approach that integrates the controls for both the power converter and parallel LED string current regulation. The architecture, shown in Fig. 1, creates new opportunities for system level optimization by having a single element control both the power delivery and what is now a deterministic load, characterized by the current level and on/off state for each LED string. The system input is a dimming or light level command, which is processed to provide coordinated responses by the converter and LED string current regulation. Key advantages are achieved by performing phase shifted pulse width modulation (PS-PWM) of the LED strings to eliminate pulsed currents from the converter output and dynamic bus voltage regulation for improved efficiency. A hardware efficient digital PWM is adopted from [11, 12] for natural phase shifting of the PWM drive signals to each parallel LED string. Dynamic bus voltage regulation is achieved through feed-forward of load changes from the PS-PWM, active sensing of the required drive voltage for each LED string and optimal sequencing of LED strings.

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A discussion on forward voltage variations and the motivation to perform dynamic voltage scaling is provided in Section II. A complete description of the digital architecture is then provided in Section III followed by experimental result in Section IV based on a test system driving 8 parallel strings of 8 series LEDs, each rated for a forward current of 50 mA. Our conclusions are summarized in Section V.

II. Forward Voltage Variations and LED Binning

One drawback to driving parallel LED strings from a single bus voltage is that series elements are required in each string to block the difference between the string voltage and the bus voltage. In the architecture of Fig. 1, linear current sinks are used for string current regulation and to inherently block the required voltage. A common approach for selecting the bus voltage is to preset a constant value based on the worst case maximum data sheet LED forward voltage drops. Since the power loss in each string is directly proportional to the difference between the bus voltage and the sum of the LED string forward voltage drops, a worst case design results in over design of the power stage and increased driver losses. In order to optimize the power stage design, it is of interest to study the variations expected in forward voltage drop.

HB-LEDs are ternary alloys of III-P and III-N material with high light extraction efficiency. The bandgap voltage across the LED pn-junction required to generate light of particular wavelength is given by

$$h\nu(eV) = \frac{1239.5}{\lambda(nm)}, \quad (1)$$

where $h\nu$ is the semiconductor bandgap energy and λ is the wavelength of the photon emitted (in visible or near UV spectra) [13]. Based on (1) a bandgap of approximately 1.8 V to 2.0 V is required to generate light in amber to red region whereas a bandgap of approximately 2.2 V to 2.9 V is required to generate light in near UV to green region of visible spectra. Table 1, lists the values for forward voltage drop from two LED manufacturers, along with the calculated difference between minimum and maximum values [14, 15]. Over a 30% variation in forward voltage per LED can be expected due to manufacturing variation which then suggests that a similar variation can be expected between worst case and best case LED strings. Common reasons sited for such large variations include the need for various buffer layers along with immature epitaxial growth processes [16, 17].

	Color	Min. (*V*)	Typ. (*V*)	Max. (*V*)	Diff. (*V*)
Luxeon Emitter (350 mA)	Red	2.31	2.95	3.51	1.2
	Green	2.79	3.42	3.99	1.2
	Blue	2.79	3.42	3.99	1.2
Osram MultiLED (20 mA)	Red	1.8	2.1	2.4	0.6
	Green	2.9	3.2	3.7	0.8
	Blue	2.9	3.2	3.7	0.8

Table 1. Datasheet values of LED forward voltages for two HB-LED manufacturers

Bin	Min.(*V*)	Typ.(*V*)
E	2.31	2.55
F	2.55	2.79
G	2.79	3.03
H	3.03	3.27
J	3.27	3.51
K	3.51	3.75
L	3.75	3.99

Table 2. Forward voltage bin structure for all Luxeon emitters and arrays

As the development of manufacturing techniques is slow, such large variations are expected to remain as dominant design considerations. One approach that reduces the demands on the drive circuit is to perform binning of LEDs by optical and electrical characteristics, often resulting in an expensive two step process to bin first for wavelength, then for forward voltage [3, 4, 18]. An example of forward voltage bins available from one manufacturer is given in Table 2, where statistical analysis shows a near uniform distribution of components in all binned categories [3]. An alternative to binning in the manufacturing process is to make the circuit more capable of adapting efficiently to component variations. Dynamic bus voltage regulation in the proposed architecture takes one step in this direction by taking advantage of digital power stage control along with PS-PWM to reduce the losses associated with driving a large array of unsorted LEDs.

III. Digital Architecture for Driving Large LED Arrays

The proposed architecture, shown in Fig. 1, consists of a power converter driving multiple strings of LEDs, controlled current sources, digital multiphase modulator block, threshold detector circuit to sense the voltage drop across each string and digital control logic. The basic operation of each functional block is described below.

A. Digital phase shifted pulse width modulator (PS-PWM)

The PS-PWM block controls the switching sequence and duty cycle of individual current sources based on the digital dimming command (*d bits*) received from microcontroller or color control ASIC. Then for *N* LED strings, the dimming command, *Dim* can be divided into *n* coarse quantization bits (most significant bits, MSB) and '*m*' lower fine quantization bits (least significant bits, LSB), were '*n'* and '*m'* is given by

$$N = 2^n \quad (2)$$

$$m = d - n \quad (3)$$

The PWM hardware architecture uses the MSB portion of the dimming level command to determine the *number* of strings that are active at any point in time [11, 12]. The modulator rotates *which* strings are active, resulting in a natural phase shifting of the LED string drive signals that responds immediately to command inputs. The high resolution LSB portion of the command is added to the trailing edge of coarse pulses to achieve high resolution. The operation of 8 bit PS-PWM for 8 phases (n = 3 and m = 5) with a dimming command of 40% and a period of T_{sLED} corresponding to

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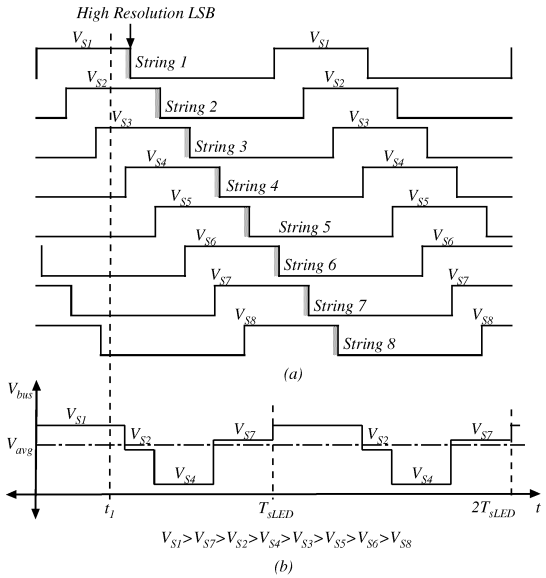


Figure 2(a). PS-PWM operating waveforms at 40% dimming command (*Dim*=0110_0110 {102}, *MSB* = 011 {3}, *LSB* = 0_0110 {6}) illustrating the phase rotation, with three LED strings '*on*' at a given time and the LSB output (shaded area) added to end of each MSB to generate required resolution.

Figure 2(b). Diagram illustrating dynamic bus voltage regulation were the bus voltage is scaled to a value corresponding to the maximum voltage drop across LED strings in regulation.

PWM frequency f_{sLED} is shown in Fig. 2a. It can be seen that the individual outputs of the PS-PWM are phase shifted and the dimming command input is directly related to the number of phases that are on simultaneously, i.e. for 40% command at any given time 3 out of the eight outputs are '*on*'. Further, each phase has an appropriate high resolution LSB portion (shaded area) added to the trailing edge to generate a complete 8-bit resolution dimming command.

The primary advantage of the PS-PWM is that the load current of the power stage has a peak to peak variation less than or equal to just one LED string current over the full range of dimming command. This is in contrast to the output current transients observed with a synchronized or time-delay based PWM, where the load current pulse amplitude is equal to N times one LED string current. The significant reduction in load current pulse amplitude results in reduced converter component requirements, more efficient converter operation in continuous, discontinuous and pulsed operation modes over the dimming range and a significant reduction in the size of the converter output capacitance. An additional benefit of lower current pulses is a reduction in conducted and radiated EMI in the system.

B. Dynamic Bus Voltage Regulation

It was shown in Section II that large manufacturing variations in LED forward voltage and hence LED string voltage can be expected. Dynamic bus voltage regulation is used to improve efficiency by maintaining the bus voltage at the minimum value required to keep all active LED strings in regulation. As shown in Fig. 2(a), the PS-PWM continually rotates through which phases are active for the input command *Dim* < 100%. Thus, the minimum required voltage changes in time according to the active phases. For example, at two extremes: for *Dim* = 1, all phases are on and the required bus voltage is constantly the maximum of the string voltages; for *Dim* = 1/*N*, only one phase is on at a time and the required voltage tracks the forward voltage of each string.

The approach is illustrated in Fig. 2(b), where the forward voltage for each string is indicated as V_{Si}, and i is the string number. The bus voltage plot depicts the dynamics of the required bus voltage for an 8-string system (N = 8) with an input command *Dim* = 40% and assumed relative magnitudes of the string voltages as shown. At time t_1, V_{S1} is dominant, followed by V_{S2}, V_{S4} and V_{S7}. The average bus voltage is lower than the worst case string voltage, resulting in improved efficiency since the load current is same with or without dynamic bus scaling. The efficiency improvement achieved by performing dynamic voltage scaling is given by

$$\Delta\eta = \left(\frac{V_F - V_{avg}}{N \cdot V_F \cdot V_{avg}} \right) \cdot \sum_{i=1}^{N} V_{Si} \qquad (4)$$

where, V_F is fixed (worst-case) bus voltage being used in the comparison and V_{avg} is the average bus voltage with dynamic bus voltage scaling. According to (4), the greatest efficiency improvement comes at low dimming command where V_{avg} is minimum. Note that the circuit requirements can be simplified while maintaining some efficiency improvement by sensing the actual maximum of the string voltages and fixing the bus voltage to that value, as opposed to using worst-case datasheet values. This results in a relatively slow tracking of the bus voltage that is independent of the input *Dim* command.

Additional efficiency improvements can be achieved at low dimming levels by disabling appropriate strings and dynamically changing the number of strings used in the PS-PWM rotation. However, this results in a degradation in the uniformity of the light source and may not be acceptable for applications such as backlighting for LCD-TV.

C. Threshold detector and LED string voltage ordering

A hardware efficient approach for sensing the forward voltage drop across the LED string is shown in Fig. 1. A single comparator is used for each LED string, which compares the voltage across the current sink devices to a known threshold limit. For any voltage greater than the threshold, the current sink maintains a near constant output current. The comparator output changes states whenever the voltage falls below the threshold indicating that the corresponding current sink has dropped out of regulation. Detection is performed by sweeping the power supply bus voltage from a minimum to maximum value in steps equal to the desired groups formed for dynamic voltage scaling. The outputs of the comparator then indicate for each voltage step

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the number of strings that have entered regulation. In this manner, simultaneous forward voltage detection along with ordering of strings is performed. The detection process can be performed at startup or periodically due to the slow nature of changes in the diode forward voltages. The LED strings are then ordered according to the desired dynamic voltage scaling waveshape, e.g. a triangle or sawtooth waveshape.

The same technique can also be used to detect LED failures. An occurrence of an open would cause sudden changes in the current sink voltage that can be easily detected from comparator outputs. On detection of failure, control action can be initiated, which can include complete shut-down or circuit techniques that would be used to mitigate the failure.

It is possible to improve the hardware utilization by using a single comparator with a muxed function implemented at its input. The voltage detection is performed by sweeping the output voltage once per LED string.

D. Power stage design and digital control

Integration of the power stage controller along with dimming logic provides opportunity for system level optimization. The appropriate converter topology depends on the input voltage and number of LEDs per string. A boost topology is shown in Fig. 1 as appropriate for operating from a battery voltage or standardized low voltage bus. A buck topology is more likely when operating from a rectified AC line voltage. Digital control is selected to take greatest advantage of the feedforward and dynamic voltage scaling opportunities facilitated by having direct control of the load [19-21].

A variety of control strategies are possible based on the level of integration and interaction between the boost and load controllers. A straightforward approach is to use a conventional digital boost regulator with ADC, programmable digital PID compensator and digital pulse width modulator (DPWM), with a feedforward command from the LED string PS-PWM controller, as shown in Fig. 1. The feedforward path is used to send the load current and required bus voltage for upcoming load steps. In the simplest case, the boost converter ignores the load current information and uses feedback regulation to track the bus reference voltage command. The response of the regulation loop to reference transients needs to be faster than the LED PS-PWM period. The boost compensator can also be pre-loaded from look-up tables for improved performance based on the known load current change information. Another alternative is to remove the conventional boost regulation loop and ADC altogether and merge the LED and boost control. In this case, the controller could rely more directly on feedforward information with precomputed tables of boost switch timing based on the known load current and voltage steps. The threshold detector could be used in a slow integral loop to track changes in the input voltage or LED string voltages. The experimental results of Section IV are based on a conventional boost regulator with feedforward reference control.

E. Programmable Current Reference and LED Array

The LED luminous flux output and the junction temperature are functions of the LED forward current. It is essential to precisely control LED forward current to meet the desired specifications as well as to prevent thermal run-away. It is has been reported in literature that excessive current ripple could cause thermal cycling and result in premature failure [22]. Hence it is best suited to drive LEDs with a constant current, with minimum or no ripple. In this architecture a linear programmable current sink is used to regulate the LED forward current to a desired level. Amplitude modulation (AM) is achieved by programming the reference current level at which the sink regulates while pulse width modulation is implemented by enabling or disabling the current regulation device. The programmable linear current sink can be constructed using discrete components, as described in section IV, or can be easily integrated on chip using precision programmable current mirrors [9, 10]. Combination of AM and PWM schemes can be then used to achieve a wide dynamic dimming ratio, a feature key to many LED lighting applications.

As the specifications are mentioned in terms of light output, it is important to consider the LED array as an integral part of the architecture. Development of HB-LEDs are taking place in two diverse trends, one involving high power (> 1*W*) large chip area LEDs (1 mm^2) with high flux output [14] and other based on low-power (less than few mW) high efficiency LEDs with moderate flux output [15]. High-power LEDs result in fewer components but significantly increase the cost of optical and thermal design. The proposed topology is suitable for either trend, but emphasizes solutions with a relatively large number of LED strings in parallel. .

IV. Experimental Setup

The complete experimental setup is shown in Fig. 3. The boost converter is designed to output a 40 V signal from 12 V input supply, with a current ripple of 460 mA and output ripple of 100 mV. The output is fed to an LED board, with an array of 64 LEDs split into 8 parallel strings of 8 LEDs each. The measured total forward voltage drop for each LED string at 45 mA is given in Table. 3. The forward current through the LEDs is regulated by a discrete precision programmable current sink, as shown in Fig. 4. Amplitude modulation (AM) is implemented using a programmable voltage source (V_{prog}) the value of which can be set either using analog or digital techniques (using a digital-to-analog converter). An analog SPDT switch, controlled by the PS-PWM module is used to implement PWM dimming techniques. For demonstrating just PS-PWM operation, V_{prog} reference is fixed to a bandgap value and the LED string current is regulated to a value of

V_{s1}	V_{s2}	V_{s3}	V_{s4}	V_{s5}	V_{s6}	V_{s7}	V_{s8}
31.7	29.4	29.3	27.7	26.6	25.9	25	21.9

Table 3. Measured LED string forward voltage drop

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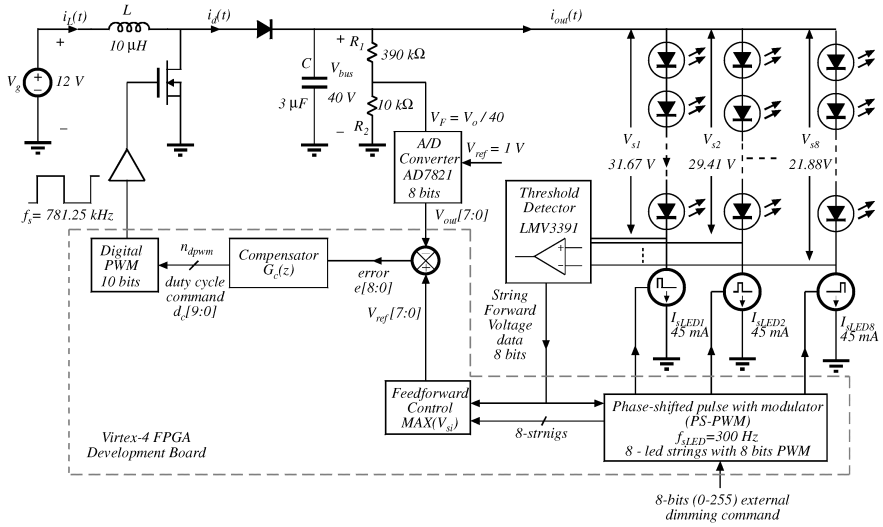


Figure 3. Experimental setup, consisting of a 15 W boost converter, 64 Osram MULTILEDs, linear programmable current regulator, 8-bit half-flash ADC, comparator based threshold detector circuit and digital PS-PWM and control logic implemented on Virtex-4 FPGA

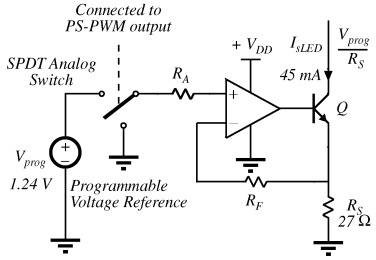


Figure. 4. An op-amp based precision programmable current sink with AM and PWM control options

45 mA by the choice of appropriate resistor, R_s. Note that the threshold voltage of the current sink is determined by the reference voltage, equal to the bandgap value in this case. An 8-bit (256 steps) 300 Hz PS-PWM is implemented on FPGA to control the operation of individual current sinks. An external dimming command, received by the PS-PWM module, is used to determine the appropriate phase-shift and duty cycle of individual control output signals. Figures 5 and 6 illustrate operation of PS-PWM for two dimming commands of *Dim* = 93.7% and *Dim* = 50%, respectively. In each case,3 out of the 8 string currents and the total current are plotted. It can be seen that there is a uniform phase shift between the commands issued for each phase. Recall from Section III.A. that the peak-to-peak load current amplitude is limited by the PS-PWM block to just one LED string regulation current (45 mA). The LSB portion of the *Dim* command determines the percent of time the load current is in two adjacent positions. This is seen in Figures 5 and 6, where the LSB portion of the command is 50% and 0%, respectively. No large *di/dt* transitions occur in the output current over the complete range of dimming, allowing use of a small output capacitor *C* and resulting in low system EMI.

The functioning of threshold detector block is summarized by waveforms shown in Fig. 7 consisting of boost output voltage and 3 of the 8 comparator outputs. The boost output voltage is swept from a value of 24 V up to 34 V in steps of 2 V. The comparator output changes states as soon as the bus voltage exceeds the sum of the forward voltage drop across the LED string and the current sink threshold voltage. The outputs are then latched by the FPGA and stored in a memory to perform feedforward operation. A forward voltage drop sensed by the comparator for individual strings is in close

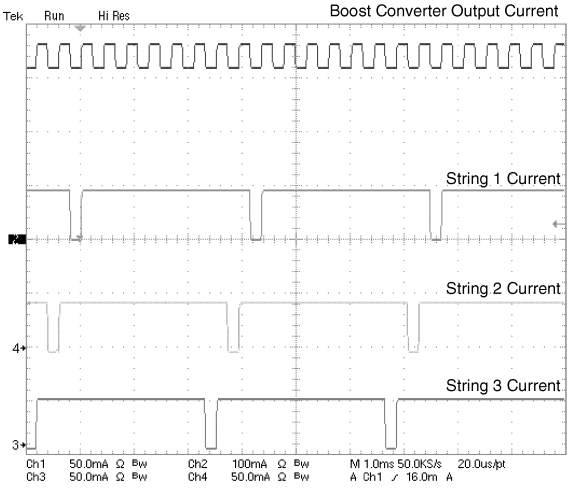


Figure 5. Experimental system waveforms demonstrating operation of the PS-PWM block at an input command *Dim* = 93.7%. Current waveforms are shown for the boost converter output and 3 of the 8 LED string currents.

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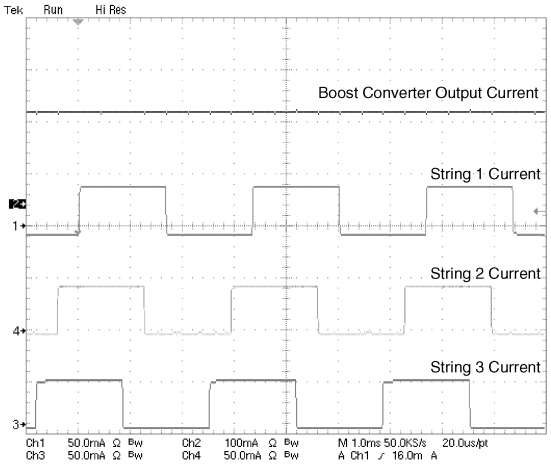


Figure. 6. Experimental system waveforms demonstrating operation of the PS-PWM block at an input command *Dim* = 50%. Current waveforms are shown for the boost converter output and 3 of the 8 LED string currents.

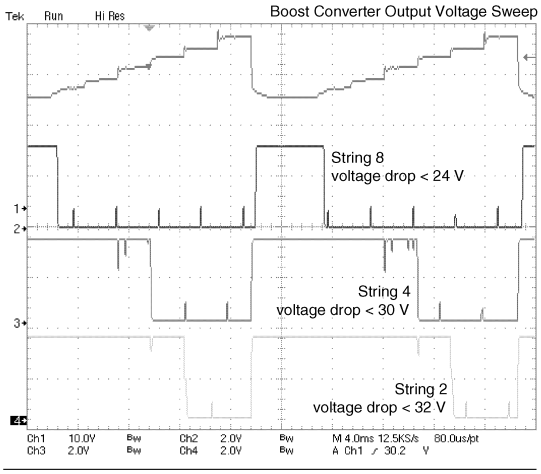
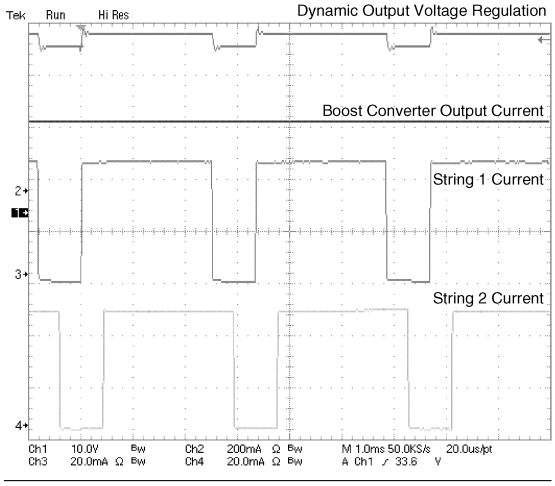


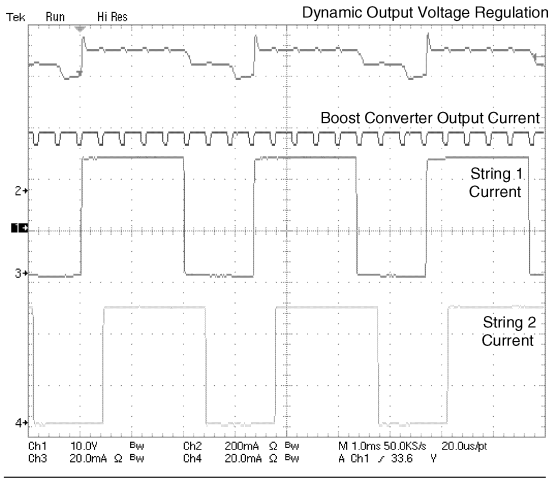
Figure 7. Experimental waveforms illustrating threshold detection during initialization. Shown are the converter output voltage and comparator outputs for three of the LED strings with varying forward voltages according to Table 3.

agreement with the actual forward voltage drop listed in Table 3.

Figure 8 demonstrates complete operation of the system at two dimming levels including LED string PS-PWM and dynamic bus voltage regulation based on feedforward of string data collected by performing threshold detection at initialization. The boost converter output voltage scales along with the dimming command and PS-PWM operation to the lowest possible value for the given number of strings that are '*on*'. Note that the voltage scaling operation does not adversely affect the LED string currents, which are well regulated to the nominal value. Based on the data collected,



(a)



(b)

Figure 8. Dynamic voltage regulation illustrated at two input commands: (a) *Dim* = 80% and (b) Dim = 60%. Current waveforms are shown for the boost converter output and 2 LED strings that belong to different voltage groups

the efficiency improvement over fixed bus voltage drive is calculated. Figure 9 summarizes the experimental efficiency improvement and compares it with the theoretically calculated value based on (4). The fixed bus voltage used for comparison is V_F = 35 V, based on worst case datasheet values. Up to 14% experimental improvement in efficiency is observed at a duty command of 12.5%. Overall, the experimental efficiency improvement is about 4% below the theoretical, primarily due to the finite number of voltage levels used to group the LEDs and the rise and fall time performance of the converter waveforms.

V. Conclusion

An architecture is presented suitable for efficient drive of a scalable number of parallel LED strings. Key advantages are

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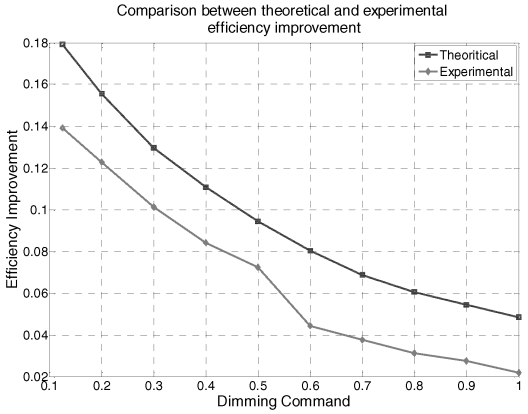


Figure 9. Plot of theoretical and experimental improvement in efficiency ($\Delta\eta$) as a result of dynamic voltage scaling over an assumed fixed bus voltage of $V_F = 35$ V.

achieved by combining and coordinating control of the power converter and LED strings, resulting in a system with deterministic load behavior. Uniform phase shifting of LED strings is performed to minimize load current variations, resulting in reduced output capacitance, improved converter efficiency and reduced system EMI. LED string voltages are detected online and used in a feedforward path for dynamic bus voltage scaling, resulting in improved system efficiency at low dimming levels. Experimental results are presented for a 15 W boost converter with FPGA based digital control driving a 64 LED array with 8 LED strings.

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