

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

VIZIO, INC.,
Petitioner,

v.

POLARIS POWERLED TECHs, LLC,
Patent Owner.

IPR2024-00073
Patent 7,843,148 B2

Before JOHN F. HORVATH, DANIEL J. GALLIGAN and
KARA L. SZPONDOWSKI, *Administrative Patent Judges*.

HORVATH, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

A. *Background and Summary*

Vizio, Inc. (“Petitioner”) filed a Petition requesting *inter partes* review of claims 1–22 (“the challenged claims”) of U.S. Patent No. 7,843,148 B2 (Ex. 1001, “the ’148 patent”). Paper 1 (“Pet.”), 16. Polaris PowerLED Technologies, LLC (“Patent Owner”) did not file a Preliminary Response in the period allotted for filing such a response. *See* Paper 3 (filing notice dated October 27, 2023); 37 C.F.R. § 42.107(b) (allowing a preliminary response to be filed within 3 months of this date). We have jurisdiction and authority under 35 U.S.C. §§ 6, 314 and 37 C.F.R. § 42.4.

Upon consideration of the Petition, we are persuaded that Petitioner has demonstrated a reasonable likelihood that it would prevail in showing the unpatentability of at least one challenged claim, and we institute *inter partes* review of all challenged claims on all grounds raised.

B. *Real Parties-in-Interest*

Petitioner and Patent Owner identifies themselves, respectively, as the real parties-in-interest. Pet. 85; Paper 4, 1.

C. *Related Matters*

Petitioner and Patent Owner identify *Polaris PowerLED Techs, LLC v. Vizio, Inc.*, 2:23-cv-03478 (C.D. Cal.), as a district court proceeding that can affect or be affected by this proceeding. Pet. 86; Paper 4, 1.

D. *The ’148 Patent*

The ’148 patent is directed to a “light emitting diode (LED) driver that drives LEDs in parallel.” Ex. 1001, 1:6–7. Such a driver is illustrated in Figure 4, which is reproduced below.

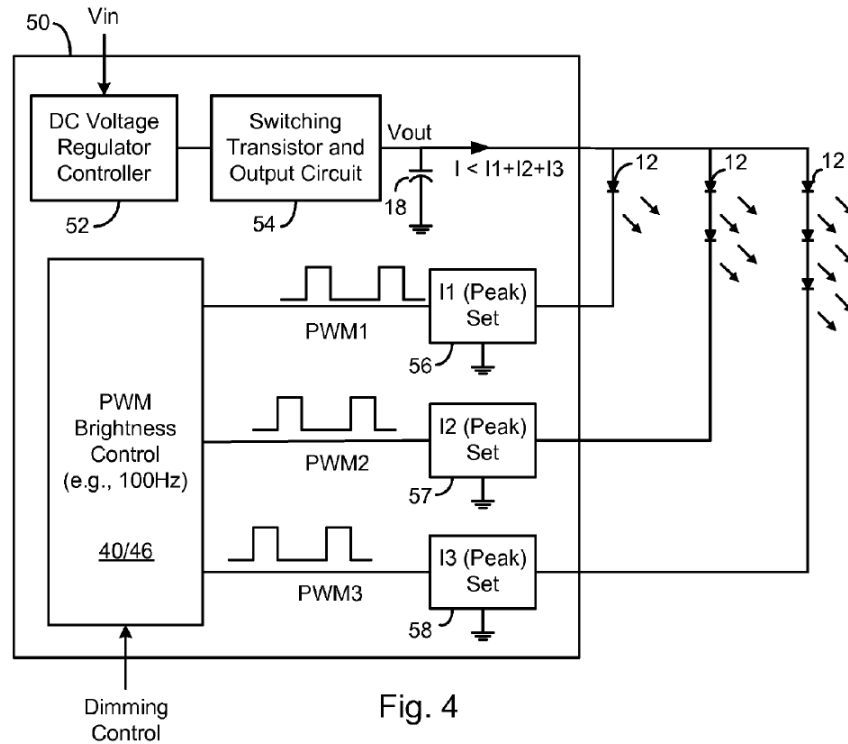


Fig. 4

Figure 4 is a schematic illustration of an LED driver that powers three parallel LED strings 12. *Id.* at 5:12–25. LED driver 50 includes DC voltage regulator controller 52, switching transistor and output circuit 54, capacitor 18, pulse width modulating (PWM) brightness controller 40/46, and current set circuits 56–58. *Id.* at 5:26–57. DC voltage regulator controller 52 “may be a boost regulator controller, a buck regulator controller, or any other type of regulator controller needed to generate an output voltage (V_{out}) that exceeds the forward voltage drop for each parallel path of LEDs.” *Id.* at 5:26–30. It generates a high frequency PWM signal that turns the switching transistor on and off with a duty cycle that determines V_{out} . *Id.* at 5:31–34.

Although all parallel LED paths 12 are energized by the same voltage V_{out} , they may draw different currents that are determined by current set circuits 56–58 that are selectively “enabled and disabled by their associated staggered PWM brightness control signal[s] PWM1, PWM2, [and] PWM3.” *Id.* at 5:48–52. Figures 5 and 6, which illustrate different embodiments of

current set circuits 56–58, are reproduced below. *Id.* at 5:58–59, 6:7–8.

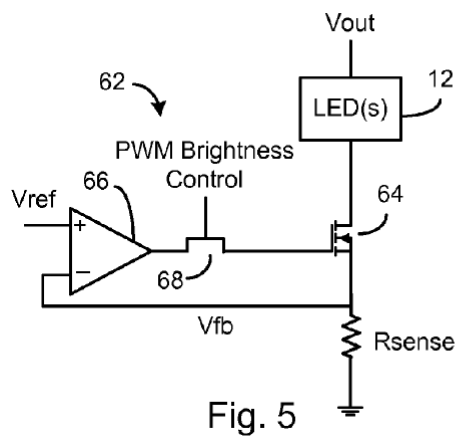


Fig. 5

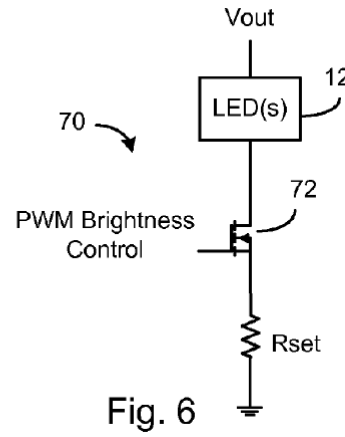


Fig. 6

Figures 5 (left) and 6 (right) are schematic illustrations of different embodiments of current set circuits 56–58 shown in Figure 4. *Id.*

In the Figure 5 embodiment, a “low value sense resistor (R_{sense}) and MOSFET 64 are connected in series with the one or more LEDs 12.” *Id.* at 5:59–61. The voltage V_{fb} across R_{sense} , which is “proportional to the current through the LEDs, is applied to an inverting input of an op amp 66.” *Id.* at 5:62–64. Op amp 66 is configured as a comparator and its non-inverting input “is coupled to a reference voltage (V_{ref}).” *Id.* at 5:64–65. The output of op-amp 66 is coupled to the gate of MOSFET 64 during the positive phase of the PWM brightness control signal via pass transistor 68. *Id.* at 6:3–6. When pass transistor 68 is enabled, op amp 66 “controls the gate voltage of the MOSFET 64 to cause V_{fb} to equal V_{ref} ,” thereby limiting the current flowing through LED string 12 to V_{ref}/R_{sense} . *Id.* at 5:65–66.

In the Figure 6 embodiment, a “current set resistor R_{set} and MOSFET 72 are connected in series with the one or more LEDs 12.” *Id.* at 6:9–10. MOSFET 72 is enabled during the positive phase of the PWM brightness

control signal, limiting the current flowing through LED string 12 to V_{out}/R_{set} . *Id.* at 6:11–16.

PWM brightness controller 40/46 generates “stagger[ed] PWM brightness control signals” and supplies them to different parallel LED paths. *Id.* at 4:3–4. “The LEDs in each path are switched on and off in accordance with the PWM duty cycle to create a certain perceived brightness level, but the paths are energized at different times” determined by the different phases of the staggered PWM brightness control signals. *Id.* at 4:4–7. An N-bit shift register can generate the staggered PWM brightness control signals, where “[t]he number of [shift register] bits determines the fineness in selecting PWM brightness control signal duty cycles.” *Id.* at 4:13–15. Such a shift register is shown in Figure 2A, which is reproduced below.

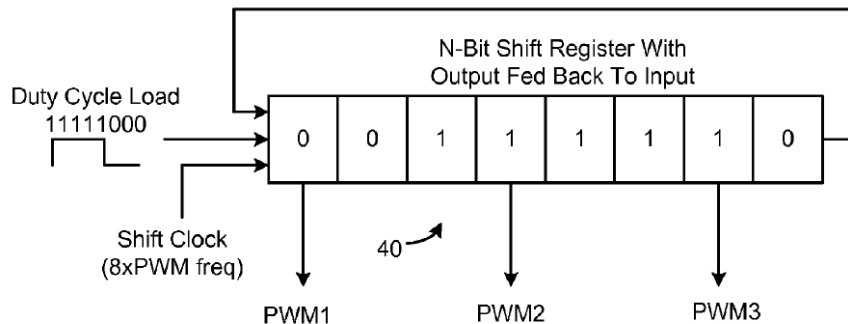


Fig. 2A

Figure 2A is a schematic illustration of an 8-bit shift register that can be used to generate staggered PWM signals. *Id.* at 4:31–32. An eight-bit word loaded into the shift-register determines the duty cycle of the staggered PWM signals. *Id.* at 4:31–33. A shift clock having a frequency that is 8 times the frequency of the generated PWM signal “shift[s] the bit pattern to the right for every shift clock cycle.” *Id.* at 4:34–37. “The PWM brightness control signals for each parallel path of LEDs are tapped from different

positions along the shift register 40,” creating a plurality of staggered PWM brightness control signals. *Id.* at 4:43–46. For example, as shown in Figure 2A, staggered signals PWM1, PWM2, and PWM3 are obtained by tapping shift register 40 at locations 0, 3, and 6. *Id.* at 49–51. The three PWM signals generated in this way all have a 62.5% duty cycle that is determined by the duty cycle word (11111000) that is loaded into shift register 40 and have staggered or phase-shifted start times that are determined by the shift register locations from which they are tapped. *Id.* at 4:51–52. The staggered PWM signals obtained from each tap are shown in Figure 2B, which is reproduced below.

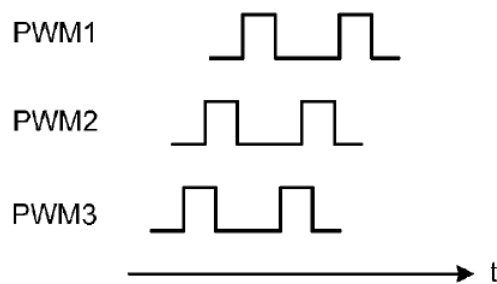


Fig. 2B

Figure 2B is a schematic illustration of staggered PWM signals having the same duty cycle but phase-shifted start times that are obtained by tapping an N-bit shift register at different shift register locations. *Id.* at 4:55–57.

E. Illustrative Claim

Claims 1 and 14 are independent claims, reciting a light emitting diode (LED) driver and a method for driving LEDs, respectively. Ex. 1001, 6:35–54, 7:51–8:8. Claims 2–13 depend directly or indirectly from claim 1 and claims 15–22 depend directly or indirectly from claim 14. *Id.* at 6:55–7:50, 8:9–58. Claim 1 is illustrative of the challenged claims and is reproduced below.

1. A light emitting diode (LED) driver for driving LEDs connected to different parallel paths, the driver comprising:
 - a voltage source for connection to first ends of LEDs in a plurality of parallel paths;
 - a plurality of current set circuits, one current set circuit per parallel path, each current set circuit controlling a peak current through one or more LEDs connected in each parallel path; and
 - a pulse-width modulated (PWM) brightness control signal generator connected to the plurality of current set circuits, the brightness control signal generator being configured to generate staggered PWM brightness control signals to the plurality of current set circuits,
 - each current set circuit being configured to draw the peak current through its associated one or more LEDs at a duty cycle substantially corresponding to a duty cycle of a PWM brightness control signal applied to it, such that the plurality of current set circuits conduct current through their associated one or more LEDs at the same duty cycle but out of phase with each other.

Id. at 7:35–54.

F. Evidence

	Reference	Date	Exhibit
Thomas	US 5,317,307 B2	May 31, 1994	1005
Zane	<i>Digital Architecture for Driving Large LED Arrays with Dynamic Bus Voltage Regulation and Phase Shifted PWM</i> , Montu Doshi and Regan Zane ¹	Mar. 1, 2007	1006

¹ Petitioner contends an electronic copy of this paper was made publicly available to over 2,500 registered attendees of the 22nd Annual IEEE Applied Power Electronics Conference and Exposition, held in Anaheim, CA from February 25, 2007 until March 1, 2007. At this stage of the proceeding, based on our review of Petitioner’s supporting evidence, we find that Petitioner has shown a reasonable likelihood that Zane qualifies as a prior art

Reference		Date	Exhibit
Tatewaki	US 6,402,354 B1	June 11, 2002	1007

Petitioner also relies upon the Declaration of Regan Zane, Ph.D.
(Ex.1003).

G. Asserted Grounds

Petitioner asserts the challenged claims are unpatentable on the
following grounds (Pet. 17):

Claims Challenged	35 U.S.C. §	Reference(s)/Basis
1, 3, 7, 9–12, 14, 17, 18, 20–22	102	Thomas
1, 3, 6, 7, 9–12, 14, 17, 18, 20–22	103(a)	Thomas
2, 13, 15	103(a)	Thomas, AAPA ²
8, 19	103(a)	Thomas, Tatewaki
1–4, 11, 12, 14, 17, 22	102	Zane
1–4, 5, 11–17, 22	103(a)	Zane

II. ANALYSIS

A. Level of Ordinary Skill in the Art

Petitioner identifies a person of skill in the art (“POSITA”) at the time of the invention as someone that would have had “a bachelor’s degree in physics, electrical engineering, or a related field, and approximately two years of experience in the fields of LED technology, backlights, LED devices and control thereof, or other related fields.” Pet. 16 (citing Ex. 1003 ¶¶ 34–35). Petitioner further contends that “advanced education in the fields of physics, electrical engineering, or a related field can compensate for lesser

printed publication. *See* Ex. 1003 ¶ 46 and Exs. 1016–19; *Hulu, LLC v. Sound View Innovations, LLC*, IPR2018-01039, Paper 29 at 13 (PTAB Dec. 20, 2019) (precedential).

² Applicant Admitted Prior Art

work experience in the relevant fields” and that the merits of the Petition “do[] not turn on this specific definition of the level of ordinary skill.” *Id.*

“[T]he level of skill in the art is a prism or lens through which a judge, jury, or the Board views the prior art and the claimed invention.” *Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001). At this stage of the proceeding, we find Petitioner’s assessment of the level of skill in the art to be reasonable and commensurate with the problems and solutions disclosed in the prior art. *See In re GPAC Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995). Accordingly, for purposes of this Decision, we adopt Petitioner’s description as our own.³

B. Claim Construction

In *inter partes* reviews, we interpret a claim “using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. 282(b).” 37 C.F.R. § 42.100(b) (2019). Under this standard, a claim is construed “in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.” *Id.* Only claim terms which are in controversy need to be construed and only to the extent necessary to resolve the controversy. However, “[t]he Board is required to construe ‘only those terms . . . that are in controversy, and only to the extent necessary to resolve the controversy.’” *Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) (internal citations omitted).

Petitioner contends “no claim terms need to be expressly construed to resolve the invalidity issues in this Petition.” Pet. 16. At this stage of the

³ We omit the open-ended phrase “at least” that is included in Petitioner’s definition.

proceeding, because no claim terms are in dispute or appear to require express construction, we decline to expressly construe any claim term. *See Realtime Data*, 912 F.3d at 1375.

C. Anticipation by Thomas

Petitioner contends claims 1, 3, 7, 9–12, 14, 17, 18, and 20–22 are anticipated by Thomas. Pet. 17–45. For the reasons discussed below, we find Petitioner demonstrates a reasonable likelihood of showing these claims are anticipated by Thomas.

1. Thomas

Thomas discloses “a method and an apparatus for power demand load leveling of a power supply driving a plurality of LED’s through the use of pulse width modulation.” Ex. 1005, 2:18–21. Thomas’s apparatus is illustrated in Figure 1, reproduced below.

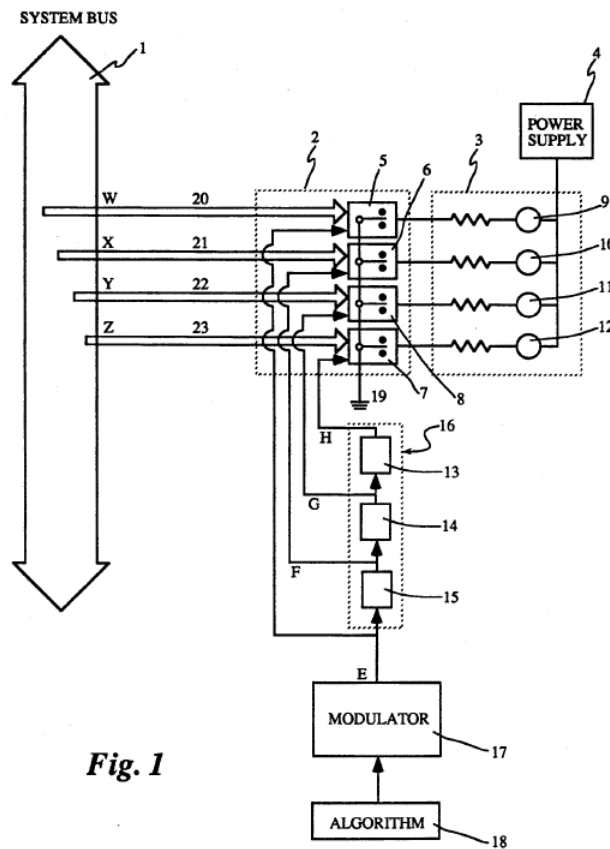


Figure 1 of Thomas is a block diagram of Thomas's load-leveling apparatus. *Id.* at 2:66–3:2. A plurality of control signals (W–Z) are transmitted to a plurality of LED groups (9–12) through a plurality of activation switches (5–8). *Id.* at 3:28–32. When enabled, switches 5–8 allow current to flow to LED groups 9–12 from power supply 4. *Id.* at 3:32–45. To reduce the current demand on power supply 4, modulator 17 presents “a first modulating signal E to a delay means (16), to generate a predetermined number of delayed modulating signals (F, G, H).” *Id.* at 3:63–67. Activation switches 5–8 are turned “on and off according to the input of the respective control signal [W, X, Y, Z] and modulating signal [E, F, G, H].” *Id.* at 4:65–5:8. “Because the modulating signals (E, F, G, H) vary in phase . . . each set of activation switches (5–8) is sequentially turned on . . . so that no more than one group of LED's . . . is activated (or switched on) at any one time.” *Id.* at 5:13–20. Further details of Thomas's apparatus are shown in Figure 2, which is reproduced below.

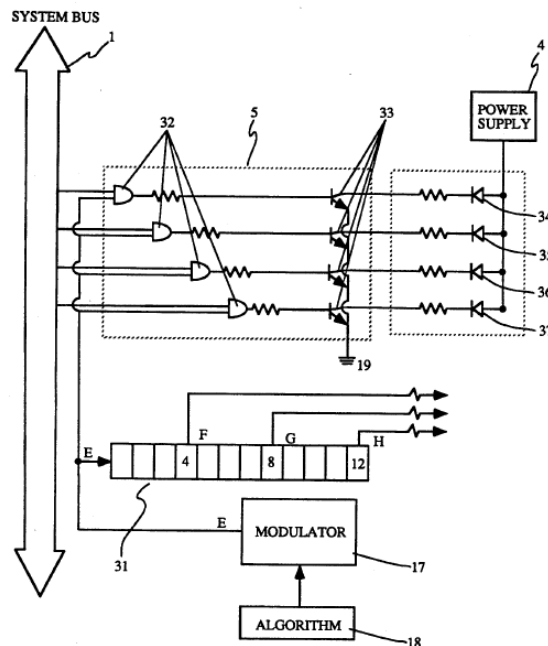


Fig. 2

Figure 2 of Thomas is a “partial circuit diagram . . . showing one group of four LED’s with their respective control lines and control devices.” *Id.* at 3:3–5. Figure 2 differs from Figure 1 in that it shows “only one group of LED’s (9) with a corresponding set of switches (5)” consisting of “gating control logic (32) forming AND gates and transistors (33).” *Id.* at 3:32–35, 4:17–19. The AND gates receive a control signal W (not shown) and PWM modulating signal (E) as input and, when enabled, “generate output to their respective transistors (33)” that enable the transistors in order to “provide current from the power supply (4) for activating the associated LED’s (34–37) in the group of LED’s (9).” *Id.* at 3:39–45.

Figure 2 also differs from Figure 1 in that it illustrates Figure 1’s delay element 16 as a “twelve bit shift register (31) [that] is used to generate the delayed modulating signals (F, G, H).” *Id.* at 4:19–21. Shift register 31 “sequentially stor[es] twelve binary values corresponding to the pulses or lack of pulses in the first modulating signal (E)” and generates signals (F, G, H) “by tapping the values stored within the fourth, eighth, and twelfth cells of the shift register (31).” *Id.* at 4:21–26. As shown in Thomas’s Figure 3, when signals (F, G, H) are generated in this way, they are identical to signal (E) but phase-shifted by (25, 50, 75) percent of the period T of signal (E). *Id.* at 4:51–59, Fig. 3.

2. *Claims 1 and 14*

Claim 1 recites a light emitting diode (LED) driver for driving LEDs connected to different parallel paths. Ex. 1001, 6:35–36. At this stage of the proceeding, Petitioner reasonably demonstrates how Thomas discloses such an LED driver. Pet. 17–23 (citing Ex. 1005, 2:18–21, 3:3–5, 3:12–15, 3:24–45, 5:11–13, Figs. 1, 2). The LED driver shown in Figures 1 and 2 of

Thomas drives LED groups 9–12, each consisting of a plurality of LEDs 34–37, in parallel as required by the preamble.⁴ Ex. 1005, Figs. 1, 2.

Claim 1 requires the LED driver to include a voltage source connected to first ends of the LEDs in the plurality of parallel paths. Ex. 1001, 6:37–38. At this stage of the proceeding, Petitioner reasonably demonstrates how Thomas’s LED driver includes such a voltage source. Pet. 23–25 (citing Ex. 1005, 3:12–15, 3:42–45, Figs. 1, 2). Figures 1 and 2 of Thomas illustrate power supply 4 connected to the first ends of parallel LED groups 9–12, each group consisting of a plurality of parallel LEDs 34–37. Ex. 1005, Figs. 1, 2.

Claim 1 further requires the LED driver to include a plurality of current set circuits, one per parallel path, for controlling a peak current through one or more LEDs in each parallel path. Ex. 1001, 6:39–42. At this stage of the proceeding, Petitioner reasonably demonstrates how Thomas’s LED driver includes such a plurality of current set circuits. Pet. 25–26 (citing Ex. 1003 ¶¶ 62–63; Ex. 1005, Figs. 1, 2). Figures 1 and 2 of Thomas show each of Thomas’s parallel LED paths include a resistor 3 coupling the LEDs in the path to ground such that current from power supply 4 flows through the LEDs and resistor 3 to ground. Ex. 1005, Figs. 1, 2. On this record, we are persuaded by Petitioner’s contention, supported by the testimony of Petitioner’s declarant, that a person skilled in the art

would have understood from Thomas’ disclosure that the purpose of those resistors is to limit the current flowing through each of the parallel paths of LEDs to a peak current I , based on the resistance R of the resistor, the voltage V output by the

⁴ Because Petitioner demonstrates how Thomas discloses the preamble, we need not decide whether the preamble is limiting.

power supply, [and] the voltage drop across the LED [according to] the equation $I = (V - V_{LED})/R$.

Pet. 26 (citing Ex. 1003 ¶ 63). We note that the '148 patent itself identifies a resistor in series with one or more LEDs in an LED string as a current set circuit. Ex. 1001, 6:7–13, Fig. 6.

Claim 1 further requires the LED driver to include a PWM brightness control signal generator connected to the plurality of current set circuits configured to generate staggered PWM brightness control signals to the plurality of current set circuits. Ex. 1001, 6:43–47. At this stage of the proceeding, Petitioner reasonably demonstrates how Thomas's LED driver includes such a PWM signal generator. Pet. 27–29 (citing Ex. 1005, 1:23–42, 3:46–4:18, Figs. 1, 3). Figure 1 of Thomas illustrates a pulse width modulator 17 that generates and provides PWM signal E to delay means 16, which generates staggered PWM signals F–H. Ex. 1005, Fig. 1. Together, PWM modulator 17 and delay means 16 are a PWM control signal generator that is coupled to the plurality of current set circuits (resistors 3) via switches 5–8 that generates staggered PWM control signals E–H to the current set circuits . *Id.*

Finally, claim 1 requires each current set circuit of the LED driver be configured to draw the peak current through its LEDs at a duty cycle substantially corresponding to a duty cycle of the PWM brightness control signal applied to it but out of phase with the other current set circuits. Ex. 1001, 6:48–54. At this stage of the proceeding, Petitioner reasonably demonstrates how Thomas's current set circuits meet this limitation. Pet. 30–32 (citing Ex. 1005, 3:24–63, 4:66–5:20, Figs. 1, 3). Figure 3 of Thomas illustrates that each of the PWM control signals E–H generated by Thomas's PWM controller (PWM generator 17 and delay means 16) has the same duty

cycle but a different phase. Figure 1 illustrates that each of PWM control signals E–H is coupled to a different current set circuit (resistor 3) through a respective one of switches 5–8, such that each current set circuit draws current through a respective LED group 9–12 at the same duty cycle, but out of phase with the other current set circuits. Ex. 1005, Figs. 1, 3.

At this stage of the proceeding, for the reasons discussed above, we find Petitioner has demonstrated a reasonable likelihood of showing all the limitations of claim 1 are taught by Thomas and that claim 1 is anticipated by Thomas. Claim 14 is substantially similar to claim 1, reciting a method for driving a plurality of LEDs in a plurality of parallel paths that is substantially similar to the method the LED driver of claim 1 is configured to perform. *Compare* Ex. 1001, 7:51–8:8, *with id.* at 6:35–54. Petitioner’s analysis of claim 14 refers back to its analysis of claim 1. Accordingly, at this stage of the proceeding, Petitioner demonstrates a reasonable likelihood of showing claim 14 is anticipated by Thomas.

3. *Claims 3, 7, 9–12, 17, 18, and 20–22*

Claims 3, 7, 9, 10–12 recite additional limitations for drivers configured to drive a plurality of LEDs in a plurality of parallel paths, and claims 17, 18, and 20–22 recite corresponding methods performed by those drivers. We have reviewed Petitioner’s contentions that these claims are anticipated by Thomas (Pet. 32–45) and find, at this stage of the proceeding, that Petitioner demonstrates a reasonable likelihood of showing these claims are anticipated by Thomas.

D. *Remaining Challenges*

As noted above, in addition to challenging various claims of the ’148 patent as anticipated by Thomas, Petitioner challenges claims as obvious over Thomas alone or over Thomas combined with AAPA or Tatewaki and

also challenges claims as anticipated by or obvious over Zane. Because Patent Owner does not contest any of these challenges at this stage of the proceeding and because Petitioner has demonstrated that it is reasonably likely to be able to show at least one of the challenged claims is unpatentable for the reasons discussed above, we need not review Petitioner's remaining challenges. *See* 35 U.S.C. § 314(a) ("The Director may not authorize an *inter partes* review to be instituted unless . . . there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.").

III. CONCLUSION

We have reviewed the Petition, and have considered all of the evidence and arguments presented by Petitioner. We find, on this record, Petitioner has demonstrated a reasonable likelihood of showing at least one claim of the '148 patent is unpatentable, and we institute *inter partes* review of all claims on all grounds raised in the Petition.

The Board has not yet made a final determination with respect to any claim construction issue or the patentability of any challenged claim.

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that, pursuant to 35 U.S.C. § 314, an *inter partes* review is hereby instituted on all challenged claims on all grounds; and

FURTHER ORDERED that, pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial commencing on the entry date of this Decision.

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