Filed October 20, 2023

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

VIZIO, INC.,
Petitioner
v.
POLARIS POWERLED TECHNOLOGIES, LLC
Patent Owner

IPR2024-00073
Patent No. 7,843,148

CORRECTED PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 7,843,148

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EXHIBIT LIST

Exhibit No.	Description
1001	U.S. Patent No. 7,843,148 to Gater et al.
1002	Prosecution History of U.S. Pat. No. 7,843,148
1003	Declaration of Regan A. Zane, Ph.D.
1004	Regan Zane Curriculum Vitae
1005	U.S. Patent No. 5,317,307 to Thomas, Jr. ("Thomas")
1006	Montu Doshi & Regan Zane, "Digital Architecture for Driving Large LED Arrays with Dynamic Bus Voltage Regulation and Phase Shifted PWM," APEC 07 ("*Zane*")
1007	U.S. Patent No. 6,402,354 to Tatewaki et al. ("Tatewaki")
1008	Excerpts from Paul Horowitz & Winfield Hill, *The Art of Electronics* (2nd ed. 1989)
1009	Declaration of Rachel J. Watters re *The Art of Electronics*
1010	U.S. Patent No. 3,972,031 to Riemenschneider et al.
1011	Excerpt from Noel M. Morris, *Digital Electronic Circuits and Systems* (The Macmillan Press Ltd. 1974)
1012	UK Patent Application Publication GB 2459009A to Gater et al.
1013	PDF Printout dated October 6, 2023 of Case Details for GB2459009 from UK Intellectual Property Office website, available at https://www.ipo.gov.uk/p-ipsum/Case/PublicationNumber/GB2459009 (
1014	Excerpt from *Comprehensive Dictionary of Electrical Engineering* (2nd ed. 2005)
1015	Plaintiff's Disclosure of Asserted Claims and Infringement Contentions Against VIZIO Pursuant to Northern District

Exhibit No.	Description
	of California Patent Local Rules 3-1 and 3-2, in *Polaris PowerLED Technologies, LLC v. VIZIO, Inc. et al.*, No. 2:23-cv-03478-GW-PDx
1016	Montu Doshi & Regan Zane, "Digital Architecture for Driving Large LED Arrays with Dynamic Bus Voltage Regulation and Phase Shifted PWM," APEC 07 Digest
1017	Table of Contents for APEC 07
1018	Montu Doshi & Regan Zane, "Digital Architecture for Driving Large LED Arrays with Dynamic Bus Voltage Regulation and Phase Shifted PWM," APEC 07 Presentation
1019	List of APEC 2007 Exhibitors
1020	Declaration of Gordon MacPherson from IEEE re *Zane*
1021	U.S. Patent Application Publication No. US 2007/0257869A1 to Huang et al. ("Huang")
1022	*Stratosaudio v. Hyundai,* 22-CV-01712, GW-PD (C.D. Cal.), Tentative Ruling on Motion to Stay, April 26, 2022
1023	*Stratosaudio v. Hyundai,* 22-CV-01712, GW-PD (C.D. Cal.), Order Adopting Tentative Ruling, April 28, 2022
1024	*Vivint, Inc. v. Skybell Technologies, Inc.*, 21-CV-9472, GW-GJS, Order Granting Motion to Stay, November 10, 2022
1025	*Blackberry Limited v. Facebook, Inc.*, 18-CV-1844, GW-KS, Order on Motion to Stay, Feb. 13, 2020
1026	Linear Technology, *LTC3783 Specification Sheet*, 2005
1027	U.S. Patent No. 6,621,235 to Chang ("Chang")
1028	Katherine K. Vidal, "Updated Guidance on the Treatment of Statements of the Applicant in the Challenged Patent in Inter Partes Reviews Under § 311" (Memorandum to

Exhibit No.	Description
	Members of the Patent Trial and Appeal Board dated June 9, 2022)

CLAIM LISTING

Preamble [1.pre]	A light emitting diode (LED) driver for driving LEDs connected to different parallel paths,
Limitation [1.a]	the driver comprising: a voltage source for connection to first ends of LEDs in a plurality of parallel paths;
Limitation [1.b]	a plurality of current set circuits, one current set circuit per parallel path, each current set circuit controlling a peak current through one or more LEDs connected in each parallel path; and
Limitation [1.c]	a pulse-width modulated (PWM) brightness control signal generator connected to the plurality of current set circuits, the brightness control signal generator being configured to generate staggered PWM brightness control signals to the plurality of current set circuits,
Limitation [1.d]	each current set circuit being configured to draw the peak current through its associated one or more LEDs at a duty cycle substantially corresponding to a duty cycle of a PWM brightness control signal applied to it, such that the plurality of current set circuits conduct current through their associated one or more LEDs at the same duty cycle but out of phase with each other.
Claim 2	The driver of claim 1 wherein the voltage source is a step up voltage regulator.
Claim 3	The driver of claim 1 wherein each current set circuit is a current regulator.
Preamble [4.pre]	The driver of claim 1 wherein each current set circuit is a current regulator comprising:
Limitation [4.a]	a current control transistor in series with one or more LEDs in an associated parallel path; and
Limitation [4.b]	a feedback circuit connected to detect a current through the parallel path and connected to the current control transistor to control a conductivity of the current control transistor to cause the current through the parallel path to match a reference level.
Preamble [5.pre]	The driver of claim 4 wherein each current set circuit further comprises

Limitation [5.a]	a PWM brightness control transistor connected between an output of the feedback circuit and a control terminal of the current control transistor,
Limitation [5.b]	the PWM brightness control transistor being connected to the PWM brightness control signal generator for receiving a staggered PWM brightness control signal to couple the output of the feedback circuit to the control terminal of the current control transistor at a duty cycle of the staggered PWM brightness control signal.
Preamble [6.pre]	The driver of claim 1 wherein each current set circuit comprises:
Limitation [6.a]	a current set resistor in series with one or more LEDs in an associated parallel path; and
Limitation [6.b]	a PWM brightness control transistor connected in series between the current set resistor and the one or more LEDs in an associated parallel path, the PWM brightness control transistor being connected to the PWM brightness control signal generator for receiving a staggered PWM brightness control signal.
Preamble [7.pre]	The driver of claim 1 wherein the PWM brightness control signal generator comprises:
Limitation [7.a]	a shift register storing bits corresponding to a PWM duty cycle of a brightness control signal, the shift register having bit positions;
Limitation [7.b]	a clock connected to the shift register for shifting the bits along the shift register; and
Limitation [7.c]	taps off the shift register coupled to different bit positions of the shift register, each tap providing a different staggered PWM brightness control signal connected to an associated current set circuit.
Claim 8	The driver of claim 7 wherein the shift register has a connection that connects an end bit position to a first bit position so that bits in the shift register are recirculated in the shift register.
Claim 9	The driver of claim 7 wherein the bits corresponding to a PWM duty cycle of a brightness control signal are serially and continuously loaded into a first bit position of the shift register, then shifted by the clock.

Claim 10	The driver of claim 7 wherein the clock shifts the bits at a rate equal to N times a frequency of the PWM brightness control signal, where N equals the number of bits representing a single PWM duty cycle.
Claim 11	The driver of claim 1 wherein the plurality of parallel paths comprises at least three paths.
Claim 12	The driver of claim 1 further comprising the LEDs connected to the driver.
Claim 13	The driver of claim 1 wherein the driver is formed as an integrated circuit.
Preamble [14.pre]	A method for driving light emitting diodes (LEDs) connected to different parallel paths, the method comprising:
Limitation [14.a]	supplying a voltage to first ends of LEDs in a plurality of parallel paths;
Limitation [14.b]	setting a peak current through one or more LEDs connected in each of the parallel paths, the peak current being set by a current set circuit for each parallel path;
Limitation [14.c]	generating staggered pulse width modulated (PWM) brightness control signals;
Limitation [14.d]	applying a different staggered PWM brightness control signals to each current set circuit; and
Limitation [14.e]	drawing the peak current through the one or more LEDs in each parallel path, set by its associated current set circuit, at a duty cycle corresponding to a duty cycle of an associated PWM brightness control signal, such that the parallel paths of LEDs conduct current at substantially the same duty cycle but out of phase with each other.
Claim 15	The method of claim 14 further comprising varying the duty cycle of the staggered PWM brightness control signals to change an average current through the parallel paths of LEDs to change a perceived brightness of the LEDs.
Preamble [16.pre]	The method of claim 14
Limitation [16.a]	wherein setting a peak current through one or more LEDs connected in each of the parallel paths comprises setting the peak current by controlling conductivity of a current control transistor in series with each parallel path, and
Limitation [16.b]	wherein applying a different staggered PWM brightness control signal to each current set circuit comprises: coupling

	each staggered PWM brightness control signal to a control terminal of an associated pass transistor, each pass transistor being connected between a control terminal of a respective current control transistor and a regulating control voltage, such that the current control transistor is turned on and off corresponding to a duty cycle of the associated pass transistor.
Claim 17	The method of claim 14 wherein applying a different staggered PWM brightness control signal to each current set circuit comprises applying each staggered PWM brightness control signals to an associated transistor connected in series with the one or more LEDs in an associated parallel path, such that the transistor is turned on and off corresponding to the duty cycle of the staggered PWM brightness control signal applied to it.
Preamble [18.pre]	The method of claim 14 wherein generating staggered PWM brightness control signals comprises:
Limitation [18.a]	storing bits corresponding to a PWM duty cycle of a brightness control signal in a shift register, the shift register having bit positions;
Limitation [18.b]	shifting the bits along the shift register under control of a clock; and
Limitation [18.c]	receiving bits tapped off the shift register at different bit positions of the shift register to generate a different staggered PWM brightness control signal from the bits at each of the different bit positions.
Claim 19	The method of claim 18 further comprising recirculating bits in the shift register by feeding a bit at an output bit position to an input bit position along the shift register.
Claim 20	The method of claim 18 further comprising serially and continuously loading bits corresponding to a PWM duty cycle of a brightness control signal into a first bit position the shift register, then shifting the bits by the clock.
Claim 21	The method of claim 18 wherein the clock shifts the bits at a rate equal to N times a frequency of the PWM brightness control signal, where N equals the number of bits representing single PWM duty cycle.
Claim 22	The method of claim 14 wherein the plurality of parallel paths comprises at least three paths.

VIZIO, Inc. ("Petitioner") requests *inter partes* review of Claims 1-22 of U.S. Patent 7,843,148 ("the '148 Patent").

I. INTRODUCTION

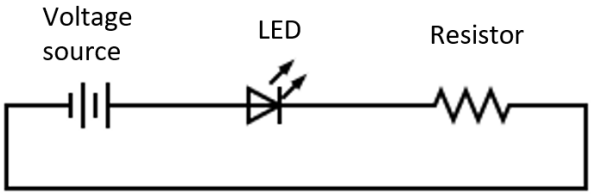
The '148 Patent is directed to an LED driver for driving LEDs that are connected in parallel. EX1001, Abstract. The '148 Patent explains that when there are multiple parallel sets of LEDs in the circuitry, the combined currents of the paths can be so high that the dimming control of the LEDs could cause large instantaneous changes in current through the circuit, causing voltage ripples and noise in the power supply that could affect other circuits connected to the power supply. *Id.* at 2:41-55. The '148 Patent accordingly describes an LED driver that produces less ripple and noise. *Id.* at 2:56-57. However, as demonstrated in this Petition, these LED drivers were described in prior art to the '148 Patent and were already well-known to a POSITA at the time of the alleged invention of the '148 Patent.

II. BACKGROUND

A. Light-Emitting Diodes (LEDs)

LEDs are semiconductor circuit elements that emit light when electric current passes through them. Compared to prior lighting technologies, LEDs provide advantages such as low power consumption, high energy efficiency, compact size, and the ability to emit light in specific spectra, that make them desirable for a wide range of lighting purposes. EX1003, ¶¶36-37. For example, LEDs are commonly

used to provide backlighting for displays, such as in TVs, computer monitors, and smartphones. *Id.* at ¶37. The following circuit diagram illustrates a simple example circuit for driving an LED, which consists of an LED in series with a voltage source and a resistor. *Id.* at ¶36.



The brightness of an LED is determined by the magnitude of the current flowing through the LED. *See, e.g.,* EX1001, 1:15-19; EX1003, ¶36. Thus, in the example circuit above, the brightness of the LED can be changed by varying the resistance, which in turn varies the current via the equation $I=(V-V_{LED})/R$, where V is the voltage provided by the voltage source, V_{LED} is the voltage drop across the LED, and R is the resistance of the resistor. EX1003, ¶36.

LED brightness is typically controlled using pulse-width modulation (PWM). EX1003, ¶38. PWM control of an LED allows one to change the *average* current flowing through the LEDs by using a fixed current through the LEDs, but turning the LEDs on and off very rapidly at frequencies that would be imperceptible to human vision. *See id.*; EX1001, 2:9-18. For example, the LED may be turned "on" and "off" very rapidly, such that it is "on" 60% of the time. The average current flowing through the LED is 60% of the fixed current, and the human eye would

perceive the LED to be at about 60% of peak brightness. EX1003, ¶38. The "duty cycle" of an LED driver refers to the percentage of time that the PWM signal is "on" in a period. *See id.*; EX1001, 2:9-18; *see also* EX1014, 4.

B. <u>The '148 Patent</u>

LEDs are often driven in parallel, such as for display backlighting. *See* EX1001, 1:20-39. The '148 Patent recognizes a potential drawback: if all the LEDs are driven in parallel simultaneously with the same PWM signals, the combined currents through the LEDs when they are turned "on" can be high. *See id.* at 2:41-43. This means the power supply must supply a large current to drive the LEDs and switch between that large current and no current very rapidly. *Id.* at 2:43-47. Such instantaneous large current changes can cause a "voltage ripple" in the power supply, and can cause noise that affects other circuits. *Id.* at 2:47-55; EX1003, ¶41. The '148 Patent illustrates this problem with the admitted prior art in Figure 1, annotated below, which identifies the current *I* that must be supplied when all LEDs are turned on.

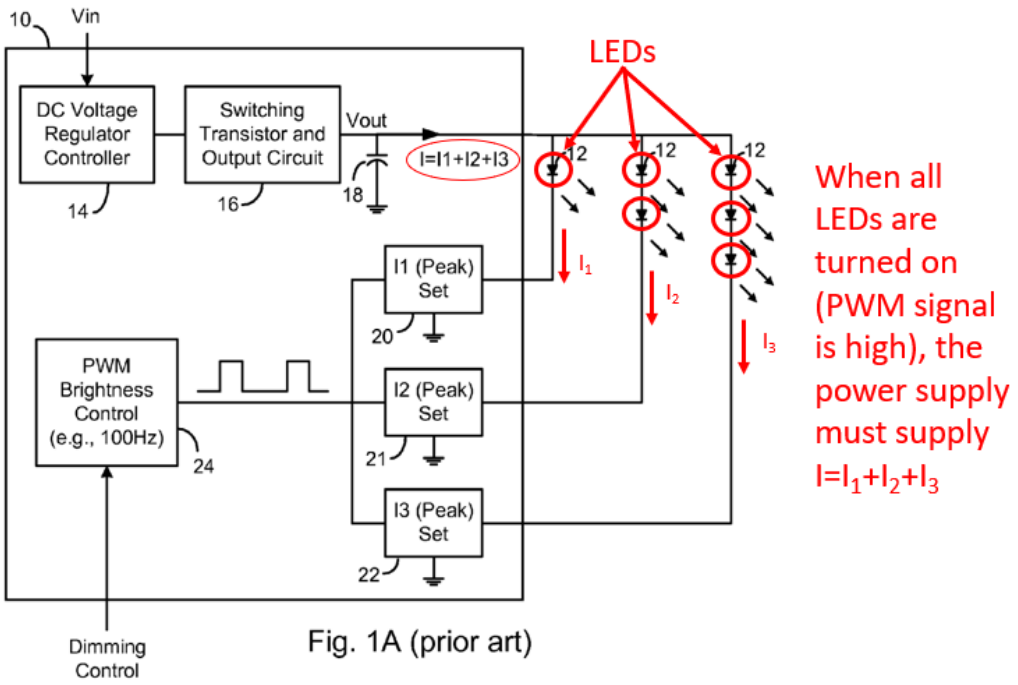


Fig. 1A (prior art)

EX1001, Fig. 1A (annotated); EX1003, ¶41.

The '148 Patent describes a solution: drive the LEDs in each parallel path with staggered PWM signals. *See* EX1001, 2:65-67. Thus, the LEDs would be driven with the same duty cycle, but the PWM signals are staggered such that not all the LEDs are turned "on" at the same time. EX1003, ¶42.

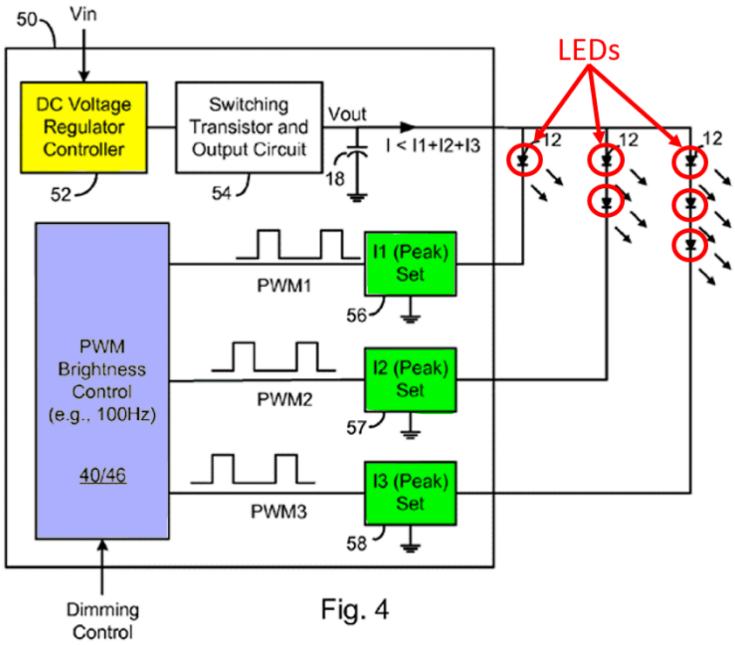


Fig. 4

EX1001, Fig. 4 (annotated); EX1003, ¶39.

Figure 2B, annotated below, illustrates an example with three staggered PWM signals. The three PWM signals have the same duty cycle, but are staggered in time, such that the PWM high states (labeled "ON" below) occur at different times relative to each other. EX1003, ¶¶40, 42.

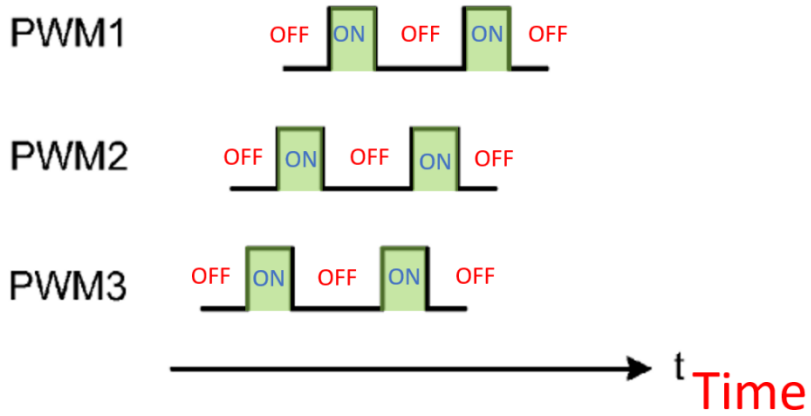
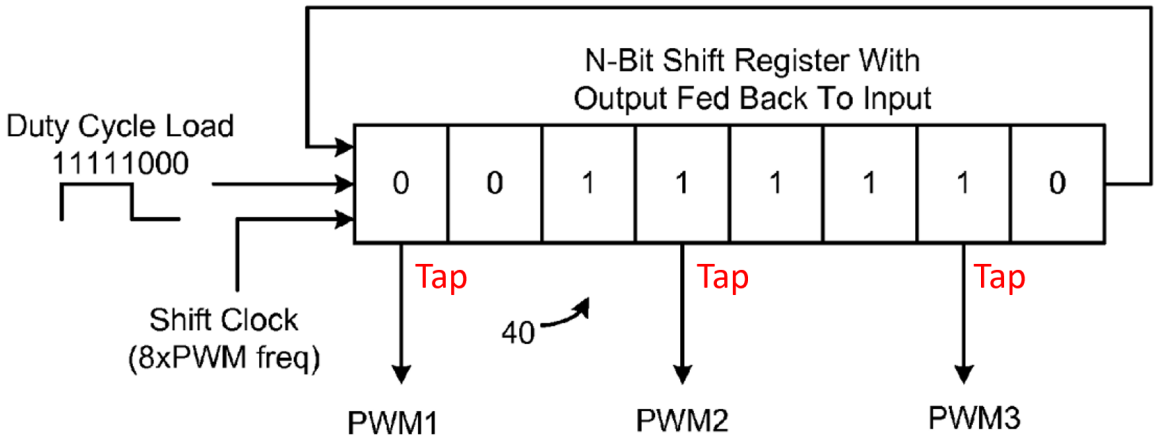


Fig. 2B

EX1001, Fig. 2B (annotated); *see also id.* at 4:55-62, 3:49-50. Moreover, in this example, the duty cycle is set low enough such that only one parallel path of LEDs would be turned on at a time while the other two paths would be turned off. *Id.* at 4:58-62. EX1003, ¶42. However, the '148 Patent also explains that "[i]f the driver drives many parallel paths, some paths may be driven in phase and other paths driven out of phase." EX1001, 4:63-64. In other words, the "ON" states of some staggered PWM signals may overlap, but in some circumstances such as Figure 2B, it is also possible that none of the "ON" states overlap. EX1003, ¶42.

The '148 Patent describing using a shift register to generate staggered PWM signals. *See* EX1001, 3:45-51, 4:3-64, Figs. 2A-2B; EX1003, ¶40. A shift register is a circuit that contains an array of flip-flops for holding a pattern of bits (0's and 1's) and connected such that when they are driven by a clock, the pattern of bits is shifted over by one bit location. EX1003, ¶40; *see also* EX1008, 525; EX1011, 114; EX1010, 1:12-35. A PWM signal is generated by converting the output of the shift register into a signal with high- and low-states corresponding to the 1's and 0's. *Id.*; EX1001, 4:13-30. Figure 2A (annotated below) shows an 8-bit pattern 11111000, which corresponds to a duty cycle of 62.5% where 5/8 (62.5%) of the bits are high (1). EX1001, 4:23-41; EX1003, ¶40.



EX1001, Fig. 2A (annotated).

The '148 Patent explains that the PWM brightness control signals for each parallel path of LEDs are tapped from different locations along the shift register. EX1001, 4:42-54; EX1003, ¶40. Figure 2A (above) shows three taps at different bit locations in the shift register that create three output signals. *Id.* Figure 2B illustrates the "staggering of the PWM brightness control signals." EX1001, 3:49-50, Fig. 2B, *see also id.* at 4:55-61; EX1003, ¶40. The '148 Patent describes these PWM signals that are staggered in time as "out of phase with each other." EX1001, 4:55-61.

However, the '148 Patent's solution of using staggered PWM signals to drive parallel LEDs was already well known and had been described in numerous patents and other references, including references from Petitioner's expert, Dr. Regan Zane. Even the specific way in which the '148 Patent generates the staggered PWM signals

by using a shift register with taps was previously disclosed in a patent filed 16 years before the '148 Patent. *See* EX1005.

C. Prosecution History

The '148 Patent issued from nonprovisional application No. 12/099,729 ("the '729 Application"), filed on April 8, 2008 by the original assignee, Micrel Inc. ("Applicant"). EX1001, Cover. The USPTO did not issue any office actions rejecting any claims of the '729 Application. On August 5, 2010, the USPTO issued a Notice of Allowance indicating that Claims 1-22 were allowed, with an Examiner's amendment addressing a typo and claim renumbering. EX1002, 48, 52; EX1003, ¶43.

The Applicant never submitted an Information Disclosure Statement or otherwise identified prior art that it knew of to the USPTO during prosecution of the '729 Application. *See generally* EX1002. Shortly after filing the '729 Application, the Applicant also filed a patent application in the UK, No. 0903201.2, which published on October 14, 2009 as GB 2459009A. *See* EX1012. The published UK application included a search report conducted by the Intellectual Property Office identifying GB 2346004A, WO 2008/007106A1, and JP 2009032497A as prior art. *See* EX1012, 19. The Applicant subsequently abandoned the UK application, but never informed the USPTO of this prior art, which also describes using staggered

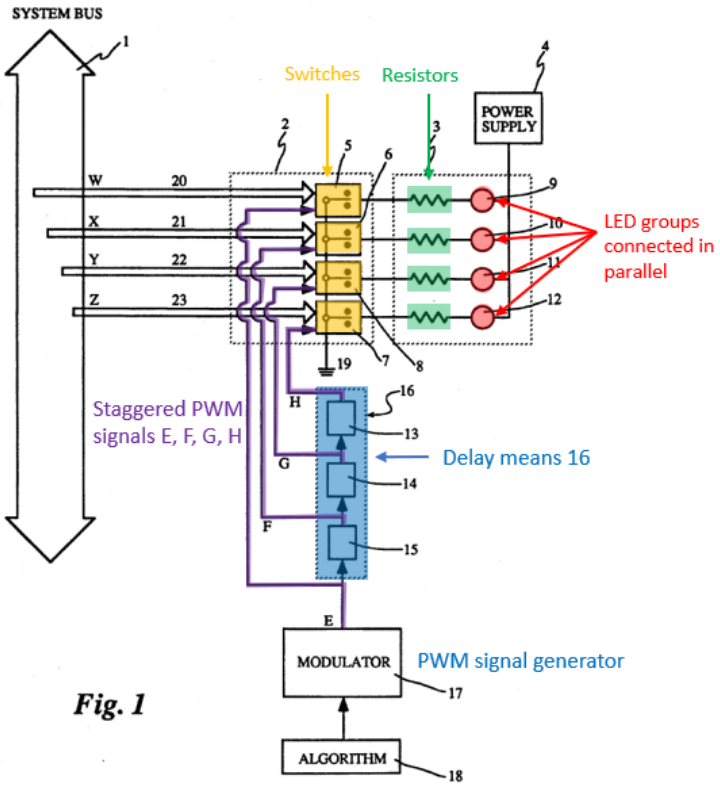
PWM signals to drive parallel LEDs. *See* EX1013 (listing status of UK application as "Terminated before grant").

D. The Prior Art

1. U.S. Patent No. 5,317,307 ("Thomas") (EX1005)

U.S. Patent. No. 5,317,307 is titled, "Method for Pulse Width Modulation of LEDs with Power Demand Load Leveling," and was issued on May 31, 1994. *See* EX1005, Cover. Thomas is prior art under pre-AIA § 102(b).[1] EX1003, ¶44. Thomas describes an LED driver with multiple LEDs connected in parallel to a power supply and driven with multiple, staggered PWM signals.

[1] Pre-AIA law applies because the application that became the '148 Patent was filed in 2008. Leahy-Smith America Invents Act, Pub. L. No. 112-29, 125 Stat. 284 (2011).



EX1005, Fig. 1 (annotated); EX1003, ¶44.

Modulator 17 generates a PWM signal *E* which is sent to both the activation switch for one LED and to a delay means 16, which generates three additional PWM signals *F*, *G*, and *H*, which are time-delayed versions of the PWM signal *E*. *See* EX1005, 3:46-4:16; EX1003, ¶44. In Thomas' preferred embodiment, the delay means 16 is implemented as a 12-bit shift register which sequentially stores bits corresponding to the PWM signal *E*. EX1005, 3:68-4:5, 4:17-23. Time-delayed PWM signals *F*, *G*, and *H* are generated by tapping the shift register at three cells within the shift register, as shown in FIG. 2. An example of the digital pulses of the signals is shown in FIG. 3. EX1005, 4:23-28, Fig. 2; EX1003, ¶¶44-45.

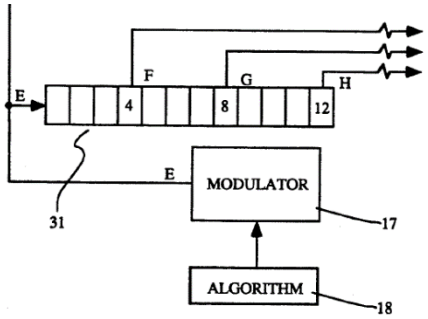


Fig. 2

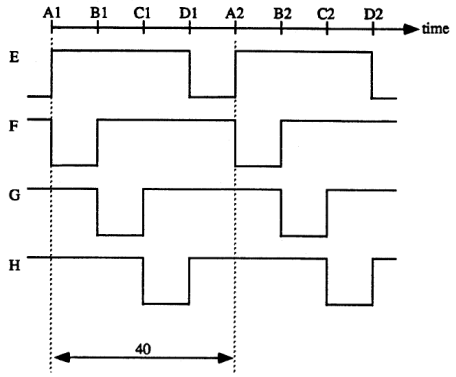


Fig. 3

EX1005, Figs. 2 (cropped), Fig. 3 (PWM signals *E*, *F*, *G*, *H*).

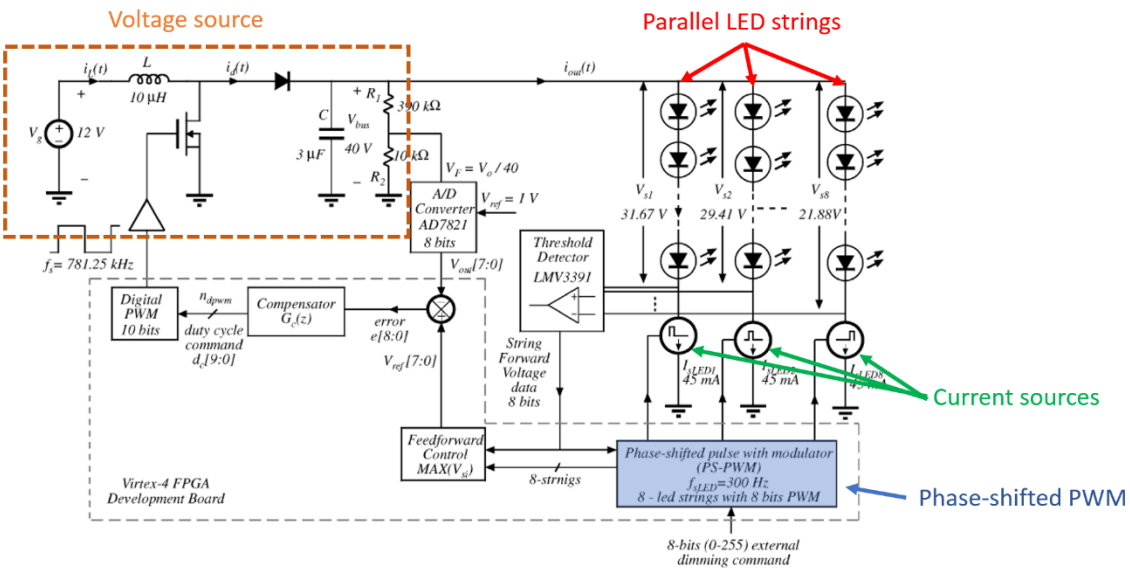
2. <u>Digital Architecture for Driving Large LED Arrays with Dynamic Bus Voltage Regulation and Phase Shifted PWM ("Zane") (EX1006)</u>

Zane is a paper presented by Dr. Regan Zane and his student, Montu Doshi, at the 22nd Annual IEEE Applied Power Electronics Conference and Exposition ("APEC 07").[2] EX1006; EX1003, ¶46. APEC 07 was held between February 25, 2007 to March 1, 2007 in Anaheim, California. EX1003, ¶46. APEC is an annual IEEE conference attended by power electronics professionals, which includes engineers who design LED drivers, power supplies, DC-DC converters, electrical motors, and other power electronic circuits. *Id.* Major industry players attended APEC 2007. *Id.*; *see also* EX1019. Dr. Zane and his student submitted a digest summarizing the paper to APEC 07 in August 2006 and the paper itself in December

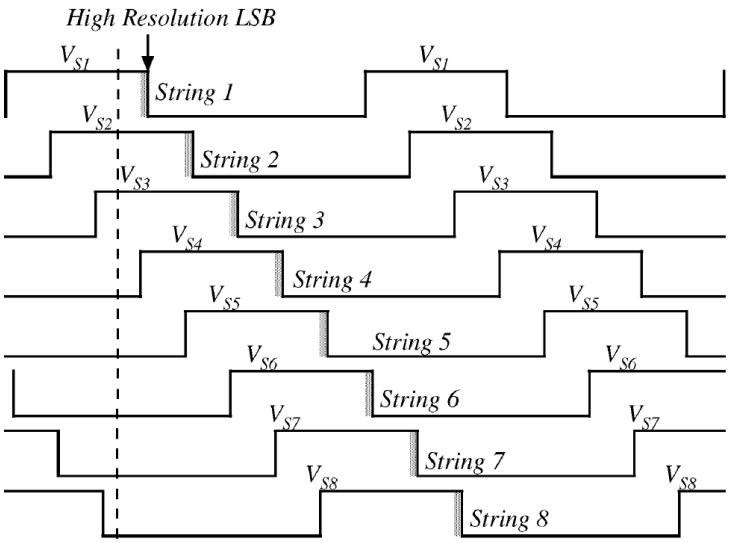
[2] Petitioner uses "*Zane*" in *italics* to refer to the conference paper and "Dr. Zane" to refer to Petitioner's expert witness.

2006, and presented the *Zane* conference paper during the conference during a presentation attended by around a few dozen conference attendees. EX1003, ¶47; *see also* EX1016; EX1017; EX1018. Electronic copies of *Zane* were available to over 2,500 registered attendees on the first date of the conference. EX1003, ¶¶46-47; *see also* EX1020 (IEEE custodian of records also testifying that the *Zane* paper was available no later than March 1, 2007). Thus, *Zane* is a pre-AIA § 102(b) prior art printed publication based on its dissemination and public accessibility to the public interested in the art at the APEC 07 conference. EX1003, ¶48; *see In re Klopfenstein*, 380 F.3d 1345, 1350-52 (Fed. Cir. 2004) (paper displayed at conference for several days was publicly accessible and therefore a prior art printed publication). *Zane* is also prior art under pre-AIA § 102(a) because it was described in a printed publication before the invention of the '148 Patent. EX1003, ¶48.

Zane discloses an LED driver circuit for driving parallel LED "strings" (multiple series LEDs in a parallel path). *See* EX1006, 287; EX1003, ¶49. *Zane* uses a digital phase shifted pulse width modulator (PS-PWM) to control the switching sequence and duty cycle for the parallel LED strings such that the LED strings are driven by PWM signals that are out of phase with each other. *Id.*; EX1006, 287-289.



EX1006, Fig. 3 (annotated); EX1003, ¶49. Figure 2A, below, shows an example of the phase shifted PWM signals for eight strings of LEDs at a 40% dimming command. EX1006, Fig. 2A. As shown below, only three out of the eight LED strings are on at a given time. *Id.*; EX1003, ¶49.



EX1006, Fig. 2A (showing phase-shifted PWM signals).

3. U.S. Patent No. 6,402,354 ("Tatewaki") (EX1007)

Tatewaki is titled "Indirect Lighting System for Vehicle Interior," and issued on June 11, 2002. *See* EX1007, Cover. Tatewaki is prior art under pre-AIA § 102(b). EX1003, ¶50. Tatewaki describes an LED roof lamp for use inside a vehicle cabin. EX1007, Abstract, 11:52-13:47. The LED in the roof lamp is driven with a PWM control circuit. *See id.* at 12:11-31. Further, the PWM control circuit contains a ring counter (which a POSITA would understand as a recirculating shift register) which controls the brightness of the LED. *See id.* at 13:26-47; EX1003, ¶¶50, 139.

4. Applicant-Admitted Prior Art ("AAPA") (EX1001)

The '148 Patent describes Figures 1A and 1B as a "prior art LED driver, driving LEDs connected in different parallel paths" and a "prior art PWM brightness control signal generator." EX1001, 3:41-44; *see also id.* at 1:40-55 (describing Figures 1A and 1B), Figs. 1A-1B; EX1003, ¶51. Thus, Figures 1A and 1B and the related description in the '148 Patent constitute applicant-admitted prior art.

AAPA may be used in IPRs to establish "what a skilled artisan would have known at the time of invention," "furnish[] a motivation to combine," or "supply[] a missing claim limitation." *Qualcomm Inc. v. Apple Inc.*, 24 F.4th 1367, 1375-76 (Fed. Cir. 2022); *see also* Katherine K. Vidal, "Updated Guidance on the Treatment of Statements of the Applicant in the Challenged Patent in Inter Partes Reviews

Under § 311" (Memorandum to Members of the Patent Trial and Appeal Board dated June 9, 2022) (EX1028).

5. Paul Horowitz & Winfield Hill, *The Art of Electronics* (2nd ed. 1989) (EX1008)

The Art of Electronics is a textbook on electronic circuit design published in 1989. EX1008 is a scanned excerpt of a copy of this textbook from the University of Wisconsin-Madison Library, which was available to library patrons at least as early as September 27, 1989. *See* EX1009; EX1003, ¶52. *The Art of Electronics* is therefore a publicly available printed publication and is prior art under pre-AIA § 102(b). *Id.*

6. Noel Morris, Digital Electronic Circuits and Systems (1974) (EX1011)

Digital Electronic Circuits and Systems is a textbook on electronic circuit design published in 1974. EX1011 is a scanned excerpt of a copy of this textbook from the Idaho State University Library. The library check-out slip inside this copy shows that it was checked out by library patrons as early as January 1977. *See* EX1011, 2; EX1003, ¶53. EX1011 is therefore a publicly available printed publication and prior art under pre-AIA § 102(b). *Id.*

III. LEVEL OF ORDINARY SKILL

The '148 Patent relates to electric circuits for driving LEDs connected in parallel using pulse-width modulated signals. *See, e.g.,* EX1001, Abstract. The patent describes generating staggered PWM signals using a shift register and also

describes two basic types of circuits that can regulate or limit the current flowing through the LEDs. *See id.* at Figs. 2A-6. A POSITA at the time of the invention of the '148 Patent would have had at least a bachelor's degree in physics, electrical engineering, or a related field, and approximately two years of experience in the fields of LED technology, backlights, LED devices and control thereof, or other related fields. EX1003, ¶¶34-35. Alternatively, advanced education in the fields of physics, electrical engineering, or a related field can compensate for lesser work experience in the relevant fields. *Id.*

This Petition does not turn on this specific definition of the level of ordinary skill. The claims are anticipated and/or would have been obvious from the perspective of any reasonable definition of a POSITA.

IV. CLAIM CONSTRUCTION

Petitioner submits that no claim terms need to be expressly construed to resolve the invalidity issues in this Petition. EX1003, ¶¶29-30. Petitioner reserves the right to respond to any claim construction disputes that may be raised by Patent Owner and to present § 112 defenses in this or any other proceeding.

V. RELIEF REQUESTED

Petitioner requests that the Board cancel Claims 1-22 of the '148 Patent as anticipated and/or obvious based on the following grounds of unpatentability:

Ground	Reference(s)	Basis	Challenged Claims
1	Thomas	Anticipation	1, 3, 7, 9, 10-12, 14, 17, 18, 20-22
2A	Thomas	Obviousness	1, 3, 6, 7, 9-12, 14, 17, 18, 20-22
2B	Thomas in view of the Applicant admitted prior art ("AAPA") and/or the knowledge of the POSITA	Obviousness	2, 13, 15
2C	Thomas in view of Tatewaki and the knowledge of a POSITA	Obviousness	8, 19
3	*Zane*	Anticipation	1-4, 11, 12, 14, 17, 22
4	*Zane*	Obviousness	1-4, 5, 11-17, 22

The Petition is supported by the expert declaration of Dr. Regan Zane (EX1003).

VI. GROUND 1 – ANTICIPATION BY THOMAS

A. Claim 1

As discussed below, Thomas anticipates Claim 1.

1. Preamble [1.pre] – "A light emitting diode (LED) driver for driving LEDs connected to different parallel paths,"

Thomas discloses an LED driving circuit for driving LEDs connected to different parallel paths. *See* EX1005, Abstract ("The present invention discloses a method and an apparatus for power demand load leveling of a power supply driving

a plurality of LED's through the use of pulse width modulation."); 2:18-21 (same); 3:12-15 ; Figs. 1-2; EX1003, ¶54.

As shown in Figure 1, groups of LEDs (9-12) are connected in four parallel paths. EX1003, ¶55; *see also* EX1005, Fig. 1.

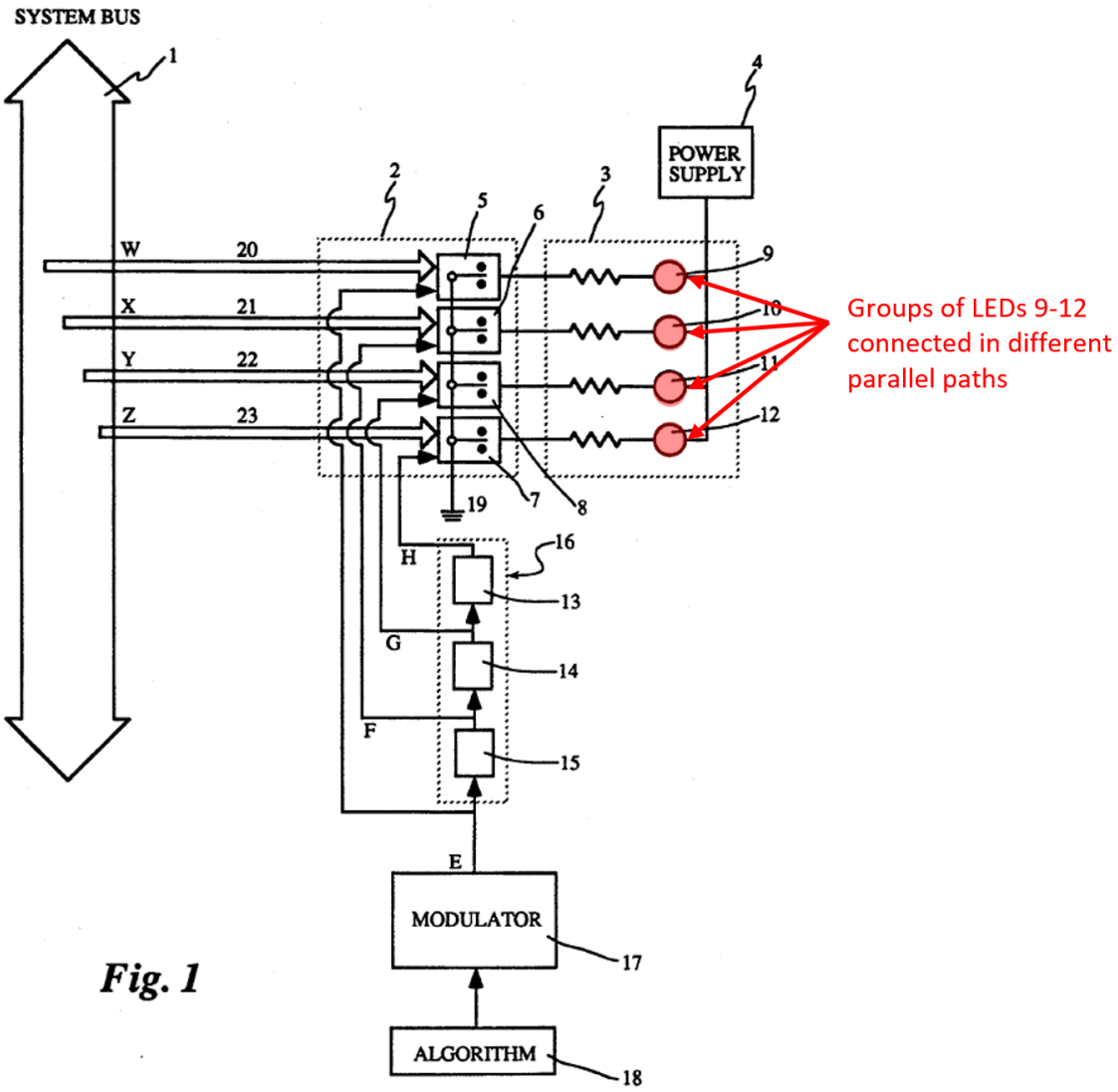


Fig. 1

EX1005, Fig. 1 (annotated); EX1003, ¶55.

Each of the four parallel paths shown in Figure 1 further comprises four parallel sub-paths. *Id.* at ¶56. Figure 2 explains that the parallel path for the LED group 9 in Figure 1 comprises four parallel sub-paths, with one LED and one resistor shown per path. *See* EX1005, Fig. 2 (annotated below); 3:3-5 ("FIG. 2 is a partial circuit diagram of the present invention showing one group of four LED's with their respective control lines and control devices."); 3:42-45 (explaining that "group of LED's (9)" consists of "LED's (34-37)"); *see also* 3:24-45 (further explaining the relationship between the circuits shown in Figures 1 and 2); 5:11-13 (explaining that each group of LEDs 9-12 comprises 25% of the total LEDs); EX1003, ¶56.

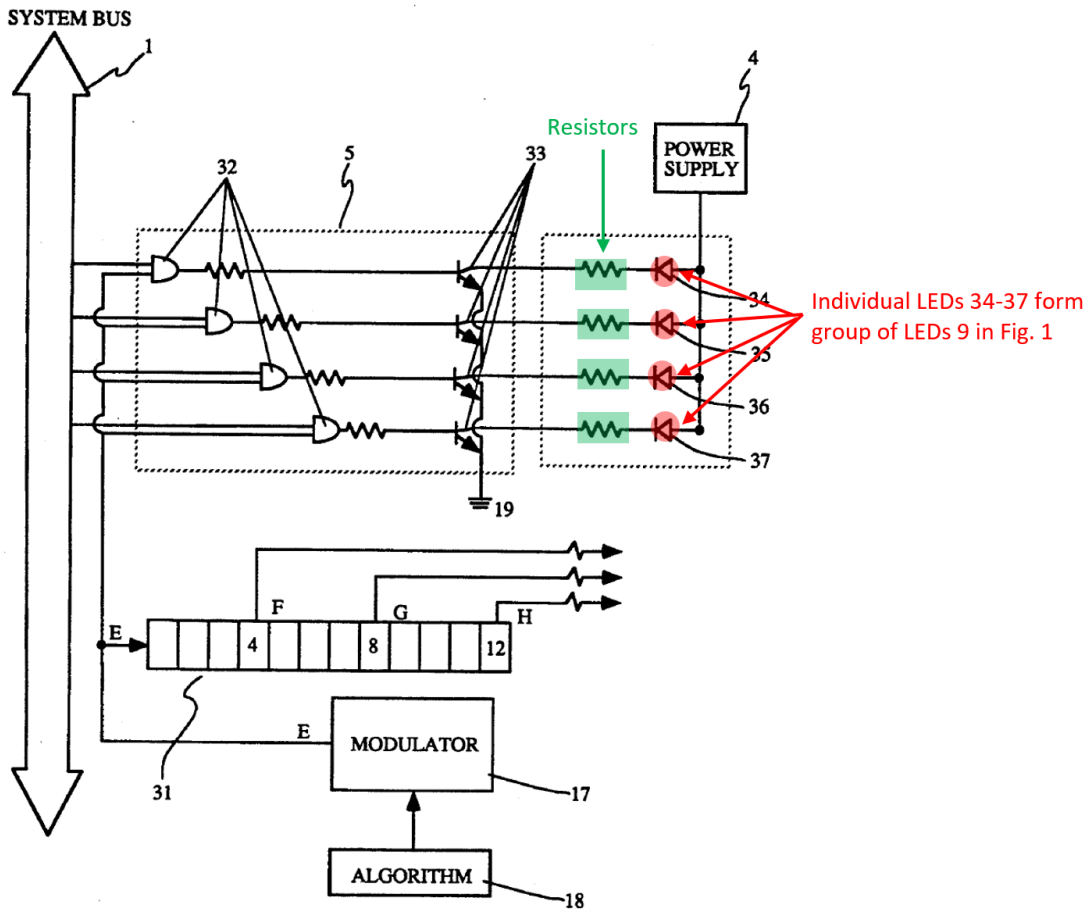
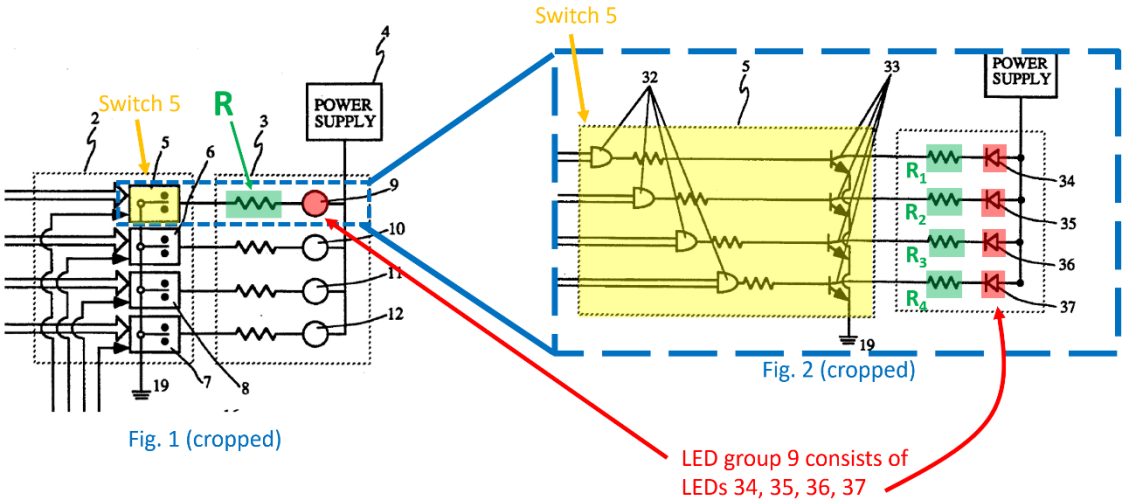


Fig. 2

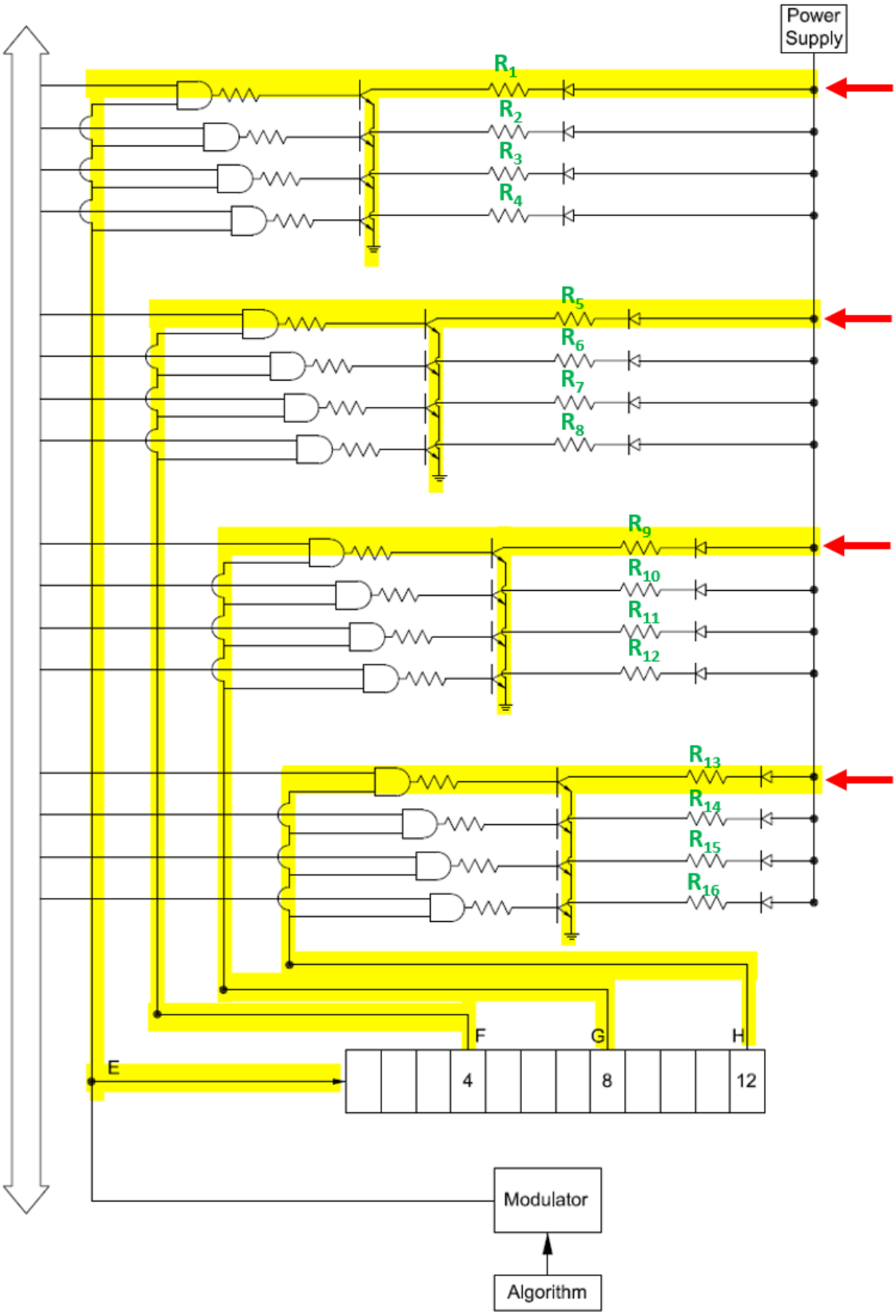
EX1005, Fig. 2 (annotated).

The following illustration further shows the relationship between the resistor (labeled R below) and LED group 9 shown in Figure 1, and the four resistors (annotated as R_1, R_2, R_3, and R_4) and individual LEDs (34-37) in Figure 2. For clarity, the switch 5 in both Figures 1 and 2 has also been highlighted yellow.



EX1005, Figs. 1-2 (cropped, annotated); EX1003, ¶57. In other words, Thomas discloses an LED driver with 4×4=16 parallel sub-paths. *Id.* at ¶¶57-58.

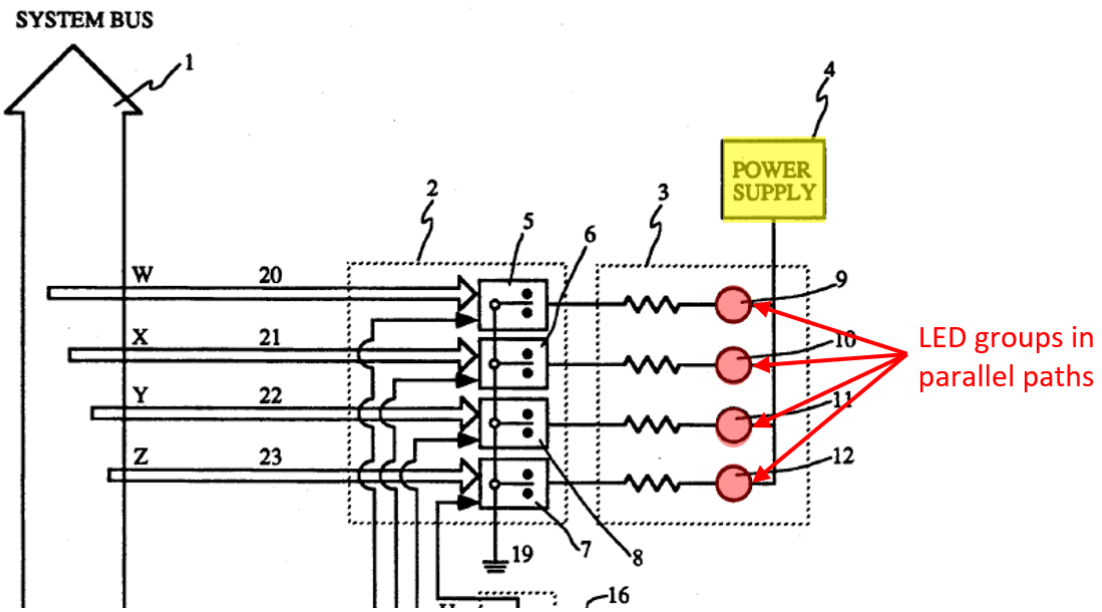
For purposes of Grounds 1 and 2, Petitioner focuses its anticipation and obviousness analyses on four of the 16 total parallel sub-paths. EX1003, ¶59. Specifically, the arguments in this Petition focus on a single sub-path per LED group shown in Figure 1. *Id.* To illustrate, the circuit diagram below expands on Thomas' Figure 2 to show all 16 parallel sub-paths. *Id.* at ¶58.


Power Supply
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
R15
R16
E
F
G
H
4
8
12
Modulator
Algorithm

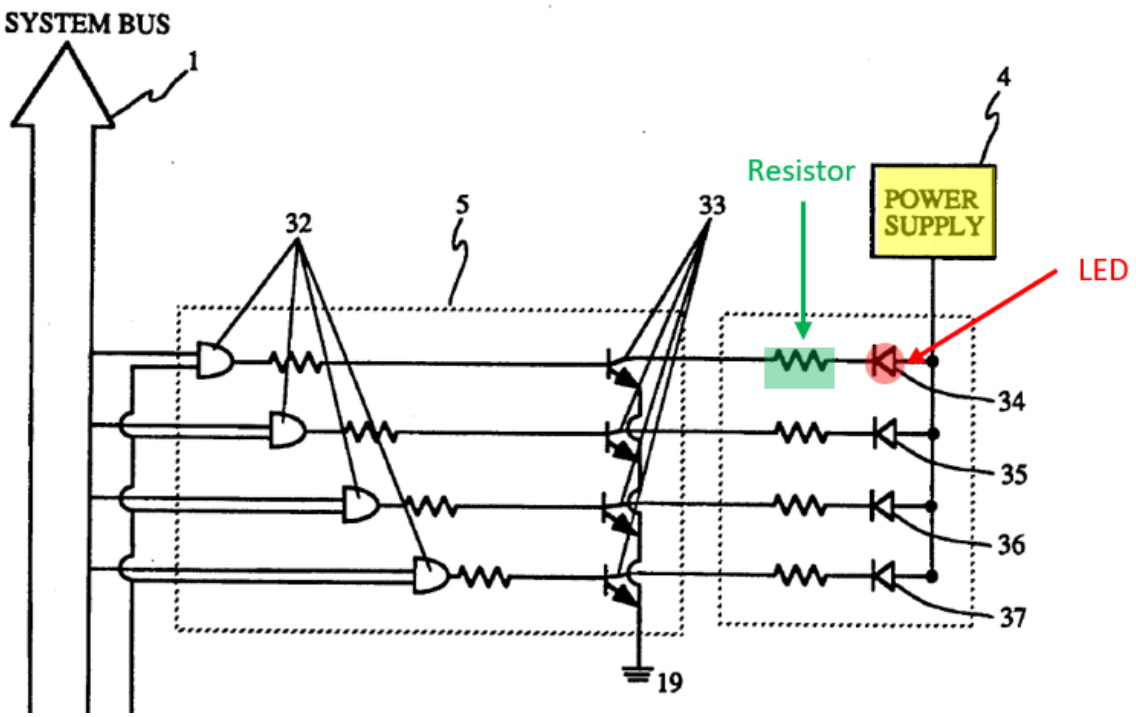
EX1003, ¶58. The 16 resistors in series with the LEDs in the 16 parallel sub-paths are labeled R_1-R_{16}. *Id.* at ¶59. The parallel sub-paths with resistors R_1-R_4 correspond to the LED group 9 in Figure 1 and are driven by the signal *E*. *Id.* Similarly, the sub-paths with resistors R_5-R_8, R_9-R_{12}, and R_{13}-R_{16} correspond to the LED groups 10, 11, and 12, respectively, and are driven by the signals *F*, *G*, and *H*, respectively. *Id.* The arguments in this Petition relating to the claimed "parallel paths" focus specifically on the parallel paths using the resistors R_1, R_5, R_9, and R_{13}. *See also id.* Petitioner is not suggesting any modification of Thomas' circuit to eliminate three out of four sub-paths per parallel path. Rather, Petitioner's arguments focus on a subset of four of the 16 total sub-paths that are discussed with respect to Thomas' Figures 1 and 2.

2. Limitation [1.a] – "the driver comprising: a voltage source for connection to first ends of LEDs in a plurality of parallel paths"

Thomas discloses a power supply (highlighted yellow below) which is connected to the first ends (anodes) of the LEDs in the four parallel paths shown in Figures 1 and 2. EX1005, Figs. 1-2, 3:12-15 (explaining power supply 4 drives the LEDs); 3:42-45 ("[T]he transistors (33) provide current from the power supply (4) for activating the associated LED's (34-37) in the group of LED's (9)."); EX1003, ¶60.



EX1005, Fig. 1 (cropped, annotated); EX1003, ¶60.

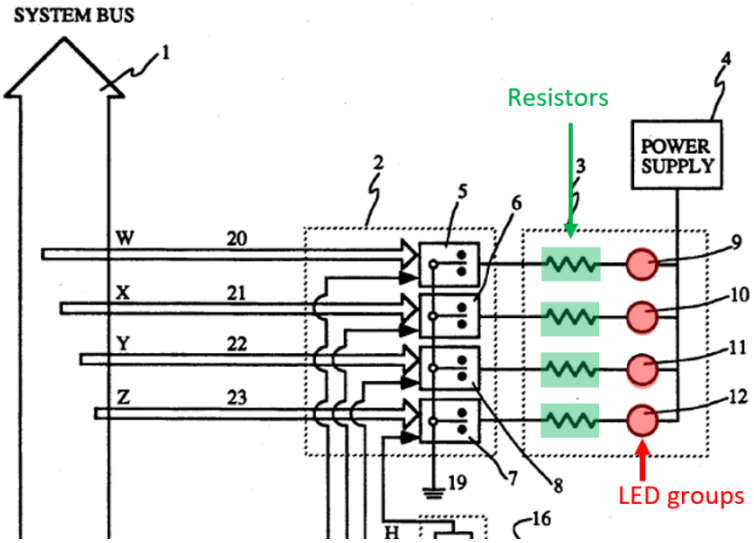


EX1005, Fig. 2 (cropped, annotated); EX1003, ¶60.

A POSITA would have understood, and Thomas confirms, that a power supply is a voltage source. EX1005, 1:66-2:10 (explaining that a goal of the invention is to "reduce[] the magnitude of the instantaneous change in the current demand on the power supply such that a more stable output ***voltage*** can be maintained.")[3]; EX1003, ¶61.

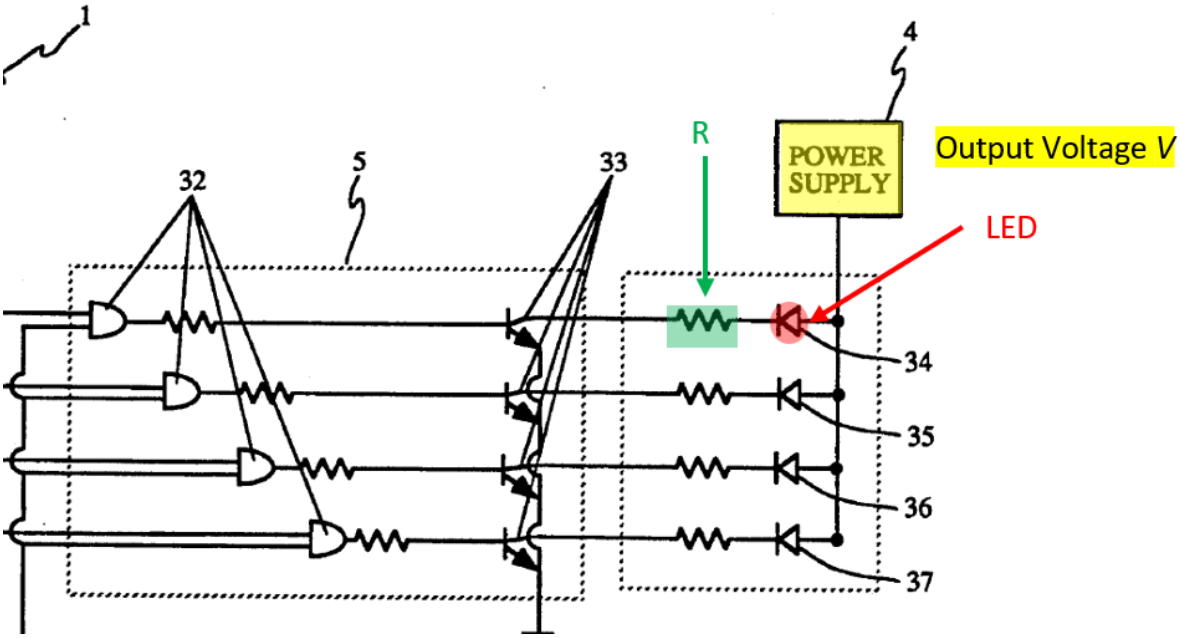
3. Limitation [1.b] – "a plurality of current set circuits, one current set circuit per parallel path, each current set circuit controlling a peak current through one or more LEDs connected in each parallel path; and"

As shown below, Thomas' Figures 1 and 2 show a resistor in series with the LED group in each parallel path. EX1003, ¶62.



EX1005, Fig. 1 (cropped, annotated); EX1003, ¶62.

[3] All ***emphases*** added unless stated otherwise.



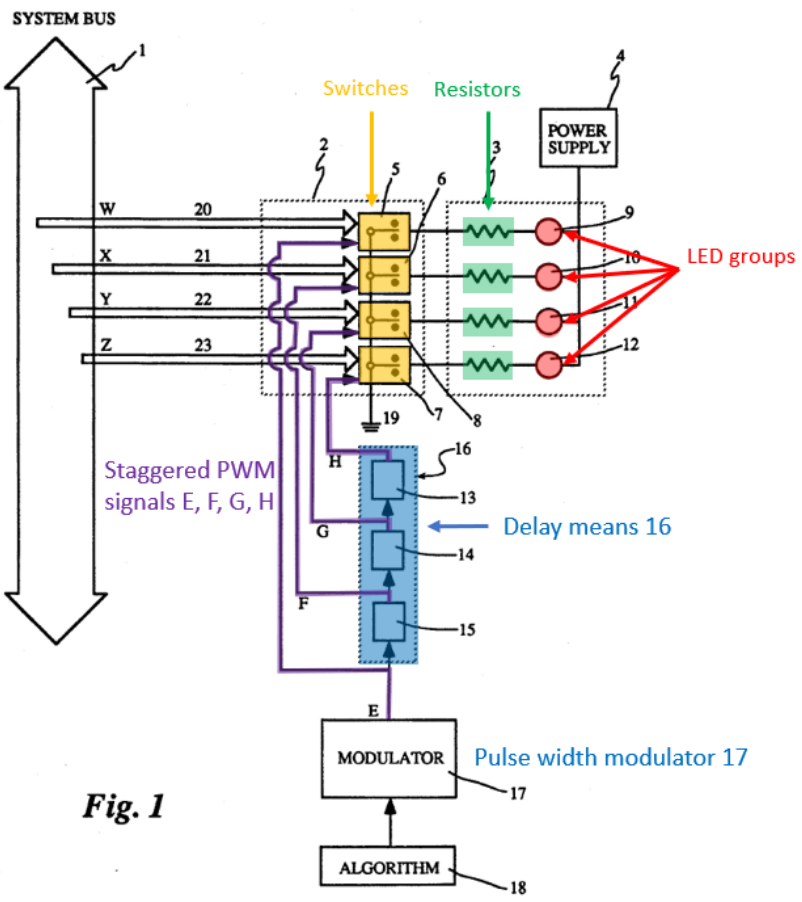
EX1005, Fig. 2 (cropped, annotated); EX1003, ¶62. A POSITA would have understood from Thomas' disclosure that the purpose of those resistors is to limit the current flowing through each of the parallel paths of LEDs to a peak current *I*, based on the resistance *R* of the resistor, the voltage *V* output by the power supply, the voltage drop across the LED, and the equation $I=(V-V_{LED})/R$.[4] EX1003, ¶63. Thus, the resistors shown in Thomas' Figure 1 (and more specifically, the individual resistors in each sub-path in Figure 2) are each a current set circuit, and there is one current set circuit per parallel path shown in Figure 1 which controls the peak current through the LED in each parallel path. *Id.*

[4] $I=(V-V_{LED})/R$ is the peak current that can flow through the LEDs in this circuit. In practice, the actual current will be slightly less than $(V-V_{LED})/R$ as due to the voltage drop on the transistor or other parasitic resistances in the circuit. EX1003, ¶63.

4. Limitation [1.c] – "a pulse-width modulated (PWM) brightness control signal generator connected to the plurality of current set circuits, the brightness control signal generator being configured to generate staggered PWM brightness control signals to the plurality of current set circuits,"

Thomas discloses a pulse width modulator 17 which "generat[es] a modulating signal having digital pulses." EX1005, 3:46-63; EX1003, ¶64. Pulse width modulation is used "[t]o control the intensity of the LED's" by rapidly activating the LEDs "so that the series of activations of the LED's produce an appearance that the LED's are being dimmed rather than being turned on and off." EX1005, 1:23-42. Furthermore, a delay means 16 receives the PWM signal *E* generated by modulator 17 and generates additional PWM signals *F, G,* and *H* which are the same waveform as the original PWM signal *E*, but staggered by different delays. *See id.* at 3:64-4:16, Figs. 1, 3; EX1003, ¶64. Additionally, the "precise wave form of the modulating signal" may be determined by an algorithm 18, which is "implemented in either software or hardware as is well-known in the art." EX1005, 3:47-51; EX1003, ¶64. The pulse width modulator 17, algorithm 18, and delay means 16 together disclose the "pulse-width modulated (PWM) brightness control signal generator" recited in Limitation [1.c]. *Id.* As shown in Figure 1, the pulse width modulator 17 and delay means 16 are connected to the plurality of current set circuits in Figure 1 (the resistors) via the activation switches 5-8

(highlighted yellow below) that are in each of the parallel circuit paths. EX1003, ¶64.



EX1005 , Fig. 1 (annotated); EX1003, ¶64.[5]

Thomas describes that the delay means 16 may be implemented in either of two ways: **(1)** using delay elements 13-15 or **(2)** using "a shift register (31) having taps," which is the "preferred embodiment of the present invention, as shown in FIG.

[5] Figure 1 is drawn with delay elements 13-15, but the specification states that delay means 16 may also be a shift register, as drawn in Figure 2. EX1005, 3:68-4:5; EX1003, ¶80 n.2.

2." EX1005, 3:68-4:18, Fig. 2; EX1003, ¶65. Both implementations anticipate Claim 1 because both implementations result in staggered PWM brightness control signals. EX1003, ¶65.

Thomas' Figure 3 illustrates that the PWM signals *E*, *F*, *G*, and *H* are staggered. EX1003, ¶66.

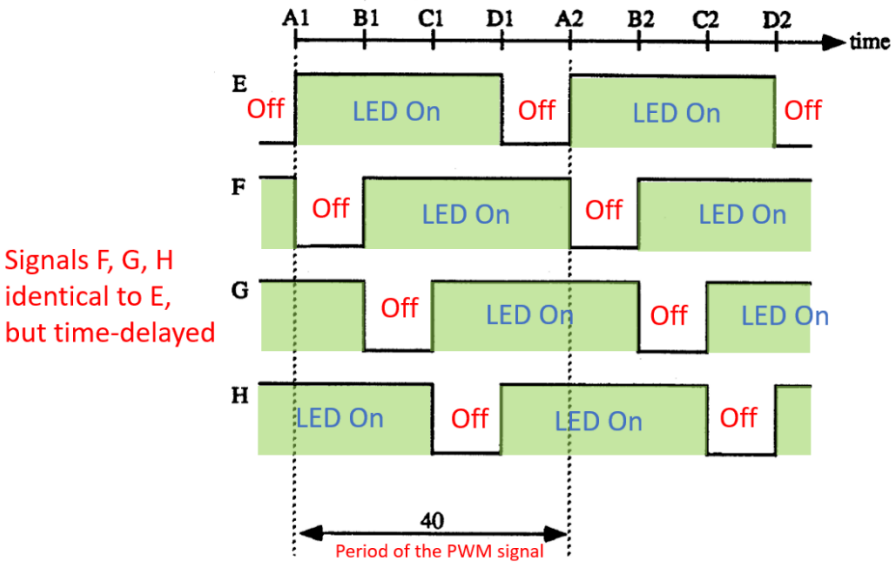
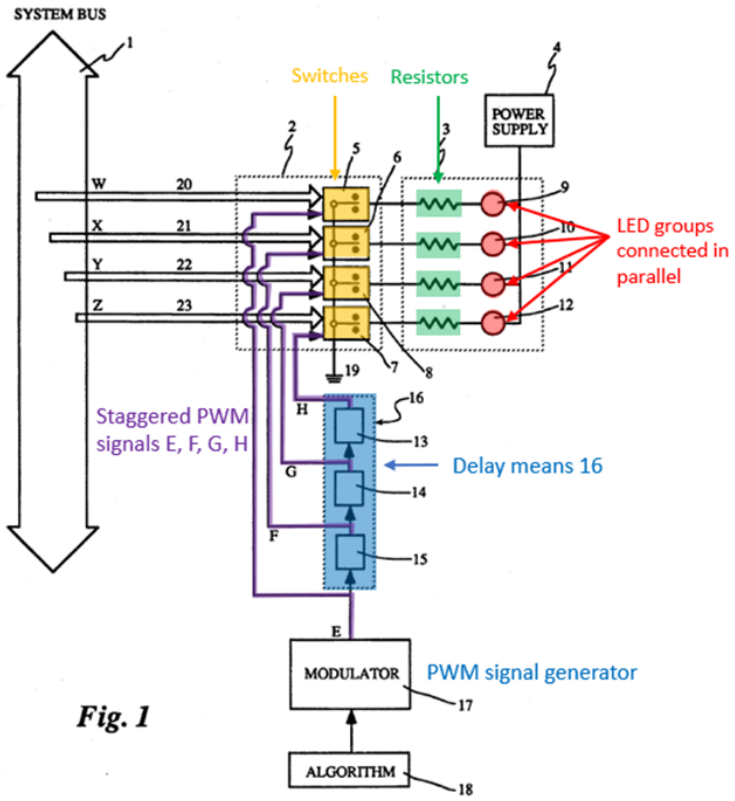


Fig. 3

EX1005, Fig. 3 (annotated); EX1003, ¶66. And as shown in Figure 1 above, different staggered PWM signals are applied to the plurality of current set circuits via the switches 5-8. EX1003, ¶66. Specifically, signals *E*, *F*, *G*, and *H* are applied to the current set circuits corresponding to LED groups 9, 10, 11, and 12, respectively. *Id.*; EX1005, Fig. 1.

5. Limitation [1.d] – "each current set circuit being configured to draw the peak current through its associated one or more LEDs at a duty cycle substantially corresponding to a duty cycle of a PWM brightness control signal applied to it, such that the plurality of current set circuits conduct current through their associated one or more LEDs at the same duty cycle but out of phase with each other."

As discussed for Limitation [1.b], the current set circuits in Thomas' Figure 1 are configured to draw a peak current through their associated LED. EX1003, ¶67. The current set circuits are further configured to draw that peak current at the duty cycle of the PWM brightness control signal applied to that current set circuit. *Id.* As annotated in Figure 1 below, the staggered PWM signals *E*, *F*, *G*, and *H* are fed into activation switches 5, 6, 8, and 7, respectively. *See* EX1005, Fig. 1, 4:66-5:10; EX1003, ¶68.



EX1005, Fig. 1 (annotated); EX1003, ¶68. The switches activate their respective parallel paths (allowing current to flow through the current set circuit) when the switches receive a high pulse from the PWM signal. *Id.* at ¶¶67-68, 70; *see also* EX1005, 3:24-63; 5:3-10.[6] Thus, the current set circuits in each parallel path draw their peak currents at a duty cycle that corresponds to the duty cycle of the PWM

[6] The switches also need a high control signal (W, X, Y, or Z) in combination with a high pulse from a PWM signal (E, F, G, or H) to turn on the LED. EX1005, 3:46-63, 4:66-5:10; EX1003, ¶¶68-69. The control signals (W, X, Y, Z) control whether the LEDs are "on" or "off" from the user's perspective, while the PWM signals (E, F, G, H) control the perceived brightness of the LEDs are when they are "on." EX1003,¶69.

brightness signal (*E*, *F*, *G*, or *H*) that are applied to them. EX1005, 3:28-63, 4:66-5:10; EX1003, ¶70.

As discussed with respect to Limitation [1.c] and shown in Figure 3, the PWM signals are identical but staggered. EX1003, ¶71; EX1005, Fig. 3. Thomas further explains, "[b]ecause the modulating signals (E, F, G, H) ***vary in phase with respect to each other***, each set of activation switches (5-8) is sequentially turned on by their respective modulating signals (E, F, G, H) so that no more than one group of LED's, comprising twenty five percent of the total LED's, is activated (or switched on) at any one time." EX1005, 5:13-20. Thus, the current set circuits in Thomas are configured to conduct current through their associated LEDs at the same duty cycle but out of phase with each other. EX1003, ¶71.

Accordingly, Thomas anticipates Claim 1. EX1003, ¶72.

B. <u>Claim 3 – "The driver of claim 1 wherein each current set circuit is a current regulator."</u>

Thomas anticipates Claim 1, as discussed above. As discussed for Limitation [1.b], Thomas discloses resistors in each parallel path which limit the current flowing through the LED to $(V\text{-}V_{LED})/R$. *See supra* Section VI.A.3; EX1003, ¶73. A resistor connected in series with the load (the LED) is a basic type of a current regulator because it limits the maximum current. *Id.* Thomas anticipates Claim 3.

C. Claim 7

1. Limitation [7.pre] – "The driver of claim 1 wherein the PWM brightness control signal generator comprises:"

Thomas anticipates Claim 1, as discussed above. EX1003, ¶74.

2. Limitation [7.a] – "a shift register storing bits corresponding to a PWM duty cycle of a brightness control signal, the shift register having bit positions;"

Thomas discloses that delay means 16 may be implemented as a shift register, as shown below. *See supra* Section VI.A.4.; EX1005, Fig. 2, 3:68-4:4:5, 4:17-32; EX1003, ¶75.

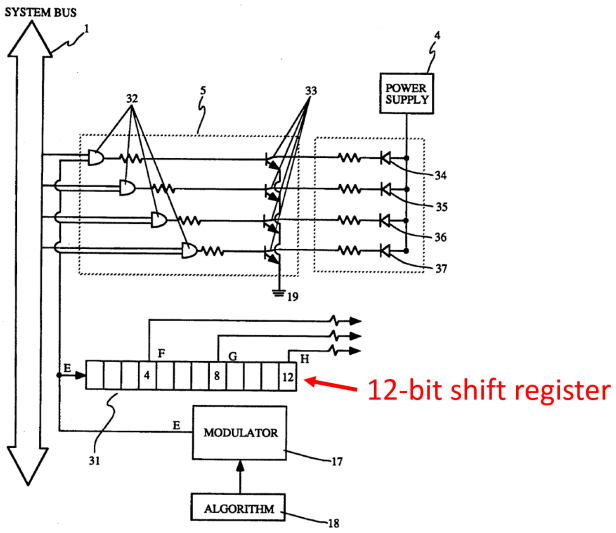


Fig. 2

EX1005, Fig. 2 (annotated); EX1003, ¶75. The shift register has 12 bit positions, shown above. *Id.* The shift register stores bits corresponding to the duty cycle of the PWM signal *E*. EX1003, ¶75; EX1005, 3:46-63, 4:17-23 ("[A] twelve bit shift register (31) is used to generate the delayed modulating signals (F, G, H) by

sequentially storing twelve binary values corresponding to the pulses or lack of pulses in the first modulating signal (E).").

3. Limitation [7.b] – "a clock connected to the shift register for shifting the bits along the shift register; and"

Thomas discloses a clock through its disclosure of a "time delay" for the staggered PWM signals. *See* EX1005, 4:33-39, *see also id.* at 3:64-4:5 (explaining that a shift register is used to generate delayed modulating signals), 4:17-32; EX1003, ¶76. Moreover, a shift register necessarily includes a clock connected to the shift register for shifting the bits along the shift register. *Id.* All shift registers ***must*** have a clock connected to them for shifting the bits.[7] *Id.*

Electronics textbooks confirm that all shift registers have a clock connected to them for shifting the bits. EX1003, ¶77. *The Art of Electronics* (2d ed.) explains:

> If you connect a series of flip-flops so that each *Q* output drives the next *D* input, and all clock inputs are driven simultaneously, you get what's called a "shift register." At each clock pulse the pattern of 0's and 1's in the register shifts to the right, with the data at the first *D* input entering from the left.

EX1008, 525.

[7] A "clock" in this context refers to a circuit that outputs pulses at predictable times, not an analog or digital clock used for telling time. EX1003, ¶76.

Without a clock, a shift register would not be able to shift the bits – it would not even be considered a shift register, but rather, just a "register." EX1003, ¶77; EX1011, 114 ("A register is simply an array of flip-flops used for the storage of binary data, and a shift register is one which is designed so that the data may be 'shifted' along the register in either direction, that is, either to the right or to the left."); *see also id.* 114-116. Thus, a clock is necessarily present within Thomas' LED driver circuit and connected to Thomas' shift register. EX1003, ¶78. Accordingly, Thomas discloses a clock that is connected to the shift register for shifting the bits along the shift register. *Id.*

4. Limitation [7.c] – "taps off the shift register coupled to different bit positions of the shift register, each tap providing a different staggered PWM brightness control signal connected to an associated current set circuit."

Thomas discloses taps off the shift register connected to different bit positions, each of the taps generating a different staggered PWM brightness control signal. *See* EX1005, 4:17-28 ("The second, third and fourth modulating signals (F, G, H) are then generated by tapping the values stored within the fourth, eighth and twelfth cells of the shift register (31) as the values are sequentially shifted through the twelve cells of the shift register (31)."), Fig. 2; EX1003, ¶79. Figure 2 shows the taps off the shift register which generate the signals F, G, and H.

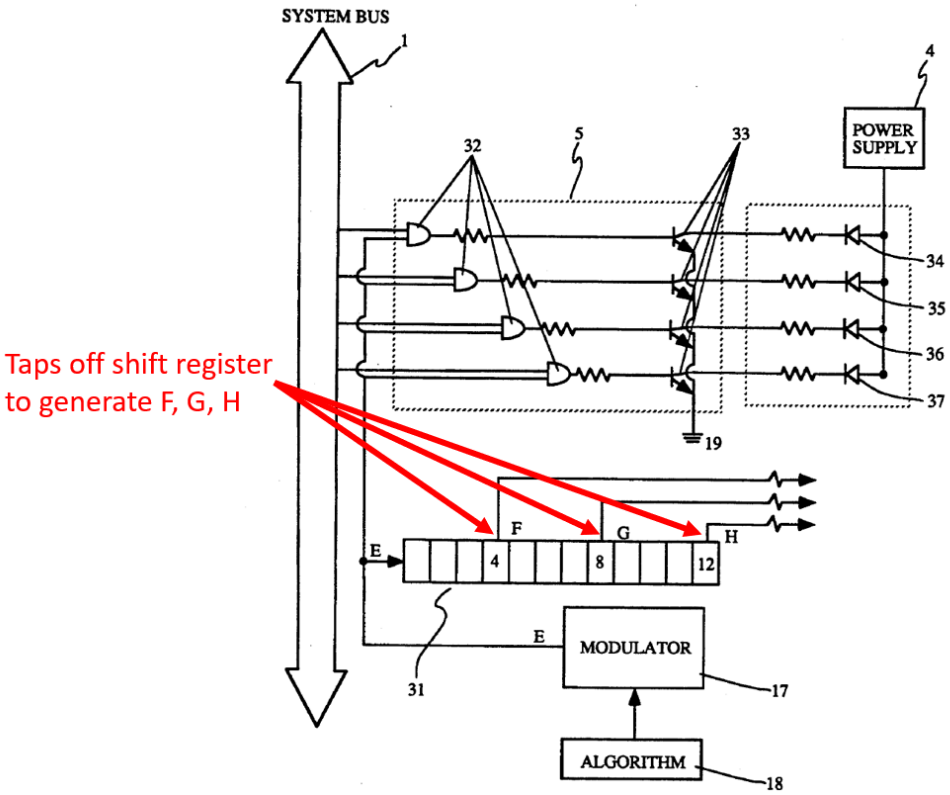
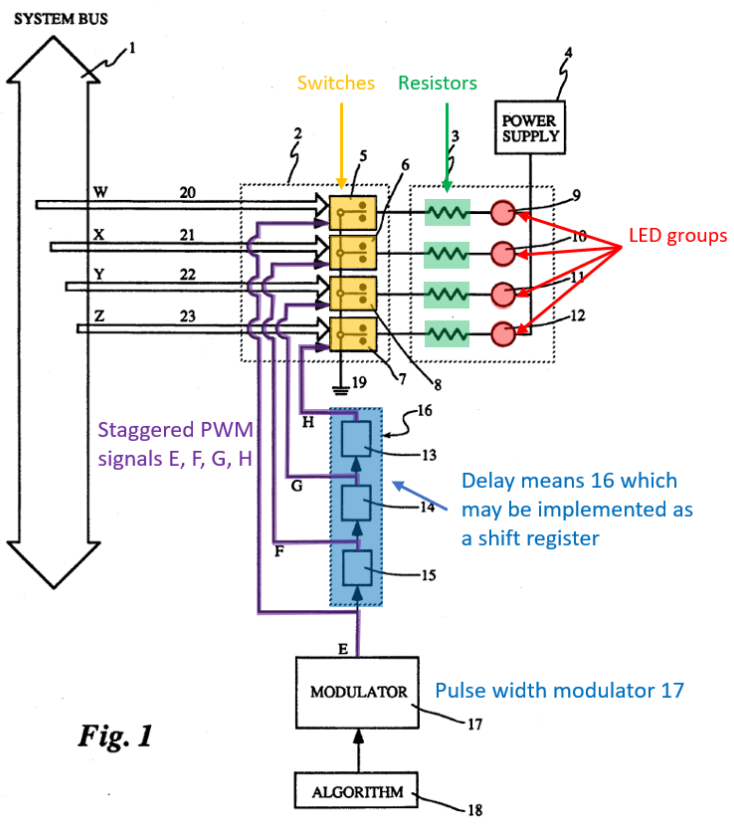


Fig. 2

EX1005, Fig. 2 (annotated); EX1003, ¶79.

As shown in Figure 1, the staggered PWM signals E, F, G, and H are connected to their associated current set circuits (the resistors). EX1003, ¶80.



EX1005, Fig. 1 (annotated); *see also id.* at Fig. 2; EX1003, ¶80. Accordingly, Thomas anticipates Claim 7.

D. <u>Claim 9 – "The driver of claim 7 wherein the bits corresponding to a PWM duty cycle of a brightness control signal are serially and continuously loaded into a first bit position of the shift register, then shifted by the clock."</u>

Thomas anticipates Claim 7, as discussed above. EX1003, ¶81. Thomas discloses the shift register "generate[s] the delayed modulating signals (F, G, H) by sequentially storing twelve binary values corresponding to the pulses or lack of pulses in the first modulating signal (E)." EX1005, 4:17-23. Figure 2 (below) shows the bits corresponding to the PWM signal *E* are loaded into the first bit position of

the shift register. EX1003, ¶81. The bits are then shifted along the shift register. *Id.*; EX1005, 4:23-28 ("[T]he values are sequentially shifted through the twelve cells of the shift register (31)."). As discussed above, all shift registers necessarily have a clock connected to them that causes the bits to shift. EX1003, ¶81.

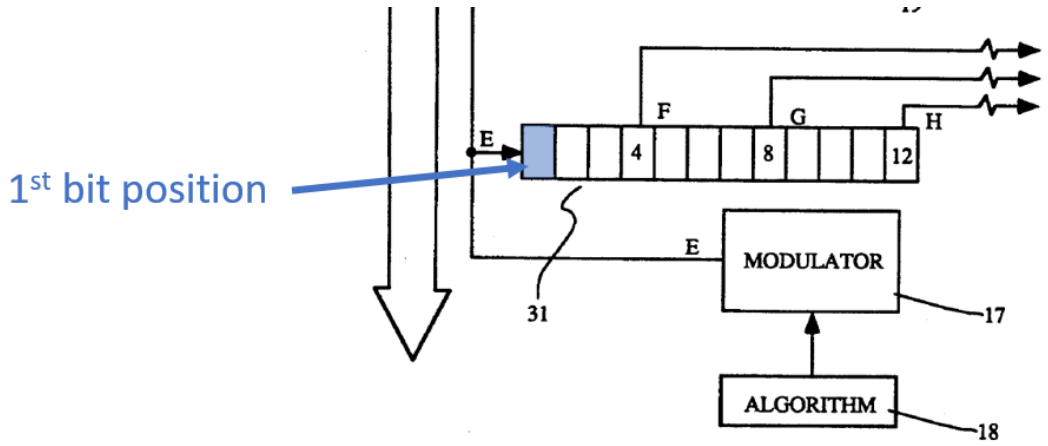


Fig. 2

EX1005, Fig. 2 (cropped, annotated); EX1003, ¶81.

Additionally, Figure 3 shows that the signal E, which is generated by the modulator 17, has a period 40 spanning from time A1 to A2 and that it repeats itself. EX1003, ¶82.

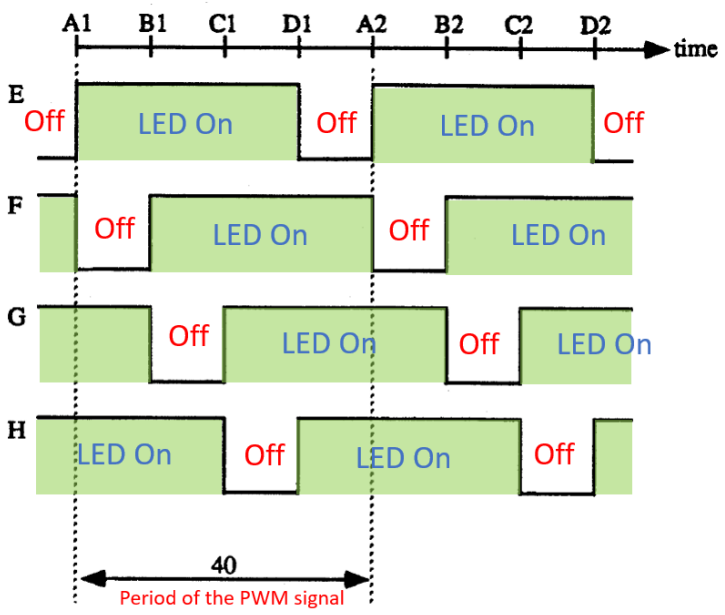


Fig. 3

EX1005. at Fig. 3 (annotated); EX1003, ¶82. Figure 3 also shows that the additional three signals *F*, *G*, and *H*, which are generated by the taps off the shift register, also repeat themselves. *Id.* Thus, the shift register is serially and continuously loading the bits corresponding to the PWM signal *E* into the shift register and generating the time-delayed signals *F*, *G*, and *H*. *Id.* Accordingly, Thomas anticipates Claim 9.

E. <u>Claim 10 – "The driver of claim 7 wherein the clock shifts the bits at a rate equal to N times a frequency of the PWM brightness control signal, where N equals the number of bits representing a single PWM duty cycle."</u>

Thomas anticipates Claim 7, as discussed above. EX1003, ¶83. Thomas inherently discloses Claim 10. *Id.* Thomas discloses a 12-bit shift register which "sequentially stor[es] twelve binary values corresponding to the pulses or lack of

pulses in the first modulating signal (E)." EX1005, 4:17-23, Fig. 2. Thus, the number of bits representing a single PWM duty cycle is N=12. EX1003, ¶83.

The frequency of a PWM signal, *f*, is defined as 1/*T*, where *T* is the period of the signal (units in seconds). EX1003, ¶84. The period *T* for the PWM signal is the time it takes for the PWM signal to complete one cycle, or in other words, to shift all 12 bits representing the PWM signal out of the shift register. *Id.* Thus, the clock must shift the bits in the shift register 12 times in the period *T*, or in other words, the clock shifts the bits every *T*/12 seconds. *Id.* Thus, the frequency of the clock is 1/(*T*/12)=12/*T*=12*f*=N*f*. *Id.*

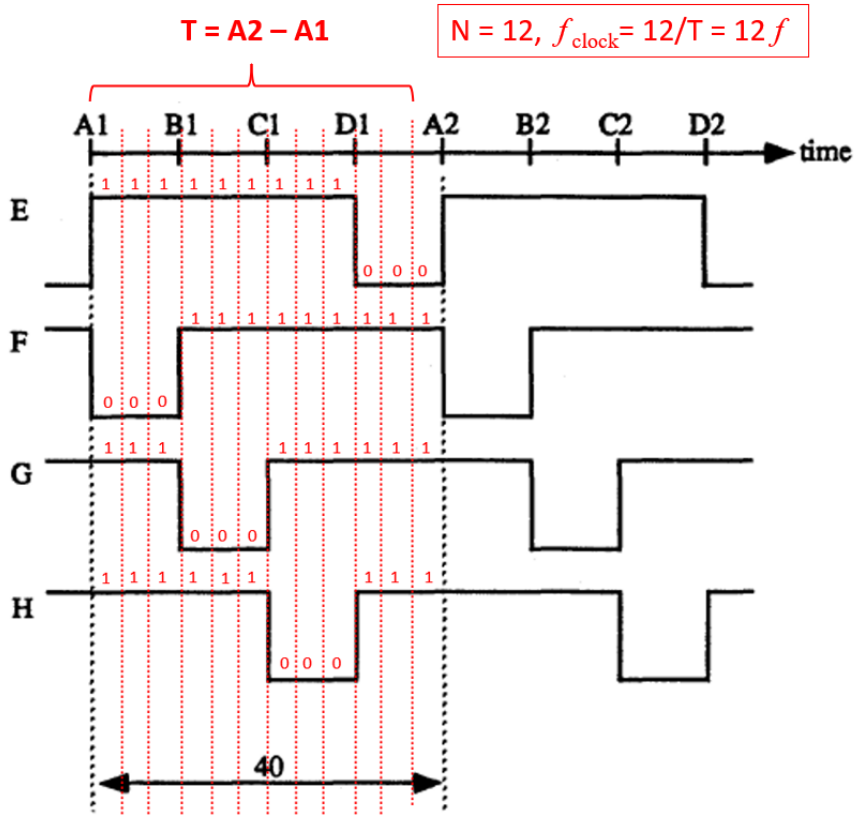


Fig. 3

EX1005, Fig. 3 (annotated); EX1003, ¶84. Accordingly, Thomas anticipates Claim 10.

F. Claim 11 – "The driver of claim 1 wherein the plurality of parallel paths comprises at least three paths."

As discussed for Claim 1, Thomas discloses more than three parallel paths. *See* EX1005, Figs. 1-2; EX1003, ¶85. Thus, Thomas anticipates Claim 11.

G. Claim 12 – "The driver of claim 1 further comprising the LEDs connected to the driver."

As discussed for Claim 1, Thomas discloses LEDs connected to the driver. *See* EX1005, Figs. 1-2; EX1003, ¶86. Thus, Thomas anticipates Claim 12.

H. Claim 14

Claim 14 is a method claim that corresponds to the limitations of Claim 1. EX1003, ¶87. For the reasons explained with respect to Claim 1, and as cross-referenced below, Thomas anticipates Claim 14. *Id.* at ¶¶87, 93.

1. Preamble [14.pre]

Thomas discloses the preamble. *See supra* Section VI.A.1; EX1003, ¶88.

2. Limitation [14.a]

See supra Section VI.A.2; EX1003, ¶89.

3. Limitation [14.b]

See supra Section VI.A.3; EX1003, ¶90.

4. Limitation [14.c]

See supra Section VI.A.4; EX1003, ¶91.

5. Limitation [14.d]

As explained for Limitations [1.c] and [1.d], Thomas discloses generating staggered PWM signals *E, F, G,* and *H* and applying a different one of those staggered PWM signals to each of the current set circuits. *See supra* Section VI.A.4-5; EX1003, ¶92.

6. Limitation [14.e]

See supra Section VI.A.5; EX1003, ¶93.

I. Claim 17 – "The method of claim 14 wherein applying a different staggered PWM brightness control signal to each current set circuit comprises applying each staggered PWM brightness control signals to an associated transistor connected in series with the one or more LEDs in an associated parallel path, such that the transistor is turned on and off corresponding to the duty cycle of the staggered PWM brightness control signal applied to it."

Thomas anticipates Claim 14, as discussed above. EX1003, ¶94. Thomas discloses transistors 33 which are connected in series with the current set resistor and the LED in each parallel path. *See* EX1005, Fig. 2 (annotated below); EX1003, ¶95.

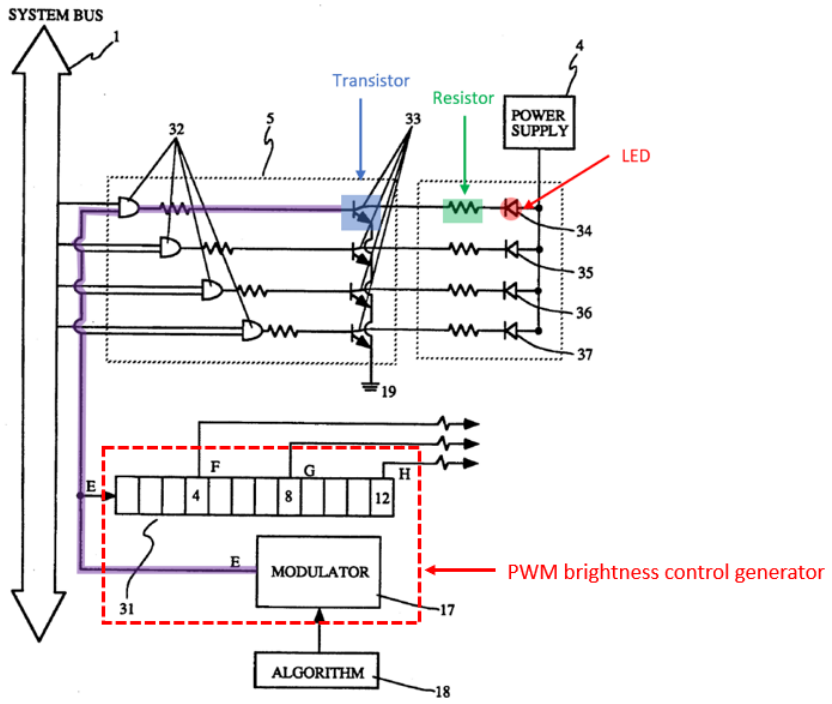


Fig. 2

Thomas explains that when the transistors 33 are turned on, they "provide current from the power supply (4) for activating the associated LED's (34-37) in the group of LED's (9)." EX1005, 3:42-45; EX1003, ¶96. As shown by the example circuit path highlighted purple above, the transistors 33 are also connected to the PWM brightness control generator (the modulator 17, algorithm 18, and delay means 16, implemented in Figure 2 as a shift register) via AND gates 32. *See* EX1005, Fig. 2, 3:24-42; EX1003, ¶96. The AND gates 32 feed control signals to turn on the transistors 33 when the AND gates receive both a high control signal (*W*, *X*, *Y*, or *Z*) for turning on the LED and a high pulse from a modulating signal (*E*, *F*, *G*, or *H*). EX1003, ¶96. Thus, the transistors 33 receive a staggered PWM brightness control

signal (*E*, *F*, *G*, or *H*) for controlling the brightness of their associated LED from the PWM brightness control generator. EX1003, ¶¶95-96. Moreover, the transistors 33 turn "on" and "off" according to the duty cycles of the staggered PWM brightness control signals applied to them. *Id.* at ¶96.

Therefore, Thomas anticipates Claim 17. *Id.* at ¶97.

J. Claim 18

Thomas anticipates Claim 18 as discussed and cross-referenced below.

1. Limitation [18.pre]

See supra Section VI.H; EX1003, ¶98.

2. Limitation [18.a]

See supra Section VI.C.2; EX1003, ¶99.

3. Limitation [18.b]

See supra Section VI.C.3; EX1003, ¶100.

4. Limitation [18.c]

See supra Section VI.C.4; EX1003, ¶101.

K. Claim 20

Thomas anticipates Claim 18 as discussed above. Thomas anticipates Claim 20 for the same reasons as Claim 9. *See supra* Section VI.D; EX1003, ¶102.

L. Claim 21

Thomas anticipates Claim 18 as discussed above. Thomas anticipates Claim 21 for the same reasons as Claim 10. *See supra* Section VI.E; EX1003, ¶103.

M. Claim 22

Thomas anticipates Claim 14 as discussed above. Thomas anticipates Claim 22 for the same reasons as Claim 11. *See supra* Section VI.F.; EX1003, ¶104.

VII. GROUND 2A – OBVIOUSNESS OVER THOMAS ALONE[8]

The discussion of Thomas from Ground 1 (Section VI) is incorporated by reference. *See also* EX1003, ¶105.

A. Claim 1

As discussed above, Thomas anticipates Claim 1. To the extent that Thomas does not anticipate Claim 1, any differences between Thomas and Claim 1 are such that Claim 1 as a whole would have been obvious to a POSITA as of the time of the invention of Claim 1. EX1003, ¶106.

For example, a POSITA would have understood from Figures 1 and 2 based on the well-known functionality of resistors that these resistors are used to limit current to a peak current $I=(V-V_{LED})/R$, as discussed for Limitation [1.b]. *See supra* Section VI.A.3.; EX1003, ¶107. Accordingly, Claim 1 would have been obvious in view of Thomas. *Id.*

[8] To the extent that Thomas anticipates a claim in the '148 Patent, it also renders the claim obvious. *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 1548 (Fed. Cir. 1983) ("[A]nticipation is the epitome of obviousness") (citation omitted).

B. Claims 3, 7, 9-12, 14, 17, 18, and 20-22

Claim 14 is a method claim that corresponds to the limitations of Claim 1. For the reasons explained for Claim 1 above, to the extent that Thomas does not anticipate Claim 14, Claim 14 would have been obvious in view of Thomas. EX1003, ¶108.

Claims 3, 7, and 9-12 depend directly or indirectly from Claim 1, and Claims 17, 18 and 20-22 depend directly or indirectly from Claim 14. EX1003, ¶109. As set forth above, the additional limitations recited by these claims are disclosed in Thomas. Therefore, to the extent that Claim 1 or 14 would have been obvious in view of Thomas, rather than anticipated by Thomas, then Claims 3, 7, 9-12, 17, 18, and 20-22 would have been obvious in view of Thomas. EX1003, ¶109.

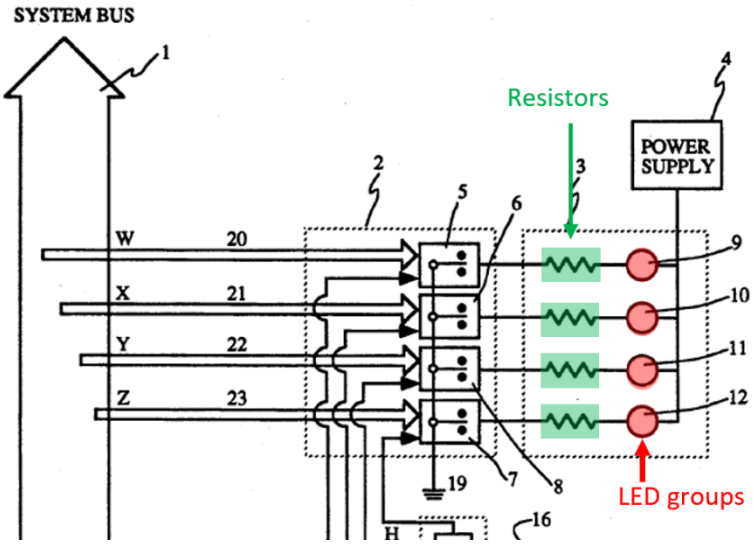
C. Claim 6

1. Preamble [6.pre] – "The driver of claim 1 wherein each current set circuit comprises:"

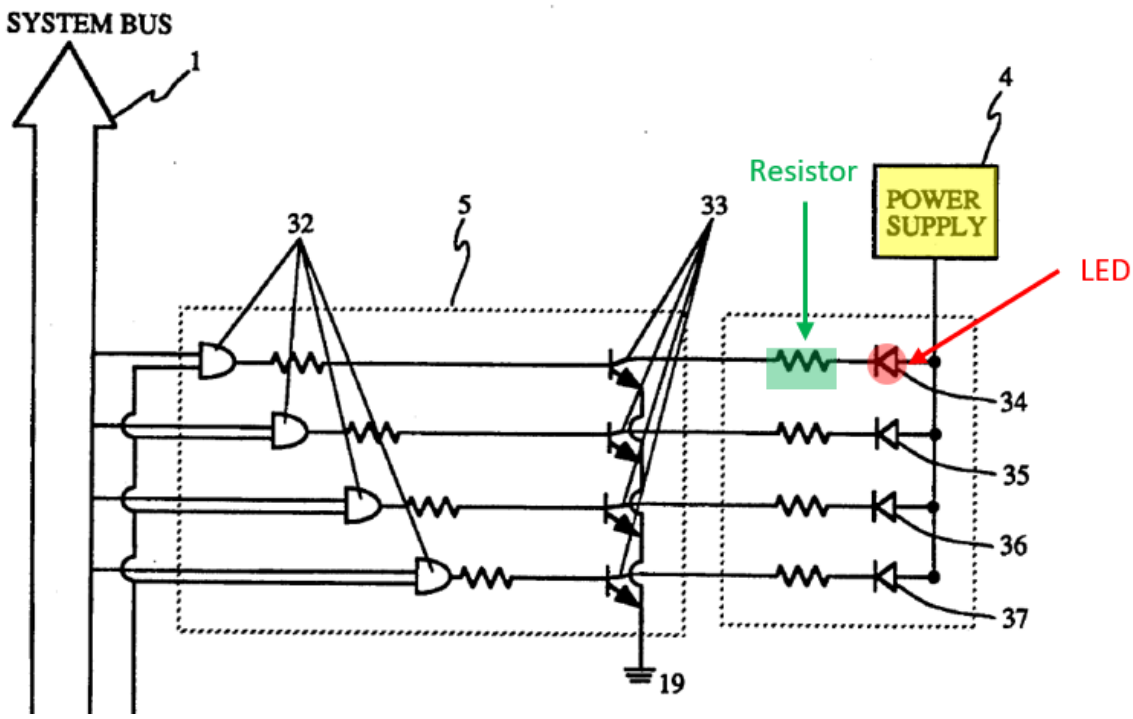
Thomas anticipates and/or renders Claim 1 obvious, as discussed above. EX1003, ¶ 110.

2. Limitation [6.a] – "a current set resistor in series with one or more LEDs in an associated parallel path; and"

Each current set circuit in Thomas' Figures 1 and 2 comprises a resistor connected in series with an LED in the parallel path associated with that resistor. EX1003, ¶111.



EX1005, Fig. 1 (cropped, annotated).



Id. at Fig. 2 (cropped, annotated); EX1003, ¶111. As discussed for Limitation [1.b], a POSITA would understand the resistors highlighted above are current set resistors

because the choice of the resistance value for those resistors sets the current that would flow through the LED according to $I=(V-V_{LED})/R$. EX1003, ¶111.

3. Limitation [6.b] – "a PWM brightness control transistor connected in series between the current set resistor and the one or more LEDs in an associated parallel path, the PWM brightness control transistor being connected to the PWM brightness control signal generator for receiving a staggered PWM brightness control signal."

As discussed for Claim 17 above, Thomas discloses transistors 33 which are connected in series with the current set resistor and the LED in each parallel path and that the transistors turn "on" and "off" according to the duty cycles of the staggered PWM brightness control signals applied to them. *See* EX1005, Fig. 2 (annotated below); EX1003, ¶112.

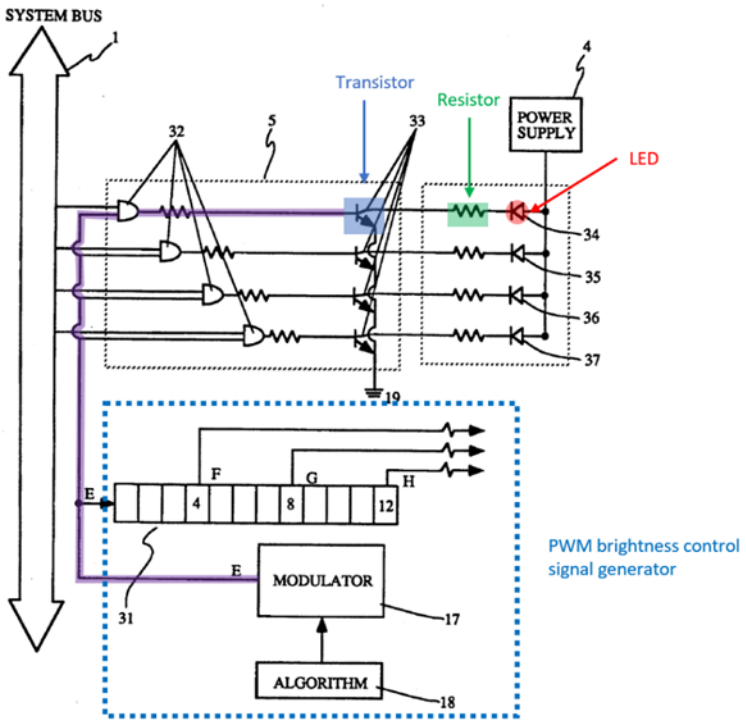
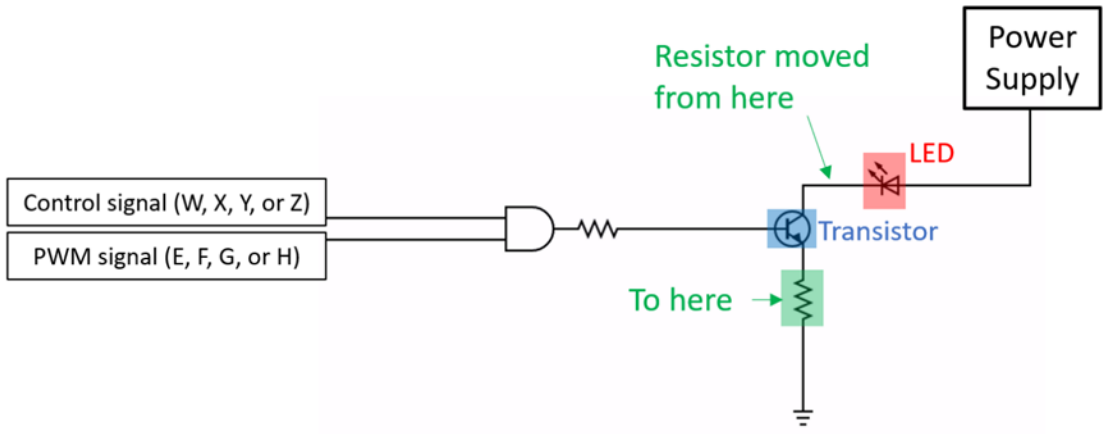


Fig. 2

Thomas does not disclose that the transistors are connected in series ***between*** the current set resistors and the LEDs in each parallel path. Thomas discloses a configuration of transistor—resistor—LED, rather than the recited configuration of resistor—transistor—LED (or the reverse). *See* EX1005, Figs. 1-2; EX1003, ¶113. However, this minor difference between Thomas and Limitation [6.b] is such that Claim 6 as a whole would have been obvious to a POSITA. EX1003, ¶113. A POSITA would have understood that the relative placement of the transistors with respect to the resistors and LEDs in each parallel path can be swapped with no change in functionality. *Id.* For example, each of the parallel paths in Thomas' Figure 2 could be modified by placing the resistor after the transistor, without changing the functionality of the circuit, as follows:



EX1003, ¶113. A POSITA would have been motivated to implement such a minor change as a design choice. *Id.* The three circuit elements (transistor, LED, and resistor) can be arranged in six ways, each of which would have operated the same

way. *Id.* Thus, a POSITA would have been motivated to use the slightly modified circuit because it would have been a simple design choice among only six possibilities that work the same way. *Id.* at ¶113 & n.3; *see also* EX1026 at 1.

In particular, a POSITA would have been motivated to connect the resistor to ground, as shown above, because the resistor can be used to easily detect the current through the LEDs. EX1003, ¶114. Engineers frequently want to be able to detect the current flowing through the load (*e.g.,* the LEDs), and having the resistor connected to ground means that the engineer only needs to measure the voltage before the resistor to determine the current (V_R/R, where V_R is the measured voltage across the resistor). *Id.* Otherwise, one would need to measure the voltage at both ends of the resistor to determine the current. *Id.* Thus, a POSITA would have been motivated to move the resistor as shown above, not only as a design choice, but also so that the resistor can act as a sense resistor for measuring the current. *Id.* A POSITA would also have had a reasonable expectation of success with this proposed modification because it would have been easy to implement with existing components with well-known techniques. EX1003, ¶115; *see e.g.* EX1026 at 1.

Accordingly, Claim 6 would have been obvious over Thomas. EX1003, ¶116.

VIII. GROUND 2B – THOMAS IN VIEW OF THE KNOWLEDGE OF A POSITA AND/OR THE AAPA

A. Claim 2 – "The driver of claim 1 wherein the voltage source is a step up voltage regulator."

Thomas anticipates and/or renders obvious Claim 1, as discussed above. EX1003, ¶117. Thomas does not expressly disclose that the voltage source is a step-up voltage regulator. Instead, Thomas discloses a generic "POWER SUPPLY." *See* EX1005, Fig. 1. It would have been obvious to a POSITA to implement a step-up voltage regulator as part of an actual embodiment of Thomas' circuit, based on the knowledge of a POSITA, and as confirmed by the AAPA. EX1003, ¶117.

Thomas describes "switching power supplies," which a POSITA would have recognized as a well-known class of power supplies that are commonly used to regulate outputs of a voltage source. EX1005, 1:68-2:4; EX1003, ¶¶118-120; EX1008, 355-360. "Switching power supplies" may be classified as step-up ("boost") or step-down ("buck") converters, or both. EX1003, ¶119; *see also* EX1001, 1:46-48. A POSITA would have been motivated to implement a step-up voltage regulator to boost an input voltage that is lower than necessary to energize the LEDs, for example from a battery or low-voltage system bus. EX1003, ¶¶121, 123. A POSITA would have had a reasonable expectation of success in implementing the power supply 4 in Thomas as a step-up voltage regulator, as the circuitry was well known. *Id.*

The '148 Patent admits that step-up voltage regulators were well known. EX1001, 1:40-41, 1:46-48, 1:57-60; EX1003, ¶122. The patent admits Figure 1A is "a typical prior art LED driver 10 that drives multiple LEDs 12 in parallel" which includes a DC voltage regulator controller 14. EX1001, 1:40-41, 1:46-48; EX1003, ¶122. The '148 Patent further admits that "***[s]uch regulators are well known*** and need not be described in detail," and that "[t]he topology of the output circuit determines whether the voltage regulator is a step up or step down regulator." EX1001, 1:57-60. Thus, the Applicant admitted that step-up voltage regulators are known in prior art LED drivers. EX1003, ¶122.

Accordingly, Claim 2 would have been obvious to a POSITA in over Thomas in view of the knowledge of a POSITA, as confirmed by the AAPA. EX1003, ¶124.

B. Claim 13 – "The driver of claim 1 wherein the driver is formed as an integrated circuit."

Thomas anticipates and/or renders obvious Claim 1, as discussed above. EX1003, ¶125. Thomas does not expressly state that the driver, or the majority of the driver, is formed as an integrated circuit, but it would have been obvious to a POSITA to implement the driver, or the majority of the driver, as an integrated circuit. EX1003, ¶125. An integrated circuit is simply a circuit that is fabricated in a package, often on a semiconductor substrate. EX1003, ¶126; *see also* EX1014, 3. In evaluating Claim 13's limitation, a POSITA would be aware that similar language is commonly used to describe a driver comprising most of its circuitry integrated

into packages while having some components such as resistors or capacitors, external to the integrated circuits.[9] EX1003, ¶126. It was standard industry practice before the '148 Patent to fabricate electronic circuits as integrated circuits. EX1003, ¶127. In practice, an engineer would design a circuit, test that design with a breadboard or computer software, and provide that design to a contract manufacturer for fabrication into an integrated circuit. *Id.* Integrated circuits have many advantages, including lower cost, ease of manufacturability, scalability for mass production, reliability, and smaller size. *Id.* A POSITA would have expected an LED driver to be fabricated as an integrated circuit. *Id.* Indeed, the '148 Patent admits that prior art LED drivers were formed as integrated circuits. *See* EX1001, 1:40-45 (describing "prior art LED driver" where "[m]ost components of the driver 10 are formed on an integrated circuit chip" and "LEDs are typically connected to pins extending from the chip package"); EX1003, ¶128. Thomas describes that an LED driver can be used for controlling indicator lights on a computer. EX1005, 1:12-22. A POSITA would have expected to implement Thomas' driver as an integrated circuit and would have had a reasonable expectation of success doing so.

[9] In fact, Patent Owner contends in its infringement contentions that Claim 13 is met because the accused televisions each have a driver in which the majority of the circuitry is part of an LED diver IC (i.e., NT5011S or AS3824). EX1015, EXHIBIT A at pp.53-56. EX1003, ¶126 n.4.

EX1003, ¶129. Thus, Claim 13 would have been obvious over Thomas in view of the knowledge of a POSITA. EX1003, ¶130.

C. Claim 15 – "The method of claim 14 further comprising varying the duty cycle of the staggered PWM brightness control signals to change an average current through the parallel paths of LEDs to change a perceived brightness of the LEDs."

Thomas anticipates and/or renders obvious Claim 14, as discussed above. EX1003, ¶131. A POSITA would have understood that Thomas describes the concept of varying the duty cycle of a PWM signal to change the brightness of the LEDs. EX1003, ¶¶131-132. Thomas explains that pulse width modulation is used "[t]o control the intensity of the LED's within the array" by "produc[ing] a series of rapid activations of the enabled LED's." EX1005, 1:23-42. Thomas explains that "[t]he width of a given pulse in the period of the modulating signal determines the length of time that the enabled LED's will be activated during the period." *Id.* at 1:36-38. A POSITA would understand Thomas as referring to the "duty cycle" of the PWM signal, which is an expression of how long the PWM signal is "on" or at its high state during its period. EX1003, ¶132. Thomas explains that the period of a modulating signal "is in the order of microseconds so that the series of activations of the LED's produce an appearance that the LED's are being dimmed rather than being turned on and off." EX1005 at 1:38-42; EX1003, ¶132. Thomas also explains that "[t]he precise wave form of the modulating signal output from the modulator may be determined by the use of an algorithm (18) implemented in either software

or hardware as is well-known in the art." *Id.* at 3:47-51. The algorithm sets the duty cycle by determining the waveform of the PWM signal to be generated by the modulator 17, and thus determining different waveforms would be varying the duty cycle. EX1003, ¶¶132-134. A POSITA would also have understood varying the duty cycle of the PWM signal as a conventional way to control the brightness of the LED's. *See* EX1003, ¶134; EX1021, ¶10. Thus, Thomas describes varying the duty cycle of the PWM signals to change the perceived brightness of the LEDs. EX1003, ¶134.

Thomas further describes varying the duty cycle when describing Figure 3. Thomas explains that the timings of the positive edges are "fixed to occur at the designated times," and that "the falling edges can occur at any subsequent time." EX1005, 4:60-65, Fig. 3 (annotated below); EX1003, ¶133.

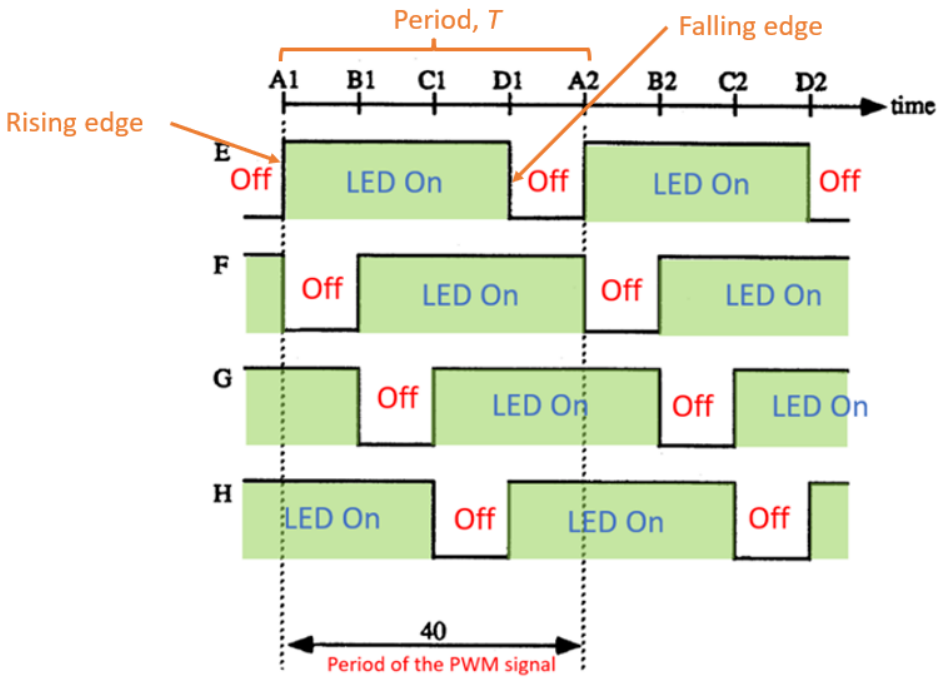


Fig. 3

By fixing the rising edge of the signal and changing the timing of the falling edge, the amount of time the LED is on in the period is varied, and thus, the duty cycle is varied. EX1003, ¶133.

Thomas does not expressly describe varying the duty cycle of a PWM signal changes the average current, but this is inherent in PWM control of an LED and a POSITA would have known that to be the purpose of PWM control. EX1003, ¶135. Indeed, the '148 Patent admits using PWM to control the average current through an LED was known. *See* EX1001, 2:7-18; EX1003, ¶136. A POSITA would have understood that a duty cycle of X% corresponds to an average current that is X% of the peak current. *Id.* at ¶135.

Accordingly, Claim 15 would have been obvious over Thomas in view of the knowledge of a POSITA, as confirmed by the AAPA. EX1003, ¶137.

IX. GROUND 2C – THOMAS IN VIEW OF TATEWAKI AND THE KNOWLEDGE OF A POSITA

A. Claim 8 – "The driver of claim 7 wherein the shift register has a connection that connects an end bit position to a first bit position so that bits in the shift register are recirculated in the shift register."

Thomas anticipates and/or renders obvious Claim 7, as discussed above. EX1003, ¶138. Thomas does not expressly disclose the shift register recirculates the end bit into the first bit position. However, it would have been obvious to modify Thomas' shift register to connect the end bit position to the first bit position so that the shift register recirculates the bits in the shift register. EX1003, ¶138.

A POSITA would have known that a shift register can have its output at the end bit fed back into its input so that the bit sequence stored in the shift register recirculates. EX1003, ¶139; EX1010, 1:17-27 (when a shift register output is input to the shift register, "the shift register operates in what is termed a 'recirculating' mode."). Recirculating shift registers are known in the art as "ring counters." EX1003, ¶139; EX1011, 119, Fig. 12.6 (reproduced below).

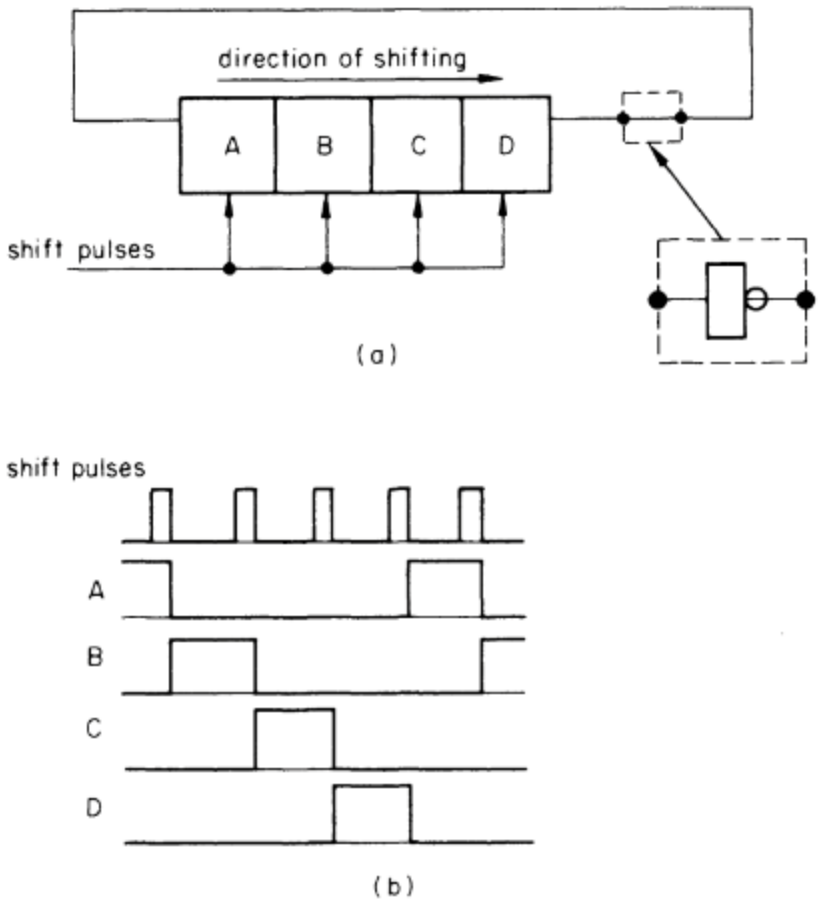


Fig. 12.6 A ring counter

EX1011, 119.

Ring counters were known to be used in LED drivers. EX1003, ¶140. Tatewaki discloses an LED lamp for a car interior which is driven with a PWM control circuit. *See* EX1007, 12:11-30, 13:25-47; EX1003, ¶140. Tatewaki explains that "a ring counter installed in the PWM control circuit" is used to control the brightness of the LEDs. EX1007, 13:26-47; EX1003, ¶140. Tatewaki explains:

> [E]ach time the on-off switch 163 is activated, a ring counter installed in the PWM control circuit 162 operates so that a duration of the on and

> off of the LED chip 132, 142 is changed, thereby controlling the brightness.

EX1007, 13:35-38; *see also id.* at 12:20-23.

A POSITA would have understood from Tatewaki's disclosure and their general knowledge of ring counters that a ring counter would be able to receive a bit sequence for a PWM duty cycle, hold that bit sequence, and recycle it indefinitely to drive the LEDs at a constant brightness until there is a command to change the brightness. EX1003, ¶141. A POSITA would have understood that modifying Thomas' shift register into a ring counter would have been beneficial because once a desired brightness is set with a particular PWM signal generated by the algorithm 18, the ring counter would be able to constantly output that PWM signal until another change in brightness is desired. EX1003, ¶142.

A POSITA would have recognized the benefits of such a modification where LED brightness is unlikely to change frequently. EX1003, ¶142. For example, Thomas describes an LED driver used to control the brightness of indicator lights on a computer front panel. EX1005, 1:12-42. There, the brightness of the LEDs is unlikely to be changed frequently, so a ring counter would be beneficial. EX1003, ¶143. Similarly, a ring counter would also be useful for a display backlight, where a user is unlikely to constantly change the screen brightness. *Id.*

A POSITA would have reasonably expected success in modifying Thomas' shift register into a ring counter because the circuitry for ring counters and their use in LED drivers was well-known and straightforward to implement. EX1003, ¶144. Modifying a shift register into a ring counter would entail connecting the output of the shift register into its input. EX1003, ¶¶139, 144; *see also* EX1011, 119. A POSITA would have known how to perform such a modification and any additional modifications necessary to implement it. EX1003, ¶144. Accordingly, Claim 8 would have been obvious to a POSITA over Thomas in view of Tatewaki and the knowledge of a POSITA. EX1003, ¶145.

B. Claim 19 – "The method of claim 18 further comprising recirculating bits in the shift register by feeding a bit at an output bit position to an input bit position along the shift register."

Thomas anticipates and/or discloses Claim 18, as discussed above. EX1003, ¶146. Claim 19 would have been obvious over Thomas in view of Tatewaki and the knowledge of a POSITA, as discussed for Claim 8, above. *Id.*

X. GROUND 3– ANTICIPATION BY *ZANE*

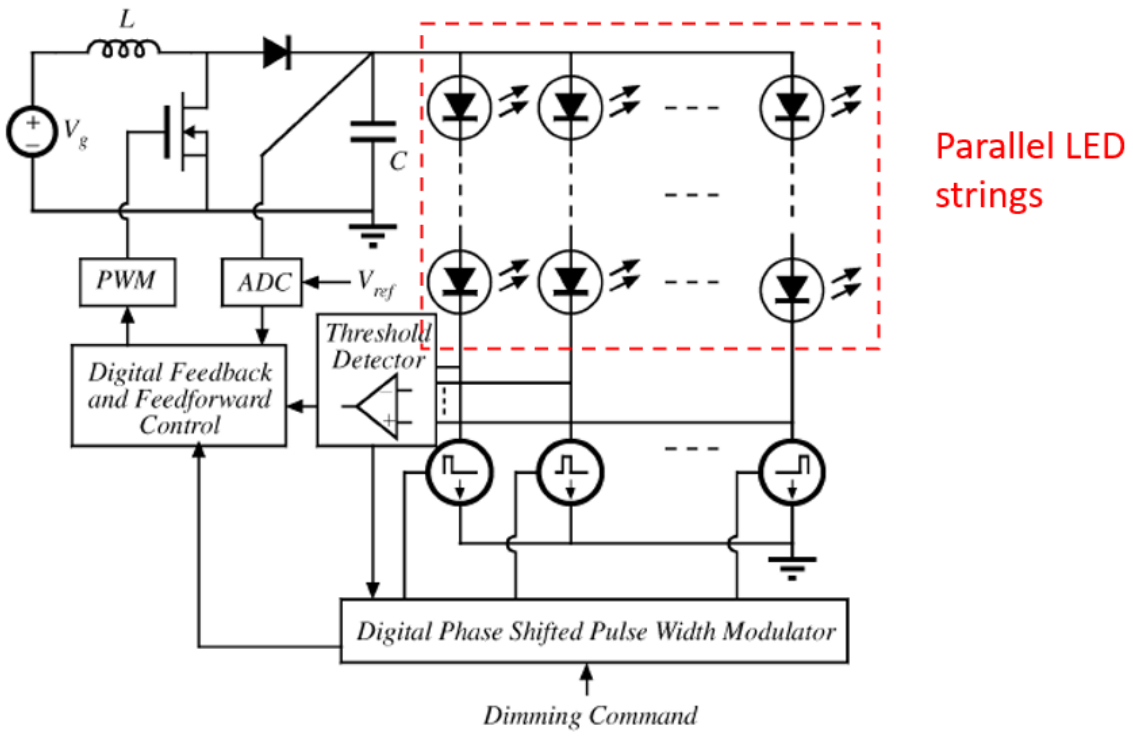
A. Claim 1

Zane anticipates Claim 1.

1. Preamble [1.pre] – "A light emitting diode (LED) driver for driving LEDs connected to different parallel paths,"

Zane discloses an LED driver and "strings" of LEDs in at least three parallel paths. *See* EX1006, 287 ("This paper introduces a digital architecture suitable for

driving a large number of High Brightness Light Emitting Diodes….”), Fig. 1 (“Proposed digital architecture for driving a scalable number of parallel LED strings.”); *see also* EX1003, ¶147.



EX1006, Fig. 1 (annotated).

2. <u>Limitation [1.a] – “the driver comprising: a voltage source for connection to first ends of LEDs in a plurality of parallel paths;”</u>

Zane discloses a voltage source for connection to first ends of LEDs in a plurality of parallel paths. *See* EX1006, 288 (“The proposed architecture, shown in Fig. 1, consists of ***a power converter driving multiple strings of LEDs***….”); Figs. 1, 3; EX1003, ¶148.

Figure 1 shows a voltage source enclosed in the orange dashed box and which includes a voltage V_g and a power converter circuit. EX1006, Fig. 1; EX1003, ¶148. The voltage source is connected to the parallel LED arrays via one end of the LEDs. *See* EX1006, Fig. 1 (annotated below); EX1003, ¶148.

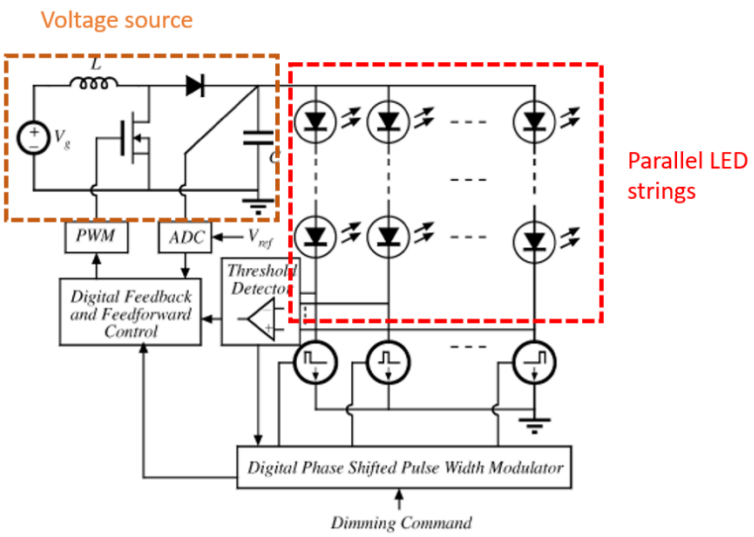
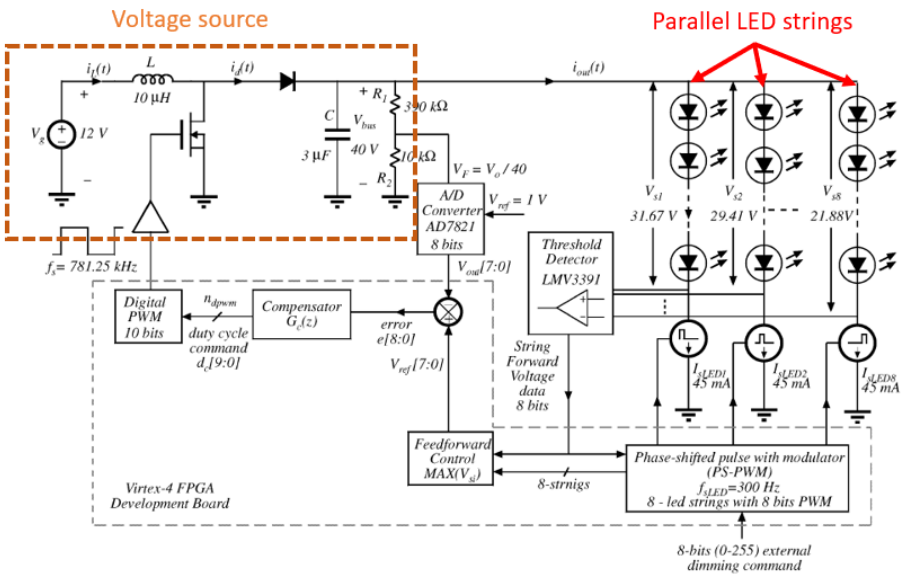


Figure 3 further details the experimental setup for the LED driver shown in Figure 1. *See* EX1006, Figs. 1, 3; EX1003, ¶149.

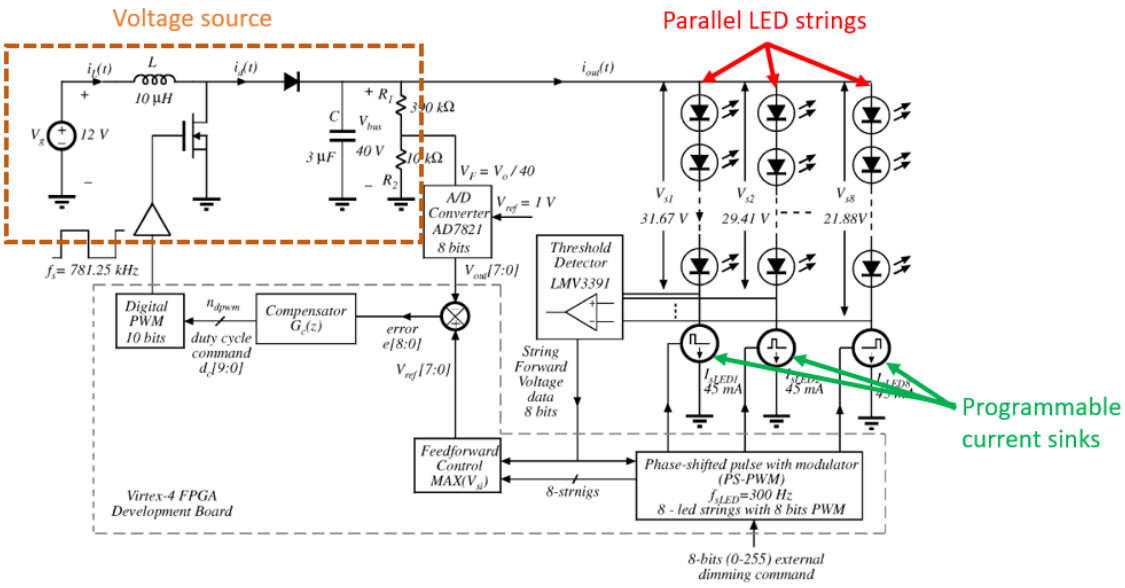


EX1006, Fig. 3 (annotated).

3. Limitation [1.b] – "a plurality of current set circuits, one current set circuit per parallel path, each current set circuit controlling a peak current through one or more LEDs connected in each parallel path; and"

Zane discloses current set circuits, specifically, programmable linear current sinks in each parallel string of LEDs, which control the peak currents through each of the LED strings. *See* EX1006, 290 ("In this architecture a linear programmable current sink is used to regulate the LED forward current to a desired level.") Figs. 3, 4; EX1003, ¶150.

As shown in Figure 3 below, the architecture comprises a plurality of these current sinks, one per parallel LED string, each connected to the cathodes of the LEDs in one of the parallel strings.



EX1006, Fig. 3 (annotated); EX1003, ¶150.

Figure 4 details the programmable current sink used in the LED driver shown in Figure 3. EX1006, Figure 4 (below); EX1003 ¶151.

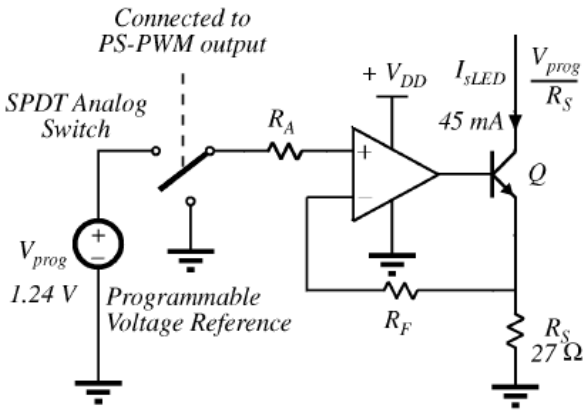


Figure. 4. An op-amp based precision programmable current sink with AM and PWM control options

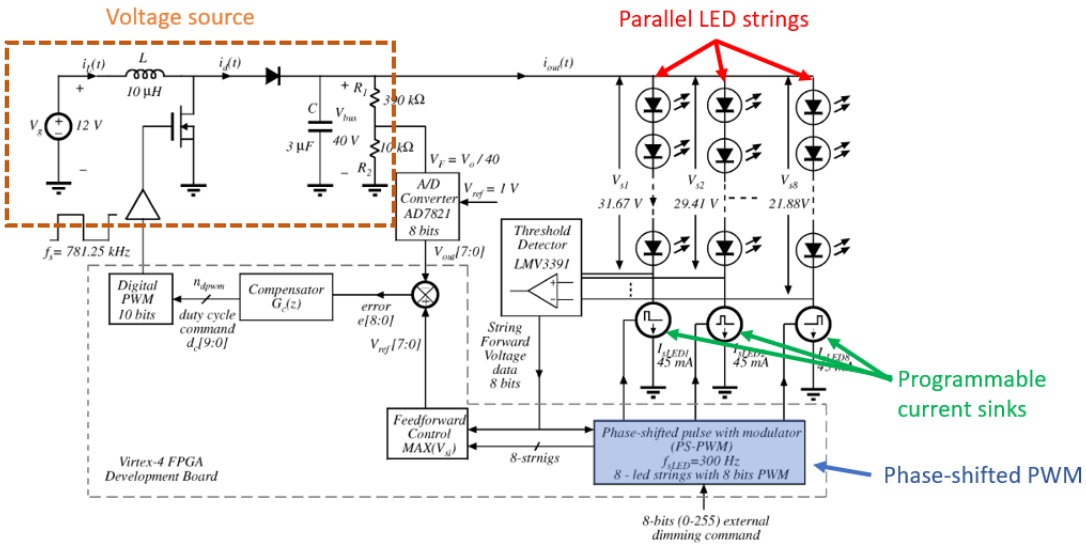
Zane discloses that "[t]he forward current through the LEDs is regulated by a discrete precision programmable current sink, as shown in Fig. 4," and that "the LED string current is regulated to a value of 45 mA by the choice of appropriate resistor,

R_s." EX1006, 290-291; *see also id.* at 291 ("[T]he peak-to-peak load current amplitude is limited by the PS-PWM block to just one LED string regulation current (45 mA)."); EX1003, ¶152. Accordingly, *Zane's* current sink controls the peak current flowing through the one or more LEDs connected in the corresponding string. *Id.*

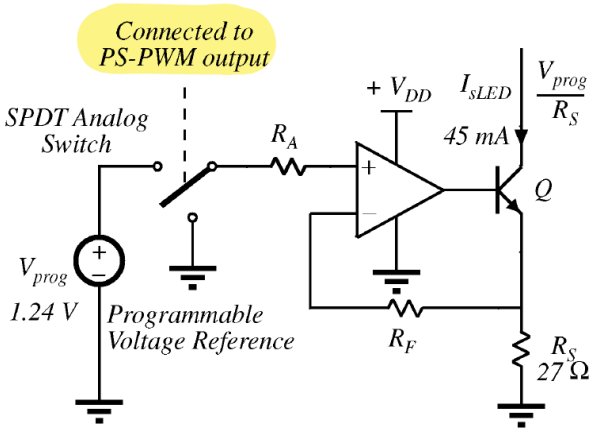
4. Limitation [1.c] – "a pulse-width modulated (PWM) brightness control signal generator connected to the plurality of current set circuits, the brightness control signal generator being configured to generate staggered PWM brightness control signals to the plurality of current set circuits,"

Zane's proposed architecture further comprises a digital phase-shifted pulse width modulator (PS-PWM) which is connected to the plurality of current set circuits (programmable current sinks). *See* EX1006, Fig. 3 (annotated below), 291 ("An 8-bit (256 steps) 300 Hz PS-PWM is implemented on FPGA to control the operation of individual current sinks."); EX1003, ¶153.[10]

[10] "FPGA" refers to a "Field Programmable Gate Array," which is an off-the-shelf integrated circuit that circuit designers can reconfigure after manufacturing for specific purposes. EX1003, ¶153 n.5.



Zane's PS-PWM generates staggered PWM brightness control signals to the plurality of current sinks. EX1003, ¶154. As shown below, the linear programmable current sink in *Zane* receives an output from the PS-PWM.



EX1006, Fig. 4 (annotated); EX1003, ¶154. "The PS-PWM block controls the switching sequence and duty cycle of individual current sources based on the digital command (d bits) received from microcontroller or color control ASIC. … The modulator rotates which strings are active, resulting in a natural phase shifting of the LED string drive signals that respond immediately to command inputs." EX1006,

288 (emphasis omitted); *see also id.* at 291 ("An external dimming command, received by the PS-PWM module, is used to determine the appropriate phase-shift and duty cycle of individual control output signals."). Figure 2(a) shows "the individual outputs of PWM signals of the PS-PWM are phase shifted," and thus the PWM signals are staggered. *Id.* at 289; EX1003, ¶155. Additionally, Figure 2(a) shows that a different staggered PWM signal is applied to each of the LED strings. *Id.*; EX1006, Fig. 2(a) (below).

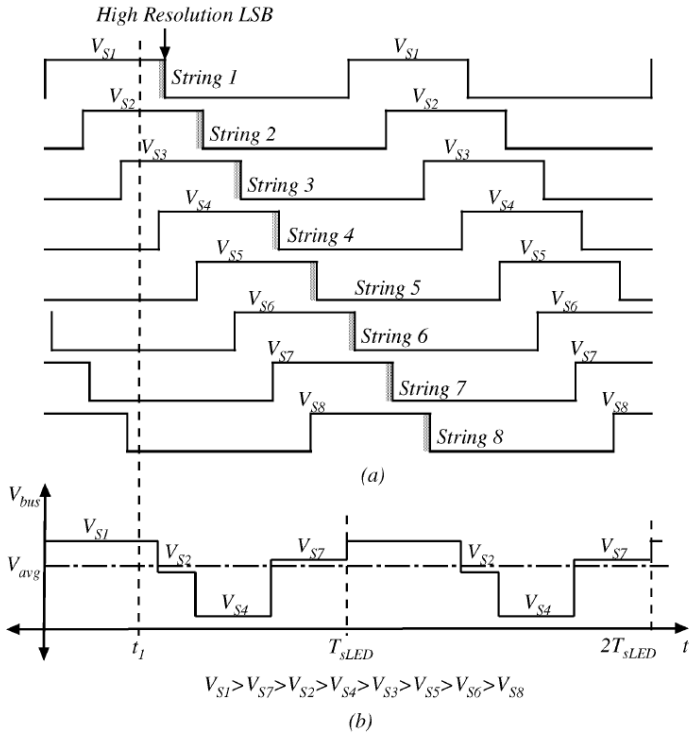


Figure 2(a). PS-PWM operating waveforms at 40% dimming command (*Dim*=0110_0110 {102}, *MSB* = 011 {3}, *LSB* = 0_0110 {6}) illustrating the phase rotation, with three LED strings '*on*' at a given time and the LSB output (shaded area) added to end of each MSB to generate required resolution.

5. Limitation [1.d] – "each current set circuit being configured to draw the peak current through its associated one or more LEDs at a duty cycle substantially corresponding to a duty cycle of a PWM brightness control signal applied to it, such that the plurality of current set circuits conduct current through their associated one or more LEDs at the same duty cycle but out of phase with each other."

Zane discloses each of the current set circuits are controlled by the PS-PWM to conduct current according to the PWM signal output to the respective strings. EX1006, 291 ("An 8-bit (256 steps) 300 Hz PS-PWM is implemented on FPGA to control the operation of individual current sinks."); EX1003, ¶156. *Zane* further discloses that the current set circuits are configured to draw the peak current through the LEDs in their associated parallel string at a duty cycle of the PWM brightness control applied to the current set circuits. EX1006, 290-291 ("[T]he LED string current is regulated to a value of 45 mA by the choice of appropriate resistor, R_S."), 291 ("An external dimming command, received by the PS-PWM module, is used to determine the appropriate phase-shift and duty cycle of individual control output signals. … [T]he peak-to-peak load current amplitude is limited by the PS-PWM block to just one LED string regulation current (45 mA)."); EX1003, ¶156.

Figure 6 illustrates the currents flowing through three parallel strings of LEDs when the PS-PWM operates with a dimming command of 50%. EX1006, 291, Fig. 6. As illustrated, the current sinks for the parallel LED strings conduct current

through their associated LEDs at the same duty cycle but out of phase with each other. EX1003, ¶157.

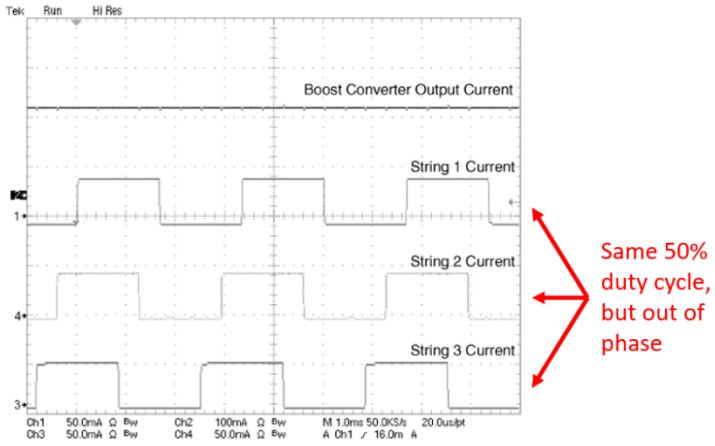


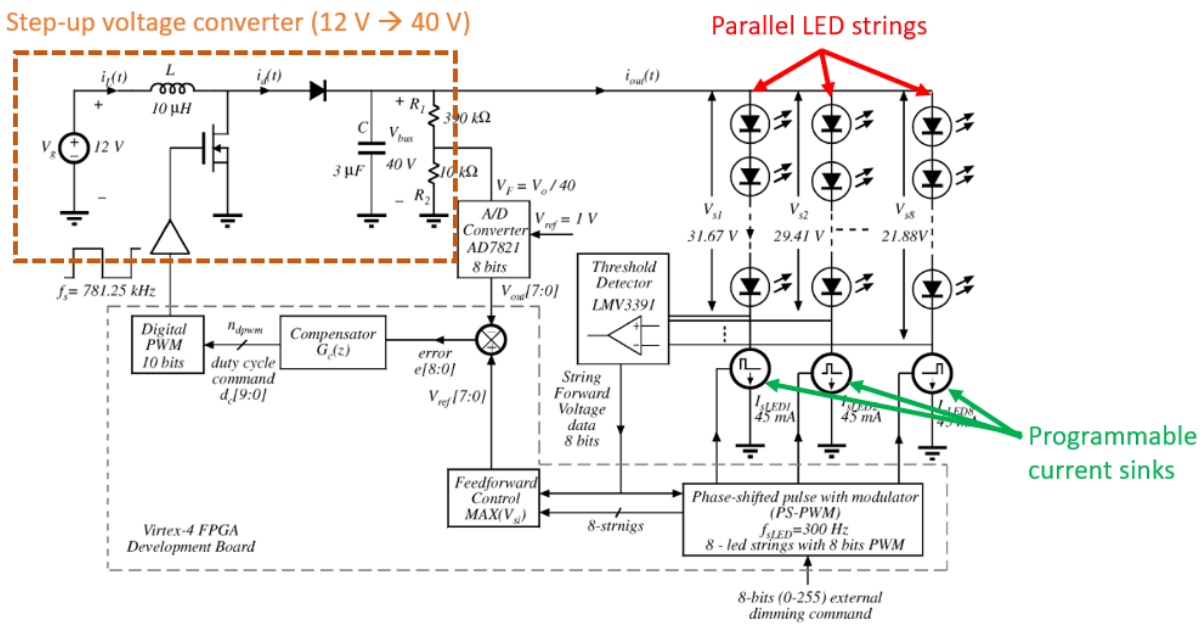
Figure. 6. Experimental system waveforms demonstrating operation of the PS-PWM block at an input command *Dim* = 50%. Current waveforms are shown for the boost converter output and 3 of the 8 LED string currents.

EX1006, Fig. 6 (annotated); EX1003, ¶157.

Accordingly, *Zane* anticipates Claim 1. EX1003, ¶158.

B. <u>Claim 2 – "The driver of claim 1 wherein the voltage source is a step up voltage regulator."</u>

Zane anticipates Claim 1, as discussed above. EX1003, ¶159. Zane discloses that the voltage source in Figure 3 is a boost converter, which steps up a 12V input (V_g) to a 40V output. *Id.*; EX1006, 290 ("The boost converter is designed to output a 40 V signal from 12 V input supply …. The output is fed to an LED board, with an array of 64 LEDs split into 8 parallel strings of 8 LEDs each.").



EX1006, Fig. 3 (annotated); EX1003, ¶159. A "boost converter" is another name for a step-up voltage converter. *Id.*; EX1008, 355-360. Accordingly, *Zane* anticipates Claim 2.

C. <u>Claim 3 – "The driver of claim 1 wherein each current set circuit is a current regulator."</u>

Zane anticipates Claim 1, as discussed above. EX1003, ¶160. As discussed for Limitation [1.b], *Zane*'s linear current sinks are current regulators. *See* EX1003, ¶160; EX1006, 290 ("In this architecture a linear programmable current sink is used to regulate the LED forward current to a desired level."), *id.* ("The forward current through the LEDs is regulated by a discrete precision programmable current sink, as shown in Fig. 4."), Figs. 3-4. Accordingly, *Zane* anticipates Claim 3.

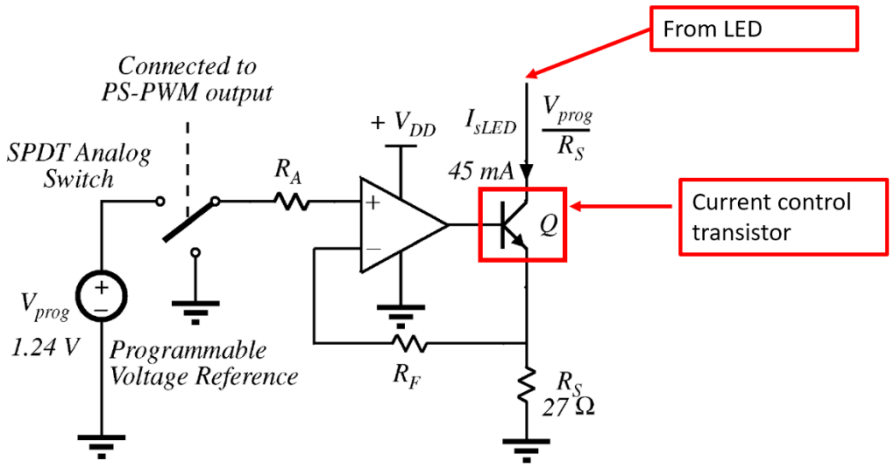
D. Claim 4

1. Preamble [4.pre] – "The driver of claim 1 wherein each current set circuit is a current regulator comprising:"

Zane anticipates Claim 1, as discussed above. EX1003, ¶161. As discussed for Claim 3, *Zane* discloses programmable current sinks, which are current regulators, in each parallel string of LEDs. *See supra* Section X.C. EX1003, ¶161.

2. Limitation [4.a] – "a current control transistor in series with one or more LEDs in an associated parallel path; and"

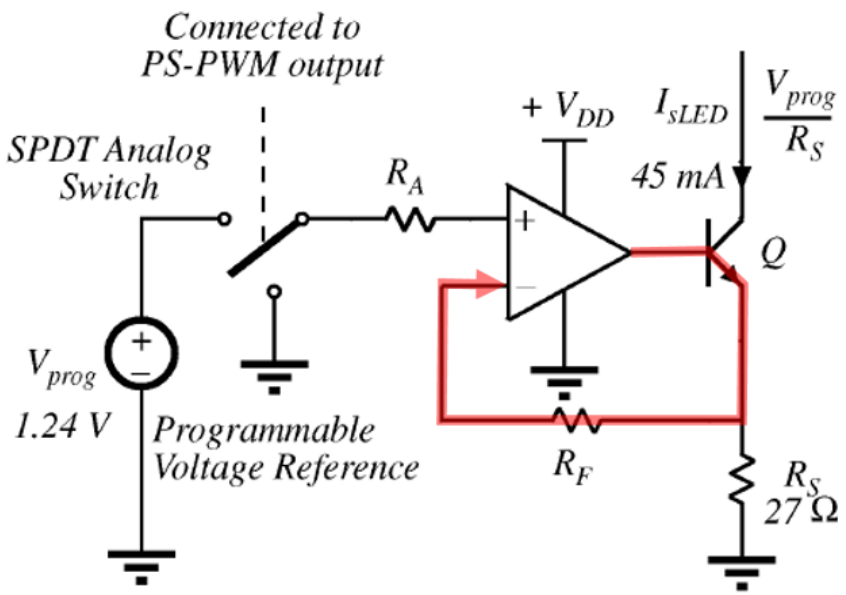
Each current sink in each parallel string comprises a current control transistor *Q* which is connected in series to the LEDs in that parallel string. *See* EX1006, Fig. 3 (showing current sinks in each parallel path), Fig. 4 (current sink circuit diagram); EX1003, ¶162.



EX1006, Fig. 4 (annotated); EX1003, ¶162.

3. Limitation [4.b] – "a feedback circuit connected to detect a current through the parallel path and connected to the current control transistor to control a conductivity of the current control transistor to cause the current through the parallel path to match a reference level."

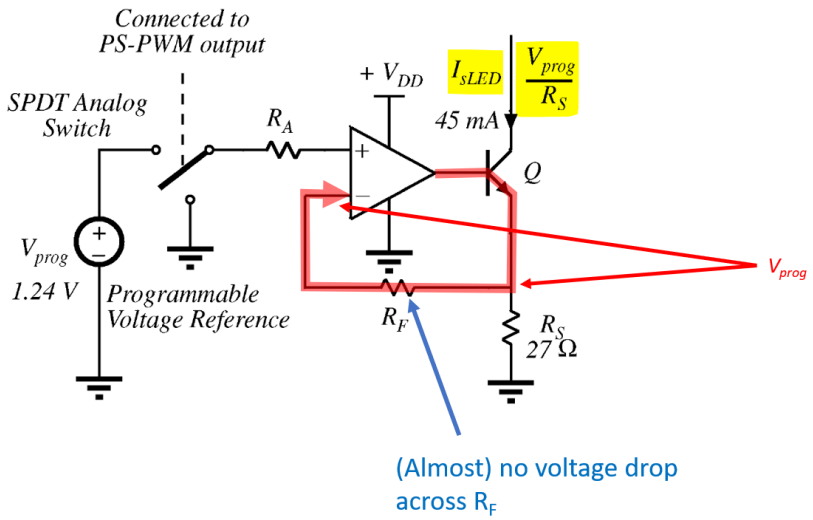
Figure 4 shows each current sink comprises a feedback circuit connected to the transistor *Q*. EX1003, ¶163. Specifically, the op amp feeds its output back into its inverting (-) input, as shown in the path highlighted red below:



EX1006, Fig. 4 (annotated); EX1003, ¶163.

The feedback circuit detects a current through the parallel path using the resistor R_s and is connected to the current control transistor, *Q*, to control the conductivity of that transistor. EX1003, ¶164. *Zane* explains that the current through the parallel path is $I_{sLED} = \frac{V_{prog}}{R_s}$, where V_{prog} is a programmable voltage

reference that is input to the noninverting input of the op amp. *See* EX1006, 290-291, Fig. 4 (annotated below); EX1003, ¶164.



Thus, *Zane*'s current sink causes the current through the parallel path to match a reference level, defined as V_{prog}/R_s. EX1003, ¶164. Thus, Zane anticipates Claim 4. EX1003, ¶165.

E. Claim 11– "The driver of claim 1 wherein the plurality of parallel paths comprises at least three paths."

Zane anticipates Claim 1, as discussed above. EX1003, ¶166. As shown in Figure 1 and discussed with relation to preamble [1.pre] above, *Zane*'s system comprises at least three parallel strings of LEDs. *See supra* Section X.A.1.; EX1006, Figure 1; EX1003, ¶166. Zane anticipates Claim 11.

F. Claim 12– "The driver of claim 1 further comprising the LEDs connected to the driver."

Zane anticipates Claim 1, as discussed above. EX1003, ¶167. As shown in Figures 1 and 3, and as discussed with relation to claim limitation [1.pre] above,

Zane's system comprises LEDs connected to the driver. *See supra* Section X.A.1.; EX1006, Figs. 1, 3; EX1003, ¶167.

G. Claim 14

Zane anticipates Claim 14. EX1003, ¶168.

1. Preamble [14.pre]

See supra Section X.A.1; EX1003, ¶169.

2. Limitation [14.a]

See supra Section X.A.2; EX1003, ¶170.

3. Limitation [14.b]

See supra Section X.A.3; EX1003, ¶171.

4. Limitation [14.c]

See supra Section X.A.4; EX1003, ¶172.

5. Limitation [14.d]

As explained for Limitations [1.c] and [1.d], *Zane* discloses generating staggered PWM brightness control signals and applying a different one of those signals to each of the current set circuits in each string of LEDs. *See supra* Section X.A.4-5; EX1003, ¶173.

6. Limitation [14.e]

See supra Section X.A.5; EX1003, ¶174.

H. Claim 17

Zane anticipates Claim 14, as discussed above. EX1003, ¶175. *Zane* discloses the additional limitation of Claim 17 as explained for Limitations [4.a] and [4.b]. *See supra* Sections X.D.2.-3.; EX1003, ¶175. *Zane* anticipates Claim 17.

I. Claim 22

Zane anticipates Claim 14, as discussed above. EX1003, ¶176. *Zane* discloses more than three parallel paths. *See supra* Sections X.A.1, X.A.4; EX1003, ¶176. *Zane* anticipates Claim 22.

XI. GROUND 4 – OBVIOUSNESS IN VIEW OF *ZANE* ALONE[11]

The discussion of *Zane* from Ground 3 (Section X) is incorporated by reference. *See also* EX1003, ¶177.

A. Claims 1-4, 11, 12, 14, 17, and 22

As discussed above, *Zane* anticipates Claim 1-4, 11, 12, 14, 17, and 22. To the extent that *Zane* does not anticipate Claim 1, any differences between *Zane* and Claim 1 are such that Claim 1 as a whole would have been obvious to a POSITA as of the time of the invention of Claim 1. EX1003, ¶178.

Claim 14 is a method claim that corresponds to the limitations of Claim 1. For the reasons explained for Claim 1 above, to the extent that *Zane* does not

[11] To the extent that *Zane* anticipates a claim in the '148 Patent, it also renders the claim obvious. *See supra* footnote 4.

anticipate Claim 14, Claim 14 would have been obvious in view of *Zane*. EX1003, ¶179.

Claims 2, 3, 4, 11, 12, and 17 depend directly or indirectly from Claim 1 and Claims 17 and 22 depend directly or indirectly from Claim 14. As explained above, the additional limitations recited by these claims are disclosed in *Zane*. Therefore, to the extent that Claim 1 or 14 would have been obvious in view of *Zane*, rather than anticipated by *Zane*, then Claims 2, 3, 11, 12, 17, and 22 would have been obvious in view of *Zane*. EX1003, ¶180.

B. Claim 5

1. Preamble [5.pre] – "The driver of claim 4"

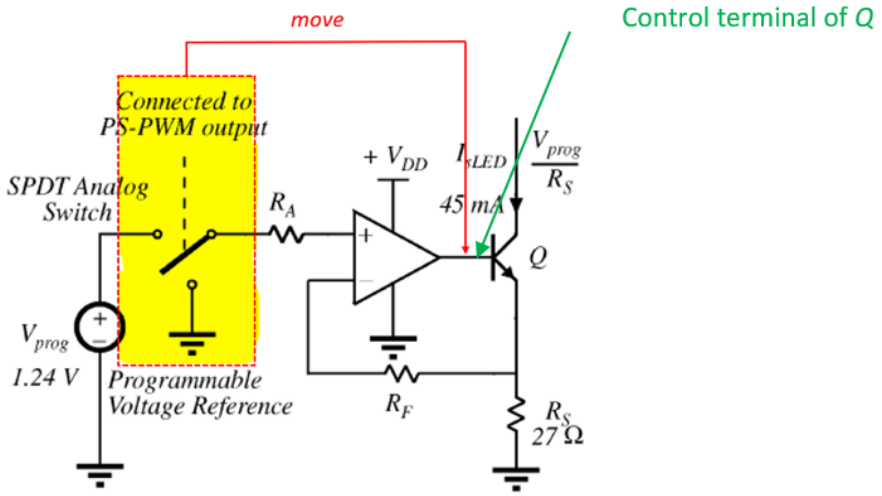
Zane anticipates and/or renders Claim 4 obvious, as discussed above. EX1003, ¶181.

2. Limitation [5.a] – "wherein each current set circuit further comprises a PWM brightness control transistor connected between an output of the feedback circuit and a control terminal of the current control transistor,"

Zane's programmable current sink further comprises a SPDT (single-pole double-throw) analog switch that connects to the PS-PWM output. *See* EX1006, Fig. 4. A POSITA would have understood that the switch would have been implemented with at least one transistor. EX1003, ¶182. A POSITA would have had many options readily at hand to implement *Zane*'s SPDT analog switch, each of which comprises one or more transistors. *Id.* Alternatively, a POSITA would have

readily implemented *Zane*'s SPDT analog switch with at least one transistor because the switch is controlled by the PS-PWM output. EX1003, ¶183. Therefore, a POSTA would have understood that *Zane*'s SPDT analog switch is or would have been implemented as a PWM brightness control transistor. *Id.*

Zane does not disclose that the PWM brightness control transistor is "connected ***between*** an output of the feedback circuit and a control terminal of the current control transistor." EX1003, ¶184. Instead, *Zane* discloses that the PWM brightness control transistor is connected before the noninverting input of the op amp. *See* EX1006, Fig. 4; EX1003, ¶184. However, it would have been obvious to modify *Zane* by moving the PWM brightness control transistor from the noninverting input of the op amp to between the output of the op amp (the output of the feedback circuit) and the control terminal of the current control transistor *Q*. *Id.* A POSITA would understand the base terminal of *Q*, identified below, is a control terminal because applying a voltage to the base terminal turns on the transistor. *Id.*



EX1006, Fig. 4 (annotated); EX1003, ¶184.

The PWM brightness control transistor may be placed in several locations in this circuit without changing the overall operation of the circuit because its function is to act as a switch that turns "on" and "off" the programmable current sink, and hence, the current through the LEDs. EX1003, ¶185. When the PWM brightness control transistor is located before the noninverting input, the transistor would switch the reference voltage between V_{prog} (current flows through LEDs) and ground (no current flows through LEDs). *Id.* When the PWM brightness control transistor is located between the output of the op amp and the control terminal of *Q*, the transistor would either open (no current through LEDs) or close (current flows through LEDs) the feedback loop. *Id.* The transistor could also be located elsewhere in the circuit as well, so long as it turns "on" or "off" the current flowing through the LEDs. *Id.* at ¶¶185-186 & n.8; EX1027 at Fig. 1. Thus, a POSITA would have understood that there are a finite number of ways in which the PWM brightness control transistor

could be connected to *Zane*'s programmable current sink, and it would have been obvious to try any of those solutions as a design choice. EX1003, ¶186. A POSITA would have also had a reasonable expectation of success with the proposed modification because it involves the use of well-known techniques in circuit design. *Id.*

3. Limitation [5.b] – "the PWM brightness control transistor being connected to the PWM brightness control signal generator for receiving a staggered PWM brightness control signal to couple the output of the feedback circuit to the control terminal of the current control transistor at a duty cycle of the staggered PWM brightness control signal."

As shown in Figures 3 and 4, the SPDT switch, which is the PWM brightness control transistor, is connected to the PS-PWM output for receiving a phase-shifted (staggered) PWM brightness control signal. *See supra* Section XI.B.2.; EX1006, Figs. 3-4; EX1003, ¶187.

After a POSITA has modified the SPDT analog switch to connect between the output of the feedback circuit and the base terminal of transistor Q, the modified SPDT analog switch would automatically couple the output of the feedback circuit to the control (base) terminal of the current control transistor according to the duty cycle of the staggered PWM brightness control signal. EX1003, ¶188. Accordingly, Claim 5 would have been obvious over *Zane*. EX1003, ¶189.

C. Claim 13 – "The driver of claim 1 wherein the driver is formed as an integrated circuit."

Zane anticipates and/or renders obvious Claim 1, as discussed above. EX1003, ¶190. As discussed in Section VIII.B., a POSITA would have been aware that similar language is commonly used to describe a driver that may have many but not all components integrated as packages.[12] *See* Section VIII.B; EX1003, ¶190.

Zane discloses that its "digital architectures for driving large LED arrays" is FPGA-based. EX1006, Abstract, 293 ("Experimental results are presented for a 15 W boost converter with ***FPGA based digital control driving a 64 LED array with 8 LED strings***."), 291 ("Experimental setup, consisting of … digital PS-PWM and control logic ***implemented on Virtex-4 FGPA***"); EX1003, ¶190. An FPGA (field-programmable gate array) is an off-the-shelf integrated circuit that an engineer can reconfigure with programming. *Id.* Thus, *Zane* discloses the use of an FPGA as an integrated circuit for the digital control functions of the driver. EX1003, ¶190.

Zane also discloses implementing the current sinks and voltage protection as integrated circuits. EX1006, 291; EX1003, ¶191. It would have been obvious to implement the entirety of the LED driver disclosed in *Zane* as an integrated circuit. EX1003, ¶191. *Zane* discloses that various integrated solutions for LED drivers

[12] As discussed in Section VIII.B., Patent Owner has asserted in infringement contentions that Claim 13 is satisfied if the majority of the circuitry is part of the integrated circuit. *See* Section VIII.B.; EX1003, ¶190 n.9.

"with multiple current sinks for driving parallel LED strings" were already well-known and commercially available. EX1006, 287; EX1003, ¶191. As discussed above in Section VIII.B., it was standard practice in the electronics industry to fabricate circuits as integrated circuits and a POSITA would have been motivated to do so for a wide variety of applications, such as for driving the LED backlighting on displays, as confirmed by the AAPA. *See supra* Section VIII.B.; EX1003, ¶¶192-193. Accordingly, it would have been obvious to a POSITA to form the LED driver in *Zane* as an integrated circuit. EX1003, ¶194. Claim 13 would have been obvious over *Zane*.

D. Claim 15– "The method of claim 14 further comprising varying the duty cycle of the staggered PWM brightness control signals to change an average current through the parallel paths of LEDs to change a perceived brightness of the LEDs."

Zane anticipates and/or renders obvious Claim 14, as discussed above. EX1003, ¶195. *Zane* discloses varying the duty cycle of the PS-PWM to change the perceived brightness of the LEDs. *Id.*; EX1006, Figs. 5-6, 8a-8b (showing PWM waveforms at various duty cycles), 291 ("An external dimming command, received by the PS-PWM module, is used to determine the appropriate phase-shift and duty cycle of individual control output signals.").

Zane does not explicitly discuss how varying the duty cycle would change the average current through the parallel paths of LEDs, but a POSITA would understand that this is fundamentally what PWM does to the current. EX1003, ¶196. As

discussed in Section VIII.C., the purpose of driving LEDs using PWM is to be able to dim the brightness of the LED by applying a fixed current and rapidly turning the LEDs on and off according to a duty cycle. *See* Section VIII.C.; EX1003, ¶196. A duty cycle of X% means that the LEDs are on X% of the time, meaning that the average current through the LEDs is X% of the fixed current. *Id.* Thus, a POSITA would understand that varying the duty cycle of a PWM signal changes the average current through the parallel path of LEDs. *Id.*; *see also* EX1001, 2:7-18 (AAPA describing PWM is used to change the average current flowing through the LEDs).

To the extent *Zane* does not expressly disclose changing the average current, it would have been obvious to a POSITA based on *Zane* and their knowledge of the art that dimming an LED with PWM is effectively changing the average current through the LEDs. EX1003, ¶197. Claim 15 would have been obvious over *Zane*.

E. Claim 16

1. Preamble [16.pre] – "The method of claim 14"

Zane anticipates and/or renders obvious Claim 14, as discussed above. EX1003, ¶198.

2. Limitation [16.a] – "wherein setting a peak current through one or more LEDs connected in each of the parallel paths comprises setting the peak current by controlling conductivity of a current control transistor in series with each parallel path, and"

As discussed above for Limitations [1.b] and [1.d] above, *Zane* discloses a plurality of current set circuits each setting a peak current flowing through their

respective string of LEDs. *See supra* Sections X.A.3., X.A.5; EX1003, ¶199. As also discussed above for Limitations [4.a] and [4.b], *Zane* discloses that each current set circuit further comprises a current control transistor *Q* in series with the LEDs in the respective string and a feedback circuit controlling the conductivity of the transistor *Q* to regulate the current through the LEDs. *See supra* Sections X.D.2.-3. EX1003, ¶199.

3. Limitation [16.b] – "wherein applying a different staggered PWM brightness control signal to each current set circuit comprises: coupling each staggered PWM brightness control signal to a control terminal of an associated pass transistor, each pass transistor being connected between a control terminal of a respective current control transistor and a regulating control voltage, such that the current control transistor is turned on and off corresponding to a duty cycle of the associated pass transistor."

As discussed for Limitations [5.a] and [5.b], *Zane* discloses an SPDT switch which a POSITA would have implemented with a transistor and which is connected to the PS-PWM output. *See supra* Sections XI.B.2.-3; EX1003, ¶200. Claim 16 uses the term "pass transistor" instead of "PWM brightness control transistor," as in Claim 5. EX1003, ¶200. The SPDT switch identified for Limitations [5.a] and [5.b] is the "pass transistor" for Limitation [16.b]. EX1003, ¶200; *see also* EX1001, 6:3-4 (explaining that the "pass transistor" is controlled by the PWM brightness control signal).

As discussed for Limitation [5.a], it would have been obvious to move the SPDT switch from the noninverting input of the op amp to between the op amp output and the control terminal of the current control transistor *Q*. *See supra* Section XI.B.2; EX1003, ¶201. As modified, the SPDT switch is between the control terminal of *Q* and a regulating control voltage, V_{prog}. *Id.* Additionally, when the SPDT switch is activated on and off based on the PWM signal applied to it, it will also turn on and off the current control transistor *Q* at the same duty cycle associated with the SPDT switch. *Id.* at ¶202. Accordingly, Claim 16 would have been obvious over *Zane*. *Id.* at ¶203.

XII. THE BOARD SHOULD NOT EXERCISE DISCRETION TO DENY INSTITUTION

A. Board Should Not Deny Institution Pursuant to 35 U.S.C. § 325(d)

The Board should not deny institution under *Advanced Bionics* because the prior art cited in this Petition was not previously considered by the Examiner and is not substantially similar to any references considered during prosecution of the '148 Patent. *See Advanced Bionics, LLC v. Med-EL Elektromedizinische Gerate GmbH*, IPR2019-01469, Paper 6 at 8 (Feb. 13, 2020) (precedential). The Examiner issued a first-action allowance, reasoning that "[n]one of the prior art teaches or fairly suggests" an LED driver where "the plurality of current set circuits conduct current through their associated one or more LEDs at the same duty cycle but out of phase with each other." EX1002, 52-53. As discussed above, Thomas and *Zane* both show

LED drivers that drive LEDs with PWM signals at the same duty cycle but out of phase with each other.

B. Board Should Not Decline Institution Pursuant to 35 U.S.C. § 314(a)

The Board should not deny institution under *General Plastic* because this is the first IPR petition filed against the '148 Patent and not a follow-on. *See Gen. Plastic Indus. Co v. Canon Kabushiki Kaisha*, IPR2016-01357, Paper 19 (Sept. 6, 2017) (precedential).

Additionally, the *Fintiv* factors weigh in favor of institution. The parties are involved in a parallel litigation involving the '148 Patent before Judge George Wu in the Central District of California. *See infra* Section XIII.A. Judge Wu has granted motions to stay pending IPRs. *See* EX1022-EX1025 (orders from prior cases). The parallel litigation is also in its infancy and the parties have not yet invested substantial resources in that matter. For example, document production has been minimal. No deposition notices have been served. The parties have not responded to interrogatories or identified any disputed terms for claim construction. No trial date has been set. Finally, this Petition presents compelling unpatentability challenges for the '148 Patent claims. Thus, the Board should institute this IPR.

XIII. MANDATORY NOTICES, GROUNDS FOR STANDING, AND FEE PAYMENT

A. Real Party-In-Interest & Related Matters (37 C.F.R. § 42.8(b)(1)-(2))

VIZIO, Inc. is the real party-in-interest for Petitioner.

Petitioner and Patent Owner are presently engaged in a district court litigation captioned *Polaris PowerLED Technologies, LLC v. VIZIO, Inc. et al.*, No. 2:23-cv-03478 (C.D. Cal.) (the "Litigation"). Patent Owner filed the complaint in the Litigation on May 8, 2023 and served a copy of the complaint on Petitioner on May 10, 2023.

In the Litigation, Polaris has asserted the '148 Patent against Petitioner and the additional defendants listed below (collectively, "Other Defendants"):

- Hon Hai Precision Industry Co., Ltd. d/b/a Foxconn Technology Group,
- Competition Team Technology USA Inc.,
- Top Victory Electronics (Taiwan) Co. Ltd.,
- Top Victory Investments Ltd.,
- TPV Technology Ltd.,
- TPV International (USA), Inc.,
- Trend Smart America, Ltd.,
- Innolux Corp.,
- Innolux USA, Inc.,
- Amtran Technology Co., Ltd.,
- Amtran Logistics, Inc.,
- Newegg, Inc.

The Other Defendants listed above may have a financial interest in or could be substantially affected by the outcome of this proceeding. The Other Defendants did not and could not exercise control over this Petition, did not contribute any funds to the preparation of this Petition or its attendant exhibits, and did not cooperate in any manner with Petitioner regarding this Petition. Accordingly, the Other Defendants are not real parties-in-interest. Additionally, none of the Other Defendants were served in a prior complaint alleging infringement of the '148 Patent. *See SharkNinja Operating LLC v. iRobot Corp.*, IPR2020-00734, Paper 11 (Oct. 6, 2020) (precedential) (no RPI analysis necessary absent allegation of time bar or estoppel based on unnamed RPI). The above-referenced litigation is the first lawsuit alleging infringement of the '148 Patent.

B. Lead and Backup Counsel (37 C.F.R. § 42.8(b)(3))

Petitioner provides the following designation of counsel, all of whom are included in Customer No. 20,995 identified in Petitioner's Power of Attorney.

Lead Counsel	Back-up Counsel
Sheila N. Swaroop (Reg. No. 53,658) Knobbe, Martens, Olson, & Bear, LLP 2sns@kmob.com Postal & Hand-Delivery Address: 2040 Main St., 14th Floor Irvine, CA 92614 Telephone: (949) 760-0404 Facsimile: (949) 760-9502	Marko R. Zoretic (Reg. No. 65,994) Knobbe, Martens, Olson, & Bear, LLP 2mrz@knobbe.com Postal & Hand-Delivery Address: 2040 Main St., 14th Floor Irvine, CA 92614 Telephone: (949) 760-0404 Facsimile: (949) 760-9502

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C. Service Information (37 C.F.R. § 42.8(b)(4))

Please direct all correspondence to lead counsel and back-up counsel at the addresses shown above. Petitioner also consents to electronic service by email to VIZIO-148IPR@knobbe.com.

D. Grounds for Standing (37 C.F.R. § 42.104)

Petitioner certifies that the ’148 Patent is available for IPR and Petitioner is not barred or estopped from requesting IPR.

E. Payment of Fees (37 C.F.R. § 42.15(a))

The Office may charge the § 42.15(a) fee to Deposit Account No. 11-1410. Review of 22 claims is requested. Payment for any additional fees due may be charged to the above-referenced Deposit Account.

XIV. CONCLUSION

Petitioner respectfully requests that the Board institute an IPR and find Claims 1-22 of the ’148 Patent unpatentable.

Dated: October 20, 2023

By: /Sheila N. Swaroop/

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CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. §§ 42.24(a) and (d), the undersigned certifies that this PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 7,843,148 contains 13,783 words according to the word-processing program used to prepare this paper. The foregoing word count complies with the 14,000 word type-volume limit specified by 37 C.F.R. § 42.24(a)(1). Pursuant to § 42.24(a)(1), the word count does not include the table of contents, table of authorities, mandatory notices under § 42.8, certificate of service or word count, or appendix of exhibits or claim listing.

Dated: October 20, 2023 By: / Sheila N. Swaroop/
KNOBBE MARTENS OLSON & BEAR, LLP

CERTIFICATE OF SERVICE

The undersigned hereby certifies that on the date below a copy of this PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 7,843,148, PETITIONER'S POWER OF ATTORNEY, AND EXHIBITS 1001-1028, were served by FedEx on the Patent Owner at the correspondence address of record for the subject patent as follows:

32566 - PATENT LAW GROUP

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