

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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VIZIO, INC.,  
Petitioner

v.

POLARIS POWERLED TECHNOLOGIES, LLC,  
Patent Owner

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Case IPR2024-00073  
U.S. Patent No. 7,843,148

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**DECLARATION OF THOMAS L. CREDELLE**

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P.O. Box 1450  
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Polaris EX2002  
Vizio v. Polaris  
IPR2024-00073

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I, Thomas L. Credelle, declare under penalty of perjury as follows:

**I. INTRODUCTION AND BACKGROUND**

1. I have been retained as an expert witness by Polaris PowerLED Technologies, LLC (“Polaris”) and have been asked to provide my expert opinions regarding U.S. Patent No. 7,843,148 (the “’148 patent”) and the prior art asserted against the ’148 patent in this *inter partes* review.

2. In this declaration I provide my independent analysis of the ’148 patent and the prior art in light of my knowledge and experience in this field during the relevant time frame. I have been asked to consider what one of ordinary skill in the art at the time of the invention of the ’148 patent (a “POSITA”; refer to Section IV below) would have understood from the specification, including scientific and technical knowledge related to the patent. I have also been asked to consider whether certain references disclose or render obvious the inventions recited by claims 1-22 of the ’148 patent.

3. My findings, as explained below, are based on my study, experience, and background in the fields discussed below, informed by my education in electrical engineering. I have also relied on my review and analysis of the prior art, information provided to me, and information that I have independently reviewed.

4. I am being compensated for my independent analysis as an expert with respect to this *inter partes* review proceeding at my standard hourly rate of

\$500/hour but my compensation is not contingent in any way on the content of my analysis or the outcome of this proceeding. I have no financial interest in Petitioner (VIZIO, Inc.) or Patent Owner (Polaris), and I have no financial interest in the challenged patent or this proceeding.

## II. QUALIFICATIONS

5. Details of my professional qualifications and background are set out in my *curriculum vitae* (EX2003). As shown in my *curriculum vitae*, I have devoted my career to the research and development and product engineering of flat panel displays and materials/optics/electronics for flat panel displays. I have over 20 years of involvement in flat panel display technology including active-matrix LCD R&D, starting in 1983 at RCA Labs and continuing at GE. I led the product development of active-matrix LCDs for notebook computers at Apple in the early 1990s and had close collaboration with many LCD developers in Asia. Later in my career, while at Clairvoyante, I made significant contributions to the design and implementation of new pixel architectures for LCDs and OLEDs; both efforts involved Thin Film Transistor (“TFT”) design modifications to achieve the desired goals of high pixel transmission and reduced circuit complexity. More recently, I have been involved in several patent litigation cases which required a detailed knowledge of TFT design and processing.

6. I am currently the President of TLC Display Consulting and have split my time between technical consulting and patent litigation support.

7. I received my M.S. degree in Electrical Engineering from the Massachusetts Institute of Technology in 1970, with an emphasis on Electro Optics and Solid-State Materials. I received my B.S. degree in Electrical Engineering in 1969 from Drexel University.

8. I was employed by RCA at Sarnoff Labs in Princeton, NJ, from 1970 through 1986 at first as a Member of the Technical Staff and later as a Group Manager in charge of all Active Matrix LCD research. During my time at RCA, I participated in research and development projects relating to optical materials and flat panel displays, including LCD devices. In 1983, I established the Thin Film Transistor (“TFT”) LCD Program at Sarnoff Labs. As a Group Manager, I led a project that resulted in the development of the first poly silicon TFT LCD at Sarnoff Labs. I received the Sarnoff Outstanding Achievement Award for Large Area Flat Panel TV Developments.

9. From 1986 to 1991, I was employed by GE as the Manager of TFT LCD Research and Development at the GE Research and Development Center in Schenectady, NY. My duties included contributing to and managing research and development efforts relating to TFT and LCD technology for avionics applications. While employed by GE, I led the team that built the world’s first 1-million-pixel

color LCD device. I also led the development of numerous other display devices utilizing LCD technology.

10. From 1991 to 1994, I was employed by Apple Computer as the Manager of Display Engineering. In my role at Apple, I supervised all TFT-LCD design (in-house and at vendors), engineering, and qualification for the first PowerBook notebook computers introduced to market in the United States. A key part of my effort was the evaluation and development of active matrix LCDs with improved performance, such as viewing angle, contrast ratio and uniformity and backlight control.

11. From 1996 to 1999, I was employed as the Director of Product Marketing for Motorola's Flat Panel Display Division, where I worked in the development of new flat panel technology, and I also worked closely with Motorola groups responsible for integrating TFT-LCD technology into mobile phone products.

12. From 1999 to 2001, I served as the Vice President of Operations of Alien Technology Corporation. During my time at Alien Technology, I was involved with the design and architecture of drive electronics packaging technology suitable for flexible LCD devices.

13. From 2001 to 2007, I served as the Vice President of Engineering for Clairvoyante, Inc. My responsibilities as the VP of Engineering included managing

research, development, engineering, and marketing of technologies for improving the resolution and power consumption of color flat panel displays, which required significant changes to the TFT-LCD layout and LED backlight. During my time at Clairvoyante, I was therefore heavily involved with the design of the active-matrix array and the LCD driving circuitry. My work resulted in the issuance of multiple patents relating to TFT-LCD and TFT-OLED display technology.

14. From 2007 to 2008, I served as the Senior VP of Engineering for Puredepth, Inc. My responsibilities included the design of hardware and software to create 3D images on TFT-LCDs. Hardware included a high-brightness, high power LED backlight source that had to survive in slot machines 24/7. LED backlight controllers were an important part of this development work.

15. From 2008 to 2012, I served as VP Engineering at Display Engineering, a company founded to design and sell high-brightness LED-LCDs for outdoor use. Commercial LCD displays were converted to high brightness through a complete redesign of the LED backlight, LED driving circuits, and LED cooling. LED controllers were selected based on the requirements of the newly engineered LED backlights, which were based on strings of LEDs.

16. From 2012 through 2015, I served as the Vice President of Application Engineering and Device Performance for Innova Dynamics, Inc., a nanotechnology company developing materials to be used in LCDs and touch

sensors. In 2008, I founded TLC Display Consulting, a company that provides technical consulting in the areas of flat panel displays, liquid crystal displays, and related electronics. I currently serve as the President of TLC Display Consulting.

17. I have been an active member of the Society for Information Display (“SID”) for over 40 years, having attended every SID Annual Technical Symposium since 1972. I was a member of the Society for Information Display’s Program Committee for 15 years, and the Director of the Society for Information Display’s Symposium Committee for 10 years. In 1984, I was awarded the title of Fellow of the Society for Information Display in recognition of my achievements and contributions to flat panel display technology.

18. I am a named inventor on over 80 U.S. patents relating to flat panel display and LCD technology. I have also authored several articles relating to LCD technology and flat panel displays that were published by industry periodicals such as Information Display and peer reviewed journals such as the Society for Information Display’s Digest of Technical Papers.

19. Because of my background, training, and experience, I am qualified as an expert in the technical areas relevant to the ’148 patent.

### **III. MATERIALS CONSIDERED**

20. In preparing this declaration, I have considered the claims, specification, and prosecution history of the ’148 patent. As part of my analysis for

this Declaration, I have considered my own knowledge and experience, including my work and experience with electrical engineering and computer science in the context of both analog (hardware) and digital (hardware and software) devices. Additional materials that I have reviewed in preparing this declaration include the Petition for *Inter Partes* Review filed by Petitioner VIZIO, Inc. (Paper 1), as well as each of the exhibits to that Petition, several of which I discuss in detail below. In addition, I have also reviewed the relevant district court claim construction orders.

#### **IV. PERSON OF ORDINARY SKILL IN THE ART (“POSITA”)**

21. I understand that the teaching of the prior art is viewed through the eyes of a POSITA. Counsel for Polaris has informed me that a person of ordinary skill in the art is a hypothetical person who is presumed to have known the relevant art at the time of the invention. I have also been informed by counsel for Polaris that the person of ordinary skill is generally familiar with the type of problems encountered in the field and the prior art solutions to those problems and possesses an ordinary level of creativity.

22. I understand from my review of both the Petition and Dr. Zane’s declaration that it is Petitioner’s position that a POSITA allegedly “would have had at least a bachelor’s degree in physics, electrical engineering, or a related field, and approximately two years of experience in the fields of LED technology, backlights, LED devices and control thereof, or other related fields” and that “advanced

education in the fields of physics, electrical engineering, or a related field can compensate for lesser work experience in the relevant fields.” Pet., 16; EX1003, ¶¶34-35. For the purposes of my opinions in this declaration, I applied Petitioner’s and Dr. Zane’s definition of a POSITA.

## **V. CLAIM CONSTRUCTION**

23. It is my opinion that none of the terms of the ’148 patent require explicit construction by the Board in order to resolve the issues presented in the Petition. In forming the opinions provided herein, I have applied the plain and ordinary meaning of each claim term as it would have been understood by a POSITA.

## **VI. BACKGROUND OF THE ’148 PATENT**

24. Entitled “Driving Multiple Parallel LEDs With Reduced Power Supply Ripple,” the ’148 patent issued on November 30, 2010, to inventors Christian Gater and Roel Van Ettinger from U.S. Patent Application No. 12/099,729, filed on April 8, 2008. EX1001, Cover. The inventors disclosed a novel LED driver for driving LEDs connected in parallel paths that operates, in part, by staggering pulse width modulated (“PWM”) brightness control signals to LEDs to produce less ripple by the power supply. As a result, this “reduces noise, eases the constraints on the power supply, improves the color output of the LEDs,

reduces artifacts caused by lights flickering, and provides other benefits.” EX1001,

4:9-12. Claim 1, which is representative, is shown as follows:

1. A light emitting diode (LED) driver for driving LEDs connected to different parallel paths, the driver comprising:

a voltage source for connection to first ends of LEDs in a plurality of parallel paths;

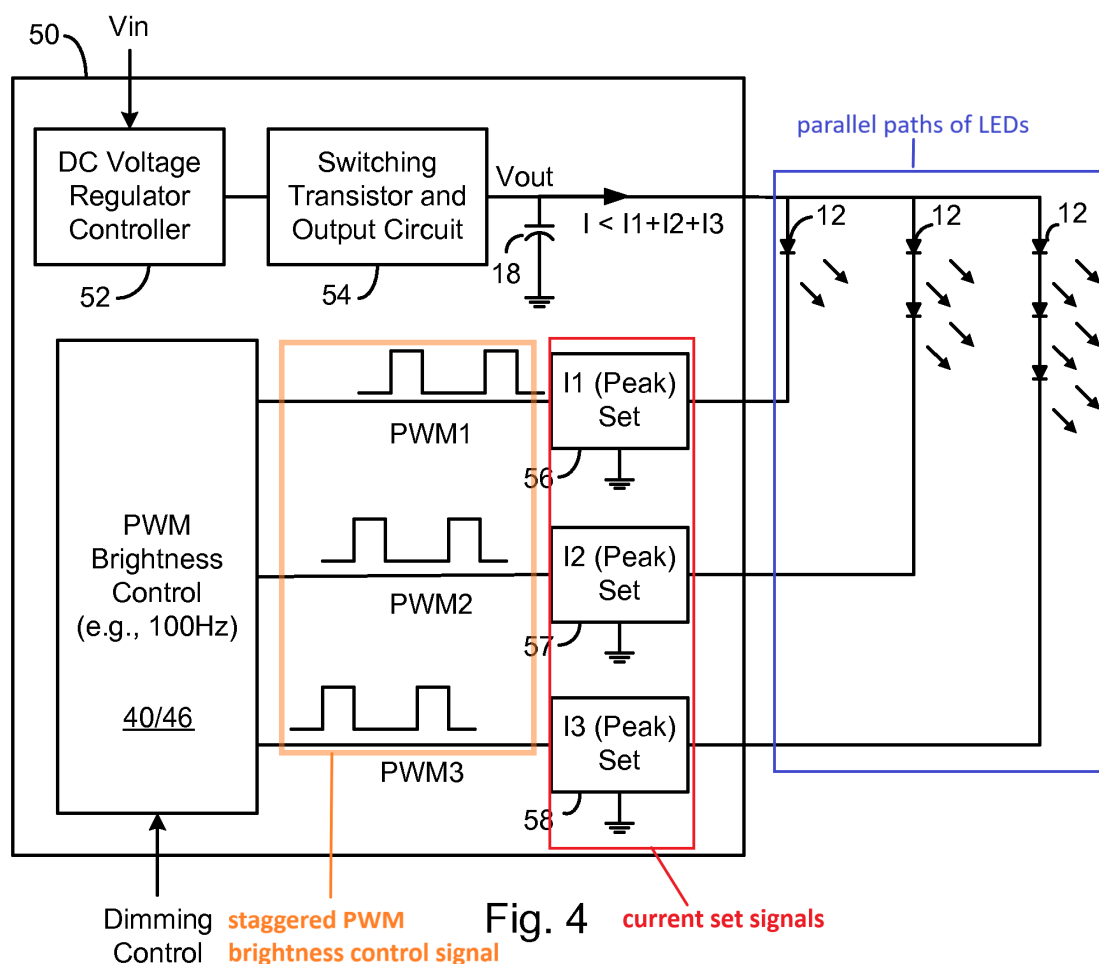
a plurality of current set circuits, one current set circuit per parallel path, each current set circuit controlling a peak current through one or more LEDs connected in each parallel path; and

a pulse-width modulated (PWM) brightness control signal generator connected to the plurality of current set circuits, the brightness control signal generator being configured to generate staggered PWM brightness control signals to the plurality of current set circuits,

each current set circuit being configured to draw the peak current through its associated one or more LEDs at a duty cycle substantially corresponding to a duty cycle of a PWM brightness control signal applied to it, such that the plurality of current set circuits conduct current through their associated one or more LEDs at the same duty cycle but out of phase with each other.

EX1001, 6:35-54.

25. The '148 patent describes several embodiments of the invention, including the embodiment shown below in Figure 4.



EX1001, FIG. 4 (annotated).

26. Figure 4 of the '148 patent illustrates a LED driver [block 50].

EX1001, 5:12-57. The LEDs [arrows at 12] are connected in parallel paths.

EX1001, 5:12-57. The DC voltage regulator controller [block 52] generates an output voltage (Vout) that exceeds the forward voltage drop for each parallel path of LEDs to turn on the LEDs. EX1001, 5:12-57. As explained in the specification, “[t]he voltage regulator controller 52 generates high frequency (e.g., 1 MHz) PWM signals that turn the switching transistor on and off, where the duty cycle controls

the level of  $V_{out}$ . An inductor and diode (in block 54) connected to the switching transistor apply ramping currents to the smoothing capacitor 18, which supplies a relatively constant output voltage ( $V_{out}$ ).” EX1001, 5:31-37. “All LED paths are energized with the same voltage but may draw different currents, set by the current set circuits 56, 57, and 58. The current set circuits 56-58 are effectively enabled and disabled by their associated staggered PWM brightness control signal PWM1, PWM2, or PWM3. There may be any number of current set circuits, each driven by a staggered PWM signal. The PWM brightness control unit 40/46 may be either of the shift registers 40 or 46 in FIGS. 2A and 2B, or may be any other circuit that operates to stagger a PWM signal, such as a delay line.” EX1001, 5:48-57.

27. The '148 patent discloses certain examples of how staggered PWM brightness control signals may be generated, for example, as illustrated in Figures 2A, 2B, and 3. For example, in Figure 3 a binary bit pattern is “continuously and serially loaded into the first bit position of the shift register 46 and then shifted by the load/shift clock. In this embodiment, there is no feeding back of any bits in the shift register, and the shift register acts as a clocked tapped delay line. The PWM brightness control signals (PWM1, PWM2, PWM3) for each parallel path of LEDs are tapped from different positions along the shift register 46 so that the PWM brightness control signals are identical but staggered, as shown in FIG. 2B.”

EX1001, 5:1-11. One implementation of the bit shifting functionality in the PWM

brightness control to generate such staggering of PWM signals is shown below in Figure 3.

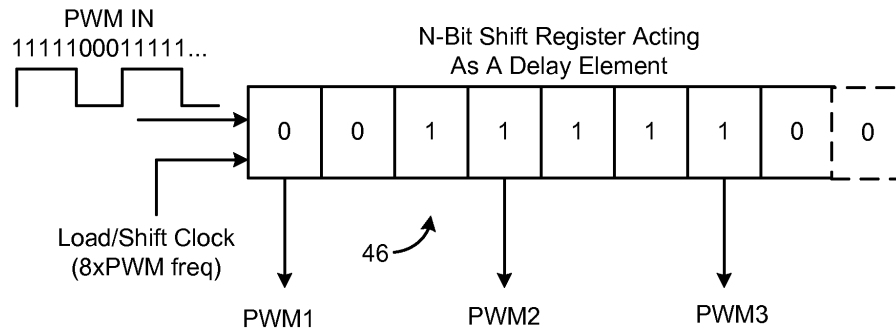


Fig. 3

EX1001, FIG. 3.

28. Ultimately, the benefits of the invention include the following: “[i]n addition to there being less power supply output voltage ripple by staggering the on-times of the different parallel paths of LEDs, there is less overall flickering of the light, since there is a shorter time (or even no time) that all the LEDs are off at the same time, compared to the prior art techniques. This is advantageous in certain situations and reduces eye fatigue.” EX1001, 6:17-23.

## VII. PRIOR ART

### A. Summary of U.S. Patent No. 5,317,307 (EX1005, “Thomas”)

29. Thomas discloses a method and apparatus that controls a plurality of LEDs using pulse width modulation. EX1005, Abstract. The PWM signal is

delayed such that four LED strings are energized sequentially with only one group of LEDs energized at a time. EX1005, Abstract.

30. Thomas discloses a control circuit shown in Figures 1 and 2 that provide modulating signals E through H that are phased using a shift register. EX1005, 3:64-4:16. Each modulating signal, and respective control signal (W through Z), is provided to gating AND logic 32 that enables LEDs to turn on; when the system bus 1 sends a high signal to the AND logic when control signal E-F are high, the LEDs will turn on. EX1005, 3:24-45. To control the intensity of the LEDs within the array, Thomas provides a PWM signal to the AND gates such that LEDs 9-12 will not turn on at the same time. EX1005, 4:66-5:10.

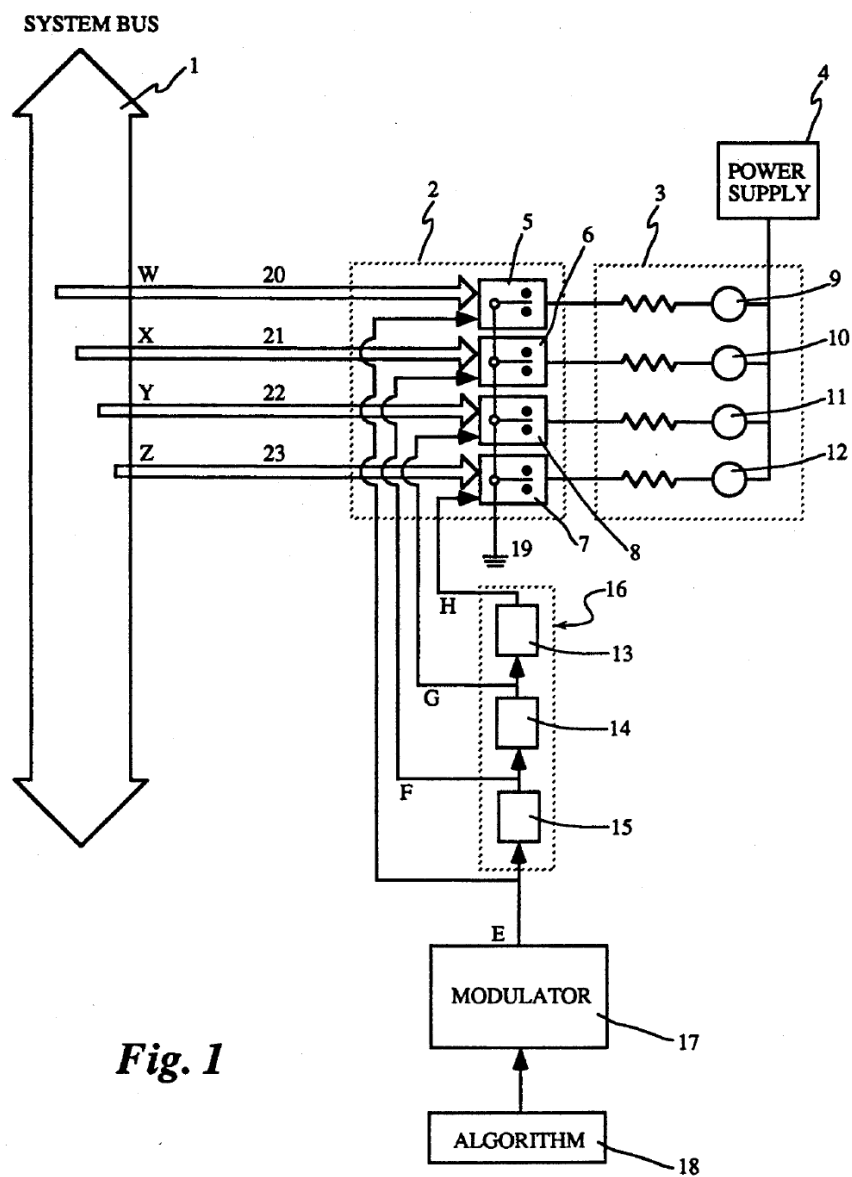


**Fig. 1**

EX1005, FIG. 1.

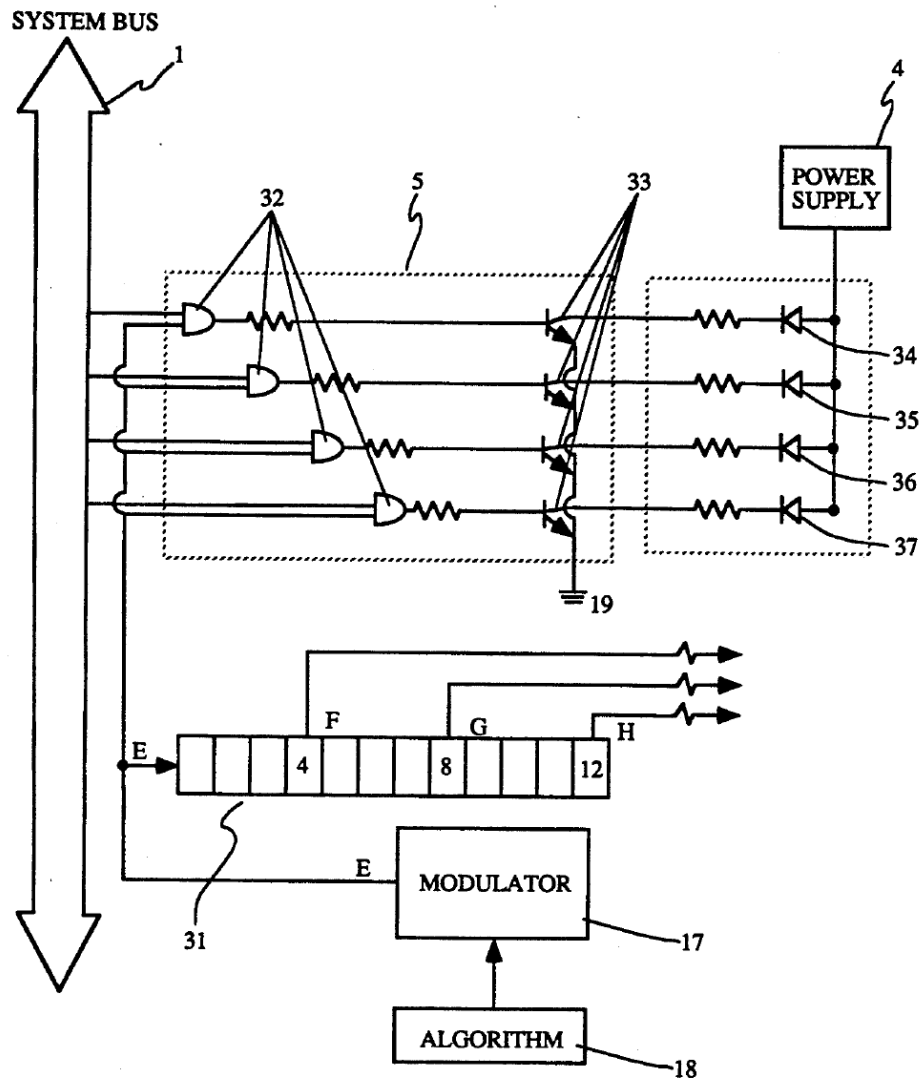


**Fig. 2**

EX1005, FIG. 2.

31. Each LED 34-37 in a group of LEDs 9 is connected to driving transistors 33 through respective resistors. EX1005, 3:32-35. The resistors, seen in Thomas's Figure 2 between driving transistors 33 and LEDs 34-37, are unlabeled and not further described. A POSITA would understand these resistors to be

passive resistors. The gates of driving transistors 33 are controlled by the output of the AND gates 32. EX1005, 3:39-42. A power supply 4 “provides current” to activate the individual LEDs in each group 9-12. EX1005, 3:42-45. The unidentified resistors shown in Figure 2 may limit the current flowing in the individual LEDs, but since the number of LEDs and their current voltage characteristics are unknown and the power supply voltage is unknown, the unidentified resistors would not set the current in the LEDs. This is because establishing a set current requires knowledge of the power supply output, the number of LEDs, the type of LEDs, and the properties of any other circuit elements e.g. control transistors between the power supply and ground.

**B. Summary of *Digital Architecture for Driving Large LED Arrays with Dynamic Bus Voltage Regulation and Phase Shifted PWM* (EX1006, “Zane”)**

32. *Zane* relates to “a digital architecture suitable for driving a large number of High Brightness Light Emitting Diodes (HB-LEDs).” EX1006, Abstract. *Zane*’s “proposed architecture . . . consists of a power converter driving multiple strings of LEDs, controlled current sources, digital multiphase modulator block, threshold detector circuit to sense the voltage drop across each string and digital control logic.” EX1006, 288.

33. A phase shifted pulse width modulator (PS-PWM) “controls the switching sequence and duty cycle of individual current sources.” EX1006, 288. “Dynamic

bus voltage regulation is used to improve efficiency by maintaining the bus voltage at the minimum value required to keep all active LED strings in regulation.”

EX1006, 289. “A single comparator is used for each LED string, which compares the voltage across the current sink devices to a known threshold limit. For any voltage greater than the threshold, the current sink maintains a near constant output current.” EX1006, 289. Further, “a linear programmable current sink is used to regulate the LED forward current to a desired level.” EX1006, 290.

## **VIII. ANALYSIS**

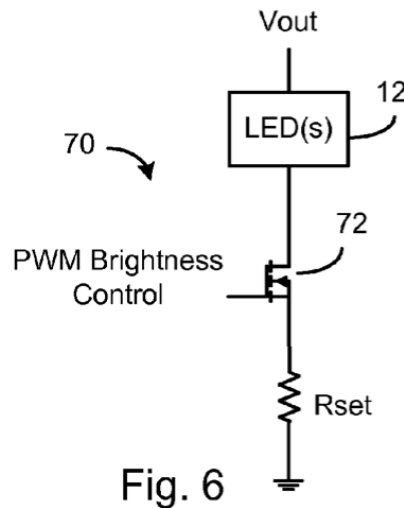
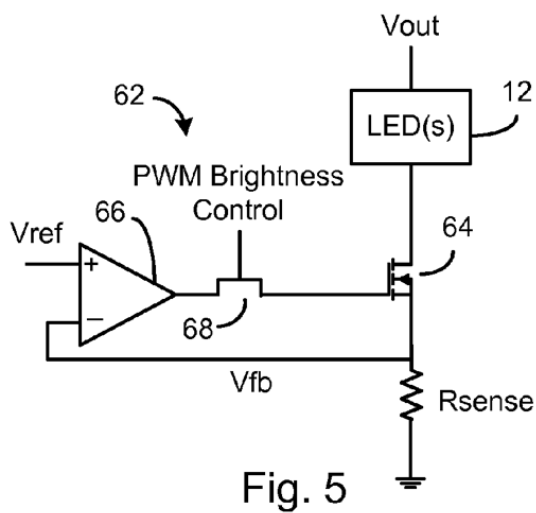
### **A. Alleged Anticipation By Thomas**

#### **1. “a plurality of current set circuits” – Claim Elements [1.b], [14.b]**

34. The Petition and Dr. Zane allege that elements [1.b] and [14.b] of independent claims 1 and 14, which recite a “plurality of current set circuits” are met by the individual passive resistors in Thomas. Pet., 25-26; EX1003, ¶¶62-63. I disagree. In my opinion, a POSITA would consider a “circuit” to require multiple components that are connected by a conductive material, such as a wire or trace on a circuit board, in order to form a “circuit.” That is, a single electronic component such as a wire, resistor, diode, or capacitor could not, by itself, comprise a

“circuit.”<sup>1</sup> Neither the Petition nor Dr. Zane have identified any “current set circuits” in Thomas, because the individual resistors they identify cannot comprise “circuits.”

35. In addition, the specification of the '148 patent discloses to a POSITA that the '148 patent's “current set circuits” are not simple resistors. For example, Figures 5 and 6 of the '148 patent both depict circuits that “may serve as each of the current set circuits 56-58 in FIG. 4.” EX1001, 5:58-59, 6:7-8. These figures are reproduced below.



EX1001, FIGs. 5, 6.

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<sup>1</sup> While integrated circuits, for example, may be packaged as a single chip, they are actually a plurality of electronic components formed in a cohesive circuit for placement in a system.

36. The '148 patent describes Figure 5 as a “low value sense resistor ( $R_{sense}$ ) and MOSFET 64 [that] are connected in series with one or more LEDs . . . .” EX1001, 5:59-61. This comports with how a POSITA would understand the term “circuit,” that is, two (or more) components connected to each other that can conduct current. Similarly, Figure 6 is described as a “current set resistor  $R_{set}$  and MOSFET 72 [that] are connected in series with the one or more LEDs . . . .” EX1001, 6:9-10. Again, multiple components connected to each other are depicted as the “current set circuit,” in accordance with how a POSITA would interpret the term “circuit.”

37. In contrast, Petitioner’s and Dr. Zane’s allegations regarding Thomas center around a single resistor serving as each “current set circuit.” Pet., 26; EX1003, ¶¶62-63. It is my opinion that this is not consistent with the specification’s description of “a plurality of current set circuits,” nor is it consistent with how a POSITA would interpret the term “circuit.”

38. Furthermore, I note that the Petition emphasizes that “a POSITA would have understood from Figures 1 and 2 [of Thomas] based on the well-known functionality of resistors that these resistors are used to limit current to a peak current  $I=(V-V_{LED})/R$ .” Pet., 45. This has nothing to do with whether or not a resistor itself is a current *set circuit*, as I have explained above. Rather, this is merely a restatement of Ohm’s Law, and that a resistor in Thomas, like a resistor

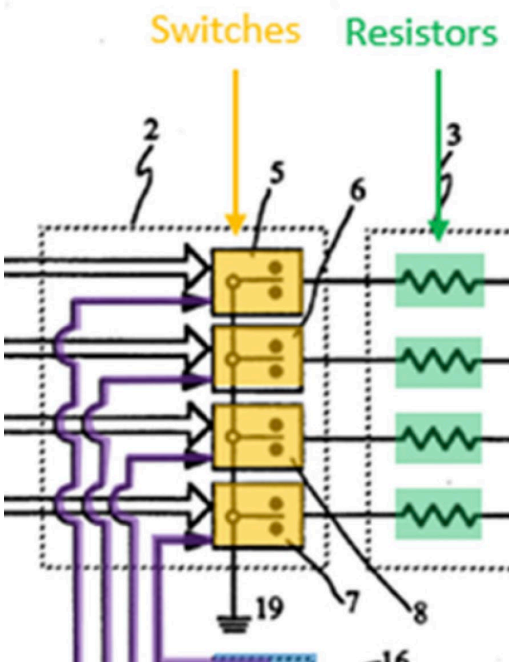
anywhere, is subject to Ohm's Law. While I do not disagree that a POSITA would understand Ohm's Law, understanding Ohm's Law would not make it obvious—or true—to a POSITA that a single resistor comprises a current set circuit. Therefore, it is my opinion that the Petition has not shown that Thomas anticipates claim 1 or 14.

**2. “each current set circuit being configured to draw the peak current through its associated one or more LEDs at a duty cycle substantially corresponding to the duty cycle of a PWM brightness control signal applied to it” – Claim Elements [1.d], [14.d]**

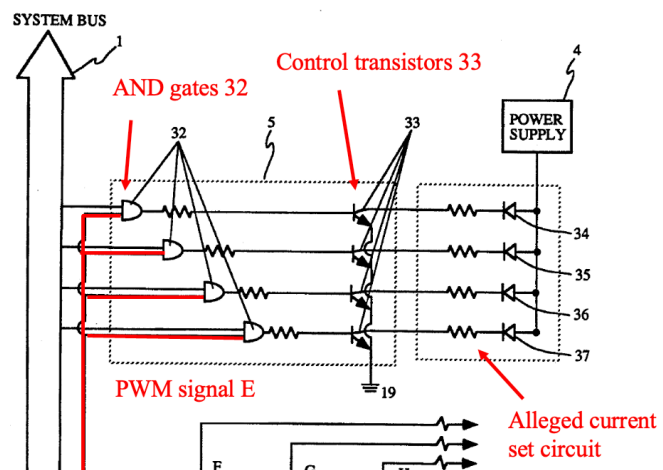
39. The Petition and Dr. Zane allege that elements [1.d] and [14.d] of independent claims 1 and 14, which recite “each current set circuit being configured to draw the peak current through its associated one or more LEDs at a duty cycle substantially corresponding to a duty cycle of a PWM brightness control signal applied to it” and “applying a different staggered PWM brightness control signals to each current set circuit,” respectively, are met by the alleged PWM brightness control signal in Thomas being applied to the switches in Thomas. Pet., 30; EX1003, ¶¶67-71. I disagree.

40. The Petition and Dr. Zane, as I discussed above, identify “each current set circuit” as being an individual passive resistor. Control of the current flow through these resistors is accomplished through a switch or AND gate (in Figure 2), to which the alleged PWM brightness control signal is applied. EX1005, 3:46-

63. In other words, the PWM signals go to the activation switches, and more specifically the gating control logic 32 thereof. EX1005, FIG. 2, 3:51-55 (“a modulating signal is supplied . . . to the gating control logic (32)”). The current that flows through the resistor is *not* the PWM brightness control signal – it is entirely separate.



EX1005, FIG. 1  
(Petitioner's annotations, excerpted).



EX1005, FIG. 2  
(annotated, excerpted).

41. As shown in the above excerpts from Figures 1 and 2 of Thomas, the PWM signal Petitioner has identified as the alleged PWM brightness control signal is not ever applied to the resistors the Petition identifies as “each current set circuit.” Rather, the PWM signal is *only* applied as input to the AND gates in

Figure 2, which also accept as input the control signal W from the system bus. The output of the AND gates are applied to the gates of the control transistors 33 (which are bipolar junction transistors or “BJTs”). When the BJTs are turned “on,” current flows from the power supply 4 through the LEDs 34-37 and the resistors (i.e., the alleged current set circuits) to ground 19.

42. Nor would it make sense to apply the PWM brightness control signal to the relevant resistors. In these circuits, not only does the alleged PWM brightness control signal not reach the resistors identified by Petitioner, but also the proper function of Thomas’s system depends on the signal *not* being applied to the resistors. Instead, the signal must be applied to the switches or gates in order to allow the resistor to conduct current, which are not part of Petitioner’s “current set circuit.” Because Petitioner’s alleged PWM brightness control signal is not ever applied to Petitioner’s alleged “current set circuit,” for this additional reason, it is my opinion that the Petition has not shown that Thomas anticipates claims 1 and 14.

### **3. “a current regulator” – Claim 3**

43. The Petition and Dr. Zane allege that claim 3, which recites “[t]he driver of claim 1 wherein each current set circuit is a current regulator,” is met by the same passive resistors identified with respect to claim 1. Pet., 32; EX1003, ¶73. I disagree.

44. A POSITA would not interpret the term “current regulator” to mean a passive component that has a simple, set resistance value. To a POSITA, a current regulator would be a component that has the ability to actively regulate the amount of conducted current. For example, the Comprehensive Dictionary of Electrical Engineering (Second Edition) (2005) defines a “current regulator” as “a device used to control the magnitude and phase of the current in DC, AC or other electrical variable speed drives.” EX2006, 163-164. The same dictionary defines a “regulator” as “a controller designed to maintain the state of the controlled variable at a constant value despite fluctuations in the load.” EX2006, 584.

45. A simple passive resistor, like those Petitioner has identified in Thomas, is not capable of actively regulating the current it conducts, and a POSITA would not consider a simple resistor to be a “current regulator.” Thus, it is my opinion that the Petition has not demonstrated that Thomas discloses claim 3 of the ’148 patent.

**4. “a clock connected to the shift register” – Claim 7**

46. The Petition and Dr. Zane allege that claim 7, which recites, in part, “a clock connected to the shift register for shifting the bits along the shift register,” is met because “[a]ll shift registers *must* have a clock connected to them for shifting the bits.” Pet., 34; EX1003, ¶76. The Petition does not identify an actual

clock in Thomas. *Id.* I disagree that the presence of a clock is a necessary component of a shift register.

47. In its simplest form, a shift register can be represented as an array of flip flops used to store binary data where the data can be shifted along the register in either direction. EX1011, 114. Data can be shifted serially or in parallel. EX1011, 114-118. Oftentimes, a clock is provided to shift data in a synchronous manner with a common clock line; see Figure 12.1 below. EX1011, 114.

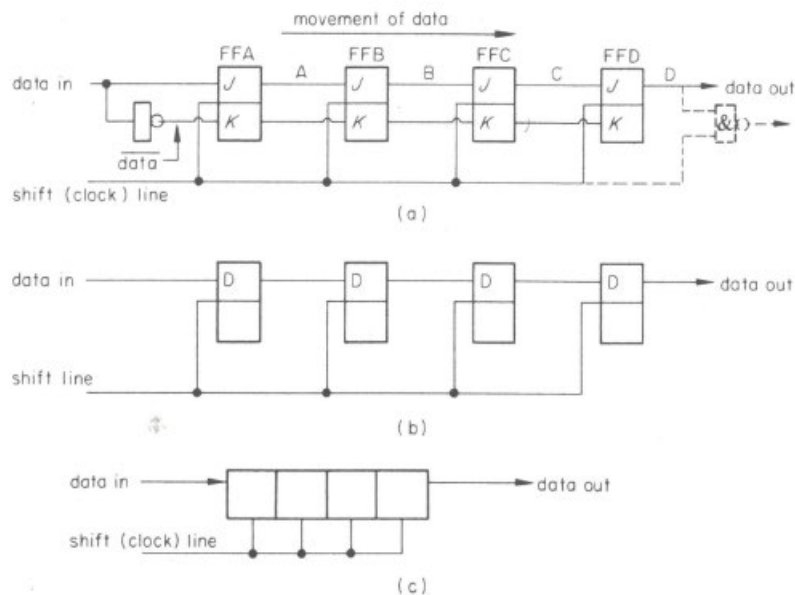


Fig. 12.1 Serial-input, serial-output shift registers

EX1011, FIG. 12.1.

48. However, shift registers can be “dynamic” and data can be shifted *asynchronously* based on the state of phased control lines; this shift register can be used in memory circuits. An example of such a dynamic shift register is shown in

Figure 12.4 of Petitioner’s Exhibit 1011, at 118, reproduced below. Data can be shifted without a clock by first setting  $\phi 1$  HIGH and then setting  $\phi 2$  HIGH.

“Hence, in a complete cycle of events  $\phi 1$  and  $\phi 2$  become logic ‘1’ in turn, and cause the input data to be . . . . *shifted to the right.*” EX1011, 118 (emphasis added). Further, “[d]uring the period of time that input data is transferred into G1, the data stored in G2 is transferred into G3. Clearly, signals  $\phi 1$  and  $\phi 2$  cause all the data stored in the register to be *shifted to the right.*” EX1011, 118 (emphasis added).

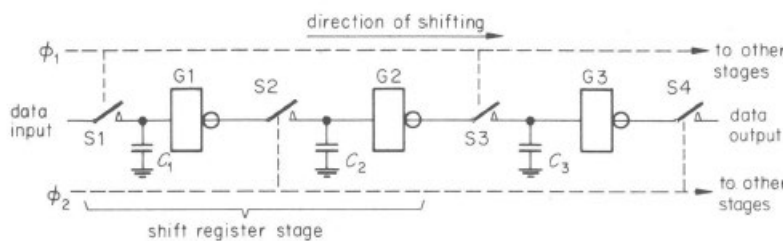


**Fig. 12.4** The basis of a MOS dynamic shift register

EX1011, FIG. 12.4.

49. A diagram of one section of a dynamic shift register is shown in Figure 12.5, reproduced below. EX1011, 118. Data in this shift register is shifted without a clock as in the simple shift register shown in Figure 12.2 from the same reference.

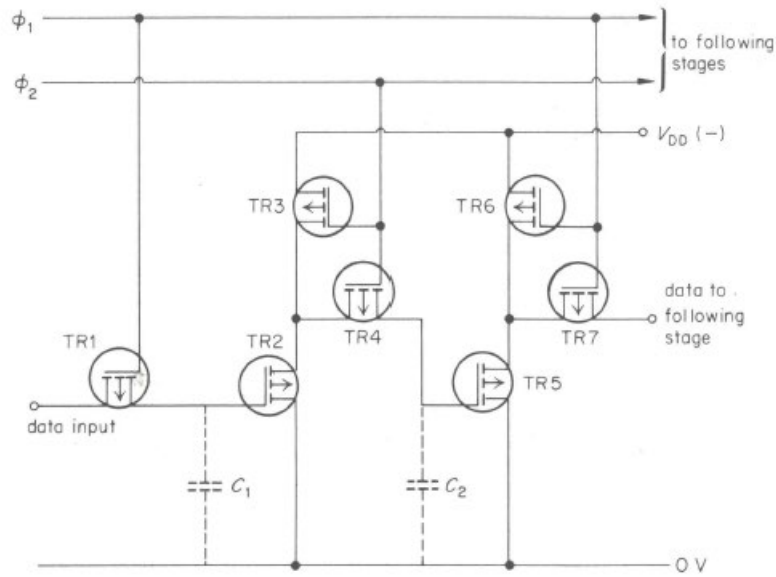


Fig. 12.5 One stage of a dynamic shift register

EX1011, FIG. 12.5.

50. Therefore, I do not agree with Petitioner's and Dr. Zane's claim that "[w]ithout a clock, a shift register would not be able to shift the bits – it would not even be considered a shift register." Pet., 35; EX1003, ¶77. As I have explained above, it is not only possible, but also readily understood that a shift register need not use a clock at all. *See, e.g.,* EX2009, 2:12-15 ("The *asynchronous device* as contrasted with the synchronous device mentioned above *does not require a clock* or timing pulse for its operation."); EX2008, 1:6-30 (describing asynchronous shift registers generally). Shift registers that do not use clocks are a well-understood electronic circuit that a POSITA would readily recognize has a variety of useful

applications, particularly in systems where direct control of the timing of the data shift is desired.

51. Because the Petition's only argument regarding claim 7 is that it necessarily *must* have a clock connected to the shift register, which is incorrect, it is my opinion that the Petition has not demonstrated that Thomas discloses claim 7 of the '148 patent.

**B. Alleged Obviousness Over *Zane***

**1. Claims 5 and 16**

52. The Petition alleges that claims 5 and 16 are obvious over *Zane*. Specifically, Petitioner and Dr. Zane allege that it would have been an obvious design choice to move components in *Zane* in order to allegedly satisfy the language of claims 5 and 16. Pet., 76-79; EX1003, ¶¶182-189. I disagree.

53. Claim 5 recites “each current set circuit further comprises a PWM brightness control transistor connected between an output of the feedback circuit and a control terminal of the current control transistor, the PWM brightness control transistor being connected to the PWM brightness control signal generator for receiving a staggered PWM brightness control signal to couple the output of the feedback circuit to the control terminal of the current control transistor at a duty cycle of the staggered PWM brightness control signal.” Claim 16 similarly reads (in part) “coupling each staggered PWM brightness control signal to a control

terminal of an associated pass transistor, each pass transistor being connected between a control terminal of a respective current control transistor and a regulating control voltage, such that the current control transistor is turned on and off corresponding to a duty cycle of the associated pass transistor.”

54. *Zane* discloses an op-amp based precision programmable current sink with AM and PWM control options in Figure 4, which I have reproduced and annotated below. EX1006, 290-91. A programmable voltage reference  $V_{\text{prog}}$  is used for amplitude modulation of LED current ( $I_{\text{LED}}=V_{\text{prog}}/R_s$ ). The precision voltage  $V_{\text{prog}}$  is applied to the op amp through an SPDT analog switch, which is connected to the PWM output, and resistor  $R_A$ . *Zane* does not disclose the properties of the analog SPDT switch or that it comprises “a PWM brightness control transistor.” Nor does *Zane* disclose the effect on the precision voltage applied to the op amp through  $R_A$  by this analog SPDT switch. EX1006, 290. A statement is simply made that the amplified output from the op amp is applied to the base of transistor Q to set the current to  $V_{\text{prog}}/R_s$ . EX1006, 290.

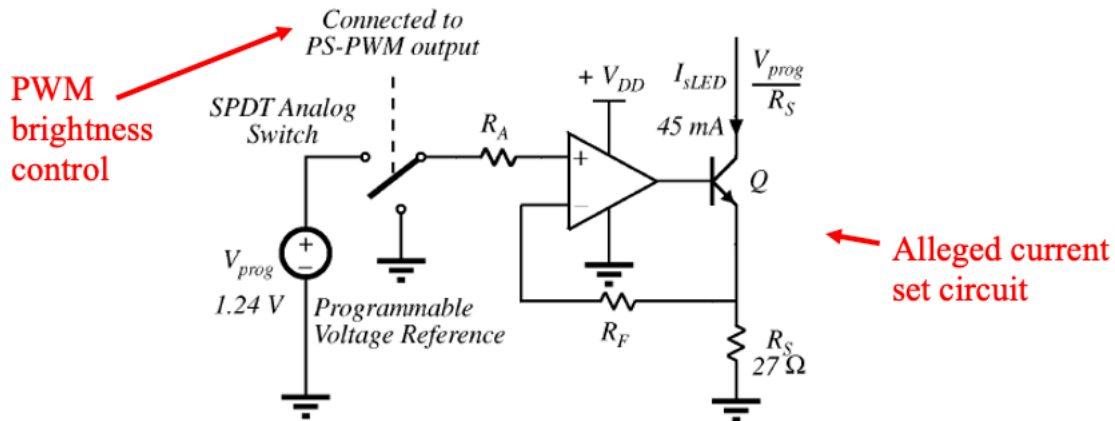
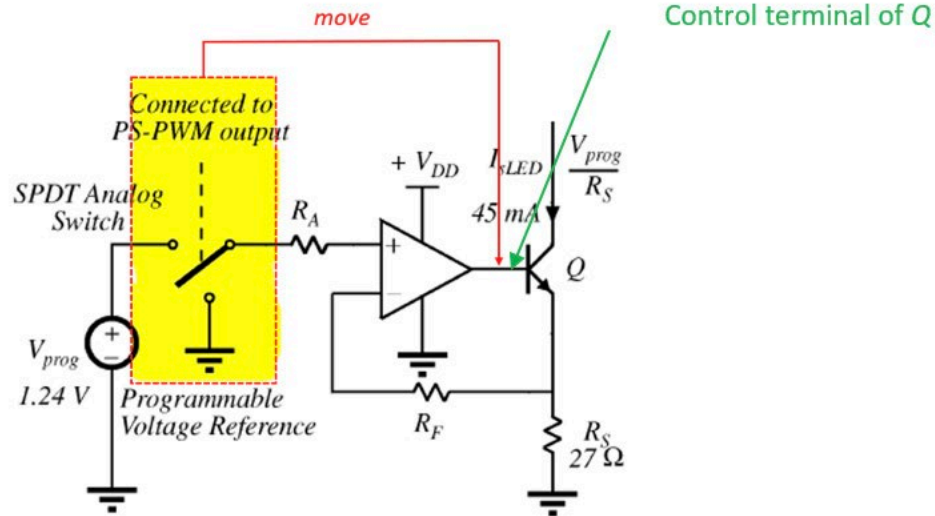


**Figure. 4.** An op-amp based precision programmable current sink with AM and PWM control options

EX1006, FIG. 4 (annotated).

55. Therefore, since *Zane* does not disclose a PWM brightness control transistor in the analog SPDT switch and the analog SPDT switch is located *before* the op amp that controls the LED current, *Zane* does not anticipate claims 5 or 16.

56. To address this deficiency, Petitioner and Dr. Zane argue that it would have been obvious to move the analog SPDT switch to a location that satisfies the claim, namely after the op amp, alleging it is one of “a finite number of identified, predictable solutions.” Pet., 78-79; EX1003, ¶¶182-186.



Pet., 78, *Zane*, FIG. 4 (Petitioner's modifications and annotations).

57. I disagree. As I have discussed above, the analog SPDT switch characteristics are not disclosed by *Zane*, but it is clear that *Zane* has designed the analog SPDT switch to apply a precision voltage to the positive terminal of the op amp to achieve a precision current flow  $V_{prog}/R_S$  in the LED strings. If the precision voltage  $V_{prog}$  is simply applied to  $R_A$ , as would occur in the modification suggested by Dr. Zane, a POSITA would not know how to adjust the op amp settings to achieve the correct voltage on the base of transistor  $Q$ . Further, if the analog SPDT switch were placed after the op amp, a POSITA would not know if the precision voltage  $V_{prog}$  would still set the LED current to the desired current because the properties of the analog SPDT switch are unknown. As such, it is my opinion that a POSITA would *not* be motivated to reorder the components in *Zane* as Petitioner suggests regarding claims 5 and 16, because it would frustrate the purpose and

function of the circuit by hampering its ability to maintain a precision voltage.

Thus, it is my opinion that the Petition has not demonstrated that *Zane* renders obvious claims 5 and 16 of the '148 patent.

## **IX. LEGAL PRINCIPLES**

58. I am not an attorney and have not been asked to offer my opinion on the law. However, I understand that I am obliged to follow existing law. I have therefore been asked to apply the following legal principles in my analysis.

59. I understand that in an *inter partes* review proceeding the party challenging the patent's validity must prove by a preponderance of the evidence that the patent claims are invalid.

60. I understand that validity based on novelty, i.e., anticipation and obviousness is governed by 35 U.S.C. §§ 102–103 (Pre-AIA) which read as follows:

### **35 U.S.C. 102 (PRE-AIA) CONDITIONS FOR PATENTABILITY; NOVELTY AND LOSS OF RIGHT TO PATENT**

A person shall be entitled to a patent unless —

- (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for patent, or
- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of the application for patent in the

United States, or

(c) he has abandoned the invention, or

(d) the invention was first patented or caused to be patented, or was the subject of an inventor's certificate, by the applicant or his legal representatives or assigns in a foreign country prior to the date of the application for patent in this country on an application for patent or inventor's certificate filed more than twelve months before the filing of the application in the United States, or

(e) the invention was described in — (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for the purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language; or

(f) he did not himself invent the subject matter sought to be patented, or

(g) (1) during the course of an interference conducted under section 135 or section 291, another inventor involved therein establishes, to the extent permitted in section 104, that before such person's invention thereof the invention was made by such other inventor and not abandoned, suppressed, or concealed, or (2) before such person's invention thereof, the invention was made in this country by another

inventor who had not abandoned, suppressed, or concealed it. In determining priority of invention under this subsection, there shall be considered not only the respective dates of conception and reduction to practice of the invention, but also the reasonable diligence of one who was first to conceive and last to reduce to practice, from a time prior to conception by the other.

35 U.S.C. § 102.

35 U.S.C. 103 Conditions for patentability; non-obvious subject matter.

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

(b)

(1) Notwithstanding subsection (a), and upon timely election by the applicant for patent to proceed under this subsection, a biotechnological process using or resulting in a composition of matter that is novel under section 102 and nonobvious under subsection (a) of this section shall be considered nonobvious if-

(A) claims to the process and the composition of matter are contained in either the same application for patent or in separate applications having the same effective filing

date; and

(B) the composition of matter, and the process at the time it was invented, were owned by the same person or subject to an obligation of assignment to the same person.

(2) A patent issued on a process under paragraph (1)-

(A) shall also contain the claims to the composition of matter used in or made by that process, or

(B) shall, if such composition of matter is claimed in another patent, be set to expire on the same date as such other patent, notwithstanding section 154.

(3) For purposes of paragraph (1), the term "biotechnological process" means-

(A) a process of genetically altering or otherwise inducing a single- or multi-celled organism to- (i) express an exogenous nucleotide sequence, (ii) inhibit, eliminate, augment, or alter expression of an endogenous nucleotide sequence, or (iii) express a specific physiological characteristic not naturally associated with said organism; (B) cell fusion procedures yielding a cell line that expresses a specific protein, such as a monoclonal antibody; and (C) a method of using a product produced by a process defined by subparagraph (A) or (B), or a combination of subparagraphs (A) and (B).

(c)

(1) Subject matter developed by another person, which qualifies

as prior art only under one or more of subsections (e), (f), and (g) of section 102, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the claimed invention was made, owned by the same person or subject to an obligation of assignment to the same person.

(2) For purposes of this subsection, subject matter developed by another person and a claimed invention shall be deemed to have been owned by the same person or subject to an obligation of assignment to the same person if —

(A) the claimed invention was made by or on behalf of parties to a joint research agreement that was in effect on or before the date the claimed invention was made;

(B) the claimed invention was made as a result of activities undertaken within the scope of the joint research agreement; and

(C) the application for patent for the claimed invention discloses or is amended to disclose the names of the parties to the joint research agreement.

(3) For purposes of paragraph (2), the term "joint research agreement" means a written contract, grant, or cooperative agreement entered into by two or more persons or entities for the performance of experimental, developmental, or research work in the field of the claimed invention.

35 U.S.C. § 103.

61. I understand that a claim is unpatentable for being anticipated (sometimes called lack of novelty) if a prior art reference disclosed, at the time of the invention, each claim element as arranged in the claim. I also understand that if a prior art reference fails to expressly disclose one or more claim elements, the claim may be anticipated if the missing element(s) are inherently disclosed. I understand that to establish inherency, the evidence must make clear that the missing claim element is necessarily present in the prior art reference. I understand that anticipation requires a high threshold because each and every claim element must be unambiguously taught by a single reference, either explicitly or inherently.

62. I understand that to be patentable, an invention must also not have been obvious to a person of ordinary skill in the pertinent art at the time the invention was made. A claim is invalid for obviousness if the differences between the subject matter sought to be patented and the prior art are such that that the claimed subject matter as a whole would have been obvious, at the time the invention was made, to a person having ordinary skill in the art to which that subject matter pertains.

63. In determining whether a claimed invention is invalid for obviousness, one should consider the scope and content of the prior art, the level of ordinary skill in the relevant art, the differences between the claimed invention and the prior art, and whether the claimed invention would have been obvious to one of ordinary

skill in the art in light of those differences. I understand that hindsight must not be used when comparing the prior art to the invention for obviousness. I understand that it is improper to stitch together an obviousness finding from discrete portions of prior art references without considering the references as a whole.

64. Obviousness may be shown by demonstrating that it would have been obvious to modify what is taught in a single piece of prior art to create the patented invention. In addition, obviousness may be shown by showing that it would have been obvious to combine the teachings of more than one item of prior art. In determining whether a piece of prior art could have been combined with other prior art or with other information within the knowledge of one of ordinary skill in the art, multiple approaches and rationales may be considered, including:

- Combining prior art elements according to known methods to yield predictable results;
- Simple substitution of one known element for another to obtain predictable results;
- Use of a known technique to improve similar devices, methods, or products in the same way;
- Applying a known technique to a known device, method, or product ready for improvement to yield predictable results;

- Applying a technique or approach that would have been “obvious to try” (choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success);
- Known work in one field of endeavor may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces if the variations would have been predictable to one of ordinary skill in the art; or
- Some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention.

65. I understand that in order for a prior art combination to render a claim obvious, the cited references must disclose each element of the challenged claim, alone or in combination. Additionally, there must have been some motivation to combine the asserted prior art, and the proposed combination would have rendered the patented claims obvious. I also understand that hindsight is inappropriate, as obviousness must be evaluated at the time of the invention. As part of my obviousness analysis, I have considered the scope and content of the prior art. I also considered whether any differences between the alleged invention and the

prior art are such that the subject matter, as a whole, would have been obvious to a POSITA.

66. It is my understanding that to demonstrate unpatentability, the burden is on the Petitioner to demonstrate that their prior art references must disclose, teach, or suggest all limitations of a given claim. To the extent that the cited references do not disclose, teach, or suggest the limitations of an independent claim, then those references also do not disclose, teach, or suggest all the limitations of any dependent claims depending therefrom.

## **X. ADDITIONAL REMARKS**

67. This declaration reflects my opinions as currently held. However, my analysis may continue such that I may consider additional information that may result in additional observations.

68. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

I declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct.

Executed on this 5<sup>th</sup> day of June, 2024, in Waco, Texas.

A handwritten signature in black ink, appearing to read "T. Credelle", written in a cursive style.

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Thomas L. Credelle