

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

VIZIO, INC.

Petitioner,

v.

POLARIS POWERLED TECHNOLOGIES, LLC

Patent Owner.

Case No. IPR2024-00073
U.S. Patent No. US 7,843,148

**DECLARATION OF REGAN ZANE, PH.D. IN SUPPORT OF
PETITIONER'S REPLY**

TABLE OF CONTENTS

Page No(s).

I.	INTRODUCTION	1
II.	INFORMATION AND MATERIALS CONSIDERED	1
III.	FOUNDATIONS 1 AND 2A-2C BASED ON THOMAS	5
	A. Thomas Discloses a Current Set Circuit (Limitations [1.b], [14.b])	5
	B. Thomas Applies a PWM Signal to the Current Set Circuit	9
	C. Thomas’s Resistor Discloses a Basic Current Regulator (Claim 3)	12
	D. Thomas’s Shift Register Necessarily Includes a Clock	13
IV.	FOUNDATIONS 3 AND 4 BASED ON <i>ZANE</i>	19
	A. Claims 5 and 16: Changing the Location of <i>Zane</i> ’s SPDT Switch Would Not Change the Overall Operation of <i>Zane</i> ’s Current Sink	19

Reply Declaration of Regan Zane, Ph.D.

I, Regan Zane, declare as follows:

I. INTRODUCTION

1. I am submitting this declaration at the request of VIZIO, Inc. in response to the Patent Owner Response and Mr. Credelle's declaration (EX2002) in this IPR proceeding.

2. I am being compensated for my work in this matter at my standard hourly rate for consulting services. My compensation in no way depends on the outcome of this proceeding.

3. My qualifications and background are discussed in my original declaration submitted as EX1003 in this IPR.

4. I have continued to apply the legal standards set forth in my original declaration.

II. INFORMATION AND MATERIALS CONSIDERED

5. I have considered the following list of materials in formulating my opinions in this matter:

Exhibit No.	Description
1001	U.S. Patent No. 7,843,148 ("the '148 Patent")
1002	File history of the '148 Patent

Reply Declaration of Regan Zane, Ph.D.

Exhibit No.	Description
1004	Regan Zane Curriculum Vitae
1005	U.S. Patent No. 5,317,307 to Thomas, Jr. (“Thomas”)
1006	Montu Doshi & Regan Zane, “Digital Architecture for Driving Large LED Arrays with Dynamic Bus Voltage Regulation and Phase Shifted PWM,” APEC 07 (“Zane”)
1007	U.S. Patent No. 6,402,354 to Tatewaki et al. (“Tatewaki”)
1008	Excerpts from Paul Horowitz & Winfield Hill, <i>The Art of Electronics</i> (2nd ed. 1989)
1009	Declaration of Rachel J. Watters re <i>The Art of Electronics</i>
1010	U.S. Patent No. 3,972,031 to Riemenschneider et al.
1011	Excerpt from Noel M. Morris, <i>Digital Electronic Circuits and Systems</i> (The Macmillan Press Ltd. 1974)
1012	UK Patent Application Publication GB 2459009A to Gater et al.
1013	PDF Printout dated October 6, 2023 of Case Details for GB2459009 from UK Intellectual Property Office website, available at https://www.ipo.gov.uk/p-ipsu/Case/PublicationNumber/GB2459009
1014	Excerpt from <i>Comprehensive Dictionary of Electrical Engineering</i> (2nd ed. 2005)
1015	Plaintiff’s Disclosure of Asserted Claims and Infringement Contentions Against Vizio Pursuant to Northern District of

Reply Declaration of Regan Zane, Ph.D.

Exhibit No.	Description
	California Patent Local Rules 3-1 and 3-2, in <i>Polaris PowerLED Technologies, LLC v. VIZIO, Inc. et al.</i> , No. 2:23-cv-03478-GW-PDx
1016	Montu Doshi & Regan Zane, “Digital Architecture for Driving Large LED Arrays with Dynamic Bus Voltage Regulation and Phase Shifted PWM,” APEC 07 Digest
1017	Table of Contents for APEC 07
1018	Montu Doshi & Regan Zane, “Digital Architecture for Driving Large LED Arrays with Dynamic Bus Voltage Regulation and Phase Shifted PWM,” APEC 07 Presentation
1019	List of APEC 2007 Exhibitors
1020	Declaration of Gordon MacPherson from IEEE re <i>Zane</i>
1021	U.S. Patent Application Publication No. US 2007/0257869A1 to Huang et al. (“Huang”)
1026	Linear Technology, <i>LTC3783 Specification Sheet</i> , 2005
1027	U.S. Patent No. 6,621,235 to Chang (“Chang”)
1029	Tentative Claim Construction Order
1030	Final Rulings on Markman/Claim Construction, <i>Polaris PowerLED Techs., LLC v. VIZIO, Inc.</i> , No. 2:23-cv-03478 (C.D. Cal. May 8, 2024)

Reply Declaration of Regan Zane, Ph.D.

Exhibit No.	Description
2002	Declaration of Thomas L. Credelle
2003	<i>Curriculum Vitae</i> of Thomas L. Credelle
2004	Transcript of the Deposition of Regan A. Zane, Ph.D.
2005	U.S. Patent No. 7,948,468
2006	“Comprehensive Dictionary of Electrical Engineering,” Taylor & Francis Group, LLC, 2 nd Ed. (2005) (Excerpts)
2007	Final Rulings on Markman/Claim Construction, <i>Polaris PowerLED Techs., LLC v. VIZIO, Inc.</i> , No. 2:23-cv-03478 (C.D. Cal. May 8, 2024) (duplicate of EX1030)
2008	U.S. Patent No. 4,156,288
2009	U.S. Patent No. 3,166,715

6. In addition to the materials referenced above, I have also reviewed the Petition, the Board’s Institution Decision, and Polaris’ Patent Owner Response. I have also reviewed all other documents and exhibits cited in my declaration, to the extent they are not listed above.

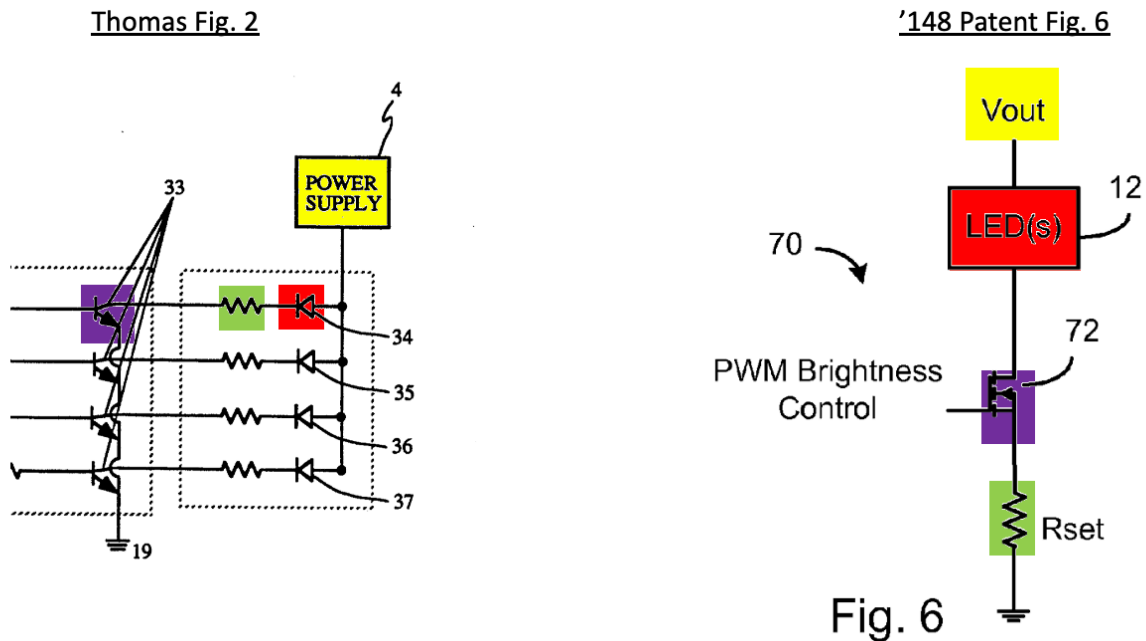
III. GROUNDS 1 AND 2A-2C BASED ON THOMAS

A. Thomas Discloses a Current Set Circuit (Limitations [1.b], [14.b])

7. Polaris and Mr. Credelle argued that the identification of Thomas's resistor does not meet the "current set circuit" limitation in Claims 1 and 14. As an initial matter, neither Polaris nor Mr. Credelle appeared to argue that Thomas *does not* disclose a current set circuit. Instead, they argued that the identification of an individual resistor is insufficient to meet the "current set circuit" limitation because a "circuit" requires at least two components that are connected. *See* POR, 8 ("The Petition does not identify an actual 'circuit' (i.e., multiple electronic components that are connected by conductive material) as required by the plain meaning of the term...."); *id.* at 9 ("A POSITA would understand 'circuit' to mean *two or more* components that are connected by conductive material so that current can flow between the components.... The claimed 'circuit' cannot be met by a single electronic component, such as a resistor or capacitor.")). I disagree for multiple reasons.

8. *First*, it should be emphasized that Thomas discloses essentially the same current set circuit as that shown in Figure 6 of the '148 Patent. The current set circuits in Thomas's Figures 1 and 2 and the '148 Patent's Figure 6 have the same circuit elements connected in series, each behaving and described in the same way to set the currents flowing through the LEDs. Both Mr. Credelle and I agree that

Figure 6 of the '148 Patent describes a current set circuit as recited in Claims 1 and 14. *See* EX2002, ¶35 (Mr. Credelle stating that “Figures 5 and 6 of the '148 patent both depict circuits that ‘may serve as each of the current set circuits 56-58 in FIG. 4.’ EX1001, 5:58-59, 6:7-8.”). As shown below, Figure 6 of the '148 Patent discloses a voltage source, V_{out} , in series with LEDs, a transistor, and a resistor R_{set} . Likewise, Thomas’s Figure 2 shows a voltage source (power supply) in series with LEDs, a resistor, and a transistor (which is part of the switch).



All four elements in both Thomas and Figure 6 of the '148 Patent behave in their normal way as understood by a POSITA. The supply voltage (highlighted yellow) provides a known voltage to the series circuit. The LEDs (highlighted red) provide light when the PWM transistor (highlighted purple) is in its “on” state. The PWM

transistor turns the LEDs on and off based on the PWM control signal. And, the current set resistor (highlighted green) sets the current in the series circuit whenever the PWM transistor is on. Thus, because Thomas discloses the same current set circuit as shown in Figure 6 of the '148 Patent, Thomas's disclosure must satisfy the "current set circuit" limitations in Claims 1 and 14.

9. **Second**, Polaris and Mr. Credelle mischaracterized my original declaration as identifying only an individual resistor "by itself" as the "current set circuit." See POR, 8; EX2002, ¶34. In my declaration, I explained how the resistor works in the series circuit and how it interacts with the voltage supply, the LEDs, and the PWM transistor, to result in a maximum current of $I=(V-V_{LED})/R$ when the PWM transistor is in its "on" state. See EX1003, ¶63. I did not identify a resistor "by itself" or to the exclusion of the other components that are connected to it. Indeed, when discussing dependent Claim 6 in my original declaration, I explained how the current set circuits in Thomas comprises both the resistors and the transistors. See EX1003, ¶¶110–112.

10. **Third**, I disagree with Polaris's and Mr. Credelle's position that a "current set circuit" cannot be met by a resistor because "a POSITA would consider a 'circuit' to require multiple components that are connected by a conductive material, such as a wire or trace on a circuit board, in order to form a 'circuit.'" EX2002, ¶34. Mr. Credelle ignores that the claim limitation is a "current set circuit,"

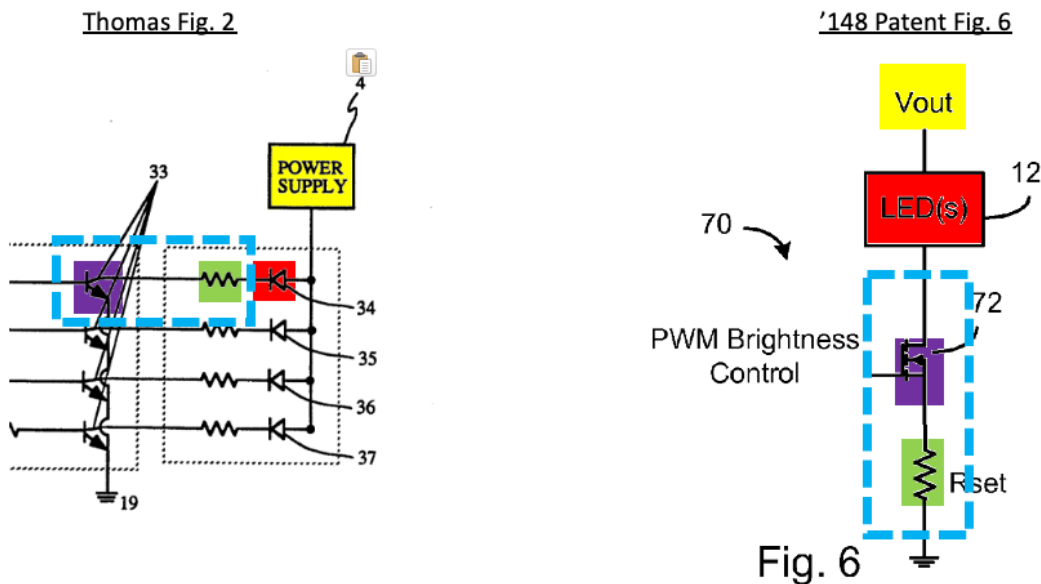
not a “circuit” in the abstract. Here, a POSITA would understand that the LED driver of claims 1 and 14 are a “circuit,” and the “current set circuit” is the portion of that LED driver that “control[s] a peak current through one or more LEDs connected in each parallel path.” Limitation [1.b]. Indeed, the ’148 Patent explains that a current set resistor may be a current setting circuit. *See* EX1001, 1:67–2:3 (“A current setting circuit 20-22 for each parallel path is shown, where each circuit 20-22 may comprise a current set resistor or a current regulator.”). I also am not aware of any language in either the specification or the prosecution history of the ’148 Patent indicating that the applicant intended to disclaim or disavow a single component from being a “current set circuit.” Thus, it would be inappropriate to further require that the “current set circuit” somehow requires at least two components connected to each other.

11. Notably, Mr. Credelle’s position would also lead to an absurd result that two resistors in series with each other could be a “current set circuit,” but a single resistor with an equivalent resistance could not.

12. ***Finally***, even under Polaris’s and Mr. Credelle’s interpretation of “current set circuit,” Thomas still anticipates Claims 1 and 14. For example, Mr. Credelle argued that the current set circuit described in Figure 6 of the ’148 Patent is a “current set resistor R_{set} and MOSFET 72 [that] are connected in series with the one or more LEDs.” EX2002, ¶36; *see also* POR, 10–11. A MOSFET is a type of

transistor. As discussed above, Thomas also discloses a current set resistor and transistor that are connected in series with the LEDs in Thomas. *See* EX1005, Figs. 1 and 2. Thus, Thomas also discloses a current set circuit, even under Polaris’s and Mr. Credelle’s construction of “current set circuit.”

13. As shown below in the dashed blue lines, if the Board were to adopt Polaris’s position that “current set circuit” must include at least two components such as a resistor and transistor, then Thomas discloses a “current set circuit” in the same way as described in the ’148 Patent. Thus, even under Polaris’s construction, Thomas still discloses limitations [1.b] and [14.b].



B. Thomas Applies a PWM Signal to the Current Set Circuit

14. Polaris and Mr. Credelle argue that Thomas does not “apply” a PWM brightness control signal to the current set circuit because Thomas does not apply

the PWM signals to the resistor. Again, their argument is based on their mischaracterization that the Petition and my original declaration only identified a single resistor by itself as the current set circuit. As explained in the previous section, that is not correct because my declaration did not identify a resistor as the current set circuit to the exclusion of the other components connected to it.

15. Polaris's and Mr. Credelle's argument also fails to distinguish Thomas from Claim 1 because, as I explained above, Thomas discloses the same current set circuit as disclosed in Figure 6 of the '148 Patent. And as explained above and in my original declaration, Thomas's current set circuit works in the same way as the current set circuit described in Figure 6 of the '148 Patent. When the PWM brightness control signal is high, the PWM transistor (reference numeral 72 in the '148 Patent, reference numeral 33 in Thomas) is turned on, and the current is set by the current set resistor and flows through the LED.

16. Polaris's and Mr. Credelle's argument also assume an additional unclaimed requirement that the PWM signal must be applied *directly* to the current set circuit. See POR, 14 (arguing "the PWM signal is never *applied* to the resistors in Thomas" and that "the PWM signals go to the activation switches") (original emphasis); EX2002, ¶41 (Mr. Credelle arguing "the PWM signal ... is not ever applied to the resistors" and that "the PWM signal is *only* applied as input to the AND gates in Figure 2") (original emphasis). But limitations [1.d] and [14.d] do not

include any requirement that the PWM signal must be applied directly to the current set circuit without any other components in between. And again, Thomas's circuit behaves exactly like the current set circuit described in Figure 6 of the '148 Patent, where the PWM signal is applied to the transistor that is connected in series with the resistor. Moreover, my original declaration explained how the PWM signals in Thomas are applied to the resistors via the activation switches. *See* EX1003, ¶70.

17. Finally, Polaris's and Mr. Credelle's argument fails under their own construction of "current set circuit." If the Board were to adopt Polaris's construction that a current set circuit must comprise at least two components connected to each other, Thomas still discloses the same current set circuit as in Figure 6 of the '148 Patent, namely a resistor and switch connected in series with each other. Under that construction, Thomas indisputably applies the PWM signal directly to the current set circuit because Thomas applies the PWM signal to the switch. *See* EX2002, ¶40 (Mr. Credelle stating that "Control of the current flow through these resistors is accomplished through a switch or AND gate ... to which the alleged PWM brightness control signal is applied."). Thus, Thomas discloses limitations [1.d] and [14.d] regardless of whether Polaris's claim construction of "current set circuit" is applied.

C. Thomas's Resistor Discloses a Basic Current Regulator (Claim 3)

18. Polaris and Mr. Credelle argued that Thomas's resistor is not a "current regulator" because it is not a "component that has the ability to actively regulate the amount of conducted current." EX2002, ¶44. Polaris and Mr. Credelle both draw a distinction between a passive component and an active component. *Id.* at ¶¶44–45; POR, 18 (Polaris arguing that "a passive resistor has no ability to *do* anything, unlike a current regulator, which would include components that can make changes to the current in real time."). I disagree with their argument.

19. First, Polaris (but not Mr. Credelle) argued that only Figure 5 of the '148 Patent is described as a current regulator but not Figure 6. POR, 18. But a POSITA would understand that Figure 6 also provides a regulated current. Specifically, the '148 Patent explains that in Figure 6, "A current set resistor R_{set} and MOSFET 72 are connected in series with one or more LEDs 12 in a single parallel path of the driver 50. Since V_{out} is substantially constant, the value of R_{set} is selected to establish the peak current through the LEDs 12." EX1001, 6:11–13. The '148 Patent also describes the voltage source as a voltage regulator. *See* EX1001, 5:26-47. A fixed resistance connected in series with a regulated voltage produces a regulated current, via Ohm's Law: $V=IR$. Thus, a POSITA would understand that Figure 6 of the '148 Patent describes a current regulator, albeit a basic one.

20. Like Figure 6 of the '148 Patent, Thomas's resistor is also in series with a regulated voltage. Thomas explains that the power supply provides a "regulated voltage." EX1005, 1:66–67. Indeed, the point of Thomas's invention is to *help* the power supply maintain a regulated voltage by mitigating sudden changes in the current demand. *See* EX1005, 1:55–2:10 (explaining "an object of the present invention [is] to provide a method and apparatus for pulse width modulation of LED's that reduces the magnitude of the instantaneous change in the current demand on the power supply such that a more stable output voltage can be maintained."). Because Thomas has a regulated voltage in series with the resistor, that results in a regulated current. Thus, as I stated originally, Thomas's resistor is a basic type of current regulator.

D. Thomas's Shift Register Necessarily Includes a Clock

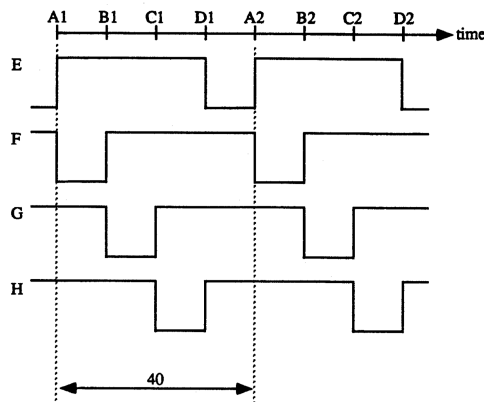
21. Polaris and Mr. Credelle argue that a shift register could be implemented without a clock. However, as set forth in my original declaration, I understand that something is inherent in the prior art if it necessarily flows from the explicit disclosure of the prior art. *See* EX1003, ¶23. Thus, in my opinion, it is not relevant whether some shift register could be implemented without a clock. Rather, the relevant question is whether *Thomas's shift register* necessarily has a clock. In my opinion, Thomas's shift register necessarily includes a clock.

22. Here, Thomas's shift register necessarily includes a clock in order to perform as described. Thomas explains:

[A] twelve bit shift register (31) is used to generate the delayed modulating signals (F, G, H) by *sequentially storing twelve binary values corresponding to the pulses or lack of pulses in the first modulating signal (E)*. The second, third and fourth modulating signals (F, G, H) are then generated by tapping the values stored within the fourth, eighth and twelfth cells of the shift register (31) *as the values are sequentially shifted through the twelve cells of the shift register* (31).

EX1005, 4:19–28. Thomas's reference to "sequentially storing twelve binary values corresponding to the pulses or lack of pulses in the first modulating signal (E)" and "as the values are sequentially shifted through the twelve cells of the shift register" confirm that the shift register must be shifting the bits each time a new bit (a pulse or lack of pulse from E) is fed into the shift register. In other words, Thomas's shift register is synchronous to the timing of the PWM signal *E* that is input into the shift register.

23. This behavior is also shown by Thomas's Figure 3, which shows how the delayed modulating signals *F*, *G*, and *H*, are continuously generated and synchronous with each new pulse or lack of pulse from *E*.



EX1005, Fig. 3. Because the shift register is shifting the bits concurrently with each new pulse or lack of pulse from *E* fed into it, the shift register is necessarily receiving a shift signal synchronous with each new pulse or lack of pulse from *E*. That synchronous shift signal is a clock signal.

24. Polaris's response suggested that there is just a "mere possibility of a clock" in Thomas's shift register. POR, 21. I disagree because the fact that Thomas's shift register has a clock connected to it is not a "mere possibility," it is a certainty. The fact that Thomas's shift register synchronously shifts the bits with each new pulse or lack of pulse that is fed into it from the modulating signal *E* confirms that there is a clock connected to Thomas. If Thomas's shift register did not have a clock, it would not be able to shift its bits synchronously with each new pulse or lack of pulse from *E*. Thus, a clock is necessarily present in Thomas's disclosed shift register.

25. Notably, neither Polaris nor Mr. Credelle have actually suggested, let alone argued, that Thomas's shift register could be implemented without a clock. *See* POR, 19–21; EX2002, ¶¶46–51. Instead, they only argued that asynchronous and dynamic shift registers may exist in other applications. *See id.* But neither Polaris nor Mr. Credelle argue that Thomas's shift register could be implemented as an asynchronous or dynamic register. *See id.*

26. For example, Mr. Credelle opined that Figure 12.4 in Exhibit 1011 (reproduced below) shows an example of a “dynamic” shift register.

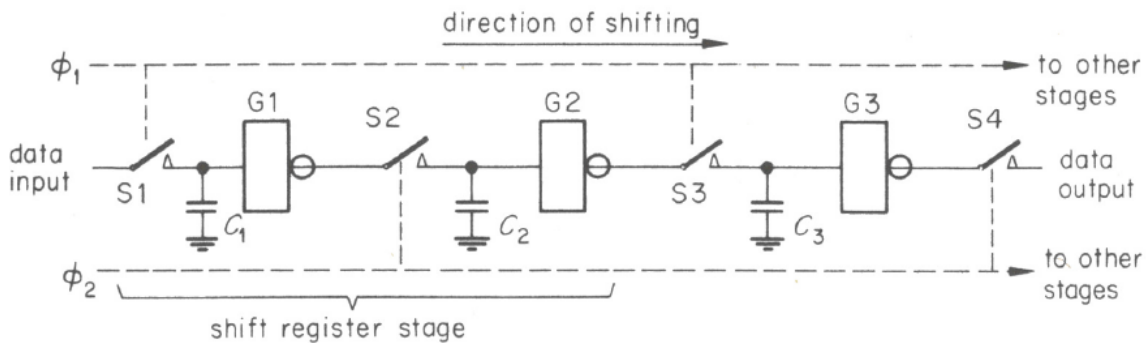


Fig. 12.4 The basis of a MOS dynamic shift register

EX1011, Fig. 12.4. In this register, the data is shifted down the register by using two control lines that are “energized by a two-phase pulse supply.” EX1011, 117. As described, the two-phase pulse supply alternates oppositely among the two phases between “1” and “0” signals in order to shift the data down the register. *Id.* at 117–18. However, Mr. Credelle does not argue that Thomas's shift register could be implemented with the register described in Figure 12.4 of Exhibit 1011. Instead,

he only stated that “this shift register can be used in memory circuits.” EX2002, ¶48. But Thomas’s shift register is not a memory circuit—it is used to continuously generate delayed versions of the modulating signal E as E is constantly being fed into the shift register. Moreover, even if Thomas’s shift register could be implemented using the register shown in Figure 12.4 of Exhibit 1011, it would still have a clock. Again, that is because Thomas’s shift register shifts the bits synchronously with the modulating signal E in order to accommodate each new bit (pulse or lack of pulse) in E fed into the shift register. Thus, the alternating signals ϕ_1 and ϕ_2 are just a two-phase clock signal.

27. Mr. Credelle also references Exhibits 2008 and 2009 and identifies them as asynchronous shift registers that “need not use a clock at all.” EX2002, ¶50. But these circuits are irrelevant to Thomas’s shift register. Thomas’s shift register is not an asynchronous shift register and cannot be implemented as an asynchronous shift register because it shifts synchronously with each new bit fed into it from the modulating signal E . Indeed, Exhibit 2008 explains that “Asynchronous shift registers ... are frequently employed between a data source which supplies data to the shift register at one speed and a data sink which intermittently takes data from the shift register at another speed.” EX2008, 1:11-16. In contrast, Thomas’s shift register is described as receiving the bits corresponding to the pulses or lack of pulses in the modulating signal E and generating the time-

delayed signals *F*, *G*, and *H*. See EX1005, 4:19–28, Figs. 2, 3. Thus, Thomas’s shift register needs to be receiving data, shifting data, and outputting data all at the same speed. It is not an asynchronous shift register. Exhibit 2009 similarly distinguishes an asynchronous shift register from a synchronous shift register. See EX2009, 2:12–21 (“The asynchronous device as contrasted with the synchronous device mentioned above does not require a clock or timing pulse for its operation.”). Thus, because Thomas’s shift register is a synchronous shift register, not an asynchronous shift register, it receives a clock signal for shifting the bits.

28. Notably, Mr. Credelle also did not suggest that an asynchronous shift register could be used as Thomas’s shift register. Mr. Credelle stated that such a shift register could be used in “a variety of useful applications, particularly in systems where direct control of the timing of the data shift is desired.” EX2002, ¶50. But Mr. Credelle did not identify Thomas’s shift register as one of those “useful applications.” Indeed, Thomas’s shift register is not a “system[] where direct control of the timing of the data shift is desired” because Thomas’s shift register shifts synchronously with each new pulse or lack of pulse from the signal *E*.

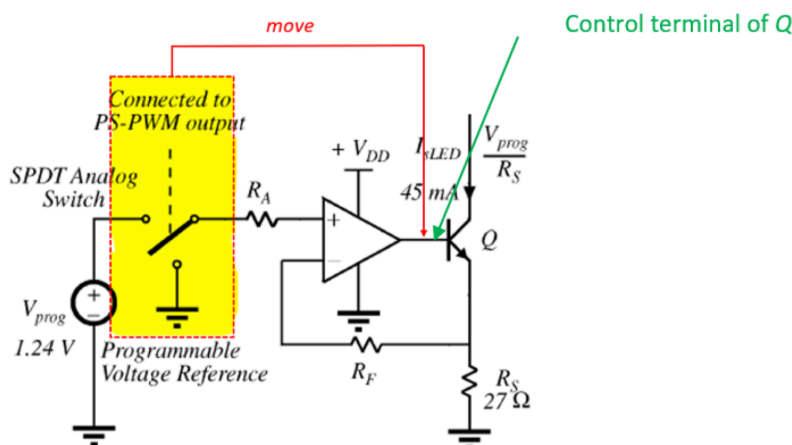
29. Thus, in my opinion, Thomas necessarily includes a clock connected to the shift register for shifting the bits down the register. The presence of a clock is certain because Thomas’s shift register is described as shifting synchronously with each new pulse or lack of pulse in the modulating signal *E*. Polaris’s and Mr.

Credelle's attempt to identify other types of shift registers that could be implemented without a clock therefore do not change the fact that Thomas's shift register must have a clock in order to operate as described.

IV. GROUNDS 3 AND 4 BASED ON ZANE

A. Claims 5 and 16: Changing the Location of Zane's SPDT Switch Would Not Change the Overall Operation of Zane's Current Sink

30. As I explained in my original declaration, Zane's current sink, shown in Figure 4 of EX1006, differs slightly from the limitations of Claims 5 and 16 with respect to the location of the transistor in the SPDT switch. See EX1003, ¶184. However, Claims 5 and 16 claim nothing more than an obvious variation of the current sink already disclosed in Zane. As I explained previously, it would have been obvious to relocate Zane's SPDT switch (which contains a transistor) from the noninverting (+) input of the op amp to between the op amp's output and the control terminal of the transistor Q , as shown below.



EX1003, ¶184 (annotating EX1005, Fig. 4). That is because the SPDT switch may be placed in several locations in *Zane*'s current sink without changing the overall operation of the circuit, and thus, a POSITA would have been motivated to try any of those locations as a matter of design choice between a finite number of identified, predictable solutions, with a reasonable expectation of success. EX1003, ¶185.

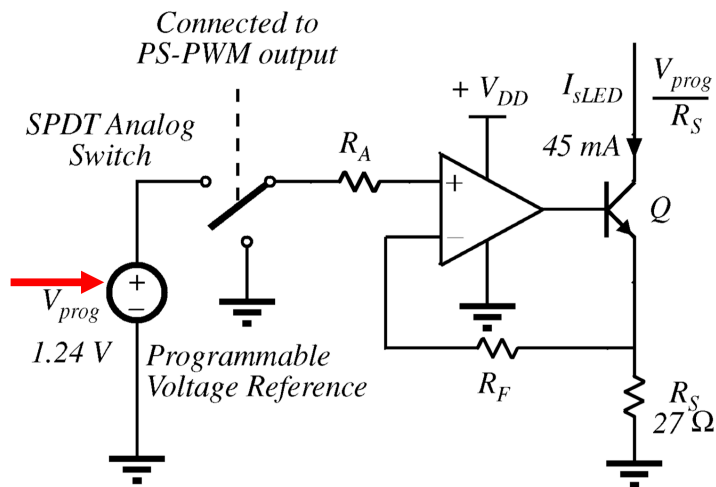
31. Polaris and Mr. Credelle disputed the motivation to combine by arguing that the modification “would affect the design and operation of the circuit.” POR, 40 (citing EX2002, ¶¶53–57). More specifically, Mr. Credelle argued that the modification “would frustrate the purpose of the circuit by hampering its ability to maintain a precision voltage.” EX2002, ¶57. I disagree with these arguments.

32. First, neither Polaris nor Mr. Credelle have actually identified any material difference caused by relocating the SPDT switch that would result in a change to the overall operation of *Zane*'s circuit. As I already explained in my original declaration and during my deposition, moving the SPDT switch from the noninverting input of the op amp to the output of the op amp would not change the operation of the circuit. *See* EX1003, ¶¶184–86; EX2004, 121:5–123:21.

33. Second, Mr. Credelle argued that “the analog SPDT switch characteristics are not disclosed by *Zane*, but it is clear that *Zane* has designed the analog SPDT switch to apply a precision voltage to the positive terminal of the op amp to achieve a precision current flow V_{prog}/R_s in the LED strings.” EX2002, ¶57;

see also id. at ¶54 (“Nor does *Zane* disclose the effect on the precision voltage applied to the op amp through R_A by this analog SPDT switch.”). These statements do not make sense because the SPDT switch does not apply a voltage to the “+” terminal of the op amp. A POSITA would understand that V_{prog} is supplied by a different component that *Zane* refers to as “a programmable voltage source” or “Programmable Voltage Reference.” EX1006, 290, Fig. 4. That programmable

voltage source is labelled with the  symbol in *Zane's* circuit diagram and identified by the red arrow below:



EX1006, Fig. 4 (annotated). The SPDT switch is simply in between the programmable voltage source that supplies V_{prog} and the “+” terminal of the op amp, and the purpose of the SPDT switch is to open and close the circuit such that V_{prog} is applied to the “+” terminal when the circuit is closed, and no voltage is applied

when the circuit is opened. In other words, the SPDT switch turns *Zane's* current sink “on” or “off.”

34. Third, Mr. Credelle also argued, “[i]f the precision voltage V_{prog} is simply applied to R_A , as would occur in the modification suggested by Dr. Zane, a POSITA would not know how to adjust the op amp settings to achieve the correct voltage on the basis of transistor Q.” EX2002, ¶57. That statement is also incorrect. Mr. Credelle ignores that this is actually how the circuit works in normal operation. When the SPDT switch is closed, V_{prog} and R_A are, in fact, directly connected via the switch. Mr. Credelle has not articulated any reason, nor am I aware of any reason, why a POSITA would be confused by the modification. To the extent Mr. Credelle was referring to some potential voltage drop across the switch, a POSITA would understand that voltage drop to be negligible and have no impact on the overall function of the circuit. A POSITA would know that an ideal op amp is modeled as having infinite input impedance, while real-world op amps have extremely high input impedance. Next to no current flows into the input terminals of an op amp. And because almost no current flows into the terminal, any voltage drop across the switch as a result of that current is also negligible compared to the reference voltage V_{prog} . Thus, a POSITA would understand that moving the SPDT switch would have essentially no impact on the reference voltage seen at the “+” input of the op amp, and no adjustment would be needed to the op amp to properly drive transistor Q.

35. Finally, Mr. Credelle argues that “if the analog SPDT switch were placed after the op amp, a POSITA would not know if the precision voltage V_{prog} would still set the LED current to the desired current because the properties of the analog SPDT switch are unknown.” EX2002, ¶57. Again, that is incorrect because a POSITA would understand that the properties of the SPDT switch are irrelevant to the current. As *Zane*’s Figure 4 states, the magnitude of the current through the LEDs is $I_{sLED} = V_{prog}/R_s$. In fact, a POSITA would understand that the point of using an op amp in a negative feedback loop is to regulate the voltage across the resistor R_s to be equal to V_{prog} , regardless of any nonidealities in the circuit. A POSITA would have learned about the operation of negative feedback loops as part of their undergraduate coursework on circuits and thus, the feedback loop in *Zane*’s current sink would have been well understood by a POSITA. The op amp accomplishes this through negative feedback by automatically adjusting the op amp voltage output to achieve the desired current in the transistor Q . Thus, a POSITA would recognize that the feedback circuit would automatically compensate for any small effect of the SPDT switch when placed between the op amp output and the base of transistor Q , such as a very small voltage drop across the switch. A POSITA would understand that no adjustments would be necessary to the feedback circuit and the circuit would still set the current to V_{prog}/R_s .

Reply Declaration of Regan Zane, Ph.D.

36. Accordingly, Mr. Credelle is incorrect in arguing that the proposed modification to *Zane* would have somehow frustrated the purpose and function of the circuit. A POSITA would have understood that the circuit would work the same way regardless of the relocation of the SPDT switch. Thus, Claims 5 and 16 would have been obvious to a POSITA over *Zane*.

I declare that all statements made herein on my own knowledge are true and that all statements made on information and belief are believed to be true, and further, that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Dated: August 15, 2024

By: 
Regan Zane, Ph.D.