

*VIZIO, INC.*  
*v.*  
*POLARIS POWERLED TECHNOLOGIES, LLC*

IPR2024-00073  
U.S. Patent No. 7,843,148

*Petitioner VIZIO, Inc.'s Demonstratives*  
*December 5, 2024*

## Overview of the Grounds

| Ground | Reference(s)                                                                                        | Basis        | Challenged Claims                   |
|--------|-----------------------------------------------------------------------------------------------------|--------------|-------------------------------------|
| 1      | <i>Thomas</i>                                                                                       | Anticipation | 1, 3, 7, 9–12, 14, 17, 18, 20–22    |
| 2A     | <i>Thomas</i>                                                                                       | Obviousness  | 1, 3, 6, 7, 9–12, 14, 17, 18, 20–22 |
| 2B     | <i>Thomas</i> in view of the Applicant admitted prior art (“AAPA”) and/or the knowledge of a POSITA | Obviousness  | 2, 13, 15                           |
| 2C     | <i>Thomas</i> in view of <i>Tatewaki</i> and the knowledge of a POSITA                              | Obviousness  | 8, 19                               |
| 3      | <i>Zane</i>                                                                                         | Anticipation | 1–4, 11, 12, 14, 17, 22             |
| 4      | <i>Zane</i>                                                                                         | Obviousness  | 1–4, 5, 11–17, 22                   |

## Level of Ordinary Skill in the Art

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- Institution Decision adopted (with modification) Petitioner's definition:

A POSITA at the time of the invention of the '148 Patent would have had ~~at least~~ a bachelor's degree in physics, electrical engineering, or a related field, and approximately two years of experience in the fields of LED technology, backlights, LED devices and control thereof, or other related fields. Alternatively, advanced education in the fields of physics, electrical engineering, or a related field can compensate for lesser work experience in the relevant fields.

- PO did not challenge the level of ordinary skill.

## No Secondary Considerations of Non-Obviousness

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PO did not raise any secondary considerations of non-obviousness in its Patent Owner Response or Sur-Reply

See *generally* POR, Sur-Reply

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# *Zane* Grounds (Grounds 3 & 4)

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# Overview of Zane

## Montu Doshi & Regan Zane, “Digital Architecture for Driving Large LED Arrays with Dynamic Bus Voltage Regulation and Phase Shifted PWM,” APEC 07 Digest

Discloses an LED driver circuit for driving parallel LED strings using a digital phase shifted pulse width modulator

### Digital Architecture for Driving Large LED Arrays with Dynamic Bus Voltage Regulation and Phase Shifted PWM

Montu Doshi and Regan Zane  
Colorado Power Electronics Center (CoPEC)  
Department of Electrical and Computer Engineering  
University of Colorado at Boulder, USA  
[montu.doshi, zane]@colorado.edu

**Abstract** – This paper introduces a digital architecture suitable for driving a large number of High Brightness Light Emitting Diodes (HB-LEDs) with improved system efficiency and reduced EMI. Key advantages are achieved by combining and coordinating control of the power converter and LED strings, resulting in a system with deterministic load behavior. Uniform phase shifting of LED strings is performed to minimize load current variations, resulting in reduced output capacitance, improved converter efficiency and reduced system EMI. LED string voltages are detected online and used in a feedforward path for dynamic bus voltage scaling, resulting in improved system efficiency at low dimming levels. Experimental results are presented for a 15 W boost converter with FPGA based digital control driving a 64 LED array with 8 LED strings.

#### 1. INTRODUCTION

The emergence of HB-LEDs has ushered a new era of solid state lighting solutions that provide distinct performance advantage over conventional lighting technology. Higher optical efficiency, long operating lifetimes, wide operating temperature range and environmentally friendly implementation are some of the key advantages cited in favor of LED technology over incandescent or gas discharge solutions [1, 2]. However, manufacturing variations in forward voltage drop, luminous flux output and peak wavelength necessitate binning strategies resulting in low yield and increased cost [3, 4]. Further, a large number of such LEDs, with matched characteristics arranged in a suitable optical housing, are required to meet the desired optical and luminance performance requirements. Dimming requirements along with the need for circuit compensation techniques to regulate light output over a range of temperature and life time render the simple resistor biased drive solution obsolete for modern LED [5].

Various circuit techniques based on switching and linear regulating devices have been described for driving a single “string” of series LEDs with precise forward current regulation and pulse modulation based dimming techniques [6-8]. Such architectures require a dedicated drive circuit for each LED string, and hence do not scale well with a large number of strings. An integrated solution with multiple current sinks for driving parallel LED strings is described in [9, 10]. The design assumes a separate independent power supply

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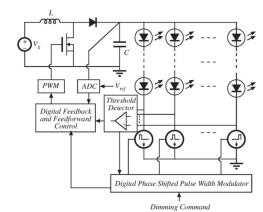


Figure 1. Proposed digital architecture for driving a scalable number of parallel LED strings. The approach integrates both converter control and current regulation of each LED string to facilitate system level optimization.

for delivering a shared voltage bus to the parallel LED string. This paper presents an approach that integrates the controls for both the power converter and parallel LED string current regulation. The architecture, shown in Fig. 1, creates new opportunities for system level optimization by having a single element control both the power delivery and what is now a deterministic load, characterized by the current level and on/off state for each LED string. The system input is a dimming or light level command, which is processed to provide coordinated responses by the converter and LED string current regulation. Key advantages are achieved by performing phase shifted pulse width modulation (PS-PWM) of the LED strings to eliminate pulsed currents from the converter output and dynamic bus voltage regulation for improved efficiency. A hardware efficient digital PWM is adopted from [11, 12] for natural phase shifting of the PWM drive signals to each parallel LED string. Dynamic bus voltage regulation is achieved through feed-forward of load changes from the PS-PWM, active sensing of the required drive voltage for each LED string and optimal sequencing of LED strings.

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Vizio Ex. 1006  
IPR Petition - USP 7,843,148

EX1006; Pet., 11–13; EX1003, ¶¶46–49

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## Overview of *Zane* Grounds (3 & 4)

| Basis                   | Challenged Claims       | Arguments by PO                                                                                                             |
|-------------------------|-------------------------|-----------------------------------------------------------------------------------------------------------------------------|
| Anticipation (Ground 3) | 1–4, 11, 12, 14, 17, 22 | Alleged bias from Dr. Zane                                                                                                  |
| Obviousness (Ground 4)  | 1–5, 11–17, 22          | <p>Legal sufficiency of arguments for Claims 1 &amp; 14;</p> <p>Proposed modification for Claims 5 &amp; 16 not obvious</p> |

## Dr. Zane Is Qualified to Give Expert Opinions about *Zane*

- PO identified no authority holding that an author of a prior art reference is unqualified to opine on that reference. Board previously rejected similar argument.
- Dr. Zane performed his analysis from the perspective of a POSITA.

32. I have performed my analyses, and expressed my opinions, from the perspective of the POSITA (as further described below) at the relevant time. In addition, while my declaration analyzes and presents opinions about *Zane*, which is a paper that I co-authored, my analysis of that paper is from the perspective of a POSITA reviewing that paper at the relevant time.

EX1003, ¶32

- PO and PO's expert offer no rebuttal to Dr. Zane's opinions about *Zane* for any claims other than Claims 5 and 16.

## Dr. Zane Explained That The Claimed Subject Matter Is Not New

PO alleges: “Dr. Zane believes that *he* invented the technology described in at least claims 1–4, 11, 12, 14, 17, and 22 of the '148 patent before the inventors of the '148 patent.” POR, 31

What Dr. Zane actually said:

Q So is it your opinion that you and Dr. Doshi invented the subject matter of Claim 1 of the '148 patent?

A I believe **that's a mischaracterization** of the opinions that I've provided here.

EX2004, 59:4–8

Now I believe you're asking me a new question. And I'm not sure the entire context of

that question with regard to whether the authors of that article, which include myself and my student at the time, now Dr. Doshi, invented elements in Claim 1. That's not an analysis that I performed, and I'm not sure what the scope and context of that in particular would be.

But **I can certainly confirm that there are many aspects of components that are used in the article, the Zane article, that the Zane article itself even indicates were known in the field at the time of that article.**

EX2004, 60:21–61:11

EX2004, 59:4–8; Reply, 4

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## “Anticipation Is the Epitome of Obviousness”

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- PO argues obviousness arguments for Claims 1 and 14 are deficient
- No modifications to *Zane* are necessary; undisputed that *Zane* anticipates Claims 1 and 14
- “[I]t is well settled that a disclosure that anticipates under § 102 also renders the claim invalid under § 103, for anticipation is the epitome of obviousness.”
  - *Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1373 (Fed. Cir. 2019) (internal quotations omitted)

## Claim 5 (Disputed)

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[5.pre] The driver of claim 4

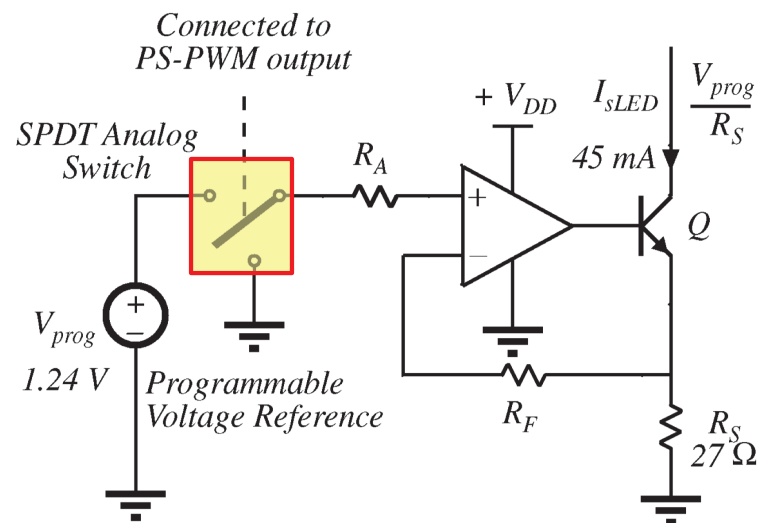
[5.a] wherein each current set circuit further comprises a PWM brightness control transistor connected **between an output of the feedback circuit and a control terminal of the current control transistor,**

[5.b] the PWM brightness control transistor being connected to the PWM brightness control signal generator for receiving a staggered PWM brightness control signal to couple the output of the feedback circuit to the control terminal of the current control transistor at a duty cycle of the staggered PWM brightness control signal.

## Zane Discloses a PWM Brightness Control Transistor

[5.a] wherein each current set circuit further comprises a PWM brightness control transistor connected between an output of the feedback circuit and a control terminal of the current control transistor,

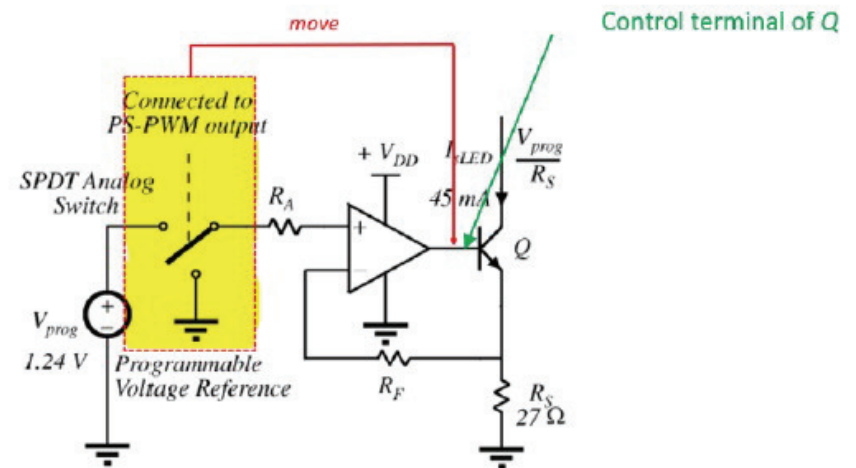
- SPDT analog switch contains a transistor



EX1006 Fig. 4 (annotated)

## Obvious to Move SPDT Switch to Claimed Position

- SPDT switch may be placed in several locations in the circuit without changing the overall operation of the circuit.
- SPDT switch is an on/off switch that controls current through LEDs. Works by opening or closing the circuit.
- Finite number of ways in which the SPDT switch can be connected to the programmable current sink → obvious to try as a design choice



EX1006, Fig. 4 (annotated)

## The Modification Would Have Been Obvious

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- PO criticized the Petition as only explaining that the SPDT switch *could* be placed in several locations, not that a POSITA *would* make the modification
- Incorrect—Petition & Dr. Zane explained:
  - “[A] POSITA would have understood that there are a finite number of ways in which the PWM brightness control transistor could be connected to *Zane’s* programmable current sink, and it would have been obvious to try any of those solutions as a design choice.” Pet., 78–79 (citing EX1003, ¶186).

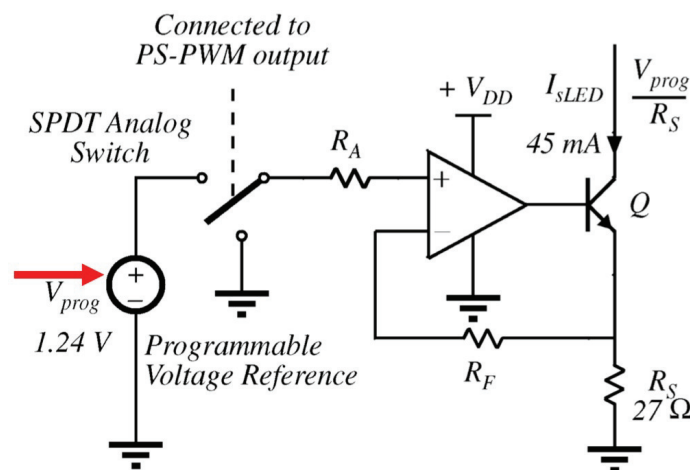
## Modification Does Not Change Operation of Circuit

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- PO & PO's expert argued the modification would "hamper[] its ability to maintain a precision voltage," but Dr. Zane explained:
  - PO identified no material difference caused by relocating the SPDT switch. EX1031, ¶32.
  - Dr. Zane: "[M]oving the SPDT switch from the noninverting input of the op amp to the output of the op amp would not change the operation of the circuit." *Id.*

## Precision Voltage Is Supplied By Different Component

- PO's expert argued that "Zane has designed the analog SPDT switch to apply a precision voltage to the positive terminal of the op amp to achieve a precision current flow  $V_{\text{prog}}/R_S$  in the LED strings." EX2002, ¶57.
  - But SPDT switch does not apply the voltage  $V_{\text{prog}}$  to the op amp "+" terminal; it is an on/off switch. EX1031, ¶33. The voltage  $V_{\text{prog}}$  is supplied by a different component. *Id.*



EX1006, Fig. 4 (annotated)

## Modification Does Not Require Adjustment to Op Amp

- PO's expert argued "[i]f the precision voltage  $V_{\text{prog}}$  is simply applied to  $R_A$ , as would occur in the modification suggested by Dr. Zane, a POSITA would not know how to adjust the op amp settings to achieve the correct voltage on the base of transistor Q." EX2002, ¶57.
  - This describes the normal operation of the circuit.  $V_{\text{prog}}$  and  $R_A$  are directly connected when the SPDT switch is closed. EX1031, ¶34.
  - PO's expert did not identify any reason why a POSITA would have been confused by the modification. *Id.* No adjustment would be needed to the op amp. *Id.*
  - The properties of the SPDT switch are irrelevant to the current; the negative feedback circuit automatically adjusts its output to achieve the desired current. *Id.*, ¶35.

## Properties of SPDT Switch Are Irrelevant to Current

- PO's expert argued "if the analog SPDT switch were placed after the op amp, a POSITA would not know if the precision voltage  $V_{\text{prog}}$  would still set the LED current to the desired current because the properties of the analog SPDT switch are unknown." EX2002, ¶57.
  - Incorrect because the properties of the SPDT switch are irrelevant to the current. EX1031, ¶35.
  - The current is  $I_{\text{sLED}} = V_{\text{prog}}/R_S$  which is independent of any properties of the SDPT switch. *Id.*
  - The negative feedback circuit automatically adjusts its output to achieve the desired current. *Id.*, ¶35.
  - "[A] POSITA would understand that the point of using an op amp in a negative feedback loop is to regulate the voltage across the resistor  $R_S$  to be equal to  $V_{\text{prog}}$ , regardless of any nonidealities in the circuit." *Id.* (emphasis added)

## Claim 16 (Disputed)

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- Claim 16 corresponds to Claim 5 and would have been obvious for the same reasons as Claim 5.
- Claim 16 uses the phrase “pass transistor” instead of “PWM brightness control transistor” in Claim 5.
  - The SPDT switch identified for Claim 5 is the “pass transistor” for Claim 16.
- For the same reasons as Claim 5, it would have been obvious to move the SPDT switch from the noninverting input of the op amp to between the op amp output and the control terminal of the current control transistor Q. EX1003 ¶¶201–203.

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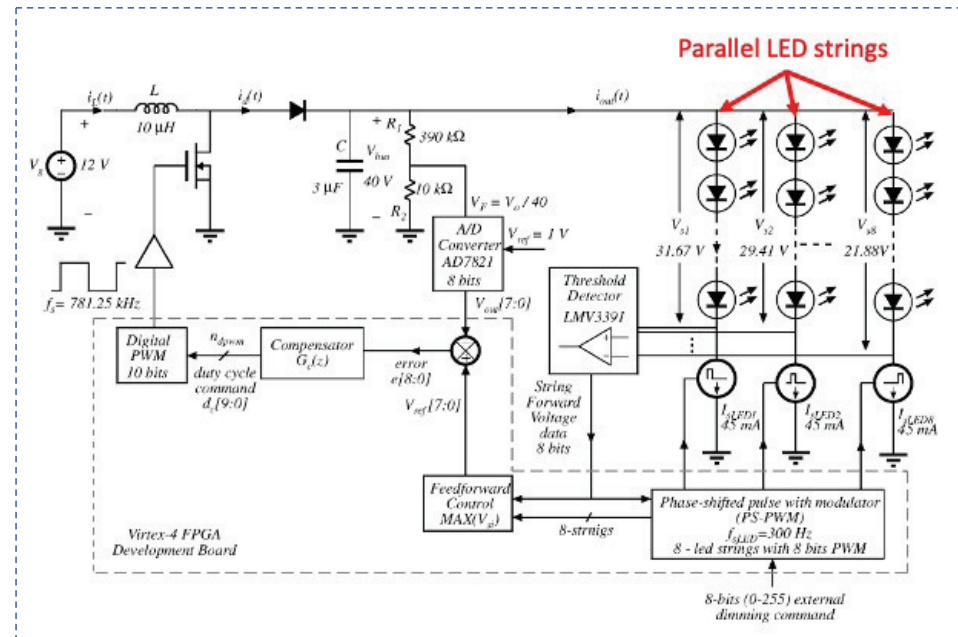
# Unrebutted Claims (*Zane* Grounds)

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## Preamble [1.pre] (Unrebutted, Grounds 3 & 4)

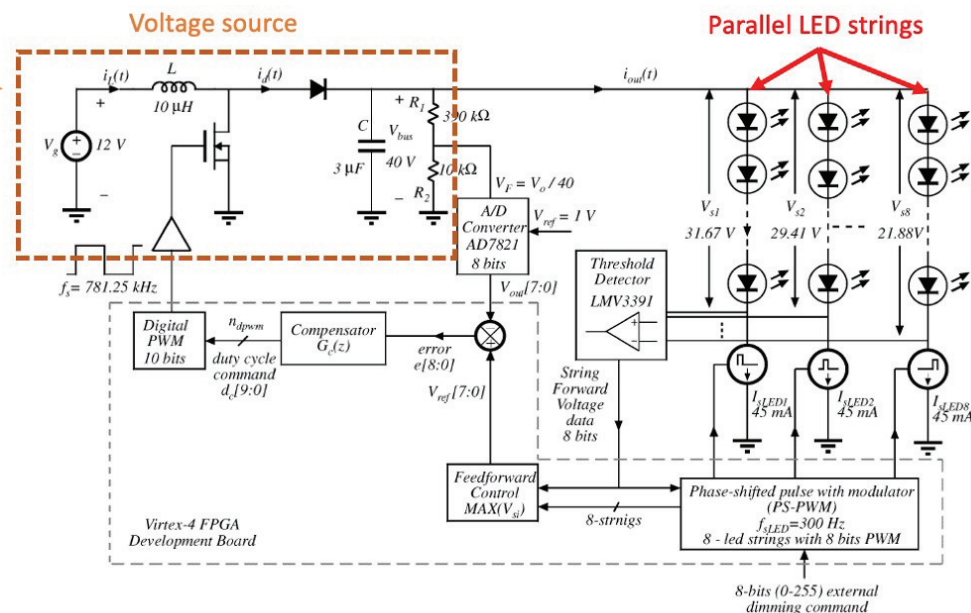
[1.pre] “A light emitting diode (LED) driver for driving LEDs connected to different parallel paths”



EX1006, Fig. 3 (annotated)

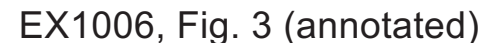
## Limitation [1.a] (Unrebutted, Grounds 3 & 4)

[1.a] “the driver comprising:  
a voltage source for  
connection to first ends of  
LEDs in a plurality of  
parallel paths”

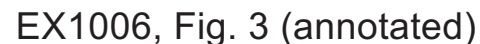


EX1006, Fig. 3 (annotated)

[1.b] “a plurality of current set circuits, one current set circuit per parallel path, each current set circuit controlling a peak current through one or more LEDs connected in each parallel path; and”



[1.c] "a pulse-width modulated (PWM) brightness control signal generator connected to the plurality of current set circuits, the brightness control signal generator being configured to generate staggered PWM brightness control signals to the plurality of current set circuits,"



## Limitation [1.c] (Unrebutted, Grounds 3 & 4)

[1.c] "a pulse-width modulated (PWM) brightness control signal generator connected to the plurality of current set circuits, the brightness control signal generator being configured to generate staggered PWM brightness control signals to the plurality of current set circuits,"

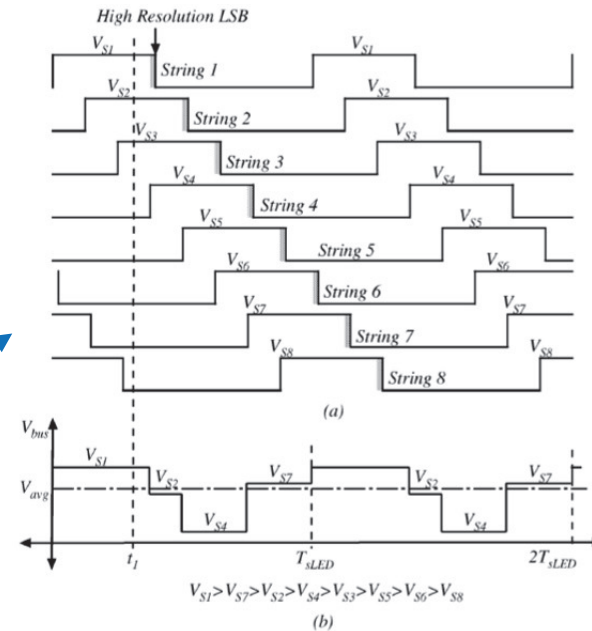


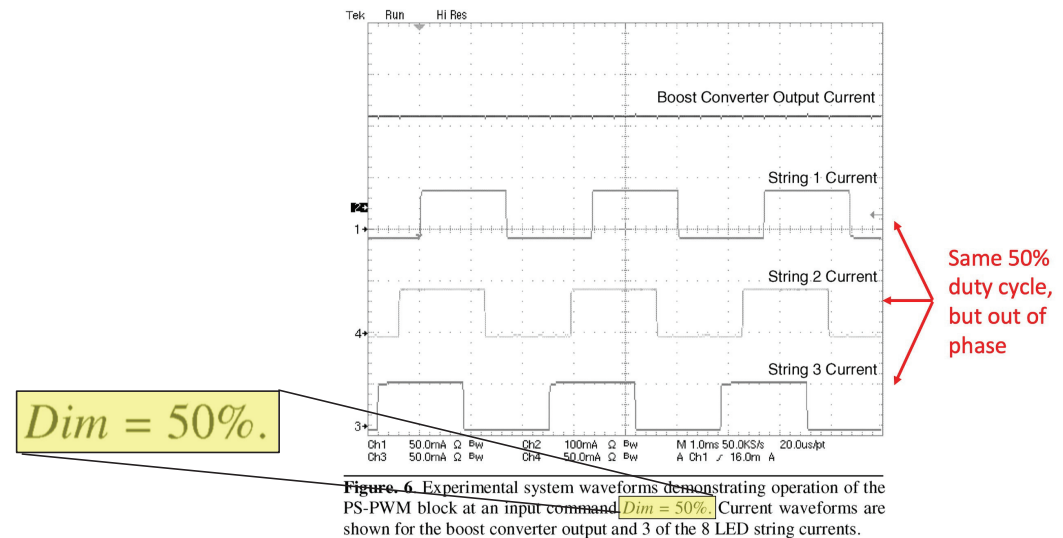
**Figure 2(a).** PS-PWM operating waveforms at 40% dimming command ( $Dim=0110\_0110$  {102},  $MSB = 011$  {3},  $LSB = 0\_0110$  {6}) illustrating the phase rotation, with three LED strings 'on' at a given time and the LSB output (shaded area) added to end of each MSB to generate required resolution.

EX1006, Fig. 2(a)

## Limitation [1.d] (Unrebutted, Grounds 3 & 4)

[1.d] “each current set circuit being configured to draw the peak current through its associated one or more LEDs at a duty cycle substantially corresponding to a duty cycle of a PWM brightness control signal applied to it, such that the plurality of current set circuits conduct current through their associated one or more LEDs at the same duty cycle but out of phase with each other.”

“An external dimming command, received by the PS-PWM module, is used to determine the appropriate phase-shift and duty cycle of individual control output signals. ... [T]he peak-to-peak load current amplitude is limited by the PS-PWM block to just one LED string regulation current (45 mA).” EX1006, 291.

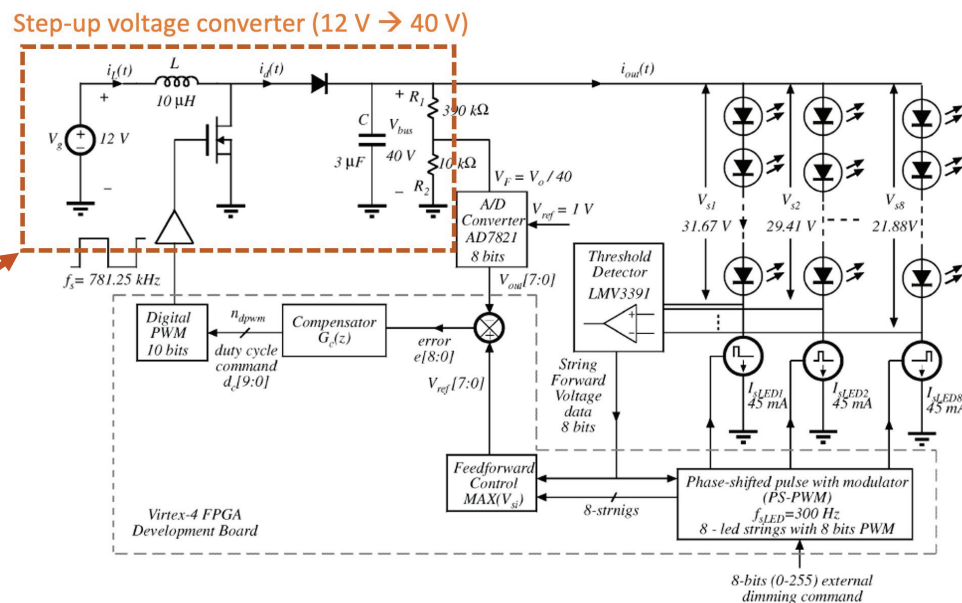


EX1006, Fig. 6

## Claim 2 (Unrebutted, Grounds 3 & 4)

Claim 2: “The driver of claim 1 wherein the voltage source is a step up voltage regulator.”

“The boost converter is designed to output a 40 V signal from 12 V input supply....” EX1006, 290.

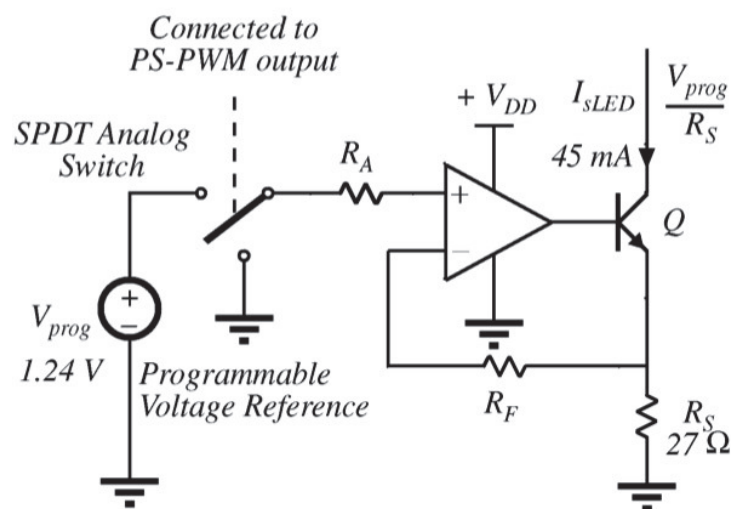


EX1006, Fig. 3 (annotated)

## Claim 3 (Unrebutted, Grounds 3 & 4)

Claim 3: “The driver of claim 1 wherein each current set circuit is a current regulator.”

“The forward current through the LEDs is regulated by a discrete precision programmable current sink, as shown in Fig. 4.” EX1006, 290



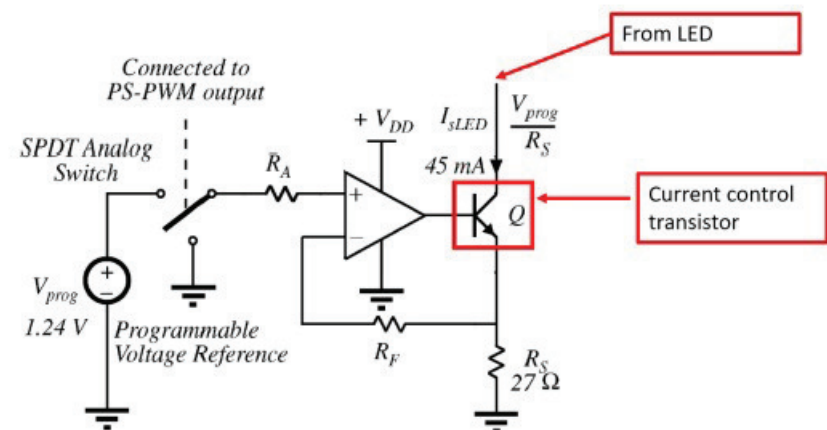
EX1006, Fig. 4

## Limitations [4.pre]-[4.a] (Unrebutted, Grounds 3 & 4)

[4.pre] “The driver of claim 1 wherein each current set circuit is a current regulator comprising:”

[4.a] “a current control transistor in series with one or more LEDs in an associated parallel path”

### Current Control Transistor in Series with LED

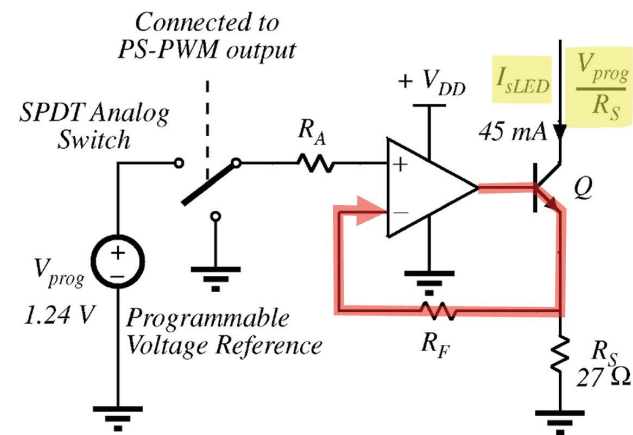


EX1006, Fig. 4 (annotated)

## Limitation [4.b] (Unrebutted, Grounds 3 & 4)

[4.b] “a feedback circuit connected to detect a current through the parallel path and connected to the current control transistor to control a conductivity of the current control transistor to cause the current through the parallel path to match a reference level.”

### Feedback Circuit



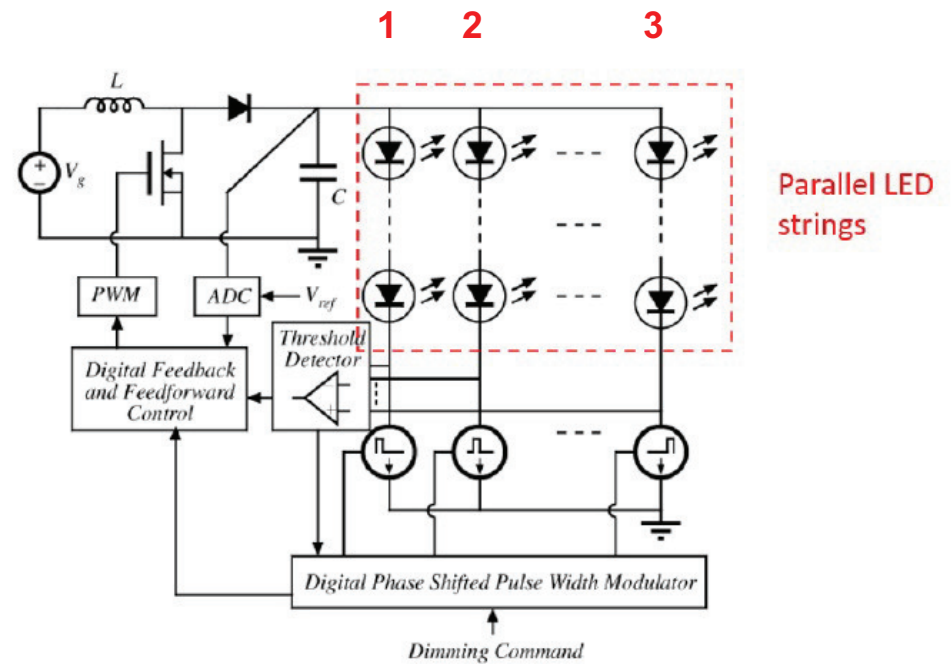
EX1006, Fig. 4 (annotated)

Current  $I_{sLED} = \frac{V_{prog}}{R_S}$ ,  $V_{prog}$  is a programmable voltage reference

## Claims 11 & 22 (Unrebutted, Grounds 3 & 4)

Claim 11: “The driver of claim 1 wherein the plurality of parallel paths comprises at least three paths.”

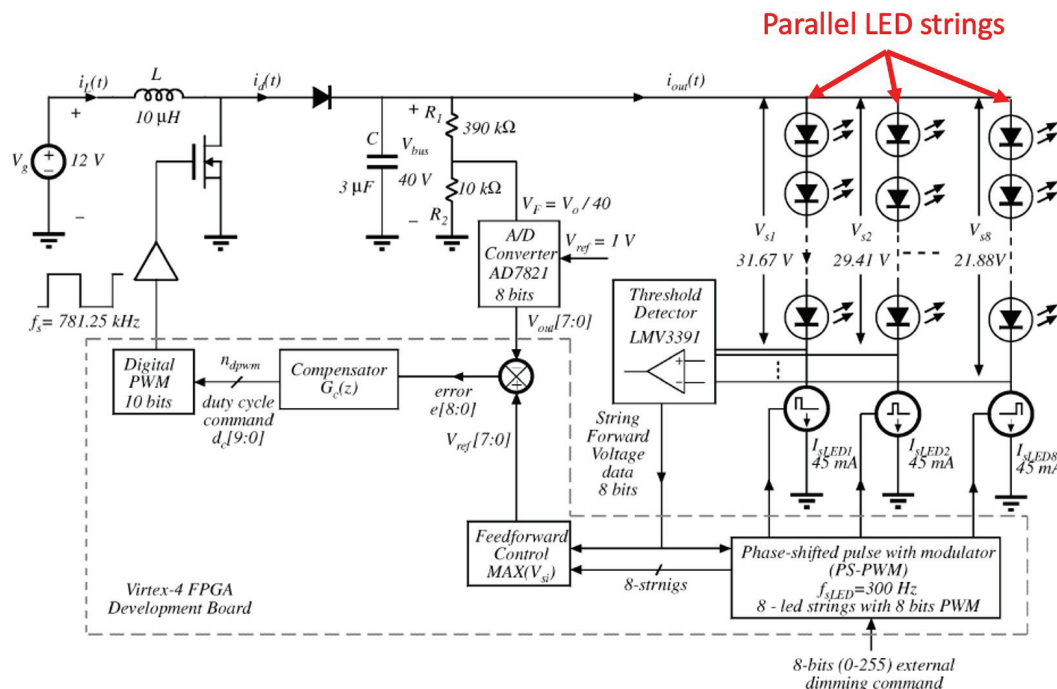
Claim 22: “The method of claim 14 wherein the plurality of parallel paths comprises at least three paths.”



EX1006, Fig. 1 (annotated)

## Claim 12 (Unrebutted, Grounds 3 & 4)

Claim 12: “The driver of claim 1 further comprising the LEDs connected to the driver.”



EX1006, Fig. 3 (annotated)

## Claim 13 (Unrebutted, Ground 4)

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Claim 13: “The driver of claim 1 wherein the driver is formed as an integrated circuit.”

- *Zane* discloses use of integrated circuits for the digital controls, current sinks, and voltage protection of the driver.
- Industry standard practice to fabricate circuits as integrated circuits, and POSITA would have been motivated to fabricate *Zane*’s LED driver as an integrated circuit.

## Claim 14 (Unrebutted, Grounds 3 & 4)

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- Claim 14 is a method claim corresponding to Claim 1
- Undisputed that Claim 14 is anticipated by *Zane* for same reasons as Claim 1
- Claim 14 also obvious for same reasons as Claim 1

## Claim 15 (Unrebutted, Ground 4)

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Claim 15: “The method of claim 14 further comprising varying the duty cycle of the staggered PWM brightness control signals to change an average current through the parallel paths of LEDs to change a perceived brightness of the LEDs.”

Dr. Zane explained:

- “[T]he purpose of driving LEDs using PWM is to be able to dim the brightness of the LEDs by applying a fixed current and rapidly turning the LEDs on and off according to a duty cycle, rather than by changing the magnitude of the current actually flowing through the LEDs.” EX1003, ¶196
- “A duty cycle of X% means that the LEDs are on X% of the time, meaning that the average current through the LEDs is X% of the fixed current.” *Id.*

## Claim 17 (Unrebutted, Grounds 3 & 4)

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Claim 17: “The method of claim 14 wherein applying a different staggered PWM brightness control signal to each current set circuit comprises applying each staggered PWM brightness control signals to an associated transistor connected in series with the one or more LEDs in an associated parallel path, such that the transistor is turned on and off corresponding to the duty cycle of the staggered PWM brightness control signal applied to it.”

*Zane* discloses all limitations for same reasons as Limitations [4.a] and [4.b].

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# Thomas Grounds (1, 2A-2C)

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# Overview of *Thomas* Disclosure

U.S. Patent No. 5,317,307 to Thomas, Jr.

Title: METHOD FOR PULSE WIDTH MODULATION OF LEDS WITH POWER DEMAND LOAD LEVELING

Issued: May 31, 1994

Discloses an LED driver with multiple LEDs connected in parallel to a power supply and driven with multiple, staggered PWM signals.

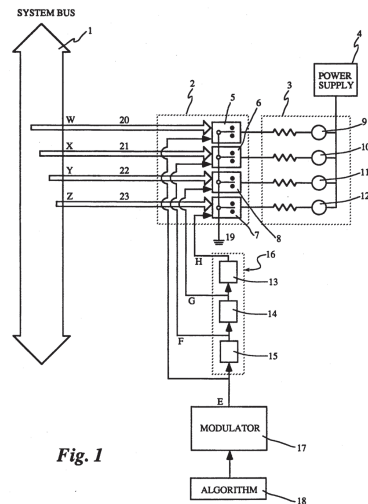


Fig. 1

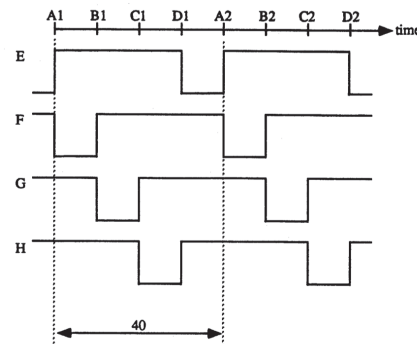
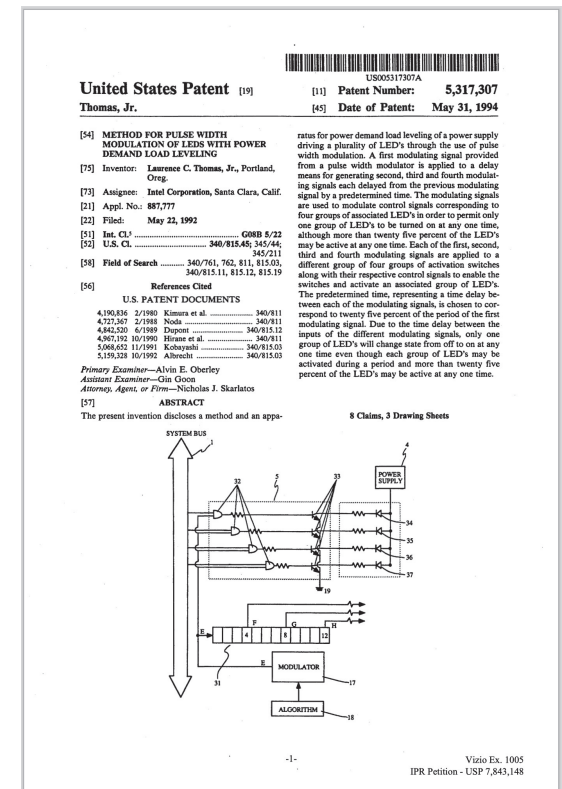


Fig. 3

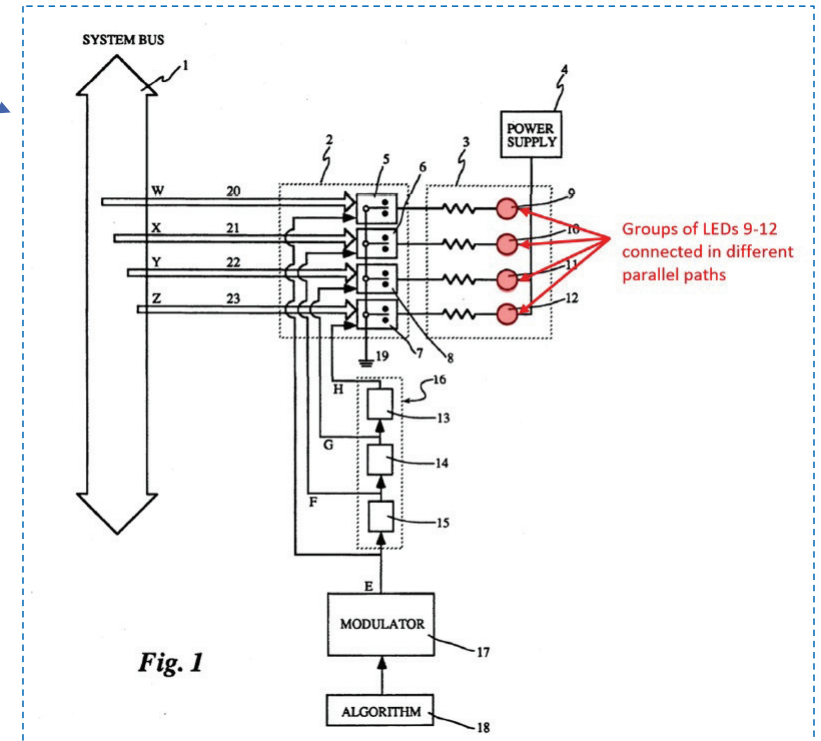


## Overview of *Thomas* Grounds (1, 2A–2C)

| Basis                         | Challenged Claims                                                                                  | Arguments by PO                                                                                                                                                                                                                                                              |
|-------------------------------|----------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Anticipation<br>(Ground 1)    | 1, 3, 7, 9–12, 14, 17, 18, 20–22                                                                   | PO disputes “current set circuit” (Limitation [1.b]/[14.b]);<br>PO disputes whether PWM signal is applied to “current set circuit” (Limitation [1.d]/[14.d]);<br>PO disputes “a current regulator” (Claim 3);<br>PO disputes whether a clock is inherent in Thomas (Claim 7) |
| Obviousness<br>(Ground 2A–2C) | <b>2A:</b> 1, 3, 6, 7, 9–12, 14, 17, 18, 20–22<br><br><b>2B:</b> 2, 13, 15<br><br><b>2C:</b> 8, 19 | Legal sufficiency of arguments for Claims 1 & 14;<br>PO disputes whether <i>Thomas</i> ’s driver would be formed as an integrated circuit (Claim 13)                                                                                                                         |

## Preamble [1.pre] (Unrebutted, Grounds 1 & 2A)

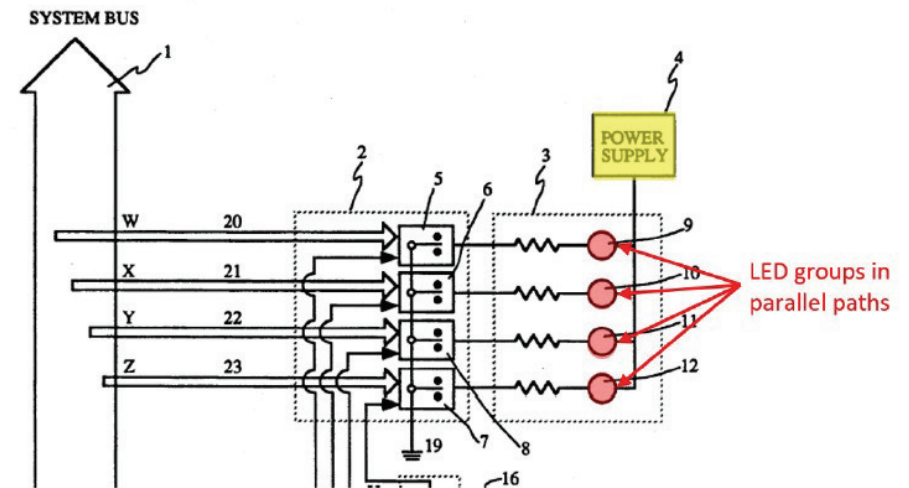
[1.pre]: “A light emitting diode (LED) driver for driving LEDs connected to different parallel paths,”



EX1005, Fig. 1 (annotated)

## Limitation [1.a] (Unrebutted, Grounds 1 & 2A)

[1.a]: “the driver comprising: a voltage source for connection to first ends of LEDs in a plurality of parallel paths”



EX1005, Fig. 1 (cropped, annotated)

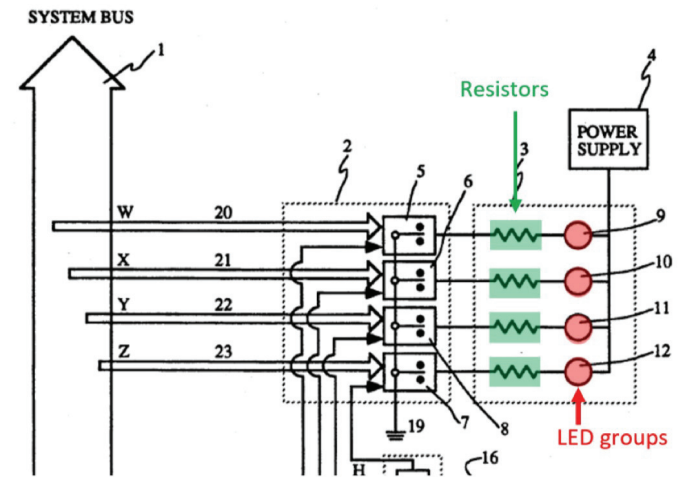
## Limitation [1.b] (Disputed, Grounds 1 & 2A)

[1.b]: “a plurality of current set circuits, one current set circuit per parallel path, each current set circuit controlling a peak current through one or more LEDs connected in each parallel path; and”

Thomas shows “a resistor in series with the LED group in each parallel path.”

Peak current:

$$I_{LED} = \frac{(V - V_{LED})}{R}$$

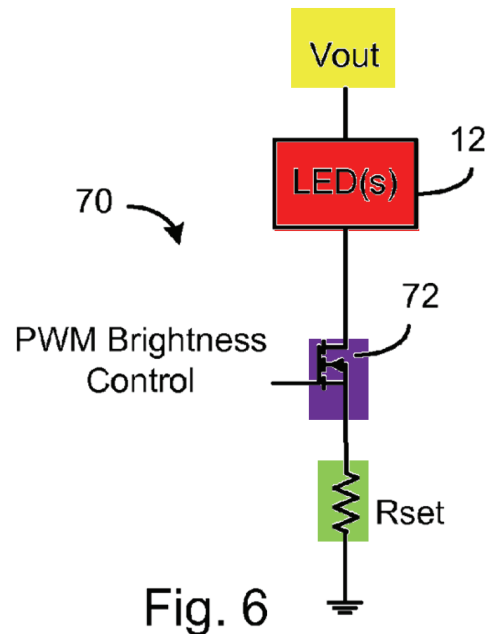


EX1005, Fig. 1 (cropped and annotated)

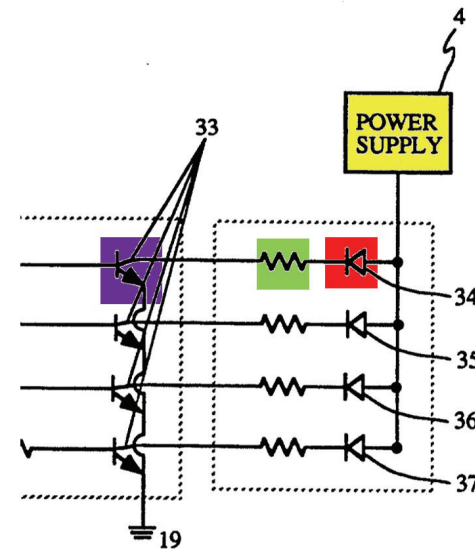
## Limitation [1.b] (Disputed, Grounds 1 & 2A)

*Thomas* discloses essentially the same current set circuit as the '148 Patent (resistor connected in series with LED(s) and other components).

'148 Patent Fig. 6

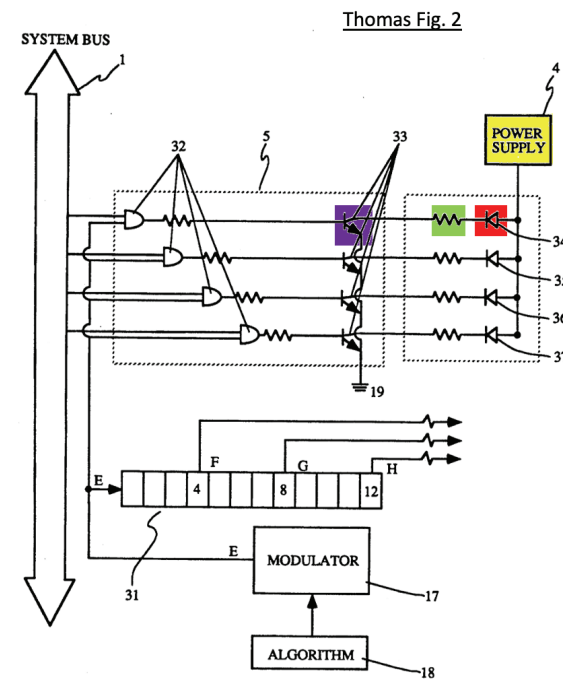
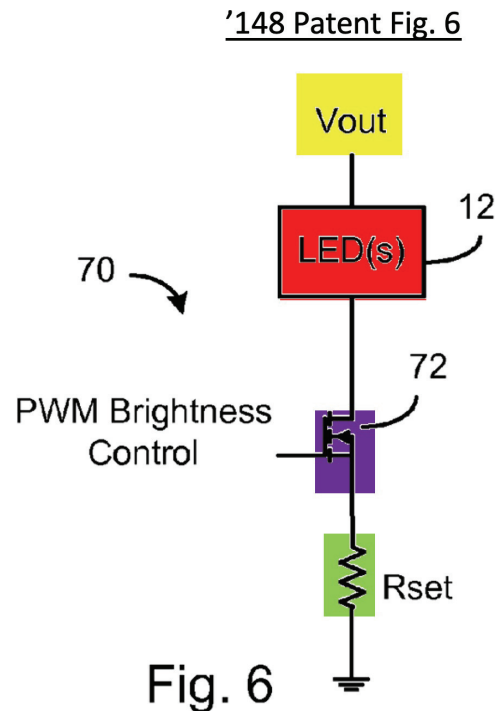


Thomas Fig. 2



## Limitation [1.b] (Disputed, Grounds 1 & 2A)

Even under PO's argument that "current set circuit" requires multiple connected components, Thomas still anticipates.



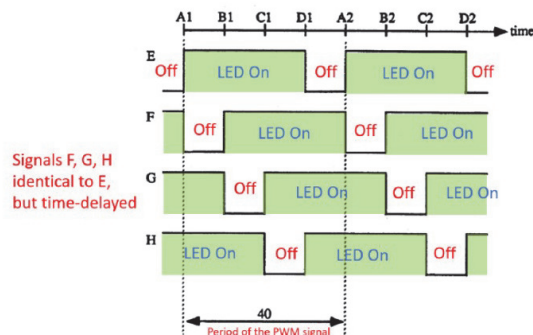
Reply, 15–16; EX1001, Fig. 6 (annotated); EX1005, Fig. 2 (annotated); EX1031, ¶¶12–13.

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# Limitation [1.c] (Unrebutted, Grounds 1 & 2A)

[1.c]: “a pulse-width modulated (PWM) brightness control signal generator connected to the plurality of current set circuits, the brightness control signal generator being configured to generate staggered PWM brightness control signals to the plurality of current set circuits,”



EX1005, Fig. 3 (annotated)

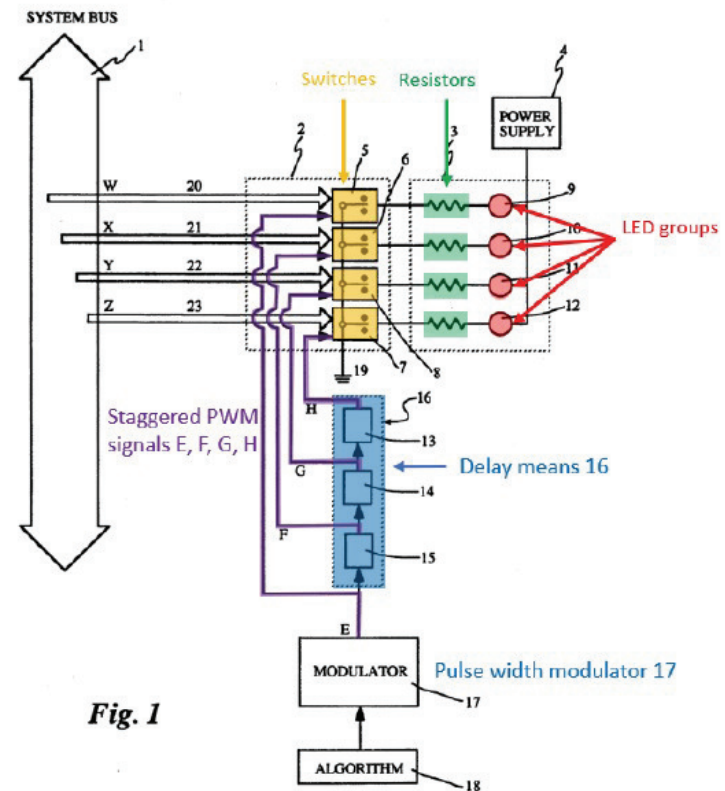


Fig. 1

EX1005, Fig. 1 (annotated)

## Limitation [1.d] (Disputed, Grounds 1 & 2A)

[1.d]: “each current set circuit being configured to draw the peak current through its associated one or more LEDs at a duty cycle substantially corresponding to a duty cycle of a PWM brightness control signal applied to it, such that the plurality of current set circuits conduct current through their associated one or more LEDs at the same duty cycle but out of phase with each other.”

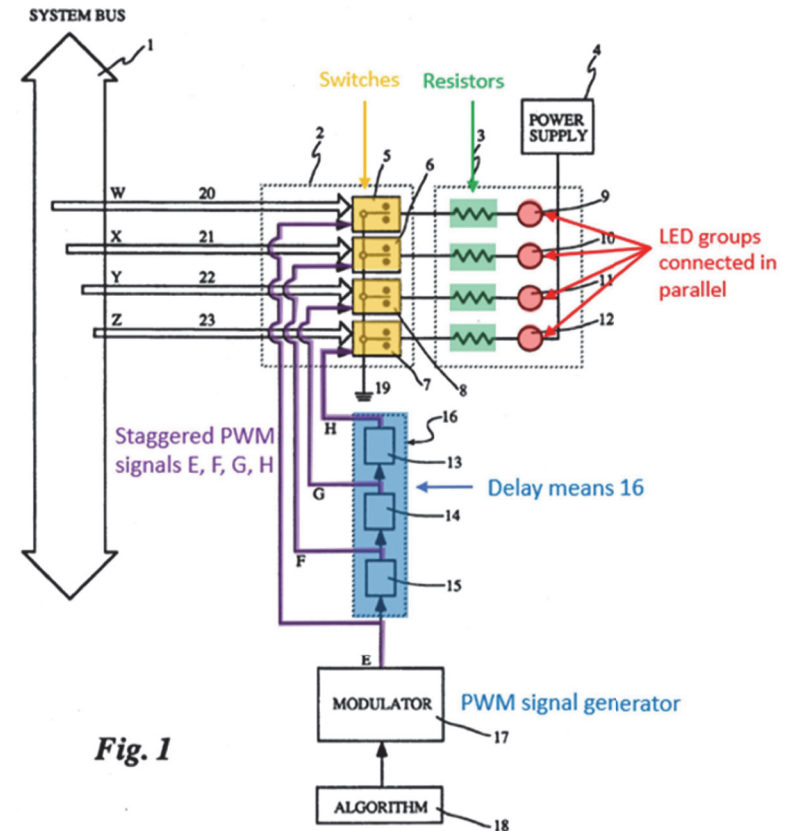


Fig. 1

EX1005 Fig. 1 (annotated)

## Petition Did Not Identify Resistors in Isolation

Petition identified “a resistor in series with the LED group in each parallel path” as the current set circuits.

As shown below, Thomas’ Figures 1 and 2 show a resistor in series with the LED group in each parallel path. EX1003, ¶62.

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Dr. Zane explained the resistors limit the current to  $I = (V - V_{LED})/R$  based on the power supply and LEDs connected to the resistors. EX1003, ¶63.

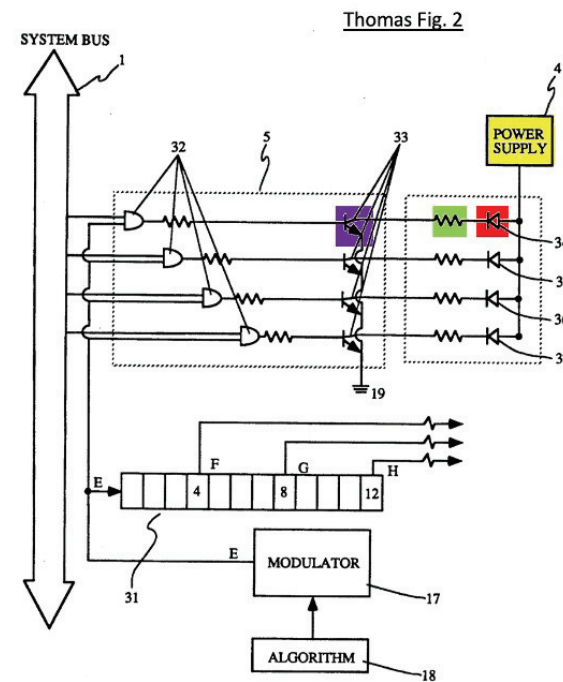
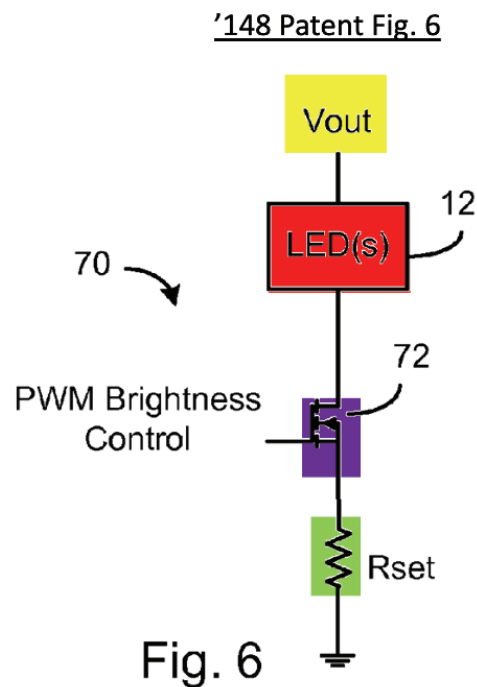
Board’s Institution Decision also recognized “a resistor in series with one or more LEDs” as a current set circuit.

Pet. 26 (citing Ex. 1003 ¶ 63). We note that the ’148 patent itself identifies a resistor in series with one or more LEDs in an LED string as a current set circuit. Ex. 1001, 6:7–13, Fig. 6.

Institution Decision, 14

## Thomas and '148 Patent Operate in the Same Way

Thomas's driver behaves the same way as the '148 Patent—applying the PWM brightness control signal to a transistor connected to a current set resistor.



Reply, 17–18; EX1031, ¶¶15–16; EX1001, Fig. 6 (annotated); EX1005, Fig. 2 (annotated)

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## Limitation [1.d] (Disputed, Grounds 1 & 2A)

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Based on PO's argument that "current set circuit" requires multiple connected components, Thomas applies a PWM signal to multiple connected components (switch + resistor).

- "Thomas still discloses the same current set circuit as in Figure 6 of the '148 Patent, namely a resistor and switch connected in series with each other." EX1031, ¶17.
- "Thomas indisputably applies the PWM signal directly to the current set circuit because Thomas applies the PWM signal to the switch." *Id.*

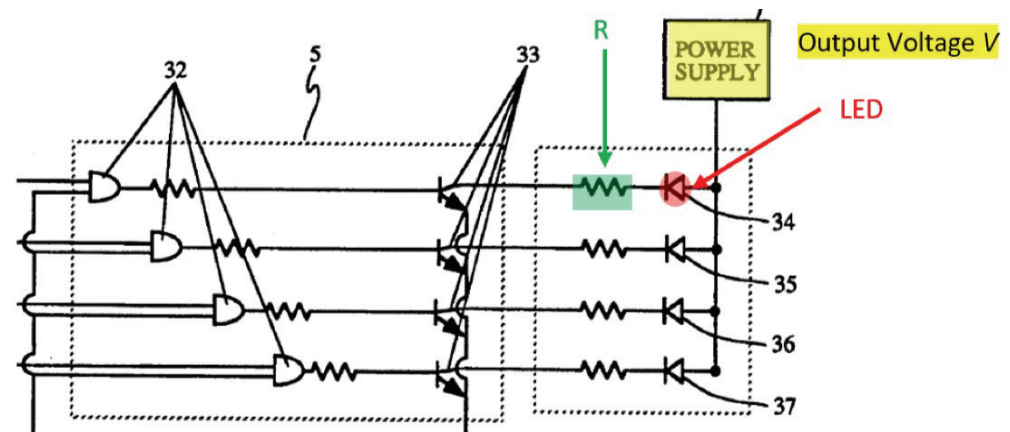
## Claim 3 (Disputed, Grounds 1 & 2A)

Claim 3: “The driver of claim 1 wherein each current set circuit is a current regulator.”

No need to address this dispute because PO did not rebut that *Zane* discloses Claim 3 in Grounds 3 & 4.

Thomas discloses a regulated voltage.

Regulated voltage + resistor → regulated current



EX1005, Fig. 2 (annotated)

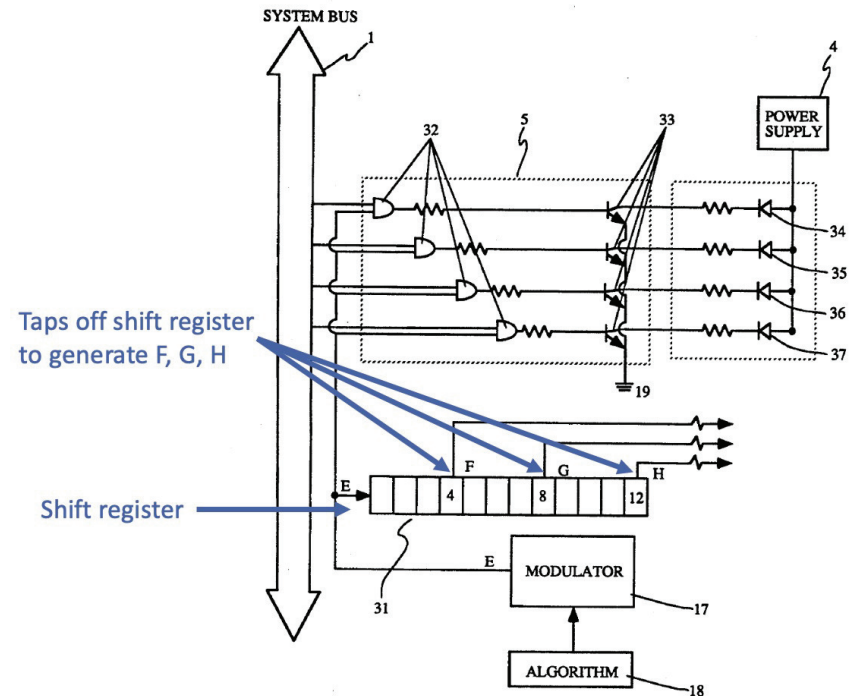
## Claim 7 (Disputed, Grounds 1 & 2A)

[7.pre] (Unrebutted): "The driver of claim 1 wherein the PWM brightness control signal generator comprises:"

[7.a] (Unrebutted): "a shift register storing bits corresponding to a PWM duty cycle of a brightness control signal, the shift register having bit positions;"

[7.b] **(Disputed)**: "a clock connected to the shift register for shifting the bits along the shift register; and"

[7.c] (Unrebutted): "taps off the shift register coupled to different bit positions of the shift register, each tap providing a different staggered PWM brightness control signal connected to an associated current set circuit."



EX1005, Fig. 2 (annotated)

## Limitation [7.b] (Disputed, Grounds 1 & 2A)

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[7.b] (**Disputed**): “a clock connected to the shift register for shifting the bits along the shift register; and”

A clock is inherent in Thomas’s shift register.

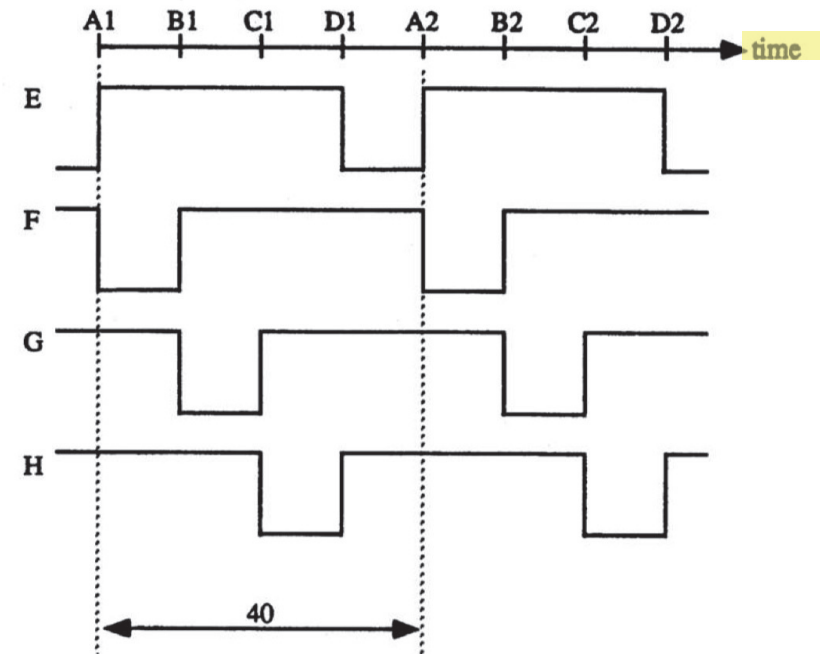
Dr. Zane: A clock in this context is “an electronic circuit that can output a current or voltage pulse at predictable times.” EX1003, ¶76.

## Claim 7 (Disputed, Grounds 1 & 2A)

Thomas's shift register necessarily includes a clock for shifting the bits.

Thomas's shift register continuously generates delayed signals F, G, H based on E. The shift register must be shifting the bits synchronously with each new pulse/lack of pulse from E.

Thomas's shift register receives a shift pulse at predictable times → Clock must be present



EX1005, Fig. 3 (annotated)

## Claim 7 (Disputed, Grounds 1 & 2A)

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PO's arguments do not apply to Thomas:

- PO did not argue Thomas's shift register could be implemented without a clock.
- PO's reference to asynchronous shift register is irrelevant because Thomas's shift register is synchronous with the PWM signal E.
- PO's reference to dynamic shift register is irrelevant because Thomas's shift register shifts synchronously with the PWM signal E—thus, there is a clock signal.

## Claim 13 (Disputed, Ground 2B)

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Claim 13: “The driver of claim 1 wherein the driver is formed as an integrated circuit.”

Board need not address this dispute—PO conceded Claim 13 in *Zane* grounds.

PO mischaracterized the Petition as not arguing the entirety of Thomas’s driver would be implemented as an integrated circuit.

Petition explained: “[I]t would have been obvious to a POSITA to implement [Thomas’s] driver, or the majority of the driver, as an integrated circuit.”

## Claim 14 (Disputed, Grounds 1 & 2A)

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- Claim 14 is a method claim corresponding to Claim 1
- Claim 14 is anticipated/rendered obvious by Thomas for same reasons as Claim 1

---

# Additional Claims (Thomas Grounds)

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## Claim 2 (Unrebutted, Ground 2B)

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Claim 2: “The driver of claim 1 wherein the voltage source is a step up voltage regulator.”

- “Thomas expressly discloses that the invention is especially useful for “switching power supplies,” and a step-up voltage regulator is one of two very well-known options for a switching power supply (step up or step down).” EX1003, ¶121
- “[A] POSITA would have been motivated to implement a step-up voltage regulator to boost the voltage source in Thomas, if the input voltage is lower than the required voltage to energize the LEDs.” EX1003, ¶123

## Claim 6 (Unrebutted, Ground 2A)

[6.pre]: “The driver of claim 1 wherein each current set circuit comprises:”

[6.a]: “a **current set resistor** in series with one or more **LEDs** in an associated parallel path; and”

[6.b]: “a PWM brightness control transistor connected in series between the current set resistor and the one or more LEDs in an associated parallel path, the PWM brightness control transistor being connected to the PWM brightness control signal generator for receiving a staggered PWM brightness control signal.

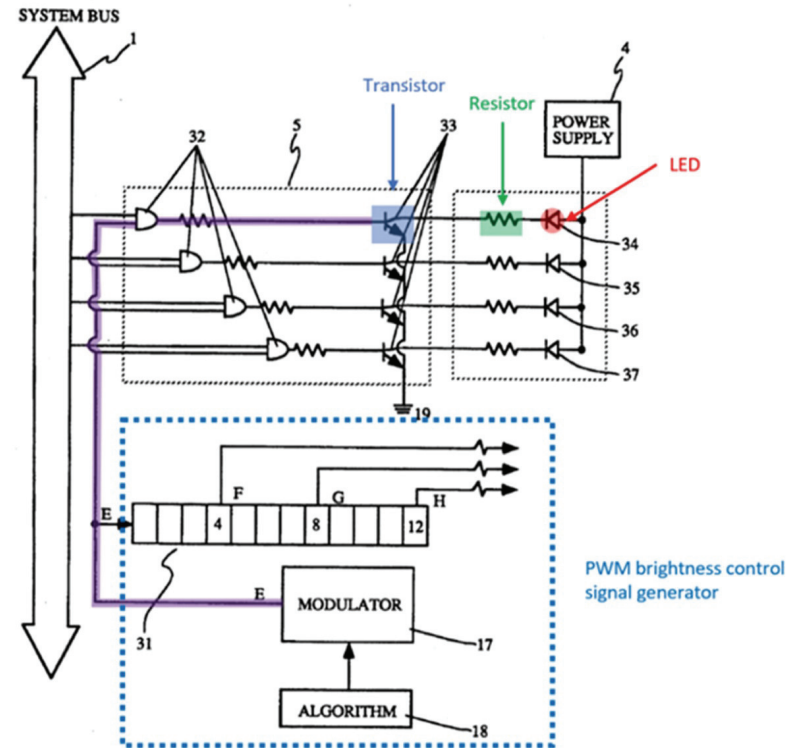


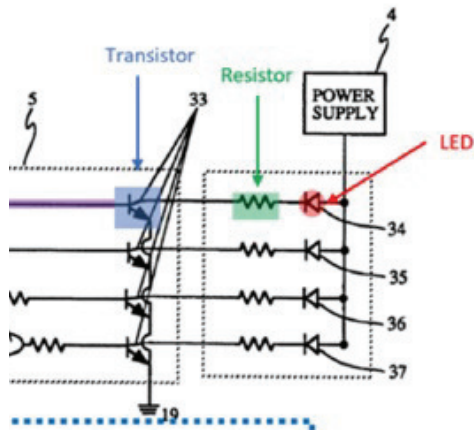
**Fig. 2**

EX1005, Fig. 2 (annotated)

## Claim 6 (Unrebutted, Ground 2A)

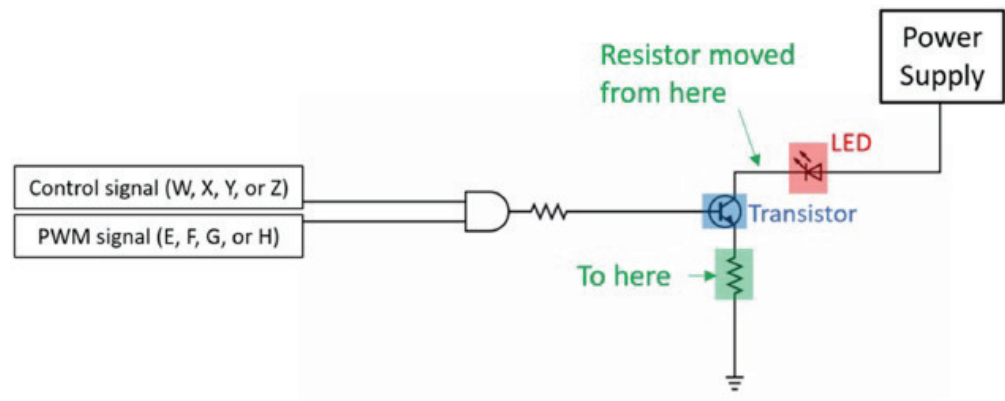
Thomas does not disclose a transistor “in series between the current set resistor and the one or more LEDs” but this would have been an obvious design choice from six possibilities. PO offered no rebuttal.

### Thomas: LED-Resistor-Transistor



EX1005, Fig. 2 (cropped, annotated)

### Claim 6: LED-Transistor-Resistor

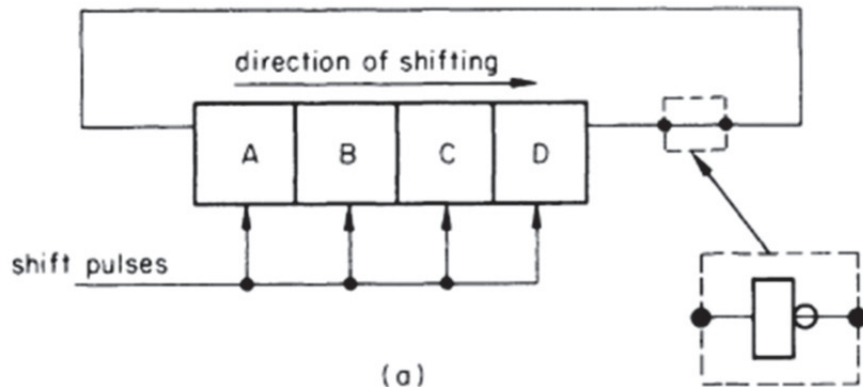


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## Claim 8 (Unrebutted, Ground 2C)

Claim 8: “The driver of claim 7 wherein the shift register has a connection that connects an end bit position to a first bit position so that bits in the shift register are recirculated in the shift register.”

Recirculating shift registers were known as “ring counters” in the art. Tatewaki (EX1007) discloses the use of a ring counter in an LED driver.



EX1011, 119

First of all, each time the on-off switch **163** is activated, a **ring counter** installed in the PWM control circuit **162** operates so that a duration of the on and off of the LED chip **132, 142** is changed, thereby controlling the brightness.

EX1007, 13:35–38

## Claim 9 (Unrebutted, Grounds 1 & 2A)

Claim 9: “The driver of claim 7 wherein the bits corresponding to a PWM duty cycle of a brightness control signal are serially and continuously loaded into a first bit position of the shift register, and then shifted by the clock.”

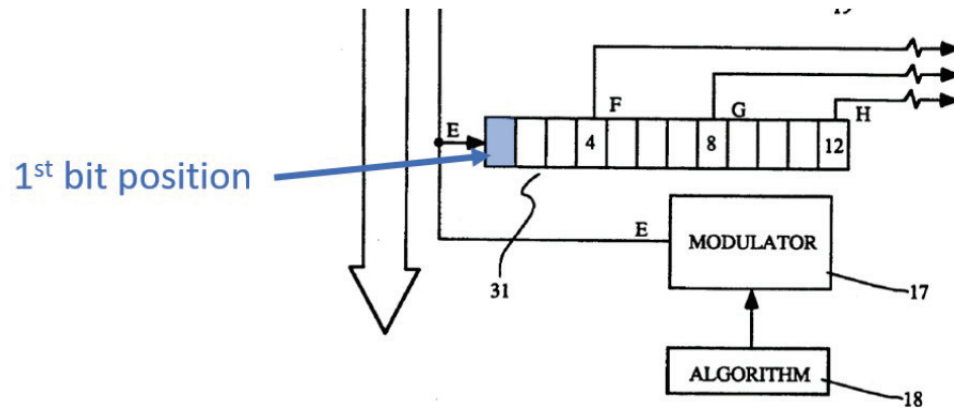


**Fig. 2**

EX1005, Fig. 2 (cropped, annotated)

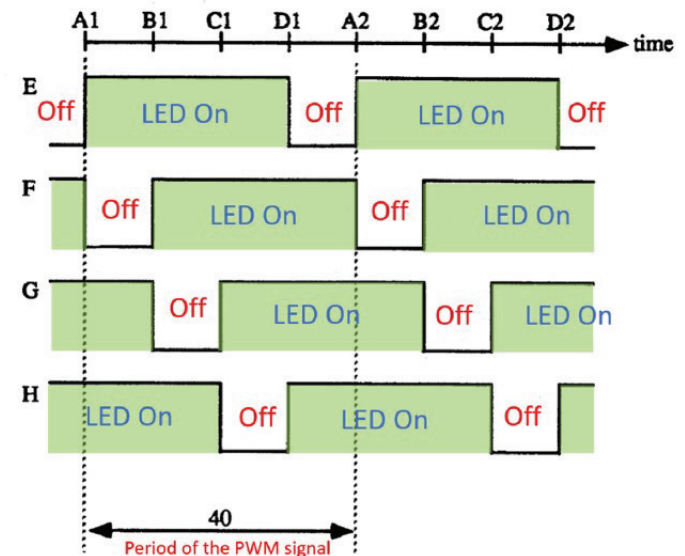


**Fig. 3**

EX1005, Fig. 3 (annotated)

## Claim 10 (Unrebutted, Grounds 1 & 2A)

Claim 10: “The driver of claim 7 wherein the clock shifts the bits at a rate equal to N times a frequency of the PWM brightness control signal, where N equals the number of bits representing a single PWM duty cycle.”

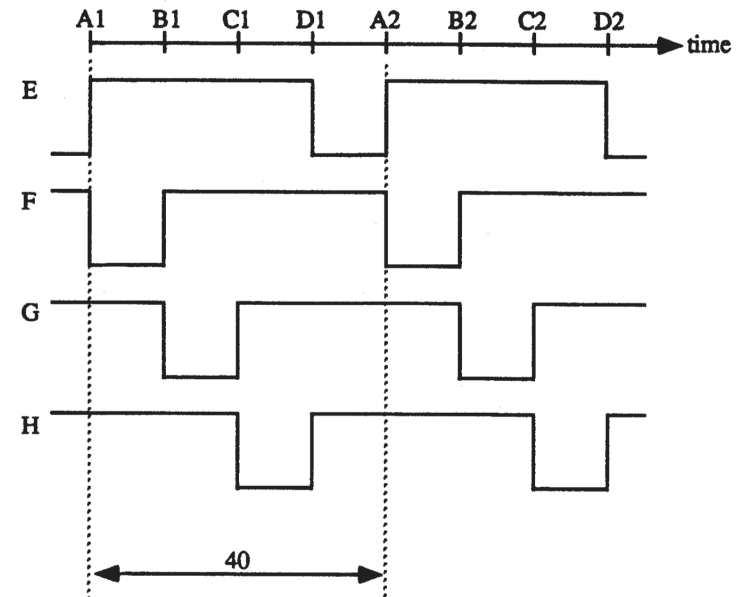
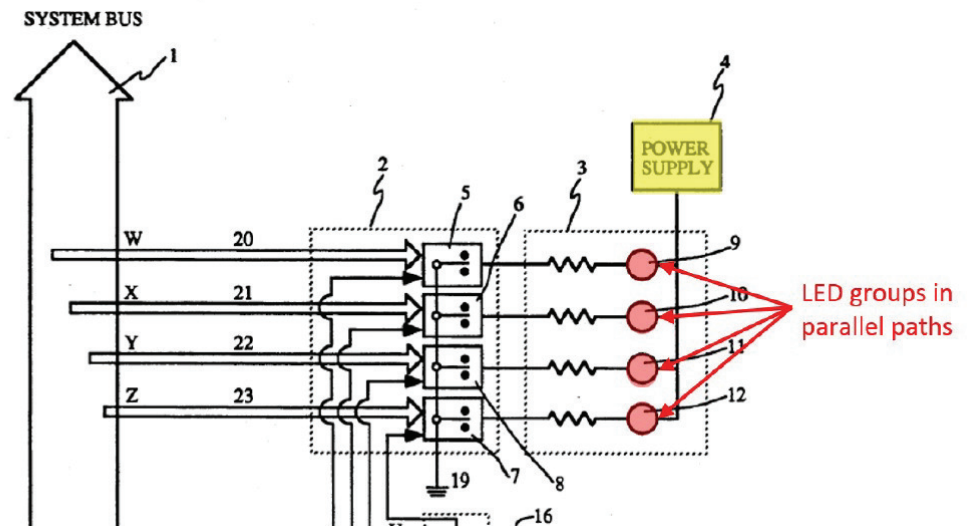


**Fig. 3**

## Claim 11 (Unrebutted, Grounds 1 & 2A)

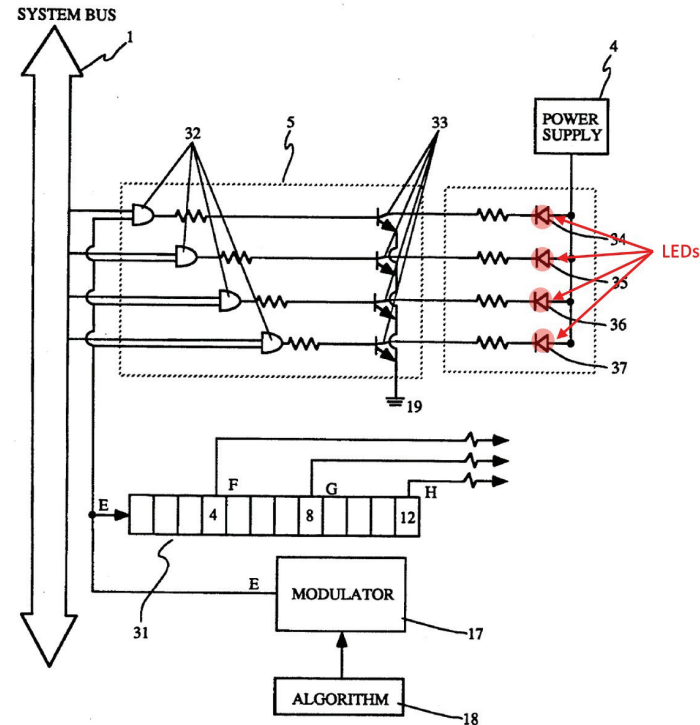
Claim 11: “The driver of claim 1 wherein the plurality of parallel paths comprises at least three paths.”



EX1005, Fig. 1 (cropped, annotated)

## Claim 12 (Unrebutted, Grounds 1 & 2A)

Claim 12: “The driver of claim 1 further comprising the LEDs connected to the driver.”



EX1005, Fig. 2 (annotated)

## Claim 15 (Unrebutted, Ground 2B)

---

Claim 15: “The method of claim 14 further comprising varying the duty cycle of the staggered PWM brightness control signals to change an average current through the parallel paths of LEDs to change a perceived brightness of the LEDs.”

- Thomas discloses using PWM “[t]o control the intensity of the LED’s within the array” EX1005, 1:23–42.
- ’148 Patent admits that using PWM to control the average current through an LED was known.
- A POSITA would have understood that a duty cycle of X% corresponds to an average current that is X% of the peak current.

## Claim 17 (Unrebutted, Grounds 1 & 2A)

Claim 17: “The method of claim 14 wherein applying a different staggered PWM brightness control signal to each current set circuit comprises applying each staggered PWM brightness control signals to an associated transistor connected in series with the one or more LEDs in an associated parallel path, such that the transistor is turned on and off corresponding to the duty cycle of the staggered PWM brightness control signal applied to it.”

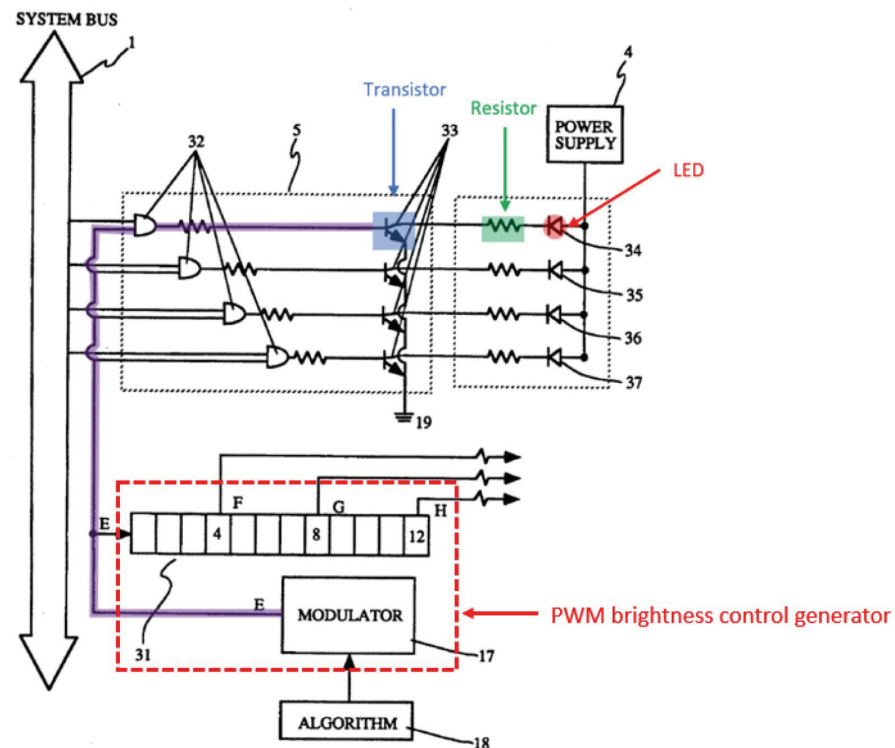


**Fig. 2**

EX1005, Fig. 2 (annotated)

## Claims 18, 20, 21, 22 (Unrebutted)

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### Claim 18 (Grounds 1 & 2A)

- Thomas anticipates/renders obvious Claim 18 for same reasons as Claim 7. EX1003, ¶¶ 98–101

### Claim 19 (Ground 2C)

- Thomas renders obvious Claim 19 for same reasons as Claim 8. EX1003, ¶¶ 146

### Claim 20 (Grounds 1 & 2A)

- Thomas anticipates/renders obvious Claim 20 for same reasons as Claim 9. EX1003, ¶ 102

### Claim 21 (Grounds 1 & 2A)

- Thomas anticipates/renders obvious Claim 21 for same reasons as Claim 10. EX1003, ¶ 103

### Claim 22 (Grounds 1 & 2A)

- Thomas anticipates/renders obvious Claim 22 for same reasons as Claim 11. EX1003, ¶ 104.

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# Appendix

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# Claim 1

|                  |                                                                                                                                                                                                                                                                                                                                                                                             |
|------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Preamble [1.pre] | A light emitting diode (LED) driver for driving LEDs connected to different parallel paths,                                                                                                                                                                                                                                                                                                 |
| Limitation [1.a] | the driver comprising: a voltage source for connection to first ends of LEDs in a plurality of parallel paths;                                                                                                                                                                                                                                                                              |
| Limitation [1.b] | a plurality of current set circuits, one current set circuit per parallel path, each current set circuit controlling a peak current through one or more LEDs connected in each parallel path; and                                                                                                                                                                                           |
| Limitation [1.c] | a pulse-width modulated (PWM) brightness control signal generator connected to the plurality of current set circuits, the brightness control signal generator being configured to generate staggered PWM brightness control signals to the plurality of current set circuits,                                                                                                               |
| Limitation [1.d] | each current set circuit being configured to draw the peak current through its associated one or more LEDs at a duty cycle substantially corresponding to a duty cycle of a PWM brightness control signal applied to it, such that the plurality of current set circuits conduct current through their associated one or more LEDs at the same duty cycle but out of phase with each other. |

# Claim 2

---

|         |                                                                                  |
|---------|----------------------------------------------------------------------------------|
| Claim 2 | The driver of claim 1 wherein the voltage source is a step up voltage regulator. |
|---------|----------------------------------------------------------------------------------|

# Claim 3

---

|         |                                                                                |
|---------|--------------------------------------------------------------------------------|
| Claim 3 | The driver of claim 1 wherein each current set circuit is a current regulator. |
|---------|--------------------------------------------------------------------------------|

# Claim 4

---

|                  |                                                                                                                                                                                                                                                                   |
|------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Preamble [4.pre] | The driver of claim 1 wherein each current set circuit is a current regulator comprising:                                                                                                                                                                         |
| Limitation [4.a] | a current control transistor in series with one or more LEDs in an associated parallel path; and                                                                                                                                                                  |
| Limitation [4.b] | a feedback circuit connected to detect a current through the parallel path and connected to the current control transistor to control a conductivity of the current control transistor to cause the current through the parallel path to match a reference level. |

## Claim 5

|                  |                                                                                                                                                                                                                                                                                                                                     |
|------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Preamble [5.pre] | The driver of claim 4 wherein each current set circuit further comprises                                                                                                                                                                                                                                                            |
| Limitation [5.a] | a PWM brightness control transistor connected between an output of the feedback circuit and a control terminal of the current control transistor,                                                                                                                                                                                   |
| Limitation [5.b] | the PWM brightness control transistor being connected to the PWM brightness control signal generator for receiving a staggered PWM brightness control signal to couple the output of the feedback circuit to the control terminal of the current control transistor at a duty cycle of the staggered PWM brightness control signal. |

## Claim 6

---

|                  |                                                                                                                                                                                                                                                                                                                 |
|------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Preamble [6.pre] | The driver of claim 1 wherein each current set circuit comprises:                                                                                                                                                                                                                                               |
| Limitation [6.a] | a current set resistor in series with one or more LEDs in an associated parallel path; and                                                                                                                                                                                                                      |
| Limitation [6.b] | a PWM brightness control transistor connected in series between the current set resistor and the one or more LEDs in an associated parallel path, the PWM brightness control transistor being connected to the PWM brightness control signal generator for receiving a staggered PWM brightness control signal. |

## Claim 7

---

|                  |                                                                                                                                                                                                              |
|------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Preamble [7.pre] | The driver of claim 1 wherein the PWM brightness control signal generator comprises:                                                                                                                         |
| Limitation [7.a] | a shift register storing bits corresponding to a PWM duty cycle of a brightness control signal, the shift register having bit positions;                                                                     |
| Limitation [7.b] | a clock connected to the shift register for shifting the bits along the shift register; and                                                                                                                  |
| Limitation [7.c] | taps off the shift register coupled to different bit positions of the shift register, each tap providing a different staggered PWM brightness control signal connected to an associated current set circuit. |

# Claim 8

---

|         |                                                                                                                                                                                                        |
|---------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Claim 8 | The driver of claim 7 wherein the shift register has a connection that connects an end bit position to a first bit position so that bits in the shift register are recirculated in the shift register. |
|---------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

## Claim 9

---

|         |                                                                                                                                                                                                                          |
|---------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Claim 9 | The driver of claim 7 wherein the bits corresponding to a PWM duty cycle of a brightness control signal are serially and continuously loaded into a first bit position of the shift register, then shifted by the clock. |
|---------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

## Claim 10

---

|          |                                                                                                                                                                                                              |
|----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Claim 10 | The driver of claim 7 wherein the clock shifts the bits at a rate equal to N times a frequency of the PWM brightness control signal, where N equals the number of bits representing a single PWM duty cycle. |
|----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

## Claim 11

---

|          |                                                                                               |
|----------|-----------------------------------------------------------------------------------------------|
| Claim 11 | The driver of claim 1 wherein the plurality of parallel paths comprises at least three paths. |
|----------|-----------------------------------------------------------------------------------------------|

## Claim 12

---

|          |                                                                            |
|----------|----------------------------------------------------------------------------|
| Claim 12 | The driver of claim 1 further comprising the LEDs connected to the driver. |
|----------|----------------------------------------------------------------------------|

## Claim 13

---

|          |                                                                              |
|----------|------------------------------------------------------------------------------|
| Claim 13 | The driver of claim 1 wherein the driver is formed as an integrated circuit. |
|----------|------------------------------------------------------------------------------|

## Claim 14

|                   |                                                                                                                                                                                                                                                                                                                                                   |
|-------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Preamble [14.pre] | A method for driving light emitting diodes (LEDs) connected to different parallel paths, the method comprising:                                                                                                                                                                                                                                   |
| Limitation [14.a] | supplying a voltage to first ends of LEDs in a plurality of parallel paths;                                                                                                                                                                                                                                                                       |
| Limitation [14.b] | setting a peak current through one or more LEDs connected in each of the parallel paths, the peak current being set by a current set circuit for each parallel path;                                                                                                                                                                              |
| Limitation [14.c] | generating staggered pulse width modulated (PWM) brightness control signals;                                                                                                                                                                                                                                                                      |
| Limitation [14.d] | applying a different staggered PWM brightness control signals to each current set circuit; and                                                                                                                                                                                                                                                    |
| Limitation [14.e] | drawing the peak current through the one or more LEDs in each parallel path, set by its associated current set circuit, at a duty cycle corresponding to a duty cycle of an associated PWM brightness control signal, such that the parallel paths of LEDs conduct current at substantially the same duty cycle but out of phase with each other. |

## Claim 15

---

|          |                                                                                                                                                                                                                                |
|----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Claim 15 | The method of claim 14 further comprising varying the duty cycle of the staggered PWM brightness control signals to change an average current through the parallel paths of LEDs to change a perceived brightness of the LEDs. |
|----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

## Claim 16

|                   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Preamble [16.pre] | The method of claim 14                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| Limitation [16.a] | wherein setting a peak current through one or more LEDs connected in each of the parallel paths comprises setting the peak current by controlling conductivity of a current control transistor in series with each parallel path, and                                                                                                                                                                                                                                                                 |
| Limitation [16.b] | wherein applying a different staggered PWM brightness control signal to each current set circuit comprises: coupling each staggered PWM brightness control signal to a control terminal of an associated pass transistor, each pass transistor being connected between a control terminal of a respective current control transistor and a regulating control voltage, such that the current control transistor is turned on and off corresponding to a duty cycle of the associated pass transistor. |

## Claim 17

---

|          |                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Claim 17 | The method of claim 14 wherein applying a different staggered PWM brightness control signal to each current set circuit comprises applying each staggered PWM brightness control signals to an associated transistor connected in series with the one or more LEDs in an associated parallel path, such that the transistor is turned on and off corresponding to the duty cycle of the staggered PWM brightness control signal applied to it. |
|----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

## Claim 18

---

|                   |                                                                                                                                                                                                                     |
|-------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Preamble [18.pre] | The method of claim 14 wherein generating staggered PWM brightness control signals comprises:                                                                                                                       |
| Limitation [18.a] | storing bits corresponding to a PWM duty cycle of a brightness control signal in a shift register, the shift register having bit positions;                                                                         |
| Limitation [18.b] | shifting the bits along the shift register under control of a clock; and                                                                                                                                            |
| Limitation [18.c] | receiving bits tapped off the shift register at different bit positions of the shift register to generate a different staggered PWM brightness control signal from the bits at each of the different bit positions. |

## Claim 19

---

|          |                                                                                                                                                                                  |
|----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Claim 19 | The method of claim 18 further comprising recirculating bits in the shift register by feeding a bit at an output bit position to an input bit position along the shift register. |
|----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

## Claim 20

---

|          |                                                                                                                                                                                                                                      |
|----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Claim 20 | The method of claim 18 further comprising serially and continuously loading bits corresponding to a PWM duty cycle of a brightness control signal into a first bit position the shift register, then shifting the bits by the clock. |
|----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

## Claim 21

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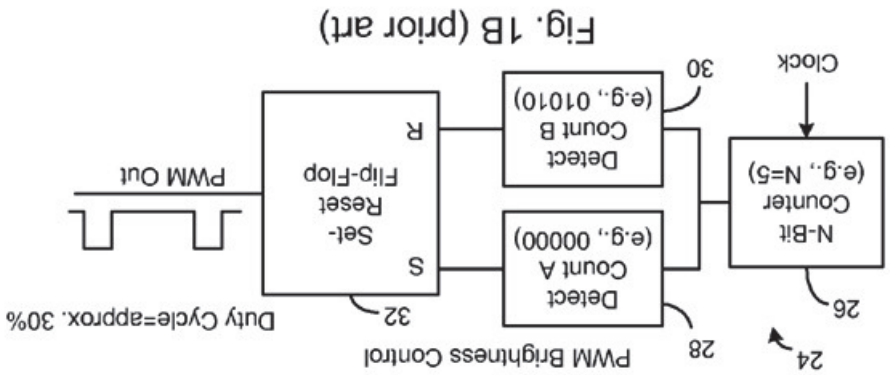
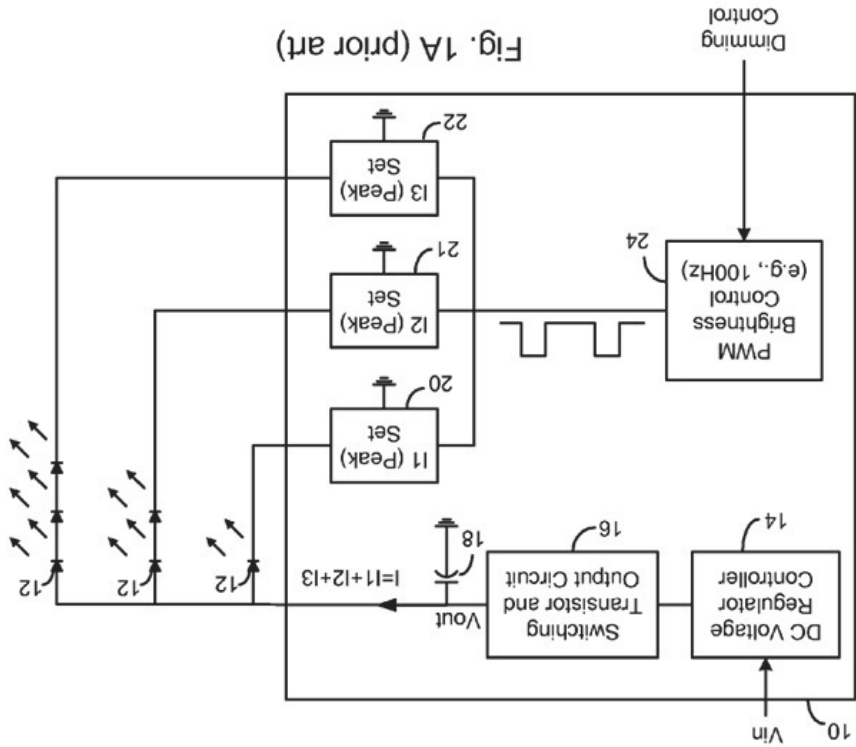
|          |                                                                                                                                                                                                             |
|----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Claim 21 | The method of claim 18 wherein the clock shifts the bits at a rate equal to N times a frequency of the PWM brightness control signal, where N equals the number of bits representing single PWM duty cycle. |
|----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

## Claim 22

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|          |                                                                                                |
|----------|------------------------------------------------------------------------------------------------|
| Claim 22 | The method of claim 14 wherein the plurality of parallel paths comprises at least three paths. |
|----------|------------------------------------------------------------------------------------------------|

## '148 Patent (EX1001) Figs. 1A-1B



## '148 Patent (EX1001) Figs. 2A-2B

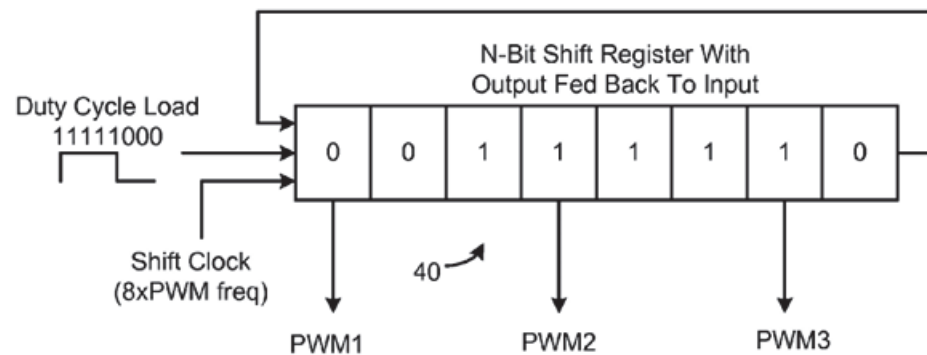


Fig. 2A

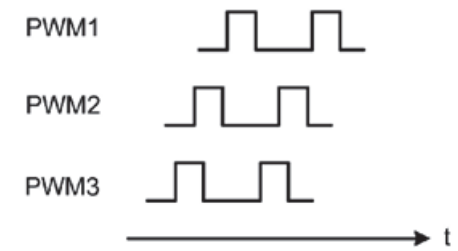


Fig. 2B

## '148 Patent (EX1001) Fig. 3

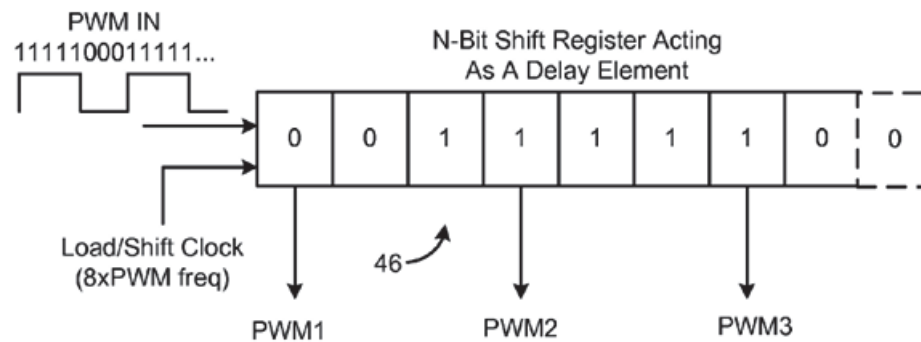


Fig. 3

## '148 Patent (EX1001) Fig. 4

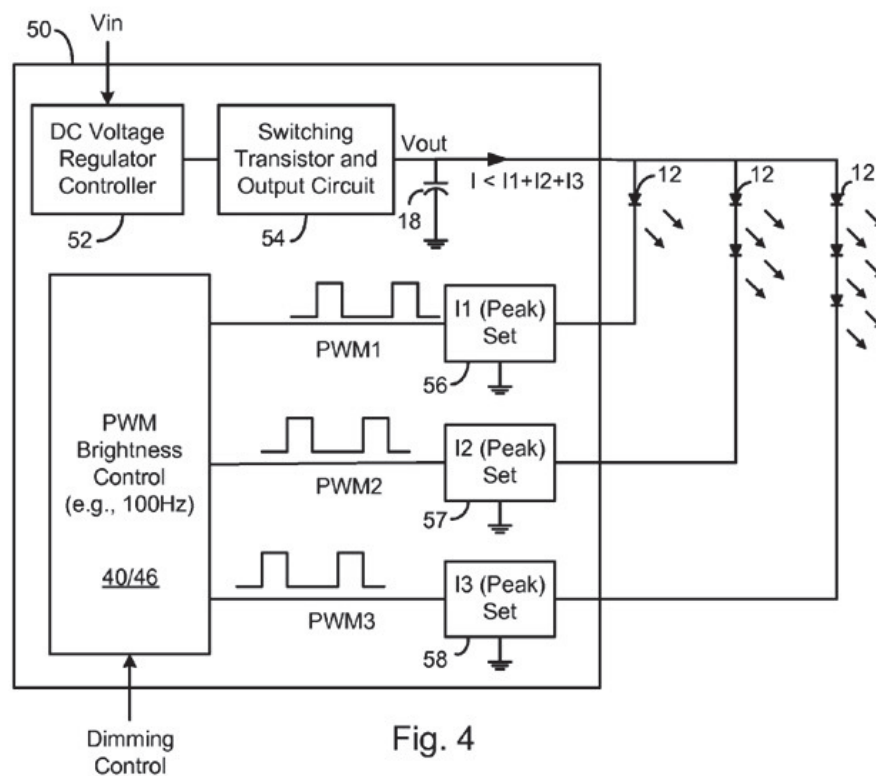
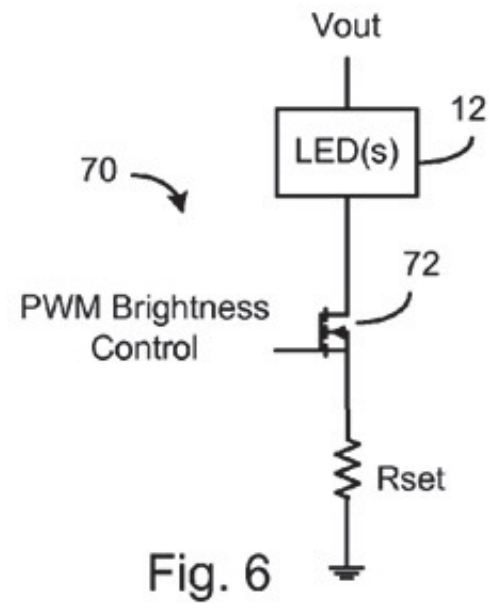
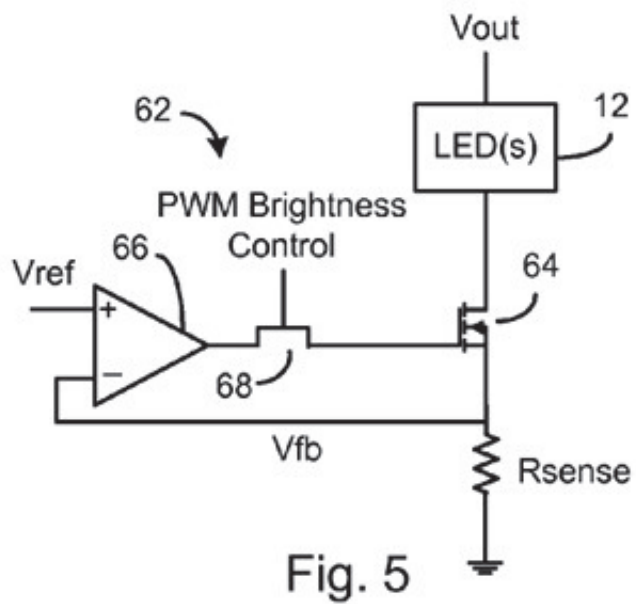


Fig. 4

DEMONSTRATIVE EXHIBIT  
NOT EVIDENCE

95

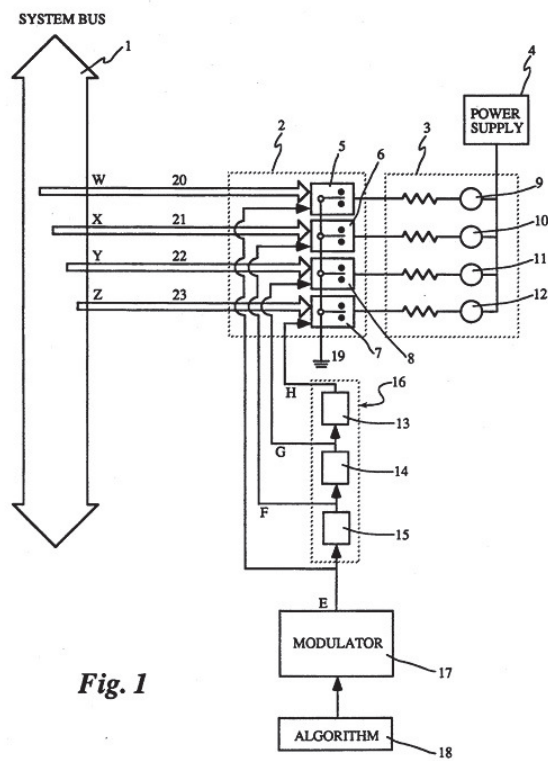
## '148 Patent (EX1001) Figs. 5 and 6



DEMONSTRATIVE EXHIBIT  
NOT EVIDENCE

96

# Thomas (EX1005) Fig. 1



DEMONSTRATIVE EXHIBIT  
NOT EVIDENCE

97

# Thomas (EX1005) Fig. 2

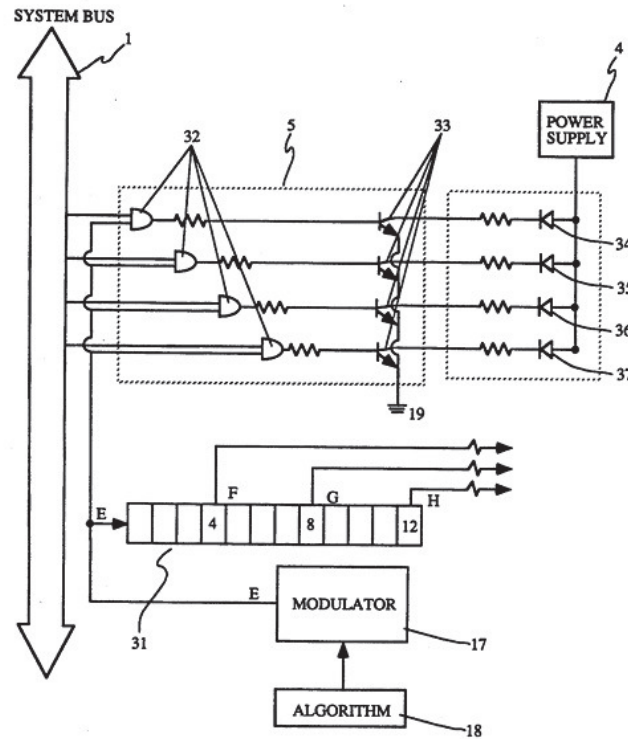


**Fig. 2**

## Thomas (EX1005) Fig. 3

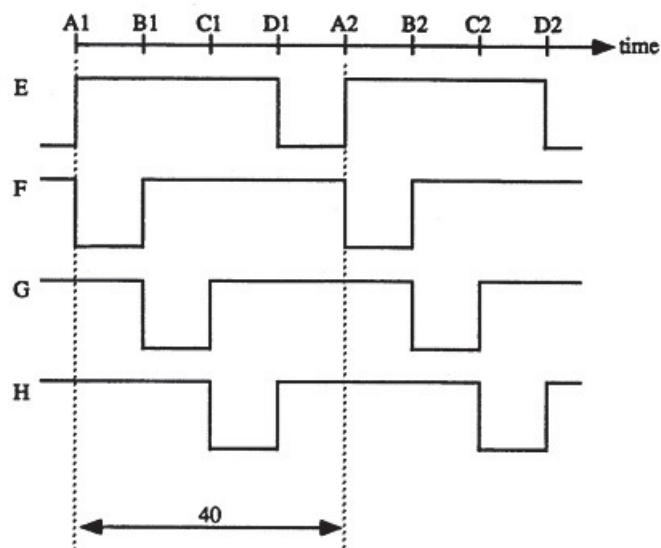
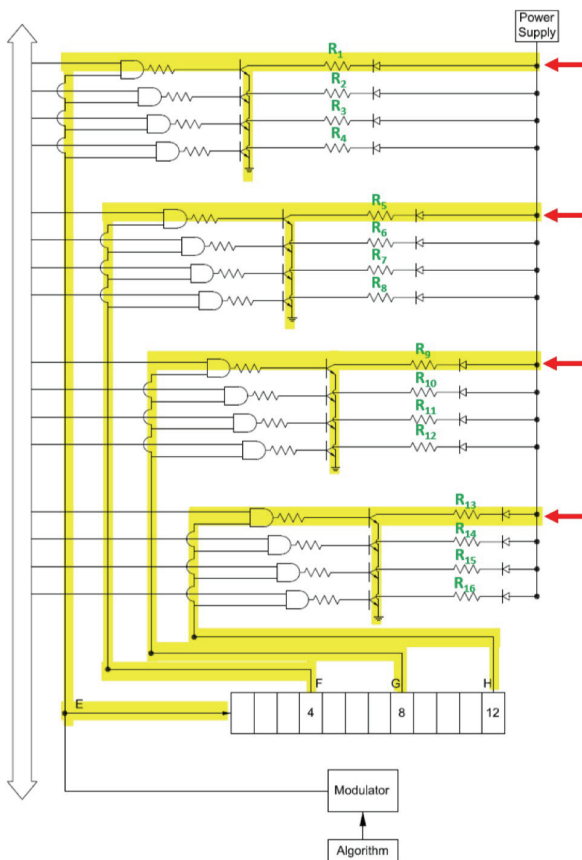


**Fig. 3**

## Expanded Version of Thomas Figure 2



## Zane (EX1006) Fig. 1

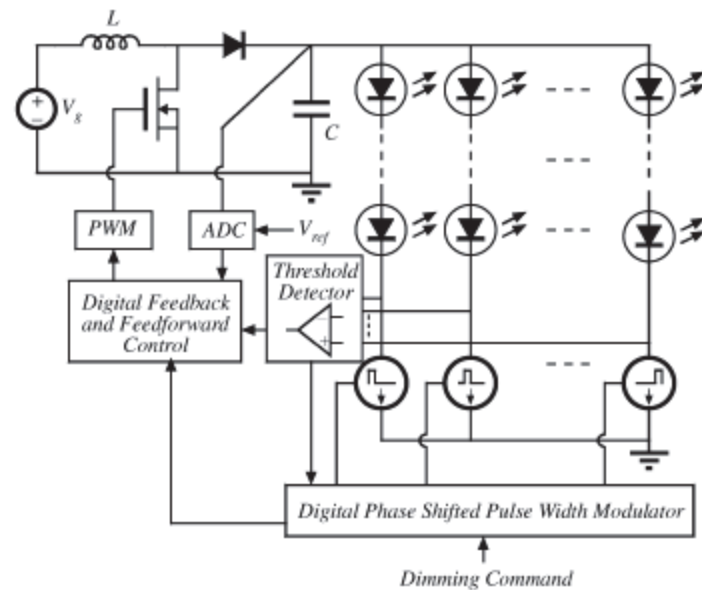


**Figure 1.** Proposed digital architecture for driving a scalable number of parallel LED strings. The approach integrates both converter control and current regulation of each LED string to facilitate system level optimization.

## Zane (EX1006) Figs. 2A-2B

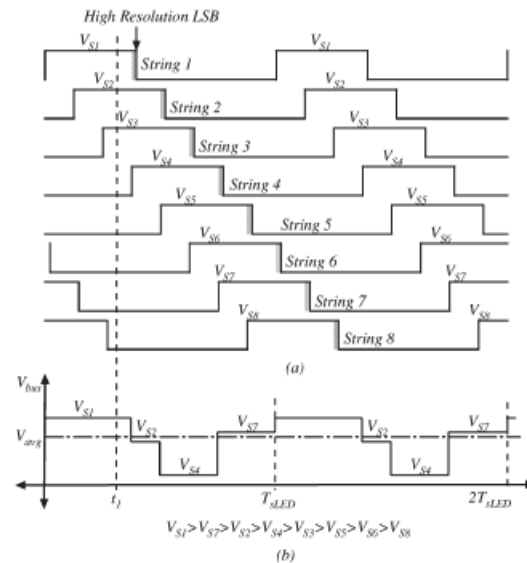


**Figure 2(a).** PS-PWM operating waveforms at 40% dimming command ( $Dim=0110\_0110$  {102},  $MSB = 011$  {3},  $LSB = 0\_0110$  {6}) illustrating the phase rotation, with three LED strings 'on' at a given time and the LSB output (shaded area) added to end of each MSB to generate required resolution.

**Figure 2(b).** Diagram illustrating dynamic bus voltage regulation where the bus voltage is scaled to a value corresponding to the maximum voltage drop across LED strings in regulation.

*Zane* (EX1006) Fig. 3

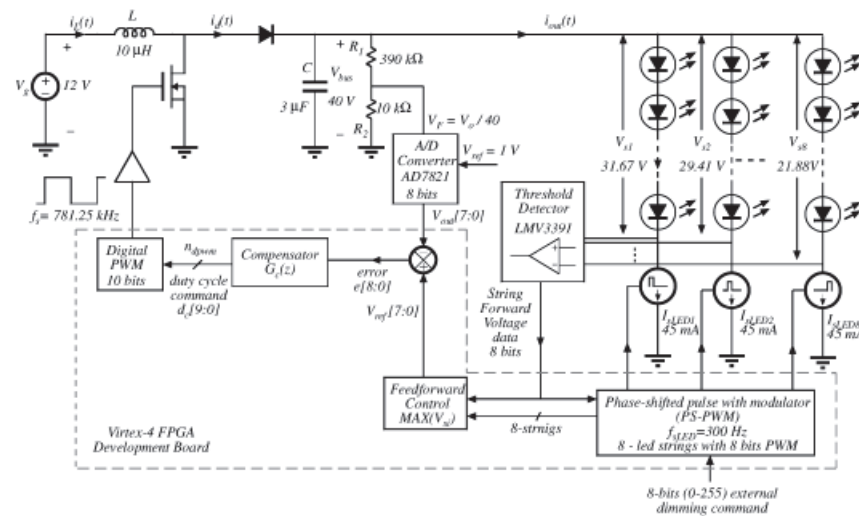


**Figure 3.** Experimental setup, consisting of a 15 W boost converter, 64 Osram MULTILEDs, linear programmable current regulator, 8-bit half-flash ADC, comparator based threshold detector circuit and digital PS-PWM and control logic implemented on Virtex-4 FPGA

## Zane (EX1006) Fig. 4

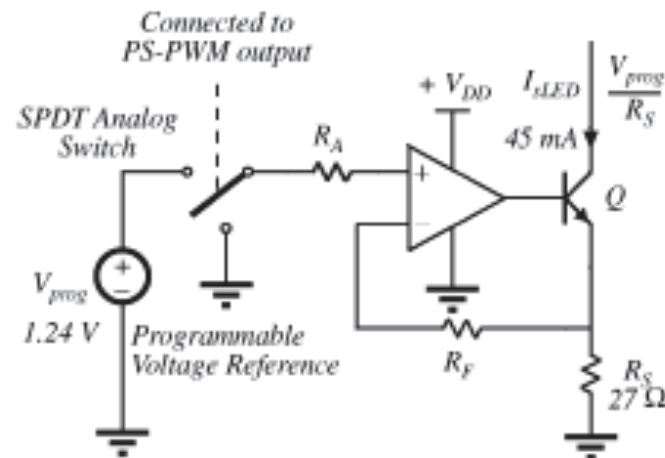


**Figure. 4.** An op-amp based precision programmable current sink with AM and PWM control options

## Zane (EX1006) Figs. 5 and 6

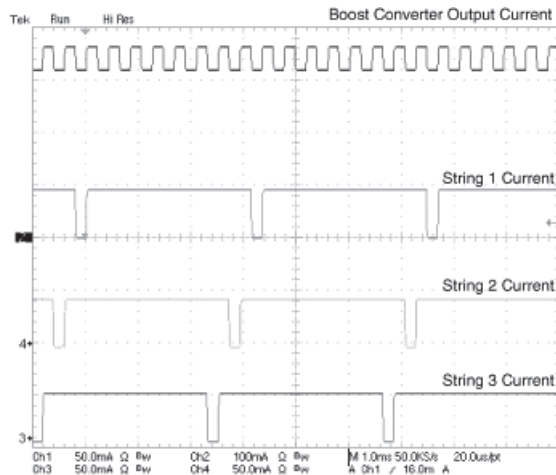


**Figure 5.** Experimental system waveforms demonstrating operation of the PS-PWM block at an input command *Dim* = 93.7%. Current waveforms are shown for the boost converter output and 3 of the 8 LED string currents.

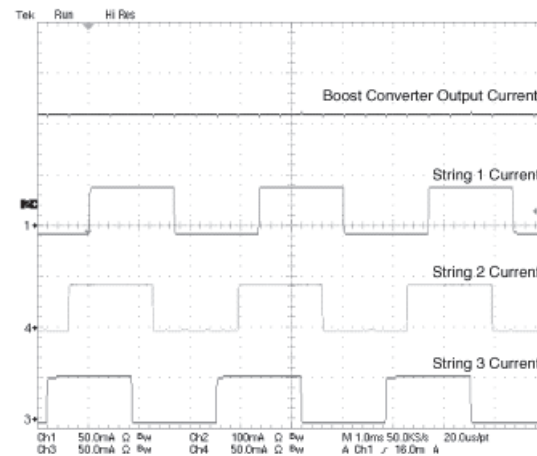


**Figure 6.** Experimental system waveforms demonstrating operation of the PS-PWM block at an input command *Dim* = 50%. Current waveforms are shown for the boost converter output and 3 of the 8 LED string currents.