

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

VIZIO, INC.,
Petitioner,

v.

POLARIS POWERLED TECHNOLOGIES, LLC,
Patent Owner.

IPR2024-00073
Patent 7,843,148 B2

Before JOHN F. HORVATH, DANIEL J. GALLIGAN and
KARA L. SZPONDOWSKI, *Administrative Patent Judges*.

Opinion for the Board filed by *Administrative Patent Judge*
JOHN F. HORVATH.

Opinion Concurring filed by *Administrative Patent Judge*
DANIEL J. GALLIGAN.

HORVATH, *Administrative Patent Judge*.

JUDGMENT

Final Written Decision

Determining All Challenged Claims Unpatentable
Dismissing Petitioner's Motion to Strike as Moot
35 U.S.C. § 318(a); 37 C.F.R. § 42.64

I. INTRODUCTION

A. Background and Summary

Vizio, Inc. (“Petitioner”) filed a corrected Petition requesting *inter partes* review of claims 1–22 (“the challenged claims”) of U.S. Patent No. 7,843,148 B2 (Ex. 1001, “the ’148 patent”). Paper 16 (“Pet.”). Polaris PowerLED Technologies, LLC (“Patent Owner”) filed a Response (Paper 18, “PO Resp.”), Petitioner filed a Reply (Paper 20, “Pet. Reply”), and Patent Owner filed a Sur-Reply (Paper 23, “PO Sur-Reply”). Petitioner moved to strike a portion of Patent Owner’s Sur-Reply and an exhibit introduced during the deposition of Petitioner’s declarant (Paper 26, “Mot.”), and Patent Owner opposed (Paper 28, “Opp.”). An oral hearing was held on December 5, 2024, and the hearing transcript is included in the record. Paper 31 (“Tr.”).

We have jurisdiction and authority under 35 U.S.C. § 6(b). This is a Final Written Decision under 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73. For the reasons set forth below, Petitioner has demonstrated by a preponderance of evidence that claims 1–22 of the ’148 patent are unpatentable.

B. Real Parties-in-Interest

Petitioner and Patent Owner identify themselves, respectively, as the real parties-in-interest. Pet. 85; Paper 4, 1.

C. Related Matters

Petitioner and Patent Owner identify *Polaris PowerLED Techs, LLC v. Vizio, Inc.*, 2:23-cv-03478 (C.D. Cal.), as a district court proceeding that can affect or be affected by this proceeding. Pet. 86; Paper 4, 1.

D. The ’148 Patent

The ’148 patent is directed to a “light emitting diode (LED) driver that drives LEDs in parallel.” Ex. 1001, 1:6–7. Such a driver is illustrated in

Figure 4 of the patent, which is reproduced below.

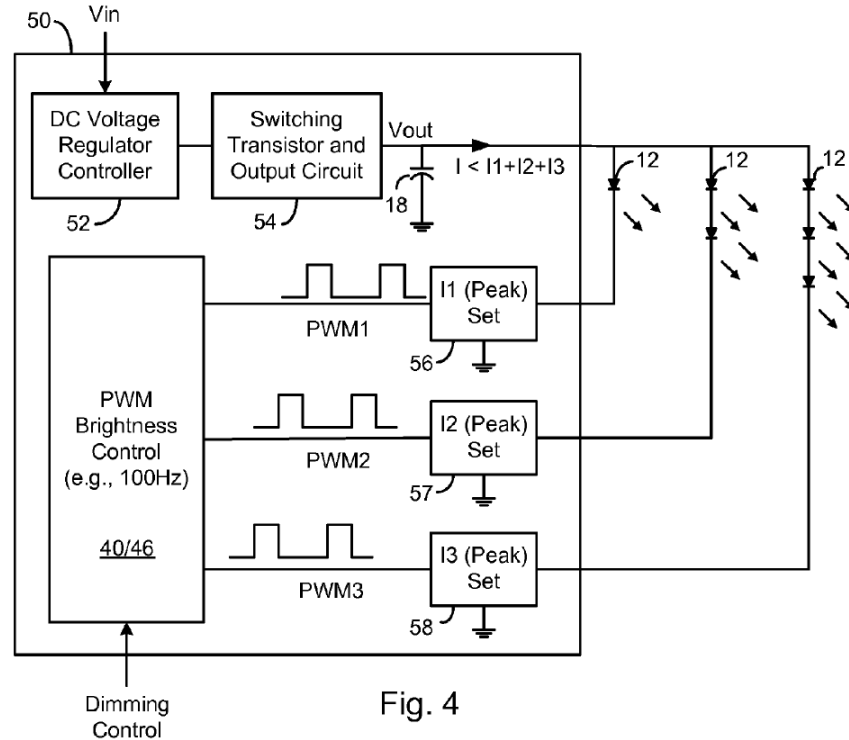
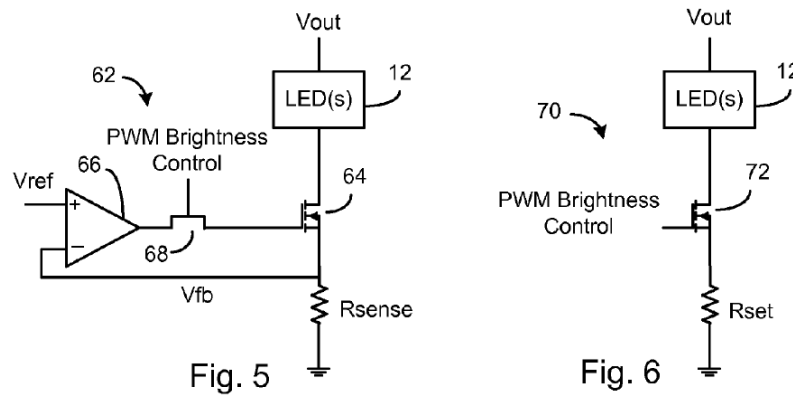


Fig. 4

Figure 4 is a schematic illustration of an LED driver that powers three parallel LED strings 12. *Id.* at 5:12–25. LED driver 50 includes DC voltage regulator controller 52, switching transistor and output circuit 54, capacitor 18, pulse width modulating (PWM) brightness controller 40/46, and current set circuits 56–58. *Id.* at 5:26–57. DC voltage regulator controller 52 “may be a boost regulator controller, a buck regulator controller, or any other type of regulator controller needed to generate an output voltage (V_{out}) that exceeds the forward voltage drop for each parallel path of LEDs.” *Id.* at 5:26–30. It generates a high frequency PWM signal that turns the switching transistor on and off at a duty cycle that determines V_{out} . *Id.* at 5:31–34.

Although all parallel LED paths 12 are energized by the same voltage V_{out} , they draw different currents determined by current set circuits 56–58, which are selectively “enabled and disabled by their associated staggered PWM brightness control signal[s] PWM1, PWM2, [and] PWM3.” *Id.* at

5:48–52. Figures 5 and 6 illustrate different embodiments of current set circuits 56–58 and are reproduced below. *Id.* at 5:58–59, 6:7–8.



Figures 5 (left) and 6 (right) are schematic illustrations of different embodiments of current set circuits 56–58 shown in Figure 4. *Id.*

In the Figure 5 embodiment, a “low value sense resistor (R_{sense}) and MOSFET 64 are connected in series with the one or more LEDs 12.” *Id.* at 5:59–61. The voltage V_{fb} across R_{sense} , which is “proportional to the current through the LEDs, is applied to an inverting input of an op amp 66.” *Id.* at 5:62–64. Op amp 66 is configured as a comparator and its non-inverting input “is coupled to a reference voltage (V_{ref}).” *Id.* at 5:64–65. The output of op amp 66 is coupled to the gate of MOSFET 64 during the positive phase of the PWM brightness control signal via pass transistor 68. *Id.* at 6:3–6. When pass transistor 68 is enabled, op amp 66 “controls the gate voltage of the MOSFET 64 to cause V_{fb} to equal V_{ref} ,” thereby limiting the current flowing through LED string 12 to V_{ref}/R_{sense} . *Id.* at 5:65–66.

In the Figure 6 embodiment, a “current set resistor R_{set} and MOSFET 72 are connected in series with the one or more LEDs 12.” *Id.* at 6:9–10. MOSFET 72 is enabled during the positive phase of the PWM brightness

control signal, allowing a limited current V_{out}/R_{set} to flow through LED string 12. *Id.* at 6:11–16.

PWM brightness controller 40/46 generates “stagger[ed] PWM brightness control signals” and supplies them to different parallel LED strings. *Id.* at 4:3–4. “The LEDs in each path are switched on and off in accordance with the PWM duty cycle to create a certain perceived brightness level, but the paths are energized at different times” determined by the staggered phases of the PWM brightness control signals. *Id.* at 4:4–7. An N-bit shift register can generate the staggered PWM brightness control signals, where “[t]he number of [shift register] bits determines the fineness in selecting PWM brightness control signal duty cycles.” *Id.* at 4:13–15. Such a shift register is shown in Figure 2A, which is reproduced below.

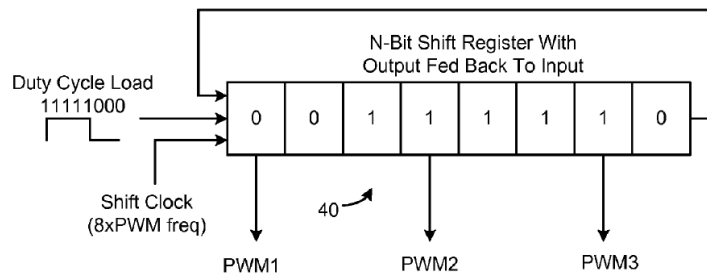


Fig. 2A

Figure 2A is a schematic illustration of an 8-bit shift register that can be used to generate staggered PWM signals. *Id.* at 4:31–32. An eight-bit word loaded into the shift register determines the duty cycle of the staggered PWM signals. *Id.* at 4:31–33. For example, the word (11111000) generates a 5/8 or 62.5% duty cycle. *Id.* at 4:52–53. A shift clock having a frequency that is 8 times the frequency of the generated PWM signal “shift[s] the bit pattern to the right for every shift clock cycle.” *Id.* at 4:34–37. The phase-shifted or staggered PWM brightness control signals for each parallel LED path are obtained by tapping “different positions along the shift register 40.”

Id. at 4:43–46. For example, as shown in Figure 2A, signals PWM1, PWM2, and PWM3 are staggered by tapping shift register 40 at locations 0, 3, and 6, respectively. *Id.* at 4:49–51. The staggered PWM signals obtained from each tap are shown in Figure 2B, which is reproduced below.

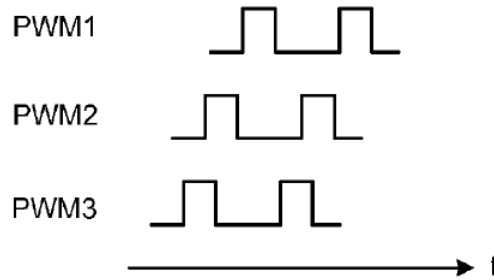


Fig. 2B

Figure 2B is a schematic illustration of staggered PWM signals having the same duty cycle but phase-shifted start times obtained by tapping an N-bit shift register at different shift register locations. *Id.* at 4:55–57.

E. Illustrative Claim

Claims 1 and 14 are independent claims, reciting a light emitting diode (LED) driver and a method for driving LEDs, respectively. Ex. 1001, 6:35–54, 7:51–8:8. Claims 2–13 depend directly or indirectly from claim 1 and claims 15–22 depend directly or indirectly from claim 14. *Id.* at 6:55–7:50, 8:9–58. Claim 1 is illustrative of the challenged claims and is reproduced below.

1. A light emitting diode (LED) driver for driving LEDs connected to different parallel paths, the driver comprising:
a voltage source for connection to first ends of LEDs in a plurality of parallel paths;
a plurality of current set circuits, one current set circuit per parallel path, each current set circuit controlling a peak current through one or more LEDs connected in each parallel path; and

a pulse-width modulated (PWM) brightness control signal generator connected to the plurality of current set circuits, the brightness control signal generator being configured to generate staggered PWM brightness control signals to the plurality of current set circuits,

each current set circuit being configured to draw the peak current through its associated one or more LEDs at a duty cycle substantially corresponding to a duty cycle of a PWM brightness control signal applied to it, such that the plurality of current set circuits conduct current through their associated one or more LEDs at the same duty cycle but out of phase with each other.

Id. at 6:35–54.

F. Evidence

Reference		Date	Exhibit
Thomas	US 5,317,307	May 31, 1994	1005
Zane	<i>Digital Architecture for Driving Large LED Arrays with Dynamic Bus Voltage Regulation and Phase Shifted PWM</i> , Montu Doshi and Regan Zane ¹	Mar. 1, 2007	1006
Tatewaki	US 6,402,354 B1	June 11, 2002	1007

Petitioner also relies upon the Declarations of Regan Zane, Ph.D. (Exs. 1003, 1031). Patent Owner relies on the Declaration of Thomas L. Credelle (Ex. 2002). Dr. Zane’s deposition transcripts have also been submitted to the record. (Exs. 2004, 2011).

¹ Petitioner contends an electronic copy of this paper was made publicly available to over 2,500 registered attendees of the 22nd Annual IEEE Applied Power Electronics Conference and Exposition, held in Anaheim, CA from February 25, 2007 until March 1, 2007. Ex. 1003 ¶ 46; *see also* Exs. 1016–19. Patent Owner does not contest the public availability of Zane. PO Resp. 29–31; PO Sur-Reply 19–26.

G. Asserted Grounds

Petitioner asserts the challenged claims are unpatentable on the following grounds (Pet. 17):

Claims Challenged	35 U.S.C. §	Reference(s)/Basis
1, 3, 7, 9–12, 14, 17, 18, 20–22	102(b)	Thomas
1, 3, 6, 7, 9–12, 14, 17, 18, 20–22	103(a)	Thomas
2, 13, 15	103(a)	Thomas, AAPA ²
8, 19	103(a)	Thomas, Tatewaki
1–4, 11, 12, 14, 17, 22	102(b)	Zane
1–4, 5, 11–17, 22	103(a)	Zane

II. ANALYSIS

A. Level of Ordinary Skill in the Art

Petitioner identifies a person of skill in the art (“POSITA”) at the time of the invention as someone that would have had “a bachelor’s degree in physics, electrical engineering, or a related field, and approximately two years of experience in the fields of LED technology, backlights, LED devices and control thereof, or other related fields.” Pet. 16 (citing Ex. 1003 ¶¶ 34–35). Petitioner further contends that “advanced education in the fields of physics, electrical engineering, or a related field can compensate for lesser work experience in the relevant fields” and that the merits of the Petition “do[] not turn on this specific definition of the level of ordinary skill.” *Id.* Patent Owner does not dispute this definition. PO Resp. 4–5.

In our Institution Decision, we found Petitioner’s assessment of the level of skill in the art to be reasonable and commensurate with the problems and solutions disclosed in the prior art and, omitting the open-ended phrase

² Applicant Admitted Prior Art

“at least” included in Petitioner’s definition, adopted it as our own. We continue to do so here.

B. Claim Construction

In *inter partes* reviews, we interpret a claim “using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. 282(b).” 37 C.F.R. § 42.100(b). Under this standard, a claim is construed “in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.” *Id.* However, “[t]he Board is required to construe ‘only those terms . . . that are in controversy, and only to the extent necessary to resolve the controversy.’” *Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)).

Petitioner contends “no claim terms need to be expressly construed to resolve the invalidity issues in this Petition.” Pet. 16. Patent Owner agrees. PO Resp. 5. In our Institution Decision, we declined to construe any claim term because we found no term required express construction. *See Realtime Data*, 912 F.3d at 1375. We maintain that finding here.

C. Anticipation by Zane

Petitioner contends claims 1–4, 11, 12, 14, 17, and 22 are anticipated by Zane. Pet. 60–75. Patent Owner disputes this. PO Resp. 29–34. For the reasons discussed below, we agree with Petitioner that Zane anticipates these claims of the ’148 patent.

1. Zane

Zane discloses “a digital architecture suitable for driving a large number of High Brightness Light Emitting Diodes (HB-LEDs) with

improved system efficiency and reduced EMI” or electromagnetic interference. Ex. 1006, Abs. This architecture is shown in Figure 1 of Zane, which is reproduced below.

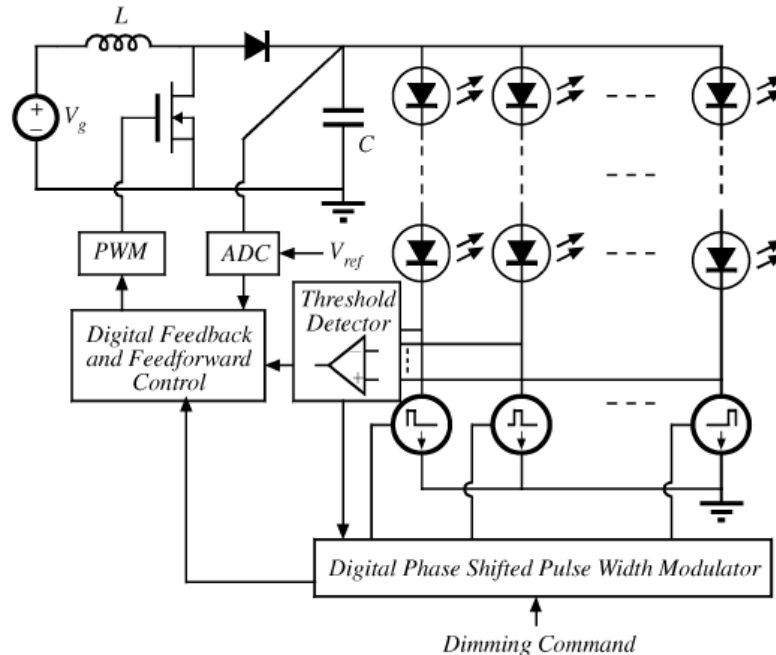


Figure 1 of Zane illustrates a “digital architecture for driving a scalable number of parallel LED strings.” *Id.* at 287. The architecture consists of “a power converter driving multiple strings of LEDs, controlled current sources, [a] digital multiphase modulator block, [a] threshold detector circuit to sense the voltage drop across each string, and digital control logic.” *Id.* at 288. The power converter has a “boost topology . . . appropriate for operating from a battery voltage or standardized low voltage bus” and is configured “to output a 40 V signal from [a] 12 V input supply.” *Id.* at 290.

Each of the parallel LED strings is coupled to ground via a “linear programmable current sink [that] is used to regulate the LED forward current to a desired level.” *Id.* The programmable current sink is illustrated in Figure 4 of Zane, which is reproduced below.

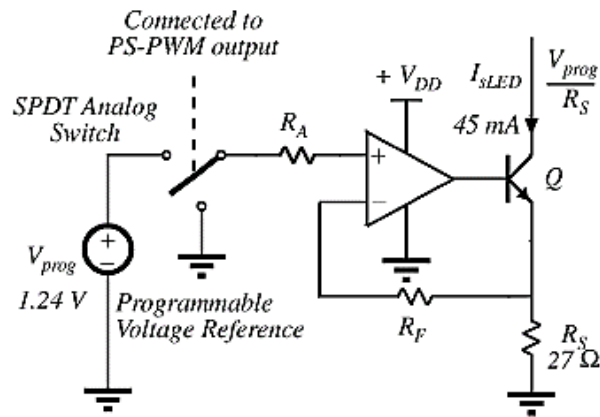


Figure 4 of Zane illustrates “[a]n op-amp based precision programmable current sink with AM [Amplitude Modulated] and PWM control options.” *Id.* at 291. “Amplitude modulation (AM) is implemented using a programmable voltage source (V_{prog}).” *Id.* at 290. PWM control, used for LED dimming, is implemented using a single-pole double-throw (SPDT) switch controlled by a phase-shifted pulse width modulator (PS-PWM). *Id.* When the switch is closed, an op-amp compares the voltage (V_{prog}) at its non-inverting (+) input to the voltage ($I_{sLED} * R_S$) at its inverting (-) input and, based on that comparison, turns transistor Q on/off to regulate the current in the LED string to the value $I_{sLED} = V_{prog} / R_S$. *Id.* at 290–91.

Zane’s PS-PWM is implemented on an “FPGA to control the operation of individual current sinks.” *Id.* at 291. When the PS-PWM receives a dimming command, it “determine[s] the appropriate phase-shift and duty cycle of individual control output signals.” *Id.* The PS-PWM thus “rotates *which* [LED] strings are active, resulting in a natural phase shifting of the LED string drive signals.” *Id.* at 288. This is shown in Figure 2(a) of Zane, which is reproduced below.

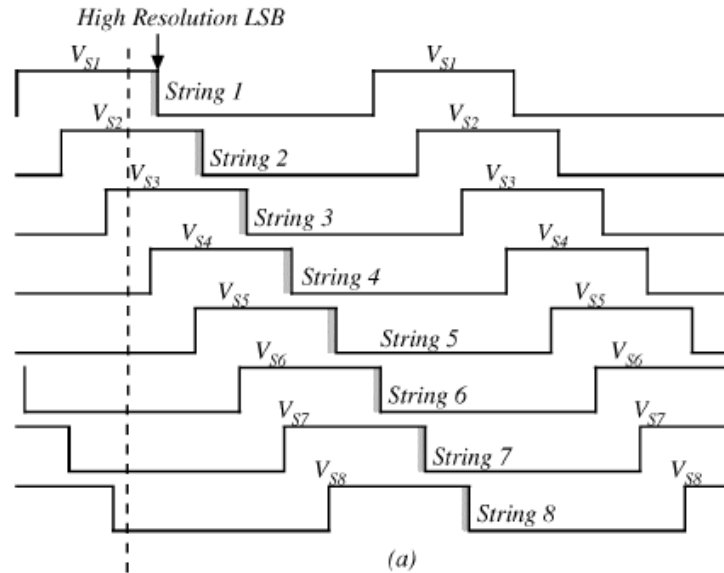


Figure 2(a) of Zane illustrates eight phase-shifted control signals (V_{S1} – V_{S8}) generated by Zane's PS-PWM to drive eight parallel LED strings at a 40% duty cycle in response to receiving a 40% dimming command. *Id.* at 288–89.

2. Whether Dr. Zane's Testimony Should be Given Any Weight

Patent Owner does not dispute Petitioner's contentions that Zane discloses each of the elements recited in claims 1–4, 11, 12, 14, 17, and 22. PO Resp. 29–34. Rather, Patent Owner argues that Petitioner's declarant, Dr. Zane, is so biased that his testimony should be given little or no weight. *Id.* Patent Owner further argues that without Dr. Zane's testimony, Petitioner's analysis consists of little more than attorney argument that is insufficient to meet its burden of proof. *Id.*; *see also* PO Sur-Reply 19–23.

Patent Owner argues that Dr. Zane's testimony is biased and ought not be considered because he, as a co-author of Zane, has insight into that reference that a POSITA would not have. PO Resp. 30–31 (citing *Glaxo Grp. Ltd. v. Apotex, Inc.*, 376 F.3d 1339, 1348–49 (Fed. Cir. 2004)). Patent Owner further argues that Dr. Zane's testimony is biased because he has

“personal incentives and motivations to invalidate the ’148 patent,” including co-inventorship of a patent disclosing similar technology and attempts to commercialize that patent.³ *Id.* at 31–32 (citing Ex. 2004, 61:22–62:21, 65:3–22, 71:1–72:11; Ex. 2005). Lastly, Patent Owner argues Dr. Zane’s testimony is biased because it is akin to uncorroborated inventor testimony regarding priority of invention. *Id.* at 33–34 (citing, *e.g.*, *Medronic, Inc. v. Teleflex Innovations S.A.R.L.*, 68 F.4th 1298, 1306 (Fed. Cir. 2023)).

Petitioner disagrees, arguing Patent Owner cites “no authority holding that an author of a prior art reference is unqualified to opine on that reference” and “no instance where Dr. Zane’s opinions went beyond what a POSITA would have understood from Zane.” Pet. Reply 3–4 (emphasis omitted). Petitioner further argues that Patent Owner’s reliance on *Glaxo* “is misplaced because that case involved experiments that an expert crafted using his knowledge of the patent-at-issue” rather than “an expert providing opinions about a prior art reference.” *Id.* at 4. Petitioner also argues that Dr. Zane’s testimony is credible because his analysis was provided “from the perspective of a POSITA reviewing [Zane] at the relevant time.” *Id.* (quoting Ex. 1003 ¶ 32). Lastly, Petitioner argues Dr. Zane’s testimony is not biased because he has no financial interest in the Zane patent and no longer receives funding for the work that led to it. *Id.* at 4–5.

Upon consideration of the evidence and argument presented, we decline Patent Owner’s invitation to categorically discount the weight of Dr. Zane’s testimony. First, that testimony concerns what is already disclosed in

³ US 7,948,468 B2 (“the Zane patent”), which issued on May 24, 2011 to Regan A. Zane and Montu Doshi and was assigned to the Regents of the University of Colorado. Ex. 2005.

Zane, and Dr. Zane testifies that his opinions are provided “from the perspective of a POSITA.” Ex. 1003 ¶ 32. Patent Owner cites no evidence to suggest otherwise.⁴ PO Resp. 29–40; PO Sur-Reply 20–26. Second, the Zane patent is assigned to the University of Colorado, and Dr. Zane testifies that he does not currently receive remuneration for that patent and does not believe he ever received remuneration for that patent. Ex. 2004, 64:12–17, 69:9–22. Third, for the reasons explained below, we find Patent Owner’s reliance on *Glaxo* and *Medtronic* inapposite given the facts presented here.

Patent Owner argues *Glaxo* stands for the proposition that an “expert could not act as a POSITA when they possessed impermissible knowledge of the reference in question.” PO Sur-Reply 21. We disagree. *Glaxo* stands for the proposition that an expert cannot show a reference inherently anticipates a claim by conducting experiments that deviate from the reference’s actual disclosure, especially after having reviewed the challenged patent. *See Glaxo*, 376 F.3d at 1345 (expert admitting he had “reviewed the [challenged] patent prior to performing his experiments” and had “deviat[ed] from the example of the [prior art] patent in which . . . [a compound’s] synthesis is disclosed”); *id.* at 1349 (finding the district court did not err when it discredited the expert’s “testimony and experiments as to whether the [prior art] patent inherently yields highly pure amorphous [compound]”). As explained above, Dr. Zane’s anticipation testimony does

⁴ We recognize that Patent Owner and Mr. Credelle, its declarant, dispute Dr. Zane’s testimony regarding modifying Zane’s circuit in support of Petitioner’s obviousness contentions. *See* Ex. 2002 ¶¶ 52–57. But that dispute does not concern Petitioner’s anticipation contentions. Moreover, a mere disagreement between competing experts regarding whether and how a POSITA would modify prior art is not, by itself, evidence that either expert’s opinion is so biased as to be unreliable.

not go beyond how a POSITA would have understood Zane’s *actual* disclosures, which we discuss further below. *See* Pet. 60–75; Ex. 1003 ¶¶ 147–176.

Patent Owner also argues *Medtronic* and similar cases stand for the proposition that “a party who inherently has a motivation to testify in favor of a reference is less credible than one who does not.” PO Sur-Reply 22. Again, we disagree. *Medtronic* stands for the more limited proposition that inventor testimony that will directly inure to the inventor’s benefit, such as testimony swearing behind prior art, must be corroborated. *Medtronic*, 68 F.4th at 1306; *cf. Thomson, S.A. v. Quixote Corp.*, 166 F.3d 1172, 1176 (Fed. Cir. 1999) (holding “the corroboration rule is needed only to counterbalance the self-interest of a testifying inventor against the patentee” such as when “the testifying inventor is asserting a claim of derivation or priority of his or her invention and is a named party, an employee of or assignor to a named party, or otherwise is in a position where he or she stands to directly and substantially gain by his or her invention being found to have priority over the patent claims at issue”).

Patent Owner has not shown that Dr. Zane’s testimony would directly and substantially inure to his benefit. Dr. Zane is not testifying against Patent Owner on behalf of Dr. Zane’s patent, is not a named party in this or the related district court proceeding, and is not asserting a claim of derivation or priority of his invention over the challenged patent. Moreover, Patent Owner has not shown that Dr. Zane has any financial or commercial interest in the circuit disclosed in Zane or in the Zane patent. Ex. 2004, 64:12–17. 69:9–22.

For the reasons explained above, we do not find Dr. Zane so biased that his testimony ought to be categorically assigned little to no weight. In

3. Claim 1

[illegible]

Claim 1 recites a driver for driving a plurality of LEDs connected to different parallel paths. Ex. 1001, 6:35–36. Petitioner demonstrates how Zane discloses an LED driver “for driving a scalable number of parallel LED strings.” Pet. 61 (quoting Ex. 1006, 287, Fig. 1). Patent Owner does not dispute this. PO Resp. 29–34.

16

Petitioner demonstrates how Zane's voltage source and power converter circuit (highlighted in orange above) are connected in parallel to the first ends of eight LED strings. Pet. 61–63 (citing Ex. 1006, Figs. 1, 3).⁵ Patent Owner does not dispute this. PO Resp. 29–34.

Claim 1 further requires the driver to include “a plurality of current set circuits, one current set circuit per parallel path, each current set circuit controlling a peak current through one or more LEDs connected in each parallel path.” Ex. 1001, 6:39–42. Petitioner demonstrates how Zane discloses a plurality of programmable current sinks (highlighted in green above), one for each of the parallel LED strings, that regulate the current through their respective LED string. Pet. 63–65 (citing Ex. 1006, 290–91, Figs. 3, 4). Patent Owner does not dispute this. PO Resp. 29–34.

Claim 1 further requires the driver to include “a [PWM] brightness control signal generator connected to the plurality of current set circuits . . . configured to generate staggered PWM brightness control signals to the plurality of current set circuits.” Ex. 1001, 6:43–47. Petitioner demonstrates how Zane's PS-PWM (highlighted in blue above) is connected to and generates a plurality of staggered PWM brightness control signals for Zane's current sinks (current set circuits). Pet. 65–67 (citing Ex. 1006, 288–89, 291, Figs. 2(a), 3, 4). Patent Owner does not dispute this. PO Resp. 29–34.

Lastly, claim 1 requires “each current set circuit being configured to draw the peak current through its associated one or more LEDs at a duty cycle substantially corresponding to a duty cycle of a PWM brightness control signal applied to it, such that the plurality of current set circuits

⁵ Petitioner contends Figure 3 “further details the experimental setup for the LED driver shown in Figure 1.” Pet. 62. Patent Owner does not dispute this. PO Resp. 29–34.

conduct current through their associated one or more LEDs at the same duty cycle but out of phase with each other.” Ex. 1001, 6:48–54.

Petitioner contends Zane’s programmable current sinks (current set circuits) “are controlled by the PS-PWM to conduct current according to the PWM signal output to the respective [LED] strings.” Pet. 68 (citing Ex. 1006, 291). Petitioner further contends that Zane’s PS-PWM, in response to receiving a dimming command, “determine[s] the appropriate phase-shift and duty cycle of individual control output signals” to be applied to Zane’s current sinks, which “draw the peak current through the LEDs in their associated parallel string at [the] duty cycle” of the applied control signal. *Id.* (quoting/citing Ex. 1006, 290–91; citing Ex. 1003 ¶ 156). Petitioner explains these contentions with an annotated version of Figure 6 of Zane, which is reproduced below. *Id.* at 68–69.

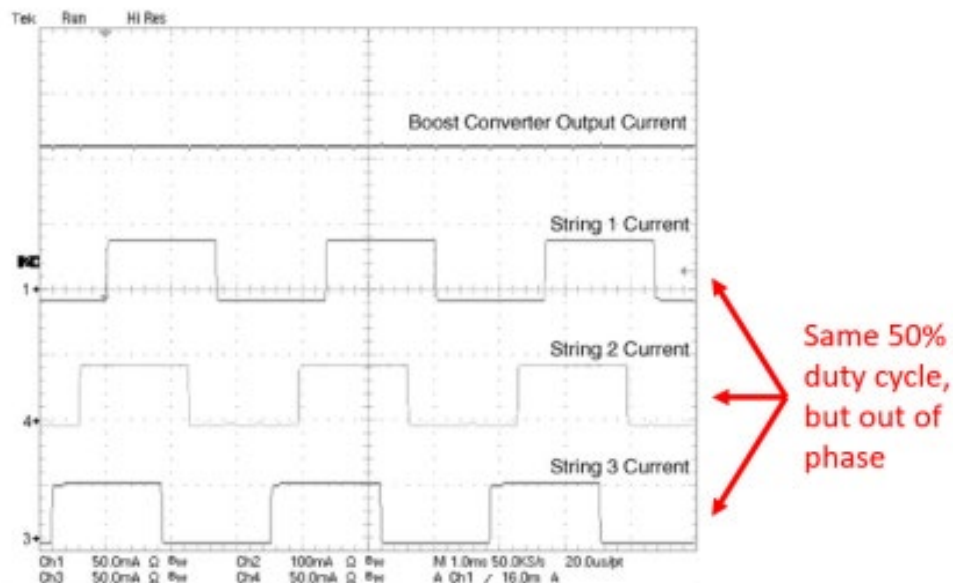


Figure. 6. Experimental system waveforms demonstrating operation of the PS-PWM block at an input command *Dim* = 50%. Current waveforms are shown for the boost converter output and 3 of the 8 LED string currents.

Petitioner's annotated version of Figure 6 of Zane shows how Zane's LED strings 1–3 draw out-of-phase currents having a 50% duty cycle in response to their programmable current sinks receiving phase-shifted control signals having a 50% duty cycle. *Id.* (citing Ex. 1006, Fig. 6; Ex. 1003 ¶ 157). The phase-shifted control signals are generated by Zane's PS-PWM in response to receiving a 50% dimming command. *Id.* Patent Owner does not dispute Petitioner's contentions, with which we agree. PO Resp. 29–34.

4. *Claims 2–4, 11, 12, 14, 17, 22*

We have reviewed Petitioner's contentions and mapping of Zane's disclosures to each of the limitations recited in claims 2–4, 11, 12, 14, 17, and 22. *See* Pet. 69–75. Patent Owner does not dispute these contentions, with which we agree. PO Resp. 29–34.

5. *Conclusions regarding Anticipation by Zane*

Petitioner through its contentions, with which we agree and adopt as our own, demonstrates by a preponderance of evidence how Zane discloses each of the limitations recited in claims 1–4, 11, 12, 14, 17, and 22. We disagree with Patent Owner's contention that Dr. Zane's testimony is entitled to little or no weight for the reasons explained above. Accordingly, we find Petitioner has demonstrated by a preponderance of evidence that Zane anticipates claims 1–4, 11, 12, 14, 17, and 22 of the '148 patent.

D. *Obviousness over Zane*

Petitioner contends claims 1–5, 11–17, and 22 would have been obvious over Zane. Pet. 75–83. Patent Owner disputes this. PO Resp. 29–40. For the reasons explained below, we find Petitioner demonstrates by a preponderance of evidence that these claims would have been obvious over Zane.

1. *Claims 1–4, 11, 12, 14, 17, 22*

Petitioner contends that to the extent these claims are not anticipated by Zane they would have been obvious over Zane because any differences between them and Zane “would have been obvious to a POSITA as of the time of the invention.” Pet. 75–76. Patent Owner argues this is a “conclusory statement unsupported by sufficient evidence or explanation to support . . . a finding” of obviousness. PO Resp. 35. Patent Owner argues this is so because “Petitioner does not allege any modifications to *Zane* to remedy any . . . deficiencies in the anticipation ground” and does not “address why it would have been obvious to make any such modifications with a reasonable expectation of success.” *Id.* at 35–36. Petitioner replies that the claims would have been obvious over Zane because they are anticipated by Zane and “it is well settled that a disclosure that anticipates under § 102 also renders the claim invalid under § 103, for anticipation is the epitome of obviousness.” Pet. Reply 6 (quoting *Realtime Data*, 912 F.3d at 1373).

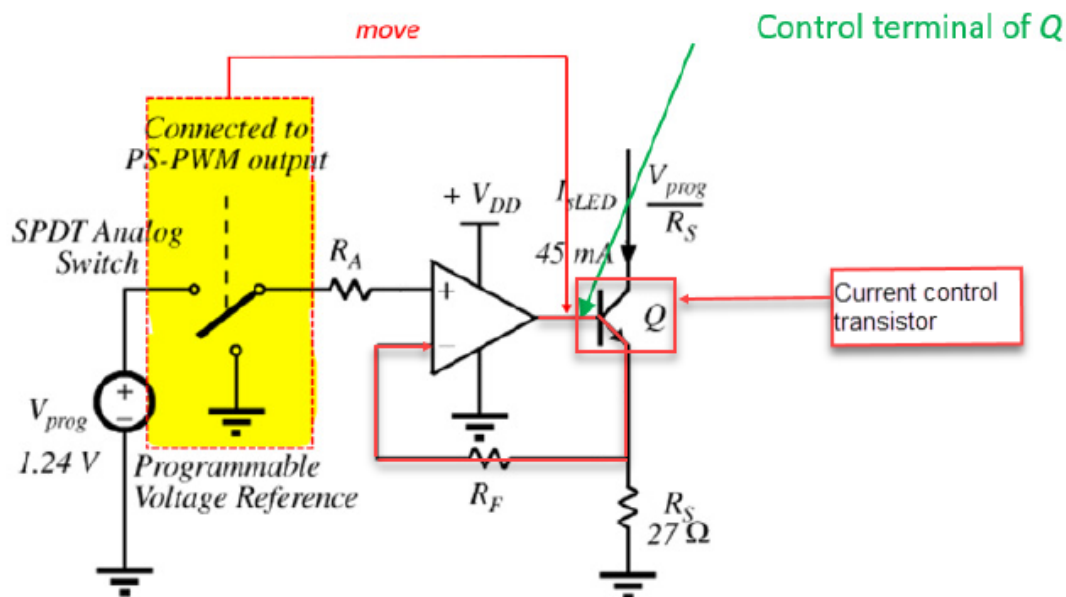
On the record before us, we agree with Petitioner. The record before us contains no secondary considerations evidence, and Petitioner has demonstrated that Zane anticipates these claims. Therefore, Petitioner has demonstrated that these claims would have been obvious over Zane. *See In re Meyer*, 599 F.2d 1026, 1031 (CCPA 1979) (recognizing as a “commonsense fact that a rejection for obviousness under § 103 can be based on a reference which happens to anticipate the claimed subject matter”).

2. *Claims 5 and 16*

Claim 5 depends from claim 4, and both claims recite further details of the “current set circuit” required by claim 1. Ex. 1001, 6:59–7:10. Claim

4 requires the circuit to include “a current control transistor in series with one or more LEDs in an associated parallel path” and “a feedback circuit connected to detect a current through the parallel path and connected to the current control transistor . . . to cause the current through the parallel path to match a reference level.” *Id.* at 6:59–67. Claim 5 requires the circuit to also include “a PWM brightness control transistor connected between an output of the feedback circuit and a control terminal of the current control transistor.” *Id.* at 7:1–4. The PWM brightness control transistor must also be “connected to the PWM brightness control signal generator for receiving a staggered PWM brightness control signal to couple the output of the feedback circuit to the control terminal of the current control transistor.” *Id.* at 7:4–8.

Petitioner’s mapping of Zane to claims 4 and 5 is most easily explained by reference to an amalgamation of several of Petitioner-annotated versions of Figure 4 of Zane, which amalgamation is reproduced below. *See* Pet. 71, 72, 78.



The amalgamation illustrates Petitioner’s identification of (a) transistor Q as the “current control transistor” required by claim 4 and its base as the control terminal required by claim 5, (b) the circuit path from the output of the op-amp, through transistor Q and resistor R_F , to the inverting (-) input of the op-amp as the “feedback circuit” required by claim 4, and (c) the SPDT switch as the “PWM brightness control transistor” required by claim 5, which Petitioner argues “would have been implemented with at least one transistor” based on the knowledges of a person skilled in the art. *Id.* at 71–73, 76–78 (citing Ex. 1003 ¶¶ 162–164, 182–184).

Although Zane’s SPDT switch is located before the op-amp’s non-inverting (+) input, Petitioner argues “it would have been obvious to modify *Zane* by moving the [SPDT switch] from the noninverting input of the op amp to between the output of the op amp (the output of the feedback circuit) and the control terminal of the current control transistor Q.” *Id.* at 77–78 (citing Ex. 1003 ¶ 184). Relying on the testimony of Dr. Zane, Petitioner argues the SPDT switch “may be placed in several locations in [*Zane*’s] circuit without changing the overall operation of the circuit because its function is to act as a switch that turns ‘on’ and ‘off’ the programmable current sink.” *Id.* at 78 (citing Ex. 1003 ¶ 185). Thus, Petitioner argues, whether before the op-amp’s non-inverting input as shown in *Zane* or after the op-amp’s output as proposed, the SPDT switch would allow or disallow current to flow through the LED string in response to the PWM brightness control signal. *Id.* at 78 (citing Ex. 1003 ¶¶ 185–186; Ex. 1027, Fig. 1). Petitioner further argues a POSITA would have made the proposed modification because “there are a finite number of ways in which the [SPDT switch] could be connected to *Zane*’s programmable current sink, and it

would have been obvious to try any of those solutions as a design choice.”
Id. at 78–79 (citing Ex. 1003 ¶ 186).

Patent Owner, in addition to arguing Dr. Zane’s testimony should be given no weight, argues “[n]either Petitioner nor Dr. Zane provides any explanation as to *why* a POSITA would have made the particular modification to *Zane* required to arrive at the claims.” PO Resp. 36, 39. Relying on the testimony of Mr. Credelle, Patent Owner further argues that “a POSITA would have understood there were material differences between *Zane* and the claimed [LED driver] arrangement that would affect the design and operation of the circuit” and that Petitioner’s “proposed modification ‘would frustrate the purpose and function of the circuit by hampering its ability to maintain a precision voltage.’” *Id.* at 40 (quoting/citing Ex. 2002 ¶¶ 53–57) (emphasis omitted); *see also* PO Sur-Reply 23–26.

We find Petitioner has articulated sufficient reasoning with rational underpinning to modify *Zane*’s Figure 4 with a reasonable expectation of success and has demonstrated that modified Figure 4 meets the limitations of claim 5. We agree with and credit Dr. Zane’s testimony that the function of *Zane*’s SPDT switch “is to turn the programmable current sink ‘on’ or ‘off’ . . . to control the passing of current through the LEDs in the associated path.” Ex. 1003 ¶ 185. We further agree that the switch would perform that function whether “placed at the noninverting (+) input, or at the output of the op amp, or even elsewhere such as between Q and R_S .” *Id.* Lastly, we agree with Dr. Zane that “a POSITA would have understood that there are a finite number of ways in which [SPDT switch] could be connected to *Zane*’s programmable current sink” to perform that function. *Id.* ¶ 186.

When cross-examined on this testimony, Dr. Zane further testified that placing the SPDT before the op-amp’s non-inverting input or after its

output “were the two [locations] that I’ve most commonly seen. And [I] would generally expect a circuit designer . . . to have considered either of these two.” Ex. 2004, 126:15–20. Dr. Zane further testified that Chang⁶ is a prior art example of “using a particular type of operational amplifier where it’s convenient to move the switch to the location of the output of the op amp.” *Id.* at 127:1–5. Dr. Zane also testified that “a skilled person would know that these multiple options I’ve described would be available and understood. And especially these two options that we were just emphasizing would be well known.” *Id.* at 128:11–15.

We credit that testimony over Mr. Credelle’s competing testimony that moving the SPDT switch would “frustrate the purpose and function of [Zane’s] circuit by hampering its ability to maintain a precision voltage” because the characteristics of the SPDT switch were not known and “a POSITA would not know how to adjust the op amp setting to achieve the correct voltage on the base of transistor Q.” Ex. 2002 ¶ 57. Replying to this testimony, Dr. Zane explained:

[A] POSITA would understand that the point of using an op amp in a negative feedback loop is to regulate the voltage across the resistor R_s to be equal to V_{prog} , regardless of any nonidealities in the circuit. A POSITA would have learned about the operation of negative feedback loops as part of their undergraduate coursework on circuits and thus, the feedback loop in Zane’s current sink would have been well understood by a POSITA. The op amp accomplishes this through negative feedback by automatically adjusting the op amp voltage output to achieve the desired current in the transistor Q. Thus, a POSITA would recognize that the feedback circuit would automatically compensate for any small effect of the SPDT switch when placed between the op amp output and the base of transistor Q, such as a very small voltage drop across the

⁶ US 6,621,235 B2 issued Sept. 16, 2003 to Chin Chang (Ex. 1027).

switch. A POSITA would understand that no adjustments would be necessary to the feedback circuit and the circuit would still set the [LED] current to V_{prog}/R_s .

Ex. 1031 ¶ 35. Patent Owner cross-examined Dr. Zane on this reply testimony and had the opportunity to challenge it in its Sur-Reply. *See* Ex. 2011; PO Sur-Reply 23–26. Instead, Patent Owner restated Mr. Credelle’s opinion that moving the SPDT switch “would create an uncertain voltage on the base of transistor Q that a POSITA would be unable to adequately address” and accused Petitioner of misstating portions of Mr. Credelle’s testimony that are not relevant to the discussion above. PO Sur-Reply 25 (citing Ex. 2002 ¶ 57).

Because we find Dr. Zane’s testimony more credible than Mr. Credelle’s, we agree with Petitioner that a person skilled in the art would have found it obvious to move Zane’s SPDT switch in the manner proposed. Pet. 77–78; *see also KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 402–03 (2007) (“When there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill in the art has good reason to pursue the known options within his or her technical grasp.”). Accordingly, we find Petitioner has demonstrated by a preponderance of evidence that claim 5 is unpatentable as obvious over Zane.

Claim 16 is a method claim that depends from claim 14. Ex. 1001, 8:13–26. The parties treat claims 5 and 16 identically. *See* Pet. 82–84 (mapping claim 16 limitations to claim 1, 4 and 5 limitations); PO Resp. 36–40; Pet. Reply 6–12; PO Sur-Reply 23–26. Accordingly, we find Petitioner has demonstrated by a preponderance of evidence that claim 16 is unpatentable as obvious over Zane for the same reasons as claim 5.

3. Claims 13 and 15

Claim 13 requires the driver of claim 1 to be “formed as an integrated circuit.” Ex. 1001, 7:49–50. Claim 15 is a method claim that depends from claim 14 and includes the step of “varying the duty cycle of the staggered PWM brightness control signals to change an average current through the parallel paths of LEDs to change a perceived brightness of the LEDs.” *Id.* at 8:9–12.

Petitioner contends a POSITA would have found these claims obvious in view of Zane’s disclosures and knowledge of the state of the art. Pet. 80–82 (citing/quoting Ex. 1006, Abs, 287, 291, 293, Figs. 5, 6, 8a, 8b; Ex. 1003 ¶¶ 190–197). Patent Owner does not dispute this. PO Resp. 29–41; PO Sur-Reply 19–26. We agree with Petitioner for the reasons stated in the Petition, which we adopt as our own, and find Petitioner has demonstrated by a preponderance of evidence that claims 13 and 15 would have been obvious over Zane.

E. Anticipation by Thomas

Petitioner contends claims 1, 3, 7, 9–12, 14, 17, 18, and 20–22 are anticipated by Thomas. Pet. 17–45. Patent Owner disputes this. PO Resp. 5–21. For the reasons discussed below, Petitioner has demonstrated that Thomas anticipated claims 14, 17, 18, and 20–22, but has not demonstrated that Thomas anticipated claims 1, 3, 7, and 9–12.

1. Thomas

Thomas discloses “a method and an apparatus for power demand load leveling of a power supply driving a plurality of LED’s through the use of pulse width modulation.” Ex. 1005, 2:18–21. Thomas’s apparatus is illustrated in Figure 1, reproduced below.

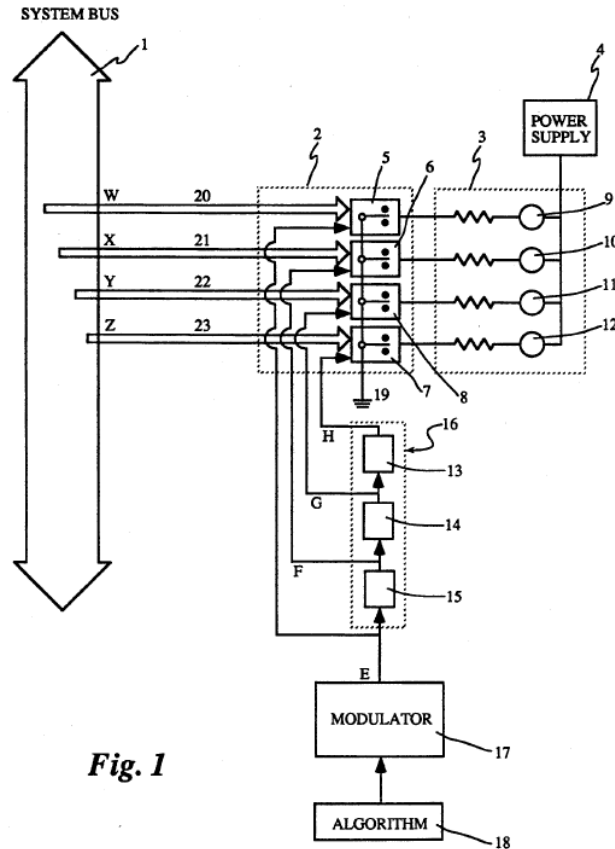


Figure 1 of Thomas is a block diagram of Thomas's load-leveling apparatus. *Id.* at 2:66–3:2. A plurality of control signals (W–Z) are transmitted to a plurality of LED groups (9–12) through a plurality of activation switches (5–8). *Id.* at 3:28–32. When enabled, switches 5–8 allow current to flow to LED groups 9–12 from power supply 4. *Id.* at 3:32–45. To reduce the current demand on power supply 4, modulator 17 presents “a first modulating signal E to a delay means (16), to generate a predetermined number of delayed modulating signals (F, G, H).” *Id.* at 3:63–67. Activation switches 5–8 are turned “on and off according to the input of the respective control signal [W, X, Y, Z] and modulating signal [E, F, G, H].” *Id.* at 4:65–5:8. “Because the modulating signals (E, F, G, H) vary in phase . . . , each set of activation switches (5–8) is sequentially turned on . . . so that no more than one group of LED's . . . is activated (or switched

on) at any one time.” *Id.* at 5:13–20. Further details of Thomas’s apparatus are shown in Figure 2, which is reproduced below.

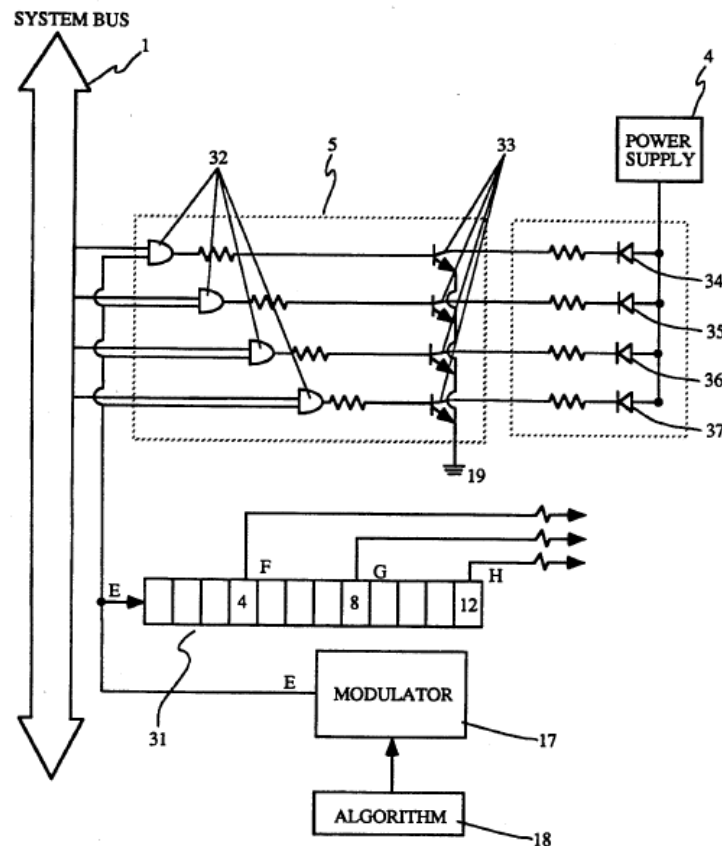


Fig. 2

Figure 2 of Thomas is a “partial circuit diagram . . . showing one group of four LED’s with their respective control lines and control devices.” *Id.* at 3:3–5. Figure 2 differs from Figure 1 in that it shows “only one group of LED’s (9) with a corresponding set of switches (5)” consisting of “gating control logic (32) forming AND gates and transistors (33).” *Id.* at 3:32–35, 4:17–19. The AND gates receive an enable or control signal W (not shown) and PWM modulating signal (E) as input and, when enabled, “generate output to their respective transistors (33)” to enable the transistors to

“provide current from the power supply (4) for activating the associated LED’s (34–37) in the group of LED’s (9).” *Id.* at 3:39–45.

Figure 2 also differs from Figure 1 in that it illustrates Figure 1’s delay element 16 as a “twelve bit shift register (31) [that] is used to generate the delayed modulating signals (F, G, H).” *Id.* at 4:19–21. Shift register 31 “sequentially stor[es] twelve binary values corresponding to the pulses or lack of pulses in the first modulating signal (E)” and generates signals (F, G, H) “by tapping the values stored within the fourth, eighth, and twelfth cells of the shift register (31).” *Id.* at 4:21–26. As shown in Thomas’s Figure 3, when signals (F, G, H) are generated in this way, they are identical to signal (E) but phase-shifted by (25, 50, 75) percent of the period T of signal (E). *Id.* at 4:51–59, Fig. 3.

2. Claim 1

Claim 1 recites a driver for driving a plurality of LEDs connected to different parallel paths comprising a plurality of current set circuits, one current set circuit per parallel path. Ex. 1001, 6:35–40. The claim further requires a pulse-width modulated brightness control signal generator to generate a plurality of staggered PWM brightness control signals. *Id.* at 6:43–47. The claim also requires each current set circuit to draw a peak current through its associated LED path at a duty cycle “substantially corresponding to a duty cycle of a PWM brightness control signal *applied to it*.” *Id.* at 6:48–51 (emphasis added).

Petitioner’s contention that Thomas anticipates claim 1 is most easily explained by reference to Petitioner’s annotation of Thomas’s Figure 1, which is reproduced below. Pet. 28.

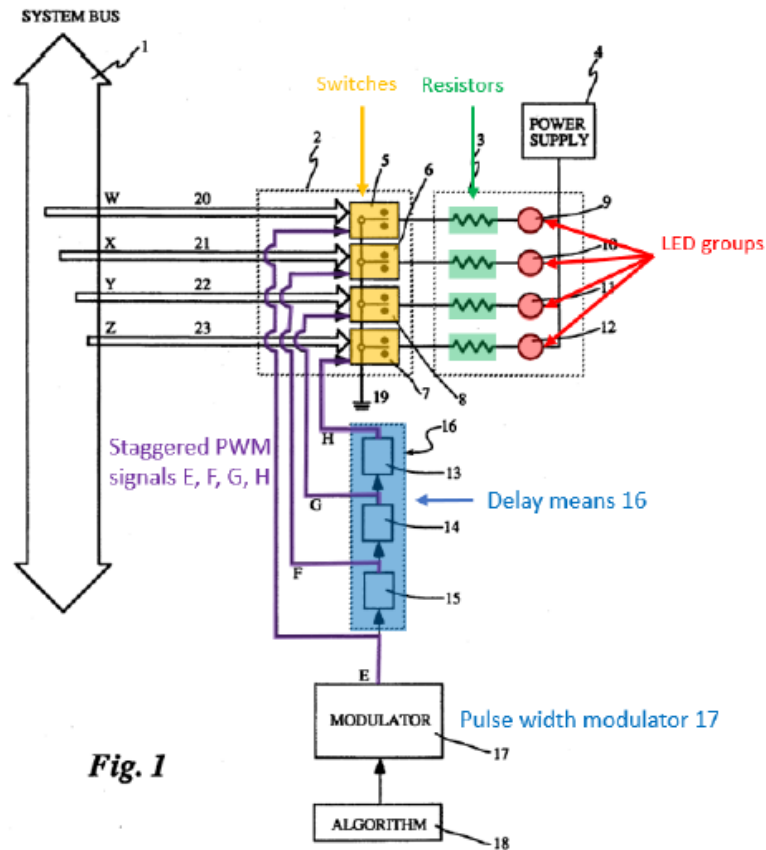


Fig. 1

Petitioner’s annotated version of Figure 1 of Thomas illustrates four LED groups 9–12 (red), each drawing current from power supply 4 when coupled to ground 19 through respective resistors (green) and switches 5–8 (yellow). Ex. 1005, 3:24–45. When enabled by respective control signals 20–23 (W, X, Y, Z), switches 5–8 couple LED groups 9–12 to ground 19 through the resistors based on the state of respective phase-shifted PWM signals (E, F, G, H) generated by modulator 17 and delay means 16. *Id.* at 3:46–4:16.

Petitioner identifies modulator 17 and delay means 16 as the recited “pulse-width modulated (PWM) brightness control signal generator” and signals E, F, G, and H as the plurality of “staggered PWM brightness control signals.” Pet. 27. Petitioner identifies the resistors as the recited “current set circuits.” *Id.* at 26 (“Thus, the resistors shown in Thomas’s Figure 1 . . . are

each a current set circuit, and there is one current set circuit per parallel path shown in Figure 1.”). Petitioner contends “the staggered PWM signals *E*, *F*, *G*, and *H* are fed into activation switches 5, 6, 8, and 7, respectively” and “activate their respective parallel paths . . . when the switches receive a high pulse from [their respective] PWM signal.” *Id.* at 30–31. Thus, Petitioner contends, “the current set circuits in each parallel path draw their peak currents at a duty cycle that corresponds to the duty cycle of the PWM brightness signal (*E*, *F*, *G*, or *H*) that are applied to them.” *Id.* at 31–32.

Patent Owner contends Petitioner’s mapping fails because “Petitioner maps the ‘current set circuits’ of claim 1 . . . to the ‘resistors’ in Thomas’s Figure 1” and “the PWM signal is never *applied* to the resistors in Thomas.” PO Resp. 13–14. Instead, Patent Owner contends, “the PWM signals go to the activation switches [5–8], and more specifically to the gating control logic 32 thereof.” *Id.* (citing Ex. 1005, 3:51–55, Fig. 2; Ex. 2002 ¶ 40). Patent Owner further contends “[t]he only thing applied to the resistors that Petitioner has identified as ‘the current set circuits’ is the current itself, which is *different* from the PWM brightness control signal.” *Id.* (citing Ex. 2002 ¶ 40).

Petitioner, in reply, argues that Thomas nonetheless anticipates claim 1 because “Thomas discloses essentially the same LED driver and current set circuit as described and claimed in the ’148 patent.” Pet. Reply 13. Petitioner supports this contention with a side-by-side comparison of Petitioner-annotated versions of a portion of Thomas’s Figure 2 and the ’148 patent’s Figure 6, which are reproduced below. *Id.* at 14.

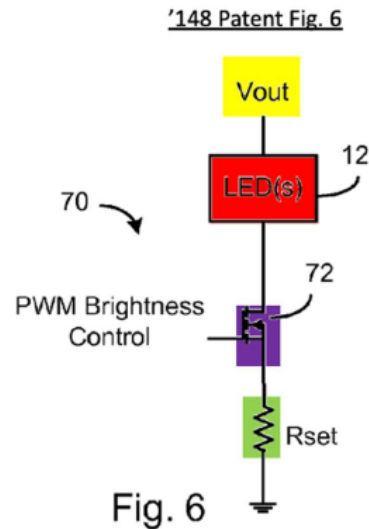
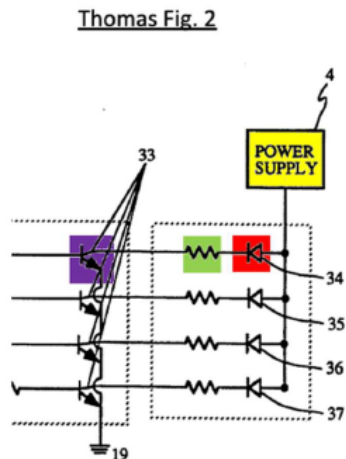


Fig. 6

Both Petitioner-annotated Figures show an LED string (red) drawing current from a power supply (yellow) to ground through a resistor (green) when a transistor (purple) in series with the resistor and LED is enabled by a PWM signal. *Id.*

Petitioner contends it permissibly identifies Thomas's transistor 33 as a component of the recited "current set circuit" in its Reply for several reasons. First, Petitioner contends its Petition did not "identif[y] the resistor as the current set circuit to the *exclusion* of other components." *Id.* Second, Petitioner contends that it "explained that Thomas's transistor is also part of the current set circuit" in the Petition's claim 6 analysis. *Id.* at 15. Third, Petitioner contends it can identify transistor 33 as a "current set circuit" component for the first time in its Reply because Patent Owner's Response included a new claim construction, namely, that a "circuit" must include multiple components. *Id.* at 15–17.

On the record before us, we find Petitioner has failed to demonstrate claim 1 is anticipated by Thomas. We agree with Patent Owner that the Petition "identified *only the passive resistor* as the 'current set circuit' of claim[] 1." PO Sur-Reply 3. The Petition clearly and categorically stated

“the resistors shown in Thomas’ Figure 1 . . . are each a current set circuit, and there is one current set circuit per parallel path shown in Figure 1.”

Pet. 26. We also agree with Patent Owner that Thomas does not apply signals E, F, G, and H, which Petitioner identified as the PWM brightness control signals, to the resistors Petitioner identified as the “current set circuits.” PO Resp. 14. Instead, Thomas applies these signals to transistors 33 when AND gates 32 are enabled by respective control signals W, X, Y, and Z. Ex. 1005, 3:24–4:16, Figs. 1, 2.

Although Petitioner’s Reply does ultimately identify transistors 33 *and* the resistors as the “current set circuits” required by claim 1, the Petition did not. Thus, the Reply contains new argument that impermissibly changes the scope of the argument set forth in the Petition. *See Henny Penny Corp. v. Frymaster LLC*, 938 F.3d 1324, 1330–31 (Fed. Cir. 2019) (“[A]n IPR petitioner may not raise in reply an entirely new rationale for why a claim would have been [unpatentable].”); *Ariosa Diagnostics v. Verinata Health, Inc.*, 805 F.3d 1359, 1367 (Fed. Cir. 2015) (affirming the Board’s rejection of a reply argument based on “previously unidentified portions of a prior art reference to make a meaningfully distinct contention”).

Moreover, although Petitioner’s claim 6 analysis did identify transistors 33 and the resistors as “current set circuits,” that analysis supported Petitioner’s contention that claim 6 would have been obvious over Thomas, not that claim 1 was anticipated by Thomas. Pet. 17, 45–50. Petitioner’s claim 6 obviousness analysis cannot cure Petitioner’s defective claim 1 anticipation analysis.

Lastly, we are not persuaded that the Reply’s identification of transistors 33 as “current set circuit” components was proper in view of Patent Owner’s contention that a “circuit” requires two or more components.

In addition to this contention, which is arguably a claim construction contention, Patent Owner argued that “[t]he only thing applied to the resistors that Petitioner has identified as the ‘current set circuits’ is the current itself, which is *different* from the PWM brightness control signal.” *Compare* PO Resp. 8, *with id.* at 14. It is the latter argument we find persuasive, and it does not depend on Patent Owner’s contention that a resistor alone cannot be a “current set circuit.” Indeed, the argument accepts Petitioner’s mapping of a single resistor to a “current set circuit,” but contends that no PWM signal is applied to the resistor. *See* PO Sur-Reply 7 (“PO explained that the PWM brightness control signal is not applied to the resistors under *any* interpretation.”) (emphasis added).

Accordingly, on the record before us and for the reasons discussed above, we find Petitioner has failed to demonstrate that claim 1 is anticipated by Thomas.

3. *Claims 3, 7, and 9–12*

Claims 3, 7, and 9–12 depend, directly or indirectly, from claim 1 and also require *applying* a PWM brightness control signal *to each of a plurality of current set circuits*. *See* 35 U.S.C. § 112 ¶ 4. Thus, on the record before us and for the reasons discussed above with respect to claim 1, we find Petitioner has failed to demonstrate that claims 3, 7, and 9–12 are anticipated by Thomas.

4. *Claims 14 and 17*

Claim 14 is a method claim reciting the method performed by an LED driver having a structure similar to the driver of claim 1, including the step of “*applying* a different staggered PWM brightness control signal[] *to each current set circuit*.” Ex. 1001, 6:55–8:8 (emphases added). Petitioner’s analysis of claim 14 refers back to its analysis of claim 1 and, therefore,

would appear to be defective for the same reasons as its claim 1 analysis. Pet. 41–42. However, claim 17 depends from claim 14 and expressly requires “applying a different staggered PWM brightness control signal to each current set circuit comprises applying each staggered PWM brightness control signal[] to an associated transistor connected in series with the one or more LEDs in an associated parallel path.” Ex. 1001, 8:27–31. Petitioner’s analysis of claim 17, discussed below, demonstrates how Thomas discloses this limitation and “cures” the defect in Petitioner’s claim 14 analysis by identifying transistor 33 as a component of claim 14’s “current set circuit” to which a staggered PWM brightness control signal is applied.

Petitioner’s analysis of claim 17, which contains all the limitations of claim 14, is most easily understood by reference to Petitioner’s annotation of Figure 2 of Thomas, which is reproduced below. Pet. 42–44.

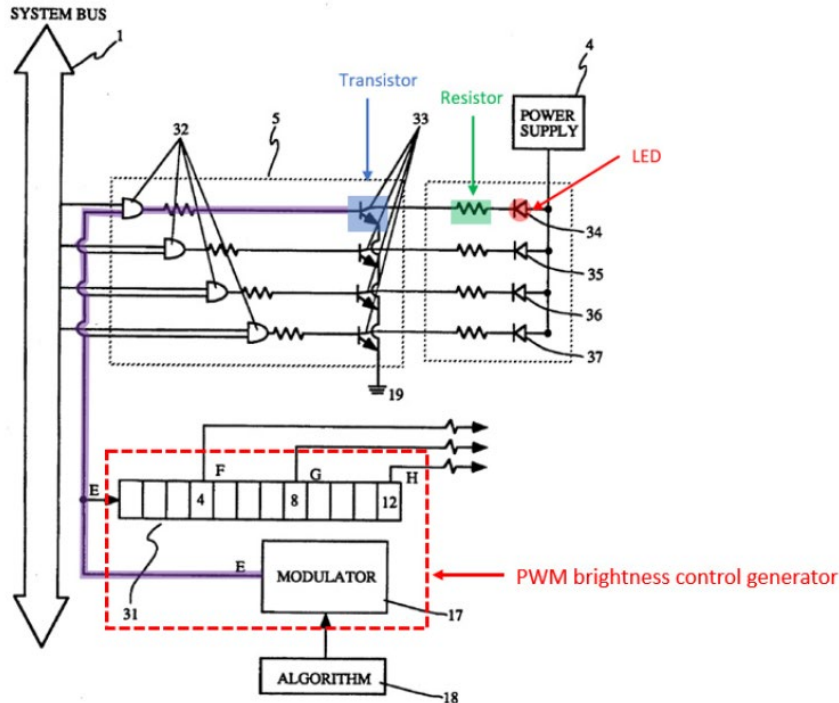


Fig. 2

Petitioner's annotated version of Figure 2 of Thomas is "a partial circuit diagram of the present [Figure 1] invention showing one group of four LED's with their respective control lines and control devices." Ex. 1005, 2:66–3:5.

Petitioner contends that Thomas discloses a method for driving a plurality of LED groups 9–12 (Figure 1) connected in parallel to power supply 4. Pet. 17–23, 41–44 (citing Ex. 1005, Figs. 1, 2).⁷ Petitioner identifies the resistor (green) as a "current set resistor" connected in series with an LED (red) and transistor 33 (blue) that sets the current in the LED path. Pet. 25–26, 42 (citing Ex. 1005, Figs. 1, 2; Ex. 1003 ¶¶ 62–63, 95). Petitioner contends that when "transistors 33 are turned on, they 'provide current from the power supply (4) for activating the associated LED's (34–37) in the group of LED's (9).'" *Id.* at 43 (quoting Ex. 1005, 3:42–45). Petitioner identifies the shift register coupled to modulator 17 and algorithm 18 as a "pulse-width modulated (PWM) brightness control signal generator" that generates "staggered PWM brightness control signals" E–H. *Id.* at 42–43 (citing Ex. 1003 ¶¶ 95–96). Petitioner contends transistors 33 are turned on "when the AND gates [32] receive both a high control signal (*W*, *X*, *Y*, or *Z*) for turning on the LED and a high pulse from a modulating signal (*E*, *F*, *G*, or *H*)."*Id.* at 43 (citing Ex. 1003 ¶ 96). Thus, Petitioner contends, the LEDs draw current when transistors 33 "receive a staggered PWM

⁷ Petitioner contends each of the four parallel LED paths shown in Figure 1 consists of four parallel LED sub-paths shown in Figure 2, and bases its contentions on only "four of the 16 total parallel sub-paths," one from each LED path shown in Figure 1. Pet. 18–23 (citing Ex. 1005, Figs. 1, 2; Ex. 1003 ¶¶ 55–58). Patent Owner does not dispute this contention, with which we agree. *See also* Pet. 22 (Petitioner's illustration of the 16 parallel sub-paths and the 4 parallel sub-paths on which its contentions rely).

brightness control signal (*E*, *F*, *G*, or *H*) for controlling the brightness of their associated LED according to the duty cycles of the staggered PWM brightness control signals applied to them.” *Id.* at 43–44 (citing Ex. 1003 ¶ 96).

Notwithstanding Patent Owner’s arguments to the contrary, discussed below, we find Petitioner demonstrates by a preponderance of evidence that Thomas discloses all the limitations of claim 17. Thomas enables parallel LED strings 9–12 by applying control signals W–Z to AND gates 32. Ex. 1005, 3:24–35, Figs. 1, 2. These control signals, when high, enable AND gates 32 to pass staggered PWM signals E–H to transistors 33 to turn them on/off at the same duty cycles as signals E–H. *Id.* at 3:35–4:16, Figs. 1, 2. This causes LED strings 9–12 to draw current from voltage supply 4 in a staggered manner at the same duty cycles and at levels set by the resistors in each LED path. *Id.* at 4:66–5:20, Figs. 1, 2. This is all claim 17 requires.

Patent Owner contends Thomas does not anticipate claim 17 because “the PWM signals go to the activation switches [5–8], and more specifically to the gating control logic 32 thereof.” PO Resp. 14 (citing Ex. 1005, 3:51–55, Fig. 2; Ex. 2002 ¶ 40).⁸ Patent Owner further contends that Thomas’s PWM control signal E is “*only* applied as input to the AND gates in Figure 2” and it is the “output of the AND gates [that] are applied to the gates of the control transistors 33.” *Id.* at 16 (citing Ex. 2002 ¶ 41). According to Patent Owner, the AND gate output “is a new signal generated from the conjunction of the brightness control signal E and the control signal W, not

⁸ Although Patent Owner’s contention is part of its argument that Petitioner fails to demonstrate how claim 14 is anticipated by or obvious over Thomas, we treat it as an argument that Petitioner fails to demonstrate that claim 17 is anticipated by or obvious over Thomas for the same reason.

the brightness control signal E itself.” PO Sur-Reply 8. This differs from the ’148 patent, Patent Owner argues, “where the PWM brightness control signal is applied *directly* to the current set circuit.” *Id.* at 9.

Patent Owner’s arguments do not dissuade us from finding Thomas discloses all the limitations of claim 17. First, claim 17 simply requires the claim 14 step of “applying a different staggered PWM brightness control signal[] to each current set circuit” to “comprise[] applying each staggered PWM brightness control signal[] to an associated transistor.” Ex. 1001, 8:27–31. It does not require *directly applying* the PWM brightness control signal to the transistor. Second, because claim 17 is open-ended, it does not prohibit *indirectly applying* a PWM brightness control signal (e.g., E) to transistor 33 via AND gate 32, which simply enables or inhibits applying that signal to the transistor based on a control signal (e.g., W). *See* Ex. 1005, 3:28–42, Figs. 1, 2 (disclosing control signals W–Z and stating that “[w]hen the gating control logic (32) is *enabled* by receiving a high control signal [e.g., W], they generate output to their respective transistors (33) for driving the transistors (33) on and off”) (emphasis added). Thus, when control signal W is high, AND gate 32 is enabled to output the signal at its other input (i.e., PWM signal E) to transistor 33. When enabled, AND gate 32’s output has the same functional form or modulation as PWM signal E. Patent Owner does not dispute this, as evidenced from the following colloquy with Patent Owner’s counsel, Mr. Alberti, during the oral hearing:

JUDGE HORVATH: Yeah, I -- and this is Judge Horvath again. I just want to -- so, I mean, if that [signal W] enables it, well, I’m [saying it] enables it, if the top signal into the AND gate was a one, right, then the output from the AND gate is going to have at least the same functional form, would you agree as the signal E? If E is high, the output of the AND gate will be high. If E is low,

the output of the AND gate will be low. Would you agree with that?

MR. ALBERTI: If it were fixed as a single, say it was one the entire time, would the output, would the waveform look similar? So, of course there's going to be inherent impedance and all that kind of stuff. The waveform would look similar. It would be a different signal, but the waveform would look similar if the AND gate, if the one gate was set to a one all the time

Tr. 37:23–38:9.

Although the signal output by AND gate 32 may differ from PWM signal E when control signal W is low, it does not differ when control signal W is high. Thus, the output of AND gate 32 is the PWM signal E at least some of the time, which is all that is required for anticipation. *See Hewlett-Packard Co. v. Mustek Sys., Inc.*, 340 F.3d 1314, 1326 (Fed. Cir. 2003) (finding “a prior art product that sometimes, but not always, embodies a claimed method nonetheless teaches that aspect of the invention”).

For the reasons discussed above, we find Petitioner demonstrates by a preponderance of evidence that Thomas anticipates claim 17. Moreover, because claim 17 depends from claim 14, Petitioner demonstrates by a preponderance of evidence that claim 14 is anticipated by Thomas. *See Soverain Software LLC v. Victoria’s Secret Direct Brand Mgmt., LLC*, 778 F.3d 1311, 1315 (finding an “invalidity determination as to claim 41 *extended to* claim 15” from which claim 41 depended) (emphasis added); *Callaway Golf Co. v. Acushnet Co.*, 576 F.3d 1331, 1344 (Fed. Cir. 2009) (“A broader independent claim *cannot be nonobvious* where a dependent claim stemming from that independent claim is invalid for obviousness.”) (emphasis added); *Ormco Corp. v. Align Tech., Inc.*, 498 F.3d 1307, 1319 (Fed. Cir. 2007) (finding that “[b]ecause [dependent] claims 10 and 17 were

found to have been obvious, the broader [independent] claims 1 and 11 *must also have been obvious.*”) (emphasis added).

5. *Claims 18, 20, and 21*

Claim 18 depends from claim 14 and requires generating the staggered PWM brightness control signals by storing bits corresponding to the signals’ duty cycle in a shift register, using a clock to shift the bits along the shift register, and tapping the staggered PWM brightness control signals off of different bit positions along the shift register. Ex. 1001, 8:35–45.

Petitioner contends Thomas discloses these limitations because Thomas implements delay means 16 (Figure 1) as a 12-bit shift register that “stores bits corresponding to the duty cycle of the PWM signal E.” Pet. 33, 44 (citing Ex. 1005, 3:68–4:5, 4:17–32, Fig. 2; Ex. 1003 ¶ 75). Petitioner contends Thomas generates staggered PWM signals F–H from the shift register by tapping it at different bit positions. *Id.* at 35 (citing Ex. 1005, 4:17–28, Fig. 2; Ex. 1003 ¶ 79). Relying on the testimony of Dr. Zane, Petitioner further contends that “a clock is necessarily present within Thomas’ LED driver circuit and connected to Thomas’ shift register” because (1) “Thomas discloses a clock through its disclosure of a ‘time delay’ for the staggered PWM signals” and (2) “all shift registers have a clock connected to them for shifting the bits.” *Id.* at 34–35 (citing Ex. 1005, 4:17–39; Ex. 1003 ¶¶ 76–78) (quoting Ex. 1008, 525; Ex. 1011, 114).

Patent Owner disputes Petitioner’s contention that Thomas inherently anticipates claim 18 because “[a]ll shift registers *must* have a clock connected to them for shifting the bits.” PO Resp. 19 (quoting Pet. 34).⁹

⁹ Although Patent Owner makes this argument with respect to claim 7, we treat it as equally applicable to claim 18, which contains a substantially similar limitation.

Relying on the testimony of Mr. Credelle, Patent Owner argues “shift registers without clocks are not only possible, but a well-understood electronic circuit with a variety of uses.” *Id.* at 20 (citing Ex. 2002 ¶¶ 47–50). As an example, Patent Owner and Mr. Credelle identify Figure 12.4 of Morris,¹⁰ which is further discussed below. *Id.* (citing Ex. 1011, Fig. 12.4).

Petitioner responds that although “a shift register without a clock might exist in some unrelated application [that] does not rebut inherent anticipation by Thomas’ shift register.” Pet. Reply 20. Petitioner contends that “[t]he fact that Thomas’ shift register has a clock is not a ‘mere possibility; but a *certainty* based on Thomas’ description.” *Id.* Petitioner argues this is so because Figure 3 of Thomas “illustrates how the signals *F*, *G*, and *H* are continuously generated and are aligned in time with each new pulse or lack of pulse from the original modulating signal *E*.” *Id.* at 21 (citing Ex. 1005, Fig. 3; Ex. 1031 ¶¶ 22–23). Relying on the testimony of Dr. Zane, Petitioner argues that because *F*, *G*, and *H* are continuously generated “as the original PWM signal *E* is being fed into the shift register, the shift register must be shifting the bits synchronously with each new pulse or lack of pulse of *E*” and that “[w]ithout a clock, Thomas’ shift register would not be able to shift synchronously with *E*.” *Id.* (citing Ex. 1031 ¶¶ 22–24).

We agree with Petitioner. Although Patent Owner and Mr. Credelle are correct that not all shift registers require a clock to shift bits, that was only one of two arguments Petitioner set forth to explain why Thomas’s shift register was connected to a clock. *See* Pet. 34 (citing Ex. 1005, 4:33–39)

¹⁰ Noel M. Morris, *Digital Electronic Circuits and Systems* 117-18 (1974) (Ex. 1011).

(relying on the “time delay” between signals E–H); Pet. Reply 21 (citing Ex. 1005, 4:19–28, Fig. 3) (relying on the alignment of signals E–H).

Figure 3 of Thomas is reproduced below.

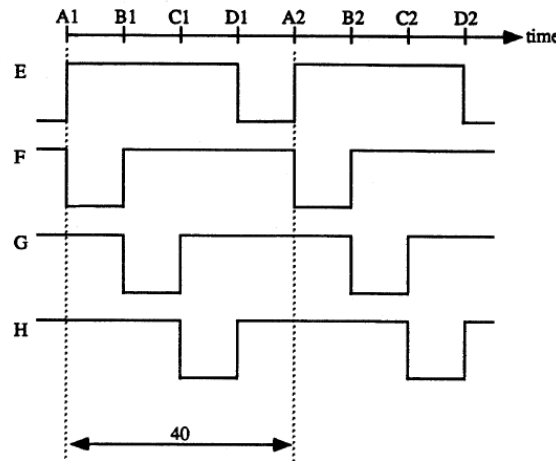


Figure 3 of Thomas is “a timing diagram showing the digital pulses of the first, second, third, and fourth modulating signals in reference to the *period* of the first modulating signal.” *Id.* at 3:6–8 (emphasis added). Thomas discloses choosing a “predetermined” time delay between signals E–H “with respect to the duration of the positive pulses in the first modulating signal (E), as shown in Fig. 3, so that the input of each modulating signal (E, F, G, H) . . . goes high during each *period* 40.” *Id.* at 4:33–39 (emphasis added). “[T]he first modulating signal (E) has a period (40) spanning from time A1 to time A2,” and the “predetermined time” between signals E–H is “one fourth of the period (40) of the first modulating signal (E).” *Id.* at 4:48–53. As a result, “the rising edge of the positive pulses within the modulating signals (E, F, G, H) are *fixed to occur at the designated times*” shown in Figure 3, i.e., as times “A1, B1, C1, and D1, respectively.” *Id.* at 4:55–61 (emphasis added). The signals E–H can only be periodic and the time delay between them can only be “predetermined” if the bits corresponding to signal E are synchronously shifted through the shift register by a clock. We

credit Dr. Zane’s testimony that the bits in Thomas’s shift register must be shifted by a clock signal. *See, e.g.*, Ex. 1031 ¶¶ 22–23; Ex. 2011, 12:10–16:18.

In its Sur-Reply, Patent Owner argues Thomas’s shift register can be implemented as Morris’s “dynamic shift register,” and could shift bits without use of a clock because “Thomas’s modulator could provide shift pulses ϕ_1 and ϕ_2 . . . without changing Thomas’s structure.” PO Sur-Reply 14–17. Petitioner does not dispute that Thomas’s shift register could be implemented as Morris’s “dynamic shift register.” Pet. Reply 22–23. Instead, relying on the testimony of Dr. Zane, Petitioner argues that such an implementation “would still be receiving the signals from ϕ_1 and ϕ_2 synchronously with the PWM signal E—in other words, ϕ_1 and ϕ_2 are a clock signal.” *Id.* (citing Ex. 1003 ¶ 26).

We agree with Petitioner. Figure 12.4 of Morris is reproduced below.

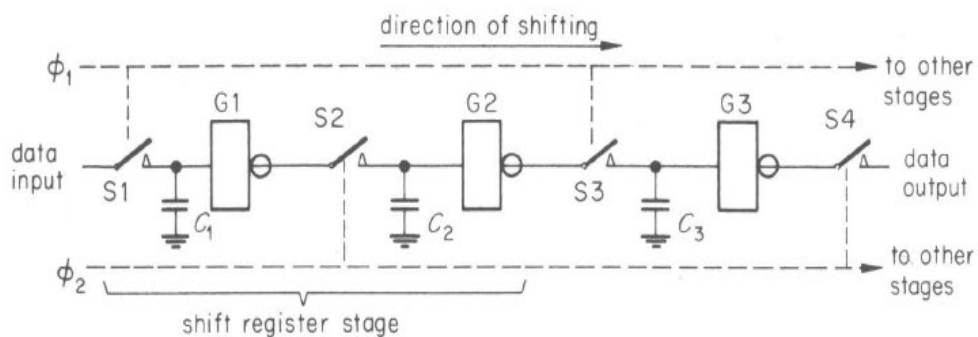


Figure 12.4 of Morris illustrates a first stage and a portion of a second stage of Morris’s dynamic shift register. Ex. 1011, 117–118. The first stage consists of switches S1/S2, capacitors C1/C2 and inverters G1/G2. *Id.* at 117 (disclosing “[t]he memory elements are the inverter stages G1, G2, G3 together with the parasitic gate capacitors C1, C2, C3” and that “[a] complete shift register stage comprises two of these memory elements [e.g., C1/G1 and C2/G2] and two MOS[] switches [e.g., S1/S2] which are turned

ON and OFF by signals ϕ_1 and ϕ_2 ”). The portion of the second stage consists of switches S3/S4, capacitor C₃ and inverter G3; missing is a second memory element, such as a capacitor C₄ and inverter G4.

Morris discloses that signals ϕ_1 and ϕ_2 are complementary—when one is high the other is low—so that “the two switches associated with each memory [e.g., S1/S2] are never closed simultaneously.” *Id.* Morris further discloses that when ϕ_1 is high, switch S1 in stage 1 closes so that “data on the input line is transferred to capacitor C₁” and switch S3 in stage 2 closes so that “data stored in G2 [stage 1] is transferred into G3 [stage 2],” i.e., new data is shifted into the input memory C1/G1 of stage 1 and the data currently stored in stage 1 memory C2/G2 is shifted into stage 2 input memory C3/G3. *Id.* at 118. When ϕ_2 is high, switch S2 in stage 1 closes so that “the input data [is] transferred into the first stage of the register” (i.e., data is transferred from stage 1 input memory C1/G1 to stage 1 memory C2/G2). *Id.* Left unsaid, when ϕ_2 is high, switch S4 in stage 1 also closes so that the data previously shifted from stage 1 memory C2/G2 into stage 2 input memory C3/G3 is transferred to stage 2 memory C4/G4 (not shown). *Id.*

Although Morris discloses ϕ_1 and ϕ_2 are generated by a two-phase pulse supply, Morris does not disclose whether ϕ_1 and ϕ_2 are generated periodically or aperiodically. We are persuaded by Dr. Zane’s testimony that implementing Thomas’s shift register as Morris’s dynamic shift register would require ϕ_1 and ϕ_2 to be generated periodically in order to synchronously shift the bits corresponding to periodic PWM signal E through the shift register over predetermined period 40, making ϕ_1 and ϕ_2 “a two-phase clock signal.” Ex. 1031 ¶ 26.

For the reasons discussed above, we find Petitioner demonstrates by a preponderance of evidence that Thomas discloses all the limitations of claim 18 and anticipates claim 18.

Claim 20 depends from claim 18, and requires serially loading the bits corresponding to the duty cycle of the PWM brightness control signal into the first bit position of the shift register, then using the clock to shift the bits. Ex. 1001, 8:49–52. Petitioner contends Thomas teaches these limitations because Thomas “sequentially stor[es] twelve binary values corresponding to the pulses or lack of pulses in the first modulating signal (E)” and continuously loads these bits into the shift register because signal E is periodic with period 40 as shown in Figure 3. Pet. 37–39, 44 (citing/quoting Ex. 1005, 4:17–28, Figs. 2, 3; Ex. 1003 ¶¶ 81–82). Patent Owner, other than disputing whether Thomas inherently discloses a clock, does not dispute Petitioner’s contentions. PO Resp. 7–21; PO Sur-Reply 3–17.

We find Petitioner demonstrates by a preponderance of evidence that Thomas uses a clock to serially load the bits corresponding to the duty cycle of PWM signal E into its shift register and, therefore, anticipates claim 20. We disagree with Patent Owner’s argument that Thomas does not inherently disclose the use of a clock for the reasons discussed above.

Claim 21 depends from claim 18, and requires the clock to shift the bits in the shift register at a rate of N times the frequency of the PWM brightness control signal, where N is the number of bits representing the duty cycle of the PWM brightness control signal. Ex. 1001, 8:49–52. Petitioner contends Thomas’s PWM signal E is a 12-bit signal ($N=12$) having a period T so “the clock must shift the bits in the shift register 12 times in the period T .” Pet. 39–40, 44 (citing Ex. 1005, 4:17–23, Fig. 2; Ex. 1003 ¶¶ 83–84). Consequently, Petitioner argues, the clock frequency is

$12/T = 12f = Nf$. *Id.* at 40 (citing Ex. 1003 ¶ 84). Patent Owner, other than disputing whether Thomas inherently discloses a clock, does not dispute Petitioner's contentions. PO Resp. 7–21; PO Sur-Reply 3–17.

We find Petitioner demonstrates by a preponderance of evidence that Thomas uses a clock to serially load the bits corresponding to the duty cycle of PWM signal E into its shift register at a rate that is 12 times the frequency of PWM signal E and, therefore, anticipates claim 21. We disagree with Patent Owner's argument that Thomas does not inherently disclose the use of a clock for the reasons discussed above.

6. Claim 22

Claim 22 depends from claim 14 and requires the plurality of parallel paths to comprise at least three paths. Ex. 1001, 8:57–58. Petitioner demonstrates how Thomas has four parallel LED paths 9–12, which are at least three paths. Pet. 17–32, 41, 45 (citing Ex. 1005, Figs. 1, 2). Patent Owner does not dispute this. PO Resp. 5–29; PO Sur-Reply 3–19. We agree with Petitioner and find Petitioner demonstrates by a preponderance of evidence that Thomas anticipates claim 22.

F. Obviousness over Thomas

Petitioner contends claims 1, 3, 6, 7, 9–12, 14, 17, 18, and 20–22 would have been obvious over Thomas. Pet. 45–50. Patent Owner disputes this. PO Resp. 21–28. For the reasons explained below, we find Petitioner demonstrates by a preponderance of evidence that claims 1, 6, 7, 9, and 10 would have been obvious over Thomas and do not reach the remaining claims.

1. Claims 1 and 6

Petitioner contends that to the extent claim 1 is not anticipated by Thomas it would have been obvious over Thomas because any differences

between “Thomas and Claim 1 are such that Claim 1 as a whole would have been obvious to a POSITA as of the time of the invention.” Pet. 45. Patent Owner argues this “bare, conclusory statement . . . falls far short of meeting Petitioner’s burden for proving obviousness” because it “cannot remedy the . . . deficiencies” in Petitioner’s anticipation analysis and “does not address any specific elements” of claim 1 that are allegedly missing from Thomas. PO Resp. 21–22. Petitioner replies that claim 1 would have been obvious over Thomas because it is anticipated by Thomas and “a reference that anticipates also renders the claim obvious.” Pet. Reply 23 (citing *Realtime Data*, 912 F.3d at 1373).

As discussed above, we find on the record before us that Petitioner has failed to demonstrate that Thomas anticipates claim 1. *See* § II.E.2, *supra*. Given Petitioner’s argument that claim 1 would have been obvious over Thomas because it is anticipated by Thomas, Petitioner’s failure to demonstrate anticipation would ordinarily be a failure to demonstrate obviousness as well. However, claim 6 depends from claim 1 and expressly requires each current set circuit to include “a current set resistor . . . and a PWM brightness control transistor” to which the PWM brightness control signal is applied. Ex. 1001, 7:11–20. Petitioner’s analysis of claim 6, discussed below, demonstrates how Thomas discloses these limitations and “cures” the defect in Petitioner’s claim 1 analysis by identifying transistor 33 as a component of claim 1’s “current set circuit” to which a staggered PWM control signal is applied.

Petitioner’s analysis of claim 6 is most easily understood by reference to Petitioner’s annotation of Figure 2 of Thomas, which is reproduced below. Pet. 46–50.

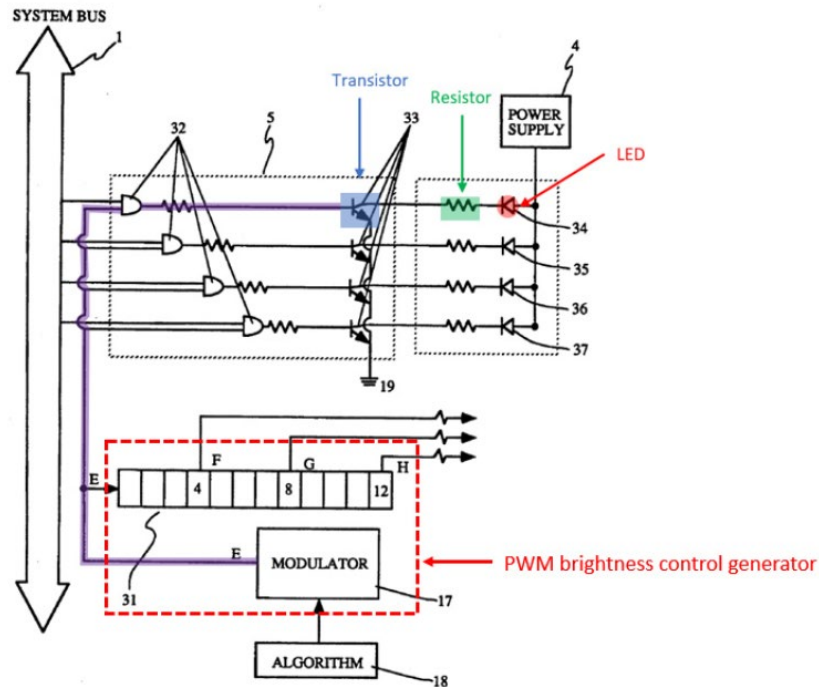


Fig. 2

Petitioner's annotated version of Figure 2 of Thomas is "a partial circuit diagram of the [Figure 1] invention showing one group of four LED's with their respective control lines and control devices."¹¹ Ex. 1005 2:66–3:5.

Claim 6, by virtue of its dependency from claim 1, contains all the limitations of claim 1. 35 U.S.C. § 112 ¶ 4. It recites an LED driver for driving LEDs connected to different parallel paths. Ex. 1001, 6:35–36, 7:11–12. Petitioner demonstrates how Figures 1 and 2 of Thomas disclose

¹¹ Petitioner contends each of the four LED paths shown in Figure 1 consists of the four LED sub-paths shown in Figure 2, and identifies "four of the 16 total parallel sub-paths," one from each LED path shown in Figure 1, as the recited plurality of LED paths. Pet. 18–23 (citing Ex. 1005, Figs. 1, 2; Ex. 1003 ¶¶ 55–58); *id.* at 22 (illustrating the 16 parallel sub-paths and the 4 sub-paths upon which Petitioner's contentions rely). Patent Owner does not dispute this contention, with which we agree.

an LED driver that drives 16 parallel LED paths.¹² Pet. 17–23 (citing Ex. 1005, 2:18–21, 3:3–5, 3:12–15, 3:24–45, 5:11–13, Figs. 1, 2). Patent Owner does not dispute this. PO Resp. 5–29; PO Sur-Reply 3–19.

Claim 6 requires the LED driver to include a voltage source connected to first ends of the LEDs in the plurality of parallel paths. Ex. 1001, 6:37–38. Petitioner demonstrates how Figures 1 and 2 of Thomas illustrate Thomas’s LED driver includes power supply 4 (a voltage source) connected to the first ends of parallel LED groups 9–12, each group consisting of parallel LED strings 34–37. Pet. 23–25 (citing Ex. 1005, 3:12–15, 3:42–45, Figs. 1, 2). Patent Owner does not dispute this. PO Resp. 5–29; PO Sur-Reply 3–19.

Claim 6 further requires the LED driver to include a plurality of current set circuits, one per parallel path, for controlling a peak current through the LEDs in each parallel path, where the current set circuit includes a current set resistor in series with the LEDs and a PWM brightness control transistor in series with and between the LEDs and the current set resistor. Ex. 1001, 6:39–42, 7:11–17.

Petitioner identifies the resistor (green) in Thomas’s Figure 2 as a “current set resistor” in series with an LED (red) and transistor 33 (blue) that sets the current in the LED path. Pet. 25–26, 42 (citing Ex. 1005, Figs. 1, 2; Ex. 1003 ¶¶ 62–63, 95). Petitioner contends that when “transistors 33 are turned on, they ‘provide current from the power supply (4) for activating the associated LED’s (34–37) in the group of LED’s (9).” *Id.* at 43 (quoting Ex. 1005, 3:42–45). Relying on the testimony of Dr. Zane, Petitioner

¹² Because Petitioner demonstrates how Thomas discloses the preamble, we need not decide whether the preamble is limiting.

contends that when current flows through each of the parallel LED strings the resistors in each string

limit the current flowing through each of the parallel paths of LEDs to a peak current I , based on the resistance R of the resistor, the voltage V output by the power supply, [and] the voltage drop across the LED [according to] the equation $I = (V - V_{LED})/R$.

Id. at 26 (citing Ex. 1003 ¶ 63). Patent Owner does not dispute these contentions. PO Resp. 5–29; PO Sur-Reply 3–19.

Petitioner identifies transistor 33 in Thomas’s Figure 2 as a PWM brightness control transistor but admits that “Thomas does not disclose that the transistors are connected in series *between* the current set resistors and the LEDs in each parallel path.” *Id.* at 48–49 (citing Ex. 1005, Fig. 2). However, relying on the testimony of Dr. Zane, Petitioner contends a person skilled in the art “would have understood that the relative placement of the transistors with respect to the resistors and LEDs in each parallel path can be swapped with no change in functionality.” *Id.* at 49 (citing Ex. 1003 ¶ 113). Thus, Petitioner contends, it would have been obvious to modify Thomas’s Figure 2 by moving the resistor in the LED-resistor-transistor path to yield claim 6’s alternate topology of an LED-transistor-resistor path.

Petitioner contends a person skilled in the art would have found it obvious to make this modification because “[t]he three circuit elements (transistor, LED, and resistor) can be arranged in six ways, each of which would have operated the same way” making the modification “a simple design choice among only six possibilities that work the same way.” *Id.* at 49–50 (citing Ex. 1003 ¶ 113). Petitioner further contends a POSITA would have found the modification obvious because it allows easy measurement of the current flowing through the LEDs by “measur[ing] the voltage before the

resistor;” the current having a value of V_R/R where V_R is the voltage across the resistor. *Id.* at 50. Patent Owner does not dispute these contentions. PO Resp. 5–29; PO Sur-Reply 3–19.

Claim 6 further requires the LED driver to include a PWM brightness control signal generator connected to the plurality of current set circuits configured to generate staggered PWM brightness control signals to the plurality of current set circuits. Ex. 1001, 6:43–47. Petitioner identifies Thomas’s delay means 16, pulse width modulator 17, and algorithm 18 as the “pulse-width modulated (PWM) brightness control signal generator” that generates “staggered PWM brightness control signals” E–H. Pet. 27–29, 46 (citing Ex. 1003 ¶¶ 64–66). Patent Owner does not dispute these contentions. PO Resp. 5–29; PO Sur-Reply 3–19.

Claim 6 further requires the PWM brightness control transistors in each path to be connected to the PWM brightness control signal generator and to receive the staggered PWM brightness control signals. Ex. 1001, 7:17–20. Petitioner contends “different staggered PWM signals are applied to the plurality of current set circuits via the switches 5–8.” *Id.* at 29 (citing Ex. 1003 ¶ 66). Patent Owner disputes this, arguing that Thomas’s signals E–H are applied “*to the AND gates 32*” and are “*not applied to the transistor*” Petitioner identifies as the PWM brightness control transistor. PO Sur-Reply 7–8.¹³ This is essentially the same argument Patent Owner made regarding a similar limitation recited in claim 17, discussed in § II.E.4,

¹³ Although Patent Owner’s argument is part of its contention that Petitioner fails to demonstrate how claim 1 is anticipated by or would have been obvious over Thomas, we treat it as an argument that Petitioner fails to demonstrate that claim 6 is anticipated by or would have been obvious over Thomas for the same reason.

supra, which does not dissuade us from finding Petitioner demonstrates by a preponderance of evidence how Thomas meets this limitation for the reasons discussed there.

Finally, claim 1 requires each current set circuit of the LED driver be configured to draw the peak current through its LEDs at a duty cycle substantially corresponding to a duty cycle of the PWM brightness control signal applied to it but out of phase with the other current set circuits. Ex. 1001, 6:48–54. Petitioner contends Figure 3 of Thomas illustrates that PWM control signals E–H have the same duty cycle but different phases and control “the perceived brightness of the LEDs . . . when they are ‘on’” or “high.” Pet. 31 n.6 (citing Ex. 1003 ¶ 69); *id.* at 32 (citing Ex. 1005, Fig. 3; Ex. 1003 ¶ 71). Petitioner further contends that when control signals W–Z are “on” or “high,” they enable or turn “on” the LEDs. *Id.* at 31 n.6 (citing Ex. 1003 ¶ 69). Finally, Petitioner contends that when control signals W–Z are high and PWM brightness control signals E–H are fed into activation switches 5–8, “[t]he switches activate their respective parallel paths (allowing current to flow through the current set circuit) when the switches receive a high pulse from the PWM signal[s].” *Id.* at 31 (citing Ex. 1005, 3:24–63, 5:3–10; Ex. 1003 ¶¶ 67, 68, 70). Thus, Petitioner contends, the “current set circuits in each parallel path draw their peak currents at a duty cycle that corresponds to the duty cycle of the PWM brightness signal (*E*, *F*, *G*, or *H*) that are applied to them.” *Id.* at 31–32 (citing Ex. 1005, 3:2863, 4:66–5:10; Ex. 1003 ¶ 70).

Patent Owner, apart from contending that Thomas’s control signals E–H are applied to AND gates 32 in switches 5 rather than to a current set circuit transistor as required by claim 6, does not dispute Petitioner’s contentions. PO Resp. 5–29; PO Sur-Reply 3–19. We find Petitioner

demonstrates by a preponderance of evidence that Thomas's signals are applied to transistors 33 for the reasons explained in § II.E.4, *supra*.

For the reasons discussed above, we find Petitioner demonstrates by a preponderance of evidence that claim 6 would have been obvious over Thomas. Moreover, because claim 6 depends from and contains all the limitations of claim 1, we find Petitioner's claim 6 obviousness analysis demonstrates by a preponderance of evidence that claim 1 also would have been obvious over Thomas. *See Soverain Software*, 778 F.3d at 1315 (finding the invalidity of a dependent claim extends to the claims from which it depends); *Callaway Golf*, 576 F.3d at 1344 (same); *Ormco*, 498 F.3d at 1319 (same).

2. *Claim 7, 9, and 10*

Claim 7 recites the driver of claim 1 comprising a shift register and clock performing the same functions recited in claim 18 (storing bits corresponding to the duty cycle of a PWM brightness control signal, using a clock to shift the bits, and tapping the shift register at different bit positions to generated phase-shifted PWM brightness control signals). *Compare* Ex. 1001, 7:21–31, *with id.* at 8:35–45. For the reasons discussed above, we find Petitioner demonstrates claim 1 would have been obvious over Thomas. Moreover, for the reasons discussed in § II.E.5, *supra*, we find Thomas discloses all the claim 7 limitations that are common to claim 18 despite Patent Owner's arguments to the contrary. Accordingly, we find Petitioner demonstrates by a preponderance of evidence that claim 7 would have been obvious over Thomas.

Claim 9 recites the driver of claim 7 performing the same functions recited in claim 20 (serially and continuously loading bits corresponding to the duty cycle of a PWM brightness control signal into the shift register's

first bit position and using a clock to shift the bits). *Compare* Ex. 1001, 7:36–39, *with id.* at 8:49–52. For the reasons discussed above, we find Petitioner demonstrates claim 7 would have been obvious over Thomas. Moreover, for the reasons discussed in § II.E.5, *supra*, we find Thomas discloses all the claim 9 limitations that are common to claim 20 despite Patent Owner’s arguments to the contrary. Accordingly, we find Petitioner demonstrates by a preponderance of evidence that claim 9 would have been obvious over Thomas.

Claim 10 recites the driver of claim 7 performing the same functions recited in claim 21 (shifting the N bits corresponding to the duty cycle of a PWM brightness control signal at a rate that is N times the frequency of the PWM brightness control signal). *Compare* Ex. 1001, 7:41–44, *with id.* at 8:53–56. For the reasons discussed above, we find Petitioner demonstrates claim 7 would have been obvious over Thomas. Moreover, for the reasons discussed in § II.E.5, *supra*, we find Thomas discloses all the claim 10 limitations that are common to claim 21 despite Patent Owner’s arguments to the contrary. Accordingly, we find Petitioner demonstrates by a preponderance of evidence that claim 10 would have been obvious over Thomas.

3. *Claims 3, 11, 12, 14, 17, 18, and 20–22*

We need not determine whether these claims would have been obvious over Thomas because we find Petitioner demonstrates they are anticipated by and would have been obvious over Zane. *See Beloit Corp. v. Valmet Oy*, 742 F.2d 1421, 1423 (Fed. Cir. 1984) (finding an administrative agency is at liberty to reach a decision based on a single dispositive issue).

4. *Claims 14, 17, 18, and 20–22*

We need not determine whether these claims would have been obvious over Thomas because we find Petitioner demonstrates they are anticipated by Thomas. *See Beloit Corp.* 742 F.2d at 1423.

G. *Obviousness over Thomas and AAPA*

Petitioner contends claims 2, 13, and 15 would have been obvious over Thomas and AAPA. Pet. 51–57. Patent Owner disputes this. PO Resp. 21–28. We need not determine whether these claims would have been obvious over Thomas and AAPA because we find Petitioner demonstrates claim 2 is anticipated by Zane and claims 2, 13, and 15 would have been obvious over Zane. *See Beloit*, 742 F.2d at 1423.

H. *Obviousness over Thomas and Tatewaki*

Petitioner contends claims 8 and 19 would have been obvious over Thomas and Tatewaki. Pet. 57–60. Patent Owner disputes this. PO Resp. 21–28. For the reasons explained below, we find Petitioner demonstrates by a preponderance of evidence that these claims would have been obvious over Thomas and Tatewaki.

1. *Tatewaki*

Tatewaki discloses a “vehicle room lamp that illuminates the interior of a vehicle such as an automobile.” Ex. 1007, 1:5–6. The room lamp is LED based and controlled by a “PWM control circuit 162 [that] connects [an] on-off switch 163 and mode switch 164 to a microcomputer or MPU.” *Id.* at 12:19–20. The MPU “lowers a battery voltage (12V) to an LED drive voltage (5V) and outputs LED drive pulses . . . at a predetermined duty ratio via a PWM output circuit.” *Id.* at 12:27–30. When “on-off switch 163 is activated, a ring counter installed in the PWM control circuit 162 operates so

that a duration of the on and off of the LED chip 132, 142 is changed, thereby controlling the [LED] brightness.” *Id.* at 13:34–37.

2. *Claims 8 and 19*

Claim 8 depends from claim 7, and requires the shift register to connect its last bit position to its first bit position so that the bits in the shift register are recirculated. Ex. 1001, 7:32–35. Claim 19 is a method claim that depends from claim 18, and contains a similar limitation. *Id.* at 8:46–48. For the reasons discussed in §§ II.F.2 and II.E.5, *supra*, Petitioner demonstrates by a preponderance of evidence that claim 7 would have been obvious over Thomas and claim 18 would have been anticipated by Thomas.

Petitioner admits that Thomas does not disclose recirculating the bits in its shift register by shifting the output bit in the last bit position back into the first bit position of Thomas’s shift register. Pet. 57. However, relying on the testimony of Dr. Zane, Petitioner argues “it would have been obvious to modify Thomas’ shift register to connect the end bit position to the first bit position so that the shift register recirculates the bits in the shift register.” *Id.* at 57 (citing Ex. 1003 ¶ 138). Petitioner contends a person skilled in the art would have known that shift registers can recirculate bits from the last bit position to the first bit position and that “[r]ecirculating shift registers are known in the art as ‘ring counters.’” *Id.* (citing Ex. 1003 ¶ 139; Ex. 1010, 1:17–27; Ex. 1011, 119, Fig. 12.6). For example, Petitioner argues, Tatewaki demonstrates that it was known to use ring counters in LED drivers to generate PWM signals to control LED brightness. *Id.* at 58–59 (citing Ex. 1003 ¶ 140; Ex. 1007, 12:11–30, 13:25–47).

Petitioner further supports its contention by reference to Figure 12.6 of Morris (Ex. 1011), which is reproduced below. *Id.* at 58.

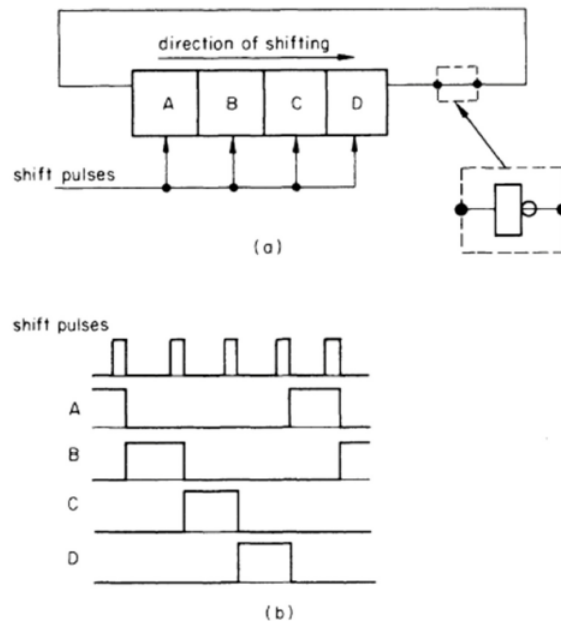


Fig. 12.6 A ring counter

Figure 12.6 of Morris (Ex. 1011, 119) illustrates a 4-bit ring counter that recirculates a bit through the four positions of a 4-bit shift register (designated A–D) by connecting the shift register’s last bit position (D) to the shift register’s first bit position (A). Morris discloses “[a] ring counter is simply a shift register whose input is derived directly from its output, in the manner shown in Figure 12.6.” Ex. 1011, 119.

Patent Owner does not dispute Petitioner’s contentions, with which we agree. PO Resp. 21–28; PO Sur-Reply 17–19. “[W]hen a patent ‘simply arranges old elements with each performing the same function it had been known to perform’ and yields no more than one would expect from such an arrangement, the combination is obvious.” *KSR*, 550 U.S. at 417.

Accordingly, for the reasons discussed above, we find Petitioner demonstrates by a preponderance of evidence that claims 8 and 19 would have been obvious over Thomas and Tatewaki.

I. Petitioner's Motion to Strike

Petitioner moves to strike an exhibit that was introduced during the deposition of Dr. Zane and is attached to his deposition transcript, as well as two sentences in Patent Owner's Sur-Reply. Mot. 1. Petitioner contends the exhibit—a dictionary definition of “strobe”—is an attempted end-run around the Board's rules prohibiting Patent Owner from filing any new evidence other than deposition transcripts in its Patent Owner Sur-Reply. Mot. 1 (citing 37 C.F.R. § 42.23(b)). Petitioner contends Patent Owner introduced the exhibit into the deposition transcript so that it could rely on it “in its sur-reply to present a new merits argument that a shift signal does not necessarily have to be a clock signal.” *Id.* at 2–3. Because Petitioner contends Patent Owner could have presented this argument in its Patent Owner Response, Petitioner moves to strike not only the exhibit but lines 4–7 on page 16 of Patent Owner's Sur-Reply. *Id.* at 3–4.

Patent Owner opposes, arguing the objected to lines of its Sur-Reply are “properly responsive to arguments raised for the first time in Petitioner's Reply and Dr. Zane's Reply Declaration.” Opp. 1. Patent Owner further argues the dictionary definition of “strobe” and the cited portions of Dr. Zane's deposition testimony are consistent with arguments made in Patent Owner's Response, namely, that shift registers do not inherently require clocks to shift bits. *Id.* at 1–2.

We need not resolve this dispute and dismiss Petitioner's Motion to Strike as moot for the following reason. One of the issues disputed by the parties was whether all shift registers require a clock to shift bits. *See* Pet. 34 (“All shift registers **must** have a clock connected to them for shifting the bits.”); PO Resp. 20 (“[S]hift registers without clocks are not only possible, but a well-understood electronic circuit with a variety of uses.”). We

resolved that dispute in § II.E.5, *supra*, finding Thomas inherently discloses using a clock to shift the bits corresponding to PWM signal E through a shift register because a clock would be needed to ensure signal E was periodic with period 40 as disclosed by Thomas. That is, we resolved the parties dispute without reference to the dictionary definition of “strobe” Patent Owner introduced during Dr. Zane’s deposition. Accordingly, we dismiss Petitioner’s motion to strike as moot.

III. CONCLUSION

We have reviewed the Petition, Patent Owner Response, Petitioner Reply, and Patent Owner Sur-Reply. We have considered all of the evidence and arguments presented by Petitioner and Patent Owner. We find, on this record, Petitioner has demonstrated by a preponderance of evidence that claims 1–22 of the ’148 patent are unpatentable.

We have also reviewed Petitioner’s Motion to Strike and Patent Owner’s Opposition to the motion. On this record, we *dismiss as moot* Petitioner’s Motion to Strike.

Claims	35 U.S.C. §	Reference(s) /Basis	Claims Shown Unpatentable	Claims Not Shown Unpatentable
1, 3, 7, 9–12, 14, 17, 18, 20–22	102(b)	Thomas	14, 17, 18, 20–22	1, 3, 7, 9–12
1, 3, 6, 7, 9–12, 14, 17, 18, 20–22	103(a)	Thomas ¹⁴	1, 6, 7, 9, 10	
2, 13, 15	103(a)	Thomas,		

¹⁴ We need not determine whether claims 3, 11, 12, 14, 17, 18, and 20–22 would have been obvious over Thomas because we find these claims unpatentable on other grounds.

		AAPA ¹⁵		
8, 19	103(a)	Thomas, Tatewaki	8, 19	
1–4, 11, 12, 14, 17, 22	102(b)	Zane	1–4, 11, 12, 14, 17, 22	
1–5, 11–17, 22	103(a)	Zane	1–5, 11–17, 22	
Overall Outcome			1–22	

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that Petitioner has shown that claims 1–22 of the '148 patent are unpatentable;

FURTHER ORDERED that this Decision is final, and a party to this proceeding seeking judicial review of the Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2; and

FURTHER ORDERED that Petitioner's Motion to Strike (Paper 26) is *dismissed* as moot.

¹⁵ We need not determine whether claims 2, 13, and 15 would have been obvious over Thomas in view of AAPA because we find these claims unpatentable on other grounds.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

VIZIO, INC.,
Petitioner,

v.

POLARIS POWERLED TECHs, LLC,
Patent Owner.

IPR2024-00073
Patent 7,843,148 B2

Before JOHN F. HORVATH, DANIEL J. GALLIGAN and
KARA L. SZPONDOWSKI, *Administrative Patent Judges*.

GALLIGAN, *Administrative Patent Judge*, concurring.

I concur that claims 1–22 of the ’148 patent are unpatentable, and I join all of the majority decision except sections II.E.2–3, which find claims 1, 3, 7, and 9–12 not unpatentable as anticipated by Thomas. I would find that Petitioner has presented preponderant evidence that Thomas anticipated claim 1 for the reasons discussed below.

Claim 1 of the ’148 patent is below with Petitioner’s limitation identifiers in brackets (*see* Pet. xvi):

[1.pre] A light emitting diode (LED) driver for driving LEDs connected to different parallel paths,
[1.a] the driver comprising: a voltage source for connection to first ends of LEDs in a plurality of parallel paths;

[1.b] a plurality of current set circuits, one current set circuit per parallel path, each current set circuit controlling a peak current through one or more LEDs connected in each parallel path; and
[1.c] a pulse-width modulated (PWM) brightness control signal generator connected to the plurality of current set circuits, the brightness control signal generator being configured to generate staggered PWM brightness control signals to the plurality of current set circuits,
[1.d] each current set circuit being configured to draw the peak current through its associated one or more LEDs at a duty cycle substantially corresponding to a duty cycle of a PWM brightness control signal applied to it, such that the plurality of current set circuits conduct current through their associated one or more LEDs at the same duty cycle but out of phase with each other.

As relevant to the disputed issues, claim 1 requires “a plurality of current set circuits” (limitation 1.b) with “each current set circuit being configured to draw the peak current through its associated one or more LEDs at a duty cycle substantially corresponding to a duty cycle of a PWM brightness control signal *applied to it*” (limitation 1.d (emphasis added)). In limitation 1.d, there is no dispute that the pronoun “it” refers to each “current set circuit.” Thus, claim 1 requires a PWM brightness control signal to be applied to each current set circuit.

The dispute arises from Petitioner’s contentions with respect to limitation 1.b, in which Petitioner asserts that “the resistors shown in Thomas’ Figure 1 (and more specifically, the individual resistors in each sub-path in Figure 2) are each a current set circuit, and there is one current set circuit per parallel path shown in Figure 1 which controls the peak current through the LED in each parallel path.” Pet. 26.

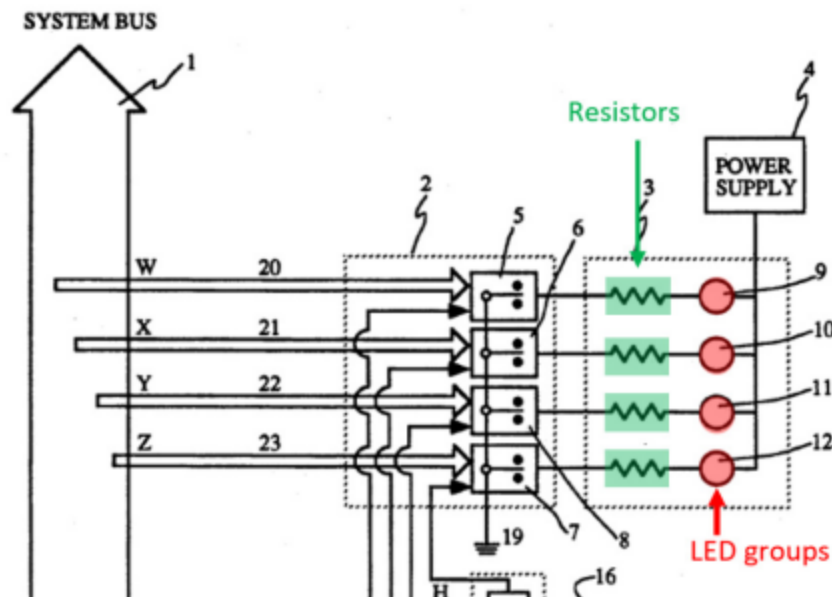
Based on this contention, Patent Owner argues that (1) a resistor alone cannot be a current set circuit because a “circuit” means “*two or more*

components that are connected by conductive material so that current can flow between the components” (PO Resp. 9); and (2) even if the identified resistor is a current set circuit, “the PWM signal is never *applied* to the resistors in Thomas” (PO Resp. 14).

I disagree with Patent Owner’s second argument for the reasons given in section II.E.4 of the majority decision.

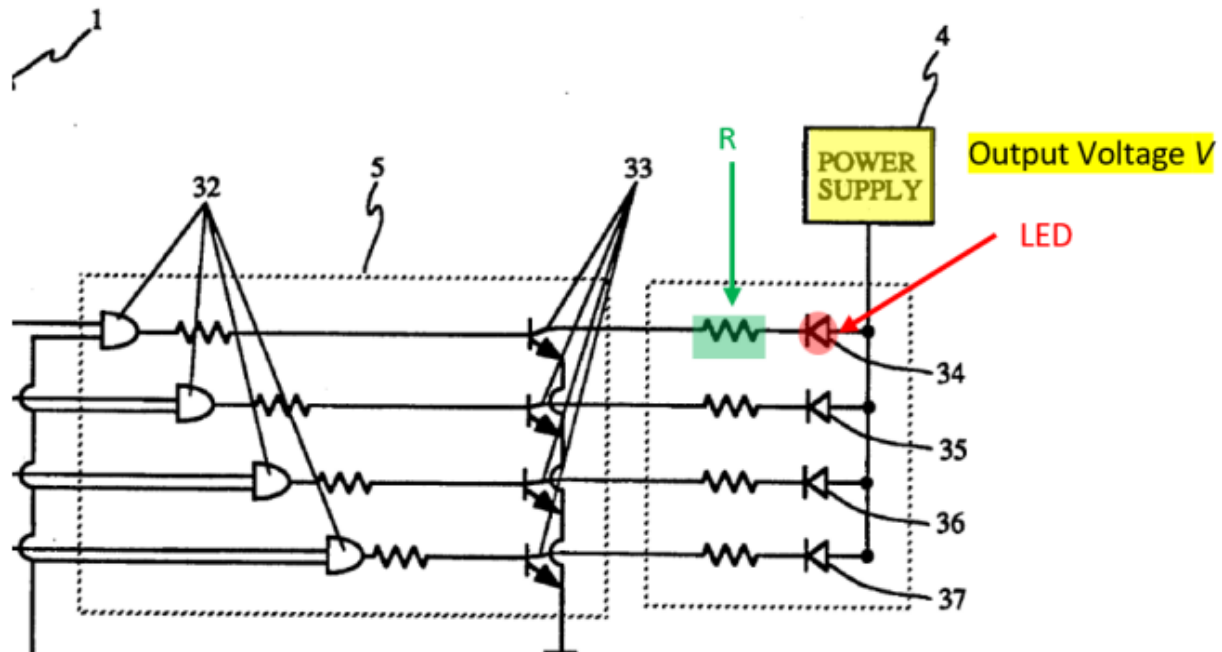
As to Patent Owner’s first argument, Thomas discloses more than a resistor alone, and Petitioner’s contentions as a whole and for limitation 1.b fairly show a circuit of multiple components in each parallel path.

Petitioner asserts that “Thomas’ Figures 1 and 2 show a resistor in series with the LED group in each parallel path.” Pet. 25 (citing Ex. 1003 ¶ 62). Petitioner provides the cropped and annotated version of Thomas’s Figure 1 below (Pet. 25).



The annotated figure above shows a portion of Thomas’s Figure 1, in which Petitioner includes (1) the caption “Resistors” in green with a green arrow pointing to resistors (shaded in green) and (2) the caption “LED groups” in red with a red arrow pointing to LED groups 9–12 (shaded in red). Pet. 25.

Petitioner also provides the cropped and annotated version of Thomas's Figure 2 below (Pet. 26).



The annotated figure above shows a portion of Thomas's Figure 2, in which Petitioner includes (1) the caption "R" in green with a green arrow pointing to a resistor (shaded in green); (2) the caption "LED" in red with a red arrow pointing to LED 34 (shaded in red); and the caption "Output Voltage" next to Power Supply 4 (shaded in yellow). Pet. 26.

For limitation 1.b, Petitioner further asserts the following:

A [person of ordinary skill in the art] would have understood from Thomas' disclosure that the purpose of those resistors is to limit the current flowing through each of the parallel paths of LEDs to a peak current I , based on the resistance R of the resistor, the voltage V output by the power supply, the voltage drop across the LED, and the equation $I=(V-V_{LED})/R$. EX1003, ¶63. Thus, the resistors shown in Thomas' Figure 1 (and more specifically, the individual resistors in each sub-path in Figure 2) are each a current set circuit, and there is one current set circuit per parallel path shown in Figure 1 which controls the peak current through the LED in each parallel path. *Id.*

Pet. 26 (footnote omitted). Petitioner’s footnote states: “ $I=(V-V_{LED})/R$ is the peak current that can flow through the LEDs in this circuit. In practice, the actual current will be slightly less than $(V-V_{LED})/R$. . . due to the voltage drop on the transistor or other parasitic resistances in the circuit. EX1003, ¶63.” Pet. 26 n.4.

Patent Owner is correct that Petitioner expressly asserts that “the resistors shown in Thomas’ Figure 1 (and more specifically, the individual resistors in each sub-path in Figure 2) are each a current set circuit, and there is one current set circuit per parallel path shown in Figure 1 which controls the peak current through the LED in each parallel path.” PO Resp. 8 (quoting Pet. 26). But the first sentence in the block quote above and Petitioner’s footnote 4 provide context for this statement. In particular, the first sentence states that the resistor is what limits the current flowing through each parallel path. Pet. 26 (citing Ex. 1003 ¶ 63). The footnote explains that the current “in this circuit” is given by the equation $I=(V-V_{LED})/R$ but that “the actual current will be slightly less than $(V-V_{LED})/R$. . . due to the voltage drop on the transistor or other parasitic resistances in the circuit.” Pet. 26 n.4. Petitioner’s contentions for limitation 1.b, therefore, assert that the resistors that limit the current flow are in a circuit with the transistor. This makes sense because, as Mr. Credelle testifies with reference to Thomas’s Figure 2, “control transistors 33 . . . are bipolar junction transistors or ‘BJTs’” and “[w]hen the BJTs are turned ‘on,’ current flows from the power supply 4 through the LEDs 34–37 and the resistors (i.e., the alleged current set circuits) to ground 19.” Ex. 2002 ¶ 41.

Notably, Mr. Credelle’s testimony regarding the operation of transistors 33 is similar to Petitioner’s contentions for claim 17, which recites in pertinent part that “applying a different staggered PWM brightness

control signal to each current set circuit comprises applying each staggered PWM brightness control signals to an associated transistor connected in series with the one or more LEDs in an associated parallel path.” For claim 17, Petitioner argues that “Thomas discloses transistors 33 which are connected in series with the current set resistor and the LED in each parallel path” and that “Thomas explains that when the transistors 33 are turned on, they ‘provide current from the power supply (4) for activating the associated LED’s (34-37) in the group of LED’s (9).” Pet. 42–43 (quoting Ex. 1005, 3:42–45; Ex. 1003 ¶ 96).

In its contentions for limitation 1.d, Petitioner asserts that “[t]he current set circuits are further configured to draw that peak current at the duty cycle of the PWM brightness control signal applied to that current set circuit.” Pet. 30. Petitioner further explains as follows:

The switches activate their respective parallel paths (allowing current to flow through the current set circuit) when the switches receive a high pulse from the PWM signal. *Id.* at ¶¶67-68, 70; *see also* EX1005, 3:24-63; 5:3-10. Thus, the current set circuits in each parallel path draw their peak currents at a duty cycle that corresponds to the duty cycle of the PWM brightness signal (*E*, *F*, *G*, or *H*) that are applied to them. EX1005, 3:28-63, 4:66-5:10; EX1003, ¶70.

Pet. 31–32 (footnote omitted). This contention further confirms that the current set circuits in Thomas include the switches and thus are not limited solely to resistors. The annotated and cropped portion of Thomas’s Figure 2 reproduced above shows that transistors 33 are part of switch 5 in Figure 1. *See* Ex. 1005, 3:32–35 (“With reference to FIG. 2, one set of activation switches (5) is comprised of gating control logic (32) forming AND gates and transistors (33) for activating one group of LED’s (9).”).

Thus, although Petitioner asserts that “the resistors shown in Thomas’ Figure 1 (and more specifically, the individual resistors in each sub-path in Figure 2) are each a current set circuit” (Pet. 26), Petitioner’s contentions for limitations 1.b and 1.d show that Petitioner identifies a circuit having a resistor in series with a transistor. In addition, Petitioner’s discussion of the preamble of claim 1 identifies the four paths that describe the claimed “parallel paths,” and Petitioner’s explanation and accompanying annotated figures show a circuit from power to ground in each path, each circuit including an LED, a resistor (which limits current), and a transistor to switch the circuit on and off. Pet. 17–23. This discussion further shows that Petitioner presented preponderant evidence of a current set circuit including a resistor and a transistor in each path.

For these reasons, I would find that Thomas anticipated claim 1.

I would find that Thomas describes the subject matter of, and therefore anticipated, dependent claims 7, 9, and 10 for the reasons given in section II.E.5 of the majority decision, which finds anticipation of claims 18, 20, and 21. I would find that Thomas anticipated claim 11 for the reasons given in section II.E.6 of the majority decision, which finds anticipation of claim 22. I would also find that Thomas describes that “the LEDs [are] connected to the driver,” as shown in Thomas’s Figures 1 and 2, and, therefore, that Thomas anticipated claim 12. *See* Pet. 41.

Because Zane anticipated claim 3, I do not opine on Petitioner’s contention that Thomas anticipated claim 3.

IPR2024-00073
Patent 7,843,148 B2

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