Paper No. _____

UNITED STATES PATENT AND TRADEMARK OFFICE

_____

BEFORE THE PATENT TRIAL AND APPEAL BOARD

_____

Inergy Technology, Inc.,

Petitioner

v.

Force Mos Technology Co., Ltd.,

Patent Owner

Patent No. 7,629,634

Issue Date: December 8, 2009

Title: TRENCHED MOSFET WITH TRENCHED SOURCE CONTACT

Inter Partes Review No. IPR2024-0093

PETITION FOR *INTER PARTES* REVIEW
OF CLAIMS 1-9 OF U.S. PATENT NO. 7,629,634
UNDER 35 U.S.C. §§ 311-319 AND 37 C.F.R. § 42.100 *ET. SEQ.*

TABLE OF CONTENTS

Page

I. INTRODUCTION 1
II. MANDATORY NOTICES 1
- A. Real Parties-in-Interest (37 C.F.R. § 42.8(b)(1)) 1
- B. Related Matters (37 C.F.R. § 42.8(b)(2)) 1
- C. Lead and Back-Up Counsel (37 C.F.R. § 42.8(b)(3)) 2
- D. Service Information (37 C.F.R. § 42.8(b)(4)) 3
- E. Payment of Fees (37 C.F.R. § 41.103) 3

III. REQUIREMENTS FOR IPR UNDER 37 C.F.R. § 42.104 3
- A. Grounds for Standing (§ 42.104(a)) 3
- B. Identification of Challenge and Statement of Precise Relief Requested for Each of the Challenged Claims (§ 42.104(b)) 3

IV. THE ’634 PATENT 4
- A. The ’634 Patent 4
- B. The ’634 Patent File History 8

V. OVERVIEW OF THE PRIOR ART 9
- A. German Patent Publication No. DE 102004009083 (“Hirler”) 9
- B. U.S. Patent Publication No. 2004/0021174 (“Kobayashi”) 11
- C. U.S. Patent Publication No. 2005/0029584 (“Shiraishi”) 13

VI. LEVEL OF ORDINARY SKILL IN THE ART 15
VII. CONSTRUCTION OF THE CLAIMS 15
- A. “the sidewalls of said trenches in said base layer” 17

VIII. CLAIM-BY-CLAIM EXPLANATION OF GROUNDS FOR UNPATENTABILITY 19
- A. Ground 1: Claims 1-2 and 6, are unpatentable under pre-AIA 35 U.S.C. § 102(b) as anticipated by Hirler. 21
  - 1. Claim 1 21
  - 2. Claim 2 27
  - 3. Claim 6 28
- B. Ground 2: Claims 3-5 and 7-9 are unpatentable under 35 U.S.C. § 103 as obvious over Hirler in light of Kobayashi and the knowledge of the POSITA. 29
  - 1. Claim 3 29
  - 2. Claim 4 30
  - 3. Claim 5 30
  - 4. Claim 7 31
  - 5. Claim 8 31
  - 6. Claim 9 32

TABLE OF CONTENTS
(continued)

Page

7. Combining Hirler and Kobayashi in light of knowledge of the POSITA 32

C. Ground 3: Claims 1 and 2 are unpatentable under 35 U.S.C. § 102(b) as anticipated by Shiraishi. 37

1. Claim 1 37
2. Claim 2 41

D. Ground 4: Claims 3-9 are unpatentable under 35 U.S.C. § 103 as obvious over Shiraishi in light of Kobayashi and the knowledge of the POSITA. 42

1. Claim 3 42
2. Claim 4 43
3. Claim 5 44
4. Claim 6 44
5. Claim 7 45
6. Claim 8 45
7. Claim 9 46
8. Combining Shiraishi and Kobayashi in light of knowledge of the POSITA 46

E. Ground 5: Claims 1-9 are unpatentable under 35 U.S.C. § 103 as obvious over Kobayashi in light of Shiraishi and the knowledge of the POSITA. 52

1. Claim 1 52
2. Claim 2 56
3. Claim 3 58
4. Claim 4 58
5. Claim 5 59
6. Claim 6 59
7. Claim 7 60
8. Claim 8 61
9. Claim 9 61
10. Combining Kobayashi and Shiraishi in light of knowledge of the POSITA 62

IX. THE BOARD'S DISCRETION UNDER 35 U.S.C. § 325(d) 66

A. Applicable law 67

B. Petitioner presents substantially different prior art and arguments from those presented by the examiner 68

TABLE OF CONTENTS
(continued)

Page

X. THE ASSERTED GROUNDS ARE NEITHER EXCESSIVE NOR REDUNDANT 70
XI. CONCLUSION 72

EXHIBIT LIST

EXHIBIT NUMBER	DESCRIPTION
1001	U.S. Patent No. 7,629,634 (the "'634 Patent")
1002	File History of the '634 Patent
1003	Declaration of Dr. David Liu
1004	Curriculum Vitae of Dr. David Liu
1005	German Patent Publication No. DE 102004009083 ("Hirler")
1006	Certified English Translation - German Patent Pub. No. DE 102004009083 ("Hirler")
1007	Affidavit of Translation - Hirler
1008	U.S. Patent Publication No. 2004/0021174 ("Kobayashi")
1009	U.S. Patent Publication No. 2005/0029584 ("Shiraishi")
1010	Complaint, *Force Mos Technology, Co. Ltd. v. Asustek Computer, Inc.*, No. 2:22-cv-00460 (E.D. Tex.)
1011	First Amended Complaint, *Force Mos Technology, Co. Ltd. v. Asustek Computer, Inc.*, No. 2:22-cv-00460 (E.D. Tex.), ECF 13
1012	Docket Control Order, *Force Mos Technology, Co. Ltd. v. Asustek Computer, Inc.*, No. 2:22-cv-00460 (E.D. Tex.), ECF 23
1013	Scheduling Order, *Alpha and Omega Semiconductor Limited, et al. v. Force MOS Technology Co. Ltd.*, Civ. No. 5:22-cv-05448 (N.D. Cal.), ECF 37

EXHIBIT NUMBER	DESCRIPTION
1014	Joint Stipulation and Order for Plaintiffs to File Their Second Amended Complaint and Extension of Case Schedule (as modified), *Alpha and Omega Semiconductor Limited, et al. v. Force MOS Technology Co. Ltd.*, Civ. No. 5:22-cv-05448 (N.D. Cal.) (March 23, 2023)
1015	Civil Docket, *Alpha and Omega Semiconductor Limited, et al. v. Force MOS Technology Co. Ltd.*, Civ. No. 5:22-cv-05448 (N.D. Cal.) (Last Accessed October 27, 2023)

I. INTRODUCTION

Petitioner, Inergy Technology, Inc. ("Inergy" or "Petitioner"), respectfully requests institution of an *inter partes* review (IPR) and cancellation of Claims 1-9 ("the Challenged Claims") of U.S. Patent No. 7,629,634 (the "'634 Patent") (Ex. 1001). The Challenged Claims generally relate to a vertical trenched MOSFET with a trenched source contact wherein there is an intermediary layer at the sidewalls of the trench as well as an intermediary layer at the bottom of the trench at the body layer. As detailed in this Petition, the claimed configurations were well-known in the relevant art prior to the effective filing date of the '634 Patent.

II. MANDATORY NOTICES

A. Real Parties-in-Interest (37 C.F.R. § 42.8(b)(1))

Inergy Technology, Inc., Asustek Computer, Inc., and Panjit International Inc. are the real parties-in-interest.

B. Related Matters (37 C.F.R. § 42.8(b)(2))

The '634 Patent is currently the subject of litigation brought by Force Mos Technology Co., Ltd. ("Force Mos" or "Patent Owner") against Asustek in *Force Mos Technology, Co. Ltd. v. Asustek Computer, Inc.*, No. 2:22-cv-00460 (E.D. Tex.) (the "Asustek Action"). The complaint and first amended complaint in the Asustek Action are attached as Exhibits 1010 and 1011. The '634 Patent is also currently the subject of litigation brought by Alpha and Omega Semiconductor

Limited and Alpha and Omega Semiconductor Incorporated ("AOS" or "Patent Challenger") against Force Mos in *Alpha and Omega Semiconductor Limited, et al v. Force Mos Technology, Co. Ltd.*, No. 4:22-cv-05448 (N.D. Ca.) (the "AOS Action"). Petitioner is not aware of any other pending judicial or administrative matter that would affect, or be affected by, a decision in this proceeding.

C. Lead and Back-Up Counsel (37 C.F.R. § 42.8(b)(3))

For purposes of this Petition, the following attorneys are lead and back-up counsel for Petitioner:

LEAD COUNSEL	
Mackenzie Martin Registration No. 77,950 **BAKER & McKENZIE LLP** 1900 North Pearl Street, Suite 1500 Dallas, Texas 75201 Tel: (214) 978-3048 mackenzie.martin@bakermckenzie.com	
BACK-UP COUNSEL	
John G. Flaim Registration No. 37,323 **BAKER & McKENZIE LLP** 1900 North Pearl Street, Suite 1500 Dallas, Texas 75201 Tel: (214) 978-3097 john.flaim@bakermckenzie.com Ellen Cheong Registration No. 71,852 **BAKER & McKENZIE LLP** 452 Fifth Avenue New York, NY 10018 Tel: (212) 626-4100	Dorian Ojemen Registration No. 72,956 **BAKER & McKENZIE LLP** 800 Capitol, Suite 2100 Houston, Texas 77002 Tel: (713) 427-5032 dorian.ojemen@bakermckenzie.com DJ Lee *pro hac vice* **BAKER & McKENZIE LLP** 1900 North Pearl Street, Suite 1500 Dallas, Texas 75201 Tel: (214) 978-3017

ellen.cheong@bakermckenzie.com	dongjae.lee@bakermckenzie.com

D. Service Information (37 C.F.R. § 42.8(b)(4))

For purposes of this Petition, Petitioner consents to electronic service by email at: mackenzie.martin@bakermckenzie.com.

E. Payment of Fees (37 C.F.R. § 41.103)

Petitioner authorizes the United States Patent and Trademark Office (USPTO) to charge the fees set forth in 37 C.F.R. § 42.15(a) for this Petition, and any additional fees that might be due, to Deposit Account No. 13-0480 (Attorney Docket No. 10148110-51064583). This Petition meets the fee requirements of 35 U.S.C. § 312(a)(1).

III. REQUIREMENTS FOR IPR UNDER 37 C.F.R. § 42.104

A. Grounds for Standing (§ 42.104(a))

Petitioner certifies that the ’634 Patent is available for IPR and that Petitioner is not barred or estopped from requesting an IPR that challenges the claims of the ’634 Patent on the grounds identified in this Petition.

B. Identification of Challenge and Statement of Precise Relief Requested for Each of the Challenged Claims (§ 42.104(b))

Petitioner respectfully requests that IPR of the Challenged Claims (*i.e.*, Claims 1-9 of the ’634 Patent) be instituted and that each of the Challenged Claims be held unpatentable and cancelled based on the following grounds:

No.	Claims	Ground	Reference(s)
1	1-2, 6	102	Unpatentable under pre-AIA 35 U.S.C. § 102(b) as anticipated by German Patent Publication No. DE102004009083 ("Hirler") (Ex. 1005-1007).
2	3-5, 7-9	103	Unpatentable under pre-AIA 35 U.S.C. § 103(a) as obvious over Hirler (Ex. 1005-1007) in view of U.S. Patent Pub. No. 2004/0021174 ("Kobayashi") (Ex. 1008) and knowledge of the POSITA.
3	1-2	102	Unpatentable under pre-AIA 35 U.S.C. § 102(b) as anticipated by U.S. Patent Publication No. 2005/0029584 ("Shiraishi") (Ex. 1009)
4	3-9	103	Unpatentable under pre-AIA 35 U.S.C. § 103(a) as obvious over Shiraishi (Ex. 1009) in view of Kobayashi (Ex. 1008) and knowledge of the POSITA.
5	1-9	103	Unpatentable under pre-AIA 35 U.S.C. § 103(a) as obvious over Kobayashi (Ex. 1008) in view of Shiraishi (Ex. 1009) and knowledge of the POSITA.

This Petition, supported by the declaration of Dr. David Liu (Ex. 1003), the prior art (Exs. 1005-1009), and other exhibits filed herewith, demonstrate that there is a reasonable likelihood that Petitioner will prevail with respect to one or more, if not all, of the Challenged Claims. *See* 35 U.S.C. § 314(a).

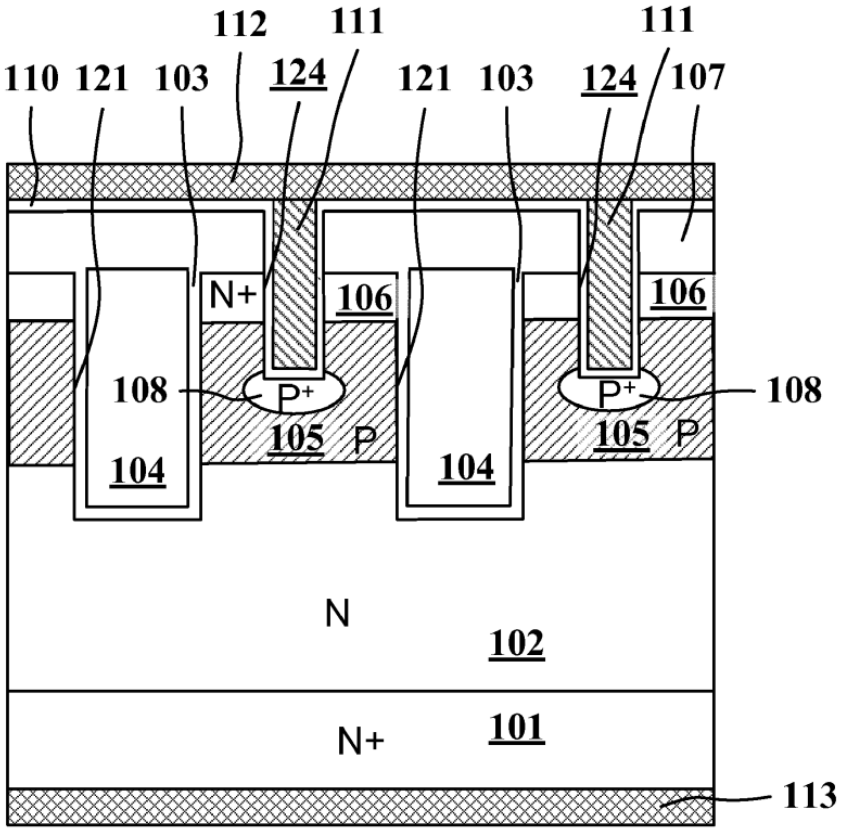
IV. THE '634 PATENT

A. The '634 Patent

The '634 Patent is generally directed to trenched Metal-Oxide-Semiconductor Field Effect Transistor ("MOSFET"). Ex. 1001 at 1:5-9; Ex. 1003 at ¶¶ 26-27. The '634 Patent addresses the issue of poor ohmic contact on the sidewall of the trenched source contact due to poorly engineered doping

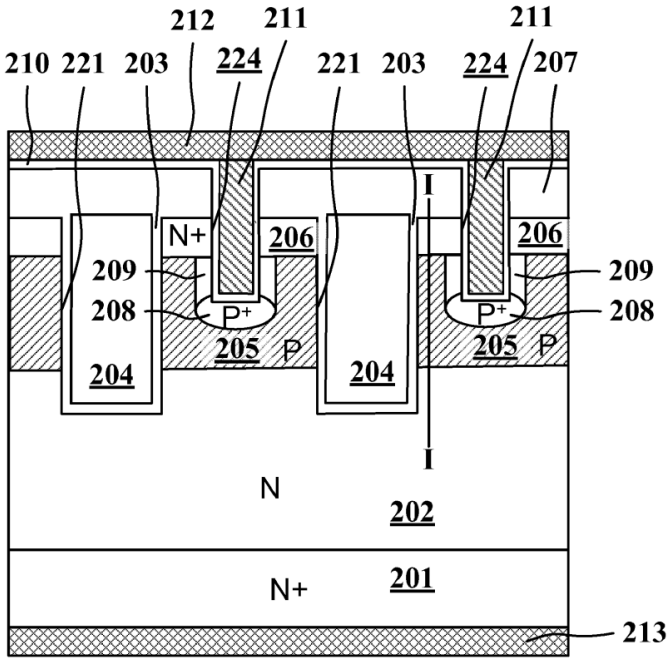
concentration profile. Ex. 1001 at 1:35-45; Ex. 1003 at ¶ 27. In particular, the ’634 Patent is directed to “a lateral contact layer” at the sidewalls of the source contact trench within the base layer, along with a “base contact layer” at the bottom of the source contact trench. Ex. 1001 at 1:5-9, 1:66-67, 2:23-26, 3:50-4:6, Fig. 2G; Ex. 1003 at ¶ 28. The ’634 Patent has one independent claim, Claim 1, and eight (8) dependent claims, Claims 2-9.

The ’634 Patent admits that, at the time of filing, a trenched MOSFET with near-identical structure, including the claimed drain region, body region, source region, front metal layer, interlayer oxide film, bottom metal layer, trenched gates formed on top of the source layer and extending down through the base layer to a portion of the epitaxial layer, and source contact trenches formed on top of the source layer and extending down through the source layer to a portion of the base layer with a heavily doped base layer at the bottom of the trench, already existed in prior art. Ex. 1001 at 1:5-9, 1:18-41, Fig. 1 (Prior Art); Ex. 1003 at ¶ 30. Figure 1, which depicts the prior art as admitted by the ’634 Patent, is shown below.



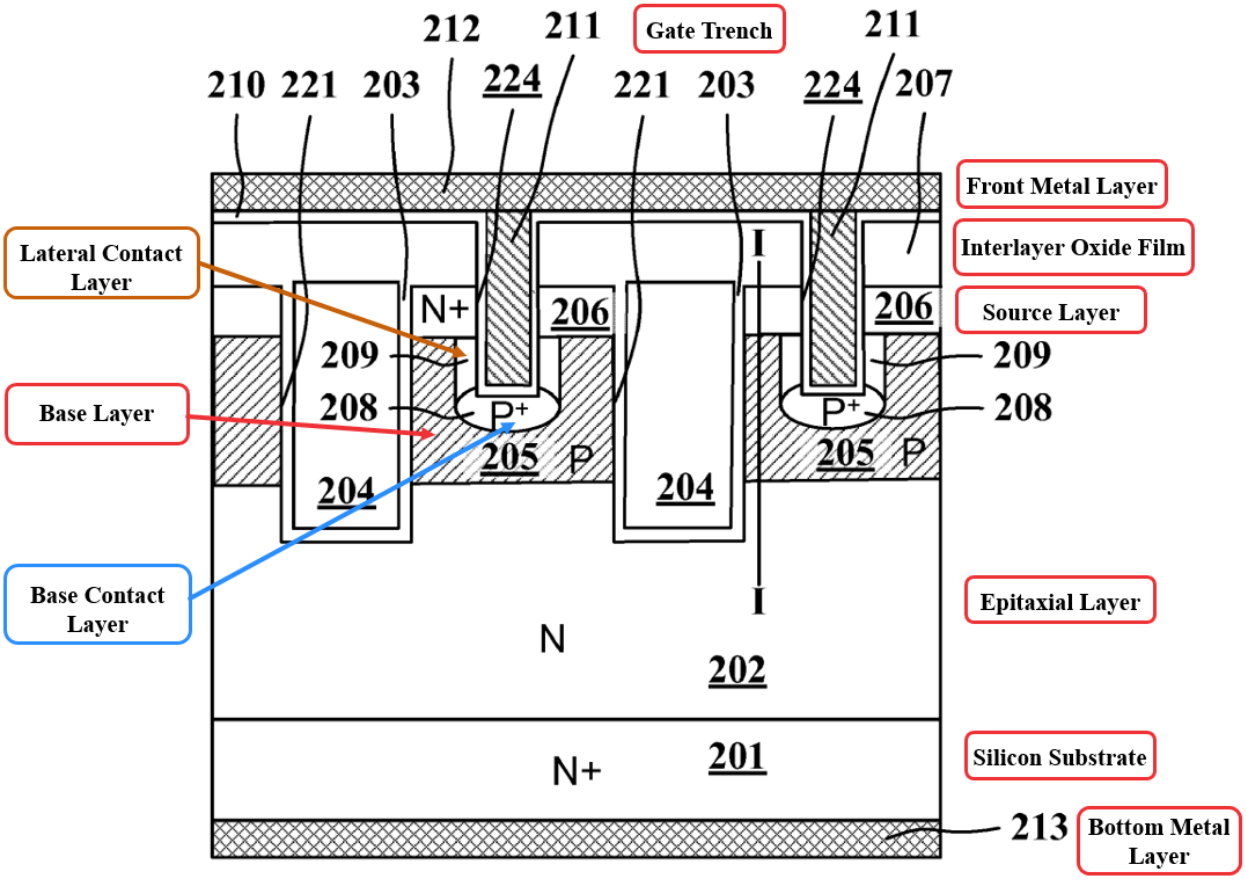
’634 Patent, Figure 1 (Prior Art)

The lateral contact layer at the sidewalls in the base layer of the source contact trenches described in the ’634 Patent is shown below in the ’634 Patent’s Figure 2G as 209. Ex. 1001 at Fig. 2G, 3:50-4:6; Ex. 1003 at ¶¶ 28-29.



’634 Patent, Figure 2G

The ’634 Patent also describes the lateral contact layer (209) at the sidewalls of the source contact trench (224) as being P*-type, the base contact layer (208) at the bottom of the source contact trench as being P+-type and the body of the MOSFET (205) being P-type. Ex. 1001 at 3:50-56, 3:65-4:6, 5:9-15. The lateral contact layer is doped to P*, where P* is more heavily doped than P and less than P+. *Id.*; Ex. 1003 at ¶¶ 28-29.



’634 Patent, Figure 2G (annotations added)

B. The ’634 Patent File History

U.S. Patent Application No. 12/036,243 (the “’243 Application”), titled “TRENCHED MOSFET WITH TRENCHED SOURCE CONTACT,” was filed on February 23, 2008, and issued as the ’634 Patent on December 8, 2009. Ex. 1001 at 1; Ex. 1002 at 48-86. The ’243 Application was filed with 9 original claims and listed Fu-Yuan Hsieh as the inventor. Ex. 1001 at 1; Ex. 1002 at 48, 66-68.

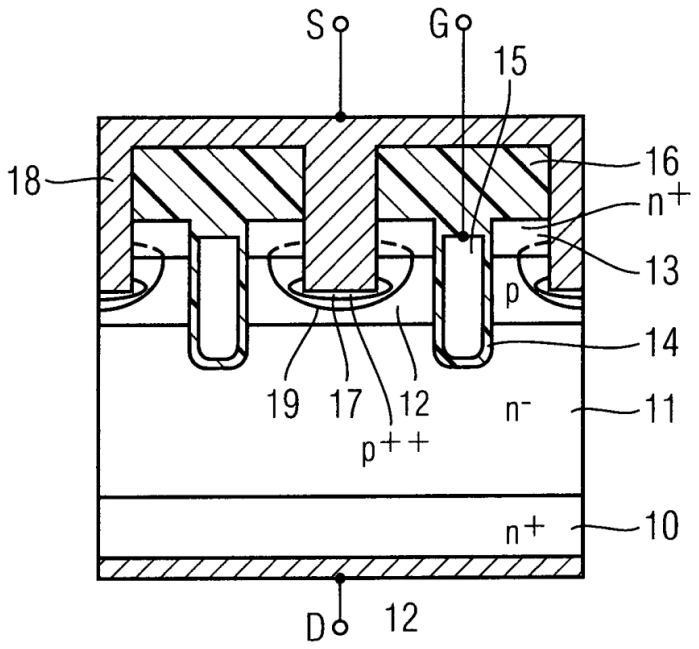
On July 15, 2009, a telephonic examiner-initiated interview took place, where the examiner and the applicant discussed the lateral contact layer “covering

[the] entire trench sidewall[,]" the prior art, and claim language. Ex. 1002 at 27. There was a follow-up email exchange and telephonic conversation on July 20, 2009. *Id.* On July 28, 2009 the examiner issued a Notice of Allowance and Fees Due on Claims 1-9 with examiner amendments to Claim 1, and the following Reason for Allowance: "Claim 1 limits the trenched MOSFET to having a trench in which the base and entire sidewall are covered with the lateral contact layer. Kobayashi (US 6,888,196) covers the base and only a portion of the trench sidewall with the lateral contact layer." *Id.* at 23-26. The '634 Patent issued on December 08, 2009. *Id.* at 20-21.

V. OVERVIEW OF THE PRIOR ART

A. German Patent Publication No. DE 102004009083 ("Hirler")

German Patent Publication No. DE 102004009083 ("Hirler") was filed on February 25, 2004, and published on September 22, 2005. Exs. 1005-1007. Hirler is prior art at least under pre-AIA 35 U.S.C. § 102(b). Hirler was not considered during the prosecution of the '634 Patent. Hirler Figure 2F is included below for reference.



Hirler, Figure 2F

Like the ’634 Patent, Hirler teaches the arrangement of a vertical MOS power transistor with tailored body zone (base layer) that has a contact zone at the bottom of the source contact trenches with a high doping concentration compared with the doping concentration of the body zone (base layer). In particular, Hirler discloses a trenched MOSFET, wherein the source contact trenches have a “body amplification zone” or “body enhancement zone” (19) at the sidewalls of the source contact trenches and a “body contact zone” (17) at the bottom of the source contact trench. Ex. 1005 at Fig. 2F; Ex. 1006 at [0013], [0030], Claim 1; Ex. 1003 at ¶¶ 39-40.

Hirler also discloses that the doping concentration of the body amplification zone (19) is more than the doping concentration of the body zone (12) and less

than the doping concentration of the body contact zone (17). Ex. 1006 at [0009], [0031], Claim 2; Ex. 1003 at ¶ 41.

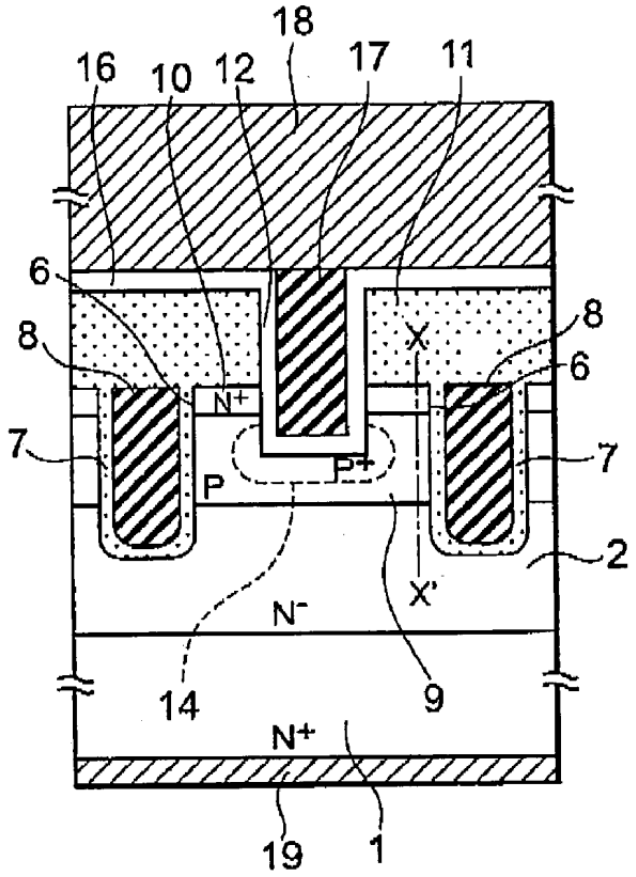
Hirler discloses that the body amplification zone allows "avalanche breakdown [to] be clamped between the transistor structures to achieve high dielectric strength while saving space without precisely defining the depth of the body contact zone." Ex. 1006 at [0007]-[0008]; Ex. 1003 at ¶¶ 42-44.

Hirler also discloses that the conductivity types can be reversed between n-type to p-type to make complementary devices, resulting from an N-channel MOSFET to a P-channel MOSFET. Ex. 1006 at [0001], [0005], [0028]; Ex. 1003 at ¶ 45.

B. U.S. Patent Publication No. 2004/0021174 ("Kobayashi")

Kobayashi was published on February 5, 2004. Ex. 1008 at cover. Kobayashi is prior art at least under pre-AIA 35 U.S.C. § 102(b). Kobayashi was considered during the prosecution of the '634 Patent. Nevertheless, the PTAB should consider Kobayashi, as explained in Section IX below.

A view of Kobayashi's Figure 5A included below for reference.



Kobayashi, Figure 5A

Like the ’634 Patent, Kobayashi teaches the tailoring of the depth of the trenched source contact with respect to the maximum base doping layer concentration profile that is in contact with the base contact layer. This tailoring considers the base doping concentration profile at the sidewall and at the bottom of the source contact structure. In particular, Kobayashi discloses a trenched vertical MOSFET with source contact trenches penetrating to the base layer of the MOSFET with a p+-type base contact layer at the bottom of the trench. Ex. 1008 at Cover, Fig. 10, [0018], [0052]; Ex. 1003 at ¶ 48.

Specifically, in relation to Figure 5A, Kobayashi discloses an embodiment comprising,

> an N^+-type silicon substrate **1** and an N^--type epitaxial layer **2** formed on one surface of the N^+-type silicon substrate **1**. A P-type base layer **9** and an N^+-type source layer **10** are formed on a surface of the N^--type epitaxial layer **2**. . . . In each of trenches **6** reaching the N^--type epitaxial layer **2** through the P-type base layer **9**, a gate oxide film **7** and a polysilicon **8** are filled. On the polysilicon **8** to serve as a gate electrode or a trench gate, an interlayer oxide film **11** is formed. Between the trench gates adjacent to each other, a contact hole **12** having a predetermined depth is formed to reach the P-type base layer **9** though the N^+-type source layer **10**. Directly under the contact hole **12**, a barrier metal **16** is deposited to extend onto the interlayer oxide film **11**. The contact hole **12**, within which the barrier metal **16** is formed, is filled with W **17**. On the surface of the W **17** and the barrier metal **16**, a source electrode **18** is formed. On the other surface, of the N^+-type silicon substrate **1**, a drain electrode **19** is formed.

Ex. 1008 at [0052].

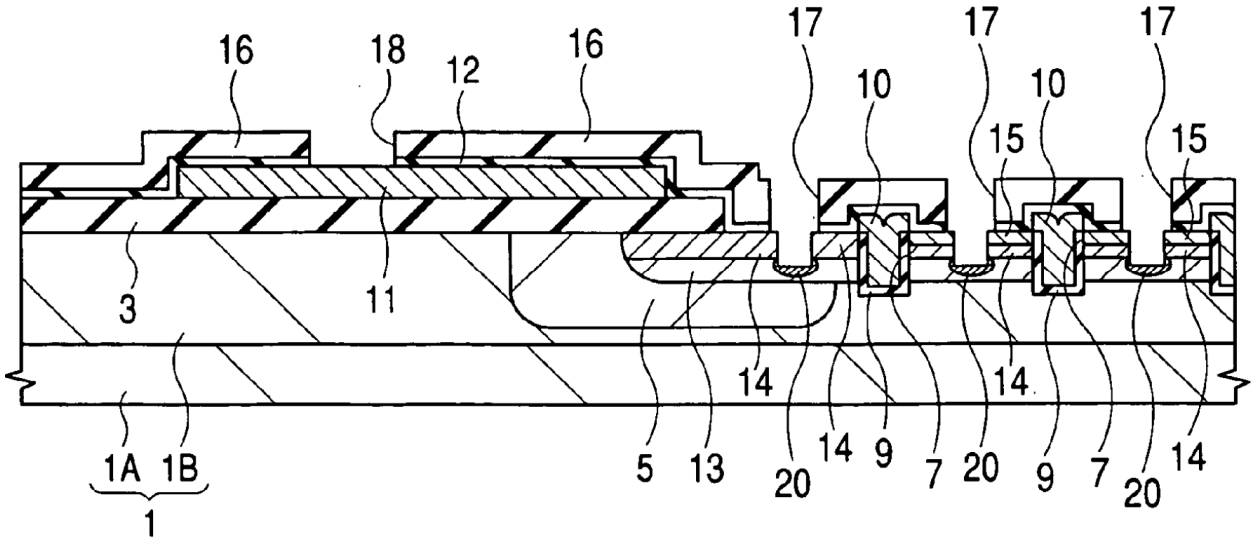
Kobayashi also discloses "a base contact layer **14** under the bottom of the contact hole **12**." Ex. 1008 at Fig. 5A, [0061]; Ex. 1003 at ¶ 50.

More specifically, Kobayashi discloses a barrier metal layer made of titanium (Ti) and titanium nitride (TiN). Ex. 1008 at [0062]. Kobayashi also discloses the use of a plurality of source contact plugs made of Tungsten. Ex. 1008 at [0052]-[0053]; Ex. 1003 at ¶ 51.

C. U.S. Patent Publication No. 2005/0029584 ("Shiraishi")

Shiraishi was published on February 10, 2005. Ex. 1009 at cover. Shiraishi is prior art at least under pre-AIA 35 U.S.C. § 102(b). Shiraishi was not

considered during the prosecution of the ’634 Patent. Shiraishi Figure 8 is included below for reference.



Shiraishi, Figure 8

Like the ’634 Patent, Shiraishi generally discloses the tailoring of the doping profile in the base region of the Vertical Power MOSFET to affect the doping profile at the sidewalls of the source contact trenches. In particular, Shiraishi discloses a power Metal Insulator Semiconductor Field Effect Transistor (“MISFET”) with source contact trenches with a p+-type base contact layer **20** at the bottom of the trench. Ex. 1009 at Abstract, Fig. 8, [0075]; Ex. 1003 at ¶¶ 53-54. Shiraishi also discloses an additional p-type semiconductor layer **14** below the source layer and along the sidewalls of the source contact trench. Ex. 1009 at Fig. 8, [0073], [0084]. This region can be doped such that the impurity concentration is

less than that of the p+ base contact layer **20** but higher than the p-type body layer **13**. Ex. 1009 at [0075].

Shiraishi also discloses that the additional p-type semiconductor layer **14** serves as a "punch-through stopper layer" for the power MISFET. Ex. 1009 at [0073], [0080], [0085]; Ex. 1003 at ¶¶ 146-147. Shiraishi also discloses that the additional p-type semiconductor layer **14** allows for reduction of base resistance of a parasitic npn bipolar transistor and for enhancement of avalanche yield strength. Ex. 1009 at [0084].

VI. LEVEL OF ORDINARY SKILL IN THE ART

Petitioner submits that a person of ordinary skill in the art of the subject matter of the '634 Patent at the alleged effective filing date of the invention of the '634 Patent ("POSITA") would have earned a Master's degree in electrical engineering, and at least two years of relevant work experience in the field of integrated circuit design and manufacturing. Ex. 1003 at ¶¶ 57, 32-37.

VII. CONSTRUCTION OF THE CLAIMS

In *inter partes* review proceedings, a claim of a patent is "construed using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. § 282(b)." 37 C.F.R. § 42.100(b). Claim terms are generally given their "ordinary and customary meaning that the term would have to a person of ordinary skill in the art." *Duncan Parking Techs., Inc. v. IPS Grp.,*

Inc., 914 F.3d 1347, 1364 (Fed. Cir. 2019).[1] Because the meaning of a claim term as understood by a POSITA is often not immediately apparent, and because patentees frequently use terms idiosyncratically, the court looks to "those sources available to the public that show what a person of skill in the art would have understood disputed claim language to mean." *Phillips v. AWH Corp.*, 415 F.3d 1303, 1314 (Fed. Cir. 2005) (en banc). Those sources include the "intrinsic evidence of record, *i.e.*, the patent itself, including the claims, the specification and, if in evidence, the prosecution history." *Vitronics Corp. v. Conceptronic*, 90 F.3d 1576, 1582 (Fed. Cir. 1996).

Specifically, "the specification may reveal an intentional disclaimer, or disavowal, of claim scope by the inventor. In that instance [], the inventor has dictated the correct claim scope, and the inventor's intention, as expressed in the specification, is regarded as dispositive." *Phillips*, 415 F.3d at 1316 (citing *SciMed Life Sys., Inc. v. Advanced Cardiovascular Sys., Inc.*, 242 F.3d 1337, 1343-44 (Fed. Cir. 2001)). If the specification distinguishes prior art, "[c]laims cannot be construed as encompassing the prior art that was distinguished in the specification . . . ." *Kinik Co. v. ITC*, 362 F.3d 1359, 1365 (Fed. Cir. 2004) (citing *SciMed*, 242

[1] A person of ordinary skill in the art is a hypothetical person who is presumed to have known the art "before the effective filing date of the claimed invention." 35 U.S.C. § 103. This person is considered one "of ordinary creativity, not an automaton." *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 421 (2007).

F.3d at 1343-44); *see Akeva LLC v. Nike, Inc.*, 817 Fed. Appx. 1005, 1009-1010 (Fed. Cir. 2020) (finding the patentee had disclaimed the embodiment of the prior art disclosed in the specification "given the patent's disparagement of conventional fixed rear sole shoes" and the patent's following characterization of the invention as removable or rotatable sole shoes).

Additionally, for IPR, claims are construed only to the extent necessary to resolve an underlying controversy. *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co. Ltd.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (internal citations omitted).

A. Claim 1: "the sidewalls of said trenches in said base layer"

Based on the specification and file history of the '634 Patent, this claim term should be construed as "entire sidewalls of the said trenches in said base layer."

The '634 Patent described the prior art as a MOSFET in which "the P^+-type region is located *only* at source contact trench bottom." Ex. 1001 at 1:33-35, Fig. 1 (Prior Art) (emphasis added). In distinguishing the prior art, the patent specification then describes the invention of the '634 Patent as a MOSFET with distinct base contact *and* lateral contact layers, wherein the base contact layer covers the *bottom* of the source contact trench and the lateral contact layer covers the entirety of the remaining *sidewalls* of the trench in the base layer. *E.g.*, Ex. 1001 at 1:43-45, Fig. 2G; Ex. 1003 at ¶ 60 (emphasis added). Specifically, the '634 Patent describes, "[t]he P+-type base layer (208) and the P*-type lateral

contact layer (209) are formed at the bottom and sidewall of the source contact trenches (224) respectively." Ex. 1001 at 5:9-12. Further, the '634 Patent figures depict the lateral contact layer and base contact layer as separate layers and provides two, separate implantation methods for forming the bottom base contact layer and the lateral contact layer. Ex. 1001 at 3:50-4:6, Figs. 3A and 3B. Specifically, the base contact layer is created with a 90° implantation angle respective to the epitaxial layer while the lateral contact layer is created with a 45° to 80° implantation angle. *Id*.

In addition, the examiner distinguished prior art reference Kobayashi on the basis of the "entire" sidewall of the source contact trench in the base layer being covered by the lateral contact layer, as opposed to only being partially covered. Ex. 1002 at 29. This "entire" sidewall distinction was cited during an Examiner initiated interview and as a reason for allowance. *Id.* at 27, 29. *See* screenshot from Ex. 1002 below.

Reasons for Allowance

2. Claims 1-9 are allowed.
3. The following is an examiner's statement of reasons for allowance:

Claim 1 limits the trenched MOSFET to having a trench in which the base and entire sidewall are covered with the lateral contact layer. Kobayashi (US 6,888,196) covers the base and only a portion of the trench sidewall with the lateral contact layer.

Claims 2-9 are allowed as being properly dependent upon allowed claim 1.

Ex. 1002 at 29

Accordingly, Petitioner construes "the sidewalls of said trenches in said base layer" to mean "the entire sidewalls of the said trenches in said base layer." *See Kinik*, 362 F.3d at 1365; *SciMed*, 242 F.3d at 1341.

VIII. CLAIM-BY-CLAIM EXPLANATION OF GROUNDS FOR UNPATENTABILITY

Pre-AIA Section 102 of the United States patent law provides that

> [a] person shall be entitled to a patent unless —
> . . .
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of the application for patent in the United States…

35 U.S.C. § 102(b) (Pre-AIA).

A claim is anticipated if "a prior art reference [] disclose[s] each and every element of the claim, either explicitly or inherently." *ADASA Inc. v. Avery Dennison Corp.*, 55 F.4th 900, 910 (Fed. Cir. 2022) (citing *Eli Lilly & Co. v. Zenith Goldline Pharms., Inc.*, 471 F.3d 1369, 1375 (Fed. Cir. 2006)). While the disclosed claim elements must be "arranged or combined in the same way as the claim," the reference need not used the same terms to describe these claims. *In re Gleave*, 560 F.3d 1331, 1334 (Fed. Cir. 2009) (internal citations omitted).

Pre-AIA Section 103 provides that "if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a

whole would have been obvious at the time the invention was made to a person having ordinary skill in the art." 35 U.S.C. § 103(a) (Pre-AIA).

The Supreme Court's decision in *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398 (2007) sets forth the standard for determining obviousness under 35 U.S.C. § 103, which is based on an analysis of several factual inquiries as set forth in *Graham v. John Deere Co. of Kansas City*, 383 U.S. 1, 17-18 (1966): (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) when available, evidence such as commercial success, long-felt but unsolved needs, and failure of others. *KSR Int'l*, 550 U.S. at 407, 419.

The Court emphasized that an "expansive and flexible approach" should be used when determining obviousness. *KSR Int'l*, 550 U.S. at 415. The Court identified several rationales and principles, including the following: (1) if a work is available in one field of endeavor, and design incentives and other market forces can prompt variations of it (either in the same field or a different one), and a person of ordinary skill can implement a predictable variation, the variation is obvious; (2) if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its application is beyond his or her skill; (3) the combination of familiar elements according to known methods is likely to be

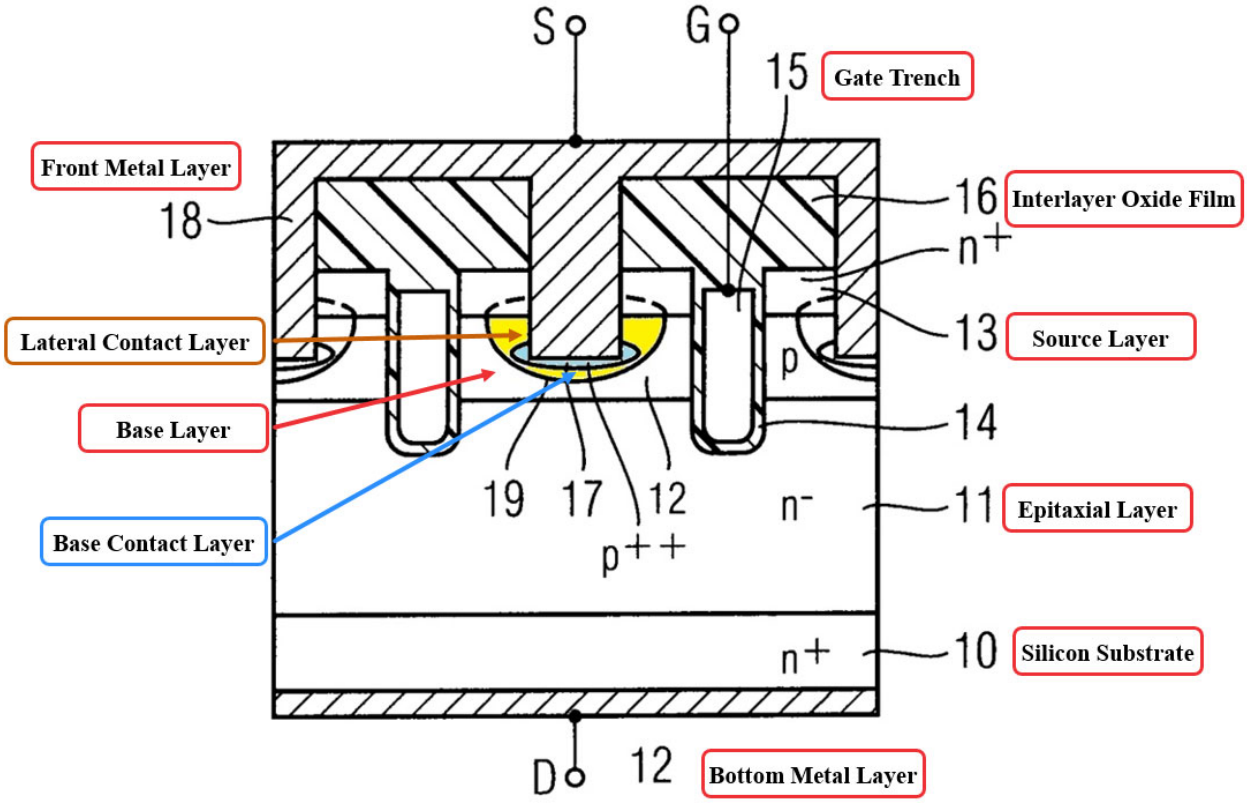
obvious when it does no more than yield predictable results; (4) if the improvement is nothing more than the predictable use of prior art elements according to their established functions, it is likely obvious, among others. *Id*. at 416-17. "Often, it will be necessary for a court to look to interrelated teachings of multiple patents; the effects of demands known to the design community or present in the marketplace; and the background knowledge possessed by a person having ordinary skill in the art, all in order to determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue." *Id.* at 418.

A. Ground 1: Claims 1-2 and 6, are unpatentable under pre-AIA 35 U.S.C. § 102(b) as anticipated by Hirler.

Claims 1-2, and 6 of the '634 Patent are unpatentable under pre-AIA 35 U.S.C. § 102(b) as anticipated by Hirler. The following discussion is fully supported by the Declaration of Dr. David Liu. Ex. 1003 at ¶¶ 63-80.

1. Claim 1

As provided in further detail below, Hirler discloses and anticipates every limitation of Claim 1. Specifically, every element of Claim 1 is disclosed in Figure 2F, annotated below. Ex. 1005 at Fig. 2F; Ex. 1003 at ¶ 63.



Hirler, Figure 2F (annotated)

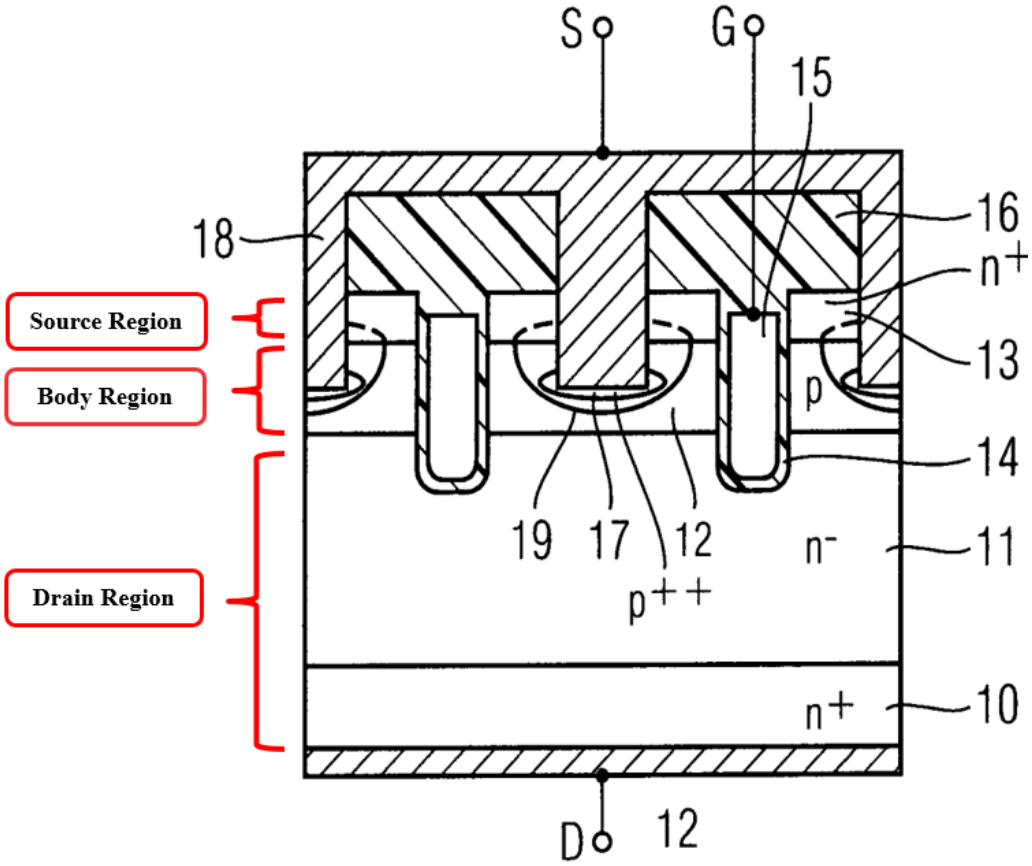
a. 1 [preamble]: "A trenched MOSFET with trenched source contact, comprising:"

To the extent the preamble is limiting, it is disclosed in Hirler, which discloses a trenched MOSFET with source contact trenches—*e.g.*, "The present invention relates to a MOS power transistor arrangement having a vertical transistor structure . . . wherein the body zone has a contact zone at the base of a contact trench . . . ." Ex. 1005 at Fig. 2F; Ex. 1006 at [0001], Cover Summary; Ex. 1003 at ¶ 64.

b. 1[a]: "a semiconductor region having a drain region, a body region and a source region, comprising, a silicon substrate, an epitaxial layer corresponding to said drain region disposed on the top of said silicon substrate, a base layer corresponding to said body region disposed on the top of said epitaxial layer, and a source layer corresponding to said source region disposed on the top of said base layer;"

Element 1[a] is disclosed in Hirler, which describes a vertical trenched MOSFET with a drain region, body region, and source region, arranged in the claimed structure. Ex. 1005 at Fig. 2F; Ex. 1006 at [0001]; Ex. 1003 at ¶ 65. Specifically, Hirler discloses "[t]he starting point is an n+ substrate **10** of silicon, an n- drift zone **11**, p-body zone areas **12** as well as n+ source zone areas **13**." Ex. 1006 at [0018], [0001].

As shown in Hirler's Figure 2F (copied below with color annotations), the disclosed MOSFET has a drain region, a body region, and a source region. Ex. 1005 at Fig. 2F, Fig. 1A; Ex. 1006 at [0018]. Moreover, the drain region is oriented at the bottom of the figure with a silicon substrate (10), an epitaxial layer (11), a body layer (12), and a source layer (13). Ex. 1005 at Fig. 2F, Fig. 1A; Ex. 1006 at [0018]; Ex. 1003 at ¶ 66.



Hirler, Figure 2F (annotated in regards to Claim element 1a)

c. 1[b]: "a front metal layer formed on the upper surface of said semiconductor region"

Element 1[b] is disclosed in Hirler, wherein a metal layer (18) is positioned on the upper surface of the MOSFET to form a source connection, S. Ex. 1005 at Fig. 2F; Ex. 1006 at [0022]; Ex. 1003 at ¶ 67.

d. 1[c]: "an interlayer oxide film formed between said source layer and said front metal layer;"

Element 1[c] is disclosed in Hirler, wherein a silicon oxide layer (16) is formed between the source layer (13) and the metal layer (18). Ex. 1005 at Fig. 2F, Fig. 1A; Ex. 1006 at [0018]; Ex. 1003 at ¶ 68.

e. 1[d]: "a bottom metal layer formed on the lower surface of said semiconductor region;"

Element 1[d] is disclosed in Hirler, wherein a metal layer (12) is positioned on the bottom surface of the MOSFET to form a drain connection, D. Ex. 1005 at Fig. 2F; Ex. 1006 at [0022]; Ex. 1003 at ¶¶ 69-70.

f. 1[e]: "a plurality of trenched gates covered by said interlayer oxide film are formed on top of said source layer extending downwardly through said base layer to a portion of said epitaxial layer; and"

Element 1[e] is disclosed in Hirler. Hirler discloses a plurality of gate trenches (15), annotated as "G", which are covered by the silicon oxide layer, begin above the source layer, and extend down through the body layer and into the epitaxial, drift layer. Ex. 1005 at 2F; Ex. 1006 at [0018]; Ex. 1003 at ¶ 71.

g. 1[f]: "a plurality of source contact trenches formed on the top of said interlayer oxide film extending downwardly through said source layer to a portion of said base layer"

Element 1[f] is disclosed in Hirler. Specifically, Hirler discloses source contact trenches formed on top of the silicon oxide layer that "penetrat[e] through the source zones areas **13** to the body zone areas **12** . . . ." Ex. 1006 at [0020], [0019]; Ex. 1005 at Fig. 2F; Ex. 1003 at ¶ 72.

h. 1[g]: "wherein the sidewalls of said trenches in said base layer are covered by the lateral contact layer;"

Element 1[g] is disclosed by Hirler. Specifically, Hirler discloses "body amplification zones" (19) implanted and formed along the sidewalls of the contact trench that is in the base layer. Ex. 1005 at Fig. 2F; Ex. 1006 at [0030], [0033]; Ex. 1003 at ¶ 73.

i. 1[h]: "wherein the bottom base of said trenches in said base layer are covered by the base contact layer."

Element 1[h] is disclosed in Hirler, in which the bottom of the contact trench is covered by a "body contact zone." Ex. 1005 at Fig. 2F, Fig. 1D; Ex. 1006 at [0021]; Ex. 1003 at ¶ 74.

2. Claim 2

a. 2[a] "The trenched MOSFET of claim 1, wherein the silicon substrate, the epitaxial layer, and the source layer are N-type;"

Element 2[a] is disclosed in Hirler. Claim 2 depends from Claim 1, which is disclosed by Hirler as described above in Section VIII(A)(1). As shown in Figure 2F above, Hirler discloses a trenched MOSFET wherein the silicon substrate, the epitaxial layer, and the source layer are N-type. Ex. 1005 at Fig. 2F; Ex. 1006 at [0018]; Ex. 1003 at ¶ 75.

b. 2[b] "the base layer and lateral contact layer are P-type;"

Element 2[b] is disclosed in Hirler. As shown in Figure 2F above, Hirler discloses a trenched MOSFET wherein the body layer is P-type. Ex. 1005 at Fig. 2F; Ex. 1006 at [0018]; Ex. 1003 at ¶ 76. In addition, Hirler discloses that the body amplification layer is also p-type—*i.e.*, p+. Ex. 1006 at [0030]; Ex. 1003 at ¶ 76.

c. 2[c] "and each of the source contact trenches further has a P-type base contact layer at a bottom thereof, and the lateral contact layer has less doping concentration than the base contact layer at bottom."

Element 2[c] is disclosed in Hirler. As shown in Figure 2F above, Hirler discloses a trenched MOSFET wherein the body contact layer is P-type—*i.e.*, p++. Ex. 1005 at Fig. 2F; Ex. 1006 at [0018]; Ex. 1003 at ¶ 77. In addition, Hirler

discloses that the doping concentration of the body amplification zone is larger than the doping concentration of the body zone and smaller than the doping concentration of the body contact zone. Ex. 1006 at [0009], [0031], Claim 2; Ex. 1003 at ¶ 77.

3. Claim 6

a. "The trenched MOSFET of claim 1, wherein the silicon substrate, the epitaxial layer, and the source layer are P-type; the base layer and lateral contact layer are N-type; and each of the source contact trenches further has a N-type base contact layer at a bottom thereof, and the lateral contact layer has less doping concentration than the base contact layer at bottom."

Claim 6 is disclosed in Hirler. Claim 6 depends from Claim 1, which is disclosed by Hirler as described above in Section VIII(A)(1). Hirler introduces a MOSFET with layers of either N- or P-type:

> The present invention relates to a MOS power transistor arrangement having a vertical transistor structure in which a drift zone of the first conductivity type and a body zone of a second conductivity type opposite to the first conductivity type and a source zone of the first conductivity type are successively provided on a semiconductor substrate of a first conductivity type, and in which a trench gate extends through the source zone and the body zone into the drift zone, wherein the body zone has a contact zone at the base of a contact trench with a high doping concentration compared with the doping concentration of the body zone.

Ex. 1006 at [0001]; Ex. 1003 at ¶ 78-80.

Further, Hirler specifies an embodiment in prior art where "a trench MOS power transistor in which a p-type layer, an n+ type body amplification zone, an n-type body region and an n++ type body contact zone are provided on the edge of a gate trench, one above the other from the base of the trench." Ex. 1006 at [0005].

B. Ground 2: Claims 3-5 and 7-9 are unpatentable under pre-AIA 35 U.S.C. § 103 as obvious over Hirler in light of Kobayashi and the knowledge of the POSITA.

Claims 3-5 and 7-9 of the '634 Patent are unpatentable under pre-AIA 35 U.S.C. § 103 as obvious over Hirler in light of Kobayashi and the knowledge of the POSITA. The following discussion is fully supported by the Declaration of Dr. David Liu. Ex. 1003 at ¶¶ 81-94.

1. Claim 3

a. 3: "The trenched MOSFET of Claim 2, wherein further comprises a barrier metal layer and a plurality of contact metal plugs."

The elements of Claim 3 are disclosed in Hirler and Kobayashi and knowledge of the POSITA. Claim 3 depends from Claim 2, and Hirler discloses the MOSFET of Claim 2, as provided in Section VIII(A)(2) above. Hirler also discloses that the source contact trench can be "filled with a conductive stopper" - *i.e.* contact metal plugs. Ex. 1006 at [0023]; Ex. 1003 at ¶¶ 81-82. Kobayashi also discloses the use of a barrier metal layer. Ex. 1008 at Fig. 5A, [0052]-[0053], [0062]; Ex. 1003 at ¶¶ 81-82.

2. Claim 4

a. 4: "The trenched MOSFET of Claim 3, wherein the barrier metal layer is Ti/TiN and the contact metal plug is Tungsten."

The elements of Claim 4 are disclosed in Hirler and Kobayashi and knowledge of the POSITA. Claim 4 depends from Claim 3, and Hirler, Kobayashi, and knowledge of the POSITA disclose the MOSFET of Claim 3, as provided in Section VIII(B)(1) above. Hirler discloses that the source contact trench can be "filled with a conductive stopper made of, for example, polycrystalline silicon or tungsten." Ex. 1006 at [0023]; Ex. 1003 at ¶ 83. Kobayashi also discloses the use of a barrier metal layer that is made of Ti and TiN. Ex. 1008 at [0062]; Ex. 1003 at ¶ 83.

3. Claim 5

a. 5: "The trenched MOSFET of Claim 4, wherein the source contact trench is selected from one of a vertical shape and a taper shape."

The elements of Claim 5 are disclosed in Hirler. Claim 5 depends from Claim 4, and Hirler, Kobayashi, and knowledge of the POSITA disclose the MOSFET of Claim 4, as provided in Section VIII(B)(2) above. In addition, Hirler, discloses a trenched MOSFET with a vertical source contact trench. Ex. 1005 at Fig. 2F; Ex. 1003 at ¶ 84.

4. Claim 7

a. 7: "The trenched MOSFET of claim 6, wherein further comprises a barrier metal layer and contact metal plugs."

The elements of Claim 7 are disclosed in Hirler and Kobayashi and the knowledge of the POSITA. Claim 7 depends on Claim 6, which is disclosed in Hirler as described above. *See supra* Section VIII(A)(3). The remaining elements are disclosed by Hirler, Kobayashi, and the knowledge of a POSITA, as described above in relation to Claim 3. *See supra* Section VIII(B)(1). The POSITA would understand that inverting the conductivity types simply allow the formation of either an N-channel MOSFET or a P-channel MOSFET. Ex. 1003 at ¶ 85.

5. Claim 8

a. 8: "The trenched MOSFET of claim 7, wherein the barrier metal layer is Ti/TiN and the contact metal plug is Tungsten."

Claim 8 depends on Claim 7, which elements are disclosed in Hirler, Kobayashi, and the knowledge of a POSITA. *See supra* VIII(B)(4). The elements of Claim 8 are disclosed in Hirler and Kobayashi and the knowledge of the POSITA, as described above in relation to Claim 4. *See supra* Section VIII(B)(2). The POSITA would understand that the inversion of conductivity types would not affect the previous disclosure and analysis. Ex. 1003 at ¶ 86.

6. Claim 9

a. 9: "The trenched MOSFET of claim 8, wherein the source contact trench is selected from one of a vertical shape and a tapered shape."

Claim 9 depends on Claim 8, which is disclosed by Hirler, Kobayashi, and the knowledge of a POSITA for the reasons explained above. *See supra* Section VIII(B)(5). The remaining elements of Claim 9 are disclosed in Hirler, as described above in relation to Claim 5. *See supra* Section VIII(B)(3). The POSITA would understand that the inversion of conductivity types would not affect the previous disclosure and analysis. Ex. 1003 at ¶ 87.

7. Combining Hirler and Kobayashi in light of knowledge of the POSITA

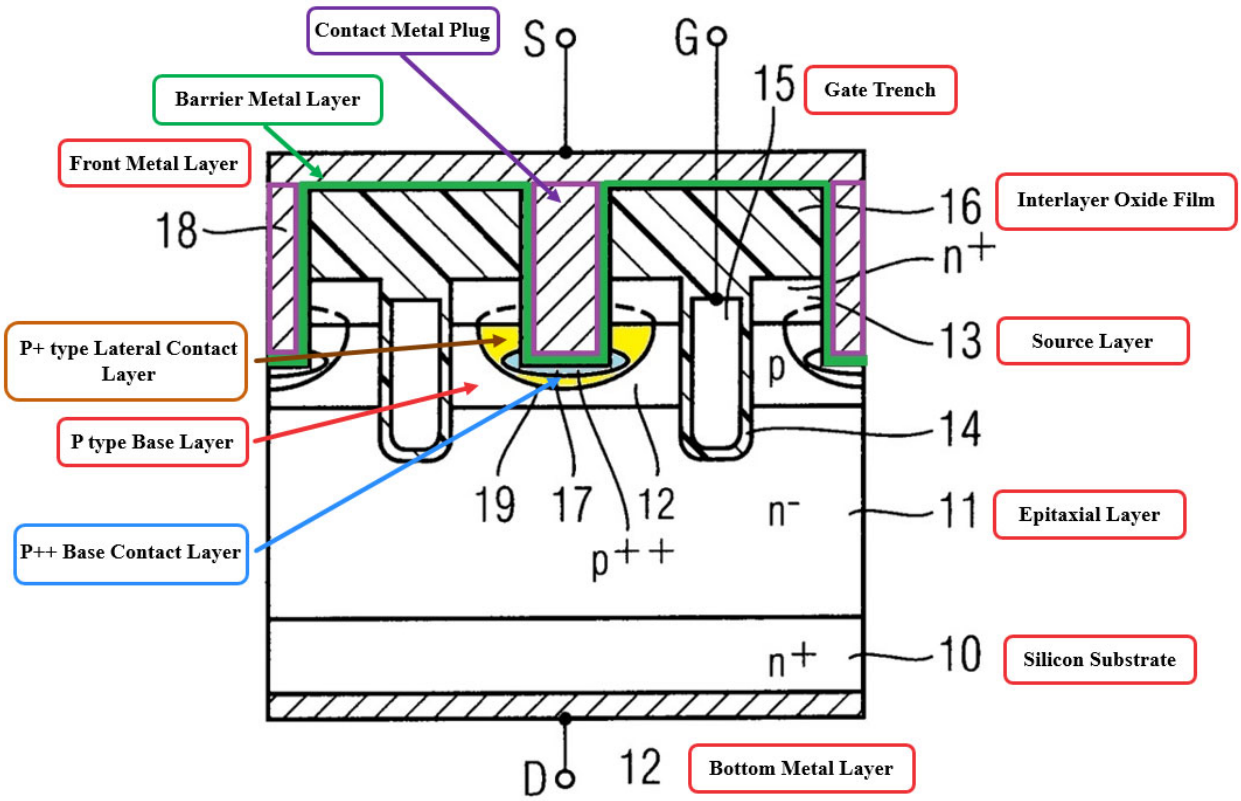
As discussed above, the combination of Hirler and Kobayashi discloses all elements of dependent Claims 3-5 and 7-9. In addition, the POSITA would have been motivated to combine the barrier metal layer of Kobayashi with the MOSFET of Hirler to arrive at the subject matter of Claims 3-5 and Claims 7-9. Ex. 1003 at ¶¶ 88-94.

First, Hirler, Kobayashi, and the '634 Patent are analogous art seeking to solve similar problems. Hirler, Kobayashi, and the '634 Patent are in the same field of endeavor, Vertical Power MOSFET structures, and the methods to improve the performance tradeoff in ON-state (ON-Resistance and speed), and OFF-state (breakdown voltage). Moreover, Hirler, Kobayashi, and the '634 Patent disclose a

similar doping concentration engineering technique, *i.e.*, dopant ion implantation, that allows for the formation of a low resistance source contact, at the bottom of the base region and/or also on the sidewall of the trenched contact region, with minimal impact to the threshold voltage or the ON-Resistance of the Power MOSFET.

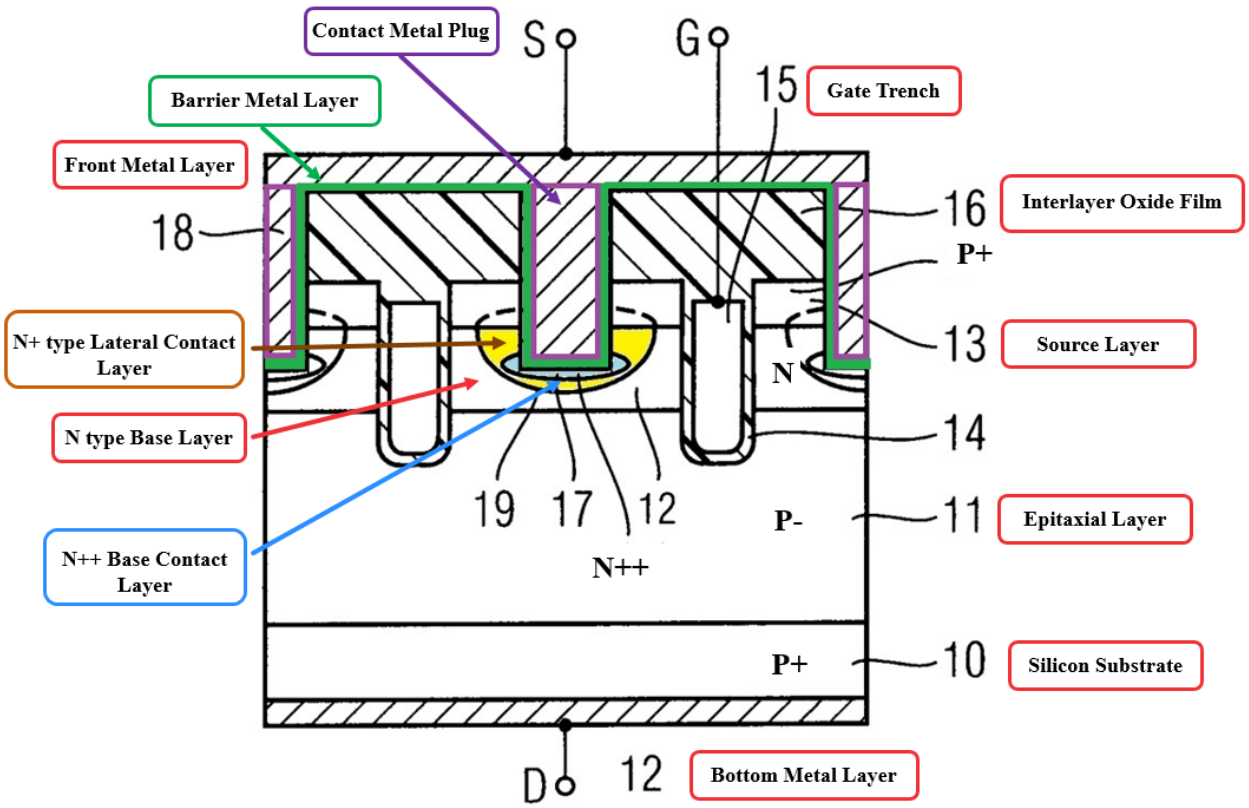
Second, the POSITA would have been motivated to combine the barrier metal layer disclosed in Kobayashi to the MOSFET disclosed in Hirler. In general, a POSITA would know that the use of a barrier metal layer, made of materials such as Ti and TiN, would help to promote the adhesion of the tungsten contact plug expressly taught in Hirler to the contact area. Ti and TiN also serve as a barrier layer to prevent unwanted elements, such as fluorine from the deposition process of W, seeping into the underlying silicon surface, which would degrade the performance of the transistor. Thus, the POSITA would be motivated to apply a known solution (the barrier layer) to a known problem (unwanted seeping of fluorine into the silicon surface) to yield predictable results. Ex. 1003 at ¶¶ 90-93.

Accordingly, the combination of Hirler and Kobayashi renders obvious Claims 3-5, 7-9, as illustrated below in a hypothetical diagram based on Hirler's Figure 2F with the addition of the tungsten contact metal plug in Hirler and the Ti/TiN barrier metal layer according to disclosure in Kobayashi. Ex. 1003 at ¶ 93.



Hirler, Figure 2F (annotated)

Below is the same hypothetical diagram but with inverted conductivity types, showing a p-channel MOSFET. Ex. 1003 at ¶ 94.



Hirler, Figure 2F (annotated)

This case is similar to *Nanya Tech. Corp., et al. v. Lone Star Silicon Innovations LLC*, where the PTAB invalidated claims directed to a MOS semiconductor with a trenched gate. IPR2018-00063, Paper 25, Final Written Decision at 6-7, 22-35 (PTAB May 15, 2019) (*dismissed as moot Lone Star Silicon Innovations, LLC v. Nanya Tech. Corp.*, 810 Fed. Appx. 878, 879 (Fed. Cir. 2020)). There, Petitioner presented both anticipation and obviousness grounds based on each of three primary references. *Nanya* at 7-8. Citing to figures in the prior art, the Board held that the Petitioner had "persuasively map[ped]" the elements of each challenged claim, such that the claims were anticipated and/or

obvious to the POSITA. *See*, *e.g.*, *id.* at 24-25. Further, the Board found the challenged claims obvious, because "any missing details in [the prior art] . . . would have been 'conventional' and, thus, fully within the grasp of an ordinarily skilled artisan." *Id.* at 34 (internal citations omitted) (finding so because the patent at issue admitted that the disputed implantation method was "conventional"); *see* Ex. 1001 at Fig. 1, 1:28 (admitting certain elements of the Challenged Claims, including "a barrier metal layer (**110**)," are in prior art).

The combination of Hirler and Kobayashi is also similar to *Micron Tech., Inc. v. Lone Star Silicon Innovations LLC*, where the Board agreed with Petitioner's expert that the proposed combination "is merely the use of known technique that improves similar devices . . . in the same way . . . to yield predictable results." IPR2017-01562, Paper 30, Final Written Decision at 35 (PTAB Dec. 13, 2018) (*aff'd Lone Star Silicon Innovations LLC v. Iancu*, 813 F. App'x 512 (Fed. Cir. 2020)) (internal quotations and citations omitted).

Based on reasons explained above, a POSITA would have found it obvious to combine the MOSFET of Hirler and the barrier metal layer of Kobayashi. *See KSR Int'l*, 550 U.S. at 415-18; *see also Micron* at 35; and *Nanya* at 24-25, 34.

C. Ground 3: Claims 1 and 2 are unpatentable under pre-AIA 35 U.S.C. § 102(b) as anticipated by Shiraishi.

Claims 1 and 2 of the ’634 Patent are unpatentable under pre-AIA 35 U.S.C. § 102(b) as anticipated by Shiraishi. The following discussion is fully supported by the Declaration of Dr. David Liu. Ex. 1003 at ¶¶ 95-111.

1. Claim 1

a. 1 [preamble]: “A trenched MOSFET with trenched source contact, comprising:”

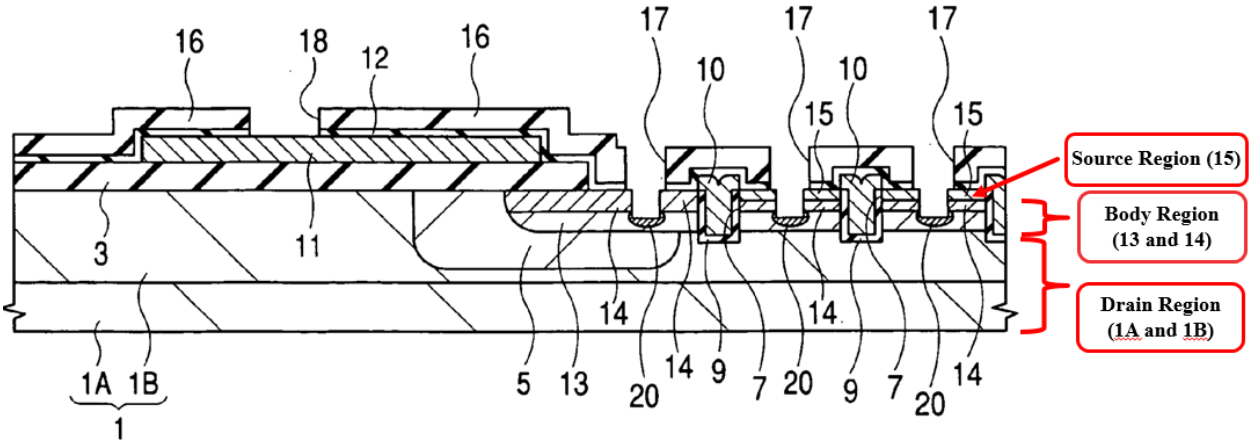
To the extent the preamble is limiting, it is disclosed in Shiraishi, which discloses a trenched MISFET with source contact trenches. Ex. 1009 at [0005], [0074], Fig. 8; Ex. 1003 at ¶ 96.

b. 1[a]: “a semiconductor region having a drain region, a body region and a source region, comprising, a silicon substrate, an epitaxial layer corresponding to said drain region disposed on the top of said silicon substrate, a base layer corresponding to said body region disposed on the top of said epitaxial layer, and a source layer corresponding to said source region disposed on the top of said base layer;”

Element 1[a] is disclosed in Shiraishi, which describes a vertical trenched MISFET with a drain region, body region, and source region, arranged in the claimed structure. Ex. 1009 at Fig. 8; Fig. 35, Ex. 1003 at ¶ 97.

As shown in Shiraishi’s Figure 8 (copied below with color annotations), the disclosed MISFET has a drain region, a body region, and a source region. Ex.

1009 at Fig. 8; Fig. 35, [0012], [0067], [0072], [00073]. Moreover, the drain region is oriented at the bottom of the figure with a silicon substrate (1A), an epitaxial layer (1B), a body layer (13), and a source layer (15). *Id.* at Fig. 8, Fig. 35, [0067], Claim 22; Ex. 1003 at ¶ 98.



Shiraishi, Figure 8 (annotated in regards to Claim element 1a)

Specifically, Shiraishi discloses that "[t]he n^+type single crystal silicon substrate **1A** and the n^-type single crystal silicon layer **1B** may serve as a drain region for the respective power MISFETs." Ex. 1009 at [0067]; Ex. 1003 at ¶ 99. Shiraishi also discloses that "the p^-type semiconductor region **13** may serve as a channel layer for the respective power MISFETs." Ex. 1009 at [0072]; Ex. 1003 at ¶ 100. Finally, Shiraishi discloses "the source region in the n^+type semiconductor region **15**." Ex. 1009 at [0073]; Ex. 1003 at ¶ 101.

c. 1[b]: "a front metal layer formed on the upper surface of said semiconductor region"

Element 1[b] is disclosed in Shiraishi, wherein a source pad (22) is located on top of the source region. Ex. 1009 at Fig. 9, [0077]; Ex. 1003 at ¶ 102.

d. 1[c]: "an interlayer oxide film formed between said source layer and said front metal layer;"

Element 1[c] is disclosed in Shiraishi, wherein an insulating film (16 and 12) is formed between the source region (15) and the source electrode (22). Ex. 1009 at Fig. 9, [0074]-[0075]; Ex. 1003 at ¶ 103.

e. 1[d]: "a bottom metal layer formed on the lower surface of said semiconductor region;"

Element 1[d] is disclosed in Shiraishi, wherein an electrically conductive film may be deposited over the back surface of the silicon substrate (1A), acting as an extraction or drain electrode. Ex. 1009 at [0097]; Ex. 1003 at ¶ 104.

f. 1[e]: "a plurality of trenched gates covered by said interlayer oxide film are formed on top of said source layer extending downwardly through said base layer to a portion of said epitaxial layer; and"

Element 1[e] is disclosed in Shiraishi. As shown in Figure 8, Shiraishi discloses a plurality of gate electrodes (10) that are covered by the insulating film (16 and 12) and extends downward through source layer (15), the channel layer

(13), and into the epitaxial layer (1B). Ex. 1009 at Fig. 8, [0070], [0074]; Ex. 1003 at ¶ 105.

g. 1[f]: "a plurality of source contact trenches formed on the top of said interlayer oxide film extending downwardly through said source layer to a portion of said base layer"

Element 1[f] is disclosed in Shiraishi. Specifically, as shown in Figure 8, Shiraishi discloses source contact trenches (17) formed on top of the insulating film (16 and 12) and extends down through the source layer (15) to the P-type body region (13 and 14). Ex. 1009 at Fig. 8, [0074]; Ex. 1003 at ¶ 106.

h. 1[g]: "wherein the sidewalls of said trenches in said base layer are covered by the lateral contact layer;"

Element 1[g] is disclosed by Shiraishi. Specifically, as shown in Figure 8, Shiraishi discloses an additional semiconductor layer (14) along the sidewalls of the contact trench. Ex. 1009 at Fig. 8, [0073], [0080], [0084]-[0085]; Ex. 1003 at ¶ 107.

i. 1[h]: "wherein the bottom base of said trenches in said base layer are covered by the base contact layer."

Element 1[h] is disclosed in Shiraishi, in which the bottom of the contact trench is covered by a semiconductor region (20). Ex. 1009 at Fig. 8, [0075]; Ex. 1003 at ¶ 108.

2. Claim 2

a. 2[a] "The trenched MOSFET of claim 1, wherein the silicon substrate, the epitaxial layer, and the source layer are N-type;"

Claim 2 depends on Claim 1, which is disclosed in Shiraishi as explained above. *See supra* Section VIII(C)(1). Element 2[a] is also disclosed in Shiraishi. Shiraishi discloses a trenched MISFET wherein the silicon substrate, the epitaxial layer, and the source layer are N-type. Ex. 1009 at [0067], [0073]; Ex. 1003 at ¶ 109.

b. 2[b] "the base layer and lateral contact layer are P-type;"

Element 2[b] is disclosed in Shiraishi. In reference to regions shown in Figure 8, Shiraishi discloses a "p-type semiconductor region **14** inside the p^-type semiconductor region **13**." Ex. 1009 at Fig. 8, [0073]; Ex. 1003 at ¶ 110.

c. 2[c] "and each of the source contact trenches further has a P-type base contact layer at a bottom thereof, and the lateral contact layer has less doping concentration than the base contact layer at bottom."

Element 2[c] is disclosed in Shiraishi. Shiraishi discloses that "p-type semiconductor region **14** may be locally higher in impurity concentration than the p type semiconductor region **13**." Ex. 1009 at Fig. 8, [0080]; Ex. 1003 at ¶ 111. In addition, Shiraishi discloses that "[i]mpurity concentration in the p^+type

semiconductor region **20** may be rendered higher than that in the p-type semiconductor region **14**." Ex. 1009 at Fig. 8, [0075]; Ex. 1003 at ¶ 111.

D. Ground 4: Claims 3-9 are unpatentable under pre-AIA 35 U.S.C. § 103 as obvious over Shiraishi in light of Kobayashi and the knowledge of the POSITA.

Claims 3-9 of the '634 Patent are unpatentable under 35 pre-AIA U.S.C. § 103 as obvious over Shiraishi in light of Kobayashi and the knowledge of the POSITA. The following discussion is fully supported by the Declaration of Dr. David Liu. Ex. 1003 at ¶¶ 112-134.

1. Claim 3

a. 3: "The trenched MOSFET of Claim 2, wherein further comprises a barrier metal layer and a plurality of contact metal plugs."

The elements of Claim 3 are disclosed in Shiraishi and Kobayashi and the knowledge of the POSITA. Claim 3 depends on Claim 2, which is disclosed in Shiraishi (as explained above). *See supra* Section VIII(C)(2). In addition, Shiraishi discloses a "TiW (titanium tungsten) film serving as a barrier conductor film . . . ." Ex. 1009 at [0076]. Kobayashi discloses the use of a plurality of contact metal plugs. Ex. 1008 at [0052], [0066], Fig. 5A.

Kobayashi also teaches that the contact metal plug is beneficial and "allows the resistance component of the source electrode **18** [to be] reduced" because the plug creates a flat surface for the source electrode. Ex. 1008 at [0066]. Further,

Kobayashi discloses that the source electrode "having a flat surface assures a wide contact area in wire bonding or clip bonding carried out for the surface so that a total on-resistance after mounting can be reduced." *Id.* Finally, "it is possible to perform chip mounting by bump connection, which is difficult when the source electrode has an irregular surface." *Id.* The POSITA would thus be motivated to combine the source contact plugs with the disclosure of Shiraishi. Ex. 1003 at ¶¶ 112-116; *see also* Section VIII(D)(8) *infra*.

2. Claim 4

a. 4: "The trenched MOSFET of Claim 3, wherein the barrier metal layer is Ti/TiN and the contact metal plug is Tungsten."

The elements of Claim 4 are disclosed in Shiraishi, Kobayashi, and the knowledge of the POSITA. Claim 4 depends on Claim 3, which is discussed above. *See supra* Section VIII(D)(1). Shiraishi further discloses the uses of a barrier metal layer that is made of TiW (titanium-tungsten). Ex. 1009 at [0076]. As described above, Kobayashi discloses the use of a tungsten (W) contact metal plug. Ex. 1008 at [0052], [0066], Fig. 5A. Kobayashi also discloses the use of a barrier metal layer that is made of Ti and TiN. Ex. 1008 at [0062]; Ex. 1003 at ¶ 117.

3. Claim 5

a. 5: "The trenched MOSFET of Claim 4, wherein the source contact trench is selected from one of a vertical shape and a taper shape."

Claim 5 depends on Claim 4, which is discussed above in Section VIII(D)(2). The remaining elements of Claim 5 are disclosed in Shiraishi, which discloses a trenched MOSFET with a vertical source contact trench and a tapered source contact trench. Ex. 1009 at Fig. 8, Fig. 35; Ex. 1003 at ¶ 118.

4. Claim 6

a. 6: "The trenched MOSFET of claim 1, wherein the silicon substrate, the epitaxial layer, and the source layer are P-type; the base layer and lateral contact layer are N-type; and each of the source contact trenches further has a N-type base contact layer at a bottom thereof, and the lateral contact layer has less doping concentration than the base contact layer at bottom."

The elements of Claim 6 are disclosed in Shiraishi and Kobayashi. Claim 6 depends on Claim 1, which is disclosed in Shiraishi as explained above in Section VIII(C)(1). In addition, Shiraishi discloses a trenched MOSFET with layers of a first conductivity type and second conductivity type opposite to the first conductivity type along with specific embodiments of an n-channel MOSFET. *See*, *e.g.*, Ex. 1008 at [0017]-[0028], [0067], Claim 1. Kobayashi similarly discloses a general trenched MOSFET with layers of a first conductivity type and

second conductivity type opposite to the first conductivity type along with specific embodiments of n-channel MOSFETs. *See*, *e.g.*, Ex. 1008 at Claim 1, [0062]. Kobayashi also discloses "inverting the conductive type, [such that] this invention is also applicable to a P-channel MOSFET structure." Ex. 1008 at [0072].

Further, a POSITA would know that inverting the conductivity types simply allow the formation of either an N-channel MOSFET or a P-channel MOSFET. Ex. 1003 at ¶¶ 119-120.

5. Claim 7

a. 7: "The trenched MOSFET of claim 6, wherein further comprises a barrier metal layer and contact metal plugs."

The elements of Claim 7 are disclosed in Shiraishi, Kobayashi and the knowledge of the POSITA. Claim 7 depends on Claim 6, which is discussed above in Section VIII(D)(4). In addition, the remaining elements are discussed as described above in relation to Claim 3. *See supra* Section VIII(D)(1). The POSITA would understand that the inversion of conductivity types would not affect the previous disclosure and analysis. Ex. 1003 at ¶¶ 121-122.

6. Claim 8

a. 8: "The trenched MOSFET of claim 7, wherein the barrier metal layer is Ti/TiN and the contact metal plug is Tungsten."

The elements of Claim 8 are disclosed in Shiraishi and Kobayashi and the knowledge of the POSITA. Claim 8 depends on Claim 7, which is discussed

above in Section VIII(D)(5). In addition, the remaining elements are discussed above in relation to Claim 4. *See supra* Section VIII(D)(2). The POSITA would understand that the inversion of conductivity types would not affect the previous disclosure and analysis. Ex. 1003 at ¶ 123.

7. Claim 9

a. 9: "The trenched MOSFET of claim 8, wherein the source contact trench is selected from one of a vertical shape and a tapered shape."

Claim 9 depends from Claim 8, which is discussed above in Section VIII(D)(6). The remaining elements of Claim 9 are disclosed in Shiraishi, as described above in relation to Claim 5. *See supra* Section VIII(D)(3). The POSITA would understand that the inversion of conductivity types would not affect the previous disclosure and analysis. Ex. 1003 at ¶ 124.

8. Combining Shiraishi and Kobayashi in light of knowledge of the POSITA

As discussed above, the combination of Shiraishi and Kobayashi discloses all elements of Claims 3-9 (*see* §§ VIII(D)(1)-(7)). For the reasons discussed below, it would have been obvious to a POSITA before the effective filing date of the '634 Patent to combine Shiraishi and Kobayashi to arrive at Claims 3-9, rendering those claims invalid under 35 U.S.C. § 103. In particular, the POSITA would have been motivated to combine the metal contact plug and barrier metal layer of Kobayashi with a reasonable likelihood of success to arrive at the subject

matter of Claims 3-5. In addition, the POSITA would have been motivated to combine the disclosure of Kobayashi to invert the P/N types of Shiraishi to arrive at the subject matter of Claims 6-9. Ex. 1003 at ¶¶ 125-134.

First, Shiraishi, Kobayashi, and the '634 Patent are analogous art seeking to solve similar problems. Shiraishi, Kobayashi, and the '634 Patent are in the same field of endeavor, Vertical Power MOSFET structures, and the methods to improve the performance tradeoff in ON-state (ON-Resistance and speed), and OFF-state (breakdown voltage). Moreover, Shiraishi, Kobayashi, and the '634 Patent disclose a similar doping concentration engineering technique, *i.e.*, dopant ion implantation, that allows for the formation of a low resistance source contact, at the bottom of the base region and/or also on the sidewall of the trenched contact region, with minimal impact to the threshold voltage or the ON-Resistance of the Power MOSFET.

Second, specific to the metal contact plugs, Kobayashi expressly teaches that the contact metal plug "allows the resistance component of the source electrode **18** [to be] reduced" because the plug creates a flat surface for the source electrode. Ex. 1008 at [0066]; Ex. 1003 at ¶ 128. Further, Kobayashi discloses that the source electrode "having a flat surface assures a wide contact area in wire bonding or clip bonding carried out for the surface so that a total on-resistance after mounting can be reduced." Ex. 1008 at [0066]. Finally, "it is possible to perform

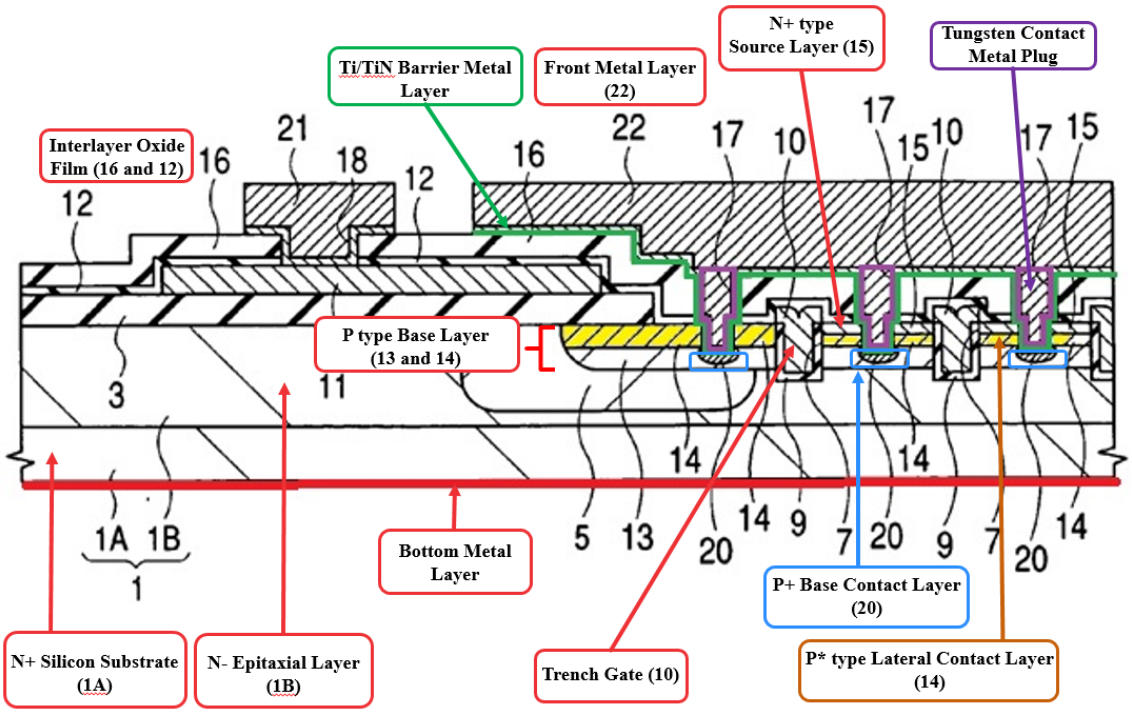
chip mounting by bump connection, which is difficult when the source electrode has an irregular surface." *Id.* In particular, Kobayashi teaches the use of tungsten metal contact plugs. The POSITA would thus be motivated to combine the metal contact plugs taught by Kobayashi with the disclosure of Shiraishi.

Third, the POSITA would have been motivated to combine the barrier metal layer disclosed in Kobayashi to the MISFET disclosed in Shiraishi. In general, a POSITA would know that the use of a barrier metal layer, made of materials such as Ti and TiN, would help to promote the adhesion of the tungsten contact plug expressly taught in Kobayashi to the contact area. Ti and TiN also serve as a barrier layer to prevent unwanted elements, such as fluorine from the deposition process of W, seeping into the underlying silicon surface, which would degrade the performance of the transistor. Thus, the POSITA would be motivated to apply a known solution (the barrier layer) to a known problem (unwanted seeping of fluorine into the silicon surface) to yield predictable results. Ex. 1003 at ¶¶ 129-131.

Fourth, inverting the P- or N-type regions of the MOSFET is known in the art. A POSITA generally inverts the regions to create either a P- or N- channel MOSFET as required by the specific product the transistor is supporting. Moreover, both Kobayashi and Shiraishi disclose a general MOSFET that could be tailored to be P- or N- channel. In particular, the POSITA would understand that

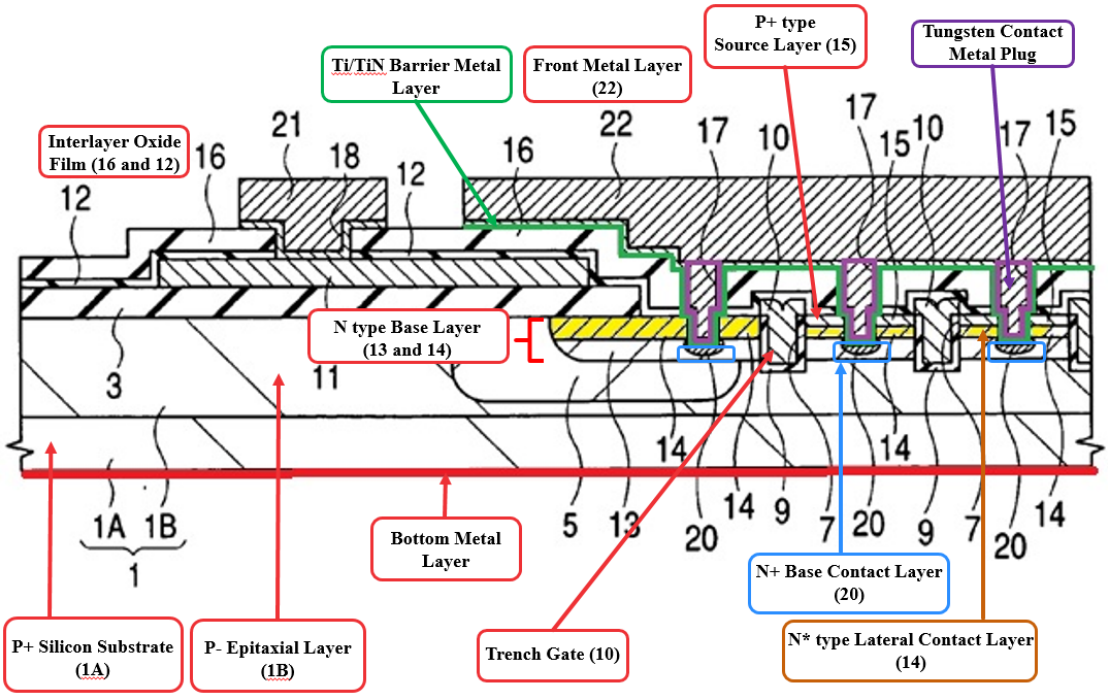
the inversion of the P- and N- types would not affect the disclosure of contact metal plugs or barrier metal layers.

Accordingly, the combination of Shiraishi and Kobayashi renders obvious Claims 3-9, as illustrated below in a hypothetical diagram based on Shiraishi's Figure 9 with the addition of the tungsten (W) source contact plugs and Ti/TiN barrier metal layer according to disclosures in Kobayashi. Ex. 1003 at ¶ 133.



Shiraishi, Figure 9 (annotated)

Below is the same hypothetical diagram but with inverted conductivity types, showing a p-channel MOSFET. Ex. 1003 at ¶ 134.



Shiraishi, Figure 9 (annotated)

This case is also similar to *Nanya*, where the PTAB invalidated claims directed to MOS semiconductor with a trenched gate. *Nanya* at 6-7, 22-35. Citing to figures in the prior art, the Board held that the Petitioner had "persuasively map[ped]" the elements of each challenged claim, such that the claims were anticipated and/or obvious to the POSITA. *See*, *e.g.*, *id.* at 24-25. Further, the Board found the challenged claims obvious, because the Petitioner provided "persuasive evidence that, to the extent that [the prior art] does not expressly disclose the [claim element] . . . , an ordinarily skilled artisan would have been led to modify [the prior art]'s MOS transistor in a series of steps that results in the subject matter of those claims." *Id.* at 25. The Board also found the challenged

claims obvious, because "any missing details in [the prior art] . . . would have been 'conventional' and, thus, fully within the grasp of an ordinarily skilled artisan." *Id.* at 34 (internal citations omitted) (finding so because the patent at issue admitted that the disputed implantation method was "conventional"); *see* Ex. 1001 at Fig. 1 (Prior Art), 1:28-29, (admitting certain elements of the Challenged Claims, including "a barrier metal layer (**110**), [and] a plurality of contact metal plugs (**111**)," are in prior art).

The combination of Shiraishi and Kobayashi regarding the barrier metal layer is likewise similar to *Micron*, where the Board agreed with Petitioner's expert that the proposed combination "is merely the use of known technique that improves similar devices . . . in the same way . . . to yield predictable results." *Micron* at 35. Further, Shiraishi and Kobayashi themselves expressly teach and "provide evidence supporting a finding that a skilled artisan would have been motivated to combine" the tungsten metal contact plug with the Shiraishi MOSFET structure. *Iancu*, 813 F. App'x at 521.

Based on reasons explained above, a POSITA would have found it obvious to combine the MISFET of Shiraishi and the barrier metal layer and contact metal plugs of Kobayashi. *See KSR Int'l*, 550 U.S. at 415-18; *see also Micron* at 35; and *Nanya* at 24-25, 34.

E. Ground 5: Claims 1-9 are unpatentable under 35 U.S.C. § 103 as obvious over Kobayashi in light of Shiraishi and the knowledge of the POSITA.

Claims 1-9 of the '634 Patent are unpatentable under 35 U.S.C. § 103 as obvious over Kobayashi in light of Shiraishi and the knowledge of the POSITA. The following discussion is fully supported by the Declaration of Dr. David Liu. Ex. 1003 at ¶¶ 135-169.

1. Claim 1

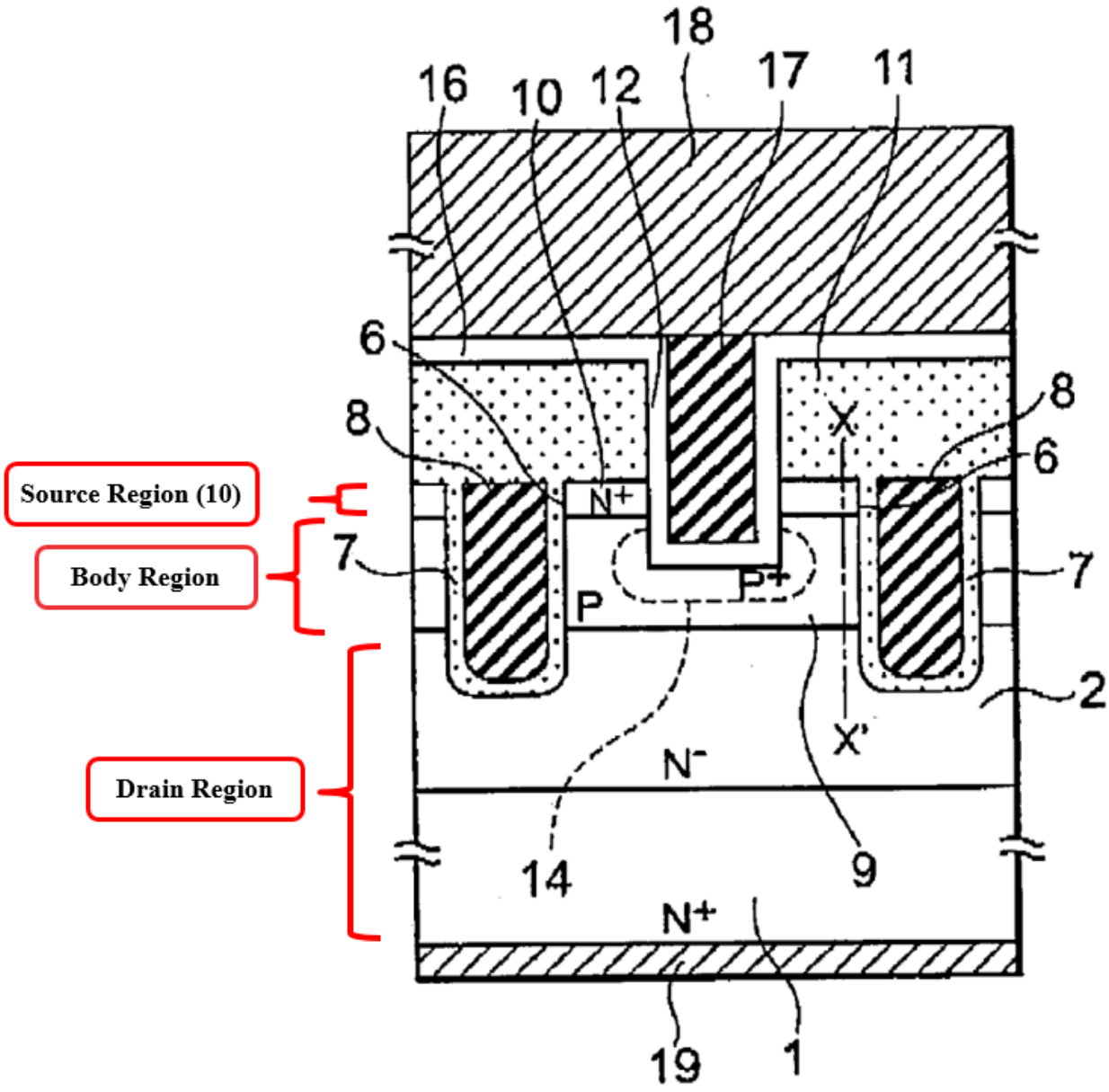
a. 1 [preamble]: "A trenched MOSFET with trenched source contact, comprising:"

To the extent the preamble is limiting, it is disclosed in Kobayashi, which discloses a trenched MOSFET with source contact trenches. Ex. 1008 at Fig. 5A, [0052]; Ex. 1003 at ¶ 135.

b. 1[a]: "a semiconductor region having a drain region, a body region and a source region, comprising, a silicon substrate, an epitaxial layer corresponding to said drain region disposed on the top of said silicon substrate, a base layer corresponding to said body region disposed on the top of said epitaxial layer, and a source layer corresponding to said source region disposed on the top of said base layer;"

Element 1[a] is disclosed in Kobayashi, which describes a vertical trenched MOSFET with a drain region, a body region, and a source region. Ex. 1008 at Fig. 5A, [0018], [0052]; Ex. 1003 at ¶ 136. Specifically, Kobayashi discloses "an N^+-type silicon substrate **1** and an N^--type epitaxial layer **2** formed on one surface

of the N^+-type silicon substrate **1**. A P-type base layer **9** and an N^+-type source layer **10** are formed on a surface of the N^--type epitaxial layer **2** . . . ." Ex. 1008 at [0052]; Ex. 1003 at ¶¶ 136-137.



Kobayashi, Figure 5A (annotated in regards to Claim element 1a)

c. 1[b]: "a front metal layer formed on the upper surface of said semiconductor region"

Element 1[b] is disclosed in Kobayashi, wherein a source electrode (18) is located on top of the barrier metal layer and source contact plug. Ex. 1008 at Fig. 5A, [0052]; Ex. 1003 at ¶ 138.

d. 1[c]: "an interlayer oxide film formed between said source layer and said front metal layer;"

Element 1[c] is disclosed in Kobayashi, wherein an interlayer oxide film (11) is formed atop the gate trenches and between the source region (10) and the source electrode (18). Ex. 1008 at Fig. 5A, [0052]; Ex. 1003 at ¶ 139.

e. 1[d]: "a bottom metal layer formed on the lower surface of said semiconductor region;"

Element 1[d] is disclosed in Kobayashi, wherein a drain electrode (19) is formed on the surface of the N^+-type silicon substrate (1). Ex. 1008 at Fig. 5A, [0052]; Ex. 1003 at ¶ 140.

f. 1[e]: "a plurality of trenched gates covered by said interlayer oxide film are formed on top of said source layer extending downwardly through said base layer to a portion of said epitaxial layer; and"

Element 1[e] is disclosed in Kobayashi. As shown in Figure 5A, Kobayashi discloses a plurality of trench gates (6) that are covered by the interlayer oxide film

(11) and extend downward through the source layer (10), the base layer (9), and into the epitaxial layer (2). Ex. 1008 at Fig. 5A, [0052]; Ex. 1003 at ¶ 141.

Specifically, Kobayashi discloses that "[i]n each of trenches **6** reaching the N^--type epitaxial layer **2** through the P-type base layer **9**, a gate oxide film **7** and a polysilicon **8** are filled." Ex. 1008 at [0052]; Ex. 1003 at ¶¶ 141-142.

g. 1[f]: "a plurality of source contact trenches formed on the top of said interlayer oxide film extending downwardly through said source layer to a portion of said base layer"

Element 1[f] is disclosed in Kobayashi. Specifically, as shown in Fig. 5A, Kobayashi discloses contact holes (12) formed on top of the interlayer oxide film and extends down through the source layer to the body region. Ex. 1008 at Fig. 5A, [0052]; Ex. 1003 at ¶ 143.

Specifically Kobayashi discloses "[b]etween the trench gates adjacent to each other, a contact hole **12** having a predetermined depth is formed to reach the P-type base layer **9** though the N^+-type source layer **10**." Ex. 1008 at [0052]; Ex. 1003 at ¶¶ 143-144.

h. 1[g]: "wherein the sidewalls of said trenches in said base layer are covered by the lateral contact layer;"

Element 1[g] is disclosed by Kobayashi, Shiraishi, and the knowledge of the POSITA. Kobayashi discloses a base contact layer that extends partially up the

sidewalls in the base layer of the source contact trenches. Ex. 1008 at Fig. 5A, [0061]; Ex. 1003 at ¶ 145; *see also* Ex. 1002 at 29.

As shown in Figure 8, Shiraishi discloses an additional semiconductor layer (14) along the entire sidewalls in the base layer of the contact trench that serves as "a punch-through stopper layer." Ex. 1009 at Fig. 8, [0073], [0080], [0084]-[0085]; Ex. 1003 at ¶¶ 146-148.

i. 1[h]: "wherein the bottom base of said trenches in said base layer are covered by the base contact layer."

Element 1[h] is disclosed in Kobayashi, in which the bottom of the contact hole is covered by a base contact layer (14). Ex. 1008 at Fig. 5A, [0061]; Ex. 1003 at ¶ 149.

2. Claim 2

a. 2[a] "The trenched MOSFET of claim 1, wherein the silicon substrate, the epitaxial layer, and the source layer are N-type;"

Claim 2 depends on Claim 1, which is discussed above in Section VIII(E)(1). Element 2[a] is otherwise disclosed in Kobayashi. Kobayashi discloses a trenched MISFET wherein the silicon substrate, the epitaxial layer, and the source layer are N-type. Ex. 1008 at Fig. 5A, [0052]; Ex. 1003 at ¶ 150.

b. 2[b] "the base layer and lateral contact layer are P-type;"

Element 2[b] is disclosed in Kobayashi, Shiraishi, and the knowledge of the POSITA. Kobayashi discloses a p-type base layer and P^+-type base contact layer. Ex. 1008 at Fig. 5A, [0052], [0061]; Ex. 1003 at ¶ 151. Shiraishi discloses a P-type lateral contact layer that serves as an anti-punch-through layer. Ex. 1009 at [0073].

c. 2[c] "and each of the source contact trenches further has a P-type base contact layer at a bottom thereof, and the lateral contact layer has less doping concentration than the base contact layer at bottom."

Claim element 2[c] are disclosed in Kobayashi, Shiraishi, and the knowledge of the POSITA. Kobayashi discloses a P^+-type base contact layer at the bottom of the source trenches. Ex. 1008 at Fig. 5A, [0061]; Ex 1003 at ¶ 152.

Shiraishi discloses an additional semiconductor layer (14) along the sidewalls in the base layer of the contact trench that serves as "a punch-through stopper layer." Ex. 1009 at Fig. 8, [0073], [0080], [0084]-[0085]. Shiraishi also discloses that "p-type semiconductor region **14** may be locally higher in impurity concentration than the p type semiconductor region **13**." Ex. 1009 at Fig. 8, [0080]. In addition, Shiraishi discloses that "[i]mpurity concentration in the p^+type semiconductor region **20** may be rendered higher than that in the p-type semiconductor region **14**." Ex. 1009 at Fig. 8, [0075]; Ex. 1003 at ¶¶ 153-154.

3. Claim 3

a. 3: "The trenched MOSFET of Claim 2, wherein further comprises a barrier metal layer and a plurality of contact metal plugs."

The elements of Claim 3 are disclosed Kobayashi in light of Shiraishi and the knowledge of the POSITA. Claim 3 depends on Claim 2, which is discussed above in Section VIII(E)(2). Koyabashi also discloses the use of contact metal plugs and a barrier metal layer. Ex. 1008 at [0052]-[0053], [0066], Fig. 5A; Ex. 1003 at ¶ 155.

4. Claim 4

a. 4: "The trenched MOSFET of Claim 3, wherein the barrier metal layer is Ti/TiN and the contact metal plug is Tungsten."

The elements of Claim 4 are disclosed in Kobayashi in light of Shiraishi and the knowledge of the POSITA. Claim 4 depends on Claim 3, which is discussed above in Section VIII(E)(3). Kobayashi further discloses the use of the contact metal plug that is made of tungsten (W). Ex. 1008 at [0052], [0066], Fig. 5A. Kobayashi also discloses the use of a barrier metal layer that is made of Ti and TiN. Ex. 1008 at [0062]; Ex. 1003 at ¶ 156.

5. Claim 5

a. 5: "The trenched MOSFET of Claim 4, wherein the source contact trench is selected from one of a vertical shape and a taper shape."

The elements of Claim 5 are disclosed in Kobayashi in light of Shiraishi and the knowledge of the POSITA. Claim 5 depends on Claim 4, which is discussed in Section VIII(E)(4). Kobayashi, further discloses a trenched MOSFET with vertical or taper shaped source contact trenches. Ex. 1008 at Fig. 5A, [0028]; Ex. 1003 at ¶ 157.

6. Claim 6

a. 6: "The trenched MOSFET of claim 1, wherein the silicon substrate, the epitaxial layer, and the source layer are P-type; the base layer and lateral contact layer are N-type; and each of the source contact trenches further has a N-type base contact layer at a bottom thereof, and the lateral contact layer has less doping concentration than the base contact layer at bottom."

The elements of Claim 6 are disclosed in Kobayashi in light of Shiraishi and the knowledge of the POSITA. Claim 6 depends from Claim 1, which is explained in Section VIII(E)(1). Kobayashi further discloses a general trenched MOSFET with layers of a first conductivity type and second conductivity type opposite to the first conductivity type along with specific embodiments of N-channel MOSFETs. *See*, *e.g.*, Ex. 1008 at Claim 1, [0062]. Kobayashi also discloses "inverting the

conductive type, [such that] this invention is also applicable to a P-channel MOSFET structure." Ex. 1008 at [0072]. Shiraishi similarly discloses a trenched MOSFET with layers of a first conductivity type and second conductivity type opposite to the first conductivity type along with specific embodiments of an n-channel MOSFET. *See*, *e.g.*, Ex. 1009 at [0017]-[0028], [0067], Claim 1; Ex. 1003 at ¶ 158.

Further, a POSITA would know that inverting the conductivity types simply allow the formation of either an N-channel MOSFET or a P-channel MOSFET. Ex. 1003 at ¶ 159.

7. Claim 7

a. 7: "The trenched MOSFET of claim 6, wherein further comprises a barrier metal layer and contact metal plugs."

The elements of Claim 7 are disclosed in Kobayashi in light of Shiraishi and the knowledge of the POSITA. Claim 7 depends on Claim 6, which is discussed in Section VIII(E)(6). The remaining elements of Claim 7 are disclosed by Kobayashi, as described above in relation to Claim 3. *See supra* Section VIII(E)(3). The POSITA would understand that the inversion of conductivity types would not affect the previous disclosure and analysis. Ex. 1003 at ¶¶ 160-161.

8. Claim 8

a. 8: "The trenched MOSFET of claim 7, wherein the barrier metal layer is Ti/TiN and the contact metal plug is Tungsten."

The elements of Claim 8 are disclosed in Kobayashi in light of Shiraishi and the knowledge of the POSITA. Claim 8 depends on Claim 7, which is discussed above in Section VIII(E)(7). The remaining elements of Claim 8 are disclosed by Kobayashi, as described above in relation to Claim 4. Section VIII(E)(4). The POSITA would understand that the inversion of conductivity types would not affect the previous disclosure and analysis. Ex. 1003 at ¶ 162.

9. Claim 9

a. 9: "The trenched MOSFET of claim 8, wherein the source contact trench is selected from one of a vertical shape and a tapered shape."

The elements of Claim 9 are disclosed Kobayashi in light of Shiraishi and the knowledge of the POSITA. Claim 9 depends on Claim 8, which is discussed above in Section VIII(E)(8). The remaining elements of Claim 9 are disclosed by Kobayashi, as described above in relation to Claim 5. *See supra* Section VIII(E)(5). The POSITA would understand that the inversion of conductivity types would not affect the previous disclosure and analysis. Ex. 1003 at ¶ 163.

10. Combining Kobayashi and Shiraishi in light of knowledge of the POSITA

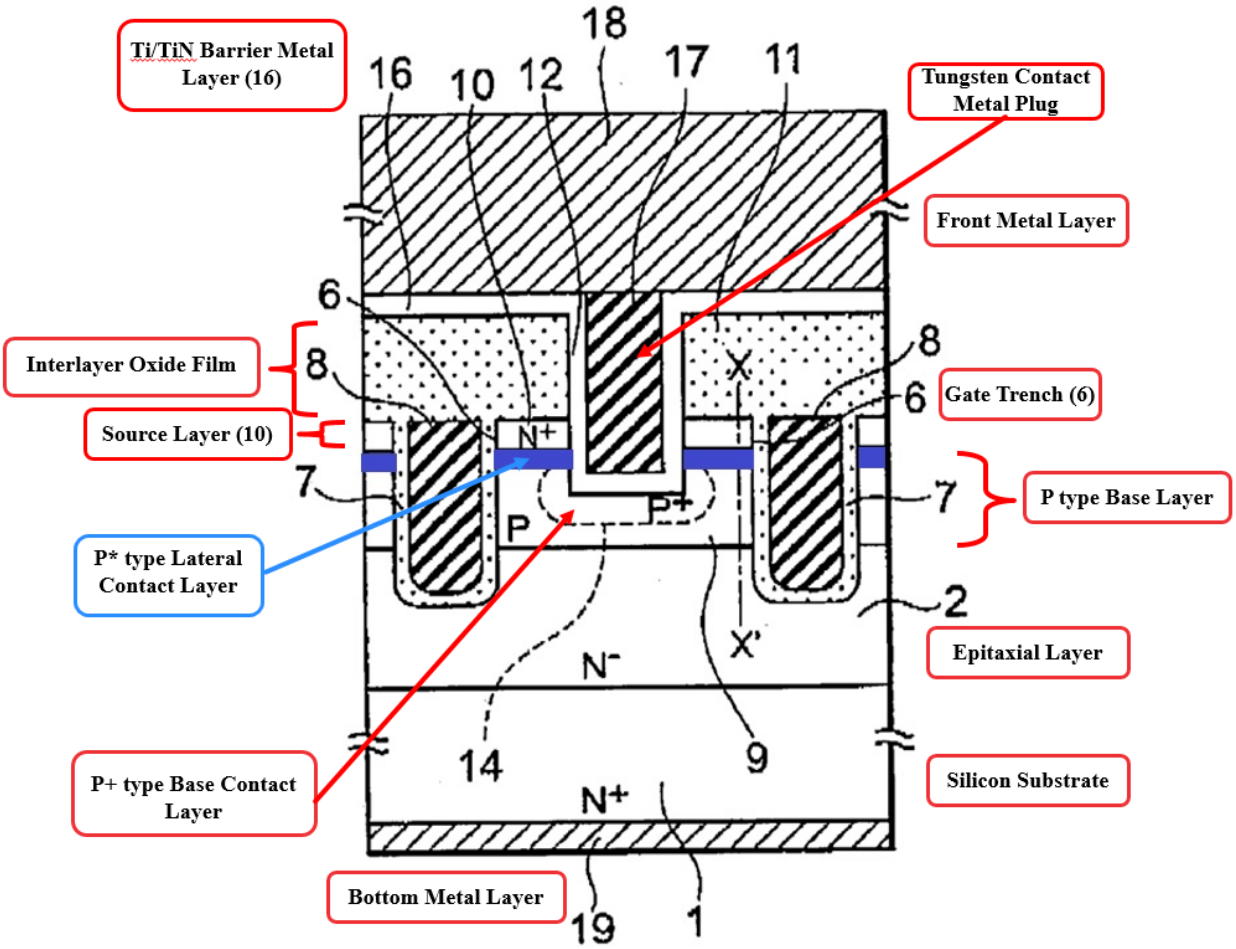
As discussed above, the combination of Kobayashi and Shiraishi discloses all elements of Claims 1-9 (*see* §§ VIII(E)(1)-(9)). For the reasons discussed below, it would have been obvious to a POSITA before the effective filing date of the ’634 Patent to combine Shiraishi and Kobayashi to arrive at Claims 1-9, rendering those claims invalid under 35 U.S.C. § 103. In particular, the POSITA would be motivated to combine the lateral contact layer and doping concentration profiles of Shiraishi with Kobayashi to arrive at the subject matter of Claims 1-2, and therefore to dependent Claims 3-9. Ex. 1003 at ¶¶ 164-170.

First, Kobayashi, Shiraishi, and the ’634 Patent are analogous art seeking to solve similar problems. Kobayashi, Shiraishi, and the ’634 Patent are in the same field of endeavor, Vertical Power MOSFET structures, and the methods to improve the performance tradeoff in ON-state (ON-Resistance and speed), and OFF-state (breakdown voltage). Moreover, Kobayashi, Shiraishi and the ’634 Patent disclose a similar doping concentration engineering technique, *i.e.*, dopant ion implantation, that allows for the formation of a low resistance source contact, at the bottom of the base region and/or also on the sidewall of the trenched contact region, with minimal impact to the threshold voltage or the ON-Resistance of the Power MOSFET.

Second, Shiraishi expressly teaches a lateral contact layer along the entire sidewalls of the contact trench in the base layer that serves as "a punch-through stopper layer." Ex. 1009 at Fig. 8, [0073], [0080], [0084]-[0085]; Ex. 1003 at ¶¶ 146-147. The POSITA would thus be motivated to combine the distinct lateral contact layer of Shiraishi with P doping concentration that is greater that the P-type concentration of the base layer but less than the P-type concentration of the base contact layer with the disclosure of Kobayashi to optimize the MOSFET and prevent punch-through.

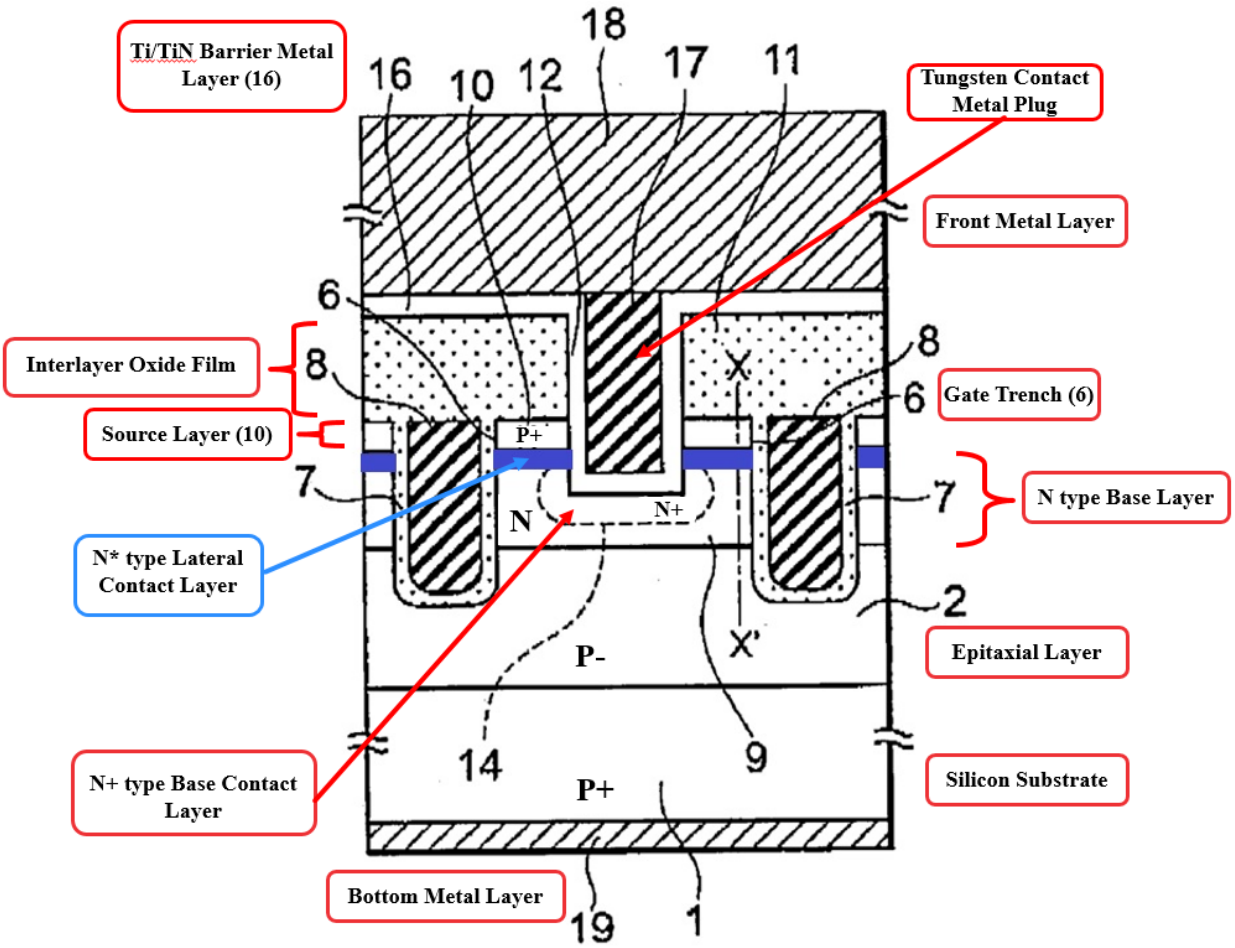
Third, Shiraishi also expressly teaches doping concentration profiles of the lateral contact layer and base contact layer that prevents punch-through. Ex. 1009 at Abstract, [0073]. Thus, the POSITA would be motivated to try these doping concentration profiles, as opposed to the doping dosing as disclosed in Kobayashi, to achieve an anti-punch-through result.

Accordingly, the combination of Kobayashi and Shiraishi renders obvious Claims 1-9, as illustrated below in a hypothetical diagram based on Kobayashi's Figure 5A with the addition of the lateral contact layer according to disclosure in Shiraishi. Ex. 1003 at ¶ 169.



Kobyashi, Figure 5A (annotated)

Below is the same hypothetical diagram but with inverted conductivity types, showing a p-channel MOSFET. Ex. 1003 at ¶ 170.



Kobyashi, Figure 5A (annotated)

This case is similar to *Micron,* where the Board found the MOS semiconductor claims to be obvious, because the prior art references "provide[d] evidence supporting a finding that a skilled artisan would have been motivated to combine." *Iancu*, 813 F. App'x at 521. Specifically, the Board in *Micron* agreed with Petitioner that "the application of the tungsten silicide layer of Ooka on the polysilicon gate of Tanaka is merely combining prior art elements (Tanaka's gate electrode and Ooka's tungsten silicide layer) according to known methods (*e.g.*, CVD, as Ooka describes) to yield predictable results (a gate with a tungsten

silicide layer on top was a conventional device), is merely the use of known technique that improves similar devices in the same way, and is merely applying a known technique to a known device ready for improvement to yield predictable results" *Micron* at 35 (cleaned-up). Here, the POSITA would have been motivated to combine the lateral contact layer of Shiraishi to the MOSFET in Kobayashi to act as a punch-through stopper layer (as taught by Shiraishi).

Based on reasons explained above, a POSITA would have found it obvious to combine Kobayashi and Shiraishi. *See KSR Int'l*, 550 U.S. at 415-18; *see also Micron* at 35; and *Nanya* at 24-25, 34.

IX. THE BOARD'S DISCRETION UNDER 35 U.S.C. § 325(d)

The U.S. Patent (No. 6,888,196) that issued from Kobayashi, presented in Grounds 2, 4, and 5, was cited by the examiner during prosecution of the '634 Patent. In the Notice of Allowance, the examiner provided the following reason for allowance: "Claim 1 limits the trenched MOSFET to having a trench in which the base and entire sidewall are covered with the lateral contact layer. Kobayashi covers the base and only a portion of the trench sidewall with the lateral contact layer." Ex. 1002 at 29. Petitioner respectfully requests reconsideration of Kobayashi, because Petitioner combines Kobayashi with Shiraishi, Shiraishi with Kobayashi, and Hirler with Kobayashi in its Petition to put forth substantially different prior art and arguments than the examiner did during prosecution. In

addition, the Petition is supported by the declaration of an expert which was not considered by the examiner.

A. Applicable law

The PTAB uses a two-part framework to determine whether to exercise its discretion under 35 U.S.C. § 325(d):

> (1) determining whether the same or substantially the same art previously was presented to the Office or whether the same or substantially the same arguments previously were presented to the Office; and (2) if either condition of [the] first part of the framework is satisfied, [determining] whether the petition has demonstrated that the Office erred in a manner material to the patentability of challenged claims.

Snap Inc. v. SRK Technology LLC, IPR2020-00820, Paper 15 at 19-20 (PTAB Oct. 21, 2020) (internal quotations omitted) (citing *Advanced Bionics, LLC v. Med-El Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 at 8 (PTAB Feb. 13, 2020) (precedential) ("*Advanced Bionics*")).

Under the *Advanced Bionics* framework, the PTAB considers the non-exclusive "*Becton, Dickinson*" factors. *Becton, Dickinson & Co. v. B. Braun Melsungen AG*, IPR2017-01586, Paper 8 at 17-18 (PTAB Dec. 15, 2017) (precedential as to Section III.C.5, first paragraph) (footnote omitted) ("*Becton, Dickinson*"). Specifically, factors (a), (b), and (d) below relate to determining whether the same or substantially the same art previously was presented to the Office or whether the same or substantially the same arguments previously were

presented to the Office. *Advanced Bionics* at 20. Factors (a), (b), and (d) are as follows:

> (a) the similarities and material differences between the asserted art and the prior art involved during examination; (b) the cumulative nature of the asserted art and the prior art evaluated during examination; . . . (d) the extent of the overlap between the arguments made during examination and the manner in which petitioner relies on the prior art;

Becton, Dickinson at 17-18.

Because Petitioner relies on Kobayashi in a substantially different way than the examiner, "neither the same or substantially the same art nor the same or substantially the same arguments" were presented previously to the Office, and there is no need to consider whether the Office erred in a material manner in step two of the *Advanced Bionics* framework. *Snap* at 28.

B. Petitioner presents substantially different prior art and arguments from those presented by the examiner

While Kobayashi was considered during original prosecution of the '634 Patent, it was considered alone and not in combination with any other prior art reference. Ex. 1001 at 1; Ex. 1002 at 29. Specifically, neither Hirler nor Shiraishi were considered during prosecution. Further, the disclosures in Hirler and Shiraishi are also not substantially similar to Kobayashi, the only other prior art evaluated by the examiner. For example, Shiraishi discloses an additional, distinct semiconductor layer at the sidewalls of the source contact trenches to serve as a punch-through layer along with a base contact layer. Ex. 1009 at [0084]-[0085].

Shiraishi also discloses that this additional semiconductor region be doped differently from the base contact layer and the body region. Ex. 1009 at [0075], [0080]. As another example, Hirler discloses an embodiment with a distinct body amplification zone at the sidewalls of the source contact trench, that is doped to a different concentration than the body contact zone. Ex. 1005 at Fig. 2F; Ex. 1006 at [0030]-[0031]. In contrast, Kobayashi discloses a single base contact layer at the bottom of the trench that extends partially up the sidewalls of the source contact trench and no distinct lateral contact layer. Ex. 1008 at Fig. 5A, [0061], Claim 1, Claim 3. Hirler and Shiraishi therefore are materially different from Kobayashi. *See Samsung Electronics Co., Ltd. v. Immersion Corp.*, IPR2018-01469, Paper 10 at 11-12 (PTAB March 7, 2019).

Moreover, the examiner did not cite Kobayashi for the same purposes as Petitioner relies on Kobayashi. *Advanced Bionics* at 20; *see also Samsung Electronics* at 13-14. Specifically, the examiner relied on Kobayashi as a single, primary reference, which disclosed, according to the examiner, the elements of Claim 1 with the exception of a lateral contact layer that covered the "entire" sidewalls of the source contact trench. Ex. 1002 at 29. On the other hand, Petitioner relies on Hirler and Shiraishi as primary references and relies on Kobayashi in combination with other references that were not considered by the examiner to show obviousness.

Finally, Kobayashi in combination with Shiraishi, Shiraishi in combination with Kobayashi, and Hirler in combination with Kobayashi are distinct combinations not considered by the examiner. *Samsung Electronics* at 13-14. These are entirely different arguments compared to the examiner's reliance on a singular reference.

Because Petitioner relies on Kobayashi in a substantially different way and presents arguments not considered during prosecution by the examiner, Petitioner requests therefore that the Board does not use its discretion to deny institution based on Petitioner's use of Kobayashi.

To the extent the Board disagrees with Petitioner in relation to the grounds based on Kobayashi, the Petition should nonetheless be instituted because the Board should not exercise its discretion where only some of the grounds fall within the scope of 35 U.S.C. § 325(d). *Unified Patents, LLC f/k/a Unified Patents Inc. v. Sovereign Peak Ventures, LLC*, IPR2021-00852, Paper 9 at 40 (PTAB Nov. 9, 2021).

X. THE ASSERTED GROUNDS ARE NEITHER EXCESSIVE NOR REDUNDANT

The five unpatentability grounds asserted herein are not excessive. *See, e.g.*, *Favored Tech Corp. v. P2i Ltd.*, IPR2020-01198, Paper 9 at 48 (PTAB Jan. 27, 2021) (instituting review and holding that asserting five distinct grounds (with no more than three references per ground, and seven references in total) was not

excessive) (distinguishing *Adaptics Ltd. v. Perfect Company*, IPR2018-01596, Paper 20 at 19 (PTAB Mar. 6, 2019)). The present Petition asserts only five grounds of unpatentability. Ground 1 challenges Claims 1-2 and 6; Ground 2 challenges Claims 3-5 and 7-9; Ground 3 challenges Claims 1-2; Ground 4 challenges Claims 3-9; and Ground 5 challenges Claims 1-9. Each claim is challenged by no more than three grounds. Further, only Grounds 2, 4, and 5 assert more than one reference, while Grounds 1 and 3 assert one reference each, Hirler and Shiraishi respectively. Accordingly, the Petition is far from the "hundreds of possible combinations" of *Adaptics*. *See Favored Tech Corp.* at 48.

Nor are the five grounds redundant. Grounds 1 and 2 are not redundant of Grounds 3, 4, and 5 at least because Grounds 1 and 2 are based on a different primary reference, Hirler, whereas Grounds 3 and 4 are based on primary reference Shiraishi, and Ground 5 is based on primary reference Kobayashi. Hirler, Shiraishi, and Kobayashi are substantively different and are mapped differently to the claims of the '634 Patent. Moreover, there is only two reference that overlap on certain Grounds. Kobayashi is relied on in Grounds 2, 4 and 5, as a secondary reference in Grounds 2 and 4 and as a primary reference in Ground 5. Shiraishi is relied on as a primary reference in Grounds 3 and 4, and as a secondary reference in Ground 5. Grounds 2, 4 and 5 are based on pre-AIA 35 U.S.C. § 103(a), while Grounds 1 and 3 are based on pre-AIA 35 U.S.C. § 102(b). Thus, Grounds 1-5 are

asserted with particularity such that discretionary denial of the petition would be improper.

XI. THE *FINTIV* FACTORS DO NOT WEIGH AGAINST INSTITUTION.

As explained above in Section VIII, this Petition presents compelling evidence of unpatentability, which alone warrants institution. Director Vidal, Memorandum, "Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation," at 9 (June 21, 2022). Here, the grounds are straightforward and explain how Hirler and Shiraishi anticipate (and how Hirler combined with Kobayashi, Shiraishi combined with Kobayashi, and Kobayashi combined with Shiraishi render obvious) all of the Challenged Claims. This evidence leads to a conclusion that one or more of the claims are unpatentable, and so the Board must decline to exercise discretion under § 314(a). *Id*.

In addition, a "holistic view" of the six *Fintiv* factors demonstrates that the Board should institute this petition. *Apple v. Fintiv*, IPR2020-00019, Paper 11 at 6 (PTAB Mar. 20, 2020).

A. Factor 1 - Stay of parallel district court litigation

Two pending litigations involve the '634 Patent. *See supra* § II(B). No party has requested a stay of litigation in either litigation, and so this factor is neutral. *Fintiv*, Paper 15 at 12 (PTAB May 13, 2020).

B. Factor 2 - Proximity of the district court's trial date

This petition is being filed in October 2023, and so a final written decision ("FWD") should issue around April 2025. Petitioner is not involved in the Asustek Action or the AOS Action, there is no district court trial date (or projected trial date) that applies to Petitioner, and so this factor favors institution.

To the extent the Board considers the time to trial in the AOS Action (which does not involve Petitioner), this factor weighs in favor of institution because the district court has not conducted a *Markman* hearing; the court has not issued a *Markman* order; expert discovery has not begun; substantial work remains before trial; and no trial date has been set. *See* Exs. 1013-1015. Also, the median time to trial in the Northern District of California is 37.1 months, which would result in a trial occurring around or after October 2025, well after the anticipated FWD.[2]

To the extent the Board considers the time to trial in the Asustek Action (which does not involve Petitioner), this also does not merit discretionary denial of the Petition. The first amended complaint in the Asustek Action was filed March 7, 2023. *See* Ex. 1011. As of March 2023, the median time to trial in the Eastern

[2] *See* "United States District Courts — National Judicial Caseload Profile," *https://www.uscourts.gov/sites/default/files/data_tables/fcms_na_distprofile0331.2023.pdf* (last accessed October 27, 2023).

District of Texas was 19 months.[3] This would result in a trial occurring in October 2023, which is six (6) months earlier than the expected FWD. However, the Asustek Action is still in the early stages. The parties in that case have not yet exchanged proposed terms for claim construction nor filed *Markman* briefs; the court has not issued a *Markman* order; expert discovery has not begun; and substantial work remains before trial. *See* Ex. 1012. Accordingly, this factor favors institution or is neutral. *RingCentral, Inc. v. Estech Systems, Inc.*, IPR2021-00574, Paper 13 at 11–12 (PTAB Oct. 6, 2021).

C. Factor 3 - Investment in parallel proceedings

This factor favors institution because Petitioner is not involved in the parallel proceedings. In addition, the district court has not issued substantive orders related to the ’634 Patent nor any claim construction orders. Both cases are still in the early stages. In both cases, the court has not issued a *Markman* order; expert discovery has not begun; and substantial work remains before trial. *See* Ex. 1012, 1015. In the AOS Action, a trial date has not been set. Accordingly, this factor weighs favors institution, as the PTAB’s institution can streamline the Asustek Action. *Fintiv*, Paper 15 at 9-12.

---

[3] *See* “United States District Courts — National Judicial Caseload Profile,” *https://www.uscourts.gov/sites/default/files/data_tables/fcms_na_distprofile0331.2023.pdf* (last accessed October 27, 2023).

D. Factor 4 - Overlap between the issues

Petitioner agrees not to pursue invalidity challenges in any district court case based on the same or substantially the same grounds relied upon in this Petition, and so this factor favors institution. Vidal Memorandum at 7-8.

E. Factor 5 - Petitioner is not the defendant in the parallel proceeding

This factor favors institution (or is neutral) because Petitioner is not the defendant in the parallel proceeding and is not an affiliate or subsidiary thereof. *Fintiv*, Paper 15 at 13-14. In addition, Petitioner has agreed not to pursue invalidity challenges in any district court case based on the same or substantially the same grounds relied upon in this Petition.

F. Factor 6 - Merits of Petitioner's challenge

This factor favors institution because the merits are strong, as discussed above. *Fintiv*, Paper 11 at 14–16.

XII. CONCLUSION

For the foregoing reasons, Petitioner respectfully asks that *inter partes* review of the '634 Patent be instituted, and Claims 1-9 of the '634 Patent be found unpatentable and canceled.

Respectfully submitted,

Dated: October 27, 2023

By: *Mackenzie Martin*

Mackenzie Martin
Registration No. 77,950
BAKER & McKENZIE LLP
1900 North Pearl Street, Suite 1500
Dallas, Texas 75201
Tel: (214) 978-3048
Mackenzie.Martin@bakermckenzie.com

Back-up Counsel:

John G. Flaim
Registration No. 37,323
BAKER & McKENZIE LLP
1900 North Pearl Street, Suite 1500
Dallas, Texas 75201
Tel: (214) 978-3097
john.flaim@bakermckenzie.com

Ellen Cheong
Registration No. 71,852
BAKER & McKENZIE LLP
452 Fifth Avenue
New York, NY 10018
Tel: (212) 626-4100
ellen.cheong@bakermckenzie.com

Dorian Ojemen
Registration No. 72,956
BAKER & McKENZIE LLP
800 Capitol, Suite 2100
Houston, Texas 77002
Tel: (713) 427-5032
dorian.ojemen@bakermckenzie.com

DJ Lee
Pro hac vice
BAKER & McKENZIE LLP
1900 North Pearl Street, Suite 1500
Dallas, Texas 75201
Tel: (214) 978-3017
dongjae.lee@bakermckenzie.com

CERTIFICATE OF COMPLIANCE

I hereby certify that this brief complies with the type-volume limitations of 37 C.F.R. § 42.24, because it contains 13,008 words (as determined by the Microsoft Word word-processing system used to prepare the brief), excluding the parts of the brief exempted by 37 C.F.R. § 42.24.

Dated: October 27, 2023

By: *Mackenzie Martin*

Mackenzie Martin
Registration No. 77,950
BAKER & McKENZIE LLP
1900 North Pearl Street, Suite 1500
Dallas, Texas 75201
Tel: (214) 978-3048
Mackenzie.Martin@bakermckenzie.com

CERTIFICATE OF SERVICE

I hereby certify that on October 27, 2023, I caused a true and correct copy of the foregoing materials:

- Petition for *Inter Partes* Review of U.S. Patent No. 7,629,634 under 35 U.S.C. § 311-319 and 37 C.F.R. § 42.100 *Et Seq.*
- Exhibits 1001 – 1015
- Power of Attorney

to be served via:

Email to: jschaefer@baconthomas.com, burcia@baconthomas.com, CHanba@dickinson-wright.com, JJones@dickinson-wright.com

and

FedEx to:

Bacon & Thomas, PLLC
201 N. Union St.
Suite 320
Alexandria, VA 22314
Ref. No. Attorney Docket # HSIE3188 /JS

Dated: October 27, 2023

By: *Mackenzie Martin*
Mackenzie Martin
Registration No. 77,950
BAKER & McKENZIE LLP
1900 North Pearl Street, Suite 1500
Dallas, Texas 75201
Tel: (214) 978-3048
Mackenzie.Martin@bakermckenzie.com