

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Inergy Technology, Inc.,

Petitioner

v.

Force Mos Technology Co., Ltd.,

Patent Owner

Case No. IPR2024-00093

Patent No. 7,629,634

DECLARATION OF DAVID KUAN-YU LIU, Ph.D.

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I, Dr. David Liu, declare and state as follows:

I. INTRODUCTION

1. I have been retained by Inergy Technology, Inc. (“Inergy” or “Petitioner”) as an independent expert in this *inter partes* review before the Patent Trial and Appeal Board (“PTAB”) of the United State Patent and Trademark Office. I am not an employee of Inergy or of any affiliate or subsidiary of Inergy.

2. I have been engaged to provide my opinions as to whether certain references disclose, teach, or suggest the features cited in the claims of U.S. Patent No. 7,629,634 (the “’634 Patent”) and whether the claims of the ’634 Patent are unpatentable as anticipated or obvious.

3. I am being compensated at \$550.00 per hour for non-testifying work and \$600.00 per hour for testifying work, including reimbursement for reasonable and necessary out-of-pocket expenses incurred in connection to my engagement. My compensation is based solely on the amount of time that I devote to this proceeding and is in no way contingent on the nature of my findings, the presentation of my findings in testimony, or the outcome of this or any other proceeding. I have no other financial interest in this proceeding.

4. My opinion and the bases for my opinions are set forth below.

II. EDUCATIONAL BACKGROUND, PROFESSIONAL EXPERIENCE, AND OTHER QUALIFICATIONS

5. I have personal knowledge or have developed knowledge of these technologies based upon education, training, or experience, of the matters set forth herein.

6. My curriculum vitae (“CV”) is attached hereto as Exhibit 1004 and provides an accurate identification of my background and experience. Among other things, my CV includes a list of my issued patents and publications for at least the last 30 years. My curriculum vitae also includes information about my expert witness experience, with case numbers where available. Below is a short summary of my professional qualifications:

7. I received a Bachelor of Science in Electrical Engineering from the University of California, Berkeley, in 1983. I received a Master of Science and Ph.D. degrees in Electrical Engineering from Stanford University in 1985 and 1989, respectively.

8. I worked on a novel Conductivity Modulated Power MOSFET for my Ph.D. thesis. The novel device uses a trench injector to facilitate an optimal tradeoff between the breakdown voltage and ON-Resistance of a Power MOSFET (Vertical DMOS) through the use of a minority carrier injector.

9. From 1989 to 1992, I was a member of technical staff at Texas Instruments, Inc. At Texas Instruments, my job responsibilities included process

integration, device modeling, high-voltage CMOS process integration, and investigating novel source-side injection mechanisms for Flash EPROM channel hot-electron programming.

10. From 1992 to 1995, I was a member of the technical staff at Advanced Micro Devices, Inc. (AMD) where I was a key contributor in optimizing Flash cell and periphery devices in AMD's CMOS-based 0.5 μm and 0.35 μm Flash EPROM technology. My job responsibilities at AMD also included process integration, device modeling, and development of triple-well process technology for accommodate x-decoder transistors and high voltage transistors for negative gate erase operation. While at AMD, I was awarded a Spotlight Award for developing a method of manufacturing a self-aligned source (SAS) etch for a NOR flash memory.

11. I spent the next five years of my career in managerial and director roles at several California-based semiconductor companies. I was responsible for increasing yield and for leading teams of engineers working to develop next-generation memory devices.

12. In 2000, I co-founded Progressant Technologies in Fremont, California. Progressant Technologies developed IP for negative differential resistance transistor technology and was eventually acquired by Synopsys, Inc.

13. From 2000 to 2004, I was a Senior Manager at Xilinx, Incorporated, where I was responsible for developing nonvolatile memory process technology for flash and CPLD product applications, as well as advanced CMOS process technology (specifically 75 nm CMOS technology node, a half node version between 90 nm and 65 nm).

14. From 2004 to 2007, I was a Senior Scientist at Maxim Integrated Products where I was responsible for developing Embedded Non-volatile Memory process technology for Power Management product applications.

15. Since 2007, I have served as a technical consultant where I have provided expert advice regarding Flash memory technology, CMOS process technology, and semiconductor device physics.

16. I am not now, and have never been an employee of the Petitioner.

III. DOCUMENTS AND REFERENCES CONSIDERED

17. I have reviewed and considered the following documents:

Exhibit No.	Citation
1001	U.S. Patent No. 7,629,634 (the “’634 Patent”)
1002	File History of the ’634 Patent
1005	German Patent Publication No. DE 102004009083 (“Hirler”)
1006	Certified English Translation - German Patent Pub. No. DE 102004009083 (“Hirler”)

Exhibit No.	Citation
1007	Affidavit of Translation - Hirler
1008	U.S. Patent Publication No. 2004/0021174 (“Kobayashi”)
1009	U.S. Patent Publication No. 2005/0029584 (“Shiraishi”)
1010	Complaint, <i>Force Mos Technology, Co. Ltd. v. Asustek Computer, Inc.</i> , No. 2:22-cv-00460 (E.D. Tex.)
1011	First Amended Complaint, <i>Force Mos Technology, Co. Ltd. v. Asustek Computer, Inc.</i> , No. 2:22-cv-00460 (E.D. Tex.), ECF 13

IV. APPLICABLE LEGAL STANDARDS

18. I am not an attorney, but I have been instructed in and applied the law as described in this section.

19. It has been explained to me that a claim must be properly construed in order to be compared to prior art. My opinion regarding how a POSITA would have understood the claims of the ’634 Patent are below in Section IX.

20. It has been explained to me that a claim is anticipated under pre-AIA Section 102(b) if a prior art reference discloses each and every element of the claim, either explicitly or inherently. I understand that while the disclosed claim elements must be arranged or combined in the same way as the claim, the reference need not use the same terms to describe these claims.

21. It has also been explained to me that a claim is unpatentable for obviousness if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art.

22. I understand that the standard for determining obviousness is based on an analysis of several factual inquiries, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) when available, evidence such as commercial success, long-felt but unsolved needs, and failure of others.

23. I understand that several rationales and principles may be employed to show obviousness, including the following: (1) if a work is available in one field of endeavor, and design incentives and other market forces can prompt variations of it (either in the same field or a different one), and a person of ordinary skill can implement a predictable variation, the variation is obvious; (2) if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its application is beyond his or her skill; (3) the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results; (4) if the improvement

is nothing more than the predictable use of prior art elements according to their established functions, it is likely obvious, among others.

24. I also understand that when looking into interrelated teachings of multiple references, there must be a motivation to combine for the POSITA to combine the prior art references to arrive at the claimed subject matter.

25. I understand that considerations to determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent-at-issue include the effects of demands known to the design community or present in the marketplace and the background knowledge possessed by a person having ordinary skill in the art.

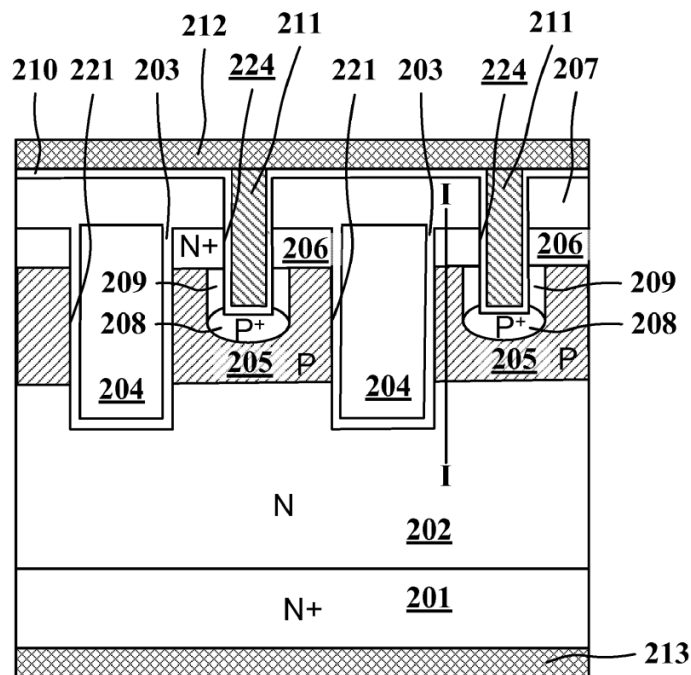
V. THE '634 PATENT

A. The '634 Patent

26. The '634 Patent is directed to trenching Metal-Oxide-Semiconductor Field Effect Transistor ("MOSFET"), a type of semiconductor structure that is used to significantly reduce the surface area occupied by the channel of the transistor on the silicon, which in turn reduces the ON-resistance of the device for a given device area. This type of semiconductor structure was well-known in the art and to the POSITA at the time of the filing date of the '634 Patent (February 23, 2008). Ex. 1001 at 1:5-9.

27. The '634 patent addresses the issue of poor ohmic contact on the sidewall of the trenched source contact to the body region due to poorly engineered doping concentration profile. Ex. 1001 at 1:35-45.

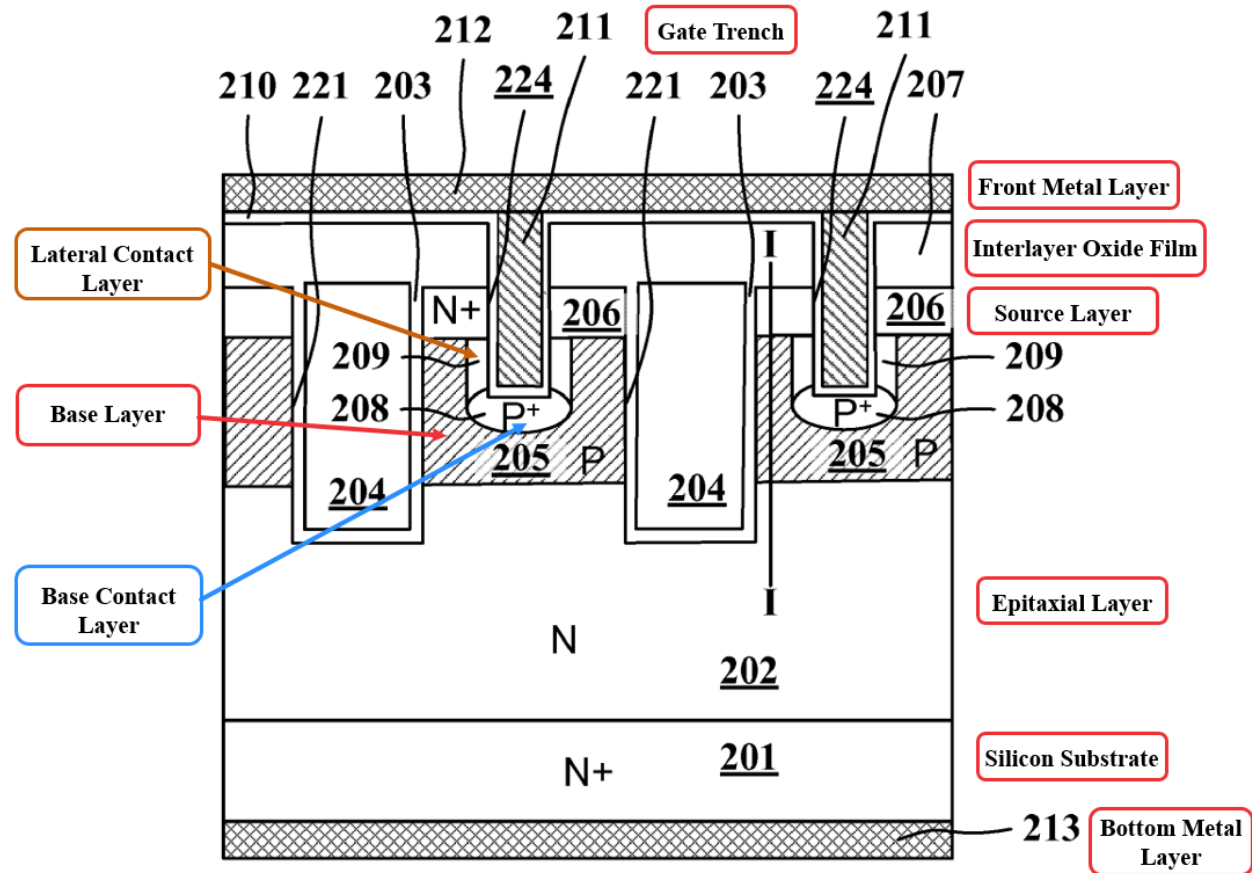
28. The '634 Patent, in particular, is directed to “a lateral contact layer” along the sidewalls within the base layer (205) of the source contact trenches. Ex. 1001 at 1:5-9, 1:66-67, 2:23-26, 3:50-4:6, Fig. 2G. The lateral contact layer described in the '634 Patent is shown below in the '634 Patent's Figure 2G as 209. Ex. 1001 at Fig. 2G, 3:50-4:6.



'634 Patent, Figure 2G

29. The '634 Patent describes the lateral contact layer (209) as being doped to P*-type, the base contact layer (208) at the bottom of the source contact trench is P+-type, and the body of the MOSFET (205) is P-type. Ex. 1001 at 3:50-

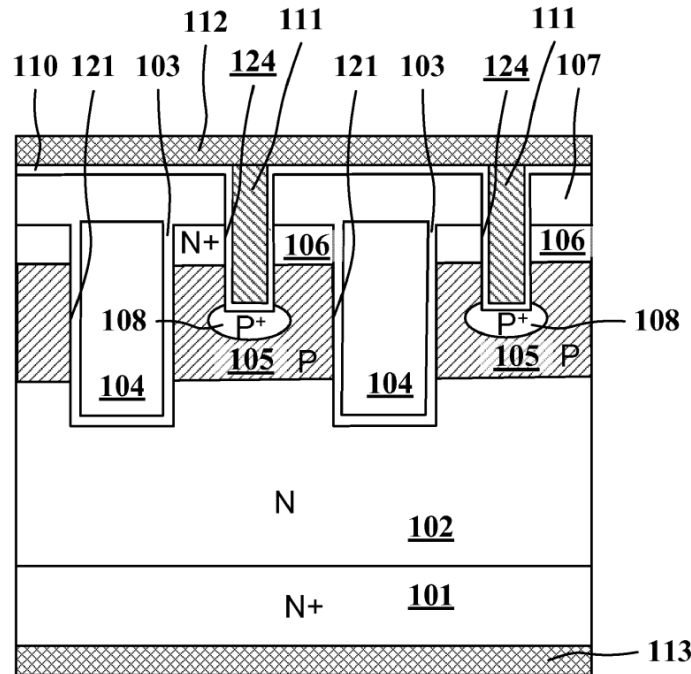
less than P^+ . *Id.*



'634 Patent, Figure 2G (annotations added)

30. The '634 Patent also discloses that a trenched MOSFET with near-identical structure already existed in the prior art as of the effective filing date, including the claimed drain region, a body region, a source regions, front metal layer, interlayer oxide film, bottom metal layer, trenched gates formed on top of the source layer and extending down through the base layer to a portion of the epitaxial layer, and source contact trenches formed on top of the source layer and

extending down through the source layer to a portion of the base layer with a heavily doped base layer at the bottom of the trench. Ex. 1001 at 1:5-9, 1:18-41, Fig. 1 (Prior Art). Figure 1 depicting the prior art as admitted by the '634 Patent is shown below.



'634 Patent, Figure 1 (Prior Art)

B. The '634 Patent File History

31. I understand that U.S. Patent Application No. 12/036,243 (the “’243 Application”), titled “TRENCHED MOSFET WITH TRENCHED SOURCE CONTACT,” was filed on February 23, 2008, and issued as the ’634 Patent on December 08, 2009. Ex. 1001 at 1 (Cover); Ex. 1002 at 48-86. I also understand that, on July 15, 2009, a telephonic examiner-initiated interview took place, where the examiner and the applicant discussed the lateral contact layer “covering [the]

entire trench sidewall[,]" the prior art, and claim language. Ex. 1002 at 27. On July 28, 2009 the examiner issued a Notice of Allowance and Fees Due on Claims 1-9 with examiner amendments to Claim 1, and the following Reasons for Allowance: "Claim 1 limits the trenched MOSFET to having a trench in which the base and entire sidewall are covered with the lateral contact layer. Kobayashi (US 6,888,196) covers the base and only a portion of the trench sidewall with the lateral contact layer." *Id.* at 23-26.

VI. STATE OF THE ART

32. At the effective filing date of the '634 Patent, February 23, 2008, a POSITA would have known that the development of MOSFETs, and specifically Power MOSFETs, focuses on the tradeoff between minimizing the ON-Resistance and maximizing the breakdown voltage capability, for a given device area.

33. The key evolutionary advancement of the MOSFET involves going from a planar DMOS (Double-Diffused MOS) to a trench MOSFET, where the gate and its associated channel of the transistor is folded vertically onto a trench into the silicon. While the use of a trench Power MOSFET reduces the ON-Resistance significantly through the reduction of the junction FET component, the dopant profile optimization of the body region and the drift region continues to be the key feature in this optimization effort.

34. However, even for well-designed doping profiles in the drift region (N-region) and the body region (P-region) in an N-channel MOSFET that minimizes the channel resistance (R_{ch}) and achieves a target avalanche breakdown voltage strength, the breakdown voltage capability could nonetheless be degraded due to the phenomena of punch-through of the body region between the drain and the source.

35. This punch-through could come from the presence of a resistive contact of the body region to the source region. Any current that is generated from the reverse biased P-N junction (the junction between drift region and the body region) can trigger the lowering of the barrier between the drain and source of the transistor in the off-state, and causes premature breakdown or conduction of the device even before the target avalanche breakdown voltage is reached.

36. Thus, while most of the work in the field at this time focused on optimizing the doping profiles of the body region and the drift region, a significant portion of these efforts also focused on the doping profile around the source/body contact in order to generate a low resistive ohmic contact to connect both the N⁺ source and the P- body of the transistor.

37. With the further evolution of using a trenched source contact to contact both the source region and the P body region, the doping profiles of the body surrounding both the sides and the bottom of the trench have significant

impact on the resistivity of the ohmic contacts required to connect both the source and the body.

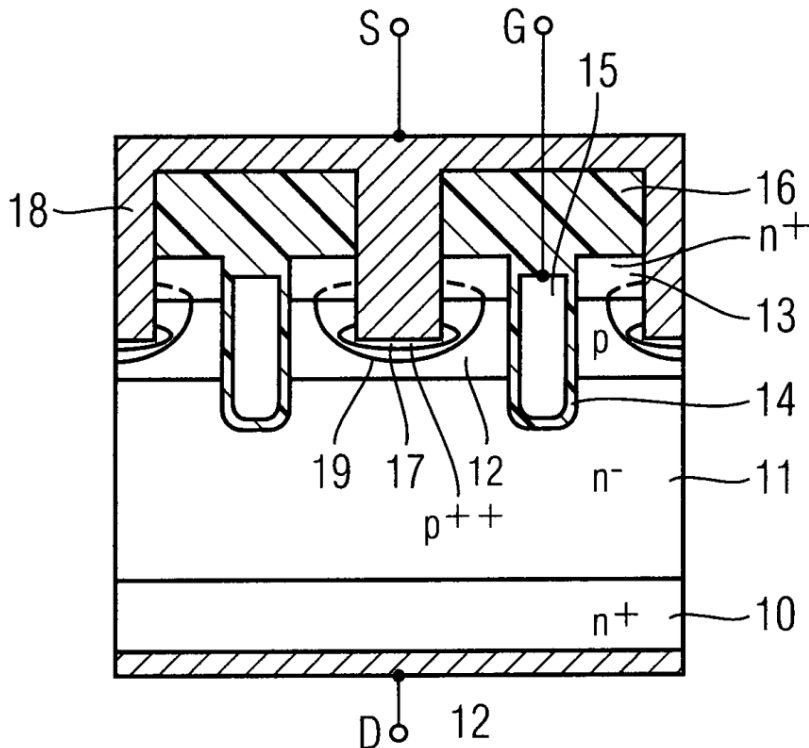
VII. OVERVIEW OF THE PRIOR ART

A. German Patent Publication DE 102004009083 (“Hirler”)

38. I understand that Hirler was filed on February 25, 2004, and published on September 22, 2005. Exs. 1005-1007. It has been explained to me that Hirler is prior art to the '634 Patent at least under pre-AIA 35 U.S.C. § 102(b), because it was publically available more than one year before the earliest priority date of the '634 Patent.

39. Hirler teaches the arrangement of a vertical MOS power transistor with a tailored body zone (base) that has a contact zone at the bottom of the contact trench with a higher doping concentration than that of the body zone (base). Hirler discloses the source contact trenches having a “body amplification zone” or “body enhancement zone” (19) along the sidewalls of the source contact trenches along with an additional “body contact zone” (17) at the bottom of the source contact trench. Ex. 1005 at Fig. 2F; Ex. 1006 at [0013], [0030], Claim 1.

40. Hirler Figure 2F is included below for reference.



Hirler, Figure 2F

41. Hirler discloses that the doping concentration of the body amplification zone (19) is larger than the doping concentration of the body zone (12) but smaller than the doping concentration of the body contact zone (17).

Ex. 1006 at [0009], [0031], Claim 2.

42. Hirler discloses that the body amplification zone allows “avalanche breakdown [to] be clamped between the transistor structures to achieve high dielectric strength while saving space without precisely defining the depth of the body contact zone.” Ex. 1006 at [0007]-[0008]. Based on this alone, the POSITA would understand that a lateral contact layer along the sidewalls of the source

contact trench was beneficial in achieving the designed avalanche breakdown target.

43. Avalanche breakdown occurs at a junction formed by layers of opposite doping polarity (for example, a P-N junction). Under a reverse bias voltage between a P-N junction, the voltage is translated into an electric field that is spread across the depletion region between the junction, with the integration of the electric field across the depletion region being the voltage. The extent of the depletion region, and thus how quickly the electric field builds up, is a function of the doping profile of the P-N junction. A higher doping profile will result in a higher electric field across a shorter distance. It is this high electric field that causes a leakage current of the reverse biased P-N junction.

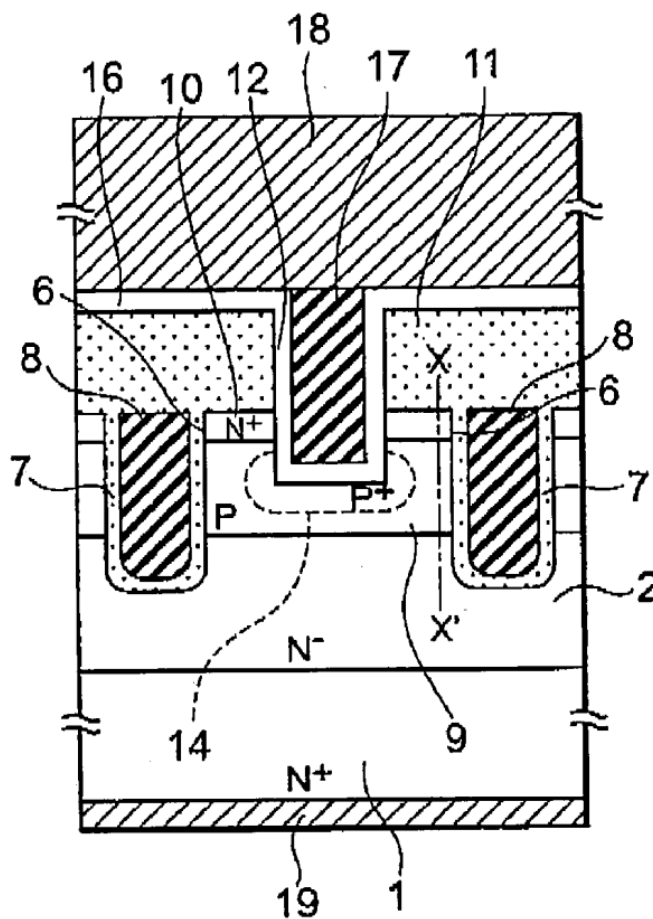
44. Once the peak electric field is built up to a critical level, the electrons and holes will go into an uncontrolled impact ionization process where additional electrons and holes are generated and multiplied by the electric field. This leads to the breakdown or runaway current at the junction.

45. Hirler discloses that the specified conductivity types can be reversed and interchanged between n- to p-type to create N-channel or P-channel MOSFET. Ex. 1006 at [0001], [0005], [0028].

B. U.S. Patent Publication No. 2004/0021174 (“Kobayashi”)

46. I understand Kobayashi was published on February 5, 2004. Ex. 1008 at cover. It has been explained to me that Kobayashi is prior art at least under pre-AIA 35 U.S.C. § 102(b), because it was publically available more than one year before the earliest priority date of the '634 Patent.

47. A view of Kobayashi's Figure 5A included below for reference.



Kobayashi, Figure 5A

48. Kobayashi discloses a trenched vertical MOSFET with source contact trenches with a p⁺-type base contact layer at the bottom of the trench. Ex. 1008 at cover, Fig. 10, [0018].

49. In Figure 5A, Kobayashi discloses:

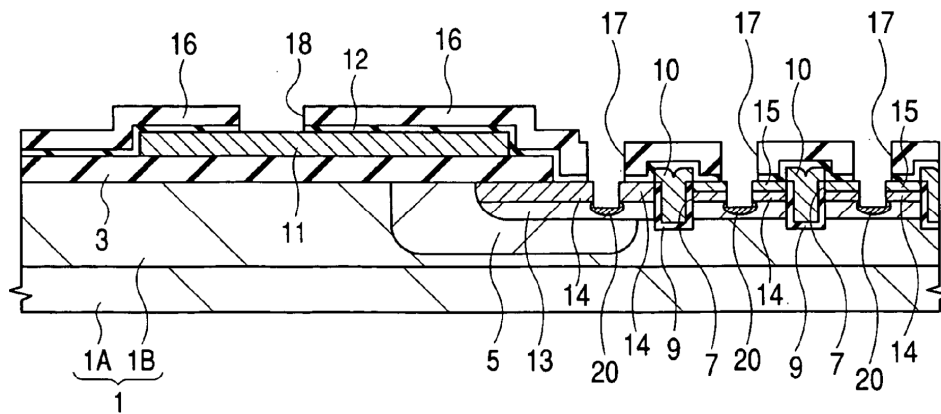
an N⁺-type silicon substrate **1** and an N⁻-type epitaxial layer **2** formed on one surface of the N⁺-type silicon substrate **1**. A P-type base layer **9** and an N⁺-type source layer **10** are formed on a surface of the N⁻-type epitaxial layer **2**. . . . In each of trenches **6** reaching the N⁻-type epitaxial layer **2** through the P-type base layer **9**, a gate oxide film **7** and a polysilicon **8** are filled. On the polysilicon **8** to serve as a gate electrode or a trench gate, an interlayer oxide film **11** is formed. Between the trench gates adjacent to each other, a contact hole **12** having a predetermined depth is formed to reach the P-type base layer **9** though the N⁺-type source layer **10**. Directly under the contact hole **12**, a barrier metal **16** is deposited to extend onto the interlayer oxide film **11**. The contact hole **12**, within which the barrier metal **16** is formed, is filled with W **17**. On the surface of the W **17** and the barrier metal **16**, a source electrode **18** is formed. On the other surface, of the N⁺-type silicon substrate **1**, a drain electrode **19** is formed.

Ex. 1008 at [0052].

50. Kobayashi also discloses “a base contact layer **14** under the bottom of the contact hole **12**.” Ex. 1008 at Fig. 5A, [0061], Claim 1 (“. . . a base contact layer **14** formed within said base layer so as to enclose a bottom of said contact and to bring said base contact layer into contact with the bottom of said contact.”), Claim 3 (“. . . said base contact layer is formed within said base layer so as to enclose only the bottom of said contact and to bring said base contact layer into contact with only the bottom of said contact.”).

C. **U.S. Patent Publication No. 2005/0029584 (“Shiraishi”)**

52. I understand Shiraishi was published on February 10, 2005. Ex. 1009 at cover. It was explained to me that Shiraishi is prior art at least under pre-AIA 35 U.S.C. § 102(b), because it was publically available more than one year before the earliest priority date of the ’634 Patent. Shiraishi’s Figure 8 is included below for reference.



53. Shiraishi discloses tailoring the doping profile in the base region of the Vertical Power MOSFET. Tailoring the doping profile will affect the doping profile at the sidewalls within the base region of the source contact trenches.

Shiraishi discloses a power Metal Insulator Semiconductor Field Effect Transistor

(“MISFET”) with source contact trenches with a p⁺-type base contact layer at the bottom of the trench. Ex. 1009 at Abstract, Fig. 8, [0075].

54. The POSITA would understand that a MISFET is interchangeable with the term MOSFET. Specifically, a MOSFET (Metal-Oxide-Semiconductor FET) is a type of MISFET (Metal-Insulator-Semiconductor FET) wherein the insulator is an oxide.

55. In addition, Shiraishi also discloses an additional p-type semiconductor layer below the source layer and at the sidewalls of the source contact trench. Ex. 1009 at Fig. 8, [0073], [0084]. Shiraishi explains that this region can be doped such that the impurity doping concentration is less than that of the disclosed p⁺ base contact layer but higher than the p-type body. Ex. 1009 at [0075].

56. In addition, Shiraishi discloses that the additional p-type semiconductor region serves as a “punch-through stopper layer” for the power MISFET. Ex. 1009 at [0073], [0080], [0085]. The additional p-type semiconductor region allows for reduction of base resistance of a parasitic npn bipolar transistor and for enhancement of avalanche yield strength. Ex. 1009 at [0084].

VIII. THE QUALIFICATIONS AND BACKGROUND OF THE PERSON OF ORDINARY SKILL IN THE ART

57. A person of ordinary skill in the art of the subject matter of the '634 Patent at the alleged effective filing date of the invention of the '634 Patent (February 23, 2008) ("POSITA") would have earned a Master's degree in electrical engineering, and at least two years of relevant work experience in the field of integrated circuit design and manufacturing.

IX. CLAIM CONSTRUCTION

58. I understand claim terms are generally given their ordinary and customary meaning that the term would have to a person of ordinary skill in the art.

59. I also understand that the court looks to public sources that show what a person of skill in the art would have understood disputed claim language to mean. I understand those sources include the "intrinsic evidence", *i.e.*, the patent itself, including the claims, the specification and, if in evidence, the prosecution history.

60. The '634 Patent explains the admitted prior art as providing a MOSFET where "the P⁺-type region is located *only* at source contact trench bottom." Ex. 1001 at 1:33-35, Fig. 1(Prior Art) (emphasis added). In contrast, the '634 Patent describes the invention as a MOSFET with distinct base contact and lateral contact layers, wherein the base contact layer covers the bottom of the source contact trench and the lateral contact layer covers the entirety of the

remaining sidewalls of the trench in the base layer. *E.g.*, Ex. 1001 at 1:43-45 (“The present invention provides a new structure of trenched MOSFET structure with a trenched source contact which improves the lack of the prior art.”), Fig. 2G. The ’634 Patent states that “[t]he P+-type base layer (208) and the P*-type lateral contact layer (209) are formed at the bottom and sidewall of the source contact trenches (224) respectively.” Ex. 1001 at 5:9-12. Further, the ’634 Patent figures depict the lateral contact layer and base contact layer as separate layers and provides two, separate implantation methods for forming the bottom base contact layer in addition to the lateral contact layer. Ex. 1001 at 3:50-4:6, Figs. 3A and 3B. The base contact layer in the ’634 Patent is created with a 90° implantation angle respective to the epitaxial layer while the lateral contact layer is created with a 45° to 80° implantation angle. *Id.*

61. I understand the examiner distinguished Kobayashi on the basis that the “entire” sidewall of the source contact trench in the base layer was covered by the lateral contact layer in the ’634 Patent, as opposed to only being partially covered as in Kobayashi. Ex. 1002 at 29.

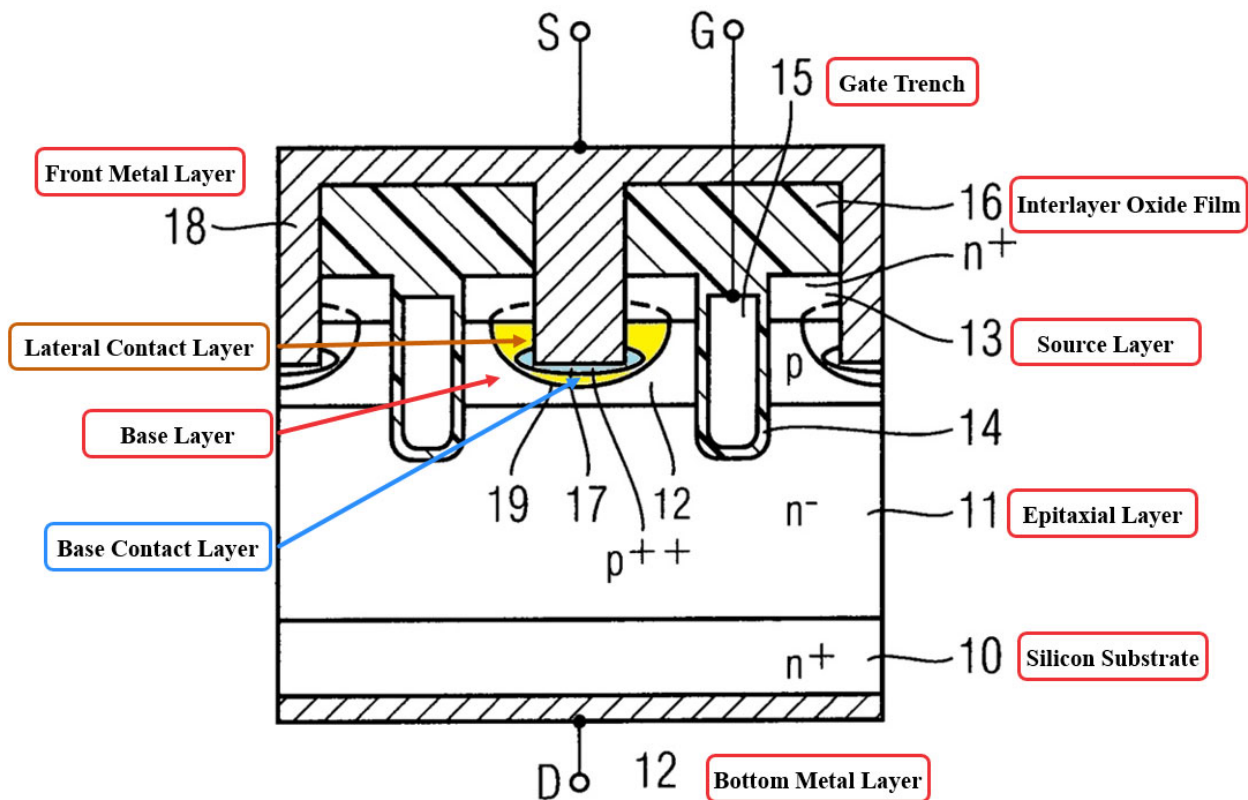
62. Based on the specification and file history, the POSITA would construe “the sidewalls of said trenches in said base layer” to mean “entire sidewalls of said trenches in said base layer.”

X. OPINIONS AS TO INVALIDITY OF THE '634 PATENT

A. Claims 1, 2 and 6 are unpatentable under pre-AIA 35 U.S.C. § 102(b) as anticipated by Hirler

1. Claim 1 is anticipated by Hirler

63. As I further explain below, every element of Claim 1 is disclosed in Figure 2F, as annotated below:



Hirler, Figure 2F (with annotation)

a. Claim 1[preamble]: “A **trenched MOSFET with trenched source contact, comprising:**”

64. The preamble of Claim 1 is disclosed in Hirler, which discloses a trenched MOSFET with source contact trenches. Ex. 1006 at [0001] (“The present invention relates to a MOS power transistor arrangement having a vertical

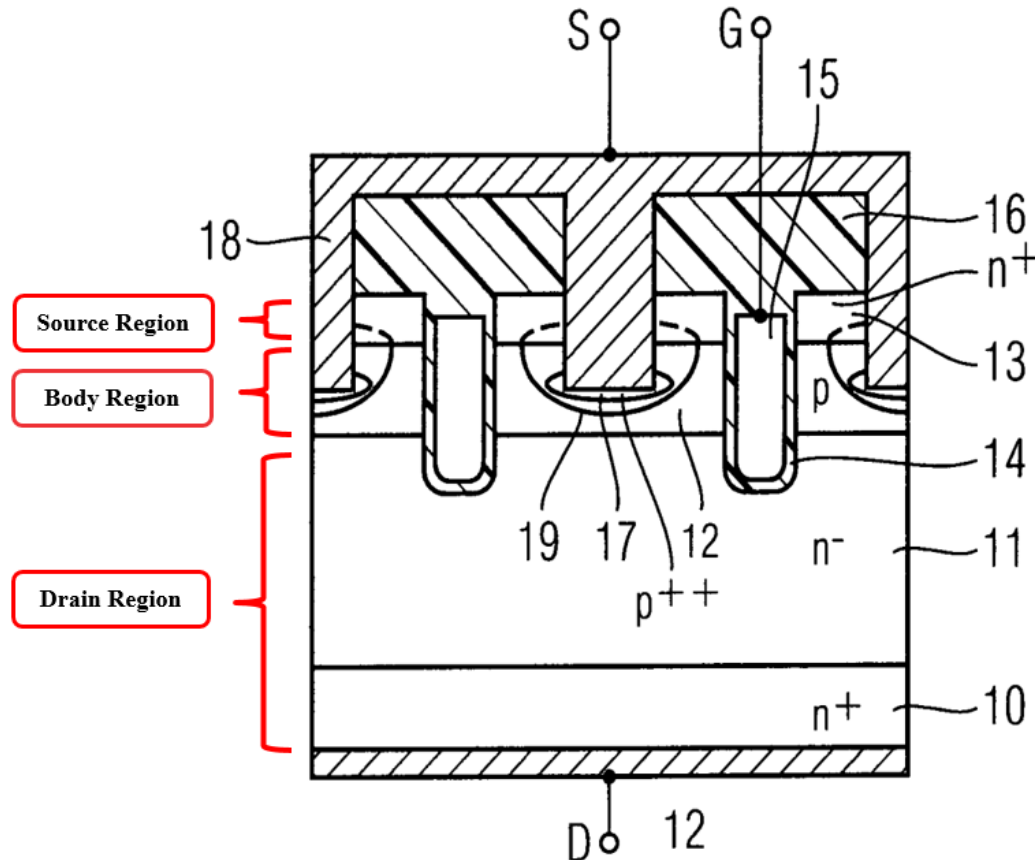
transistor structure . . . wherein the body zone has a contact zone at the base of a contact trench . . .”), Cover Summary; Ex. 1005 at Fig. 2F. A POSITA would understand that a “contact trench” as disclosed in Hirler, is a source contact trench, as it is a trench that extends through the source region and into the body region.

- b. 1[a]: “a semiconductor region having a drain region, a body region and a source region, comprising, [1] a silicon substrate, [2] an epitaxial layer corresponding to said drain region disposed on the top of said silicon substrate, [3] a base layer corresponding to said body region disposed on the top of said epitaxial layer, and [4] a source layer corresponding to said source region disposed on the top of said base layer;”**

65. This claim element is disclosed in Hirler. Hirler describes a vertical trenched MOSFET with a drain region, body region, and source region—features that a POSITA would know are universal to all MOSFETs. Ex. 1005 at Fig. 2F; Ex. 1006 at [0001].

66. Specifically, Hirler discloses “The starting point is an n+ substrate **10** of silicon, an n- drift zone **11**, p-body zone areas **12** as well as n+ source zone areas **13**.” Ex. 1006 at [0018], [0001]; Ex. 1005 at Fig. 1A, Fig. 2F. The POSITA would understand that Hirler’s Figure 2F (copied below with color annotations) shows a MOSFET with the drain region oriented at the bottom of the figure and layered as claimed, wherein (1) the “n+ substrate **10** of silicon” corresponds with “a silicon substrate,” (2) the “n- drift zone **11**” corresponds with “an epitaxial layer corresponding with a drain region,” (3) the “p-body zone areas **12**” corresponds

with “a base layer corresponding to a said body region,” and (4) “n+ source zone areas 13” corresponds with “a source layer corresponding to said source region” as provided in Claim 1 of the '634 Patent. Ex. 1006 at [0018]; Ex. 1005 at Fig. 1A, Fig. 2F.



Hirler, Figure 2F (annotated in regards to Claim Element 1[a] of Claim 1)

- c. 1[b]: “a front metal layer formed on the upper surface of said semiconductor region”

67. Hirler discloses a metal layer (18) that is positioned on the upper surface of the MOSFET to form a source connection. Ex. 1005 at Fig. 2F;

Ex. 1006 at [0022] (“The metallization **18** forms a source connection S.”). This is a feature that is well-known in the art and to the POSITA.

d. 1[c]: “an interlayer oxide film formed between said source layer and said front metal layer”

68. Hirler discloses a silicon oxide layer (16) formed between the source layer (13) and the metal layer (18). Ex. 1005 at Fig. 2F, Fig. 1A; Ex. 1006 at [0018] (“The silicon oxide layer **16** covers the entire structure”). The POSITA would understand that the “silicon oxide layer **16**” corresponds to an interlayer oxide film. This is a feature that is well-known in the art and to the POSITA.

e. 1[d]: “a bottom metal layer formed on the lower surface of said semiconductor region;”

69. Hirler discloses a metal layer (12) that is positioned on the bottom surface of the MOSFET to form a drain connection, *e.g.*, marked “D” in Figure 2F. Ex. 1005 at Fig. 2F; Ex. 1006 at [0022] (“an unspecified metallization of, for example, aluminum is applied, which forms a drain connection D.”). This is a feature that is well-known in the art and to the POSITA.

70. Notably, in Figure 2F, this bottom metal layer is mislabeled as (12). Specifically, both the body region and the bottom metal layer are labeled as (12) in Figure 2F. A POSITA would understand from the description and from Figure 1A that (12) refers to the body region, which would not be located at the drain connection. Ex. 1006 at [0022] (referring to the bottom metal layer as an

“unspecified” metallization layer), [0018] (referring to the p-body zone areas as (12) in Fig. 1A); Ex. 1005 at Fig. 1A, Fig. 2F.

- f. 1[e]: “a plurality of trenched gates covered by said interlayer oxide film are formed on top of said source layer extending downwardly through said base layer to a portion of said epitaxial layer; and”**

71. Element 1[e] is disclosed in Hirler. Hirler discloses a plurality of gate trenches (14, 15), annotated as “G”, which are covered by the silicon oxide layer, begin above the source layer, and extend down through the body layer and into the epitaxial, drift layer. Ex. 1005 at Fig. 2F; Ex. 1006 at [0018] (“The trench gates with a gate oxide **14** and a gate electrode **15** extend through the source zone areas **13** and the body zone **12** into the drift zone **11**.”). This is a feature that is well-known in the art and to the POSITA.

- g. 1[f]: “a plurality of source contact trenches formed on the top of said interlayer oxide film extending downwardly through said source layer to a portion of said base layer”**

72. Element 1[f] is disclosed in Hirler. Hirler discloses a plurality of source contact trenches that are formed on top of the silicon oxide layer and “penetrat[e] through the source zones areas **13** to the body zone areas **12**” Ex. 1006 at [0020], [0019]; Ex. 1005 at Fig. 2F. This is a feature that is well-known in the art and to the POSITA.

h. 1[g]: “wherein the sidewalls of said trenches in said base layer are covered by the lateral contact layer;”

73. Element 1[g] is disclosed by Hirler. Specifically, Hirler discloses “body amplification zones” (19) that are implanted along the sidewalls of the contact trench in the base layer. Ex. 1005 at Fig. 2F; Ex. 1006 at [0030], [0033]. The POSITA would understand that the “body amplification zone” or “body enhancement zone” disclosed in Hirler is the “lateral contact layer” in the ’634 Patent. Not only is the body amplification zone located in the same position along the sidewalls of the contact trench, the purpose of the body amplification zone is the same as the lateral contact layer—*i.e.*, to achieve the intended avalanche breakdown voltage capability, without it being degraded through the turning on of the NPN parasitic bipolar transistor. Ex. 1006 at [0007]-[0008]; Ex. 1001 at 1:35-42, 2:23-33.

i. 1[h]: “wherein the bottom base of said trenches in said base layer are covered by the base contact layer.”

74. Element 1[h] is disclosed in Hirler. Specifically, Hirler discloses a P++ type “body contact zone 17” at the bottom of the contact trench. Ex. 1005 at Fig. 2F, Fig. 1D; Ex. 1006 at [0021]. The POSITA would understand that the “body contact zone” disclosed in Hirler is the “base layer” as described in the ’634 Patent. This is a feature that is well-known in the art and to the POSITA.

2. Claim 2 is anticipated by Hirler

- a. 2[a]: “The trench MOSFET of claim 1, wherein the silicon substrate, the epitaxial layer, and the source layer are N-type;”**

75. Claim 2 depends on Claim 1, which is disclosed in Hirler, as discussed above in Section X(A)(1). Element 2[a] is disclosed in Hirler. As shown in Figure 2F above, *supra* ¶ 63, Hirler discloses a trench MOSFET, wherein the conductivity type of the silicon substrate, the epitaxial layer, and the source layer are N-type. Ex. 1005 at Fig. 2F; Ex. 1006 at [0018]. These are features of an N-channel MOSFET that are well-known in the art and to the POSITA.

- b. 2[b] “the base layer and lateral contact layer are P-type;”**

76. Element 2[b] is disclosed in Hirler. As shown in Figure 2F above, *supra* ¶ 63, Hirler discloses a trench MOSFET, wherein the conductivity type of the body layer is P-type. Ex. 1005 at Fig. 2F; Ex. 1006 at [0018]. This feature of an N-channel MOSFET is well-known in the art and to the POSITA. In addition, Hirler discloses that the conductivity type of the body amplification layer (the lateral contact layer) is also p-type—*i.e.*, p+. Ex. 1006 at [0030].

- c. 2[c] “and each of the source contact trenches further has a P-type base contact layer at a bottom thereof, and the lateral contact layer has less doping concentration than the base contact layer at bottom.”**

77. Element 2[c] is disclosed in Hirler. As shown in Figure 2F above, *supra* ¶ 63, Hirler discloses a trench MOSFET wherein the body contact layer

(the base contact layer) is P-type—*i.e.*, p⁺⁺. Ex. 1005 at Fig. 2F; Ex. 1006 at [0018]. In addition, Hirler discloses that the doping concentration of the body amplification zone is larger than the doping concentration of the body zone and smaller than the doping concentration of the body contact zone. Ex. 1006 at [0009], [0031], Claim 2. The POSITA would clearly understand this disclosure to mean that the layer at the bottom of the contact trench has a higher doping concentration of P-type than the layer at the sidewalls of the trench, which is higher than the doping concentration of the body region.

3. Claim 6 is anticipated by Hirler

- a. “The trench MOSFET of claim 1, wherein the silicon substrate, the epitaxial layer, and the source layer are P-type; the base layer and lateral contact layer are N-type; and each of the source contact trenches further has a N-type base contact layer at a bottom thereof, and the lateral contact layer has less doping concentration than the base contact layer at bottom.”**

78. Claim 6 depends on Claim 1, which is disclosed in Hirler, as discussed above in Section X(A)(1). The remaining elements of Claim 6 are disclosed in Hirler, which introduces a MOSFET with layers of either N- or P-type conductivity: “The present invention relates to a MOS power transistor arrangement having a vertical transistor structure in which a drift zone of the first conductivity type [*e.g.*, P-type] and a body zone of a second conductivity type opposite to the first conductivity type [*e.g.*, N-type] and a source zone of the first

conductivity type [e.g., P-type] are successively provided on a semiconductor substrate of a first conductivity type [e.g., P-type], and in which a trench gate extends through the source zone and the body zone into the drift zone, wherein the body zone has a contact zone at the base of a contact trench with a high doping concentration compared with the doping concentration of the body zone [e.g., N-type].” Ex. 1006 at [0001]. The POSITA would understand that the conductivity type options were limited to P-type and N-type, and that Hirler disclosed a trench MOSFET whether the first conductivity type could be P-type or N-type.

79. Further, Hirler specifies an embodiment in prior art where “a trench MOS power transistor in which a p-type layer [*sic*], an n⁺ type body amplification zone [*i.e.*, lateral contact layer], an n-type body region and an n⁺⁺ type body contact zone [*i.e.*, base contact layer] are provided on the edge of a gate trench, one above the other from the base of the trench.” Ex. 1006 at [0005]. The POSITA would understand this to disclose a P-channel MOSFET, where source and drain regions would be P-type and the body region would be N-type.

80. It would be clear to a POSITA that a MOSFET with an N-type first conductivity would correspond to an N-channel MOSFET; whereas a MOSFET with a P-type first conductivity would correspond to a P-channel MOSFET.

B. Claims 3-5 and 7-9 are unpatentable under pre-AIA 35 U.S.C. § 103(a) as obvious over Hirler in light of Kobayashi and the knowledge of the POSITA

- 1. Claim 3 is obvious over Hirler in light of Kobayashi and the knowledge of the POSITA**
 - a. 3: “The trenched MOSFET of Claim 2, wherein further comprises a barrier metal layer and a plurality of contact metal plugs.”**

81. Claim 3 depends on Claim 2, which is disclosed in Hirler, as discussed above in Section X(A)(2). The remaining elements of Claim 3 are disclosed in Hirler, Kobayashi and knowledge of the POSITA. Hirler discloses that the source contact trenches can be “filled with a conductive stopper”—*i.e.*, contact metal plugs. Ex. 1006 at [0023]. The use of a barrier metal layer is generally known to the POSITA. Moreover, Kobayashi discloses the use of a barrier metal layer deposited in the contact trenches and atop the interlayer oxide layer. Ex. 1008 at Fig. 6A, [0052]-[0053], [0062].

82. Further, a POSITA would know that the deposition of CVD tungsten is typically preceded by the usage of a barrier metal layer. This barrier metal layer acts as diffusion barrier to prevent unwanted interaction between the CVD W and the underlying silicon.

2. Claim 4 is obvious over Hirler in light of Kobayashi and the knowledge of the POSITA

a. 4: “The trench MOSFET of Claim 3, wherein the barrier metal layer is Ti/TiN and the contact metal plug is Tungsten.”

83. Claim 4 depends on Claim 3, which is discussed above in Section X(B)(1). The remaining elements of Claim 4 are disclosed in Hirler, Kobayashi, and knowledge of the POSITA. In particular, Hirler discloses that the source contact trenches can be “filled with a conductive stopper made of, for example, polycrystalline silicon or *tungsten*.” Ex. 1006 at [0023] (emphasis added). Further, Kobayashi discloses the use of a barrier metal layer deposited in the contact trenches and atop the interlayer oxide layer. Ex. 1008 at Fig. 5A, [0052]-[0053], [0062]; *see supra* ¶ 82. Kobayashi also discloses the use of a barrier metal layer that is made of Ti and TiN. *Id.* at [0062]. A POSITA would further know that the common barrier metal layer material is Ti/TiN.

3. Claim 5 is obvious over Hirler in light of Kobayashi and the knowledge of the POSITA

a. 5: “The trench MOSFET of Claim 4, wherein the source contact trench is selected from one of a vertical shape and a taper shape.”

84. Claim 5 depends on Claim 4, which is discussed above in Section X(B)(2). The remaining elements of Claim 5 are disclosed in Hirler, which discloses a trench MOSFET with a vertical source contact trench. Ex. 1005 at

Fig. 2F. Moreover, Kobayashi also discloses a source contact trench with a U-shape, V-shape, or rectangular shape. Ex. 1008 at [0072], Figs. 9A, 9B. A POSITA would know that the shape of the trenches is a function of the etching chemistry. In fact, not only can the source contact trench be selected from one of a vertical shape and tapered shape, the gate trench can also be selected from the two shapes as well, with the tapered share commonly known as VMOS, while the vertical shape is commonly known as UMOS.

4. Claim 7 is obvious over Hirler in light of Kobayashi and the knowledge of the POSITA

a. 7: “The trenched MOSFET of claim 6, wherein further comprises a barrier metal layer and contact metal plugs.”

85. Claim 7 depends on Claim 6, which is disclosed in Hirler, as discussed above in Section X(A)(3). The remaining elements of Claim 7 are disclosed in Hirler, Kobayashi, and the knowledge of the POSITA, as described above in relation to Claim 3. *See supra* Section X(B)(1). Inverting the conductivity types simply allows the formation of either an N-channel MOSFET or a P-channel MOSFET. The POSITA would understand that the inversion of conductivity types is the fundamental basis in forming Complementary Metal-Oxide-Silicon (CMOS) Field Effect Transistors. The metallurgy for contacting and interconnecting the source and drain regions is the same for either N-channel MOSFET or P-channel

MOSFET, including using the same conductive material for the barrier metal layer and the contact metal plugs.

5. Claim 8 is obvious over Hirler in light of Kobayashi and the knowledge of the POSITA

- a. 8: “The trench MOSFET of claim 7, wherein the barrier metal layer is Ti/TiN and the contact metal plug is Tungsten.”**

86. Claim 8 depends on Claim 7, which is discussed above in Section X(B)(4). The remaining elements of Claim 8 are disclosed in Hirler, Kobayashi, and the knowledge of the POSITA, as described above in relation to Claim 4. *See supra* Section X(B)(2). The POSITA would understand that the inversion of conductivity types would not affect the previous disclosure and analysis. *See supra* ¶ 84.

6. Claim 9 is obvious over Hirler in light of Kobayashi and the knowledge of the POSITA

- a. 9: “The trench MOSFET of claim 8, wherein the source contact trench is selected from one of a vertical shape and a tapered shape.”**

87. Claim 9 depends on Claim 8, which is discussed above in Section X(B)(5). The remaining elements of Claim 9 are disclosed in Hirler, as described above in relation to Claim 5. *See supra* Section X(B)(3). The POSITA would understand that the inversion of conductivity types would not affect the previous disclosure and analysis. *See supra* ¶ 84,.

7. Combining Hirler and Kobayashi in light of knowledge of the POSITA

88. The POSITA would have been motivated to combine the barrier metal layer of Kobayashi with the MOSFET of Hirler to arrive at the subject matter of Claims 3-5 and Claims 7-9.

89. First, Hirler, Kobayashi, and the '634 Patent are analogous art that seek to solve similar problems. Hirler, Kobayashi, and the '634 Patent are in the same field of endeavor, *i.e.*, Vertical Power MOSFET structures, and the methods to improve the performance tradeoff in the ON-state (ON-Resistance and speed) and OFF-state (breakdown voltage). Moreover, Hirler, Kobayashi, and the '634 Patent disclose a similar doping concentration engineering technique, *i.e.*, dopant ion implantation, that allows for the formation of a low resistance source contact, at the bottom of the base region and/or on the sidewall of the trenched contact region, with minimal impact to the threshold voltage or the ON-Resistance of the Power MOSFET.

90. Second, the POSITA would have been motivated to combine the barrier metal layer disclosed in Kobayashi to the MOSFET disclosed in Hirler. In general, a POSITA would know that the use of a barrier metal layer, made of materials such as Ti and TiN, would promote the adhesion of the tungsten contact plug of Hirler to the contact area of the source contact trenches. The Ti and TiN barrier layer also prevents unwanted elements, such as fluorine from the deposition

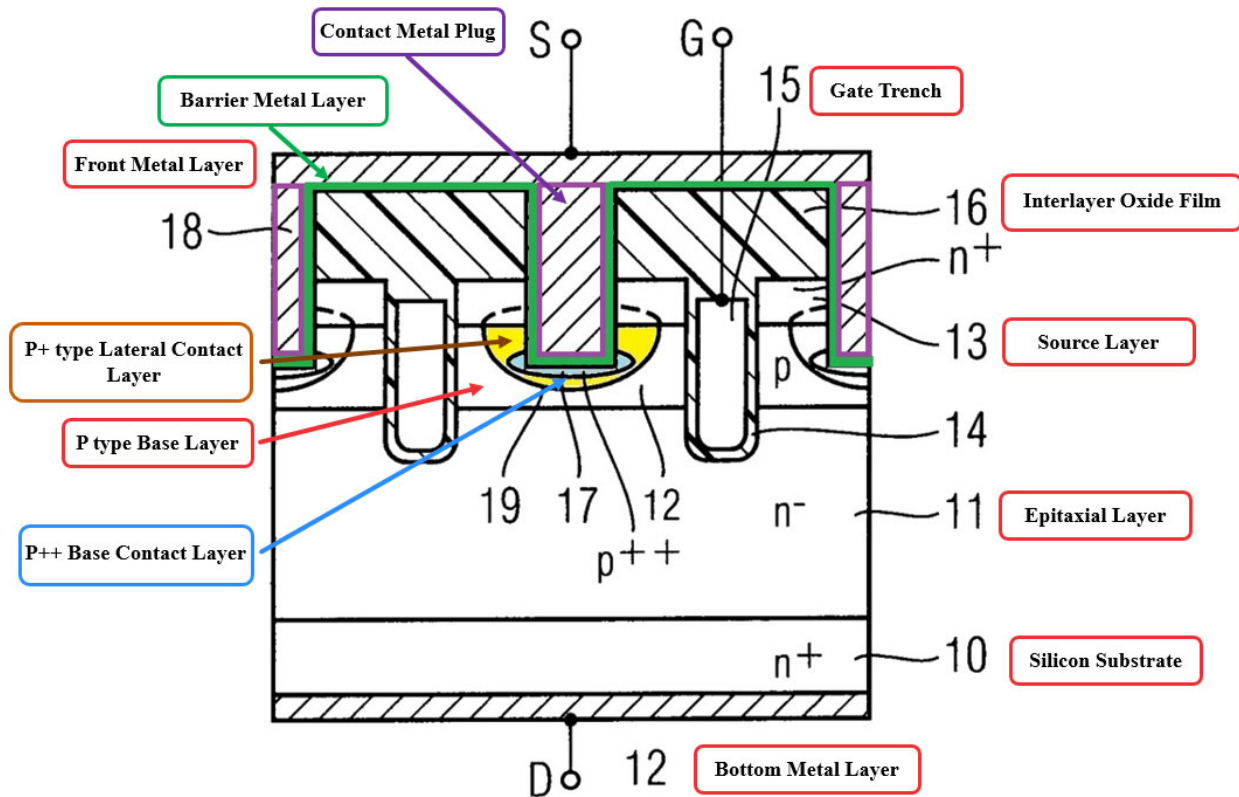
process of W, from seeping into the underlying silicon surface, which would degrade the performance of the transistor.

91. To elaborate, the use of a tungsten contact plug along with a barrier metal layer to fill contact holes or trench with high aspect ratio is well known to a POSITA. As MOSFET manufacturing process scales to smaller dimension, the need for an interconnect process with good planarization becomes increasingly critical. The requirement to fill contact holes that has high aspect ratio, like a trench, and achieve smooth top planar surface is met by the use of chemical vapor deposition (“CVD”) of tungsten. The CVD tungsten process is able to conformally fill contact holes with a high aspect ratio and produce a planar top surface after the CVD tungsten is etched back.

92. It is also obvious to a POSITA that the deposition of CVD tungsten is typically preceded by the usage of a barrier metal layer. This barrier metal layer acts as diffusion barrier to prevent unwanted interaction between the CVD W and the underlying silicon. A POSITA would further find it obvious to try Ti/TiN, as the common barrier metal layer material is Ti/TiN layer.

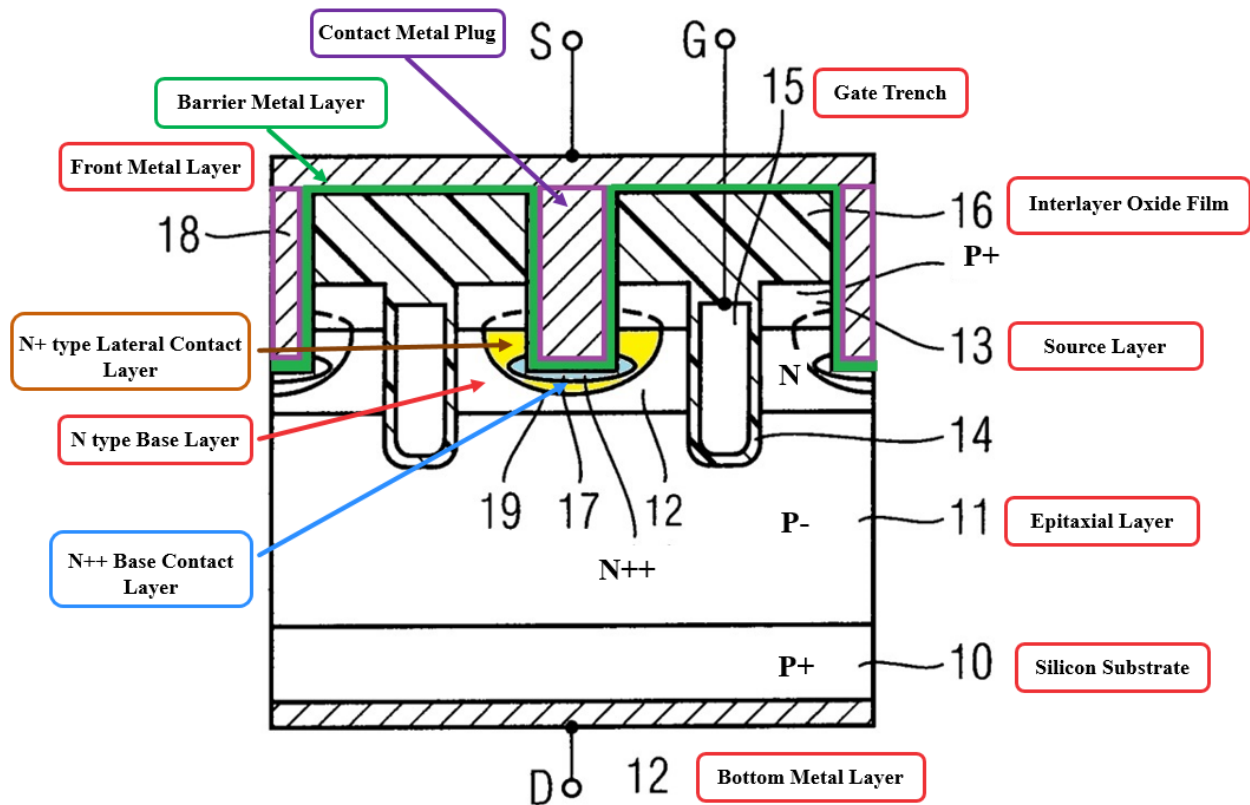
93. Accordingly, it is my opinion that the combination of Hirler and Kobayashi renders obvious Claims 3-5 and 7-9, as illustrated below in a hypothetical diagram based on Hirler’s Figure 2F with the tungsten contact metal

plug in Hirler (in purple) and the addition of the Ti/TiN barrier metal layer according to disclosure in Kobayashi (in green).



Hirler, Figure 2F (annotated)

94. Below is the same hypothetical diagram but with inverted conductivity types, showing a p-channel MOSFET.

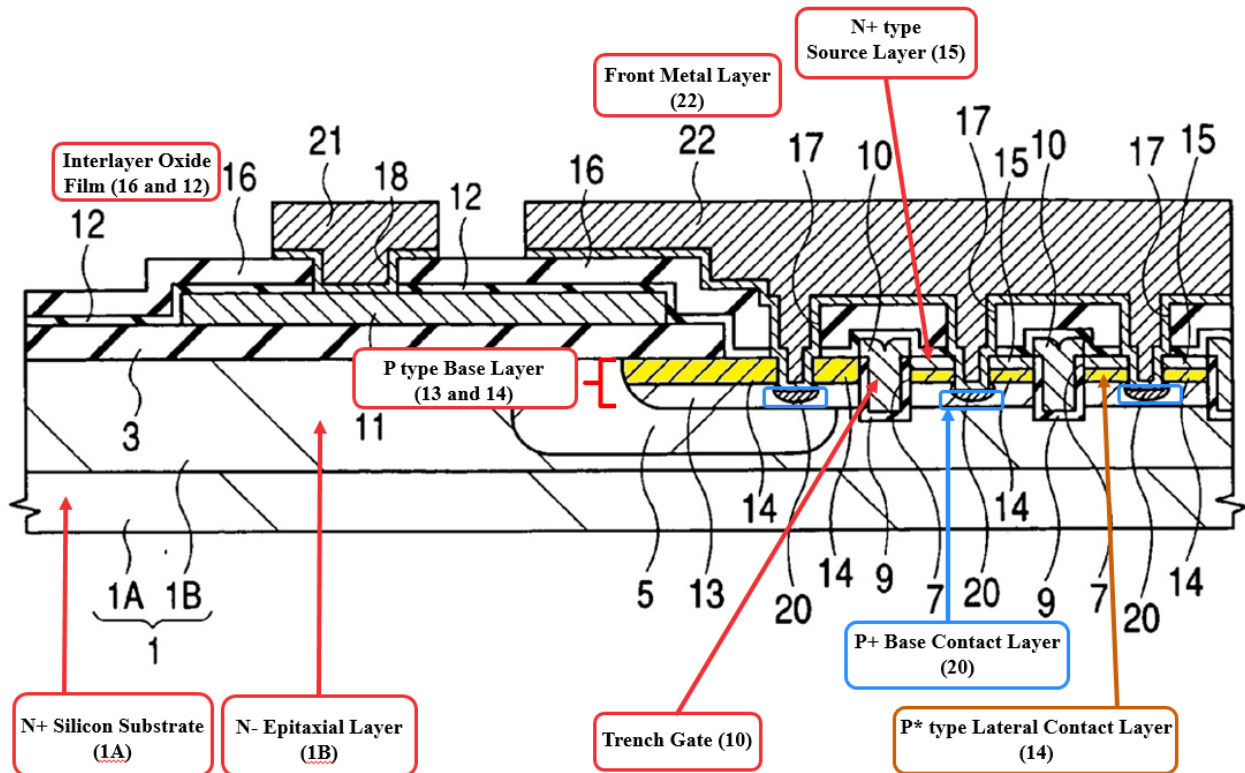


Hirler, Figure 2F (annotated)

C. Claims 1 and 2 are unpatentable under pre-AIA 35 U.S.C. § 102(b) as anticipated by Shiraishi

1. Claim 1 is anticipated by Shiraishi

95. As I further explain below, almost every element of Claim 1 is disclosed in Figure 9, as annotated below:



Shiraishi, Figure 9 (with annotation)

a. 1 [preamble]: “A trench MOSFET with trench source contact, comprising:”

96. To the extent the preamble is limiting, it is disclosed in Shiraishi, which discloses a trench MISFET with source contact trenches. Ex. 1009 at [0005], [0074], Fig. 8. The POSITA would understand that a MISFET is interchangeable with the term MOSFET. Specifically, a MOSFET (Metal-Oxide-Semiconductor FET) is a type of MISFET (Metal-Insulator-Semiconductor FET) wherein the insulator is an oxide.

99. Specifically, Shiraishi discloses that “[t]he n⁺type single crystal silicon substrate **1A** and the n⁺type single crystal silicon layer **1B** [*i.e.*, epitaxial layer] may serve as a drain region for the respective power MISFETs.” Ex. 1009 at [0067], Claim 22. The POSITA would clearly understand that the silicon substrate (1A) corresponds to a silicon substrate, and would understand the silicon layer (1B) corresponds to a epitaxial layer.

100. Shiraishi also discloses that “the p⁺type semiconductor region **13** [*i.e.*, base layer] may serve as a channel layer for the respective power MISFETs.” Ex. 1009 at [0072]. The POSITA would understand that the channel layer (13) corresponds to a body region or base layer.

101. Finally, Shiraishi discloses “the source region in the n⁺type semiconductor region **15**.” Ex. 1009 at [0073]. The POSITA would clearly understand that this region corresponds to a source region.

c. 1[b]: “a front metal layer formed on the upper surface of said semiconductor region”

102. Element 1[b] is disclosed in Shiraishi, wherein a source pad (22) is located on top of the source region. Ex. 1009 at Fig. 9, [0077] (“a source pad (a first electrode) **22** electrically connected to the n⁺type semiconductor region **15** serving as the source region for the respective power MISFETS”). A POSITA would understand that the disclosed electrode or “source pad” corresponds to and

is equivalent to a front metal layer. This is a feature that is well-known in the art and to the POSITA.

d. 1[c]: “an interlayer oxide film formed between said source layer and said front metal layer;”

103. Element 1[c] is disclosed in Shiraishi, wherein an insulating film (16 and 12) is formed between the source region (15) and the source electrode (22). Ex. 1009 at Fig. 9, [0074]-[0075]. A POSITA would understand that the “insulating film” between the source layer and the source pad corresponds to and is equivalent to an interlayer oxide film. This is a feature that is well-known in the art and to the POSITA.

e. 1[d]: “a bottom metal layer formed on the lower surface of said semiconductor region;”

104. Element 1[d] is disclosed in Shiraishi, wherein an “electrically conductive film[]” may be deposited over the back surface of the silicon substrate (1A), acting as an extraction or drain electrode. Ex. 1009 at [0097]. Although not pictured in Figures 8 or 9, a POSITA would understand that the “electrically conductive film[]” on the back surface of the silicon substrate is a bottom metal layer. This is a feature that is well-known in the art and to the POSITA.

- f. 1[e]: “a plurality of trenched gates covered by said interlayer oxide film are formed on top of said source layer extending downwardly through said base layer to a portion of said epitaxial layer; and”**

105. Element 1[e] is disclosed in Shiraishi. As shown in Figure 8, Shiraishi discloses a plurality of gate electrodes (10) that are covered by the insulating film (16 and 12) and extends downward through source layer (15), the channel layer (13), and into a portion of the epitaxial layer (1B). Ex. 1009 at Fig. 8, [0070], [0074]. This feature is well known in the art and to the POSITA.

- g. 1[f]: “a plurality of source contact trenches formed on the top of said interlayer oxide film extending downwardly through said source layer to a portion of said base layer”**

106. Element 1[f] is disclosed in Shiraishi. Specifically, as shown in Figure 8, Shiraishi discloses source contact trenches (17) formed on top of the insulating film (16 and 12) that extend down through the N⁺-type source layer (15) to the P-type body region (13 and 14). Ex. 1009 at Fig. 8, [0074]. The POSITA would understand that the additional semiconductor layer (14) is part of the body layer (13 and 14). Ex. 1009 at [0073] (“the p-type semiconductor region **14** inside the p-type semiconductor region **13**”), [0092] (“the p-type semiconductor region **14** may be implemented in the p-type semiconductor region **13**”). A body layer is defined by the layers with opposite conductivity to the source and drain regions. This is a feature that is well-known in the art and to the POSITA.

h. 1[g]: “wherein the sidewalls of said trenches in said base layer are covered by the lateral contact layer;”

107. Element 1[g] is disclosed by Shiraishi. Specifically, as shown in Figure 8, Shiraishi discloses an additional semiconductor layer (14) along the sidewalls of the contact trench. Ex. 1009 at Fig. 8; [0073], [0080], [0084]-[0085], [0092] (“The localized formation of the p-type semiconductor region **14** may be implemented in the p-type semiconductor region **13**, as discussed herein throughout *[sic]*.”) . Shiraishi discloses and the POSITA would understand that this region acts as a lateral contact layer to prevent punch-through. Ex. 1009 at [0073].

i. 1[h]: “wherein the bottom base of said trenches in said base layer are covered by the base contact layer.”

108. Element 1[h] is disclosed in Shiraishi, in which the bottom of the contact trench is covered by a semiconductor region (20). Ex. 1009 at Fig. 8, [0075] (“forming a p+type semiconductor region (a fourth semiconductor layer) **20** in such a way as to cover the respective bottom of the contact grooves **17**.”). This is a feature that is well-known in the art and to the POSITA.

2. Claim 2 is anticipated by Shiraishi

a. 2[a] “The trenched MOSFET of claim 1, wherein the silicon substrate, the epitaxial layer, and the source layer are N-type;”

109. Claim 2 depends on Claim 1, which is disclosed in Shiraishi, as discussed above in Section X(C)(1). Element 2[a] is disclosed in Shiraishi. Shiraishi discloses a trenched MISFET, wherein the silicon substrate, the epitaxial

layer, and the source layer are N-type. Ex. 1009 at [0067], [0073]. These are features of an N-channel MOSFET that are well-known in the art and to the POSITA.

b. 2[b] “the base layer and lateral contact layer are P-type;”

110. Element 2[b] is disclosed in Shiraishi. In reference to regions shown in Figure 8, Shiraishi discloses a “p-type semiconductor region **14** [*i.e.*, the lateral contact layer] inside the p-type semiconductor region **13**.” Ex. 1009 at Fig. 8, [0073]. These are features of an N-channel MOSFET that are well-known in the art and to the POSITA.

c. 2[c] “and each of the source contact trenches further has a P-type base contact layer at a bottom thereof, and the lateral contact layer has less doping concentration than the base contact layer at bottom.”

111. Element 2[c] is disclosed in Shiraishi. Shiraishi discloses that “p-type semiconductor region **14** [*i.e.*, lateral contact layer] may be locally higher in impurity concentration than the p type semiconductor region **13**.” Ex. 1009 at Fig. 8, [0080]. In addition, Shiraishi discloses that “[i]mpurity concentration in the p⁺-type semiconductor region **20** [*i.e.*, base contact layer] may be rendered higher than that in the p-type semiconductor region **14** [*i.e.*, lateral contact layer].” Ex. 1009 at Fig. 8, [0075]. The POSITA would understand that Shiraishi disclosed a lateral contact layer of p-type conductivity with a P-type doping concentration

that was higher than the underlying base layer but lower than the P-type doping concentration of the base contact layer.

D. Claims 3-9 are unpatentable under pre-AIA 35 U.S.C. § 103(a) as obvious over Shiraishi in light of Kobayashi and the knowledge of the POSITA

1. Claim 3 is obvious over Shiraishi in light of Kobayashi and the knowledge of the POSITA

a. 3: “The trenched MOSFET of Claim 2, wherein further comprises a barrier metal layer and a plurality of contact metal plugs.”

112. Claim 3 depends on Claim 2, which is disclosed in Shiraishi, as discussed above in Section X(C)(2). The remaining elements of Claim 3 are disclosed in Shiraishi, Kobayashi, and the knowledge of the POSITA. Shiraishi discloses a “TiW (titanium tungsten) film serving as a barrier conductor film” Ex. 1009 at [0076]. Kobayashi discloses the use of a plurality of contact metal plugs. Ex. 1008 at [0052], [0066], Fig. 5A, Claim 4. The use of contact metal plugs and the barrier metal layer are generally known to the POSITA. As MOSFET manufacturing process scales to smaller dimension, the need for an interconnect process with good planarization becomes increasingly critical. The requirement to fill contact holes that has high aspect ratio, like a trench, and achieve smooth top planar surface is met by the use of CVD tungsten. The CVD tungsten process is able to conformally fill contact holes with a high aspect ratio, and produce a planar top surface after the CVD tungsten is etched back.

113. A POSITA would also know that the deposition of CVD tungsten is typically preceded by the usage of a barrier metal layer. This barrier metal layer acts as diffusion barrier to prevent unwanted interaction between the CVD W and the underlying silicon.

114. Kobayashi also teaches that the contact metal plug is beneficial to the operation of the MOSFET. The plug “allows the resistance component of the source electrode **18** [to be] reduced” by creating a flat surface for the source electrode. Ex. 1008 at [0066], Claim 4 (claiming a contact hole filled with “a metal which serves as said contact and has a flattened surface, said source electrode being formed on the flattened surface of said metal . . .”).

115. Kobayashi discloses that the source electrode “having a flat surface assures a wide contact area in wire bonding or clip bonding carried out for the surface so that a total on-resistance after mounting can be reduced.” *Id.* at [0066]. A POSITA would know that eventually the source metal layer which connects to the contact metal plug will eventually be connected through bonding to a chip package that will be mounted to a circuit board. Two types of bonding techniques, bonding through a wire or bonding through a copper clip, would be commonly used. The difference between wire bonding and clip bonding is that clip employs a larger surface area for the bonding conducting material. In either bonding

technique, a flat metal source electrode or pad, would offer a better surface area for achieving low resistance bonding.

116. Finally, “it is possible to perform chip mounting by bump connection, which is difficult when the source electrode has an irregular surface.” Ex. 1008 at [0066]. The POSITA would thus be motivated to combine the source contact plugs with the disclosure of Shiraishi. *See also* Section X(D)(8) *infra*.

2. Claim 4 is obvious over Shiraishi in light of Kobayashi and the knowledge of the POSITA

a. 4: “The trench MOSFET of Claim 3, wherein the barrier metal layer is Ti/TiN and the contact metal plug is Tungsten.”

117. Claim 4 depends on Claim 3, which is discussed above in Section X(D)(1). The remaining elements of Claim 4 are disclosed in Shiraishi, Kobayashi, and the knowledge of the POSITA. Shiraishi discloses the uses of a barrier metal layer that is made of TiW (titanium-tungsten). Ex. 1009 at [0076]. Kobayashi discloses the use of the contact metal plug that is made of tungsten (W). Ex. 1008 at [0052], [0066], Fig. 5A. Kobayashi also discloses the use of a barrier metal layer that is made of Ti and TiN. Ex. 1008 at [0062]. A POSITA would further know that the common barrier metal layer material is Ti/TiN.

3. Claim 5 is obvious over Shiraishi in light of Kobayashi and the knowledge of the POSITA

- a. 5: “The trench MOSFET of Claim 4, wherein the source contact trench is selected from one of a vertical shape and a taper shape.”**

118. Claim 5 depends on Claim 4, which is discussed above in Section X(D)(2). The remaining elements of Claim 5 are disclosed in Shiraishi, which discloses a trench MISFET with a plurality of vertical source contact trenches. Ex. 1009 at Fig. 8. Kobayashi also discloses source contact trenches with a U-shape, V-shape, or rectangular shape. Ex. 1008 at [0072], Figs. 9A, 9B. A POSITA would know that the shape of the trenches is a function of the etching chemistry. In fact, not only can the source contact trench be selected from one of a vertical shape and tapered shape, the gate trench can also be selected from the two shapes as well, with the tapered share commonly known as VMOS, while the vertical shape is commonly known as UMOS.

4. Claim 6 is obvious over Shiraishi in light of Kobayashi and the knowledge of the POSITA

- a. 6: “The trench MOSFET of claim 1, wherein the silicon substrate, the epitaxial layer, and the source layer are P-type; the base layer and lateral contact layer are N-type; and each of the source contact trenches further has a N-type base contact layer at a bottom thereof, and the lateral contact layer has less doping concentration than the base contact layer at bottom.”**

119. Claim 6 depends on Claim 1, which is disclosed in Shiraishi, as discussed above in Section X(C)(1). The remaining elements of Claim 6 are disclosed in Shiraishi, Kobayashi, and the knowledge of the POSITA. Shiraishi discloses the formation of a trench MOSFET with semiconductor layers of “a first conductivity type [*e.g.*, N-type] ” and “second conductivity type opposite to the first conductivity type [*e.g.*, P-type],” along with specific embodiments of an n-channel MOSFET. *See, e.g.*, Ex. 1009 at [0017]-[0028], [0067], Claim 1. Kobayashi similarly discloses a trench MOSFET with semiconductor layers of a first conductivity type and a second conductivity type opposite to the first conductivity type, along with specific embodiments of n-channel MOSFETs. *See, e.g.*, Ex. 1008 at Claim 1, [0062]. In particular, Kobayashi discloses “inverting the conductive type, [such that] this invention is also applicable to a P-channel MOSFET structure.” Ex. 1008 at [0072]. The POSITA would understand that the conductivity type options were limited to P-type or N-type channel MOSFETs.

120. The POSITA would understand that there are only two conductivity types and would know how to alter a design to account for P-channel or N-channel MOSFET as needed.

5. Claim 7 is obvious over Shiraishi in light of Kobayashi and the knowledge of the POSITA

a. 7: “The trench MOSFET of claim 6, wherein further comprises a barrier metal layer and contact metal plugs.”

121. Claim 5 depends on Claim 6, which is discussed above in Section X(D)(4). The remaining elements of Claim 7 are disclosed in Shiraishi, Kobayashi and the knowledge of the POSITA, as described above in relation to Claim 3. *See supra* Section X(D)(1).

122. A POSITA would know that inverting the conductivity types simply allows the formation of either an N-channel MOSFET or a P-channel MOSFET. The POSITA would understand that the inversion of conductivity types is the fundamental basis in forming Complementary Metal-Oxide-Silicon (CMOS) Field Effect Transistors. The metallurgy for contacting and interconnecting the source and drain regions is the same for either N-channel MOSFET or P-channel MOSFET, including using the same conductive material for the barrier metal layer and the contact metal plugs.

6. Claim 8 is obvious over Shiraishi in light of Kobayashi and the knowledge of the POSITA

- a. 8: “The trenched MOSFET of claim 7, wherein the barrier metal layer is Ti/TiN and the contact metal plug is Tungsten.”**

123. Claim 8 depends on Claim 7, which is discussed above in Section X(D)(5). The remaining elements of Claim 8 are disclosed in Shiraishi, Kobayashi, and the knowledge of the POSITA, as described above in relation to Claim 4. *See supra* Section X(D)(2). The POSITA would understand that the inversion of conductivity types would not affect the previous disclosure and analysis. *See supra* ¶ 121.

7. Claim 9 is obvious over Shiraishi in light of Kobayashi and the knowledge of the POSITA

- a. 9: “The trenched MOSFET of claim 8, wherein the source contact trench is selected from one of a vertical shape and a tapered shape.”**

124. Claim 9 depends on Claim 8, which is discussed above in Section X(D)(6). The remaining elements of Claim 9 are disclosed in Shiraishi, as described above in relation to Claim 5. The POSITA would understand that the inversion of conductivity types would not affect the previous disclosure and analysis. *See supra* ¶ 121.

8. Combining Shiraishi and Kobayashi in light of knowledge of the POSITA

125. It is my opinion that it would have been obvious to a POSITA before the effective filing date of the '634 Patent (February 23, 2008) to combine Shiraishi and Kobayashi to arrive at the subject matter of Claims 3-9, rendering those claims invalid under 35 U.S.C. § 103.

126. In particular, the POSITA would have been motivated to combine the metal contact plug and barrier metal layer of Kobayashi and the MISFET of Shiraishi with a reasonable likelihood of success to arrive at the subject matter of Claims 3-5. In addition, the POSITA would have been motivated to combine Kobayashi with Shiraishi to invert the P/N types of Shiraishi to arrive at the subject matter of Claims 6-9. P-channel and N-channel MOSFETs are also known in the art and to the POSITA.

127. First, Shiraishi, Kobayashi, and the '634 Patent are analogous art that seek to solve similar problems. Shiraishi, Kobayashi, and the '634 Patent are in the same field of endeavor, *i.e.*, Vertical Power MOSFET structures, and the methods to improve the performance tradeoff in the ON-state (ON-Resistance and speed), and OFF-state (breakdown voltage). Moreover, Shiraishi, Kobayashi, and the '634 Patent disclose a similar doping concentration engineering technique, *i.e.*, dopant ion implantation, that allows for the formation of a low resistance source contact, at the bottom of the base region and/or on the sidewall of the trenched

contact region, with minimal impact to the threshold voltage or the ON-Resistance of the Power MOSFET.

128. Second, specific to metal contact plugs, Kobayashi expressly teaches that the contact metal plug is beneficial because it “allows the resistance component of the source electrode **18** [to be] reduced” by creating a flat surface for the source electrode. Ex. 1008 at [0066], Claim 4 (claiming use of a metal contact plug to provide a flattened surface and a source electrode deposited on said flattened surface). Further, Kobayashi teaches that the source electrode “having a flat surface assures a wide contact area in wire bonding or clip bonding carried out for the surface so that a total on-resistance after mounting can be reduced.” Ex. 1008 at [0066]. Finally, “it is possible to perform chip mounting by bump connection, which is difficult when the source electrode has an irregular surface.” *Id.* In particular, Kobayashi teaches the use of tungsten metal contact plugs. The POSITA would thus be motivated to combine the metal contact plugs taught by Kobayashi with the disclosure of Shiraishi. *See supra* ¶¶ 111-115.

129. Third, the POSITA would have been motivated to combine the barrier metal layer disclosed in Kobayashi to the MISFET disclosed in Shiraishi. In general, a POSITA would know that the use of a barrier metal layer, made of materials such as Ti and TiN, would promote the adhesion of the tungsten contact plug taught in Kobayashi to the contact area of the source contact trenches. The Ti

and TiN barrier layer also prevents unwanted elements, such as fluorine from the deposition process of W, from seeping into the underlying silicon surface, which would degrade the performance of the transistor.

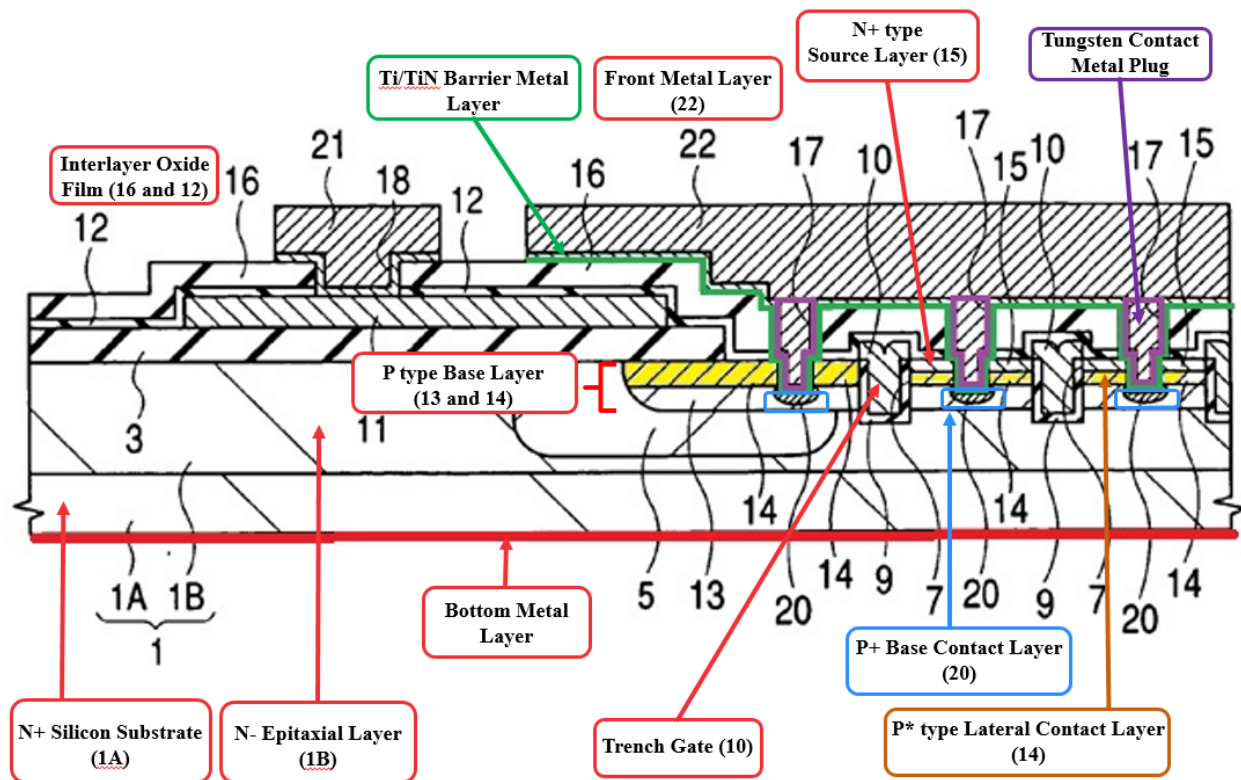
130. To elaborate, the use of a tungsten contact plug along with a barrier metal layer to fill contact holes or trench with high aspect ratio is well known to a POSITA. As MOSFET manufacturing process scales to smaller dimension, the need for an interconnect process with good planarization becomes increasingly critical. The requirement to fill contact holes that has high aspect ratio, like a trench, and achieve smooth top planar surface is met by the use of CVD tungsten. The CVD tungsten process is able to conformally fill contact holes with a high aspect ratio, and produce a planar top surface after the CVD tungsten is etched back.

131. It is also obvious to a POSITA that the deposition of CVD tungsten is typically preceded by the usage of a barrier metal layer. This barrier metal layer acts as diffusion barrier to prevent unwanted interaction between the CVD W and the underlying silicon. A POSITA would further find it obvious to try a Ti/TiN barrier metal layer, as the common barrier metal layer material is Ti/TiN layer.

132. Fourth, inverting the P- or N-type regions of the MOSFET is known in the art. A POSITA generally inverts the regions to create either a P- or N- channel MOSFET as required by the specific product the transistor is supporting.

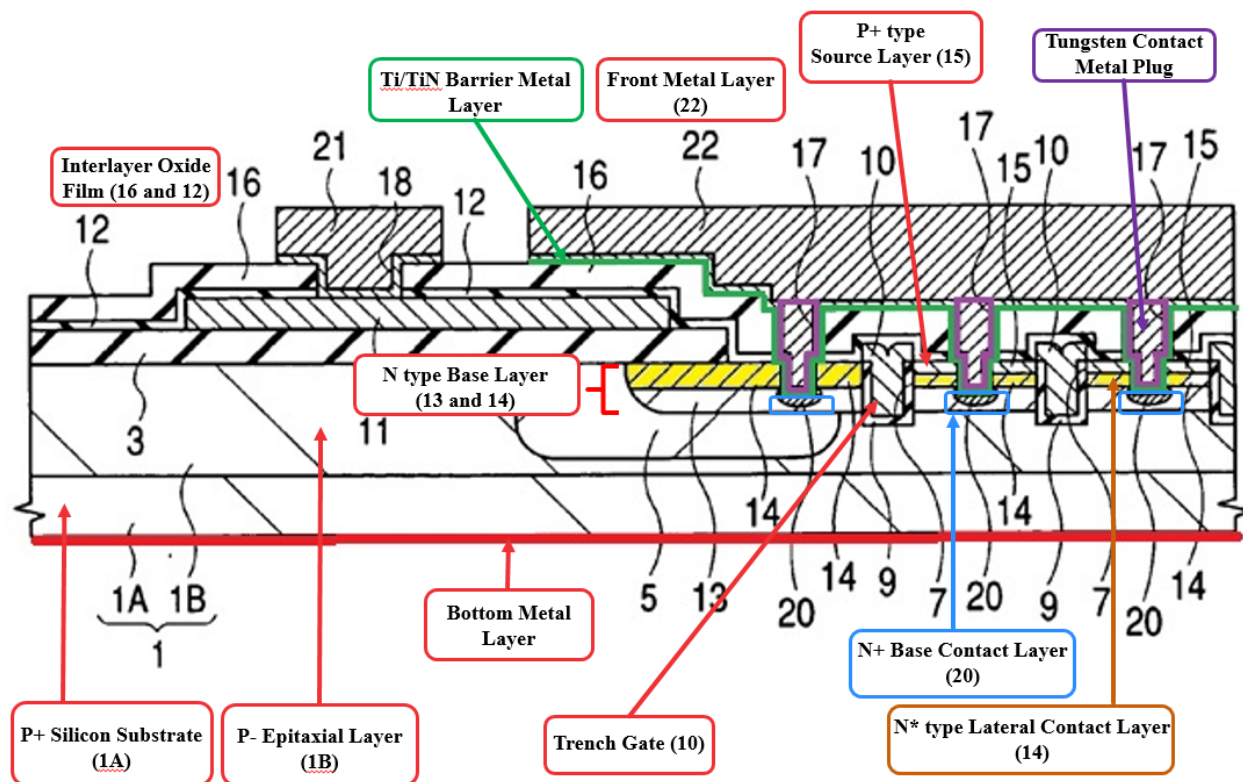
Moreover, both Kobayashi and Shiraishi disclose a general MOSFET that can be tailored to be P- or N- channel. In particular, the POSITA would understand that the inversion of the P- and N- types would not affect the disclosure of contact metal plugs or barrier metal layers. The POSITA would understand that the inversion of conductivity types is the fundamental basis in forming Complementary Metal-Oxide-Silicon (CMOS) Field Effect Transistors. The metallurgy for contacting and interconnecting the source and drain regions is the same for either N-channel MOSFET or P-channel MOSFET, including using the same conductive material for the barrier metal layer and the contact metal plugs.

133. Accordingly, the combination of Shiraishi and Kobayashi renders obvious Claims 3-9, as illustrated below in a hypothetical diagram based on Shiraishi's Figure 9 with the addition of the tungsten (W) source contact plugs (in purple) and Ti/TiN barrier metal layer (in green) according to disclosures in Kobayashi.



Shiraishi, Figure 9 (annotated)

134. Below is the same hypothetical diagram but with inverted conductivity types, showing a p-channel MOSFET.



Shiraishi, Figure 9 (annotated)

E. Claims 1-9 are unpatentable under pre-AIA 35 U.S.C. § 103(a) as obvious over Kobayashi in light of Shiraishi and the knowledge of the POSITA

1. Claim 1 is obvious over Kobayashi in light of Shiraishi and the knowledge of the POSITA

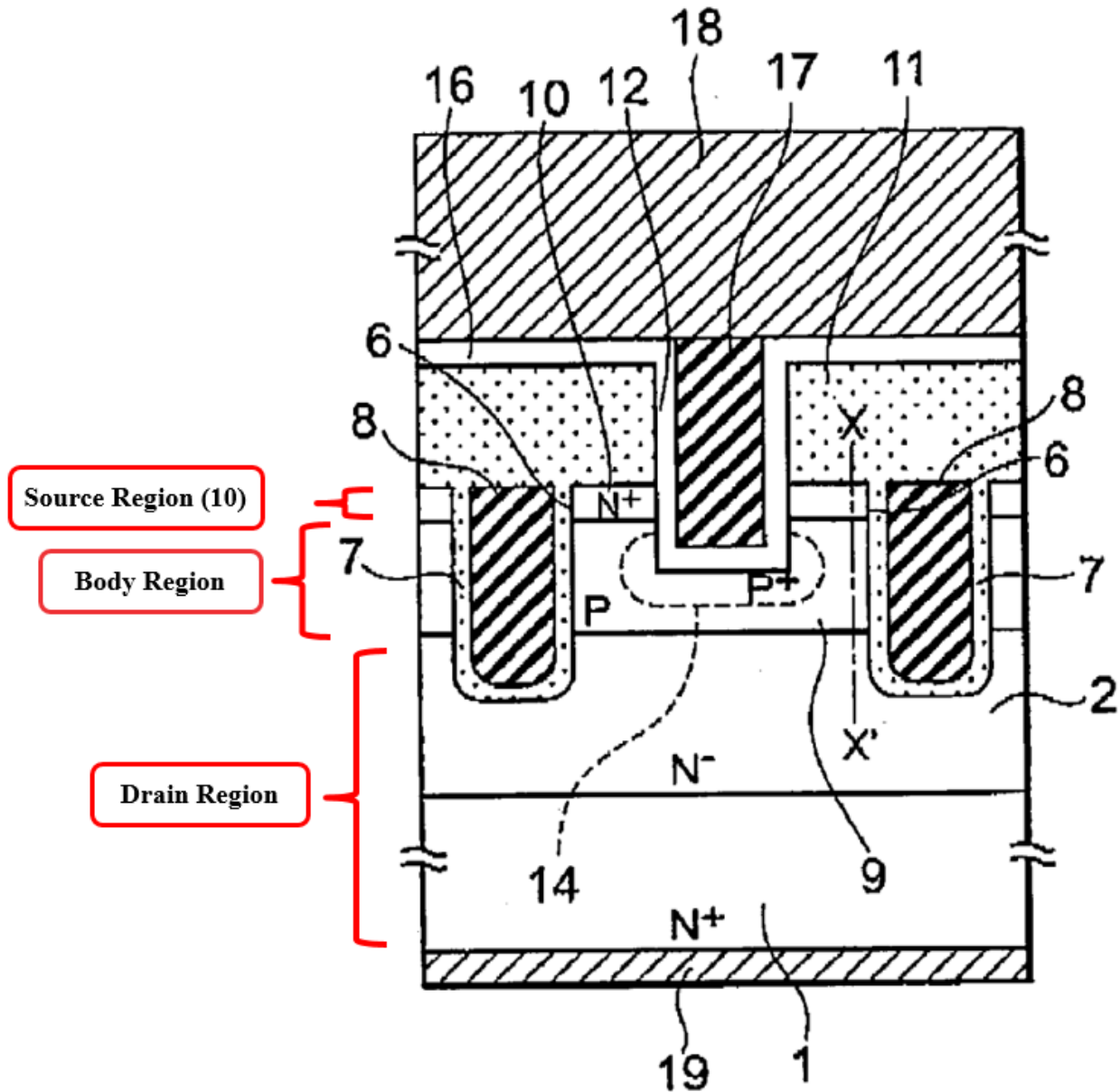
a. 1 [preamble]: “A trench MOSFET with trenched source contact, comprising:”

135. To the extent the preamble is limiting, it is disclosed in Kobayashi, which discloses a trench MOSFET with source contact trenches. Ex. 1008 at Fig. 5A, [0052].

- b. **1[a]: “a semiconductor region having a drain region, a body region and a source region, comprising, a silicon substrate, an epitaxial layer corresponding to said drain region disposed on the top of said silicon substrate, a base layer corresponding to said body region disposed on the top of said epitaxial layer, and a source layer corresponding to said source region disposed on the top of said base layer;”**

136. Element 1[a] is disclosed in Kobayashi, which describes a vertical trench MOSFET with a drain region, a body region, and a source region—features that a POSITA would know are universal to all MOSFETs. Ex. 1008 at Fig. 5A, [0018] (disclosing “Structure 1. A vertical MOSFET (or a UMOSFET) comprising: a semiconductor layer (**1, 2, 9, 10**) having first and second surface opposite to each other and . . . a unit cell formed in a region of the semiconductor layer surrounded by the pair of trench gates, the unit cell comprising a base layer (**9**) and a source layer (**10**) formed on the base layer . . .”), [0052]. The POSITA would understand that, for example in Figure 5A, Kobayashi discloses a MOSFET with a N⁺-type drain region at **1**, a P-type body region at **7**, and a N⁺-type source region at **10**. A POSITA would also understand that a base layer corresponds to and is equivalent to a body layer.

137. Specifically, Kobayashi discloses an arrangement where “an N⁺-type silicon substrate **1** and an N⁻-type epitaxial layer **2** formed on one surface of the N⁺-type silicon substrate **1**. A P-type base layer **9** and an N⁺-type source layer **10** are formed on a surface of the N⁻-type epitaxial layer **2**. . . .” Ex. 1008 at [0052].



Kobayashi, Figure 5A (annotated in regards to Claim element 1a)

- c. 1[b]: “a front metal layer formed on the upper surface of said semiconductor region”

138. Element 1[b] is disclosed in Kobayashi, wherein a “source electrode 18” is located on the surface of the barrier metal layer and source contact plug.

Ex. 1008 at Fig. 5A, [0052] (“On the surface of the W 17 and the barrier metal 16,

a source electrode **18** is formed.”), [0018] (. . . “a source electrode (**18**) formed on the contact [hole]”). The POSITA would understand that the “source electrode” corresponds to and is equivalent to a “front metal layer.” This is a feature that is well-known in the art and to the POSITA.

d. 1[c]: “an interlayer oxide film formed between said source layer and said front metal layer;”

139. Element 1[c] is disclosed in Kobayashi, wherein an interlayer oxide film (11) is formed atop the gate trenches and between the source region (10) and the source electrode (18). Ex. 1008 at Fig. 5A, [0052] (“On the polysilicon **8** to serve as a gate electrode or a trench gate, an interlayer oxide film **11** is formed”). This is a feature that is well-known in the art and to the POSITA.

e. 1[d]: “a bottom metal layer formed on the lower surface of said semiconductor region;”

140. Element 1[d] is disclosed in Kobayashi, wherein a “drain electrode **19**” is formed on the surface of the N⁺-type silicon substrate (1). Ex. 1008 at Fig. 5A, [0052] (“On the other surface of the N⁺-type silicon substrate **1**, a drain electrode **19** is formed.”), [0018]. The POSITA would understand that the “drain electrode” corresponds to and is equivalent to a “bottom metal layer.” This is a feature that is well-known in the art and to the POSITA.

- f. **1[e]: “a plurality of trenched gates covered by said interlayer oxide film are formed on top of said source layer extending downwardly through said base layer to a portion of said epitaxial layer; and”**

141. Element 1[e] is disclosed in Kobayashi. As shown in Figure 5A, Kobayashi discloses a plurality of trench gates (6) that are covered by the interlayer oxide film (11) and that extend downward through the source layer (10), the base layer (9), and into the epitaxial layer (2). Ex. 1008 at Fig. 5A, [0052], [0055]-[0058]. This is a feature that is well-known in the art and to the POSITA.

142. Specifically Kobayashi discloses that “[i]n each of trenches 6 reaching the N⁻-type epitaxial layer 2 through the P-type base layer 9, a gate oxide film 7 and a polysilicon 8 are filled.” Ex. 1008 at [0052].

- g. **1[f]: “a plurality of source contact trenches formed on the top of said interlayer oxide film extending downwardly through said source layer to a portion of said base layer”**

143. Element 1[f] is disclosed in Kobayashi. Specifically, as shown in Fig. 5A, Kobayashi discloses “contact holes 12” formed on top of the interlayer oxide film that extend down through the N⁺-type source layer to the P-type base layer. Ex. 1008 at Fig. 5A, [0052]. The POSITA would understand that “contact holes” correspond to and are equivalent to “source contact trenches.” This is a feature that is well-known in the art and to the POSITA.

144. Specifically Kobayashi discloses “[b]etween the trench gates adjacent to each other, a contact hole **12** having a predetermined depth is formed to reach the P-type base layer **9** though the N⁺-type source layer **10**.” Ex. 1008 at [0052].

h. 1[g]: “wherein the sidewalls of said trenches in said base layer are covered by the lateral contact layer;”

145. Element 1[g] is disclosed by Kobayashi, Shiraishi, and the knowledge of the POSITA. Kobayashi discloses a base contact layer that covers the bottom of the source contact trench and extends partially up along the sidewalls of the source contact trenches. Ex. 1008 at Fig. 5A, [0061], Claim 1 (“... a base contact layer **14** formed within said base layer so as to enclose a bottom of said contact and to bring said base contact layer into contact with the bottom of said contact.”), Claim 3 (“... said base contact layer is formed within said base layer so as to enclose only the bottom of said contact and to bring said base contact layer into contact with only the bottom of said contact.”); *see* Ex. 1002 at 29.

146. Specifically, as shown in Figure 8, Shiraishi discloses an additional semiconductor layer (14) (*i.e.*, lateral contact layer) along the sidewalls of the contact trench in the base layer that serves as “a punch-through stopper layer.” Ex. 1009 at Fig. 8; [0073] (“the p-type semiconductor region **14** may serve as a punch-through stopper layer for the respective power MISFETs”), [0080], [0084]-[0085]. A POSITA would understand that a punch-through stopper is desirable to

prevent punch-through of current from the source layer through the body layer and to the silicon substrate or drain region.

147. Specifically, a POSITA would understand that punch-through is an undesirable phenomenon that can occur in a structure with two junctions where a layer of a second polarity is sandwiched by a two layers of a first polarity (for example, an N-P-N structure), as pictured in Figure 5A in Kobayashi and Figure 8 in Shiraishi. Punch-through occurs when the middle second polarity layer, the body layer, can no longer act as a conduction barrier between the two first-polarity end layers, the source and drain regions. This can occur when the doping concentration of the middle layer is light, and a high voltage on one of the end layer causes the depletion region to reach all the way to the layer at the other end, *i.e.* “punch-through.” The unwanted punch-through current causes the MOSFET to malfunction and unintentionally turn “on” when the transistor should otherwise be “off.”

148. The POSITA would be motivated to combine the lateral contact layer of Shiraishi with the disclosure of Kobayashi. *See also* Section X(E)(10) *infra*.

i. 1[h]: “wherein the bottom base of said trenches in said base layer are covered by the base contact layer.”

149. Element 1[h] is disclosed in Kobayashi, in which the bottom of the source contact trench is covered by a base contact layer (14). Ex. 1008 at Fig. 5A, [0061], Claim 3 (“... said base contact layer is formed within said base layer so as

to enclose only the bottom of said contact and to bring said base contact layer into contact with only the bottom of said contact.”). This is a feature that is well-known in the art and to the POSITA.

2. Claim 2 is obvious over Kobayashi in light of Shiraishi and the knowledge of the POSITA

a. 2[a] “The trench MOSFET of claim 1, wherein the silicon substrate, the epitaxial layer, and the source layer are N-type;”

150. Claim 2 depends on Claim 1, which is discussed above in Section X(E)(1). Element 2[a] is disclosed in Kobayashi. Kobayashi discloses a trench MOSFET wherein the silicon substrate, the epitaxial layer, and the source layer are N-type. Ex. 1008 at Fig. 5A, [0052] (“... an N⁺-type silicon substrate **1** and an N⁻-type epitaxial layer **2** formed on one surface of the N⁺-type silicon substrate **1**. A P-type base layer **9** and an N⁺-type source layer **10** are formed on a surface of the N⁻-type epitaxial layer **2**.”). This is a feature that is well-known in the art and to the POSITA.

b. 2[b] “the base layer and lateral contact layer are P-type;”

151. Element 2[b] is disclosed in Kobayashi, Shiraishi, and the knowledge of the POSITA, as discussed above in Section X(E)(h). The remaining elements are disclosed in Kobayashi and Shiraishi respectively. Kobayashi discloses a P-type base layer and P⁺-type base contact layer. Ex. 1008 at Fig. 5A, [0052], [0061]. Shiraishi discloses a P-type semiconductor region **14** (lateral contact layer)

that serves as an anti-punch-through layer. Ex. 1009 at [0073]. This is a feature that is well-known in the art and to the POSITA.

- c. **2[c] “and each of the source contact trenches further has a P-type base contact layer at a bottom thereof, and the lateral contact layer has less doping concentration than the base contact layer at bottom.”**

152. Claim element 2[c] are disclosed in Kobayashi, Shiraishi, and the knowledge of the POSITA. Specifically, Kobayashi discloses a P⁺-type base contact layer at the bottom of the source trenches. Ex. 1008 at Fig. 5A, [0061].

153. Shiraishi discloses an additional semiconductor layer (14) (*i.e.* lateral contact layer) along the sidewalls of the contact trench in the base layer that serves as “a punch-through stopper layer.” Ex. 1009 at Fig. 8; [0073], [0080], [0084]-[0085]. Specifically, Shiraishi discloses that the “p-type semiconductor region **14** [*i.e.*, lateral contact layer] may be locally higher in impurity concentration than the p type semiconductor region **13**.” Ex. 1009 at [0080]. In addition, Shiraishi discloses that “[i]mpurity concentration in the p⁺type semiconductor region **20** [*i.e.*, base contact layer] may be rendered higher than that in the p-type semiconductor region **14** [*i.e.*, lateral contact layer].” Ex. 1009 at [0073].

154. The POSITA would thus be motivated to combine the doping concentration profile with the disclosure of Kobayashi. *See also* Section X(E)(10) *infra*.

3. Claim 3 is obvious over Kobayashi in light of Shiraishi and the knowledge of the POSITA

- a. 3: “The trench MOSFET of Claim 2, wherein further comprises a barrier metal layer and a plurality of contact metal plugs.”**

155. Claim 3 depends on Claim 2, which is discussed above in Section X(E)(2). The remaining elements of Claim 3 are disclosed Kobayashi, which discloses the use of contact metal plugs and a barrier metal layer. Ex. 1008 at [0052]-[0053], [0066], Fig. 5A.

4. Claim 4 is obvious over Kobayashi in light of Shiraishi and the knowledge of the POSITA

- a. 4: “The trench MOSFET of Claim 3, wherein the barrier metal layer is Ti/TiN and the contact metal plug is Tungsten.”**

156. Claim 4 depends on Claim 3, which is discussed above in Section X(E)(3). The remaining elements of Claim 4 are disclosed in Kobayashi, which discloses the use of tungsten contact metal plugs. Ex. 1008 at [0052], [0066], Fig. 5A. Kobayashi also discloses the use of a barrier metal layer that is made of Ti and TiN. Ex. 1008 at [0062].

5. Claim 5 is obvious over Kobayashi in light of Shiraishi and the knowledge of the POSITA

- a. 5: “The trench MOSFET of Claim 4, wherein the source contact trench is selected from one of a vertical shape and a taper shape.”**

157. Claim 5 depends on Claim 4, which is discussed above in Section X(E)(4). The remaining elements of Claim 5 are disclosed in Kobayashi, which discloses a MOSFET with a source contact trench with a U-shape, V-shape, or rectangular shape. Ex. 1008 at [0072], Figs. 5A, 9A, 9B. A POSITA would know that the shape of the trenches is a function of the etching chemistry. In fact, not only can the source contact trench be selected from one of a vertical shape and tapered shape, the gate trench can also be selected from the two shapes as well, with the tapered share commonly known as VMOS, while the vertical shape is commonly known as UMOS.

6. Claim 6 is obvious over Kobayashi in light of Shiraishi and the knowledge of the POSITA

- a. 6: “The trench MOSFET of claim 1, wherein the silicon substrate, the epitaxial layer, and the source layer are P-type; the base layer and lateral contact layer are N-type; and each of the source contact trenches further has a N-type base contact layer at a bottom thereof, and the lateral contact layer has less doping concentration than the base contact layer at bottom.”**

158. Claim 6 depends on Claim 1, which is discussed above in Section X(E)(1). The remaining elements of Claim 6 are disclosed in Kobayashi and Shiraishi. Kobayashi discloses a trench MOSFET with layers of a first conductivity type and second conductivity type opposite to the first conductivity type, along with specific embodiments of n-channel MOSFETs. *See, e.g.*, Ex. 1008 at Claim 1, [0062]. Kobayashi also discloses “inverting the conductive type, [such that] this invention is also applicable to a P-channel MOSFET structure.” Ex. 1008 at [0072]. Shiraishi similarly discloses a trench MOSFET with semiconductor layers of a first conductivity type and of a second conductivity type opposite to the first conductivity type, along with specific embodiments of an n-channel MOSFET. *See, e.g.*, Ex. 1009 at [0017]-[0028], [0067], Claim 1.

159. The POSITA would understand that there are only two conductivity types and would know how to alter a design to account for P-channel or N-channel MOSFET as needed.

7. Claim 7 is obvious over Kobayashi in light of Shiraishi and the knowledge of the POSITA

a. 7: “The trench MOSFET of claim 6, wherein further comprises a barrier metal layer and contact metal plugs.”

160. Claim 7 depends on Claim 6, which is discussed above in Section X(E)(6). The remaining elements of Claim 7 are disclosed in Kobayashi, as described above in relation to Claim 3. *See supra* Section (E)(3).

161. A POSITA would know that inverting the conductivity types simply allow the formation of either an N-channel MOSFET or a P-channel MOSFET. The POSITA would understand that the inversion of conductivity types is the fundamental basis in forming Complementary Metal-Oxide-Silicon (CMOS) Field Effect Transistors. The metallurgy for contacting and interconnecting the source and drain regions is the same for either N-channel MOSFET or P-channel MOSFET, including using the same conductive material for the barrier metal layer and the contact metal plugs.

8. Claim 8 is obvious over Kobayashi in light of Shiraishi and the knowledge of the POSITA

- a. 8: “The trench MOSFET of claim 7, wherein the barrier metal layer is Ti/TiN and the contact metal plug is Tungsten.”**

162. Claim 8 depends on Claim 7, which is discussed above in Section X(E)(7). The remaining elements of Claim 8 are disclosed in Kobayashi, as described above in relation to Claim 4. *See supra* Section (E)(4). The POSITA would understand that the inversion of conductivity types would not affect the previous disclosure and analysis. *See supra* ¶ 160.

9. Claim 9 is obvious over Kobayashi in light of Shiraishi and the knowledge of the POSITA

- a. 9: “The trench MOSFET of claim 8, wherein the source contact trench is selected from one of a vertical shape and a tapered shape.”**

163. Claim 9 depends on Claim 8, which is discussed above in Section X(E)(8). The remaining elements of Claim 9 are disclosed in Kobayashi, as described above in relation to Claim 5. *See supra* Section (E)(5). The POSITA would understand that the inversion of conductivity types would not affect the previous disclosure and analysis. *See supra* ¶ 160..

10. Combining Kobayashi and Shiraishi in light of knowledge of the POSITA

164. It is my opinion that it would have been obvious to a POSITA before the effective filing date of the '634 Patent (February 23, 2008) to combine

Kobayashi and Shiraishi to arrive at the subject matter of Claims 1-9, rendering those claims invalid under pre-AIA 35 U.S.C. § 103.

165. In particular, the POSITA would be motivated to combine the lateral contact layer and doping concentration profiles of Shiraishi with the MOSFET of Kobayashi to arrive at the subject matter of Claims 1-2, and therefore to dependent Claims 3-9.

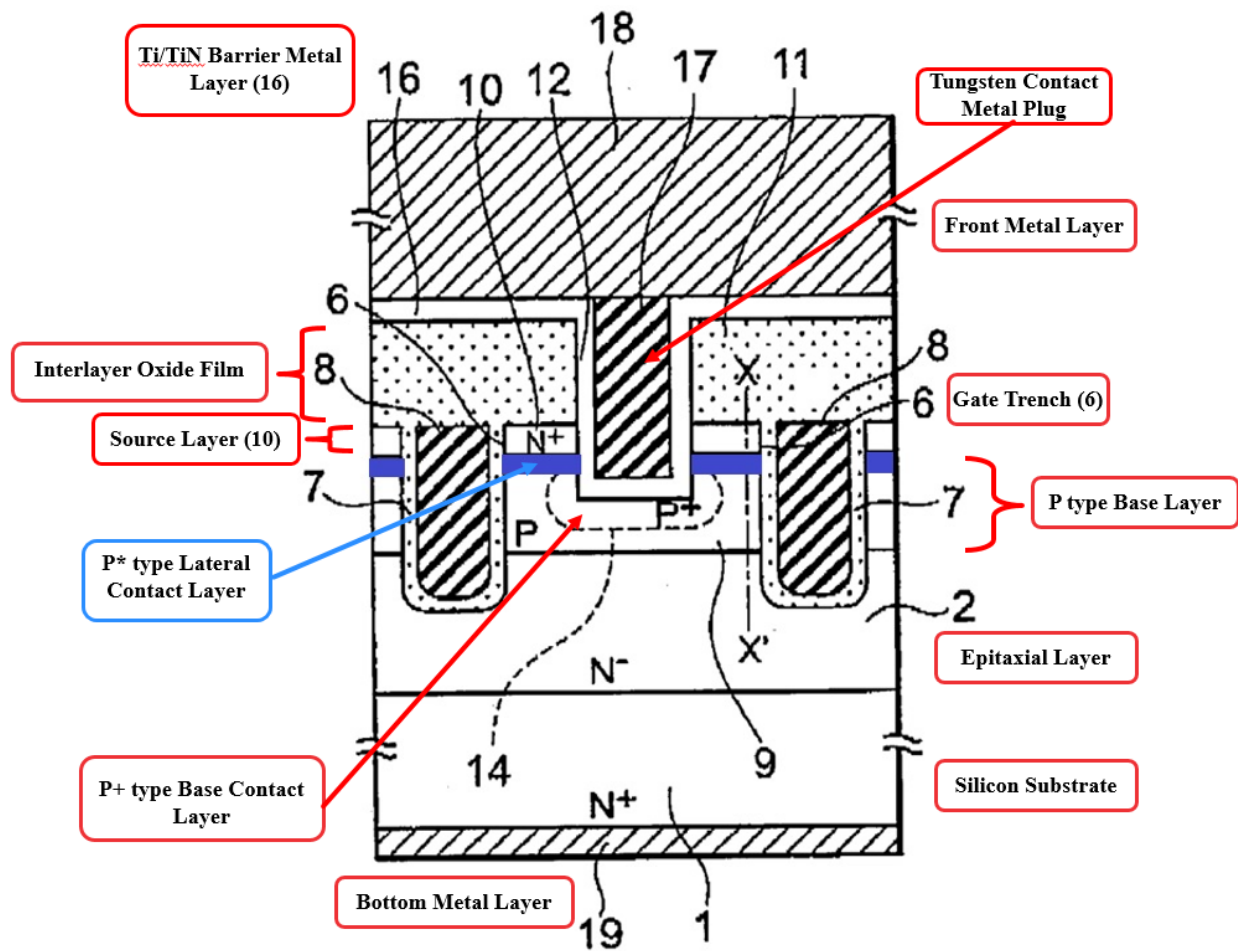
166. First, Kobayashi, Shiraishi, and the '634 Patent are analogous art that seek to solve similar problems. Kobayashi, Shiraishi, and the '634 Patent are in the same field of endeavor, *i.e.*, Vertical Power MOSFET structures, and the methods to improve the performance tradeoff in the ON-state (ON-Resistance and speed), and OFF-state (breakdown voltage). Moreover, Kobayashi, Shiraishi and the '634 Patent disclose a similar doping concentration engineering technique, *i.e.*, dopant ion implantation, that allows for the formation of a low resistance source contact, at the bottom of the base region and/or also on the sidewall of the trenched contact region, with minimal impact to the threshold voltage or the ON-Resistance of the Power MOSFET.

167. Second, Shiraishi expressly teaches a lateral contact layer along the entire sidewalls of the contact trench in the base layer that serves as “a punch-through stopper layer.” Ex. 1009 at Fig. 8; [0073], [0080], [0084]-[0085]. The POSITA would thus be motivated to combine the distinct lateral contact layer of

Shiraishi with P doping concentration that is greater than the P-type doping concentration of the underlying base layer but less than the P-type concentration of the base contact layer with the disclosure of Kobayashi to optimize the MOSFET and prevent punch-through.

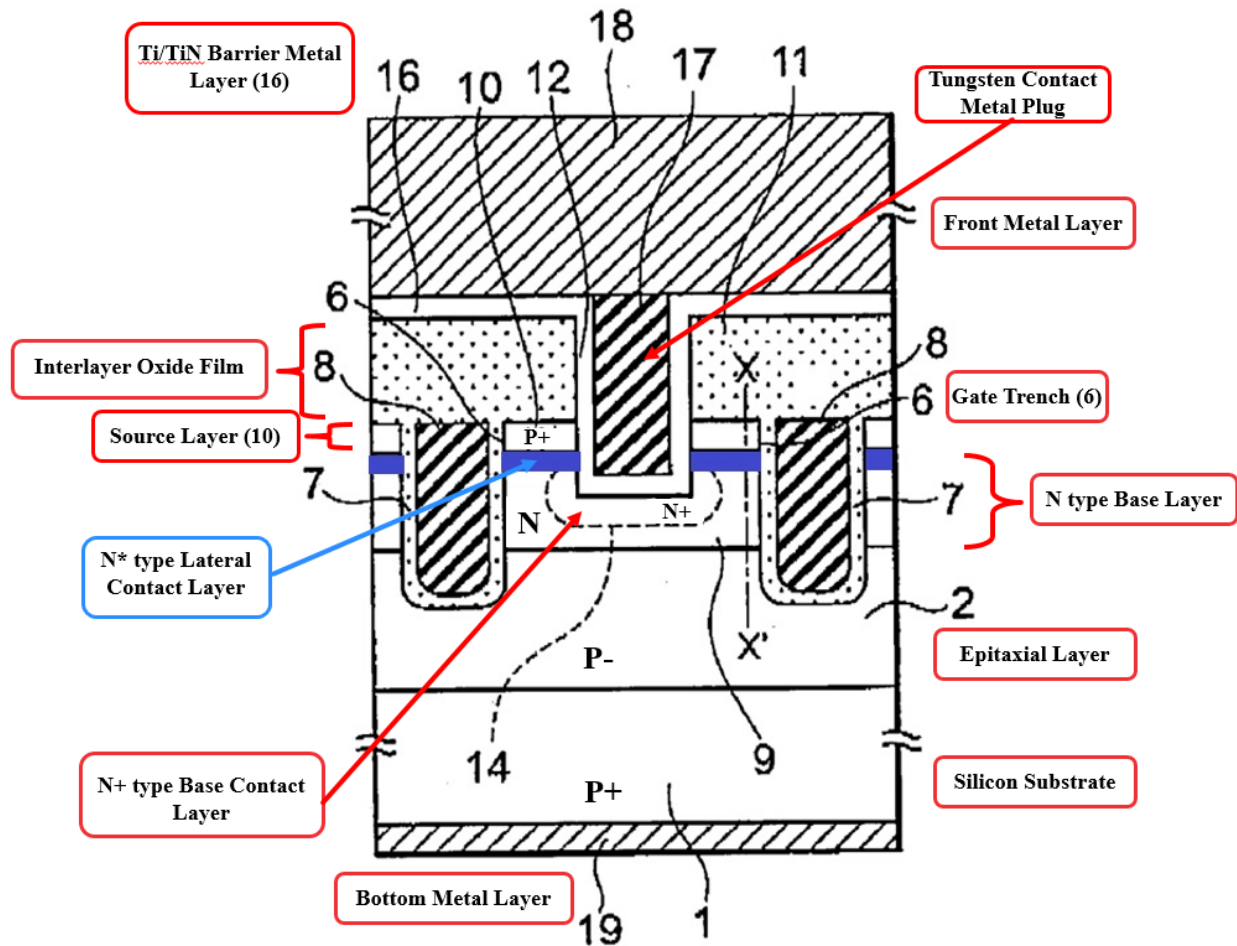
168. Third, Shiraishi expressly teaches the doping concentration profiles of the lateral contact layer and base contact layer that would prevent punch-through. Ex 1009 at Abstract, [0073]. Thus, the POSITA would be motivated to try these doping concentration profiles, as opposed to the doping dosing as disclosed in Kobayashi, to achieve an anti-punch-through result.

169. Accordingly, the combination of Kobayashi and Shiraishi renders obvious Claims 1-9, as illustrated below in a hypothetical diagram based on Kobayashi's Figure 5A with the addition of the lateral contact layer (in blue) according to disclosure in Shiraishi.



Kobayashi, Figure 5A (annotations added)

170. Below is the same hypothetical diagram but with inverted conductivity types, showing a p-channel MOSFET.



Kobayashi, Figure 5A (annotations added)

XI. OBJECTIVE INDICIA OF NON-OBVIOUSNESS

171. Having reviewed the file history and the other exhibits cited in this declaration, I am not aware of any objective indicia of non-obviousness for the claims of the '634 Patent.

XII. DECLARATION

172. I understand this declaration will be used as evidence in a contested case before the PTAB.

173. I am aware that willfully false statements in connection with this declaration are punishable by fine or imprisonment, or both under 18 U.S.C. § 1001 and may jeopardize the validity of the Petition. All statements herein are made of my own knowledge true and all statement made on information and belief are believed to be true.

I declare under penalty of perjury that the foregoing is true and correct.

Executed this 27th day of October, 2023 at Fremont, CA.

Respectfully Submitted,



Dr. David Liu