

EXHIBIT D

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UNITED STATES DISTRICT COURT
NORTHERN DISTRICT OF CALIFORNIA
OAKLAND DIVISION

ALPHA AND OMEGA SEMICONDUCTOR
LIMITED, and ALPHA AND OMEGA
SEMICONDUCTOR INCORPORATED,

Plaintiffs and Counter-Defendants,

v.

FORCE MOS TECHNOLOGY CO., LTD.,
Defendant and Counter-Plaintiff.

Case No. 4:22-cv-05448-HSG

**CORRECTED EXPERT REPORT AND
DECLARATION OF DEAN NEIKIRK,
Ph.D., REGARDING CLAIM
CONSTRUCTION**

CLAIM CONSTRUCTION DECLARATION
OF DEAN NEIKIRK, PH.D. (CORRECTED)

CASE No. 4:22-cv-05448-HSG

1 **I. INTRODUCTION**

2 1. I am submitting this report and declaration on behalf of Defendant and Counter-
3 Plaintiff Force MOS Technology Co., Ltd. (“Force MOS”) in connection with the above-captioned
4 case filed by Plaintiffs Alpha and Omega Semiconductor Limited, and Alpha and Omega
5 Semiconductor Incorporated (collectively, “AOS”). In particular, I am submitting this declaration
6 in connection with certain disputed terms of the patents-in-suit as part of the claim construction
7 proceedings in this litigation.

8 2. I understand that AOS has asserted the following patents in this litigation: U.S.
9 Pat. Nos. 7,511,361 (“the ’361 Patent”), 7,781,265 (“the ’265 Patent”), and 8,928,079 (“the ’079
10 Patent”) (collectively, “the AOS Asserted Patents”).¹ I understand that the patents that Force MOS
11 has asserted in this litigation include: U.S. Pat. Nos. 7,629,634 (“the ’634 Patent”) (“the Force
12 MOS Asserted Patents”).² Collectively, the AOS Asserted Patents and the Force MOS Asserted
13 Patents are referred to herein as the “patents-in-suit.”

14 3. I have reviewed and am familiar with the specification, claims, and prosecution
15 history of the patents-in-suit. I will cite to the specification of a U.S. Patent using the following
16 format: (Column: Line Number(s)).

17 4. I am not currently, nor have I ever been, an employee of Force MOS. I have
18 received no compensation for this declaration beyond my normal hourly compensation based on
19 my time actually spent analyzing the issues discussed herein. I will not receive any added
20 compensation based on the outcome of this proceeding or any other proceeding involving the
21 patents-in-suit (or related patents).

22 5. In forming my opinions expressed in this report, I have reviewed and, in some
23 cases, relied upon the documents and other materials cited below in preparation of this report. This
24 Report contains opinions I formed with respect to the subject matter of this proceeding based on

25
26 ¹ I also understand that AOS is asserting U.S. Patent No. 8,067,304, but I have not rendered
27 opinions regarding that patent at this time.

28 ² I also understand that Force MOS is asserting U.S. Patent No. 7,847,346 and 7,646,058, but I
have not rendered opinions regarding those patents at this time.

information available to date. I specifically reserve the right to formulate and offer additional opinions based on any additional information or discovery that may be provided or derived, and I likewise reserve the right to supplement my opinions based on future discovery or disclosures, future rulings, agreements between the parties, and additional evidence submitted by either party while this proceeding is pending. In particular, I have reviewed the parties' Patent Rule 4-2 disclosures of proposed claim constructions and supporting evidence. However, I understand that the parties may alter or provide further explanations of their claim constructions or identify additional supporting or rebuttal evidence, including providing expert testimony. Accordingly, I reserve the right to address and respond to AOS's (or AOS's expert's) theories to the extent they further elaborate upon the meaning of the disputed claim terms or provide further evidence supporting AOS's claim construction positions or rebutting Force MOS's claim construction positions.

II. SUMMARY OF OPINIONS TO BE EXPRESSED

6. As discussed in further detail below, it is my opinion that AOS's proposed constructions of the disputed terms are not supported by the evidence, and that Force MOS's proposed constructions of the disputed terms are more consistent with the intrinsic and extrinsic evidence as would be understood by a person of ordinary skill in the art at the time of the invention.

III. PROFESSIONAL BACKGROUND AND QUALIFICATIONS

7. My qualifications are most accurately reflected in my *curriculum vitae*, which is attached to this report as Appendix A. The following is a brief summary of some of my relevant experience and qualifications.

8. I have over 30 years of experience in electronic devices and systems, including the methods used to fabricate integrated circuits and devices.

9. I received a B.S. degree in 1979 in physics from Oklahoma State University, and an M.S. degree and a Ph.D. degree in 1981 and 1984, respectively, in applied physics from the California Institute of Technology.

1 10. Each of my academic degrees involved significant studies in solid state physics,
2 semiconductor devices, electrical engineering, electronic systems, electromagnetics, optics, radio
3 frequency systems, and antennas. For example, courses relating to these fields that I took include
4 two years of study in electromagnetics and optics, one year of study in solid state and
5 semiconductor physics, as well as four years of graduate research in electronic devices, antenna
6 design, antenna fabrication, microwave systems, and optical systems. My Ph.D. thesis was on the
7 design and fabrication of high frequency electromagnetic detectors and imaging arrays, including
8 research on integrated-circuit fabrication, antennas, sensors, and packaging. I designed and
9 fabricated the first monolithic integrated-circuit imaging array for use at wavelengths in the far
10 infrared (sometimes referred to as the terahertz) region of the electromagnetic spectrum. This
11 research work required the fabrication, testing, and field placement of devices with many output
12 channels, presenting a significant challenge (at that time) in packaging. I personally developed
13 packages for my devices, and personally performed the packaging itself. At that time the most
14 common method of connection made use of wirebonding, which I personally performed.

15 11. I am currently a Life Senior Member of the Institute of Electrical and Electronics
16 Engineers ("IEEE"). From March 1991 to October 1994, I served as an Associate Editor for the
17 IEEE publication called "IEEE Transactions on Education." I also served as a member of the
18 Editorial Board on the IEEE Transactions on Microwave Theory and Techniques in the 1990-2000
19 timeframe.

20 12. I have almost 40 years of experience on the faculty of the University of Texas at
21 Austin. My work as a professor began in 1984, when I joined the University of Texas at Austin as
22 an assistant professor. In 1988, I became an associate professor, and became a full professor in
23 1992.

24 13. My research over the last forty years has concentrated heavily in the areas of
25 electromagnetics, microwave engineering, microelectronics, semiconductor devices, integrated
26 circuit (IC) fabrication, and new sensors. This research work has been funded by many agencies,
27 focusing on the fabrication and modeling of semiconductor devices, electromagnetic devices and
28

1 detectors, chemical sensors, temperature sensors, proximity sensors, and pressure sensors, as well
2 as research on the high frequency properties of transmission lines, RF devices, and infrared to
3 terahertz detectors for use in focal plane imaging arrays. My research related to the development
4 of new chemical sensors (an “electronic taste” sensor) was selected for a commercialization
5 venture between The University of Texas and two outside startup companies.

6 14. Over the years, I have also taught a variety of electrical engineering courses at the
7 University of Texas. These include Integrated Circuit Fabrication, VLSI Fabrication Techniques,
8 Ultra Large Scale Integrated Circuit Fabrication Techniques, Integrated Circuit
9 Nanomanufacturing Techniques, Electromagnetics in Packaging, Simulation Methods in
10 CAD/VLSI, Micro-Electromechanical Systems, Electromagnetic Engineering, and Microwave
11 and Radio Frequency Engineering. I have also taught several continuing education courses in these
12 fields.

13 15. In 1985, I established the Microelectronics Fabrication Teaching Laboratory at The
14 University of Texas at Austin, which continues to this day to provide undergraduate and graduate
15 students with hands-on experience in integrated circuit fabrication. I have taught many courses in
16 integrated-circuit fabrication, microwave devices, integrated circuit packaging, electromagnetics,
17 computer aided design methods for circuit simulation, sensors of all sorts, and
18 microelectromechanical systems.

19 16. I conducted research with students and research scientists in the
20 Microelectromagnetics Research Group in the Microelectronics Research Center at The University
21 of Texas at Austin for 37 years. For over ten years, I also served as the Graduate Advisor of the
22 Department of Electrical and Computer Engineering at the University of Texas at Austin, as well
23 as serving for over five years as an Associate Chairman of the Electrical and Computer
24 Engineering Department at The University of Texas at Austin. I also served as Associate Dean of
25 Graduate Studies from 2014 to 2021.

26 17. In addition to my work at The University of Texas at Austin, I have done part-time
27 consulting work since 1984 as an independent consultant to the industry for technical projects and
28

1 as a technical expert in legal cases. I am a senior member of the IEEE. Through my work on
2 sensors, electronic systems, and innovations in other related fields, I have been named an inventor
3 on 17 U.S. patents. These are summarized in my curriculum vitae.

4 18. As a result of my professional education and experience, I am qualified to render
5 opinions in the areas of semiconductors and their fabrication, and in particular, the subject matter
6 of the patents-in-suit.

7 **IV. RELEVANT LEGAL PRINCIPLES AND UNDERSTANDINGS**

8 19. I am not an attorney and I offer no opinions on the law. Despite this, counsel has
9 informed me of the legal standards that apply to the issues of claim construction, indefiniteness,
10 and other issues related thereto. I have applied these standards in arriving at my conclusions.
11 Accordingly, each of the opinions I have reached are based on my understanding of these legal
12 standards and their relevant factors.

13 20. I understand that claims are interpreted from the perspective of one of ordinary skill
14 in the art at the time of the invention, and I have considered such an interpretation in forming my
15 opinions on infringement.

16 21. I further understand that for claim construction purposes, the principal sources of
17 information are the claims, the specification, patent drawings, and the prosecution history, which
18 can be referred to as the patent's intrinsic evidence. Extrinsic evidence, such as expert and inventor
19 testimony, dictionaries, and learned treatises, may also be relied upon; however, such evidence is
20 viewed as less significant than the intrinsic record in determining the meaning and scope of the
21 claims. I understand that, when interpreting the claims of the patents, one of the relevant doctrines
22 is the doctrine of "claim differentiation," under which it is presumed that there is a difference in
23 meaning and scope when different words or phrases are used in separate claims. However, I
24 understand that differently worded claims and claim terms may ultimately be construed to have
25 the same meaning and/or scope when the specification or prosecution history provides otherwise,
26 thus overcoming the presumption of claim differentiation.

27 22. I understand that claims are interpreted from the perspective of a person of ordinary
28

1 skill in the art (*i.e.*, “POSA”) at the time of the alleged invention and not from the perspective of
2 a judge, a lay person, or those skilled in different arts.

3 23. I further understand that the characteristics of this hypothetical person having
4 ordinary skill in the art should be defined before engaging in any claim construction, infringement
5 or invalidity analysis. Factors that can be considered in determining the level of ordinary skill in
6 the art include (1) the educational level of the inventor(s); (2) the type of problems encountered in
7 the art; (3) the prior art solutions to those problems; (4) the rapidity with which innovations are
8 made; (5) the sophistication of the technology; and (6) the educational level of active workers in
9 the field. As discussed below in Section V, I have considered each of these factors and determined
10 the level of ordinary skill for the patent in this case.

11 24. I have been informed by counsel and understand that a patent is presumed valid,
12 and that, for the purposes of this proceeding, invalidity (including indefiniteness) must be
13 established by clear and convincing evidence, which is higher than the normal preponderance of
14 the evidence standard. I have been informed that a preponderance of the evidence means that the
15 fact that is to be proven is more likely true than not; *i.e.*, that the evidence in favor of that fact
16 being true is sufficient to tip the scale, even if slightly, in its favor. I understand that, in contrast,
17 to decide whether the fact has been proven by clear and convincing evidence one must have been
18 left with a clear conviction that the fact has been proven. Clear and convincing evidence is a lower
19 standard than the “beyond a reasonable doubt” criminal standard (which is not used in or relevant
20 to patent cases) but higher than the preponderance of the evidence standard that applies to issues
21 like infringement and damages. I understand that clear and convincing evidence means that there
22 is a high probability that a fact is true.

23 25. I understand that, to satisfy the definiteness requirement of 35 U.S.C. § 112(2), a
24 patent must conclude with one or more claims that particularly point out and distinctly claim what
25 the applicant regards as the invention.

26 26. I understand that the inquiry with respect to indefiniteness is whether the patent
27 claim, viewed in light of the specification and prosecution history, informs those skilled in the art
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1 about the scope of the invention with reasonable certainty. I understand that in evaluating the
 2 question of whether the specification and the prosecution history provide adequate detail for a
 3 POSA to understand the objective boundaries of a claim term, that an evaluation should be made
 4 to determine whether the term provides enough certainty to a POSA to understand its bounds when
 5 read in light of the specification and the claim as a whole.

6 27. I understand that the definiteness requirement does not require that the claim have
 7 absolute or mathematical precision. However, I understand that when a claim uses a word or term
 8 of degree, to be definite, the patent must provide objective boundaries to a POSA. For example, I
 9 understand that a term of degree fails to provide sufficient notice of its scope if it depends on the
 10 unpredictable vagaries of any one person's opinion.

11 28. I understand that when a claim uses subjective language or terms of degree, to be
 12 definite, the written description of the patent must provide sufficient guidance regarding the
 13 claim's scope as to that subjective language.

14 29. I understand that a claim may be held indefinite where the claim language might
 15 mean several different things and no informed and confident choice is available among the
 16 contending definitions.

17 30. I understand that examples in the specification may adequately provide certainty as
 18 to the scope of a claim, but that it is improper to cull a single example from the specification (i.e.
 19 to reject or disregard all other potential embodiments that the patent contemplates) and to use that
 20 single example to provide the exclusive definition of a claim term.

21 31. I understand that even if a claim term's definition can be reduced to words, the claim
 22 is still indefinite if a person of ordinary skill in the art cannot translate the definition into
 23 meaningfully precise claim scope.

24 **V. LEVEL OF ORDINARY SKILL IN THE ART**

25 32. I have studied the patents-in-suit and believe that the technology described therein.
 26 Based on my review of the patents-in-suit, the other materials referenced in this report, and my
 27 experiences, and applying the factors set forth in the legal standards section above, I believe that
 28

a person of ordinary skill in the art (“POSA”) would have had a minimum of a master’s degree in electrical engineering, or a related field, along with at least two years of professional experience in semiconductor device design and fabrication. Additional significant experience in the field could substitute for some degree of the formal education, and vice-versa.

33. Consistent with the summary of my relevant experience provided above and reflected in my attached *curriculum vitae*, my skill exceeds that of a person of ordinary skill in the art. Beyond the experiences and expertise gained through my formal education, I have approximately 40 years of technical experience related to semiconductor design and fabrication.

VI. MATERIALS CONSIDERED

34. In preparing this report, I have reviewed—among other materials—the patents-in-suit and their file histories, the parties’ most recent infringement and invalidity contentions, the parties’ Patent Rule 4-2 disclosures of proposed claim constructions and evidence, and the most recent complaint and answer.

35. In forming my opinions, I also relied on my education, experience, and knowledge of the industry.

36. In forming my opinions, I have also considered any documents cited in this report and declaration.

37. In forming my opinions, I have also considered the understanding of a person of ordinary skill in the art (“POSA”) around the time of the invention of the patents-in-suit.

VII. BACKGROUND OF THE PATENTS-IN-SUIT

A. The AOS Asserted Patents

i) The ‘361 and ‘265 Patents

38. The ‘361 and ‘265 Patents relates to a dual-flat non-leded (DFN)³ semiconductor package for use in a power MOSFET⁴. ‘361 Patent, Abstract; ‘265 Patent, Abstract; ‘361 Patent

³ A dual flat non-leded package is a small rectangular or square semiconductor package that is flat (i.e. which is designed to be applied to the surface of a single side of a circuit board, rather than using holes through the circuit board) and has no leads, instead using pads or lands along two sides of the package for an electrical connection to the circuit board.

⁴ MOSFET is short for metal-oxide-semiconductor field-effect transistor. MOSFETs are a type of transistor—a semiconductor device used to switch or amplify an electrical signal. Power

1 at 1:15-50.⁵

2 39. The '361 and '265 Patents identify the thermal and electrical performance of a DFN
3 power MOSFET as being issues raised by the prior art. '361 Patent at 1:38-. In particular, because
4 package resistance contributes the total electrical resistance Rds(on) of a MOSFET (i.e. drain-
5 source on resistance, which affects the maximum current rating of a MOSFET), it is desired to
6 reduce package resistance. *Id.* at 39-43. However, package resistance depends on the amount and
7 diameter of bond wires. *Id.* at 47-50. The specification characterizes the prior art as having "only
8 11 narrow and short bond wires [] for connecting source leads [] to a semiconductor device" and
9 "consequently does not provide reduced Rds(on)." *Id.* 1:51-57.

10 40. The '361 and '265 Patents purport to solve that problem by providing a DFN
11 package with source and gate lead bonding areas of "increased area," which allows "for an
12 increased number of source bonding wires having a 2 mil diameter." '361 Patent, Abstract; '265
13 Patent, Abstract; '361 Patent at 1:66-2:19; 3:59-65.

14 41. I understand that AOS has asserted claims 1-7 of the '361 Patent and claim 1 of the
15 '265 Patent in this litigation. I also understand that claim 1 is the sole independent claim of the
16 '361 Patent, and claim 1 is similarly the sole independent claim of the '265 Patent.

17 ii) The '079 Patent

18 42. The '079 Patent relates to MOS devices (e.g. MOSFETs) with low injection diodes,
19 including gate trenches and active region contact trenches. '079 Patent, Abstract. In the claimed
20 embodiments, a layer of body region separates the active region contact electrode from the
21 epitaxial layer, and a low injection diode is formed below a body/drain junction. *Id.*; *id.* at claim
22 1, Figs. 1D-1F, 5:26-44.

23 43. The '079 Patent identifies a problem with the prior art that in such devices, there is
24

25 MOSFETs are used to handle significant power levels preferably with high switching speed,
26 good efficiency, and with low voltage drop. Applications of Power MOSFETs include power
27 supplies, power amplifiers, DC-to-DC converters, voltage regulators, motor controllers, and
28 various other applications in numerous types of electronic devices.

⁵ My citations to specific portions of the '361 Patent should be understood as also encompassing the corresponding portions of the '265 Patent.

a tradeoff between performance and breakdown voltage, and that reducing the value of Rds(on) (i.e. drain-source on resistance, which affects the maximum current rating of a MOSFET), either the channel length can be reduced (i.e. using a shallower source and body) and/or the density of the cells per unit area of the MOSFET can be increased by reducing the cell size. '079 Patent at 1:33-45. However, channel length is limited by punch-through, and cell density is limited by manufacturing technology and the limitations of good contact to the source and body regions. *Id.* at 41-45. And, as cell density increases (thereby increasing the total number of power cells), this leads to an increase in total gate capacitance. *Id.* Thus, the '079 Patent identifies it would be desirable to reduce Rds(on) and gate capacitance.

44. The '079 Patent purports to solve these problems using, *inter alia*: anti-punch-through implants which permits shallow trench / short-channel devices. '079 Patent at 3:62-4:27. The '079 Patent also discloses Schottky diodes parallel with the body diode which reduce body diode forward drop and make the MOSFET more efficient. '079 Patent at 4:28-44. And the '079 Patent discloses, as an alternative to a Schottky diode, using a thin layer of body region to separate the body of the active region contact trench from the epitaxial layer, thereby forming a low injection diode below the body/drain junction and ensuring that the layer is almost depleted in reverse bias but not depleted in forward bias. '079 Patent at 5:26-44.

45. I understand that AOS has asserted claims 1-3, 5-14, and 16-22 of the '079 Patent in this litigation. I also understand that claims 1 and 13 are the independent claims of the '079 Patent.

B. The AOS Asserted Patents

i) The '634 Patent

46. The '634 Patent relates to trench MOSFETs with source contact trenches, where each of the source contact trenches has a lateral contact layer at a sidewall thereof. '634 Patent, Abstract.

47. The '634 Patent recognizes that, in a traditional trench MOSFET design, the sidewall of the source contact trench has no ohmic contact with the contact metal plug which

1 results in poor performance during Unclamp Inductance Switching test. ‘634 Patent at 1:35-38. .
 2 When P base resistance from the channel to the contact metal plug is high enough, device
 3 destruction can occur. *Id.* at 1:38-42.

4 48. The ‘634 Patent addresses the problem of the prior art by applying the P*-type
 5 lateral contact layer to parts of the sidewall of the source contact trench, where the P* has less
 6 doping than the P+ base contact layer which is located at the bottom of the source contact trench.
 7 ‘634 Patent at 2:1-11.⁶ The ‘634 Patent describes optimizing the P*-type lateral contact layer
 8 doping concentration by having the ohmic contact to the barrier metal layer/the contact metal plug
 9 without significantly increasing threshold voltage of the device. *Id.*

10 49. I understand that Force MOS has asserted claims 1-9 of the ‘634 Patent in this
 11 litigation. I also understand that claim 1 is the sole independent claim of the ‘634 Patent.

12 VIII. CONSTRUCTION OF CERTAIN DISPUTED TERMS

13 A. “sidewalls of said trenches in said base layer are covered by the lateral 14 contact layer” (‘634 Patent, claim 1)

AOS’s Proposed Construction	Force MOS’s Proposed Construction
entire sidewalls of source contact trenches are covered by the lateral contact layer	Plain and ordinary meaning / no express construction required

17 50. In my opinion, Force MOS’s proposed construction is the appropriate construction

18 ⁶ P-type and N-type are types of doping of semiconductors. Doping is the process of introducing
 19 impurities into semiconductor material (e.g. silicon) to affect its electrical properties. N-type
 20 semiconductors are created by doping a semiconductor with an electron donor element (e.g.
 21 phosphorus or arsenic). N refers to the negative charge of an electron. P-type semiconductors
 22 are created by doping a semiconductor with an electron acceptor element (e.g. boron or gallium).
 23 P refers to the positive charge of a hole—a hole is quasiparticle denoting the lack of an electron
 24 at a position where one could exist in an atom or atomic lattice. At a junction of P-type and N-
 25 type semiconductor materials (a so called p-n junction), current can only readily pass in only one
 26 direction—what is called forward biased—i.e. electrons pass from the N-type to the P-type
 27 material. N+ doping is used to refer to material which has been more highly doped with electron
 28 donor impurities than standard N-type doping, while N- doping is used to refer to material which
 is more lightly doped with electron donor impurities standard N-type doping. Similarly, P+
 doping is used to refer to material which has been more highly doped with electron acceptor
 impurities than standard P-type doping, while P- doping is used to refer to material which is
 more lightly doped with electron acceptor impurities standard P-type doping. The ‘634 Patent
 uses the “P*” notation (e.g. as used in P*-type lateral contact layer (209)) to refer to P-type
 doping which is less than P+ doping (e.g. as used in P+ type base contact layer (208)) but more
 than standard P-type doping (e.g. as used in P-type base layer (205)). ‘634 Patent at 2:1-11 (“the
 lateral contact layer P* has less doping concentration than the P+ base contact layer at the source
 contact trench but higher doping concentration than P-base layer”), 3:50-4:6.

1 because it most naturally aligns with the intrinsic and extrinsic evidence as would be viewed by a
2 POSA at the time of the invention.

3 51. The central dispute apparent from the parties' constructions is whether the *entire*
4 base layer portion of the sidewalls of the source contract trenches must be covered by the lateral
5 contact layer, as AOS proposes, or whether less than *entire* coverage can meet the claim, consistent
6 with the plain meaning of this term (and therefore also consistent with Force MOS's construction).
7 Another apparent dispute is whether, assuming the "entire" limitation is added to the claim (as
8 AOS's construction provides), whether the "lateral contact layer" must actually apply to the *entire*
9 sidewall as AOS proposes, or only the base layer.

10 52. As a threshold issue, in my opinion, nothing in the language of claim 1 of the '634
11 Patent requires that the *entire* sidewalls of the source contact trenches, or even the entire portion
12 of the base layer adjacent to the sidewalls, be covered in the lateral contact layer. Indeed, that is
13 evident from the fact that AOS's proposed construction essentially repeats the claim language but
14 adds the word "entire" and deletes the phrase "in said base layer."

15 53. Notably, it appears that AOS's construction—which not only adds "entire" to the
16 claim language, but also removes "in said base layer" from the claim language appears to require
17 that the *entire* sidewall of the trench, not just the portion of the sidewall in the base layer, must be
18 covered by the lateral contact layer. However, this is plainly inconsistent with the language of
19 claim 1 which only requires that "sidewalls of said trenches *in said base layer* are covered by the
20 lateral contact layer." '634 Patent, cl. 1. Moreover, requiring the entire sidewall, not just the
21 portion in the base layer, be covered by the lateral contact layer would also exclude all the disclosed
22 embodiments of the '634 Patent, which depict the source layer (206) and the interlayer oxide film
23 (207) contacting the side wall of the source contact trench above where the lateral contact layer
24 (209) ends. '634 Patent, Figs. 2E-2G, 3B. This is further demonstrated in the following annotated
25 version of Fig. 2E of the '634 Patent, which shows that, in the described embodiments, the lateral
26 contact layer covers less than the entire sidewalls of the source contact trenches:⁷

27
28 ⁷ As shown in this annotated version of Fig. 2E, A POSA would understand that the source
contact trench (and thus its sidewalls) encompasses the entire depth of the indentation depicted in

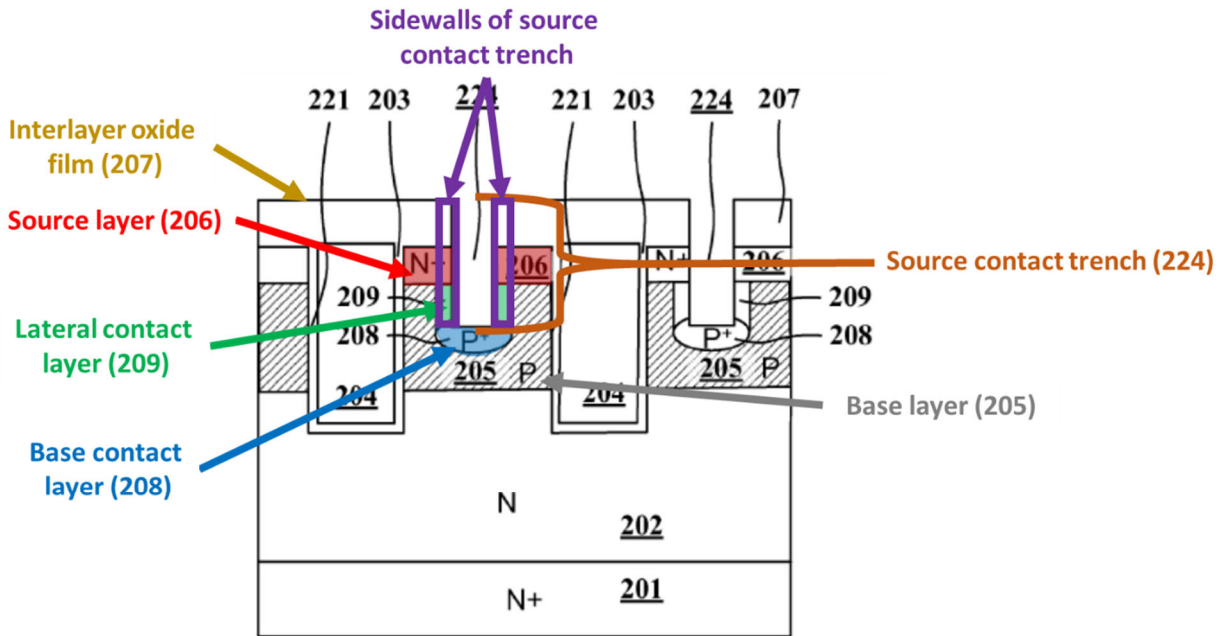


Fig. 2E

As shown, in the preferred embodiments, the lateral contact layer does not cover the portions of the sidewalls at the source layer (206) or the inter layer oxide film (207). I understand that, under the law of claim construction, a claim construction that would exclude all of the embodiments of an invention disclosed in the specification is rarely, if ever, correct. In my opinion, AOS's construction would do exactly that, and therefore a POSA would be unlikely to believe it is correct.

54. However, even assuming that AOS's proposed construction were corrected to add back in the claim language's "in said base layer" (i.e. requiring the *entire portion* of the source contact trench's sidewalls in the base layer to be covered by the lateral contact layer), AOS's construction would still be incorrect, in my opinion. I have also reviewed the specification of the '634 Patent, and in my opinion, its disclosures contradict AOS's proposed construction. For

Fig. 2E (i.e. from immediately above the base contact layer 208 up to the top of the opening in the interlayer oxide film 207). Indeed, the '634 Patent teaches that the trench is etched through interlayer oxide film (207), source layer (206) and into P-type base material (205). '634 Patent at 3:46-49. This is also reflected in the text of claim 1, which recites that the each of the "source contact trenches" is "formed on the top of said interlayer oxide film [(207)]" and "extend[s] downwardly through said source layer [(206)] to a portion of said base layer [(205)]."

example, the Abstract states that “each of the source contact trenches has a lateral contact layer *at a sidewall* thereof.” In my opinion, a POSA would understand this broad language of “at a sidewall” as not requiring any minimum degree of coverage of the sidewall, and therefore inconsistent with AOS’s addition of “entire” to the claim. Similar language appears in the “Summary of the Invention” of the ‘634 patent. ‘634 Patent at 1:65-67 (“each of the source contact trenches has a lateral contact layer at a sidewall thereof”). And, the detailed description of the preferred embodiments also repeats this broad “at a sidewall” language. ‘634 Patent at 5:9-12 (“The P+-type base contact layer (208) and the P*-type lateral contact layer (209) are formed at the bottom and sidewall of the source contact trenches (224), respectively.”).

55. Figures 2E and 3B of the ‘634 Patent are the figures where the implantation of a lateral contact layer into the sidewalls of a source contract trench is depicted in an embodiment of the ‘634 Patent. Although Figures 2E and 3B of the ‘634 Patent include a lateral contact layer (209) covering the entire base layer portion of the sidewall of the depicted source contact trench, in my opinion, a POSA would understand those figures as merely depicting an idealized application of the invention in one embodiment (e.g. where the doping by ion implantation is able to successfully dope all of the sidewall between the source layer and the base contact layer). In my opinion, a POSA would not understand the disputed claim term as limited to what is shown in the depicted embodiments of Figs. 2E and 3B. Indeed, Figs. 2E and 3B are discussed in the portion of the specification entitled “Detailed Description of the Embodiments.” ‘634 Patent at 2:51-54, 3:50-4:6. The beginning of this section of the ‘634 Patent expressly states that “The present invention is described by the following specific embodiments” but “[t]he present invention can also be implemented with different embodiments.” ‘634 Patent at 2:55-63. I also note that the same section of the ‘634 Patent concludes with the statement that “Although various embodiments are specifically illustrated and described herein, it will be appreciated that modifications and variations of the present invention are covered by the above teachings and are within the purview of the appended claims without departing from the spirit and intended scope of the invention.” ‘634 Patent at 5:30-35. It is my understanding that, under the law of claim construction, it is

generally improper to use claim construction to simply import aspects of the preferred embodiments into the claims. In my opinion, nothing in the discussion of Figs. 2E and 3B in the specification of the '634 Patent indicates that these figures depict the only contemplated embodiments of the invention of the '634 Patent.

56. Additionally, the method by which the lateral contact layer is formed in the preferred embodiment described in the '634 Patent is also inconsistent with AOS's proposed construction requiring the "entire" sidewall of the source contact to be covered. In particular, the '634 Patent describes that "Referring to FIGS. 2E and 3B, thereafter, another implantation procedure of BF2 with angle ranging from 45 to 80 degree respective to the surface of the epitaxial layer (202) and dose ranging from $1\text{E}14$ to $4\text{E}14\text{ cm}^{-2}$, and another activation by heat treatment are carried out to form a P*-type lateral contact layer (209) at the sidewall of the source contact trench (224) and corresponding to the P-type base layer (205) while the implantation angle of the implantation procedure respective to the surface of the epitaxial layer (202) is less than the implantation angle of the implantation procedure of the P+-type base contact layer (208)." '634 Patent at 3:50-65. As depicted in Fig. 3B, a POSA would understand that the degree of coverage of the sidewall would depend on various implementation issues, including both the capabilities of the tooling applying the ion implantation, the angle of ion implantation, and the dimensions of the source contact trench. And, notably, nothing in the '634 Patent describes the invention as having a specific source contact trench depth. Accordingly, in my opinion, a POSA would understand that the described method of creating the lateral contact layer would necessarily not cover the entire sidewalls of the base layer in at least some embodiments of the invention.

57. I understand the prosecution history of a patent is also relevant to claim construction, but that because the prosecution history represents an ongoing negotiation between the PTO and the applicant, rather than the final product of that negotiation, it often lacks the clarity of the specification and thus may be less useful for claim construction purposes. I understand that AOS identifies the following portions of the prosecution history of the '634 Patent as supporting its claim construction: 7/28/09 Notice of Allowability (Reasons for Allowance), 7/28/09

Examiner-Initiated Interview Summary, and U.S. Patent No. 6,888,196. I have reviewed these materials, and the rest of the prosecution history of the '634 Patent, and in my opinion, nothing in the prosecution history supports AOS's proposed construction.

58. In particular, I understand that in the July 28, 2009 Notice of Allowability, the examiner of the '634 Patent provided statements regarding why the examiner believed the invention of the '634 Patent was patentable, but I understand such a statement does not necessarily reflect the patentee's understanding or agreement with the reasons for patentability or the scope of the invention. In that statement, the examiner stated that "Claim 1 limits the trenched MOSFET to having a trench in which the base and the entire sidewall are covered with the lateral contact layer. Kobayashi (US 6,888,196) covers the base and only a portion of the trench sidewall with the lateral contact layer." 7/28/2009 Notice of Allowability at p. 3. Concurrent with that notice of allowability, the examiner filed an interview summary that identified "the general nature of what was discussed" as "Discussed novelty of invention (lateral contact covering entire trench sidewall), prior art and claim language on 7/15/09 resulting in proposed claim language (via e-mail) 7/20/09, and further telephone conversation of 7/20/09." 7/28/2009 Examiner's Statement. Again, I understand that this is the examiner's statement characterizing what was discussed, rather than a characterization or admission of the scope of the claim by the patentee.

59. Notably, prior to the notice of allowability, the examiner had not issued any office action rejecting the claims, and thus the patentee never had an opportunity to file a formal response to address the examiner's position regarding Kobayashi or the scope of the claims of the application that issued as the '634 Patent. Additionally, the only change to the claims of the '634 Patent compared to those as originally filed with the application came in an examiner's amendment that was also filed on July 28, 2009. A comparison of the original text of claim 1 and claim 1 as amended by the examiner is as follows:

Original Text of Claim 1 of Appl. No. 12/036,243	Claim 1 of '634 Patent After Examiner's amendment
1. A trenched MOSFET with trenched source contact, comprising: a semiconductor region, further comprising a silicon substrate, a epitaxial layer	1. A trenched MOSFET with trenched source contact, comprising: a semiconductor region having a drain region, a body region and a source region,

1	corresponding to the drain region of the	comprising, a silicon substrate, an epitaxial
2	trenched MOSFET, a base layer	layer corresponding to said drain region
3	corresponding to the body region of the	disposed on the top of said silicon substrate, a
4	trenched MOSFET, and a source layer	base layer corresponding to said body region
5	corresponding to the source region of the	disposed on the top of said epitaxial layer, and
6	trenched MOSFET;	a source layer corresponding to said source
7		region disposed on the top of said base layer;
8	an interlayer oxide film formed on the source	a front metal layer formed on the upper
9	layer;	surface of said semiconductor region;
10	a front metal layer formed on a upper surface	an interlayer oxide film formed between said
11	of the semiconductor region;	source layer and said front metal layer,
12	a back metal layer formed on a lower surface	
13	of the semiconductor region;	a bottom metal layer formed on the lower
14		surface of said semiconductor region;
15	a plurality of trenched gates formed to reach	a plurality of trenched gates covered by said
16	the epitaxial layer through the source layer	interlayer oxide film are formed on top of said
17	and the base layer, and is covered by the	source layer extending downwardly through
18	interlayer oxide film; and	said base layer to a portion of said epitaxial
19		layer;
20	a plurality of source contact trenches formed	and a plurality of source contact trenches
21	to reach the base layer through the interlayer	formed on the top of said interlayer oxide film
22	oxide film and the source layer, and is	extending downwardly through said source
23	covered by the front metal layer;	layer to a portion of said base layer; wherein
24		the sidewalls of said trenches in said base
25	wherein the silicon substrate, the epitaxial	layer are covered by the lateral contact layer;
26	layer, the base layer, and the source layer are	wherein the bottom base of said trenches in
27	stacked in sequence; and each of the source	said base layer are covered by the base
28	contact trenches has a lateral contact layer at a	contact layer.
	sidewall and a base contact layer at bottom of	
	source contact trench thereof.	

60. Furthermore, a track changes comparison of the language of the original versus issue claim is as follows:

1
2
3 1. A trenched MOSFET with a trench source contact, comprising:
4 a semiconductor region, further having a drain region, a body region and a source region,
5 comprising a silicon substrate, an epitaxial layer corresponding to the said drain region
6 disposed on the top of the trenched MOSFET, said silicon substrate, a base layer
7 corresponding to the said body region disposed on the top of the trenched MOSFET, said
8 epitaxial layer, and a source layer corresponding to the said source region disposed on
9 the top of the trenched MOSFET, said base layer, a front metal layer formed on the upper
10 surface of said semiconductor region;

11 an interlayer oxide film formed on the between said source layer, and said front metal
12 layer,

13 a front metal layer formed on an upper surface of the semiconductor region;

14 a back a bottom metal layer formed on the lower surface of the said semiconductor
15 region;

16 a plurality of trench gates formed to reach the epitaxial layer through the source layer
17 and the base layer, and is covered by the said interlayer oxide film; are formed on top of
18 said source layer extending downwardly through said base layer to a portion of said
19 epitaxial layer;

20 and

21 a plurality of source contact trenches formed to reach on the base layer through the top of
22 said interlayer oxide film and the source layer, and is extending downwardly through said
23 source layer to a portion of said base layer; wherein the sidewalls of said trenches in said
24 base layer are covered by the front metal layer;

25 wherein the silicon substrate, the epitaxial layer, the base layer, and the source layer are
26 stacked in sequence; and each of the source contact trenches has a lateral contact layer
27 at a sidewall and a base contact; wherein the bottom base of said trenches in said base
28 layer at bottom of source are covered by the base contact trench thereof.

61. As is evident from the above comparison, the extensive changes in the text of claim 1 made in the examiner's amendment clearly addressed matters unrelated to the extent of the lateral contact layer's coverage of the source contact trench's sidewalls. In my opinion, a POSA would not read these changes as clearly evidencing that the patentee had agreed to disclaim source contact sidewalls not entirely covered by the lateral contact layer (or having a base layer of the sidewall not entirely covered by the lateral contact layer). Rather, in my opinion, a POSA would not see clarity in these amendments, but the overall impression to a POSA would appear to be stylistic

changes to the structure of the claim.

62. I have also reviewed U.S. Patent No. 6,888,196 (“Kobayashi”), which was cited in the examiner’s reasons for allowance and is identified by AOS as supporting its construction. Kobayashi is generally directed to a vertical MOSFET with trench gates. Kobayashi at Abstract. The structures of Kobayashi are manifestly different from those of the ‘634 Patent in a number of ways relevant to this claim term. Kobayashi’s source contact holes—which the examiner apparently analogized to the ‘634 Patent’s source contact trenches—are not described as trenches. *E.g.*, Kobayashi at Abstract, 2:33-38, 3:18-23, 6:35-42, 11:50-53. This is in contradiction to Kobayashi’s description of its “trench gates” as being “formed in the trenches.” Kobayashi at Abstract.

63. Moreover, the ‘634 Patent describes the “lateral contact layer” as a “P*-type” layer which “has less doping concentration than the P+ base contact layer at the source contact trench but higher doping concentration than P-base layer to achieve ohmic contact between the P*-type region, which is lower doping concentration than P+-type region, and the contact metal plug while threshold voltage V_{th} is not significantly affected by P*-type region.” ‘634 Patent at 2:1-11. As the ‘634 Patent describes, this addresses the prior art’s problem of “[t]he sidewall of source contact trench has no ohmic contact (due to low doping concentration of P base) with the contact metal plug resulting in poor ruggedness performance during UIS (Unclamp Inductance Switching) test” and “[a] parasitic N+/P/N is easily turned on when P base resistance from channel to the contact metal plug is high enough, causing [the] device [to be] destroyed.” ‘634 Patent at 1:33-51.

64. An example of a prior art trenched MOSFET is depicted in Fig. 1 of the ‘634 Patent, which shows a P+ region at the bottom of the source contact trench, and a P region adjacent to the sidewalls of the source contact trench for the portions below the N+ doped source layer. ‘634 Patent, at Fig. 1. The prior art MOSFET depicted in Fig. 1 of the ‘634 Patent is substantially identical to Kobayashi Figs. 7D, 8A-8C, particularly in regards to the dopings of the source contact hole/trench sidewalls and bottom. That is, like the prior art of Fig. 1 of the ‘634 Patent—and unlike the other figures or descriptions of any of the embodiments of the ‘634 Patent—Kobayashi’s

embodiments of Figs. 7D and 8A-8C simply depict a conventional P⁺ doped region at the bottom of a source contact hole, with a P region contacting the sidewalls of the source contact hole. *See also* Kobayashi at 5:50-51 (“the base contact layer is not present on the Side wall of the contact”). Similarly, the doping process that creates the P⁺ doped region in Kobayashi depicts ion implantation with BF₂⁺ ions at 90 degrees (Kobayashi, Fig. 9A), rather than the angled implantation that the ‘634 Patent uses for creating the P* lateral contact layer (‘634 Patent at Fig. 3B, 3:55-65). Kobayashi does describe a “second embodiment” (Kobayashi at 11:5-12:63, Figs. 10, 11A-11D) but in this embodiment, again there is no lateral contact layer created by doping any portion of the sidewall. Indeed, Kobayashi’s Figs. 9B, 10, and 11A-11D show the same doped regions as Kobayashi’s first embodiment and the prior art of Fig. 1 of the ‘634 Patent (i.e. a P⁺ type doping at the bottom of the source contact, a P-type body near the source contact’s side walls, and an N⁺ source layer near the side walls but above the P-type body) *See also* Kobayashi at 11:54-57 (“The depth d of the contact hole 12 is selected to be similar to that in the first embodiment and the base contact layer 14 is not formed on the side wall of the contact hole 12.”). Compared to Kobayashi’s first embodiment, the second embodiment of Kobayashi merely adds a “silicide layer 15 [which] is formed on the bottom and the side wall of the contact hole.” Kobayashi at 11:8-13, Figs. 10, 11A-11D (element 15). This process does involve ion implantation at an angle other than 90 degrees (Kobayashi, Fig. 9B, 11:23:-27), but unlike the ‘634 Patent, the off-angle ion implantation in Kobayashi’s second embodiment is only of Arsenic ions for the purpose of amorphization of the silicon prior to titanium sputtering (which thereby creates a titanium silicide). Kobayashi at Fig. 9B, 11:16-20.⁸ A POSA would not understand Kobayashi’s silicide layer as comparable to the P* lateral contact layer disclosed in the ‘634 Patent, as the silicide layer is a method of facilitating low resistance ohmic contact which is distinct from increasing the concentration of P-doping. In any event, a POSA would not consider the silicide layer of Kobayashi’s as a basis for importing the “entire” limitation into the construction of this term (as AOS proposes). In particular, the silicide layer (15) in Kobayashi is depicted extending

⁸ Amorphization is the process of causing some of the silicon to become amorphous, i.e. lacking a regular defined crystal structure.

over *more of the* source contact hole than the preferred embodiments of the ‘634 Patent, i.e., Kobayashi’s silicide layer 15 covers not only the Kobayashi’s P-type doped base layer (9) but also but also Kobayashi’s N⁺ source layer (10). Kobayashi, Figs. 10, 11A-11D.

65. In short, in my opinion, a POSA would not clearly understand the examiner’s statements regarding having the lateral contact layer cover the “entire” sidewall as a characteristic of the ‘634 Patent or a basis for distinguishing Kobayashi. Nothing in Kobayashi appears to even arguably correspond to a sidewall partially covered by a lateral contact layer. Moreover, as discussed, the examiner’s statement, literally understood, would appear to require the entire sidewall of the source contact trench (rather than just the entire portion of the base layer) to be covered by the lateral contact layer. But, as discussed, that would be expressly contrary to the language of claim 1 of the ‘634 Patent and would exclude all of the described embodiments of the ‘634 Patent. I understand that, as a matter of claim construction law, a disclaimer in the prosecution must be made by the patentee and must be clear and unambiguous. In my opinions, the examiner’s statements during prosecution of the ‘634 Patent are none of these—they are far less clear than the language of the specification and claims of the ‘634 Patent which do not include the “entire” limitation of AOS’s construction.

66. Accordingly, in my opinion, Force MOS’s construction is correct because it accurately captures how a POSA would interpret this claim term in light of the background knowledge of a POSA and the disclosures of the specification (i.e. that the word “entire” should not be imported into the claim”).

B. “the source lead bonding area and the gate lead bonding area being of increased area” (‘361 Patent, cl. 1) / “the gate lead bonding area and the source lead bonding area being of increased area” (‘265 Patent, cl. 1)

AOS’s Proposed Construction	Force MOS’s Proposed Construction
Plain Meaning: the source lead bonding area and the gate lead bonding area are larger than in conventional semiconductor packages to allow an increased number of bonding wires to be bonded thereto	Indefinite

67. In my opinion, this term is indefinite because a POSA, reviewing the intrinsic

evidence, would not be able to understand its scope (and thus the scope of the claims including the term) with reasonable certainty. In particular, I believe that a POSA would understand “being of increased area” as a term of degree that necessarily calls for a comparison against some baseline (i.e., increased compared to what area?). However, as explained in further detail below, neither the background knowledge of a POSA nor the specifications of the ‘361 or ‘265 Patents provide sufficient guidance to a POSA to determine what is the relative point of comparison for the size of gate lead and source lead bonding areas.

68. The ‘265 Patent issued as a divisional application of U.S. Appl. No. 11/150,489 (*see* ‘265 Patent cover page at (60) – Related U.S. Application Data), which is the application which resulted in the ‘361 Patent (*see* ‘361 Patent cover page at (21) – Appl. No.). I understand that the ‘361 Patent’s specification is therefore part of the intrinsic record of the ‘265 Patent. It also appears that the ‘265 and ‘361 Patents share substantially identical specifications (other than the claims and Abstracts). Thus, I will use citations to the ‘361 Patent’s specification for analyzing both patents, but the corresponding portions of the ‘265 Patent’s specification are equally applicable to the ‘265 Patent.

69. Also, as an initial matter, a POSA would recognize these two claim terms: “the source lead bonding area and the gate lead bonding area being of increased area” (‘361 Patent, cl. 1) / “the gate lead bonding area and the source lead bonding area being of increased area” (‘265 Patent, cl. 1) to be substantively identical, as the only literal difference in the claim text is the order of “gate lead bonding area” and “source lead bonding area” has been flipped in the ‘265 Patent’s claim. However, because both “gate lead bonding area” and “source lead bonding area” are joined on either side of an “and” in each claim term, both claim terms require that both the source lead bonding area and the gate lead bonding area “be” “of increased area.”

70. Since the claims define the scope of the invention, I understand a POSA would look to the claims for guidance regarding the meaning of the terms therein. However, no guidance is provided regarding these claim terms in any of the claims of the ‘361 or ‘265 Patents. There is simply no indication or even hint in the claims as to what the relevant point of comparison is that

the source and gate lead bonding areas are increased compared to.

71. The specification of the '361 and '265 Patents similarly provides inadequate guidance regarding the relevant point of comparison for the "being of increased area" limitations. The Abstract is not helpful as it similarly repeats the claim language without providing the point of comparison. '361 Patent at Abstract ("the source lead bonding area and the gate lead bonding area being of increased area"); '265 Patent at Abstract ("the gate lead bonding area and a source lead bonding area being of increased area;"). Similarly, the "Summary of the Invention" section is also not helpful because it simply repeats the unhelpful claim language without identifying the point of comparison: "gate lead bonding area and a source lead bonding area, the gate lead bonding area and a source lead bonding area being of increased area," "the source lead bonding area and the gate lead bonding area being of increased area," and "the first and source lead bonding areas and the first and second gate lead bonding areas being of increased area." '361 Patent at 2:1-4, 2:13-15, 2:23-26.

72. The "Background of the Invention" provides some clues as to these limitations, but is not enough (even in conjunction with the rest of the specification) to provide reasonable certainty. In particular, the "Background of the Invention" states that:

Chip resistance depends upon the wafer process technology used to fabricate the chip and die size while package resistance depends upon the quantity, diameter and length of bond wires used to bond internal chip bonding areas to external package leads. By increasing the amount of bond wires and/or their diameters, total Rds(on) can be reduced dramatically. QFN and DFN packages of the prior art suffer from the disadvantage of having high Rds(on).

A prior art 6×5 mm DFN package 700 is shown in FIG. 7. A leadframe 710 includes a narrow source bonding area 720 and a narrow gate bonding area 730. The narrow source bonding area 720 of DFN package 700 allows for only 11 narrow and short bonding wires 760 for connecting source leads 735 to a semiconductor die 750 and consequently does not provide reduced Rds(on).

'361 Patent at 1:43-57. This section of the specification indicates a purpose of increasing the source and gate lead bonding areas: decreasing Rds(on) (drain-source on resistance, which affects the maximum current rating of a MOSFET). And this section explains how the '361 Patent

purports to achieve that goal: “increasing the amount of bond wires and/or their diameters.” *Id.* And the patent identifies the size of the gate lead and source lead bonding areas of the prior art as an impediment to that goal (i.e. that the prior art’s “narrow” source bonding area and “narrow” gate bonding area “allows for only 11 narrow and short bonding wires.”) *Id.* However, nothing in this passage tells us the actual size of the prior art’s “narrow” source and gate bonding areas, or how much the ‘361 and ‘265 Patents have increased from those prior art bonding areas. I also do not believe the disclosure regarding “11 narrow and short bonding wires” to be sufficient. Indeed, “narrow” and “short” in this context are vague terms of degree.

73. Moreover, a POSA would not understand the independent claims of the ‘361 and ‘265 patents (i.e. claim 1) to be limited to any particular number of bonding wires. Indeed, this is demonstrated by the fact that one of the dependent claims do recite particular minimum numbers of bond wires. ‘265 Patent, cl. 2 (“wherein coupling the die source bonding area to the source lead gate bonding area and a source lead bonding area comprises using at least 21 source bonding wires”). Moreover, as the examiner acknowledged during prosecution, Figures 2A-3A of the ‘361 Patent do not have 21 source bonding wires. ‘361 Patent, Figs. 2A, 3A; May 16, 2007 Office Action response at p. 2. Indeed, the various disclosed embodiments depict a wide variation in the number of bonding wires. *See* ‘361 Patent at Fig. 2A (seven source lead bond wires), Fig. 4 (five source lead bond wires), Fig. 8 (twenty-one source lead bond wires), Fig. 9 (six source lead bonding wires per MOSFET in two MOSFET package), Fig. 10 (four source lead bonding wires per MOSFET in two MOSFET package), Fig. 11 (three source lead bonding wires per MOSFET in two MOSFET package), Fig. 12 (same as Fig. 11). Thus, a POSA would recognize that the number of bonding wires cannot act as a stand-in to provide reasonable certainty for the “being of increased area” limitations.

74. And, because the passage in the Background of the Invention itself teaches that there is a relationship between the required minimum size of the gate/source bonding areas and *both* the number and thickness of the bonding wires (‘361 Patent at 1:43-57), a POSA would understand that a particular number of bonding wires cannot act as a stand-in to provide reasonable

certainty (i.e. because for the same sized gate/source bonding area, you could accommodate more or fewer wires by varying the wire thickness). Additionally, a POSA would not understand the decrease in $R_{ds(on)}$ referenced in this passage ('361 Patent at 1:43-57) to be able to act as a stand-in to provide reasonable certainty for these claim terms, because the specification teaches that $R_{ds(on)}$ is not *directly* affected by the gate/source lead bonding areas but the number and thickness of the bond wires (which as discussed above, also cannot act as an adequate stand in to provide reasonable certainty). And, nowhere in the specification is there any specific disclosure regarding the amount of reduction in $R_{ds(on)}$ provided by the invention.

75. The rest of the specification (i.e. the figures and the "Detailed Description of the Invention") likewise fails to help to provide sufficient guidance regarding the scope of these claim terms, disclosing:

- "An increased source bonding area provides for an increased number of source bonding wires having a 2 mil diameter" ('361 Patent at 3:61-63).
- "The source lead 230 (FIG. 2A) may be larger than in conventional semiconductor packages to enable the use of an increased number of source wires 285 which preferably are formed from gold or copper. Increasing the number of source wires 285 advantageously decreases the semiconductor package 200 resistance significantly." ('361 Patent at 4:21-30).
- "In yet another aspect of the invention, a 6×5 mm DFN semiconductor package generally designated 890 (FIG. 8) may include a leadframe 891 having a source bonding area 892 of increased area. A gate bonding area 893 may also be of an increased area. The source bonding area 892 allows for the use of 21 source bonding wires of 2 mil diameter rather than the conventional package which allows for the use of 11 source bonding wires." ('361 Patent at 5:5-12).
- "In another aspect of the invention, a 2×5 mm DFN semiconductor package generally designated 900 (FIG. 9) may include a leadframe 910 having a pair of source bonding areas 920 a and 920 b of increased area. Gate bonding areas 930 a and 930 b may also be of an increased area." ('361 Patent at 5:13-17).
- "In yet another aspect of the invention and with reference to FIG. 10, a 3×3 mm DFN semiconductor package generally designated 1000 may include a leadframe 1010 having a pair of source bonding areas 1020 a and 1020 b of increased area. Gate bonding areas 1030 a and 1030 b may also be of an increased area." ('361 Patent at 5:32-35).

- 1 • “In another aspect of the invention and with reference to FIG. 11, a 3×3 mm DFN
2 semiconductor package generally designated 1100 may include a leadframe 1110
3 having a pair of source bonding areas 1120 a and 1120 b of increased area. Gate
4 bonding areas 1130 a and 1130 b may also be of an increased area.” (‘361 Patent
5 at 5:51-54).
- 6 • “In yet another aspect of the invention and with reference to FIG. 12, a 2×3 mm
7 DFN semiconductor package generally designated 1200 may include a leadframe
8 1210 having a pair of drain pads 1250 a and 1250 b and a pair of corresponding
9 source bonding areas 1220 a and 1220 b of increased area. Gate bonding areas 1230
10 a and 1230 b may also be of an increased area.” (‘361 Patent at 6:5-11).

8 In my opinion, none of these passages provide reasonable certainty regarding the “being of
9 increased area” limitations. As a threshold issue, the discussions regarding Figs. 9, 10, 11, and 12
10 are unhelpful because they generally use the same unhelpful language of the claim (i.e. they merely
11 state that source and gate bonding areas are of “increased area” without any other details or point
12 of comparison). The discussion of Fig. 2A merely notes that the increased bonding areas can allow
13 more wires and decreases $R_{ds(on)}$, which as discussed above, does not provide reasonable
14 certainty. The discussion of Fig. 2A also mentions “conventional semiconductor packages,” but
15 does not identify what those packages are or the dimensions of their source or gate lead areas. A
16 POSA would be well aware that, at the time of filing of the ‘361 and ‘265 Patents, there were large
17 variations in the packaging of semiconductors, including MOSFETS. *See, e.g.*, US20040041242,
18 Figs. 1-4; Fairchild Semiconductor Power MOSFET Selection Guide (September 2001) (attached
19 as Exhibit 1 hereto); R. Gulino, AN1703 APPLICATION NOTE GUIDELINES FOR USING
20 ST’S MOSFET SMD PACKAGES (June 2003) (attached as Exhibit 2 hereto).⁹ A POSA would
21 also be well aware that a number of factors could affect the relative sizes of the source and gate
22 lead areas. *See also* ‘361 Patent at Figs. 8-12 (reflecting the diversity of different die configurations
23 for MOSFETs). Indeed, a fundamental lack of clarity with respect to these limitations is that, if a
24 POSA was examining a new design for a MOSFET (rather than an improvement for an existing
25 MOSFET design that existed prior to the ‘361 and ‘265 patents), they would not know what

26 ⁹ Although the ‘361 and ‘265 Patents are specifically directed to DFN MOSFETs, a POSA would
27 be well aware that the same variations in packages of dual lead surface-mount MOSFETs
28 would also apply to DFN MOSFETs (e.g. package size, number of MOSFETs per package,
number and location of drain, source, and gate lead-outs, etc.).

relevant design to compare it to. That is, even prior to the '361 and '265 Patent, too many factors affect the choice of source and gate lead bonding area sizes for a POSA to be certain of a particular size of a source and gate lead bonding area appropriate for a particular MOSFET die and package, and thus no clear base line to determine whether a new design has an "increased" area.

76. The discussion at '361 Patent at 3:61-63 indicates that the preferred embodiment uses 2 mil diameter bond wires, which is another detail that is not disclosed in the Background of the Invention. Similarly, the discussion of Fig. 8 ('361 Patent at 5:5-12) discloses 2 mil diameter bond wires, and also that the invention permits an increase in the number of bond wires from "11 source bonding wires" in a "conventional package" to "21 source bonding wires of 2 mil diameter." '361 Patent at 5:9-12 However, in my opinion, a POSA would not understand these disclosures as providing reasonable certainty, even in connection with the other disclosures in the patent. Notably, there is no disclosure of the diameter (or even the shape or any other dimensions) of the bond wires in the "conventional package which allows for the use of 11 source bonding wires," thus there is no ability to use calculations to determine the relevant point of comparison for the "being of increased area" limitations.¹⁰ A POSA would understand that the diameter of that point of comparison would be necessary in understanding what is the *area* of the source bonding area being increased *from*. Thus, these passages do not provide even the minimum facts a POSA would need to begin the process of engaging in calculations to estimate the relative area of the point of comparison "conventional" semiconductor package source and gate lead bonding areas.

77. Moreover, even if the claims were limited to a particular number of bond wires (which, as discussed, there is no indication of that other than claim 2 of the '265 patent), and assuming 2 mil diameter of bond wires in both the invention and in the comparison "conventional" prior art package, there would be various other factors that could affect the *minimum* required space in a bonding area to accommodate those bond wires, such as the overall die size and layout

¹⁰ A POSA would understand the specification as disclosing the "2 mil" figure as only being used in an embodiment of the invention, and not disclosing the "2 mil" diameter bond wires as being used in the "conventional" prior art package. Indeed, the '361 Patent discloses "increasing the amount of bond wires **and/or their diameters**." '361 Patent at 1:47-50; *see also* '361 Patent at 1:54-55 (characterizing the prior art 11 bond wire embodiment as having "narrow" bond wires).

of the source areas on the semiconductor die, the material which the bond wires are made of, the amount of bond wire deformation at the location of connection, and the desired performance properties of the MOSFET—none of which are adequately specified in these passages (or anywhere else in the ‘361 or ‘265 patents). And, in any event, a POSA would recognize that the *minimum* required space for a specific number of bonding wires would not allow bond wires to act as a stand in to provide reasonable certainty for these claim terms because any given semiconductor package design could provide more than the minimum source lead bonding area required for a given number of source bond wires—and, as discussed, the claim term calls for an examination of *area* not the number of bond wires.

78. Additionally, notably, there is no discussion in the specification regarding the invention allowing for an increase or other improvement in the number of bond wires for the *gate* lead bonding area, even though the claim term requires the gate lead bonding area to be of “increased area” as well. Indeed, the figures of the specification consistently show one bond wire at each gate bonding area, in *both* the prior art and in the disclosed embodiments of the invention. *Compare* Fig. 7 (one wire in prior art Fig. 7 connecting gate bonding area 730 to the rectangular gate area on semiconductor die 750) *with* Fig. 8 (one wire in embodiment of Fig. 8 connecting gate bonding area 893 to the rectangular gate area of the semiconductor die); *see also* Fig. 2A (showing one bond wire connecting the gate area on top of the semiconductor die to the gate lead 240), Fig. 4 (same as Fig. 2A), Fig. 9 (in a two-MOSFET package, one wire between each gate and gate bonding area 930, 930b), Fig. 10 (in a two-MOSFET package, one wire between each gate and gate bonding areas 1030a, 1030b), Fig. 11 (in a two-MOSFET package, one wire between each gate and gate bonding areas 1130a, 1130b), Fig. 12 (in a two-MOSFET package, one wire between each gate and gate bonding areas 1230a, 1230b). That is, even if the number of bonding wires could act as a stand-in to provide reasonable certainty for the “source lead area” “being of increased size”—in my opinion it cannot—the number of bond wires cannot act as a stand-in for the “gate lead area” “being of increased size” because the specification teaches that the number of bond wires connected to the gate lead area appears to remain the same compared to the prior art (i.e. the

increase in the gate lead bonding area size does not correspond to an increase in the number of bond wires connected to the gate lead bonding area).

79. I have also examined the various figures of the specification, but, in my opinion, they also fail to provide reasonable certainty regarding the scope of these terms. In particular, Fig. 7 is identified as the schematic representation of a “prior art” package. ‘361 Patent at 3:43-44. This is the “prior art 6×5 mm DFN package 700” with “11 narrow and short bonding wires” I discuss above. ‘361 Patent at 1:51-57.¹¹ Figs. 8-12 are identified as schematic representation of semiconductor packages of the invention and provide a top down view. *Id.* at 3:45-55, Figs. 8-12. Similarly, Figs. 3A, 3B, 4, and 5A are representations of the semiconductor packages from an isometric perspective. *Id.* at 3:28-40. In totality, these figures appear to show a wide variation in the shapes of the source and gate lead bonding areas in the disclosed embodiments of the invention. Most of them are not useful because they are not comparable to the disclosed prior art, as they use different package sizes and layouts. *Compare, e.g.*, Fig. 7 (prior art 6x5mm DFN package) to Fig. 9 (2x4 mm DFN package). The only disclosed embodiment which appears directly comparable to the prior art is Fig. 8, as both Fig. 7 and Fig. 8 are 6x5 mm DFN packages. ‘361 Patent at 3:44-48.

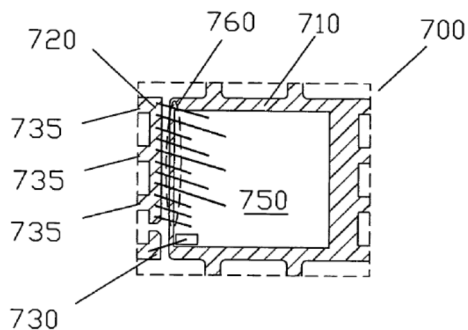


Fig 7

Prior Art

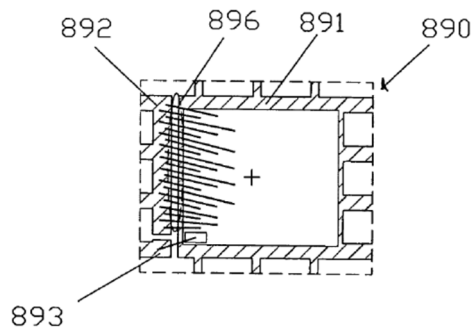


Fig 8

Comparing Figs. 7 and 8, it would be evident that the gate bonding areas (730 in Fig. 7 and 893 in Fig. 8) are of different shapes, with the gate bonding area 730 in Fig. 7 being overall more “L” shaped and the gate bonding area 893 in Fig. 8 being more rectangular in shape. However, it

¹¹ Figs. 1A and 1B are also identified as prior art (‘361 Patent at 3:18-21), but those figures do not adequately show the source or gate lead bonding areas for evaluation by a POSA.

would not be clear to a POSA from simply examining the two figures (without measurement) what the areas of either figure's gate bonding area is. As to the source bonding areas (720 in Fig. 7 and 892 in Fig. 8), they both generally appear to have the same overall shape, with the bonding areas in Fig. 8 perhaps being somewhat wider (extending overall slightly more in the left to right direction and having a slightly smaller gap between the bottom portion of the source bonding area and the top portion of the gate bonding area in the depicted figures). However, again, it would not be clear to a POSA from simply examining the two figures (without measurement) what the areas of either figure's source bonding area is. Notably, I observe no disclosure in the specification that any of the figures in the specification are drawn to scale, and thus I understand, as a matter of claim construction law, that it would be considered improper to actually attempt to measure the diagrams to attempt to determine an area. Also, examining the other figures (e.g. Figs. 9-12), it is apparent that the specification does not limit the source or gate bonding areas to any particular shape. Similarly, the claims recite "increased area," not a particular shape. Thus, in my opinion, a POSA would not understand the shape of the source or gate bonding area as acting as a stand in to provide reasonable certainty for the "being of increased area" limitation.

80. Finally, I have also reviewed the prosecution histories of the '361 and '265 Patent, but they do not provide any additional certainty regarding the scope of these terms. During the prosecution of the '361 Patent, the examiner issued a restriction without a rejection. November 28, 2006 Office Action. The patentee then elected the set of claims drawn to the semiconductor device, rather than the method of making the semiconductor device. *Id.*; December 22, 2006 Election Response. The examiner then issued another restriction requirement without rejection. March 16, 2007 Office Action. The patentee then elected the claims corresponding to the embodiment of Figures 2A and 3A. April 19, 2007 Election Response. The examiner then issued a rejection for some but not all claims, rejecting then-pending claims 1 and 5-11 as anticipated by U.S. Pub. No. 2004/0004272 ("Luo"). May 16, 2007 Office Action. The examinee responded by attempting to distinguish Luo as not disclosing a dual flat non-leaded package, but did not make substantive amendments to the claims. Sep. 20, 2007 Response to Office Action. The examiner

1 then issued an office action again rejecting the claims over Luo. Feb. 25, 2008 Office Action. The
 2 patentee again attempted to distinguish Luo as not having dual flat non-leaded package and
 3 amended the claims to emphasize the dual flat non-leaded package. June 2, 2008 Response to
 4 Office Action. The examiner then issued an advisory action that the amendment was not sufficient
 5 for patentability. July 28, 2008 Office Action. The patentee then filed a request for continued
 6 examination. August 29, 2008 Request for Continued Examination. Subsequently, the examiner
 7 issued an office action allowing the elected claims without further explanation. November 17,
 8 2008 Notice of Allowance at pp. 2-3. Thus, there was no substantive discussion of the “being of
 9 increased area” limitation by the patentee during the prosecution of the ‘361 Patent. The
 10 prosecution of the ‘265 Patent was similar with the examiner issuing a restriction requirement
 11 without a rejection (Jan. 25, 2010 Office Action), the patentee electing one claim set (Feb. 11,
 12 2010 Election), and the examiner then allowing the claims without any rejection and without
 13 substantive discussion of the “being of increased area” limitation (April 16, 2010 Notice of
 14 Allowance).

15 81. I have also reviewed the Luo reference (U.S. Pub. No. 2004/0004272) which was
 16 applied during prosecution of the ‘361 Patent. In my opinion, that reference (and the examiner’s
 17 rejections applying it) also do not provide reasonable certainty for this claim term. Luo is another
 18 AOS patent, but with different listed inventors than the ‘361 and ‘265 Patents. Luo is directed to
 19 MOSFETs and the problem of package resistance (and resulting heat) and inductance as density
 20 increases. Luo at [0001] and [0002]. Luo purports to address that problem “by giving up some of
 21 the real estate reserved for the silicon or die to re-distribute a bonding area, such as for the source
 22 or other heavy current loaded terminal” and “contemplates an ‘L’-shaped bonding area, a ‘C’-
 23 shaped bonding area, a ‘J’-shaped bonding area and/or an I shaped bonding area or any
 24 combination thereof.” Luo at [0013]-[0014]. Like the ‘361 and ‘265 Patents, Luo presents a
 25 number of figures showing different configurations of semiconductor packages of the prior art
 26 (Luo Figs. 1-3) and of the disclosed embodiments (Luo Figs. 4-19). Although Luo discloses a
 27 wide variety of bonding area *shapes*, Luo does not recite any specific disclosure of the actual
 28

“area” of any of the gate or source lead bonding areas. Accordingly, in my opinion, Luo (and the examiner’s rejections over Luo) do not provide reasonable certainty regarding the scope of these claim terms. Luo also teaches spreading bond wires further apart to reduce mutual coupling inductance, further showing that are and bond wire count are not substitutes for one another. Luo at [0009].

C. “the thickness of the layer of body region is substantially less than the depth of the active region contact trench” (’079 Patent, cls. 1, 13)

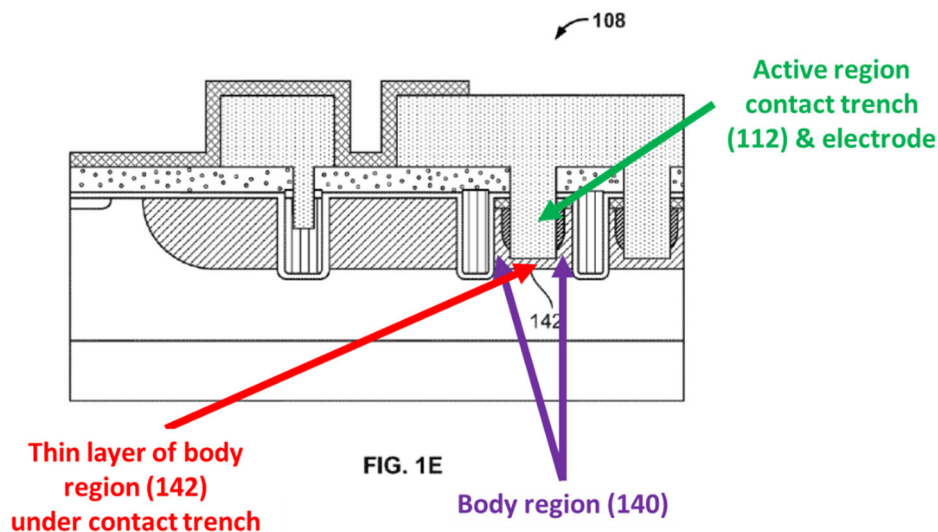
AOS’s Proposed Construction	Force MOS’s Proposed Construction
Plain Meaning: the thickness of the layer of body region is substantially less than the depth of the active region contact trench, where the thickness of the layer of the body region is measured from the bottom of the active region contact trench to the bottom of the body and the depth of the active region contact trench is measured from the top surface of the substrate to the bottom of the active region contact trench	Indefinite

82. In my opinion, this term is indefinite because a POSA, reviewing the intrinsic evidence, would not be able to understand its scope (and thus the scope of the claims including the term) with reasonable certainty. In particular, I believe that a POSA would understand that the term “substantially” in the context of these terms is a term of degree. However, as explained in further detail below, neither the background knowledge of a POSA nor the specification of the ’079 Patent provide sufficient guidance to a POSA to determine what thickness of body region under the active region contact trench is required, i.e. how much “less” than the depth of the active region contact trench may the thickness of the layer of body region be without being “substantially less.”

83. I understand that terms of degree, including the word “substantially,” do not necessarily render a claim indefinite. Rather, I understand evaluating the meaning and definiteness of a term of degree requires examination of the background knowledge of a POSA and the disclosures of the specification. I understand that the word “substantially,” when used in a claim, can denote either language of approximation or language of magnitude. In my opinion, a POSA

would recognize the use of “substantially” immediately followed by the word “less” in this claim term to convey language of magnitude, i.e. the thickness of the layer of body region must not just be *less* than the depth of the contact trench, but it must be *substantially less*. However, rather than provide helpful guidance to a POSA in understanding the scope of “substantially” in this limitation, the ‘079 Patent only demonstrates the lack of reasonable certainty around the scope of this term.

84. As discussed, the specification of the ‘079 Patent describes two general categories of embodiments: embodiments which include a body region under the active region contact trench (‘079 Patent, Figs. 1D-1F), and embodiments which do not, i.e. which have unconnected body regions on either side of the trench (‘079 Patent, Figs. 1A-C, 4U, 5-10).¹² However, the independent claims of the ‘079 Patent are only directed to the first set of embodiments, i.e. those with a layer of body region under the active region contact trench and electrode. ‘079 Patent, cl. 1, 13 (“a layer of body region separates the active region contact electrode from the epitaxial layer”). This is shown in the following annotated version of Fig. 1E of the ‘079 Patent:



85. As shown in this figure, the ‘079 Patent describes the embodiments of Figs. 1D-1F as having a “a thin layer of body region 142 [which] separates the bottom of the active region trench from the epi [i.e. the N- epitaxial layer (104)], forming a low injection diode below the

¹² As the ‘079 Patent describes, the “body” of an N-channel MOSFET is P-type doped semiconductor material (e.g. silicon doped with boron).

body/drain junction.” ‘079 Patent at 5:29-32. However, a POSA would not find the word “thin” helpful in trying to ascertain the scope of this claim term, as, in this context, it is too subjective, relative, and vague to assist in understanding the claim’s scope with reasonable certainty—thinness or thickness would depend on the design and the goals of the design. The ‘079 Patent continues, stating that “[t]he thickness and the doping level of the thin body layer, which lies between the active region contact trench and the drain, are adjusted so that in reverse bias this thin body layer is almost completely depleted while in forward bias the body layer is not depleted.” ‘079 Patent at 5:32-36. Although this passage does refer to the thickness of the layer of body region, it is not helpful as it does not provide any specific scope, but instead identifies the thickness of the thin layer of body region and the doping of that same body region as two factors that may be “adjusted” to accomplish the goal of “in reverse bias ... thin body layer is almost completely depleted while in forward bias the body layer is not depleted.” *Id.* But, claims 1 and 13 of the ‘079 Patent do not recite any particular degree of doping of the layer of body region under the active region contact trench, so this passage cannot provide reasonable certainty as to the claim scope, i.e. for any particular thinness of body region, there are degrees of doping of the layer of body region that can succeed or fail to achieve the goal of near depletion in reverse bias and non-depletion in forward bias, and thus a POSA could not understand such goal as being a test or stand-in for the appropriate relative thickness of the body region.

86. Indeed, during prosecution, the examiner rejected the patentee’s attempt to claim the layer of body region by specifying its depletion in forward and reverse bias. *See, e.g.*, April 16, 2014 Office Action at pp. 3 (“With respect to claim limitation the layer of body region is formed to have such thickness and doping level that the layer of body region is substantially depleted while in reverse bias, and not depleted while in forward bias. [A] recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim”); August 14, 2014 Amendment at p. 2 (removing the language regarding depletion in reverse and forward bias

and adding in language of claim term instead). Thus, in my opinion, a POSA would not understand the claim as requiring any particular effect on depletion in forward and reverse bias, and therefore would not understand this passage as providing reasonable certainty.

87. Finally, the ‘079 Patent states that “In some embodiments, the thickness of the layer is approximately 0.01~0.5 μm .” ‘079 Patent at 5:36-38. Although this numeric disclosure would appear to provide additional certainty, because the claim is recited in relative terms (i.e. the thickness of the body region must be substantially less *than the depth of the active region contact trench*), a POSA would have to also examine the ‘079 Patent’s disclosure regarding depth of the active region contact trench to understand the scope of “substantially less” in the claim. Indeed, standing on its own, the range of 0.01 to 0.5 microns is a very large range in the context of semiconductor devices of the era of filing of the ‘079 Patent. Moreover, a POSA would understand that as semiconductor process nodes evolve over time and continue to miniaturize that many of the measurements of the structures of a MOSFET implementing the ‘079 Patent would expect to shrink—this is certainly reflected in the fact that the claims of the ‘079 Patent (other than claim 2) are not limited to any particular semiconductor process node or any specific measurements.

88. Thus, the ‘079 Patent’s disclosures regarding the depth of the active contact trench are critical to a POSA’s understanding of the “substantially less” limitation and contextualizing the ‘079 Patent’s disclosure of a thin layer of body region of “approximately 0.01~0.5 μm .” However, the ‘079 Patent’s disclosures regarding the depth of the active region contact trench only further demonstrate a lack of reasonable certainty. In particular, the only disclosures of the ‘079 Patent with numeric figures provided for the active region contact trench are:

- “FIGS. 4O-4T illustrate the formation of the contact trench and various implants along the contact trench. A first contact etch is performed to form trenches 468 and 470. In some embodiments, the depth of the first contact trench is between 0.2-2.5 μm .” (‘079 Patent at 7:55-60).

- “In FIG. 4R, a second contact etch takes place. Since the etching process does not affect the dielectric layer, the second contact etch does not require an extra mask. The depth of the trenches is increased by 0.2-0.5 μm in some embodiments.” (‘079 Patent at 8:5-8).

89. These ranges provided for the depth of the active region contact trench are also extremely broad. Following these two passages together, on the low end, the passage for Figs. 4O-4T provides 0.2 μm deep trench. Regarding the passage of 4R, it is not clear if the second etch (and consequent increase in trench depth) is mandatory as it is only described in “some embodiments.” Assuming the second etch is mandatory, the two passages together provide a low-end depth of the trench as 0.4 μm (0.2 μm from the first etching + 0.2 μm for the second etching). At the high end, the two passages disclose a maximum depth of 3.0 μm (2.5 μm from the first etching + 0.5 μm for the second etching). Thus, the range of the active region contact trench depth provided by the ‘079 Patent’s specification is 0.4 μm to 3.0 μm if the second etching is mandatory. Rather than providing guidance to a POSA to show how much *less* the thickness of the layer of body region must be compared to the depth of the trench, the two ranges *overlap* (i.e. the 0.5 μm upper end for the thickness of the “thin” layer of body region is greater than the 0.4 μm lower end for the depth of the contact trench).¹³ That is, the specification discloses ranges of numeric values which are outside the scope of the claims (which require that the trench be deeper than the body region) and thus cannot provide guidance to how much “less” is “substantially less” in the claims.

90. Said another way, if in attempting to understand this claim term, a POSA tried to calculate the percentage of the thickness of the layer of body region as compared to the depth of the contact trench as disclosed in the specification of the ‘079 patent, they would get a range of 0.3% (for a 0.01 μm thick layer of body region and a 3.0 μm deep contact trench) to 125% (for a 0.5 μm thick layer of body region and a 0.4 μm deep contact trench). This result is extremely

¹³ If the second contact trench etching was optional, the problem would be more pronounced, as the lower limit of the depth of the active region contact trench would be provided solely by the first etching’s lower bound of 0.2 μm , which would more extensively overlap with the 0.01 to 0.5 μm disclosed thickness of the layer of body region.

1 broad and provides no meaningful guidance to a POSA for determining the scope of “substantially
2 less” (as the specification’s ranges include layers of body region whose thicknesses are less, equal
3 to, or more, than the source contact trench depth). In short, because the ‘079 Patent discloses
4 extremely broad ranges for the measurements of the features relevant to this claim term, and does
5 not disclose any other useful relationship between the two figures, a POSA would not be informed
6 with reasonable certainty by the specification of the ‘079 Patent how much “less” is “substantially
7 less.”

8 91. I understand that the prosecution history and the background knowledge of a POSA
9 may also be relevant to definiteness. However, in my opinion, the background knowledge of a
10 POSA at the time of the invention would not solve this problem. In particular, from the prosecution
11 history of the ‘079 Patent, it is evident that the thickness of the layer of body region limitation was
12 the specific limitation added during prosecution to overcome the prior art. Sep. 25, 2014 Notice
13 of Allowability at 2 (identifying disputed term as not disclosed in pertinent prior art); August 14,
14 2014 Response to Office Action, at pp. 2, 6 (adding the disputed term to claim 1 in response to
15 office action immediately prior to issuance and identifying it as distinguishing the prior art). I
16 also reviewed the prior art that was asserted by the examiner in the office action prior to allowance:
17 U.S. Patent No. 6,433,396 (“Kinzer”), US Pub. No. 2005/0167742 (“Challa”), and U.S. Pub. No.
18 2005/0029584 (“Shiraishi”), U.S. Patent No. 6,686,814 (“Tihanyi”), U.S. Patent No. 5,489,787
19 (“Amaratunga”), and U.S. Pub. 2006/0138533 (“Hirler”). See April 16, 2014 Office Action. In
20 my opinion, neither the prosecution history nor the prior art references cited therein provide
21 sufficient guidance to a POSA to understand the scope of this limitation with reasonable certainty.
22 In particular, Kinzer was the only reference the examiner asserted as disclosing a layer of body
23 region underneath a source contact (April 16, 2014 Office Action at pp. 3, 5-6), but Kinzer provides
24 no numeric or other guidance regarding the thickness of that body region layer. Thus, assuming
25 that the ‘079 Patent is novel and non-obvious, a POSA would not be aware of any relevant or
26 pertinent background for how appropriately thin a layer of body region can be.

1 92. For these reasons, in my opinion, a POSA would not be informed of the scope of
2 “the thickness of the layer of body region is substantially less than the depth of the active region
3 contact trench” (or the claims reciting it) with reasonable certainty.

4 I declare under penalty of perjury that the foregoing is true and correct.
5

6 Executed on: August 4, 2023



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8 Dean Neikirk, Ph.D
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EXHIBIT 1

Power MOSFET Selection Guide

September 2001



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Analog

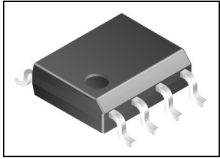
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SO-16	8
SOT-223	7
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SuperSOT [™] -6	5
SuperSOT [™] -8	4
TO-92	7
TO-220	18
TO-247 (TO-3P)	29
TO-251	11
TO-264	33
TSSOP-8	5

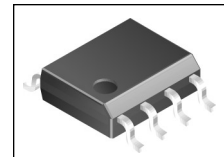
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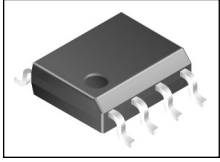
Part Number	V _{DS} (V)	R _{DS(ON)} Max. (mΩ) @ V _{GS} =				Q _g (nC) @ V _{GS} = 5V	I _D (A)	P _D (W)	Configuration
		10V	4.5V	2.5V	1.8V				
SO-8 N-Channel									
RF1K49211	12		20			35	7	2	
RF1K49090			50			12	3.5	2	Dual
FDS6574A	20		6	7	9	75	16	2.5	
FDS6572A			6	7		57	16	2.5	
FDS6570A			7.5	10		47	15	2.5	
NDS8426A			13.5	16@2.7			10.5	2.5	
FDS6890A			18	22		23	7.5	2	Dual
NDS8425			25	30@2.7			7.4	2.5	
FDS9926A			30	43		7	6.5	2	Dual
FDS7760A	30	5.5	8			37	15	2.5	
FDS7064A		5.5	7.5			33			
FDS6688		6	7			40	16	2.5	
FDS6676		7	8			45	14.5	2.5	
FDS7764A			7.5				16	2.5	
FDS6670A		8	10			35	13	2.5	
FDS6672A		8	9.5			33	12.5	2.5	
SI4420DY		9	13			23	12.5	2.5	
FDS6670S		9	12.5			24	13.5	2.5	SyncFET
FDS6680A		9.5	13			23	12.5	2.5	
FDS6680		10	15			19	11.5	2.5	
ITF86130SK8T		7.8	10			31.5	14	2.5	
FDS6680S		11	17			17	11.5	2.5	SyncFET
FDS6694		11	13.5			13	12	2.5	
HUF76132SK8		11.5	16			24	11.5	2.5	
FDS6692		12	14.5			18	12	2.5	
FDS6690A		12.5	17			17	11	2.5	
HUF76131SK8		13	18			22	10	2.5	
FDS4410		13.5	20			13	10	2.5	
FDS6690		13.5	20			13	10	2.5	
SI4410DY		13.5	20			13	10	2.5	
HP4410DY		13.5					10	0	
FDS6982		15	20			18.5	8.6	2	Dual
FDS6690S		28	35			8.5	6.3	2	Dual
		16	25			17	10	2.5	SyncFET
FDS6982S		16	22			17.5	8.6	2	Dual
		28	35			8.5	6.3	2	SyncFET
FDS6614A		18	25			12	9.3	2.5	
FDS6990A		18	23			17	7.5	2	Dual
SI4416DY		18	28			13	9	2.5	
FDS6984S		19	28			11	8.5	2	Dual
		40	55			5	5.5	2	SyncFET
FDS6678A	20	24			13	7.5	2.5		
FDS6612A	22	30			9	8.4	2.5		
FDS9412	22	36			9	7.9	2.5		
FDS6990S	22	30			11	7.5	2	Dual SyncFET	
ISL9N322ASK8T	22				8.6	8.3	2.5		
HUF76121SK8	23	31			14	8	2.5		
HUF76112SK8T	26	33			7.2	7.5	2.5		
FDS6912	28	42			7	6	2	Dual	
FDS6912A	28	35			9	6	2	Dual	
FDS8936A	28	40				6	2	Dual	
NDS9410A	28	42			9	7.3	2.5		
SI4412DY	28	42			9	7	2.5		
FDS6986S	29	38			6.5	6.5	2	Dual	
	20	28			11	7.9	2	SyncFET	
FDS8926A		30	38			5.5	2	Dual	
SI9410DY		30	50			7	2.5		
HUF76113SK8		30	41			10	6.5	2.5	
RF1K49156			30			29	6.3	2	
RF1K49157		30	60			25	6.3	2	
HUF76113DK8		32	43			8.4	6	2.5	
NDS8936		35	50				5.3	2	
SI4936DY		37	55			5	5.8	2	
HP4936DY		37					5.8	0	
FDS6630A		38	53			5	6.5	2.5	

Part Number	V _{DS} (V)	R _{DS(ON)} Max. (mΩ) @ V _{GS} =				Q _g (nC) @ V _{GS} = 5V	I _D (A)	P _D (W)	Configuration
		10V	4.5V	2.5V	1.8V				
SO-8 N-Channel (continued)									
FDS6930A	30	40	55			5	5.5	2	Dual
HUF76105DK8		50	78			5.3	5	2.5	Dual
HUF76105SK8		50	78			5.3	5.5	2.5	
RF1K49088			60			13	3.5	2	Dual
NDS9956A		80	110				3.7	2	Dual
FDS6961A		90	140			2.1	3.5	2	Dual
FDS6961AZ		90	140			2.1	3.5	2	Dual
FDS4672A	40		13			35	11	2.5	
NDS9959	50	300	500				2	2	Dual
SSD2007A		300	500			9.5	2	2	
FDS5670	60	14	17@6			49	10	2.5	
FDS5680		20	25@6			30	8	2.5	
FDS5690		28	33@6			23	7	2.5	
HUF76407DK8T		90	105			9.4	3.8	2.5	Dual
SI9945DY		100	200				3.3	2	Dual
FDS9945		100	200			8	3.5	2	Dual
SSD2025		100				24	3.3	2	
NDS8433		7500					3.5	2.5	
NDS8434							3.5	2.5	
NDS8435							3.5	2.5	
NDS9943							3.5	2.5	
NDS9953							3.5	2.5	
NDS9956							3.5	2.5	
FDS3570	80	19	22@6			54	9	2.5	
FDS3580		27	31@6			34	7.6	2.5	
HUF75531SK8		30				37	6	2.5	
FDS3590		37	43@6			23	6.5	2.5	
FDS3890		44	50@6			29	4.7	2	Dual
FDS3512		70	80@6			13	4	2.5	
FDS3812		74	84@6			13	3.4	2	Dual
FDS3670	100	30	33@6			57	6.3	2.5	
HUF75631SK8		39				35	5.5	2.5	
FDS3680		43	48@6			38	5.2	2.5	
FDS3690		59	66@6			28	5	2.5	
FDS3612		120	130@6			14	3.4	2.5	
FDS3912		125	135@6			14	3	2	Dual
FDS3601		480	530@6			3.7	1.3	2	Dual
FDS2570	150	80	90@6			39	4	2.5	
HUF75831SK8T		95				35	3	2.5	
FDS2670	200	130				27	3	2.5	
FQS4901	400	4200				5.8	0.45	2	Dual
FQS4903	500	6200				6.3	0.37	2	Dual
SO-8 P-Channel									
RF1K49093	-12		130			10	2.5	2	Dual
FDS4465	-20		8.5	10.5	14	86	13.5	2.5	
SI4467DY			8.5	2.5	1.8	86	13.5	2.5	
FDS6575			13	17		50	10	2.5	
FDS6576			14	20		43	11	2.5	
FDS6375			24	32		23	8	2.5	
NDS8434A			24	32			7.8	2.5	
SI9424DY			24	32		23	8	2.5	
FDS6875			30	40		23	6	2	Dual
FDS8433A			47	70			5	2.5	
FDS8934A			55	72			4	2	Dual
NDS9405			60	115@2.7			3.5	2.5	
NDS9430			60	115			3.5	2.5	
NDS9430A			60	115			3.5	2.5	
FDS9933A			75	105		8	3.8	2	Dual
FDS9431A			130	180		6	3.5	2.5	
NDS9933A			140	200			2.8	2	Dual
SI9953DY	-30	250	400				2.3	2	Dual
FDS6679		9	13			71	13	2.5	
FDS6679Z		9	13			67	13	2.5	
FDS6675		14	20			30	11	2.5	
FDS4435A		17	25			21	9	2.5	

SO-8

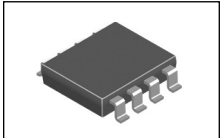


SO-8



Part Number	V _{DS} (V)	R _{DS(ON)} Max. (mΩ) @ V _{GS} =				Q _g (nC) @ V _{GS} = 5V	I _D (A)	P _D (W)	Configuration
		10V	4.5V	2.5V	1.8V				
SO-8 P-Channel (continued)									
FDS4435	-30	20	35			17	8.8	2.5	
FDS6685		20	35			19	8.8	2.5	
SI4435DY		20	35			17	8.8	2.5	
SI4835DY		20	35			19	8.8	2.5	
NDS8435A		23	35				7.9	2.5	
FDS4935		23	35			15	7	2	Dual
FDS6609A		32	50			18	6	2.5	
FDS6975		32	45			14.5	6	2	Dual
SI4925DY		32	45			14.5	6	2	Dual
FDS9435A		45	75				5.3	2.5	
NDS9435A		50	90				5.3	2.5	
FDS4953		53	95			8	5	2	Dual
SI4953DY		53	95			8	4.9	2	Dual
NDS8947		65	100				4	2.5	
NDS9953A		130	200				2.9	2	Dual
NDS9400A		130	200				3.4	2.5	
FDS9400A		130	200			2.5	3.4	2.5	
FDS9953A		130	200			2.5	2.9	2	Dual
RF1K49223		150	360			8	2.5	2	Dual
FDS4675	-40	13	17			40	11	2.4	
NDS9407	-60	150	240				3	2.5	
NDS9948		250	500				2.3	2	Dual
SO-8 Complementary N-P Channel									
RF1K49092	12		130			12	3.5	2	Comp
FDS4501H	30	18	27			18.5	9.3	2.5	Comp
	-20	18	50	63		18.5	5.6	2.5	Comp
FDS8958A	30	28	40				7	2	Comp
	-30	52	80				5	2	Comp
FDS8928A	30		30	38			5.5	2	Comp
	-20		55	72			4	2	Comp
NDS8858H	30	35	50				6.3	2.5	Comp
	-30	65	100				4.8	2.5	Comp
SI4532DY	30	65	95				3.9	2	Comp
	-30	85	190				3.5	2	Comp
NDS9952A	30	80	110				3.7	2	Comp
	-30	130	200				2.9	2	Comp
FDS4559	60	55	75			12.5	4.5	2	Comp
	-60	105	135			15	3.5	2	Comp
FQS4900	60	550	650			1.6	1.3	2	Comp
	-300	15500	16000			3.6	0	2	Comp

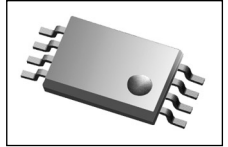
SuperSOT-8



SuperSOT-8 N-Channel									
FDR6580	20		9	11		34	11.2	1.8	
FDR4410	20	13	20				9.3	1.8	
	-30	90	150				4	1.8	
NDH833N	20		20	25@2.7			7.1	1.8	
FDR8305N			22	28		16.2	4.5	0.8	Dual
FDR4420A	30	9	13			23	11	1.8	
FDR6674A		8.5	9.5			33	11.5	1.8	
FDR6678A		20	24			13	7.5	1.8	
SuperSOT-8 P-Channel									
FDR840P	-20		11	16		41	10	1.8	
FDR844P			11	14	20	53	10	1.8	
FDR838P			17	24		30	8	1.8	
FDR836P			30	40			6.1	1.8	
	-30		170	250			1.6	1.8	
NDH834P			35	45@2.7			5.6	1.8	
FDR8308P			50	70		13	3.2	0.8	Dual
NDH832P			60	80@2.7			4.2	1.8	
NDH8304P			70	95@2.7			2.7	0.8	Dual
FDR858P		19	28			21	8	1.8	
FDR856P		25	40				6.3	1.8	
FDR8508P		50	75			8	3	0.8	Dual

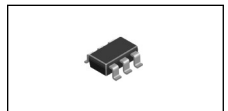
Part Number	V _{DS} (V)	R _{DS(ON)} Max. (mΩ) @ V _{GS} =				Q _g (nC) @ V _{GS} = 5V	I _D (A)	P _D (W)	Configuration	
		10V	4.5V	2.5V	1.8V					
TSSOP-8 N-Channel										
FDW2501N	20		18	28			6	1	Dual	
FDW2501NZ			18	25		14	6	1	Dual	
FDW2507NZ			19	23		20	7.5	1.6	Dual	
FDW2507N			19	23		20	7.5	1.6	Dual	
FDW2503N			21	35		10.5	5.5	1	Dual	
SI6926DQ			21	35		12	5.5	1	Dual	
SI6966DQ			21	35		12	5.5	1	Dual	
P-Channel										
FDW252P	-20		12	18			8.8	1.3		
FDW254P			12	15	21.5	60	9.2	1.3		
SI6467DQ			12	15	21.5	60	9.2	1.3		
SI6463DQ			12.5	18		41	8.8	1.3		
FDW2506P			22	32			5.3	1	Dual	
FDW2502P			35	57			4.4	1	Dual	
FDW2502PZ			35	57		14	4.4	1	Dual	
FDW2504P			43	70		10	3.8	1	Dual	
SI6963DQ			43	70		9.7	3.8	1	Dual	
SI6923DQ			45	75		9.7	3.5	1.2	Dual	
FDW262P			47	65	100	13	4.5	1.3		
FDW256P		-30	13.5	20			28	8	1.3	
Complementary N-P Channel										
FDW2520C	20		18	28			7.2	3	Comp	
	-20		33	57			5.3	3	Comp	
FDW2521C	20		21	35		12	7	1	Comp	
	-20		43	72		12	4	1	Comp	

TSSOP-8

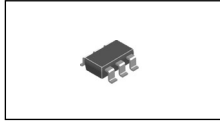


SuperSOT-6 N-Channel									
FDC637AN	20		24	32		10.5	6.2	1.6	
SI3446DV			24	32		10.5	6.2	1.6	
NDC631N			60	75@2.7			4.1	1.6	
FDC6401N			70	95		3.3	3	0.96	Dual
FDC6305N			80	120		3.5	2.7	0.9	Dual
SI3442DV		6000	7500			10	4.1	1.6	
FDC6303N	25		450	600@2.7			0.68	0.9	Dual
FDC6301N			4000	5000@2.7			0.22	0.9	Dual
FDC655AN	30	27	35			9	6.3	1.6	
FDC645N		30	26			13	5.5	1.6	
FDC653N		35	55				5	1.6	
FDC633N			42	54			5.2	1.6	
NDC651N		60	90				3.2	1.6	
FDC6561AN		95	145			2.1	2.5	0.9	Dual
SI3948DV	50	95	145			2.3	2.5	0.96	Dual
NDC7002N		2000	4000				0.51	0.9	Dual
FDC5612	60	55	64@6			12.5	4.3	1.6	
FDC3512	80	77	88@6			13	3	1.6	
FDC3612	100	125	135@6			14	2.6	1.6	
FDC3601N		500	550@6			3.7	1	0.96	Dual
FDC2512	150	425	475@6			8	1.4	1.6	
FDC2612	200	725				8	1.1	1.6	
P-Channel									
FDC604P	-20		33	43	60	19	5.5	1.6	
SI3447DV			33	43	60	19	5.5	1.6	
SI3445DV			33	43	60	19	5.5	1.6	
FDC602P			35	50		14	5.5	1.6	
FDC638P			45	65		13	4.5	1.6	
FDC640P			50	77		10	4.5	1.6	
FDC642P			65	100		7.2	4	1.6	
SI3443DV			65	100		7.2	4	1.6	
FDC634P			80	110			3.5	1.6	
SI3441DV			80	110		7.2	3.5	1.6	
FDC6312P			115	155	225	4.4	2.3	0.96	Dual
FDC6310P			125	190		3.7	2.2	0.96	Dual
FDC636P			130	180			2.8	1.6	

SuperSOT-6

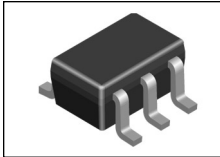


SuperSOT-6



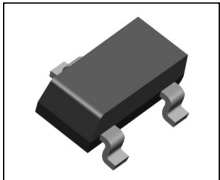
Part Number	V _{DS} (V)	R _{DS(ON)} Max. (mΩ) @ V _{GS} =				Q _g (nC) @ V _{GS} = 5V	I _D (A)	P _D (W)	Configuration
		10V	4.5V	2.5V	1.8V				
SuperSOT-6 P-Channel (continued)									
FDC6306P	-20		170	250		3	1.9	0.9	Dual
FDC6308P			180	300		3	1.7	0.9	Dual
FDC6304P	-25		1100	1500@2.7			0.46	0.9	Dual
FDC6302P			10000	13000@2.7			0.12	0.9	Dual
FDC658P	-30	50	75			8	4	1.6	
SI3457DV		50	75			6	4	1.6	
FDC654P		75	125				3.6	1.6	
SI3455DV		75	125			3.6	3.6	1.6	
NDC652P		110	180			5.5	2.4	1.6	
FDC6506P		170	280			2.3	1.8	0.9	Dual
FDC5614P	-60	100	130			15	3	1.6	
Complementary N-P Channel									
FDC6420C	20		70	95					Comp
	-20		70	95					Comp
FDC6402N	20		70	95		3.3	30	0.96	Comp
	-20		125	190		3.7	2.2	0.96	Comp
FDC6327C	20		80	120		3.2	2.7	0.9	Comp
	-20		170	250		2.8	1.6	0.9	Comp
FDC6321C	25		450	600@2.7			0.68	0.9	Comp
	-25		1100	1500@2.7			0.46	0.9	Comp
FDC6320C	25		4000	5000@2.7			0.22	0.9	Comp
	-25		10000	13000@2.7			0.12	0.9	Comp
FDC6322C	25		4000	5000@2.7			0.22	0.9	Comp
	-25		1100	1500@2.7			0.46	0.9	Comp
FDC6333C	30	95	150			4.7	2.5	0.96	Comp
	-30	150	220			4.1	2	0.96	Comp
NDC7001C	50	2000	4000				0.51	0.9	Comp
	-50	5000	7500				0.34	0.9	Comp

SC70-6



SC70-6 N-Channel									
FDG329N	20		90	115			1.5	0.42	
FDG327N			90	100	140	4.5	1.5	0.42	
FDG311N			115	150		3	1.9	0.48	
FDG313N	25		450	600@2.7			0.95	0.48	
FDG6303N			450	600@2.7			0.5	0.3	Dual
FDG6301N			4000	5000@2.7			0.22	0.3	Dual
FDG315N	30	120	160			2.1	2	0.48	
FDG361N	100	500	550@6			3.7	0.6	0.42	Dual
P-Channel									
FDG328P	-20		135	190			1.5	0.48	
FDG326P			140	180	250		1.5	0.75	
FDG312P			180	250		3.3	1.2	0.48	
FDG318P			200	350		3	1.5	0.48	
FDG6308P			400	550	800	1.8	0.6	0.3	Dual
FDG6306P			420	630		1.4	0.6	0.3	Dual
FDG314P	-25		1100	1500@2.7			0.65	0.48	
FDG6304P			1100	1500@2.7			0.41	0.3	Dual
FDG6302P			10000	13000@2.7			0.14	0.3	Dual
FDG316P	-30	190	300			3.5	1.6	0.48	
Complementary N-P Channel									
FDG6321C	25		450	600@2.7			0.5	0.3	Comp
	-25		1100	1500@2.7			0.41	0.3	Comp
FDG6320C	25		4000	5000@2.7			0.22	0.3	Comp
	-25		10000	13000@2.7			0.14	0.3	Comp
FDG6322C	25		4000	5000@2.7			0.22	0.3	Comp
	-25		1100	1500@2.7			0.41	0.3	Comp

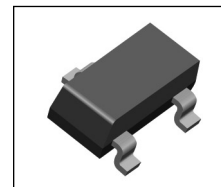
SuperSOT-3



SuperSOT-3 (SOT-23) N-Channel									
FDN339AN	20		35	50		7	3	0.5	
FDN371N			50	60		7.6	2.5	0.5	
FDN335N			70	100		3.5	1.7	0.5	
FDN327N			70	80	120	4.5	2	0.5	
NDS335N			110	140@2.7			1.7	0.5	

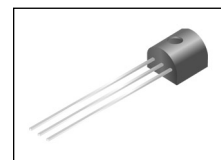
Part Number	V _{DS} (V)	R _{DS(ON)} Max. (mΩ) @ V _{GS} =				Q _g (nC) @ V _{GS} = 5V	I _D (A)	P _D (W)	Configuration
		10V	4.5V	2.5V	1.8V				
SuperSOT-3 / SOT-23 N-Channel (continued)									
NDS331N	20		160	210@2.7			1.3	0.5	
FDV303N	25		450	600@2.7			0.68	0.35	
FDV301N			4000	5000@2.7			0.22	0.35	
FDN359AN	30	46	60			5	2.7	0.5	
FDN357N		60	90				1.9	0.5	
FDN337N			65	82			2.2	0.5	
NDS355AN		85	125				1.7	0.5	
NDS355N		85	125				1.6	0.5	
FDN361AN		100	150			2.1	1.8	0.5	
NDS351AN		160	250				1.2	0.5	
BSS138		50	3500	6000				0.22	0.36
FDN5630	60	100	120@6			7	1.7	0.5	
NDS7002A		2000	3000				0.28	0.3	
MMBF170		5000					0.5	0.3	
2N7002		7500	7500				0.12	0.2	
NDS351N							3.5	0.5	
BSS123	100	6000	10000				0.17	0.36	
P-Channel									
FDN304P	-20		52	70	100	12	2.4	0.5	
FDN302P			55	80			2.4	0.5	
FDN340P			70	110		8	2	0.5	
FDN342P			80	130		6.3	2	0.5	
FDN308P			125	190		3.8	1.5	0.5	
FDN338P			130	180			1.6	0.5	
FDN336P			200	270		3.6	1.2	0.5	
NDS332P			300	410@2.7			1	0.5	
NDS336P							3.5	0.5	
NDS352P							3.5	0.5	
NDS356P							3.5	0.5	
FDV304P		-25		1100	1500@2.7			0.46	0.35
FDV302P			10000	13000@2.7			0.12	0.35	
FDN360P	-30	80	125			5	2	0.5	
FDN358P		125	200				1.5	0.5	
NDS356AP		200	300				1.1	0.5	
NDS352AP		300	500				0.9	0.5	
BSS84	-50		10000				0.13	0.36	
FDN5618P	-60	170	230			8.6	1.2	0.5	
NDS0605		5000	7500				0.18	0.36	
NDS0610		10000	20000				0.12	0.36	

SuperSOT-3



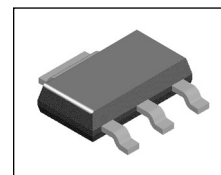
TO-92 N-Channel									
BS270	60	2000	3000				0.4	0.625	
BS170		5000					0.5	0.83	
2N7000		5000	5300				0.2	0.4	
2N7000M		5000					0.2	0.4	
2N7008		7500							
BSS100	100	6000	10000				0.22	0.63	
FQNL2N50B	500	5300				6	0.35	1.5	
FQNL1N50B		9000				4	0.27	1.5	
P-Channel									
BSS110	-50	10000					0.17	0.63	

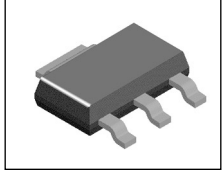
TO-92



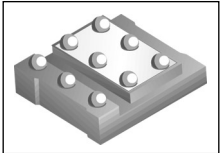
SOT-223 N-Channel									
NDT455N	30	15	20				11.5	3	
NDT453N		28	42				8	3	
HUF76113T3ST		31	40			9.5	4.7	1.1	
FDT459N		35	55				6.5	3	
FDT439N			45	58			6.3	3	
NDT451N		50	80				5.5	3	
FDT457N		60	90				5	3	
HUF75309T3ST	55	70				10.7	3	1.1	
HUF75307T3ST		90				8.3	2.6	1.1	
FQT13N06	60	140				5.8	2.8	2.1	

SOT-223

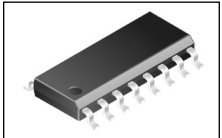


SOT-223

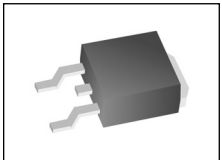
Part Number	V _{DS} (V)	R _{DS(ON)} Max. (mΩ) @ V _{GS} =				Q _g (nC) @ V _{GS} = 5V	I _D (A)	P _D (W)	Configuration
		10V	4.5V	2.5V	1.8V				
SOT-223 N-Channel (continued)									
NDT014L	60	160	200				2.8	3	
FDT3612	100	120	130@6			14	3.7	3	
IRFM120A		200				16	2.3	2.4	
IRFM110A		400				8.5	1.5	2	
IRLM110A			440			5.5	1.5	2.2	
IRLM120A				220		10.2	2.3	2.7	
IRFM220A	200	800				12	1.1	2.4	
IRFM210A		1500				7	0.77	2	
IRLM210A			1500			6.1	0.77	1.8	
IRFM224A	250	1100				14	0.92	2.5	
IRFM214A		2000				8.5	0.64	2.1	
P-Channel									
FDT434P	-20		50	70		14	5.5	3	
NDT456P	-30	30	45				7.5	3	
NDT454P		50	90				5.9	3	
NDT452AP		65	100				5	3	
FDT458P		130	200			2.5	3.4	3	
RFT2P03L		150	360			8	2.1	1.1	
NDT452P	-60	180	320				3	3	
NDT2955		300	500				2.5	3	
SFM9014		500				9	1.8	2.8	
SFM9110		-100	1200			9	1	2.5	
SFM9210	-200	3000			9	0.5	1.6		
SFM9214	-250	4000			9	0.45	1.6		

BGA (Bottomless)

BGA (Bottomless) N-Channel									
FDZ201N	20		18	30			9	2.7	
FDZ2551N			18	30			9	3	Dual
FDZ5047N	30	3.5	5			50	22	3.3	
FDZ7064N		5.7	7.5			33			
P-Channel									
FDZ206P	-20		8.5	13.5					
FDZ202P			45	75		9	5.5	2	
FDZ2552P			45	75			6	3	Dual
FDZ204P			45	75		9	4.5	1.8	

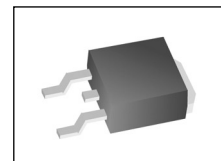
SO-16

SO-16 Complementary N-P Channel									
NDM3000	30	90	130				3	2.5	Motor
	-30	160	250				3	2.5	Motor
NDM3001	30	115	160				2.9	2.5	Motor
	-30	240	360				2.9	2.5	Motor

PAK (TO-252)

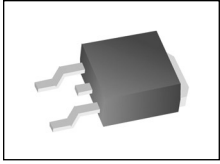
PAK (TO-252) N-Channel									
HUF76013D3S	20	22	30			7.8	20	50	
HUF76009D3S		27	39			5.7	20	41	
FDD6530A			32	47		6.5	21	33	
ISL9N306AD3ST	30	6	9.5			30	50	125	
ISL9N2357D3ST		7				85	50	100	
ISL9N307AD3ST		7				28	50	100	
FDD6676		7.5	8.5			45	78	83	
FDD6670A		8	10			35	66	70	
FDD6672A		8	9.5			33	65	70	
ISL9N308AD3ST		8				24	50	100	
FDD6644		8.5	10.5			25	67	68	
FDD6670S		9.4	13			17	64	70	SyncFET
FDD6680A		9.5	13			23	56	60	
FDD6680		10	15			19	55	60	
ISL9N310AD3ST		10				17	35	70	
FDD6680S		11	17			17	55	60	SyncFET
FDD6692		12	14.5			18	54	57	
ISL9N312AD3ST		12				13	50	75	
FDD6690A		12.5	16			17	46	50	

Part Number	V _{DS} (V)	R _{DS(ON)} Max. (mΩ) @ V _{GS} =				Q _g (nC) @ V _{GS} = 5V	I _D (A)	P _D (W)	Configuration
		10V	4.5V	2.5V	1.8V				
DPAK (TO-252) N-Channel (continued)									
ISL9N316AD3ST	30	15.5				13	48	65	SyncFET
FDD6030BL		16	22			22	42	50	
HUF76129D3S		16	23			22	20	105	
FDD6690S		16.7	24.5			17	40	50	
ISL9N318AD3ST		18				8.6	30	45	
FQD60N03L		19	24			34	40.3	56	
HPLR3103		19					20	0	
FDD6612A		20	28			9	30	36	
ISL9N322AD3ST		22				8.6	45	20	
FDD603AL		23	37			9	33	39	
HUF76121D3S		23	33			13	20	75	
FQD45N03L		25	31			20	30	45	
ISL9N327AD3S		27	40			8.7	20	50	
FDD6630A		35	50			5	21	28	
HUF76107D3S		52	85			4.7	20	35	
HUF75329D3S	55	26				32	20	128	
HUF75321D3S		36				21	20	93	
HUF75309D3S		70				11	19	55	
HUF75307D3S	60	90				9	15	45	
FDD5670		15	18@6			49	48	70	
FDD5680		21	24@6			33	38	60	
HUF76429D3S		23	27			38	20	110	
FDD5690		27	32@6			23	30	50	
HUF76423D3S		32	37			28	20	85	
HUF76419D3S		37	43			23	20	75	
FQD30N06L		39	47			15	24	44	
FQD30N06		45				19	22.7	44	
HUF76413D3S		49	56			17	20	60	
FDD5612		55	64@6			7.5	18	42	
FQD20N06LE		60	75			9.5	17.2	38	
FQD20N06L		60	75			9.5	17.2	38	
FQD20N06		63				11.5	16.8	38	
HUF76409D3S		63	71			12	18	49	
HUF76407D3S		92	107			9.4	12	38	
FQD13N06L		110	140			4.8	11	28	
FQD13N06		140				7.5	10	28	
RFD3055SM		150				10	12	53	
FDD3570		80	19	22@6			54	10	69
FDD3580			29	33@6			35	7.7	42
FQD24N08			60				19	19.6	50
FQD17N08L			100	115			8.8	12.9	40
FQD17N08			115				12	12.9	40
FQD9N08L			210	230			4.7	7.4	25
FQD9N08	210					5.9	7.4	25	
FDD3670	100	32	35@6			57	34	83	
FDD3680		46	51@6			38	7	60	
HUF76629D3S		52	54			38	20	110	
FDD3690		64	71@6			28	22	60	
HUF76619D3S		85	87			24	18	75	
HUF75617D3S		90				18	16	64	
FQD19N10L		100	110			14	15.6	50	
FQD19N10		100				19	15.6	50	
IRFR130A		110				27	13	41	
HUF76609D3S		160	165			13	10	49	
FQD13N10L	100	180	200			8.7	10	40	
FQD13N10		180				12	10	40	
IRFR120A		200				16	8.4	32	
IRFR120*		270				9.7	8.4	50	
IRFR120T*		270				9.7	8.4	50	
FQD7N10L		350	380			4.6	5.8	25	
FQD7N10		350				5.8	5.8	25	
IRFR110A		400				8.5	4.7	20	
IRFR110*		540				5.2	4.7	30	
IRFR110T*		540				5.2	4.7	30	
IRLR110A		440			5.5	4.7	22		

DPAK (TO-252)

*These Industry Standard IRF devices can be specified by adding the suffix R494x to the part number when ordering. Example: IRF840AR4944. The suffix will not appear in the brand.

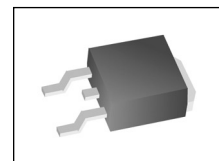
DPAK (TO-252)



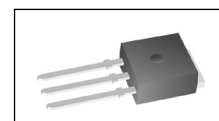
Part Number	V _{DS} (V)	R _{DS(ON)} Max. (mΩ) @ V _{GS} =				Q _g (nC) @ V _{GS} = 5V	I _D (A)	P _D (W)	Configuration	
		10V	4.5V	2.5V	1.8V					
DPAK (TO-252) N-Channel (continued)										
IRLR120A	100		220			10.2	8.4	35		
IRLR130A			120			16.9	13	46		
FDD2570	150	80	90@6			39	4.7	70		
HUF75829D3S		110				31	18	110		
HUF75823D3S		150				23	14	85		
FQD16N15		160				23	11.8	55		
FQD14N15		210				18	10	50		
FQD9N15		400				10	7	45		
FDD2512		420	470@6			8	6.7	42		
FQD6N15		600				6.5	5.2	37		
FQD5N15		800				5.4	4.3	30		
FDD2670		200	130				27	3.6	70	
HUF75925D3ST	275					32	11	100		
FQD12N20L	280		320			16	9	55		
FQD12N20	280					18	9	55		
FQD10N20L	360		380			13	7.6	51		
FQD10N20	360					13.5	7.6	51		
FQD630	400					19	7	46		
IRFR230B	400					22	7.5	50		
IRFR230A	400					22	7.5	50		
FQD7N20	690					8	5.3	45		
FDD2612	720					8	4.9	42		
FQD7N20L	750		780			6.8	5.5	45		
IRFR220B	800					12	4.6	40		
IRFR220A	800					12	4.6	40		
IRFR220*	800					12	4.6	50		
IRFR220T*	800					12	4.6	50		
FQD5N20L	1200		1250			4.8	3.8	37		
FQD5N20	1200					6	3.8	37		
FQD4N20L	1350		1400			4	3.2	30		
FQD4N20	1400					5	3	30		
IRFR210B	1500					7.2	2.7	26		
IRFR210A	1500					7	2.7	26		
IRLR210A			1500			6.1	2.7	21		
IRLR220A			800			10.3	4.6	33		
IRLR230A			400			18.6	7.5	48		
FQD9N25	250		420				15.5	7.4	55	
IRFR234B			450				29	6.6	49	
FQD8N25			550				12	6.2	50	
FQD6N25			1000				6.6	4.4	45	
IRFR224B			1100				13.5	3.8	42	
IRFR224A		1100				14	3.8	42		
FQD4N25		1750				4.3	3	37		
IRFR214B		2000				8.1	2.2	25		
IRFR214A		2000				8.5	2.2	25		
FQD3N25		2200				4	2.4	30		
FQD7N30	300	700				13	5.5	50		
FQD5N30		900				9.8	4.4	45		
FQD3N30		2200				5.5	2.4	30		
FQD2N30		3700				3.7	1.7	25		
IRFR330B	400	1000				25	4.5	48		
FQD6N40		1150				13	4.2	50		
FQD5N40		1600				10	3.4	45		
IRFR320B		1750				14	3.1	41		
IRFR320A	400	1800				19	3.1	41		
IRFR310B		3400				7.7	1.7	26		
FQD3N40		3400				6	2	30		
IRFR310A		3600				10	1.7	26		
FQD2N40	500	5800				4	1.4	25		
IRFR430B		1500				25	3.5	48		
FQD5N50		1800				13	3.5	50		
IRFR420B		2600				14	2.3	41		
FQD4N50		2700				10	2.6	45		
IRFR420A		3000				19	2.3	41		
IRFR420RT4941		3000				13	2.5	50		

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Part Number	V _{DS} (V)	R _{DS(ON)} Max. (mΩ) @ V _{GS} =				Q _g (nC) @ V _{GS} = 5V	I _D (A)	P _D (W)	Configuration	
		10V	4.5V	2.5V	1.8V					
DPAK (TO-252) N-Channel (continued)										
FQD2N50	500	5300				6	1.6	30		
SSR1N50B		5500				8.3	1.3	26		
FQD1N50		9000				4	1.1	25		
SSR4N60B	600	2500				22	2.8	49		
FQD3N60		3600				10	2.4	50		
FQD2N60		4700				9	2	45		
SSR2N60B		5000				12.5	1.8	44		
SSR2N60A		5000				15	1.8	44		
FQD1N60		11500				5	1	30		
SSR1N60B		12000				5.9	0.9	28		
SSR1N60A		12000				7.5	0.9	28		
FQD2N80		800	6300				12	1.8	50	
FQD2N90	900	7200				12	1.7	50		
P-Channel										
RFD10P03LSM	-30		220			13	10	65		
FDD5614P	-60	100	130			15	15	42		
FQD17P06		135				21	12	44		
SFR9034		140				30	14	49		
FQD11P06		185				13	9.4	38		
SFR9024		280				15	7.8	32		
FDD5202P		300	500				8	39		
SFR2955		300				15	7.6	32		
FQD7P06		450				6.3	5.4	28		
SFR9014		500				9	5.3	24		
FQD12P10		-100	290				21	9.4	50	
SFR9130			300				30	9.8	57	
FQD8P10			530				12	6.6	44	
SFR9120	600					16	4.9	32		
IRFR9120*	600					12	5.6	42		
IRFR9120T*	600					12	5.6	42		
FQD5P10	1050					6.3	3.6	25		
SFR9110	1200					9	2.8	20		
FQD7P20	-200		690				19	5.7	55	
FQD5P20		1400				10	3.7	45		
SFR9220		1500				15	3.1	30		
IRFR9220T*		1500				20	3.6	42		
FQD3P20		2700				6	2.4	37		
SFR9210		3000				9	1.6	19		
FQD6P25		-250	1100				21	4.7	55	
FQD4P25			2100				10	3.1	45	
SFR9224			2400				16	2.5	30	
SFR9214	4000					9	1.5	19		
FQD2P25	4000					6.5	2	37		
FQD4P40	-400	3100				18	2.7	50		
FQD2P40		6500				10	1.6	38		
SFR9310		8000				17	1.5	36		
FQD3P50	-500	4900				18	2.1	50		
FQD1P50		10500				11	1.2	38		

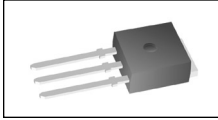
DPAK (TO-252)

IPAK (TO-251) N-Channel									
FDU6644	30	8.5	10.5			25	67	68	
FDU6680A		9.5	13			23	56	60	
FDU6692		12	14.5			18	54	57	
FDU6030BL		16	22			22	42	50	
HUF76129D3		16	23			22	20	105	
HPLU3103		19					20	0	
FDU6612A		20	28			9	30	36	
HUF76107D3		52	85			4.7	20	35	
HUF75329D3	55	26				32	20	128	
HUF75321D3		36				21	20	93	
HUF75307D3		90				9	15	45	
HUF76429D3	60	23	27			38	20	110	
HUF76423D3		32	37			28	20	85	
HUF76419D3		37	43			23	20	75	

IPAK (TO-251)

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IPAK (TO-251)

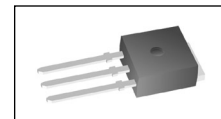


Part Number	V _{DS} (V)	R _{DS(ON)} Max. (mΩ) @ V _{GS} =				Q _g (nC) @ V _{GS} = 5V	I _D (A)	P _D (W)	Configuration
		10V	4.5V	2.5V	1.8V				
IPAK (TO-251) N-Channel (continued)									
FQU30N06L	60	39	47			15	24	44	
FQU30N06		45				19	22.7	44	
HUF76413D3		49	56			17	20	60	
FQU20N06L		60	75			9.5	17.2	38	
FQU20N06		63				11.5	16.8	38	
HUF76409D3		63	71			12	18	49	
HUF76407D3		92	107			9.4	12	38	
FQU13N06L		110	140			4.8	11	28	
FQU13N06		140				5.8	10	28	
FDU3580	80	29	33@6			35	7.7	42	
FQU24N08		60				19	19.6	50	
FQU17N08L		100	115			8.8	12.9	40	
FQU17N08		115				12	12.9	40	
FQU9N08L		210	230			4.7	7.4	25	
FQU9N08		210				5.9	7.4	25	
HUF76629D3	100	52	54			38	20	110	
HUF76619D3		85	87			24	18	75	
HUF75617D3		90				18	16	64	
FQU19N10L		100	110			14	15.6	50	
FQU19N10		100				19	15.6	50	
IRFU130A		110				27	13	41	
HUF76609D3		160	165			13	10	49	
FQU13N10L		180	200			8.7	10	40	
FQU13N10		180				12	10	40	
IRFU120A		200				16	8.4	32	
IRFU120*		270				9.7	8.4	50	
FQU7N10L		350	380			4.6	5.8	25	
FQU7N10		350				5.8	5.8	25	
IRFU110A		400				8.5	4.7	20	
IRFU110*		540				5.2	4.7	30	
IRLU110A			440			5.5	4.7	22	
IRLU120A			220			10.2	8.4	35	
IRLU130A			120			16.9	13	46	
HUF75829D3	150	110				31	18	110	
HUF75823D3		150				23	14	85	
FQU16N15		160				23	11.8	55	
FQU14N15		210				18	10	50	
FQU9N15		400				10	7	45	
FQU6N15		600				6.5	5.2	37	
FQU5N15		800				5.4	4.3	30	
FQU12N20L	200	280	320			16	9	55	
FQU12N20		280				18	9	55	
FQU10N20L		360	380			13	7.6	51	
FQU10N20		360				13.5	7.6	51	
FQU630		400				19	7	46	
IRFU230B		400				22	7.5	50	
IRFU230A		400				22	7.5	50	
FQU7N20		690				8	5.3	45	
FQU7N20L		750	780			6.8	5.5	45	
IRFU220B		800				12	4.6	40	
IRFU220A	800				12	4.6	40		
IRFU220*	200	800				12	4.6	50	
FQU5N20L		1200	1250			4.8	3.8	37	
FQU5N20		1200				6	3.8	37	
FQU4N20L		1350	1400			4	3.2	30	
FQU4N20		1400				5	3	30	
IRFU210B		1500				7.2	2.7	26	
IRFU210A		1500				7	2.7	26	
IRLU210A			1500			6.1	2.7	21	
IRLU220A			800			10.3	4.6	33	
IRLU230A		400			18.6	7.5	48		
FQU9N25	250	420				15.5	7.4	55	
IRFU234B		450				29	6.6	49	
FQU8N25		550				12	6.2	50	
FQU6N25		1000				6.6	4.4	45	

*These Industry Standard IRF devices can be specified by adding the suffix R494x to the part number when ordering. Example: IRF840AR4944. The suffix will not appear in the brand.

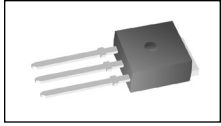
Part Number	V _{DS} (V)	R _{DS(ON)} Max. (mΩ) @ V _{GS} =				Q _g (nC) @ V _{GS} = 5V	I _D (A)	P _D (W)	Configuration	
		10V	4.5V	2.5V	1.8V					
IPAK (TO-251) N-Channel (continued)										
IRFU224B	250	1100				13.5	3.8	42		
IRFU224A		1100				14	3.8	42		
FQU4N25		1750				4.3	3	37		
IRFU214B		2000				8.1	2.2	25		
IRFU214A		2000				8.5	2.2	25		
FQU3N25		2200				4	2.4	30		
FQU7N30	300	700				13	5.5	50		
FQU5N30		900				9.8	4.4	45		
FQU3N30		2200				5.5	2.4	30		
FQU2N30		3700				3.7	1.7	25		
IRFU330B	400	1000				25	4.5	48		
FQU6N40		1150				13	4.2	50		
FQU5N40		1600				10	3.4	45		
IRFU320B		1750				14	3.1	41		
IRFU320A		1800				19	3.1	41		
IRFU310B		3400				7.7	1.7	26		
FQU3N40		3400				6	2	30		
IRFU310A		3600				10	1.7	26		
FQU2N40		5800				4	1.4	25		
IRFU430B	500	1500				25	3.5	48		
FQU5N50		1800				13	3.5	50		
IRFU420B		2600				14	2.3	41		
FQU4N50		2700				10	2.6	45		
IRFU420A		3000				19	2.3	41		
FQU2N50		5300				6	1.6	30		
SSU1N50B		5500				8.3	1.3	26		
IRFU410A		5500				9.5	1.3	26		
FQU1N50		9000				4	1.1	25		
IRFU410B		10000				5.1	0.9	20		
SSU4N60B		600	2500				22	2.8	49	
FQU3N60			3600				10	2.4	50	
FQU2N60			4700				9	2	45	
SSU2N60B			5000				12.5	1.8	44	
SSU2N60A			5000				15	1.8	44	
FQU1N60	11500					5	1	30		
SSU1N60B	12000					5.9	0.9	28		
SSU1N60A	12000					7.5	0.9	28		
FQU2N80	800		6300				12	1.8	50	
FQU2N90	900	7200				12	1.7	50		
P-Channel										
RFD10P03L	-30		220			13	10	65		
FQU17P06	-60	135				21	12	44		
SFU9034		140				30	14	49		
FQU11P06		185				13	9.4	38		
SFU9024		280				15	7.8	32		
SFU2955		300				15	7.6	32		
FQU7P06		450				6.3	5.4	28		
SFU9014		500				9	5.3	24		
FQU12P10	-100	290				21	9.4	50		
SFU9130		300				30	9.8	57		
FQU8P10		530				12	6.6	44		
SFU9120	-100	600				16	4.9	32		
IRFU9120*		600				12	5.6	42		
FQU5P10		1050				6.3	3.6	25		
SFU9110		1200				9	2.8	20		
FQU7P20	-200	690				19	5.7	55		
FQU5P20		1400				10	3.7	45		
SFU9220		1500				15	3.1	30		
FQU3P20		2700				6	2.4	37		
SFU9210		3000				9	1.6	19		
FQU6P25		-250	1100				21	4.7	55	
FQU4P25	2100					10	3.1	45		
SFU9224	2400					16	2.5	30		
SFU9214	4000					9	1.5	19		
FQU2P25		4000				6.5	2	37		

IPAK (TO-251)

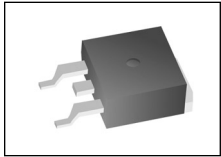


*These Industry Standard IRF devices can be specified by adding the suffix R494x to the part number when ordering. Example: IRF840AR4944. The suffix will not appear in the brand.

IPAK (TO-251)



TO-263

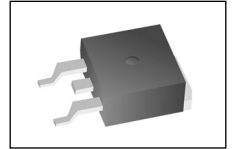


Part Number	V _{DS} (V)	R _{DS(ON)} Max. (mΩ) @ V _{GS} =				Q _g (nC) @ V _{GS} = 5V	I _D (A)	P _D (W)	Configuration
		10V	4.5V	2.5V	1.8V				
IPAK (TO-251) P-Channel (continued)									
FQU4P40	-400	3100				18	2.7	50	
FQU2P40		6500				10	1.6	38	
SFU9310		8000				17	1.5	36	
FQU3P50	-500	4900				18	2.1	50	
FQU1P50		10500				11	1.2	38	

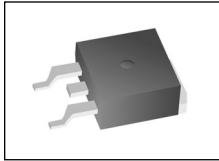
TO-263 N-Channel									
ISL9N302AS3ST	30	2.3	3.3			110	75	345	
ISL9N303AS3ST		3.2	5			68	75	215	
FDB8030L		3.5	4.5			120	80	187	
FDB7045L		4.5	6			50	100	125	
HUF76145S3S		4.5				73	75	0	
ISL9N304AS3ST		4.5	7.5			38	75	145	
HUF76143S3S		5.5	8.5			50	75	225	
FDB6676		6	7.5			43	84	93	
ISL9N306AS3ST		6	9.5			30	75	125	
FDB6670AL		6.5	8.5			35	80	75	
FDB6676S		6.7	8.2			40	76	70	SyncFET
FDB7030L		7	10				100	125	
ISL9N307AS3ST		7				28	75	100	
FDB7042L		7.5	9			32	50	83	
HUF76139S3S		7.5	11			38	75	165	
ISL9N308AS3ST		8				24	75	100	
FDB6644		8.5	15			27	50	83	
FDB7030BL		9	12			23	60	65	
HUF76137S3S		9	14			31	75	145	
ISL9N7030BLS3ST		9				24	12.9	2.5	
FDB6644S		10	12			27	55	60	SyncFET
ISL9N310AS3ST		10				17	62	70	
RF1S70N03SM		10				120	70	150	
FDB7030BLS		10.5	16.5			15	56	65	SyncFET
FDB6035L		11	19				58	75	
HUF76132S3S		11	18			25	75	120	
ISL9N312AS3ST		12				13	58	75	
FDB6035AL		12.5	17			17	48	58	
FDB6030L		13.5	20				52	75	
FQB60N03L		13.5	19			34	60	100	
ISL9N316AS3ST		15.5				13	48	65	
HUF76129S3S		16	23			19	56	105	
FDB6030BL		18	24			12	40	60	
HUF76121S3S		21	31			13	47	75	
NDB603AL		22	40				25	50	
FDB603AL		22	36				33	50	
ISL9N322AS3ST		22				8.6	33	45	
FDB4030L		35	55				20	37.5	
HUF75345S3S	55	7				125	75	325	
HRF3205S		8				170	75	175	
HUF75343S3S		9				92	75	270	
HUF75339S3S		12				60	75	200	
HUF75337S3S		14				51	75	175	
HUF75321S3S	55	34				21	35	93	
HUF76445S3S	60	6.5	7.5			124	75	310	
HUF76443S3S		8	9.5			107	75	260	
FDB5645		9.5	11@6			76	80	125	
FQB85N06		10				86	85	160	
HUF76439S3S		12	14			70	75	180	
HUF76437S3S		14	17			59	71	155	
FQB65N06		16				48	65	150	
HUF76432S3S		17	19			44	59	130	
FDB5680		20	23@6			33	40	65	
FQB55N06		20				35	55	133	
FQB50N06L		21	25			24.5	52	121	
FQB50N06		22				31	50	120	
HUF76429S3S		22	25			38	47	110	

Part Number	V _{DS} (V)	R _{DS(ON)} Max. (mΩ) @ V _{GS} =				Q _g (nC) @	I _D	P _D	Configuration
		10V	4.5V	2.5V	1.8V	V _{GS} = 5V	(A)	(W)	
TO-263 N-Channel (continued)									
FDB5690	60	27	32@6			23	32	58	
HUF76423S3S		30	35			28	35	85	
FQB30N06L		35	45			15	32	79	
HUF76419S3S		35	40			22	29	75	
FQB30N06		40				19	30	79	
FQB20N06L		55	70			9.5	21	53	
FQB20N06		60				11.5	20	53	
FQB13N06L		110	140			4.8	13.6	45	
FQB13N06		135				5.8	13	45	
HUF75545S3S	80	10				105	75	270	
HUF75542S3S		14				80	75	230	
FQB90N08		16				84	71	160	
FQB70N08		17				75	70	155	
FQB58N08		24				50	57	146	
FQB44N08		34				38	44	127	
FQB24N08		60				19	24	75	
FQB17N08L		100	115			8.8	16.5	65	
FQB17N08		115				12	16.5	65	
FQB9N08L	100	210	230			4.7	9.3	40	
FQB9N08		210				5.9	9.3	40	
HUF75645S3S		14				106	75	310	
HUF76645S3S		14	15			127	75	310	
FQB70N10		25				85	57	160	
HUF75639S3S		25				57	56	200	
FQB55N10		26				75	55	155	
HUF76639S3S		26	27			71	51	180	
HUF75637S3S		30				48	44	155	
HUF76633S3S	35	36			56	39	145		
FQB44N10	39				48	43.5	146		
IRFW550A	40				75	40	167		
HUF75631S3S	40				35	33	120		
IRFW540A	52				60	28	107		
FQB33N10L	52	55			30	33	127		
FQB33N10	52				38	33	127		
HUF75623S3S	64				23	22	85		
FQB19N10L	100	110			14	19	75		
FQB19N10	100				19	19	75		
IRFW530A	110				27	14	55		
FQB13N10L	180	200			8.7	12.8	65		
FQB13N10	180				12	12.8	65		
IRFW520A	200				16	9.2	45		
FQB7N10L	350	380			4.6	7.3	40		
FQB7N10	350				5.8	7.3	40		
IRFW510A	400				8.5	5.6	33		
IRLW510A		440			5.5	5.6	37		
IRLW520A		220			10.2	9.2	49		
IRLW530A		120			16.9	14	62		
IRLW540A		58			38.4	28	121		
FQB46N15	150	42				85	45.6	210	
HUF75842S3S		42				77	43	230	
FDB2570		80	90@6			40	22	93	
FQB28N15		90				40	28	168	
FQB16N15		160				23	16.4	108	
FQB14N15		210				18	14.4	104	
FQB9N15		400				10	9	75	
FQB6N15		600				6.5	6.4	63	
FQB5N15		800				5.4	5.4	54	
HUF75945S3ST	200	71				118	38	310	
FQB34N20L		75	80			55	31	180	
FQB34N20		75				60	31	180	
RFW650B		85				95	28	156	
HUF75939S3ST		125				64	22	180	
FDB2670		130				27	19	93	
FQB19N20L		140	150			27	21	140	
FQB19N20		150				31	19.4	140	

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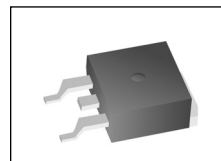
TO-263



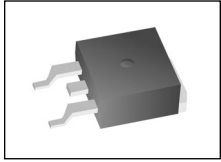
Part Number	V _{DS} (V)	R _{DS(ON)} Max. (mΩ) @ V _{GS} =				Q _g (nC) @ V _{GS} = 5V	I _D (A)	P _D (W)	Configuration
		10V	4.5V	2.5V	1.8V				
TO-263 N-Channel (continued)									
IRFW640B	200	180				45	18	139	
IRFW640A		180				44	18	139	
FQB12N20L		280	320			16	11.6	90	
FQB12N20		280				18	11.6	90	
FQB10N20L		360	380			13	10	87	
FQB10N20		360				13.5	10	87	
IRFW630B		400				22	9	72	
IRFW630A		400				22	9	72	
FQB630		400				19	9	78	
FQB7N20		690				8	6.6	63	
FQB7N20L		750	780			6.8	6.5	63	
IRFW620B		800				12	5	47	
IRFW620A		800				12	5	47	
FQB5N20L		1200	1250			4.8	4.5	52	
FQB5N20		1200				6	4.5	52	
FQB4N20L		1350	1400			4	3.8	45	
FQB4N20		1400				5	3.6	45	
IRFW610B		1500				7.2	3.3	38	
IRFW610A		1500				7	3.3	38	
IRLW610A				1500		6.1	3.3	33	
IRLW620A				800		10.3	5	39	
IRLW630A				400		18.6	9	69	
IRLW640A				180		40	18	110	
FQB27N25	250	110				50	25.5	180	
IRFW654B		140				95	15	156	
FQB16N25		230				27	16	142	
IRFW644B		280				47	14	139	
IRFW644A		280				46	14	139	
FQB9N25		420				15.5	9.4	90	
IRFW634B		450				29	8.1	74	
IRFW634A		450				30	8.1	74	
FQB8N25		550				12	8	87	
FQB6N25		1000				6.6	5.5	63	
IRFW624B		1100				13.5	4.1	49	
IRFW624A		1100				14	4.1	49	
FQB4N25		1750				4.3	3.6	52	
IRFW614B		2000				8.1	2.8	40	
IRFW614A		2000				8.5	2.8	40	
FQB3N25		2200				4	2.8	45	
FQB14N30	300	290				30	9.1	147	
FQB9N30		450				17	9	98	
FQB7N30		700				13	7	85	
FQB5N30		900				9.8	5.4	70	
FQB3N30		2200				5.5	3.2	55	
FQB2N30		3700				3.7	2.1	40	
FQB11N40	400	480				27	11.4	147	
IRFW740B		540				41	10	134	
IRFW740A		550				58	10	134	
FQB7N40		800				16.5	7	98	
IRFW730B		1000				25	5.5	73	
IRFW730A		1000				32	5.5	73	
FQB6N40		1150				13	5.5	85	
FQB5N40		1600				10	4.5	70	
IRFW720B		1750				14	3.3	46	
IRFW720A		1800				19	3.3	46	
IRFW710B		3400				7.7	2	36	
FQB3N40		3400				6	2.5	55	
IRFW710A		3600				10	2	36	
FQB6N45	450	1100				16	6.2	98	
FQB9N50	500	730				28	9	147	
IRFW840B		850				41	8	134	
IRFW840A		850				57	8	134	
FQB6N50		1300				17	5.5	98	
IRFW830A		1500				33	4.5	73	
FQB5N50		1800				13	4.5	85	

Part Number	V _{DS} (V)	R _{DS(ON)} Max. (mΩ) @ V _{GS} =				Q _g (nC) @ V _{GS} = 5V	I _D (A)	P _D (W)	Configuration
		10V	4.5V	2.5V	1.8V				
TO-263 N-Channel (continued)									
IRFW820B	500	2600				14	2.5	49	
FQB4N50		2700				10	3.4	70	
IRFW820A		3000				19	2.5	49	
FQB2N50		5300				6	2.1	55	
SSW1N50B		5500				8.3	1.5	36	
SSW1N50A		5500				11	1.5	36	
FQB12N60	600	700				42	10.5	180	
SSW10N60B		800				54	9	156	
FQB7N60		1000				29	7.4	142	
SSW7N60B		1200				38	7	147	
SSW7N60A		1200				49	7	147	
FQB6N60		1500				20	6.2	130	
FQB5N60		2000				16	5	120	
FQB4N60		2200				15	4.4	106	
SSW4N60B		2500				22	4	100	
FQB3N60		3600				10	3	75	
FQB2N60		4700				9	2.4	64	
SSW2N60B		5000				12.5	2	54	
SSW2N60A		5000				15	2	54	
FQB1N60		11500				5	1.2	40	
SSW1N60B		12000				5.9	1	34	
SSW1N60A		12000				7.5	1	34	
FQB6N70	700	1500				30	6.2	142	
FQB7N80	800	1500				40	6.6	167	
FQB6N80		1950				31	5.8	158	
SSW5N80A		2200				52	5	140	
FQB5N80		2600				25	4.8	140	
FQB4N80		3600				19	3.9	130	
FQB3N80		5000				15	3	107	
FQB2N80		6300				12	2.4	85	
FQB6N90	900	1900				40	5.8	167	
FQB5N90		2300				31	5.4	158	
FQB4N90		3100				24	4.2	140	
FQB3N90		4250				20	3.6	130	
FQB2NA90		5800				15	2.8	107	
SSW3N90A		6200				28	3	100	
FQB2N90		7200				12	2.2	85	
P-Channel									
FDB6021P	-20		30	40	65	20	28	37	
NDB6020P			50	70@2.7			24	60	
FQB47P06	-60	26				84	47	160	
FQB27P06		70				33	27	120	
FQB17P06		120				21	17	79	
SFW9Z34		140				30	18	82	
FQB11P06		175				13	11.4	53	
SFW9Z24		280				15	9.7	49	
SFW2955		300				15	9.4	49	
FQB7P06		410				6.3	7	45	
SFW9Z14		500				9	6.7	38	
FQB22P10	-100	125				40	22	125	
FQB17P10		190				30	16.5	100	
SFW9540	-100	200				43	17	132	
FQB12P10		290				21	11.5	75	
SFW9530		300				30	10.5	66	
FQB8P10		530				12	8	65	
SFW9520		600				16	6	49	
FQB5P10		1050				6.3	4.5	40	
SFW9510		1200				9	3.6	32	
FQB12P20	-200	470				31	11.5	120	
SFW9640		500				46	11	123	
FQB7P20		690				19	7.3	90	
SFW9630		800				29	6.5	70	
FQB5P20		1400				10	4.8	75	
SFW9620		1500				15	3.5	38	
FQB3P20		2700				6	2.8	52	

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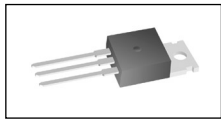
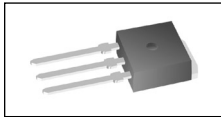


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Part Number	V _{DS} (V)	R _{DS(ON)} Max. (mΩ) @ V _{GS} =				Q _g (nC) @ V _{GS} = 5V	I _D (A)	P _D (W)	Configuration
		10V	4.5V	2.5V	1.8V				
TO-263 P-Channel (continued)									
SFW9610	-200	3000				9	1.8	20	
FQB9P25	-250	620				29	9.4	120	
SFW9644		800				45	8.6	123	
FQB6P25		1100				21	6	90	
SFW9634		1300				29	5	70	
FQB4P25		2100				10	4	75	
SFW9624		2400				16	2.7	38	
SFW9614		4000				9	1.6	20	
FQB2P25		4000				6.5	2.3	52	
FQB4P40	-400	3100				18	3.5	85	
FQB2P40	-500	6500				10	2	63	
FQB3P50		4900				18	2.7	85	
FQB1P50		10500				11	1.5	63	

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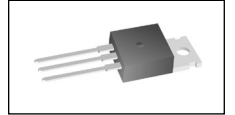
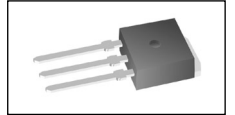
I²PAK

TO-220 / I²PAK N-Channel									
HUF76013P3	20	22	30			7.5	20	50	
HUF76009P3		27	39			5.7	20	41	
ISL9N302AP3	30	2.5	3.3			110	75	345	
ISL9N303AP3		3.2	5			61	75	215	
FDP8030L		3.5	4.5			120	80	187	
FDP7045L		4.5	6			50	100	125	
HUF76145P3		4.5	6.5			73	75	270	
ISL9N304AP3		4.5	7.5			38	75	145	
HUF76143P3		5.5	8.5			50	75	225	
FDP6676		6	7.5			43	84	93	
ISL9N306AP3		6	9.5			30	75	125	
FDP6670AL		6.5	8.5			35	80	75	
FDP6676S		6.7	8.2			40	76	70	SyncFET
FDP7030L		7	10				100	125	
ISL9N307AP3		7				28	75	100	
FDP7042L		7.5	9			32	50	83	
HUF76139P3		7.5	11			38	75	165	
ISL9N308AP3		8				24	75	100	
FDP6644		8.5	15			27	50	83	
FDP7030BL		9	12			23	60	65	
HUF76137P3		9	14			31	75	145	
ISL9N7030BLP3		9				24	75	100	
FDP6644S		10	12			27	55	60	SyncFET
ISL9N310AP3		10				17	62	70	
RF1S70N03		10				120	70	150	
RFP70N03		10				120	70	150	
FDP7030BLS		10.5	16.5			15	56	65	SyncFET
FDP6035L		11	19				58	75	
HUF76132P3		11	18			25	75	120	
ISL9N312AP3		12				13	58	75	
FDP6035AL		12.5	17			17	48	58	
FDP6030L		13.5	20				52	75	
FQP60N03L		13.5	19			34	60	100	
ISL9N316AP3		15.5				13	48	65	
HUF76129P3		16	23			19	56	105	
FDP6030BL		18	24			12	40	60	
FQP45N03L		18	25			20	45	75	
HUF76121P3		21	31			13	47	75	
FDP603AL		22	36				33	50	
NDP603AL		22	40				25	50	
ISL9N322AP3		22				8.6	33	45	
FDP4030L		35	55				20	37.5	
HUF76107P3		52	85			4.7	20	35	
BUZ11*	50	40					30	75	
BUZ71*		100					14	40	
BUZ71A*		120					13	40	
HUF75345P3	55	7				125	75	325	
HUF75345S3		7				125	75	325	
HRF3205		8				170	75	175	

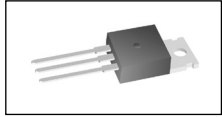
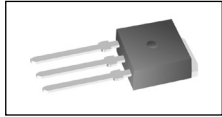
*These Industry Standard IRF devices can be specified by adding the suffix R494x to the part number when ordering. Example: IRF840AR4944. The suffix will not appear in the brand.

Part Number	V _{DS} (V)	R _{DS(ON)} Max. (mΩ) @ V _{GS} =				Q _g (nC) @ V _{GS} = 5V	I _D (A)	P _D (W)	Configuration
		10V	4.5V	2.5V	1.8V				
TO-220 / I ² PAK N-Channel (continued)									
HUF75344P3	55	8				90	75	285	
HUF75343P3		9				92	75	270	
HUF75343S3		9				92	75	270	
HUF75339P3		12				60	75	200	
HUF75337P3		14				51	75	175	
HUF75333P3		16				40	66	150	
HUF75333S3		16				40	66	150	
HUF75332P3		19				40	60	145	
HRFZ44N		22				43	49	120	
HUF75229P3		22				35	44	90	
HUF75329P3		26				35	49	128	
HUF75329S3		26				35	49	128	
HUF75321P3		34				21	35	93	
HUF75309P3		70				11	19	55	
HUF75307P3		90				9	15	45	
HUF76445P3	60	6.5	7.5			124	75	310	
HUF76443P3		8	9.5			107	75	260	
FDP5645		9.5	11@6			76	80	125	
FQPF85N06		10				86	53	62	
FQP85N06		10				86	85	160	
FQI85N06		10				86	85	160	
HUF76439P3		12	14			70	75	180	
HUF76437P3		14	17			59	71	155	
FQPF65N06		16				48	40	56	
FQP65N06		16				48	65	150	
FQI65N06		16				48	65	150	
HUF76432P3		17	19			44	59	130	
FDP5680		20	23@6			33	40	65	
FQPF55N06		20				35	33	48	
FQP55N06		20				35	55	133	
FQI55N06		20				35	55	133	
FQPF50N06L		21	25			24.5	32.6	47	
FQP50N06L		21	25			24.5	52	121	
FQI50N06L		21	25			24.5	52	121	
FQPF50N06		22				31	31	47	
FQP50N06		22				31	50	120	
FQI50N06		22				31	50	120	
HUF76429P3		22	25			38	47	110	
FDP5690		27	32@6			23	32	58	
HUF76423P3		30	35			28	35	85	
FQPF30N06L		35	45			15	22.5	38	
FQP30N06L		35	45			15	32	79	
FQI30N06L		35	45			15	32	79	
HUF76419P3		35	40			22	29	75	
FQPF30N06		40				19	21	39	
FQP30N06		40				19	30	79	
FQI30N06		40				19	30	79	
RF1S25N06		47				35	25	72	
HUF76413P3		49	56			17	23	60	
FQPF20N06L		55	70			9.5	15.7	30	
FQP20N06L		55	70			9.5	21	53	
FQI20N06L		55	70			9.5	21	53	
FQPF20N06		60				11.5	15	30	
FQP20N06		60				11.5	20	53	
FQI20N06		60				11.5	20	53	
HUF76409P3		62	70			12	18	49	
HUF76407P3		92	107			9.4	13	38	
FQPF13N06L		110	140			4.8	10	24	
FQP13N06L		110	140			4.8	13.6	45	
FQI13N06L		110	140			4.8	13.6	45	
FQPF13N06		135				5.8	9.4	24	
FQP13N06		135				5.8	13	45	
FQI13N06		135				5.8	13	45	
HUF75545P3	80	10				105	75	270	
HUF75542P3		14				80	75	230	

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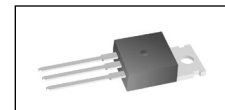
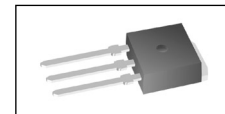
I²PAK

Part Number	V _{DS} (V)	R _{DS(ON)} Max. (mΩ) @ V _{GS} =				Q _g (nC) @	I _D	P _D	Configuration
		10V	4.5V	2.5V	1.8V	V _{GS} = 5V	(A)	(W)	
TO-220 / I ² PAK N-Channel (continued)									
FQPF90N08	80	16				84	44	62	
FQP90N08		16				84	71	160	
FQI90N08		16				84	71	160	
FQPF70N08		17				75	43.6	60	
FQP70N08		17				75	70	155	
FQI70N08		17				75	70	155	
FQPF58N08		24				50	35	55	
FQP58N08		24				50	57	146	
FQI58N08		24				50	57	146	
FQPF44N08		34				38	25	41	
FQP44N08		34				38	44	127	
FQI44N08		34				38	44	127	
FQPF24N08		60				19	17	38	
FQP24N08		60				19	24	75	
FQI24N08		60				19	24	75	
FQPF17N08L		100	115			8.8	11.2	30	
FQP17N08L		100	115			8.8	16.5	65	
FQI17N08L		100	115			8.8	16.5	65	
FQPF17N08		115				12	11.2	30	
FQP17N08		115				12	16.5	65	
FQI17N08		115				12	16.5	65	
FQPF9N08L		210	230			4.7	7	23	
FQPF9N08		210				5.9	7	23	
FQP9N08L		210	230			4.7	9.3	40	
FQI9N08L		210	230			4.7	9.3	40	
FQP9N08		210				5.9	9.3	40	
FQI9N08		210				5.9	9.3	40	
HUF75645P3	100	14				106	75	310	
HUF76645P3		14	15			127	75	310	
SSS70N10A		23				151	28	49	
FQPF70N10		25				85	35	62	
FQP70N10		25				85	57	160	
FQI70N10		25				85	57	160	
HUF75639P3		25				57	56	200	
HUF75639S3		25				57	56	200	
FQPF55N10		26				75	34.2	60	
FQP55N10		26				75	55	155	
FQI55N10		26				75	55	155	
HUF76639P3		26	27			71	51	180	
HUF75637P3		30				48	44	155	
HUF76633P3		35	36			56	39	145	
FQPF44N10		39				48	27	55	
FQP44N10		39				48	43.5	146	
FQI44N10		39				48	43.5	146	
IRFS550A		40				75	21	46	
IRFI550A		40				75	40	167	
IRF550A		40				75	40	167	
HUF75631P3		40				35	33	120	
IRF540N*		40				35	33	120	
IRFS540A		52				60	17	39	
FQPF33N10L		52	55			30	18	41	
FQPF33N10		52				38	18	41	
IRFI540A		52				60	28	107	
IRF540A		52				60	28	107	
FQP33N10L		52	55			30	33	127	
FQI33N10L		52	55			30	33	127	
FQP33N10		52				38	33	127	
FQI33N10		52				38	33	127	
HUF75623P3		64				23	22	85	
IRF530N*		64				23	22	85	
IRF540*		77				38	28	120	
FQPF19N10L		100	110			14	13.6	38	
FQPF19N10		100				19	13.6	38	
FQP19N10L		100	110			14	19	75	
FQI19N10L		100	110			14	19	75	

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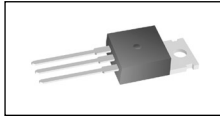
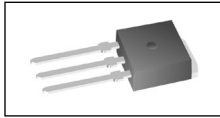
Part Number	V _{DS} (V)	R _{DS(ON)} Max. (mΩ) @ V _{GS} =				Q _g (nC) @ V _{GS} = 5V	I _D (A)	P _D (W)	Configuration	
		10V	4.5V	2.5V	1.8V					
TO-220 / I ² PAK N-Channel (continued)										
FQP19N10	100	100				19	19	75		
FQI19N10		100				19	19	75		
IRFS530A		110				27	10.7	32		
IRFI530A		110				27	14	55		
IRF530A		110				27	14	55		
IRF530*		160				18	14	79		
FQPF13N10L		180	200			8.7	8.7	30		
FQPF13N10		180				12	8.7	30		
FQP13N10L		180	200			8.7	12.8	65		
FQI13N10L		180	200			8.7	12.8	65		
FQP13N10		180				12	12.8	65		
FQI13N10		180				12	12.8	65		
IRFS520A		200				16	7.2	28		
IRFI520A		200				16	9.2	45		
IRF520A		200				16	9.2	45		
IRF520*		270				10	9.2	60		
FQPF7N10L		350	380			4.6	5.5	23		
FQPF7N10		350				5.8	5.5	23		
FQP7N10L		350	380			4.6	7.3	40		
FQI7N10L		350	380			4.6	7.3	40		
FQP7N10		350				5.8	7.3	40		
FQI7N10		350				5.8	7.3	40		
IRFS510A		400				8.5	4.5	21		
IRFI510A		400				8.5	5.6	33		
IRF510A		400				8.5	5.6	33		
IRF510*		540				5	5.6	43		
IRLS510A				440		5.5	4.5	23		
IRLI510A				440		5.5	5.6	37		
IRL510A				440		5.5	5.6	37		
IRLS520A				220		10.2	7.2	30		
IRLI520A				220		10.2	9.2	49		
IRL520A				220		10.2	9.2	49		
IRLS530A				120		16.9	10.7	36		
IRLI530A				120		16.9	14	62		
IRL530A				120		16.9	14	62		
IRLS540A				58		38.4	17	44		
IRLI540A				58		38.4	28	121		
IRL540A				58		38.4	28	121		
FQPF46N15	150	42				85	25.6	66		
FQP46N15		42				85	45.6	210		
FQI46N15		42				85	45.6	210		
HUF75842P3		42				77	43	230		
HUF75842S3		42				77	43	230		
FDP2570		80	90@6			40	22	93		
FQPF28N15		90				40	16.7	60		
FQP28N15		90				40	28	168		
FQI28N15		90				40	28	168		
FQPF16N15		160				23	11.6	53		
FQP16N15		160				23	16.4	108		
FQI16N15		160				23	16.4	108		
FQPF14N15		210				18	9.8	48		
FQP14N15		150	210				18	14.4	104	
FQI14N15			210				18	14.4	104	
FQPF9N15			400				10	6.9	44	
FQP9N15			400				10	9	75	
FQI9N15			400				10	9	75	
FQPF6N15	600					6.5	5	38		
FQP6N15	600					6.5	6.4	63		
FQI6N15	600					6.5	6.4	63		
FQPF5N15	800					5.4	4.2	32		
FQP5N15	800					5.4	5.4	54		
FQI5N15	800					5.4	5.4	54		
SSS45N20B	200		65				133	20	57	
SSP45N20B		65				133	35	176		
HUF75945P3		71				118	38	310		

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I²PAK

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TO-220

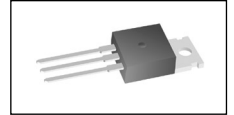
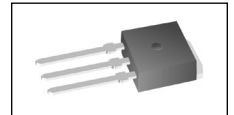
I²PAK

Part Number	V _{DS} (V)	R _{DS(ON)} Max. (mΩ) @ V _{GS} =				Q _g (nC) @ V _{GS} = 5V	I _D (A)	P _D (W)	Configuration
		10V	4.5V	2.5V	1.8V				
TO-220 / I ² PAK N-Channel (continued)									
FQPF34N20L	200	75	80			55	17.5	55	
FQPF34N20		75				60	17.5	55	
FQP34N20L		75	80			55	31	180	
FQI34N20L		75	80			55	31	180	
FQP34N20		75				60	31	180	
FQI34N20		75				60	31	180	
IRFS650B		85				95	15.8	50	
IRFS650A		85				95	15.8	50	
IRFI650B		85				95	28	156	
IRF650B		85				95	28	156	
HUF75939P3		125				64	22	180	
FDP2670		130				27	19	93	
FQPF19N20L		140	150			27	12.8	50	
FQP19N20L		140	150			27	21	140	
FQI19N20L		140	150			27	21	140	
FQPF19N20		150				31	11.8	50	
FQP19N20		150				31	19.4	140	
FQI19N20		150				31	19.4	140	
IRF640N*		150				64	18	150	
IRFS640B		180				45	9.8	43	
IRFS640A		180				44	9.8	43	
IRFI640B		180				45	18	139	
IRFI640A		180				44	18	139	
IRF640B		180				45	18	139	
IRF640A		180				44	18	139	
IRF640*		180				43	18	125	
HUF75925P3		275				32	11	100	
FQPF12N20L		280	320			16	8.2	45	
FQPF12N20		280				18	8.2	45	
FQP12N20L		280	320			16	11.6	90	
FQI12N20L		280	320			16	11.6	90	
FQP12N20		280				18	11.6	90	
FQI12N20		280				18	11.6	90	
IRF630N*		300				32	9.3	82	
FQPF10N20L		360	380			13	6.8	40	
FQPF10N20		360				13.5	6.8	40	
FQP10N20L		360	380			13	10	87	
FQI10N20L		360	380			13	10	87	
FQP10N20		360				13.5	10	87	
FQI10N20		360				13.5	10	87	
FQPF630	400				19	6.3	38		
IRFS630B	400				22	6.5	38		
IRFS630A	400				22	6.5	38		
IRFI630B	400				22	9	72		
IRFI630A	400				22	9	72		
IRF630B	400				22	9	72		
IRF630A	400				22	9	72		
FQP630	400				19	9	78		
FQI630	400				19	9	78		
IRF630*									
FQPF7N20		690				8	4.8	37	
FQP7N20		690				8	6.6	63	
FQI7N20		690				8	6.6	63	
FQPF7N20L		750	780			6.8	5	37	
FQP7N20L		750	780			6.8	6.5	63	
FQI7N20L		750	780			6.8	6.5	63	
IRFS620B		800				12	4.1	32	
IRFS620A		800				12	4.1	32	
IRFI620B		800				12	5	47	
IRFI620A		800				12	5	47	
IRF620B		800				12	5	47	
IRF620A		800				12	5	47	
IRF620*		800				11	5	40	
FQPF5N20L		1200	1250			4.8	3.5	32	
FQPF5N20		1200				6	3.5	32	

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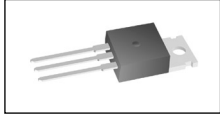
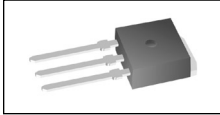
Part Number	V _{DS} (V)	R _{DS(ON)} Max. (mΩ) @ V _{GS} =				Q _g (nC) @	I _D	P _D	Configuration
		10V	4.5V	2.5V	1.8V	V _{GS} = 5V	(A)	(W)	
TO-220 / I ² PAK N-Channel (continued)									
FQP5N20L	200	1200	1250			4.8	4.5	52	
FQI5N20L		1200	1250			4.8	4.5	52	
FQP5N20		1200				6	4.5	52	
FQI5N20		1200				6	4.5	52	
FQPF4N20L		1350	1400			4	3	27	
FQP4N20L		1350	1400			4	3.8	45	
FQI4N20L		1350	1400			4	3.8	45	
FQPF4N20		1400				5	2.8	27	
FQP4N20		1400				5	3.6	45	
FQI4N20		1400				5	3.6	45	
IRFS610B		1500				7.2	2.5	22	
IRFS610A		1500				7	2.5	22	
IRFI610B		1500				7.2	3.3	38	
IRFI610A		1500				7	3.3	38	
IRF610B		1500				7.2	3.3	38	
IRF610A		1500				7	3.3	38	
IRF610*		1500				5.3	3.3	43	
IRLS610A			1500			6.1	2.5	19	
IRLI610A			1500			6.1	3.3	33	
IRL610A			1500			6.1	3.3	33	
IRLS620A			800			10.3	4.1	26	
IRLI620A			800			10.3	5	39	
IRL620A			800			10.3	5	39	
IRLS630A		400			18.6	6.5	36		
IRLI630A		400			18.6	9	69		
IRL630A		400			18.6	9	69		
IRLS640A		180			40	9.8	40		
IRLI640A		180			40	18	110		
IRL640A		180			40	18	110		
FQPF27N25	250	110				50	14	55	
FQP27N25		110				50	25.5	180	
FQI27N25		110				50	25.5	180	
IRFS654B		140				95	12	50	
IRFS654A		140				88	12	50	
IRFI654B		140				95	15	156	
IRF654B		140				95	15	156	
FQPF16N25		230				27	9.5	50	
FQP16N25		230				27	16	142	
FQI16N25		230				27	16	142	
IRFS644B		280				47	7.9	43	
IRFS644A		280				46	7.9	43	
IRFI644B		280				47	14	139	
IRFI644A		280				46	14	139	
IRF644B		280				47	14	139	
IRF644A		280				46	14	139	
FQPF9N25		420				15.5	6.7	45	
FQP9N25		420				15.5	9.4	90	
FQI9N25		420				15.5	9.4	90	
IRFS634B		450				29	5.8	38	
IRFS634A		450				30	5.8	38	
IRFI634B		450				29	8.1	74	
IRFI634A		450				30	8.1	74	
IRF634B		450				29	8.1	74	
IRF634A		450				30	8.1	74	
FQPF8N25		550				12	5.5	40	
FQP8N25		550				12	8	87	
FQI8N25		550				12	8	87	
FQPF6N25		1000				6.6	4	37	
FQP6N25		1000				6.6	5.5	63	
FQI6N25		1000				6.6	5.5	63	
IRFS624B		1100				13.5	3.4	34	
IRFS624A	1100				14	3.4	34		
IRFI624B	1100				13.5	4.1	49		
IRFI624A	1100				14	4.1	49		
IRF624B	1100				13.5	4.1	49		

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TO-220

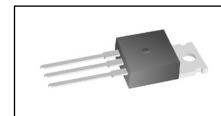
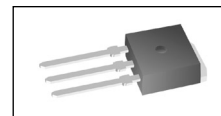
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Part Number	V _{DS} (V)	R _{DS(ON)} Max. (mΩ) @ V _{GS} =				Q _g (nC) @ V _{GS} = 5V	I _D (A)	P _D (W)	Configuration
		10V	4.5V	2.5V	1.8V				
TO-220 / I ² PAK N-Channel (continued)									
IRF624A	250	1100				14	4.1	49	
FQPF4N25		1750				4.3	2.8	32	
FQP4N25		1750				4.3	3.6	52	
FQI4N25		1750				4.3	3.6	52	
IRFS614B		2000				8.1	2.1	22	
IRFS614A		2000				8.5	2.1	22	
IRFI614B		2000				8.1	2.8	40	
IRFI614A		2000				8.5	2.8	40	
IRF614B		2000				8.1	2.8	40	
IRF614A		2000				8.5	2.8	40	
FQPF3N25		2200				4	2.3	27	
FQP3N25		2200				4	2.8	45	
FQI3N25		2200				4	2.8	45	
IRF646*	275	280				39	14	125	
FQPF22N30	300	160				47	12	56	
FQP22N30		160				47	21	170	
FQPF14N30		290				30	8.5	50	
FQP14N30		290				30	9.1	147	
FQI14N30		290				30	9.1	147	
FQPF9N30		450				17	6	42	
FQP9N30		450				17	9	98	
FQI9N30		450				17	9	98	
FQPF7N30		700				13	4.9	39	
FQP7N30		700				13	7	85	
FQI7N30		700				13	7	85	
FQPF5N30		900				9.8	3.9	35	
FQP5N30		900				9.8	5.4	70	
FQI5N30		900				9.8	5.4	70	
FQPF3N30		2200				5.5	2	20	
FQP3N30		2200				5.5	3.2	55	
FQI3N30		2200				5.5	3.2	55	
FQP2N30		3700				3.7	1.3	16	
FQPF2N30		3700				3.7	2.1	40	
FQI2N30		3700				3.7	2.1	40	
FQPF17N40	400	270				45	9.5	56	
FQP17N40		270				45	16	170	
IRFS750A		300				101	8.4	49	
FQPF11N40		480				27	6.6	50	
FQP11N40		480				27	11.4	147	
FQI11N40		480				27	11.4	147	
IRFS740B		540				41	5.7	44	
IRFI740B		540				41	10	134	
IRF740B		540				41	10	134	
IRFS740A		550				58	5.7	44	
IRFI740A		550				58	10	134	
IRF740A		550				58	10	134	
IRF740A*		550				25	10	147	
IRF740*		550				41	10	125	
FQPF7N40		800				16.5	4.6	42	
FQP7N40		800				16.5	7	98	
FQI7N40		800				16.5	7	98	
IRFS730B		1000				25	3.9	38	
IRFS730A		1000				32	3.9	38	
IRFI730B		1000				25	5.5	73	
IRFI730A		1000				32	5.5	73	
IRF730B		1000				25	5.5	73	
IRF730A		1000				32	5.5	73	
IRF730*		1000				20	5.5	75	
FQPF6N40		1150				13	3.7	39	
FQP6N40		1150				13	5.5	85	
FQI6N40		1150				13	5.5	85	
FQPF5N40		1600				10	3	35	
FQP5N40		1600				10	4.5	70	
FQI5N40		1600				10	4.5	70	
IRFS720B		1750				14	2.8	33	

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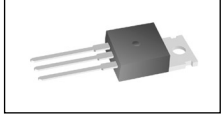
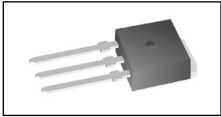
Part Number	V _{DS} (V)	R _{DS(ON)} Max. (mΩ) @ V _{GS} =				Q _g (nC) @ V _{GS} = 5V	I _D (A)	P _D (W)	Configuration	
		10V	4.5V	2.5V	1.8V					
TO-220 / I ² PAK N-Channel (continued)										
IRFI720B	400	1750				14	3.3	46		
IRF720B		1750				14	3.3	46		
IRFS720A		1800				19	2.8	33		
IRFI720A		1800				19	3.3	46		
IRF720A		1800				19	3.3	46		
IRF720*		1800				12	3.3	50		
IRFS710B		3400				7.7	1.6	23		
FQPF3N40		3400				6	1.6	20		
IRFI710B		3400				7.7	2	36		
IRF710B		3400				7.7	2	36		
FQP3N40		3400				6	2.5	55		
FQI3N40		3400				6	2.5	55		
IRFS710A		3600				10	1.6	23		
IRFI710A		3600				10	2	36		
IRF710A		3600				10	2	36		
IRF710*		3600				7	2	36		
FQPF2N40		5800				4	1.1	16		
FQP2N40		5800				4	1.8	40		
FQPF6N45		450	1100				16	4	42	
FQP6N45			1100				16	6.2	98	
FQI6N45	1100					16	6.2	98		
FQPF13N50	500	430				45	7.3	56		
FQP13N50		430				45	12.5	170		
FQPF9N50		730				28	5.3	50		
FQP9N50		730				28	9	147		
FQI9N50		730				28	9	147		
IRFS840B		850				41	4.6	44		
IRFS840A		850				57	4.6	44		
IRFI840B		850				41	8	134		
IRFI840A		850				57	8	134		
IRF840B		850				41	8	134		
IRF840A		850				57	8	134		
IRF840A*		850				20	8	147		
IRF840*		850				42	8	125		
FQPF6N50		1300				17	3.6	42		
FQP6N50		1300				17	5.5	98		
FQI6N50		1300				17	5.5	98		
IRFS830A		1500				33	3.1	38		
IRFI830A		1500				33	4.5	73		
IRF830A		1500				33	4.5	73		
IRF830*		1500				22	4.5	75		
FQPF5N50		1800				13	3	39		
FQP5N50		1800				13	4.5	85		
FQI5N50		1800				13	4.5	85		
IRFS820B		2600				14	2.1	33		
IRFI820B		2600				14	2.5	49		
IRF820B		2600				14	2.5	49		
FQPF4N50		2700				10	2.3	35		
FQP4N50		2700				10	3.4	70		
FQI4N50		2700				10	3.4	70		
IRFS820A		3000				19	2.1	33		
IRFI820A		3000				19	2.5	49		
IRF820A		3000				19	2.5	49		
IRF820*		3000				12	2.5	50		
FQPF2N50		5300				6	1.3	20		
FQP2N50		5300				6	2.1	55		
FQI2N50		5300				6	2.1	55		
SSS1N50B		5500				8.3	1.2	23		
SSS1N50A		5500				11	1.2	23		
SSP1N50B		5500				8.3	1.5	36		
SSP1N50A		5500				11	1.5	36		
SSI1N50B	5500				8.3	1.5	36			
SSI1N50A	5500				11	1.5	36			
FQP1N50	9000				4	1.4	40			
FQPF1N50	9000				4	0.9	16			

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TO-220

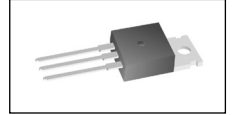
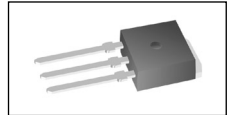
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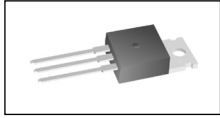
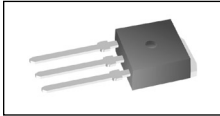
Part Number	V _{DS} (V)	R _{DS(ON)} Max. (mΩ) @ V _{GS} =				Q _g (nC) @	I _D	P _D	Configuration
		10V	4.5V	2.5V	1.8V	V _{GS} = 5V	(A)	(W)	
TO-220 / I ² PAK N-Channel (continued)									
FQPF12N60	600	700				42	5.8	55	
FQP12N60		700				42	10.5	180	
FQI12N60		700				42	10.5	180	
SSS10N60B		800				54	5.1	50	
SSS10N60A		800				74	5.1	50	
SSP10N60B		800				54	9	156	
SSP10N60A		800				74	9	156	
SSI10N60B		800				54	9	156	
FQPF7N60		1000				29	4.3	48	
FQP7N60		1000				29	7.4	142	
FQI7N60		1000				29	7.4	142	
SSS7N60B		1200				38	4	48	
SSS7N60A		1200				49	4	48	
SSP7N60B		1200				38	7	147	
SSP7N60A		1200				49	7	147	
SSI7N60B		1200				38	7	147	
SSI7N60A		1200				49	7	147	
IRFBC40*		1200				40	6.2	125	
FQPF6N60		1500				20	6.2	44	
FQP6N60		1500				20	6.2	130	
FQI6N60		1500				20	6.2	130	
FQPF5N60		2000				16	2.8	40	
FQP5N60		2000				16	5	120	
FQI5N60		2000				16	5	120	
FQPF4N60		2200				15	2.6	36	
FQP4N60		2200				15	4.4	106	
FQI4N60		2200				15	4.4	106	
SSS4N60B		2500				22	2.3	33	
SSS4N60AS		2500				25	2.3	33	
SSP4N60B		2500				22	4	100	
SSP4N60AS		2500				25	4	100	
SSI4N60B		2500				22	4	100	
FQPF3N60		3600				10	2	34	
FQP3N60		3600				10	3	75	
FQI3N60		3600				10	3	75	
FQPF2N60		4700				9	1.6	28	
FQP2N60		4700				9	2.4	64	
FQI2N60		4700				9	2.4	64	
SSS2N60B		5000				12.5	1.3	23	
SSS2N60A		5000				15	1.3	23	
SSP2N60B	5000				12.5	2	54		
SSP2N60A	5000				15	2	54		
SSI2N60B	5000				12.5	2	54		
SSI2N60A	5000				15	2	54		
FQP1N60	11500				5	1.2	40		
FQI1N60	11500				5	1.2	40		
FQPF1N60	11500				5	0.9	21		
SSS1N60B	12000				5.9	0.7	17		
SSS1N60A	12000				7.5	0.7	17		
SSP1N60B	12000				5.9	1	34		
SSP1N60A	12000				7.5	1	34		
SSI1N60B	12000				5.9	1	34		
SSI1N60A	12000				7.5	1	34		
FQPF6N70	700	1500				30	3.5	48	
FQP6N70		1500				30	6.2	142	
FQI6N70		1500				30	6.2	142	
SSS6N70A		1800				51	4	40	
SSP6N70A	800	1800				51	6	130	
SSI6N70A		1800				51	6	130	
FQPF7N80		1500				40	3.8	56	
FQP7N80		1500				40	6.6	167	
FQI7N80	800	1500				40	6.6	167	
SSS7N80A		1800				67	4	50	
SSP7N80A		1800				67	7	160	
FQPF6N80		1950				31	3.3	51	

Part Number	V _{DS} (V)	R _{DS(ON)} Max. (mΩ) @ V _{GS} =				Q _g (nC) @	I _D	P _D	Configuration
		10V	4.5V	2.5V	1.8V	V _{GS} = 5V	(A)	(W)	
TO-220 / I ² PAK N-Channel (continued)									
FQP6N80	800	1950				31	5.8	158	
FQI6N80		1950				31	5.8	158	
SSS6N80A		2000				67	3.5	50	
SSP6N80A		2000				67	6	160	
SSS5N80A		2200				52	3	45	
SSP5N80A		2200				52	5	140	
SSI5N80A		2200				52	5	140	
FQPF5N80		2600				25	2.8	47	
FQP5N80		2600				25	4.8	140	
FQI5N80		2600				25	4.8	140	
SSS4N80AS		3000				40	2.8	40	
SSP4N80AS		3000				40	4.5	130	
FQPF4N80		3600				19	2.2	43	
FQP4N80		3600				19	3.9	130	
FQI4N80		3600				19	3.9	130	
SSS4N80A		4000				32	2.5	40	
SSP4N80A		4000				32	4	120	
SSS3N80A		4800				27	2	35	
SSP3N80A		4800				27	3	100	
FQPF3N80		5000				15	1.8	39	
FQP3N80		5000				15	3	107	
FQI3N80		5000				15	3	107	
SSI2N80A		6000				22	2	80	
FQPF2N80		6300				12	1.5	35	
FQP2N80		6300				12	2.4	85	
FQI2N80		6300				12	2.4	85	
FQPF6N90	900	1900				40	3.4	56	
FQP6N90		1900				40	5.8	167	
FQI6N90		1900				40	5.8	167	
FQPF5N90		2300				31	3	51	
SSS6N90A		2300				68	3.5	50	
FQP5N90		2300				31	5.4	158	
FQI5N90		2300				31	5.4	158	
SSP6N90A		2300				68	6	160	
SSS5N90A		2900				54	3	45	
SSP5N90A		2900				54	5	140	
FQPF4N90		3100				24	2.5	47	
FQP4N90		3100				24	4.2	140	
FQI4N90		3100				24	4.2	140	
SSS4N90AS		3700				42	2.8	40	
SSP4N90AS		3700				42	4.5	130	
FQPF3N90		4250				20	2.1	43	
FQP3N90		4250				20	3.6	130	
FQI3N90		4250				20	3.6	130	
SSP4N90A		5000				35	4	120	
FQPF2NA90		5800				15	1.7	39	
FQP2NA90		5800				15	2.8	107	
FQI2NA90		5800				15	2.8	107	
SSS3N90A		6200				28	2	35	
SSI3N90A		6200				28	3	100	
SSS2N90A		7000				24	1.5	30	
SSP2N90A		7000				24	2	80	
FQPF2N90		7200				12	1.4	35	
FQP2N90		7200				12	2.2	85	
FQI2N90		7200				12	2.2	85	
RFP4N100	1000	3500				55	4.3	150	
P-Channel									
FDP6021P	-20		30	40	65	20	28	37	
NDP6020P			50	70@2.7			24	60	
FDP4020P			80	110			16	37.5	
FQPF47P06	-60	26				84	30	62	
FQP47P06		26				84	47	160	
FQI47P06		26				84	47	160	
FQPF27P06		70				33	17	47	
FQP27P06		70				33	27	120	

TO-220

I²PAK

TO-220

I²PAK

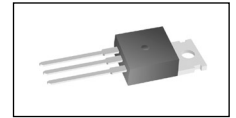
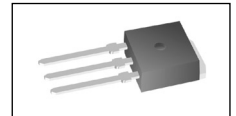
Part Number	V _{DS} (V)	R _{DS(ON)} Max. (mΩ) @ V _{GS} =				Q _g (nC) @	I _D	P _D	Configuration
		10V	4.5V	2.5V	1.8V	V _{GS} = 5V	(A)	(W)	
TO-220 / I ² PAK P-Channel (continued)									
FQI27P06	-60	70				33	27	120	
FQPF17P06		120				21	12	39	
FQP17P06		120				21	17	79	
FQI17P06		120				21	17	79	
SFS9Z34		140				30	12	36	
SFP9Z34		140				30	18	82	
SFI9Z34		140				30	18	82	
FQPF11P06		175				13	8.6	30	
FQP11P06		175				13	11.4	53	
FQI11P06		175				13	11.4	53	
MTP2955V		200					12	60	
SFS9Z24		280				15	7.5	29	
SFP9Z24		280				15	9.7	49	
SFI9Z24		280				15	9.7	49	
SFS2955		300				15	7.3	29	
SFP2955		300				15	9.4	49	
SFI2955		300				15	9.4	49	
FQPF7P06		410				6.3	5.3	24	
FQP7P06		410				6.3	7	45	
FQI7P06		410				6.3	7	45	
SFS9Z14		500				9	5.3	24	
SFP9Z14		500				9	6.7	38	
SFI9Z14		500				9	6.7	38	
FQPF22P10	-100	125				40	13.2	45	
FQP22P10		125				40	22	125	
FQI22P10		125				40	22	125	
FQPF17P10		190				30	10.5	41	
FQP17P10		190				30	16.5	100	
FQI17P10		190				30	16.5	100	
SFS9540		200				43	10.7	53	
SFP9540		200				43	17	132	
SFI9540		200				43	17	132	
IRF9540*		200				70	19	150	
FQPF12P10		290				21	8.2	38	
FQP12P10		290				21	11.5	75	
FQI12P10		290				21	11.5	75	
SFS9530		300				30	8	39	
SFP9530		300				30	10.5	66	
SFI9530		300				30	10.5	66	
IRF9530*		300				25	12	75	
FQPF8P10		530				12	5.3	28	
FQP8P10		530				12	8	65	
FQI8P10		530				12	8	65	
SFS9520		600				16	4.6	29	
SFP9520		600				16	6	49	
SFI9520		600				16	6	49	
IRF9520*		600				16	6	40	
FQPF5P10		1050				6.3	2.9	23	
FQP5P10		1050				6.3	4.5	40	
FQI5P10		1050				6.3	4.5	40	
SFS9510		1200				9	2.5	16	
SFP9510		1200				9	3.6	32	
SFI9510		1200				9	3.6	32	
IRF9510*		1200				8.5	3	20	
FQPF12P20	-200	470				31	7.3	50	
FQP12P20		470				31	11.5	120	
FQI12P20		470				31	11.5	120	
SFS9640		500				46	6.2	40	
SFP9640		500				46	11	123	
SFI9640		500				46	11	123	
IRF9640*		500				70	11	125	
FQPF7P20		690				19	5.2	45	
FQP7P20		690				19	7.3	90	
FQI7P20		690				19	7.3	90	
SFS9630		800				29	4.4	33	

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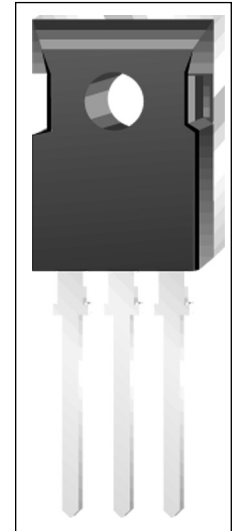
Part Number	V _{DS} (V)	R _{DS(ON)} Max. (mΩ) @ V _{GS} =				Q _g (nC) @ V _{GS} = 5V	I _D (A)	P _D (W)	Configuration
		10V	4.5V	2.5V	1.8V				
TO-220 / I ² PAK P-Channel (continued)									
SFP9630	-200	800				29	6.5	70	
SFI9630		800				29	6.5	70	
IRF9630*		800				31	6.5	75	
FQPF5P20		1400				10	3.4	38	
FQP5P20		1400				10	4.8	75	
FQI5P20		1400				10	4.8	75	
SFS9620		1500				15	3	28	
SFP9620		1500				15	3.5	38	
SFI9620		1500				15	3.5	38	
IRF9620*		1500				16	3.5	40	
FQPF3P20		2700				6	2.2	32	
FQP3P20		2700				6	2.8	52	
FQI3P20		2700				6	2.8	52	
SFS9610		3000				9	1.4	13	
SFP9610		3000				9	1.8	20	
SFI9610		3000				9	1.8	20	
FQPF9P25	-250	620				29	6	50	
FQP9P25		620				29	9.4	120	
FQI9P25		620				29	9.4	120	
SFS9644		800				45	4.9	40	
SFP9644		800				45	8.6	123	
SFI9644		800				45	8.6	123	
FQPF6P25		1100				21	4.2	45	
FQP6P25		1100				21	6	90	
FQI6P25		1100				21	6	90	
SFS9634		1300				29	3.4	33	
SFP9634		1300				29	5	70	
SFI9634		1300				29	5	70	
FQPF4P25		2100				10	2.8	38	
FQP4P25		2100				10	4	75	
FQI4P25		2100				10	4	75	
SFS9624		2400				16	2.4	28	
SFP9624		2400				16	2.7	38	
SFI9624		2400				16	2.7	38	
SFS9614		4000				9	1.3	13	
SFP9614		4000				9	1.6	20	
SFI9614		4000				9	1.6	20	
FQPF2P25		4000				6.5	1.8	32	
FQP2P25		4000				6.5	2.3	52	
FQI2P25		4000				6.5	2.3	52	
FQPF4P40	-400	3100				18	2.4	39	
FQP4P40		3100				18	3.5	85	
FQI4P40		3100				18	3.5	85	
FQPF2P40		6500				10	1.3	28	
FQP2P40		6500				10	2	63	
FQI2P40		6500				10	2	63	
FQPF3P50	-500	4900				18	1.9	39	
FQP3P50		4900				18	2.7	85	
FQI3P50		4900				18	2.7	85	
FQPF1P50		10500				11	1	28	
FQP1P50		10500				11	1.5	63	
FQI1P50		10500				11	1.5	63	

TO-247/TO-3P/PWR-247 N-Channel									
RFG75N05E	50	8				170	75	240	
HUF75345G3	55	7				125	75	325	
HUF75344G3		8				90	75	285	
HUF75343G3		9				92	75	270	
HUF75339G3		12				60	75	200	
HUF75332G3	60	19				40	60	145	
HUF75329G3		26				35	49	128	
FQA170N06		5.6				220	170	375	
FQAF85N06		10				86	67	100	
FQA85N06		10				86	100	214	

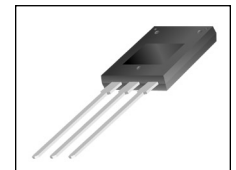
TO-220

I²PAK

TO-247

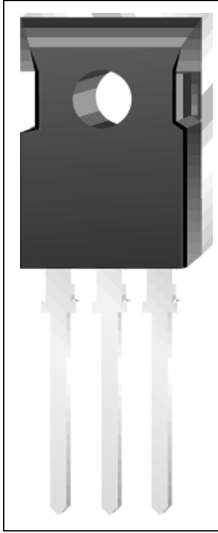


PWR-247

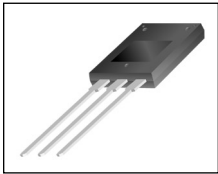


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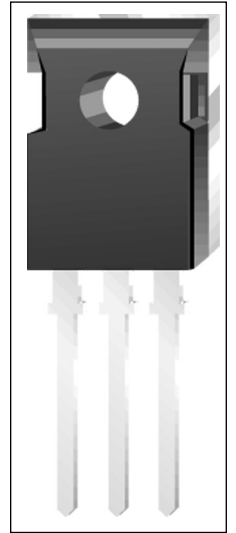


Part Number	V _{DS} (V)	R _{DS(ON)} Max. (mΩ) @ V _{GS} =				Q _g (nC) @ V _{GS} = 5V	I _D (A)	P _D (W)	Configuration
		10V	4.5V	2.5V	1.8V				
TO-247/TO-3P/PWR-247 N-Channel (continued)									
FQAF65N06	60	16				48	49	86	
FQA65N06		16				48	72	183	
FQA160N08	80	7				220	160	375	
FQAF90N08		16				84	56	100	
FQA90N08		16				84	90	214	
FQAF70N08		17				75	53	90	
FQA70N08		17				75	77	190	
FQAF58N08		24				50	44	85	
FQA58N08		24				50	64	180	
FQAF44N08		34				38	35.6	83	
FQA44N08		34				38	49.8	163	
HUF75652G3		100	8				211	75	515
FQA140N10	10					220	140	375	
SSF70N10A	23					151	44	120	
SSH70N10A	23					151	70	300	
FQAF70N10	25					85	45	100	
FQA70N10	25					85	70	214	
HUF75639G3	25					57	56	200	
FQAF55N10	26					75	41.9	90	
FQA55N10	26					75	61	190	
IRFP150N*	30					48	44	155	
FQAF44N10	39					48	33	85	
FQA44N10	39					48	48	180	
IRFS150A	40					75	31	100	
IRFP150A	40					75	43	193	
IRFP140N*	40					35	33	120	
IRFS140A	52					60	23	72	
FQAF33N10L	52		55			30	25.8	83	
FQAF33N10	52					38	25.8	83	
IRFP140A	52					60	31	131	
FQA33N10L	52		55			30	36	163	
FQA33N10	52					38	36	163	
IRFP150*	55					70	40	180	
IRFP140*	77					38	27	180	
HUF75852G3	150		16				215	75	500
FQA90N15		18				220	90	375	
FQAF70N15		28				135	44	130	
FQA70N15		28				135	70	330	
FQAF46N15		42				85	33.5	113	
FQA46N15		42				85	50	250	
SFH154		75				90	34	204	
FQAF28N15		90				40	22	102	
FQA28N15		90				40	33	227	
FQA65N20	200	32				170	65	310	
FQAF48N20		50				100	30	108	
FQA48N20		50				100	48	280	
SSF45N20B		65				133	26.4	100	
SSF45N20A		65				117	26.4	100	
SSH45N20B		65				133	45	278	
SSH45N20A		65				117	45	278	
HUF75945G3		71				118	38	310	
FQAF34N20L		75	80			55	23	95	
FQAF34N20		75				60	23	95	
FQA34N20L		75	80			55	34	210	
FQA34N20		75				60	34	210	
IRFP250N*		75				114	30	214	
IRFS250B		85				95	21.3	90	
IRFS250A		85				95	21.3	90	
IRFP250B		85				95	32	204	
IRFP250A		85				95	32	204	
IF4E33N20S		85				120	33		
IRFP250*		85				79	33	180	
FQAF19N20L		140	150			27	16	85	
FQA19N20L		140	150			27	25	190	
FQAF19N20		150				31	15	85	

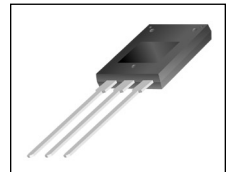
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Part Number	V _{DS} (V)	R _{DS(ON)} Max. (mΩ) @ V _{GS} =				Q _g (nC) @ V _{GS} = 5V	I _D (A)	P _D (W)	Configuration
		10V	4.5V	2.5V	1.8V				
TO-247/TO-3P/PWR-247 N-Channel (continued)									
FQA19N20	200	150				31	23	190	
IRFS240B		180				45	12.8	73	
IRFS240A		180				44	12.8	73	
IRFP240B		180				45	20	180	
IRFP240A		180				44	20	180	
IRFP240*		180				43	20	150	
FQA55N25	250	40				140	55	310	
FQAF40N25		70				85	24	108	
FQA40N25		70				85	40	280	
FQAF27N25		110				50	19	95	
FQA27N25		110				50	27	210	
IRFS254B		140				95	16	90	
IRFS254A		140				88	16	90	
IRFP254B		140				95	25	221	
IRFP254A		140				88	25	221	
FQAF16N25		230				27	12.4	85	
FQA16N25		230				27	18.5	190	
IRFS244B		280				47	10.2	73	
IRFS244A		280				46	10.2	73	
IRFP244B		280				47	16	180	
IRFP244A		280				46	16	180	
FQA44N30	300	69				120	43.5	310	
FQA38N30		85				90	38.4	290	
FQAF26N30		135				60	19	110	
FQA26N30		135				60	25.5	200	
FQAF22N30		160				47	16	100	
FQA22N30		160				47	22	190	
FQAF14N30		290				30	11.4	90	
FQA14N30		290				30	15	160	
FQA35N40	400	105				110	35	310	
FQA30N40		140				90	30	290	
SSF25N40A		200				140	14.3	100	
SSH25N40A		200				140	25	278	
FQAF20N40		220				60	14	110	
FQA20N40		220				60	19.5	200	
FQAF17N40		270				45	12.2	100	
FQA17N40		270				45	17.2	190	
IRFS350A		300				101	11.5	92	
IRFP350A		300				101	17	202	
FQAF11N40		480				27	8.8	90	
FQA11N40		480				27	11.8	160	
IRFS340B		540				41	8	85	
IRFP340B		540				41	11	162	
IRFS340A		550				58	8	85	
IRFP340A		550				58	11	162	
RF4E20N50S	500	85				79	20	180	
FQA28N50F		160				110	28.4	310	
FQA28N50		160				110	28.4	310	
FQA24N50F		200				90	24	290	
FQA24N50		200				90	24	290	
SSH22N50A		250				182	22	278	
IRFP460A*		270				56	20	280	
IRFP460*		270				120	20	250	
FQAF16N50		320				17	11.3	110	
FQA16N50		320				17	16	200	
IRFS450B		400				87	9.6	96	
IRFS450A		400				121	9.6	96	
IRFP450B		400				87	14	205	
IRFP450A		400				121	14	205	
IRFP450A*		400				33	14	190	
IRFP450*		400				82	14	180	
FQAF13N50		430				45	9.6	100	
FQA13N50		430				45	13.4	190	
FQAF9N50		730				28	7.2	90	
FQA9N50		730				28	9.6	160	

TO-247

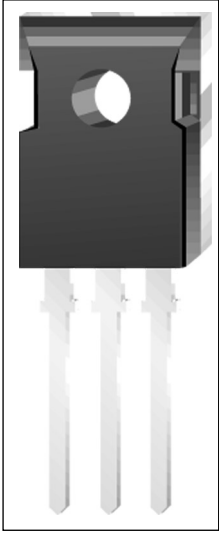


PWR-247

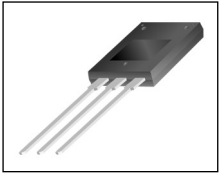


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TO-247



PWR-247

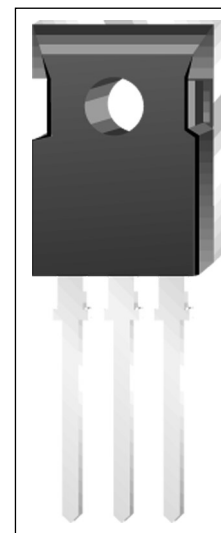


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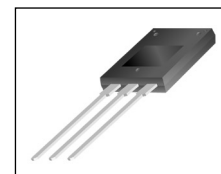
Part Number	V _{DS} (V)	R _{DS(ON)} Max. (mΩ) @ V _{GS} =				Q _g (nC) @	I _D	P _D	Configuration
		10V	4.5V	2.5V	1.8V	V _{GS} = 5V	(A)	(W)	
TO-247/TO-3P/PWR-247 N-Channel (continued)									
IRFS440B	500	850				41	6.2	85	
IRFS440A		850				57	6.2	85	
IRFP440B		850				41	8.5	162	
IRFP440A		850				57	8.5	160	
IRFP440*		850				42	8.8	150	
FQA24N60	600	240				110	23.5	310	
FQAF19N60		380				70	11.2	120	
FQA19N60		380				70	18.5	300	
SSF17N60A		450				128	9	100	
FQAF12N60		700				42	7.8	100	
FQA12N60		700				42	12	240	
SSF10N60B		800				54	6.9	90	
SSF10N60A		800				74	6.9	90	
SSH10N60B		800				54	10	193	
SSH10N60A		800				74	10	193	
FQAF7N60		1000				29	5.7	83	
FQA7N60		1000				29	7.7	152	
SSF7N60B		1200				38	5.4	86	
SSF7N60A		1200				49	5.4	85	
SSH7N60B		1200				38	7.3	160	
SSH7N60A		1200				49	7.3	160	
FQAF15N70	700	560				70	9.5	120	
FQA15N70		560				70	15	300	
FQAF6N70		1500				30	4.7	83	
FQA6N70		1500				30	6.4	152	
SSF6N70A	800	1800				51	5	85	
SSH6N70A		1800				51	6	140	
FQAF13N80		750				68	8	120	
FQA13N80		750				68	12.6	300	
SSF10N80A		950				125	6.5	100	
SSH10N80A		950				125	10	280	
FQAF10N80		1050				55	6.7	113	
FQA10N80		1050				55	9.8	240	
FQAF8N80		1200				44	5.9	107	
FQA8N80		1200				44	8.4	220	
SSF9N80A		1300				93	6	95	
SSH9N80A		1300				93	9	240	
FQAF7N80		1500				40	5	96	
SSF8N80A		1500				93	5.5	95	
FQA7N80		1500				40	7.2	198	
SSH8N80A		1500				93	8	240	
SSH7N80A	1800				67	7	200		
FQAF6N80	900	1950				31	4.4	90	
FQA6N80		1950				31	6.3	185	
SSH6N80AS		2000				67	6	200	
FQAF11N90		960				72	7.2	120	
FQA11N90		960				72	11.4	300	
SSF10N90A		1200				127	6.5	100	
SSH10N90A		1200				127	10	280	
FQAF9N90		1300				55	5.9	113	
FQA9N90		1300				55	8.6	240	
SSH9N90A		1400				127	9	280	
FQAF7N90		1550				45	5.2	107	
FQA7N90		1550				45	7.4	220	
SSF8N90A		1600				94	5.5	95	
SSH8N90A		1600				94	8	240	
SSF7N90A		1800				94	5	95	
SSH7N90A		1800				94	7	240	
FQAF6N90	900	1900				40	4.5	96	
FQA6N90		1900				40	6.4	198	
FQAF5N90		2300				31	4.1	90	
FQA5N90		2300				31	5.8	185	
SSH6N90A		2300				68	6	200	
SSH5N90A		2900				54	5	160	

Part Number	V _{DS} (V)	R _{DS(ON)} Max. (mΩ) @ V _{GS} =				Q _g (nC) @ V _{GS} = 5V	I _D (A)	P _D (W)	Configuration
		10V	4.5V	2.5V	1.8V				
TO-247/TO-3P/PWR-247 P-Channel									
FQAF47P06	-60	26				84	38	100	
FQA47P06		26				84	55	214	
FQAF22P10	-100	125				40	16.6	70	
FQA22P10		125				40	24	150	
IRFP9150*		150				82	25	150	
FQAF17P10		190				30	12.4	56	
FQA17P10		190				30	18	120	
SFF9140		200				43	13	80	
SFH9140		200				43	19	166	
IRFP9140*		200				37	19	125	
SFH9154	-150	200				100	18	204	
FQAF12P20	-200	470				31	11.5	70	
FQA12P20		470				31	12.6	150	
SFF9240		500				46	7.6	60	
SFH9240		500				46	11	126	
IRFP9240*		500				38	12	150	
FQAF9P25	-250	620				29	7.1	70	
FQA9P25		620				29	10.5	150	
SFF9244		800				45	6	60	
SFH9244		800				45	8.7	126	

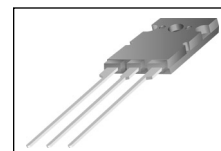
TO-247



PWR-247



TO-264



TO-264 N-Channel									
FQL50N40	400	75				160	50	460	
FQL40N50F	500	110				155	40	460	
FQL40N50		110				155	40	460	

*These Industry Standard IRF devices can be specified by adding the suffix R494x to the part number when ordering. Example: IRF840AR4944. The suffix will not appear in the brand.

Power MOSFET Special Functions

Integrated Load Switches

Part Number	V _{IN} (Max)	R _{DS(ON)} Max. (mΩ) @ V _{IN} =				I _L (A) @ V _(DROP) = 0.2V		
		12V	5V	2.5V	1.8V	V _{IN} = 12V	V _{IN} = 5V	V _{IN} = 2.5V
SuperSOT-8								
FDR8321L	8		7	10.5			2.9	2.0
FDR8521L	20	7	11.5			2.9	1.8	

SuperSOT-6								
FDC6331L	8		5.5	7			2.8	2.5
FDC6329L			7	10.5			2.8	1.9
FDC6325L			13	18			1.5	1.0
FDC6323L			20	30			1.0	0.67
FDC6330L	20	8	12.5			2.5	1.6	
FDC6326L		12.5	20			1.5	1.0	
FDC6324L		20	30			1.0	0.67	
SI3861DV	25		55	70				

SC70-6								
FDG6323L	8		55	75			0.36	0.27
FDG6324L	20	55	75			0.36	0.27	

Part Number	V _{DS} (V)	R _{DS(ON)} Max. (mΩ) @ V _{GS} =				Q _g (nC) @ V _{GS} = 5V	I _D (A)	P _D (W)	Configuration
		10V	4.5V	2.5V	1.8V				
SC70-6 N-Channel									
FDG6331L	-25		260	330	450		0.9	0.3	Dual

MOSFET & Schottky Combos

MOSFET						Schottky Diode		P _D (W)
Part Number	V _{DS} (V)	I _D (A)	R _{DS(ON)} Max. (mΩ) @ V _{GS} =		Q _g (nC) @ V _{GS} = 5V	V _F (V)	@ I _F (A)	
			10V	4.5V				
SO-8 N-Channel								
FDFS6N303	30	6	4	6	6	0.42	3	2.5
P-Channel								
FDFS2P102	-20	3.3	12.5	20	3.5	0.58	2	2
FDFS2P102A		3.3	12.5	20	2.1	0.58	2	2
FDFS2P106A	-60	3	11	14	15	0.58	2	2

TSSOP-8 P-Channel								
FDW6923	-20	3.5	5	9	10	0.5	2	2

NOTES

NOTES

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EXHIBIT 2



AN1703 APPLICATION NOTE

GUIDELINES FOR USING ST'S MOSFET SMD PACKAGES

R.Gulino

1. ABSTRACT

The trend from through-hole packages to low-cost SMD-applications is marked by the improvement of chip technologies. "Silicon instead of heatsink" is therefore possible in many cases. Many applications today use PCBs assembled with SMD-technologies, the emphasis being on Power ICs in SMD packages mounted on single-sided PCBs laminated on one side.

The printed circuit board (PCB) itself becomes the heatsink. In early fabrications a solid heatsink was either screwed or clamped to the power package. It was easy to calculate the thermal resistance from the geometry of the heatsink.

In SMD-technology, this calculation is much more difficult because the heat path must be evaluated: chip (junction) - lead frame - case or pin - footprint - PCB materials (basic material, thickness of the laminate) - PCB volume - surroundings.

As the layout of the PCB is a main contributor to the result, a new technique must be applied. Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package.

The power dissipation for a SMD device is a function of the drain pad size, which can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. The measurements achieved on SMD packages for different drain pad size show that by increasing the area of the drain pad the power dissipation can be increased.

Although one can achieve improvements in power dissipation with this method, the tradeoff is to use valuable board area.

Next we consider the common ST MOSFET SMD packages (D²PAK, DPAK, SOT-223, SO-8, PowerSO-8™, PowerFLAT™ (5x5) and (6x5), TSSOP8 and PowerSO-10™) with their recommended footprints. For each of these packages we will show the power dissipation for the minimum footprint and for a large drain pad area (1in² or 600mm²) using the max measured $R_{THJ-PCB}$.

We will show the maximum allowable power dissipation versus drain pad area for different T_J-T_A values as well.

Finally we will make a thermal performance comparison for all SMD packages analysed.

Information regarding the mechanical dimensions for each SMD package can be found on the related datasheets.

2. THERMAL MEASUREMENTS

The most practical method of optimizing thermal performance is to characterize the MOSFET on the PCB where it will be used. The basis of this method is to dissipate a known amount of power in the MOSFET, and to measure the amount of temperature rise this causes in the junction, given the data

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required to calculate the junction to PCB thermal resistance ($^{\circ}\text{C}/\text{W}$).

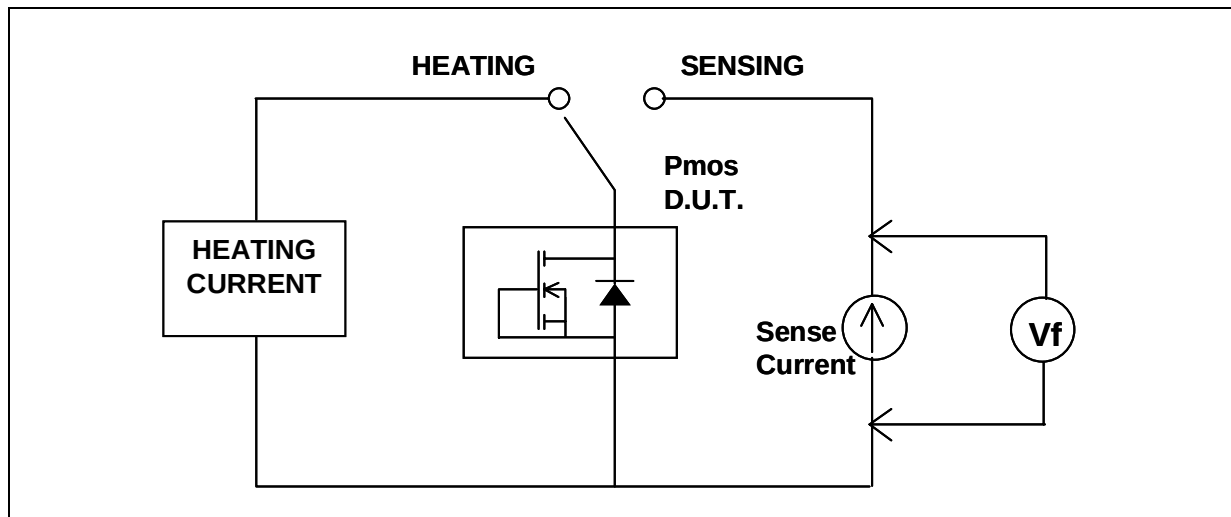
The procedure has two main steps. First is the characterization of the body diode. Second is the temperature rise measurements and calculation of the thermal resistance.

As an inherent part of the MOSFET structure, the body diode makes the ideal sensor to measure the junction temperature, since the forward voltage V_F varies with temperature, approximately $-2.2\text{mV}/^{\circ}\text{C}$. For this the diode's temperature coefficient is needed to get an accurate representation of the junction temperature. The forward voltage is measured with a low level current flowing through it to ensure there is no self heating, which would make the junction temperature measurement inaccurate.

The MOSFET being characterized is soldered on to the thermal test PCB and has the gate shorted to the source, to insure the MOSFET cannot turn on. The copper mounting pad reaches the remote connection points through fine traces that do not contribute significant thermal dissipation but serve the purpose of electrical connections.

Figure 1 illustrate the schematic of R_{TH} measurements where the MOSFET 's drain and source are connected with two power supplies.

Figure 1: Schematic of temperature measurements



The first power supply forces current through the body diode to heat the junction with a fixed power level, when the switch is in the "heating" position. The second power supply provides the sensing current for measuring the junction temperature, through the V_F measurement, when the switch is in the "sensing" position.

The measure of $R_{THJ-PCB}$ is based on the well know relationship between the power being dissipated in the devices and the relevant arising junction temperature:

$$R_{THJ-PCB} = \frac{\Delta T}{P_D} = \frac{T_J - T_C}{P_D}$$

This computation is made from pulsed operation to steady state in order to achieve the whole thermal transient response of the device under test. The applied power P_D is fixed by the equipment in terms of magnitude and time duration, so it is an input data.

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What we now have to compute is the T_J value since T_C is also an input data related to ambient or case temperature. To detect the arising junction temperature (T_J), we look at the variation of the forward drop of the drain-source diode, since this variation is proportional to the change in junction temperature.

3. D²PAK

The D²PAK is a surface mounting version of the standard TO-220 package, with the lead formed and the tab removed. It has been designed to achieve the high quality and reliability levels required by end users in the automotive industry.

Figure 2 shows D²PAK and its recommended footprint:

Figure 2: D²PAK and its recommended footprint (all dimensions are in mm)

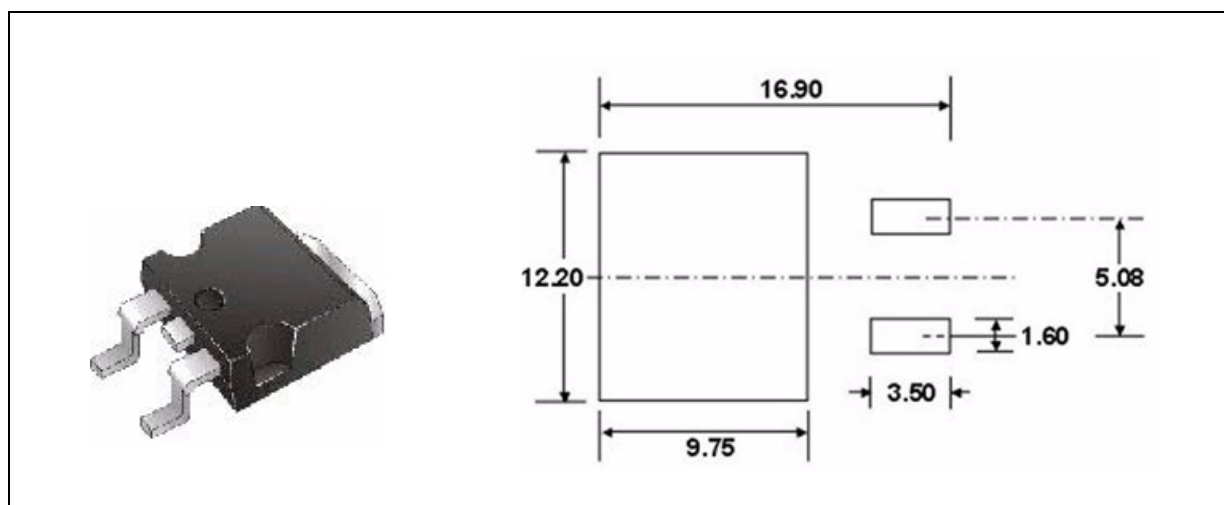
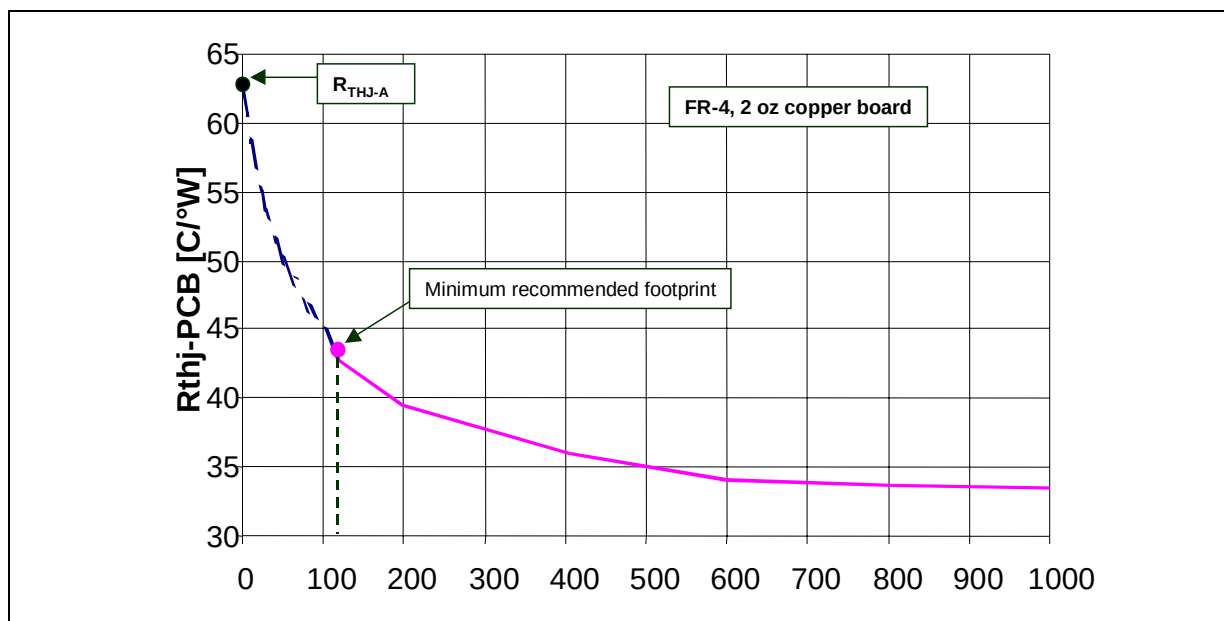


Figure 3 shows a graph of $R_{THJ-PCB}$ versus drain pad area from minimum recommended footprint to 10cm^2 :

Figure 3: $R_{THJ-PCB}$ versus drain pad area for D²PAK



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In free air we must consider the R_{THJ-A} , with a value of 62.5°C/W , like that of the TO-220.

For the minimum recommended footprint (120mm^2) the $R_{THJ-PCB}$ value is 42°C/W and the maximum allowable power dissipation turns out to be:

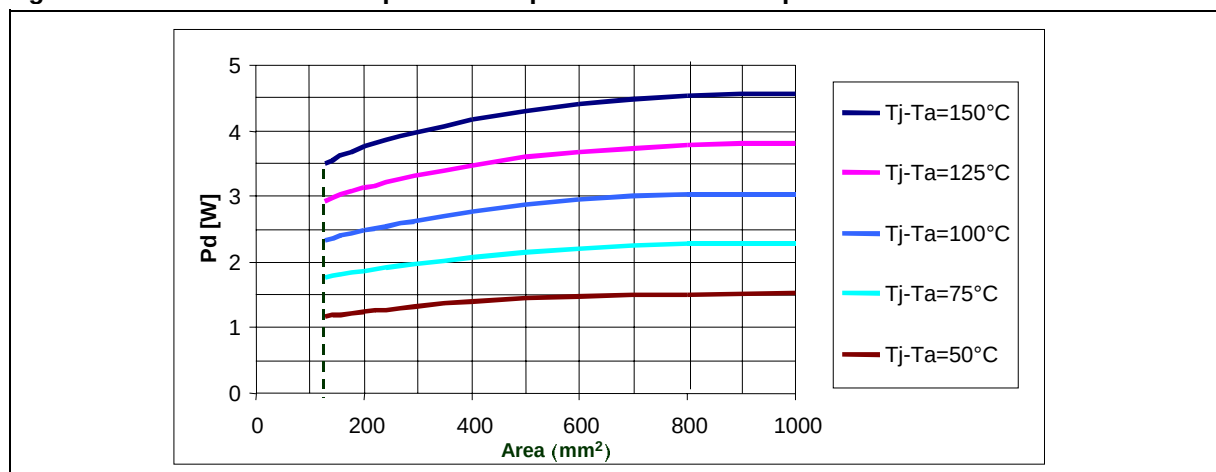
$$P_D = \frac{\Delta T}{R_{THJ-PCB}} = \frac{150}{42} = 3.5\text{W} \quad (T_{JMAX} = 175^{\circ}\text{C}, T_C = 25^{\circ}\text{C})$$

For a drain pad area of 1in^2 (about 600mm^2) we obtain:

$$R_{THJ-PCB} = 34^{\circ}\text{C/W} \Rightarrow P_D = \frac{\Delta T}{R_{THJ-PCB}} = 4.4\text{W}$$

The next figure shows the maximum allowable power dissipation versus drain pad area for different $T_J - T_A$ values:

Figure 4: Maximum allowable power dissipation versus drain pad area



4. DPAK

Similar considerations can be made for DPAK, where its minimum recommended footprint is shown in figure 5:

Figure 5: DPAK and its recommended footprint (all dimensions are in mm)

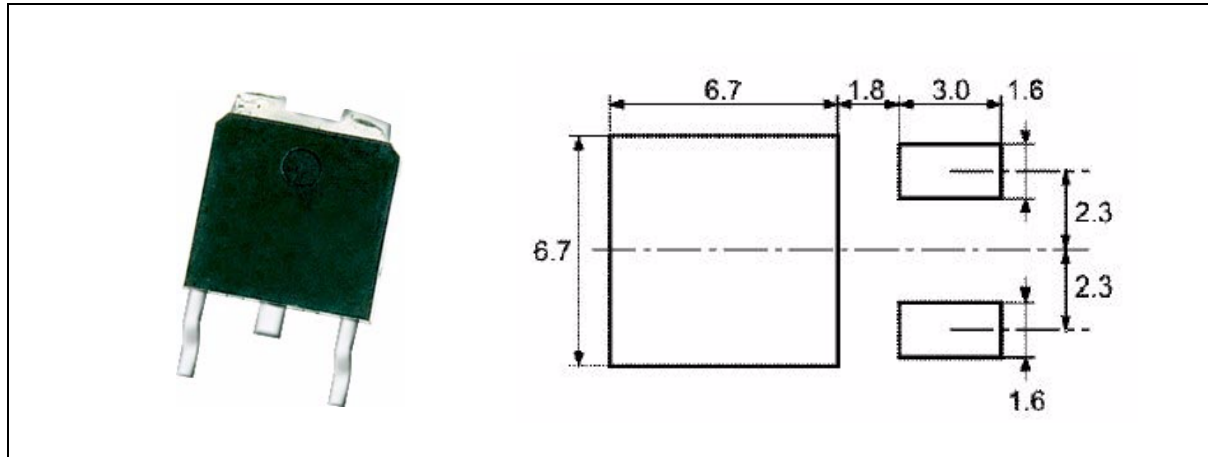
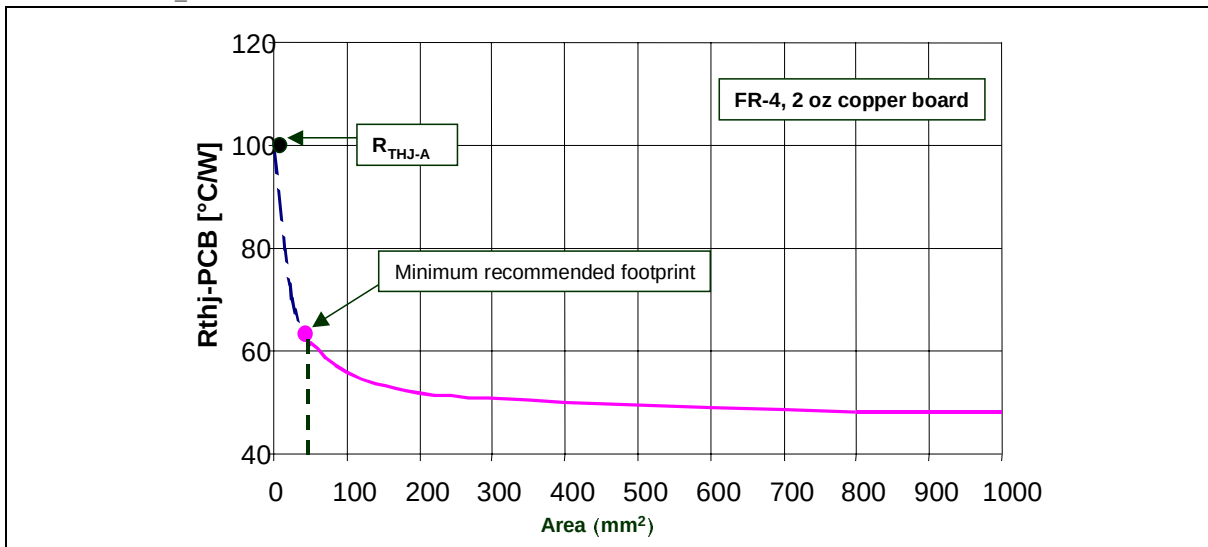


Figure 6 shows a graph of $R_{THJ-PCB}$ versus drain pad area from minimum recommended footprint to 10cm^2 :

Figure 6: R_{THJ_PCB} versus drain pad area for DPAK



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In free air we must consider the R_{THJ-A} and its value 100°C/W .

For the recommended footprint (45mm^2) the $R_{THJ-PCB}$ value is 62°C/W and the maximum allowable power dissipation is:

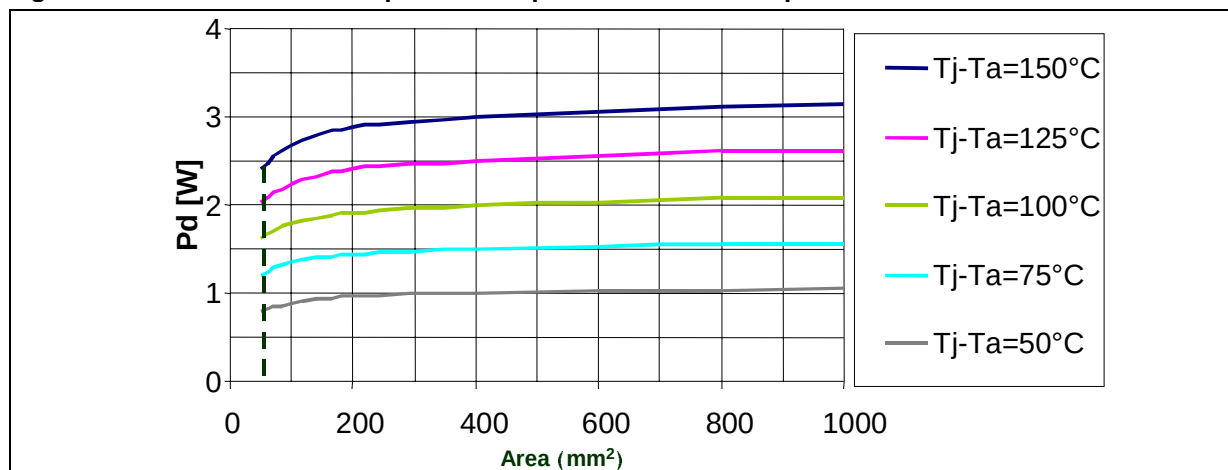
$$P_D = \frac{\Delta T}{R_{THJ-PCB}} = \frac{150}{62} = 2.4\text{W} \quad (T_{JMAX} = 175^{\circ}\text{C}, T_C = 25^{\circ}\text{C})$$

For a drain pad area of 1in^2 (about 600mm^2) we obtain:

$$R_{THJ-PCB} = 50^{\circ}\text{C/W} \Rightarrow P_D = \frac{\Delta T}{R_{THJ-PCB}} = 3\text{W}$$

The next figure shows the maximum allowable power dissipation as function of a PCB drain pad area for different T_J-T_A values:

Figure 7: Maximum allowable power dissipation versus drain pad area



5. SOT-223

The SOT-223 is a small package designed for surface mount applications. The formed leads absorb thermal stress during soldering, thereby eliminating the possibility of damage to the die. The encapsulation material used in this package enhances the device reliability which allows it to exhibit excellent performance in high temperature environments.

Figure 8: SOT-223 and its recommended footprint (all dimensions are in mm)

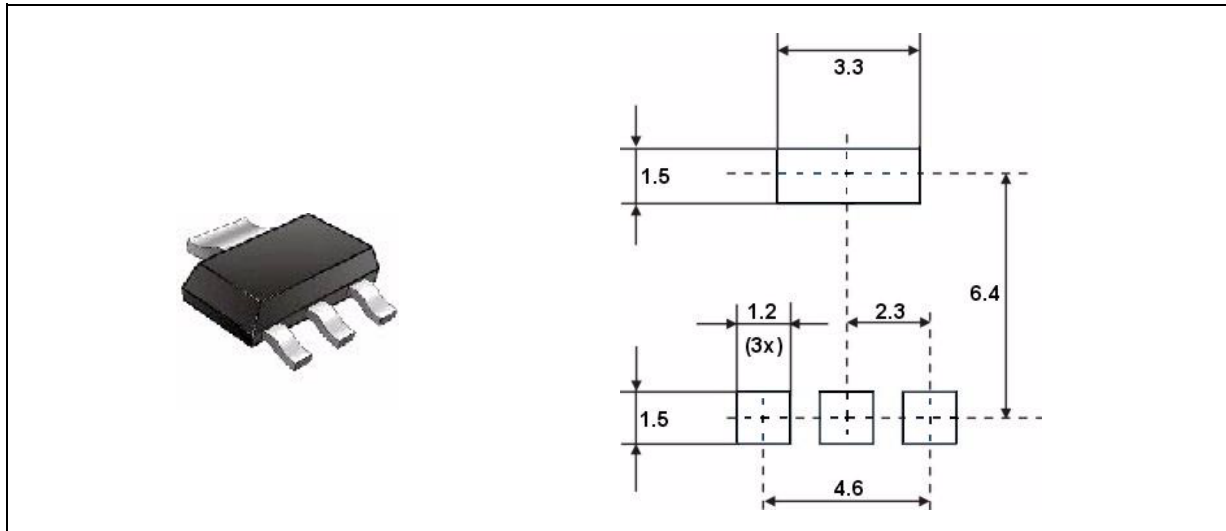
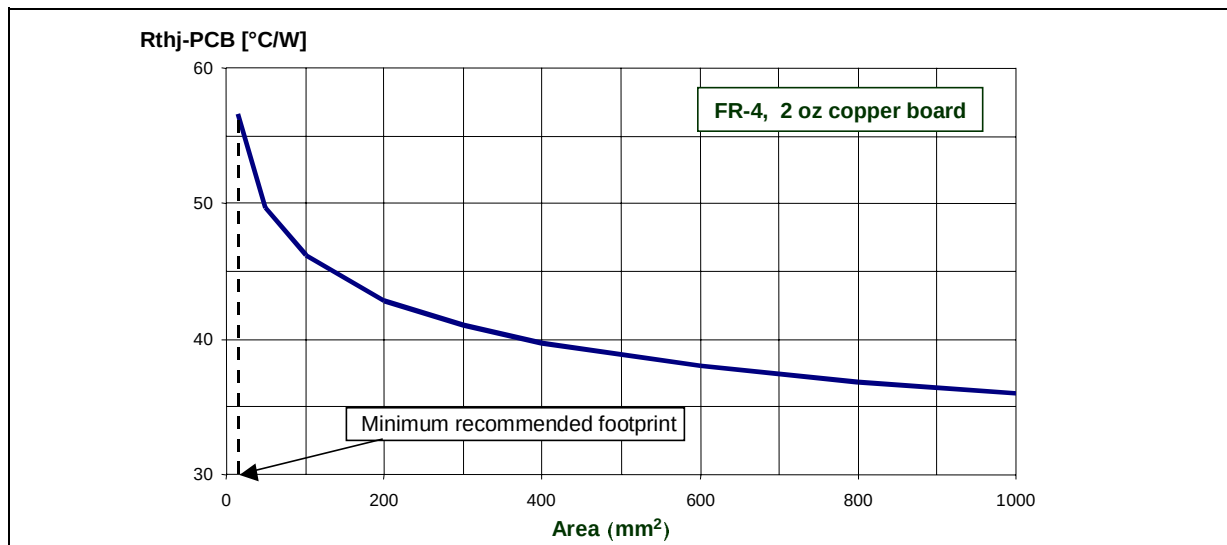


Figure 9 shows the measured values of $R_{THJ-PCB}$ versus drain pad area from minimum recommended footprint to 10cm^2 , for $t \leq 10\text{s}$ as power pulse:

Figure 9: $R_{THJ-PCB}$ versus drain pad area for SOT-223

Measurements performed for minimum recommended footprint (15mm^2) and $t \leq 10\text{s}$ give $R_{THJ-PCB} = 56.6^\circ\text{C/W}$ and the maximum allowable power dissipation results:

$$P_D = \frac{\Delta T}{R_{THJ-PCB}} = \frac{125}{56.6} = 2.2\text{W} \quad (T_{JMAX} = 150^\circ\text{C}, T_C = 25^\circ\text{C})$$

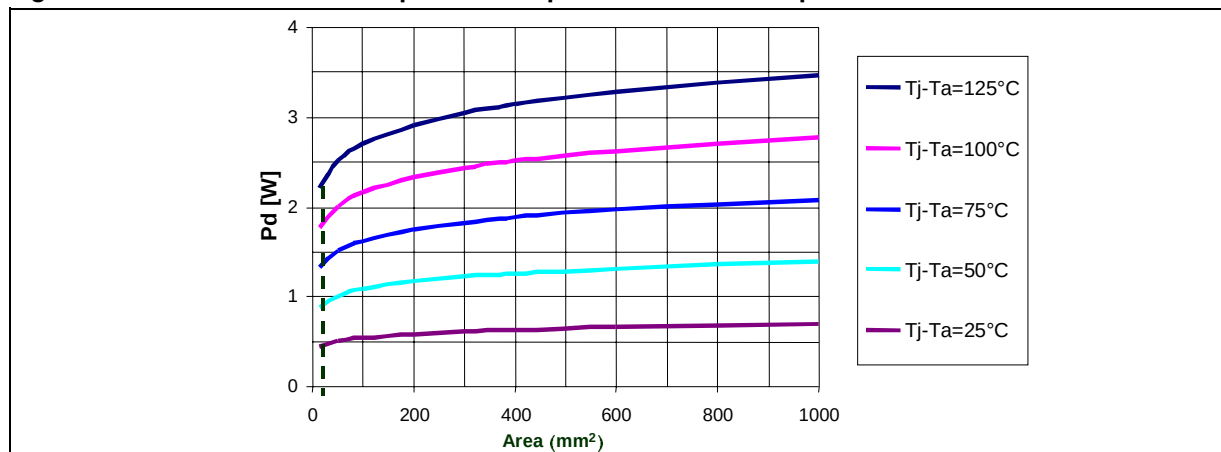
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For a drain pad area of 1in^2 (about 600mm^2) we obtain:

$$R_{THJ-PCB} = 38^\circ\text{C}/\text{W} \Rightarrow P_D = \frac{\Delta T}{R_{THJ-PCB}} = 3.3\text{W}$$

In the next figure the maximum allowable power dissipation as function of a PCB drain pad area for different T_J-T_A values is shown:

Figure 10: Maximum allowable power dissipation versus drain pad area



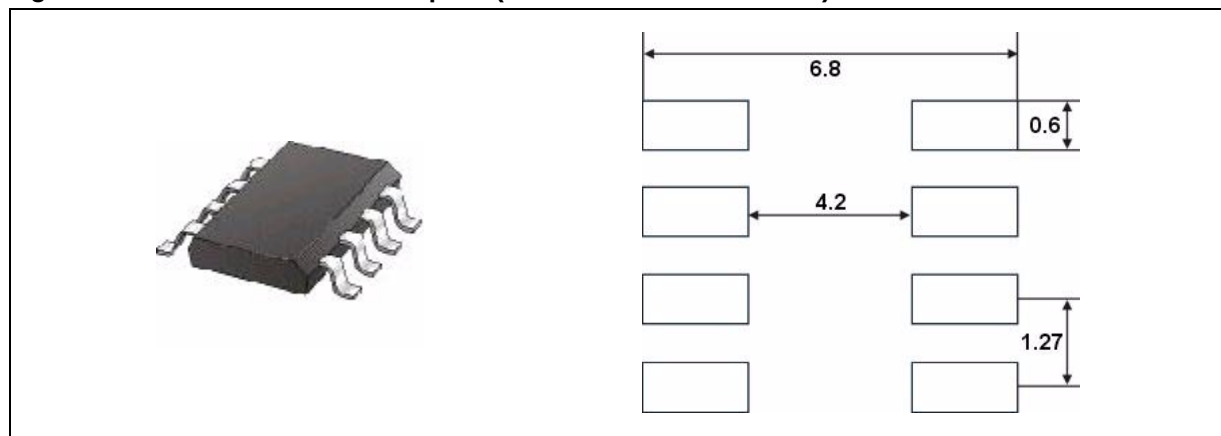
6. SO-8

The basis of the pad design for an SO-8 MOSFET is the package footprint. In converting the footprint to the pad set for a MOSFET, designers must make two connections: an electrical connection and a thermal connection, to draw heat away from the package.

For the SO-8 the thermal connections are very simple. Pins 5, 6, 7 and 8 are the drain of the MOSFET for a single MOSFET package and are connected together. In a dual package, pins 5 and 6 are one drain, and pins 7 and 8 are the other drain.

In figure 11 the basic SO-8 footprint is shown.

Figure 11: SO-8 and its basic footprint (all dimensions are in mm)

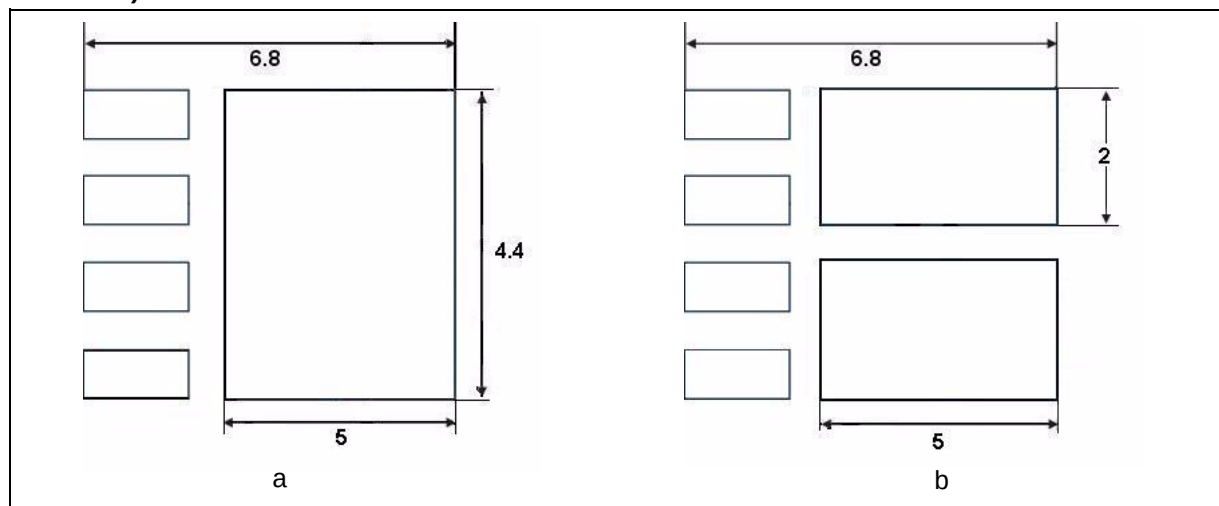


For a small-signal device or integrated circuit, typical connections would be made with traces that are 0.020 inches wide. Since the drain pins serve the additional function of providing the thermal connection to the package, this level of connection is inadequate.

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The minimum recommended pad patterns for the single MOSFET SO-8 (figure 12a) and dual MOSFET SO-8 (figure 12b) show the starting point for utilizing the board area available for the heat-spreading copper. To create this pattern, a plane of copper overlies the drain pins.

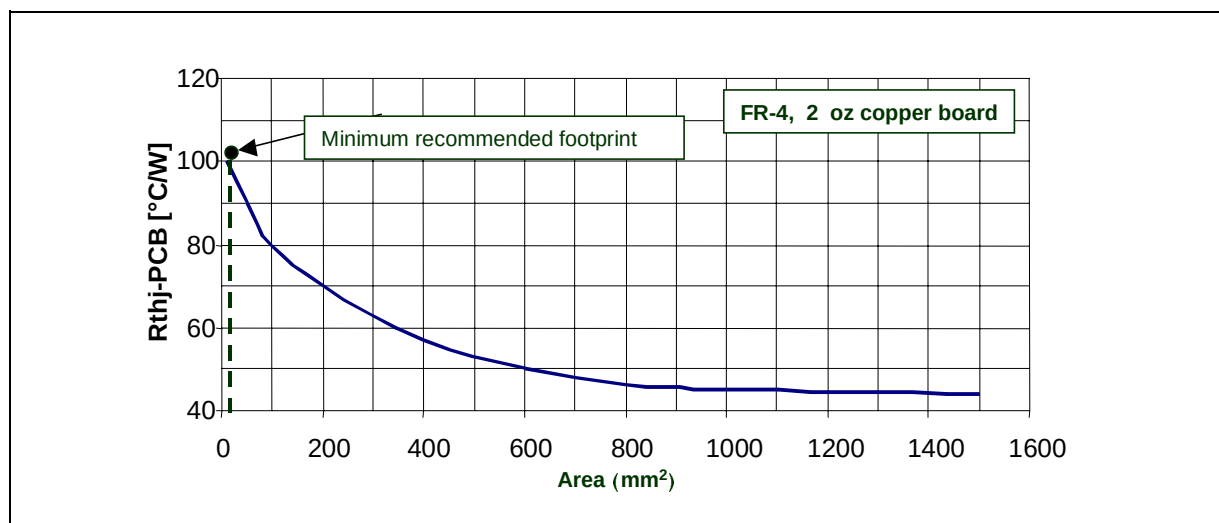
Figure 12: Single (a) & dual MOSFET (b) SO-8 minimum recommended pad pattern (all dimensions are in mm)



These connections provide planar copper to draw heat from the drain leads and start the process of spreading the heat so it can be dissipated into the PCB. These patterns use all the available area underneath the body for this purpose.

Figure 13 shows a graph of $R_{THJ-PCB}$ versus drain pad area from minimum recommended footprint to 15cm^2 , for $t \leq 10\text{s}$ as power pulse:

Figure 13: $R_{THJ-PCB}$ versus drain pad area for SO-8



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For the minimum recommended footprint (22mm² for a single MOSFET and 10mm² for a dual MOSFET) the thermal resistance value is about $R_{THJ-PCB} = 100^{\circ}\text{C}/\text{W}$ and the maximum allowable power dissipation results:

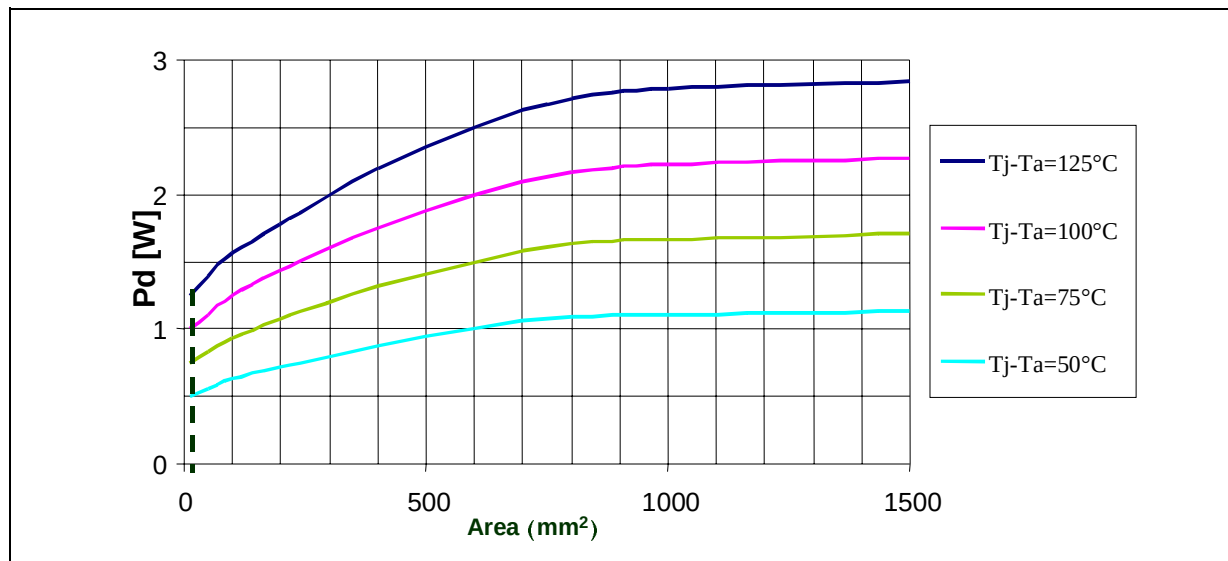
$$P_D = \frac{\Delta T}{R_{THJ-PCB}} = \frac{125}{100} = 1.25\text{W} \quad (T_{JMAX} = 150^{\circ}\text{C}, T_C = 25^{\circ}\text{C})$$

For a drain pad area of 1in² (about 600mm²) we obtain:

$$R_{THJ-PCB} = 50^{\circ}\text{C}/\text{W} \Rightarrow P_D = \frac{\Delta T}{R_{THJ-PCB}} = 2.5\text{W}$$

The next figure shows the maximum allowable power dissipation as function of a PCB drain pad area for different $T_J - T_A$ values.

Figure 14: Maximum allowable power dissipation versus drain pad area



7. PowerSO-8™

To enlarge our product range and, in the meantime, improve the performance of our MOSFETs housed in SMD packages, we are introducing new options to comply with the next generation of DC to DC converters for the computer and telecom areas. In such applications high output current and good thermal performances are required. This new package tailored to the above requirements is PowerSO-8. Furthermore, power devices housed in this package can be used for automotive applications such as body electronic applications (door looking, wipers, seat positioning systems and so on).

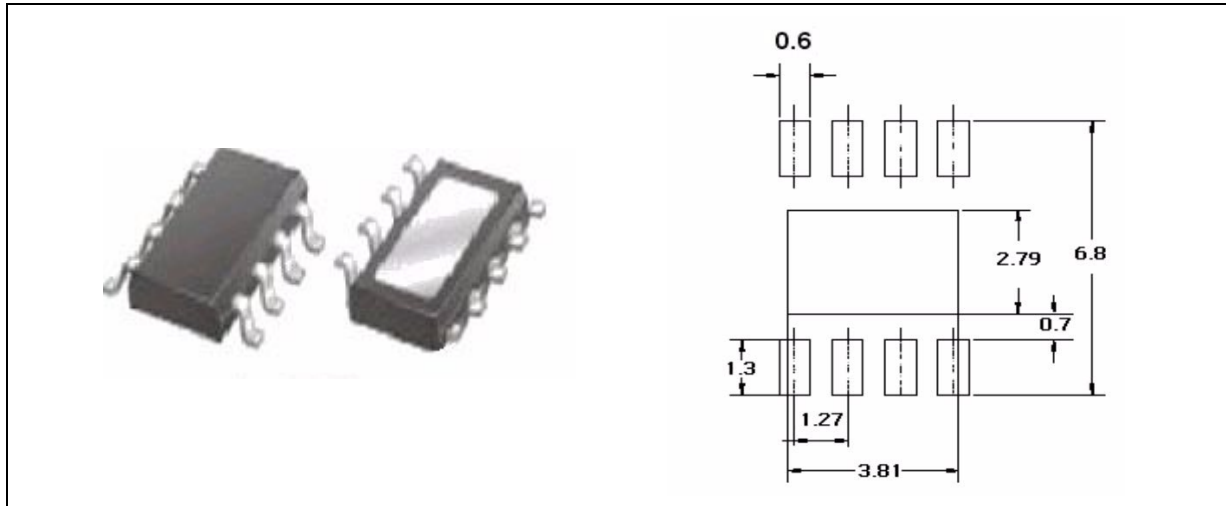
PowerSO-8 is the power version of the standard SO-8 package. It maintains the same footprint as SO-8, but it also has a solderable drain contact on the back. Given that heat is dissipated through the drain and source leads and also through the back of the package, the junction-case thermal resistance is

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drastically reduced and consequently the device is able to manage higher currents.

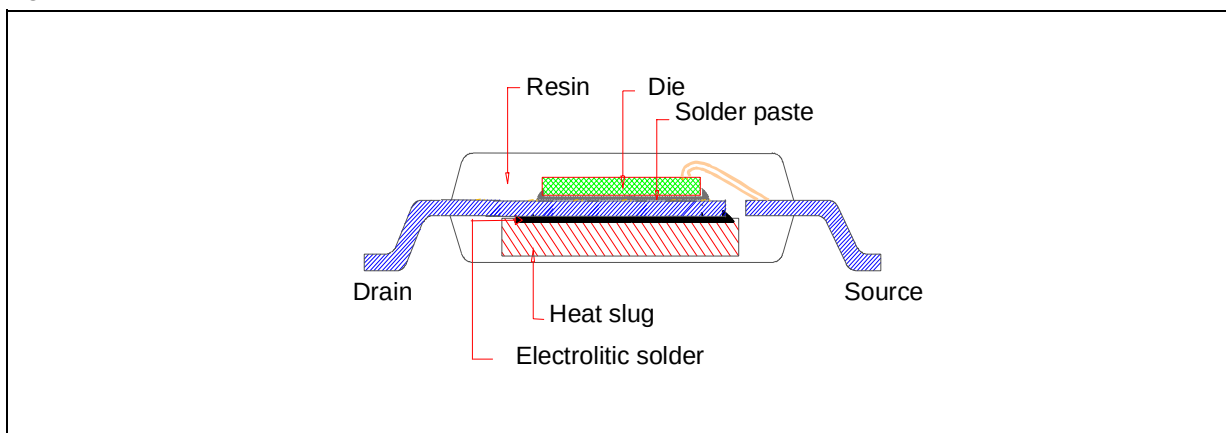
Figure 15 shows PowerSO-8 and its minimum recommended footprint.

Figure 15: PowerSO-8 with its minimum recommended footprint (all dimension are in mm)



Commonly pins 5 to 8 are the drain and are connected together to the exposed pad, so we have the same situation as figure 12a, while pin 4 is the gate and pins 1 to 3 are the source. Figure 16 shows the PowerSO-8 internal structure.

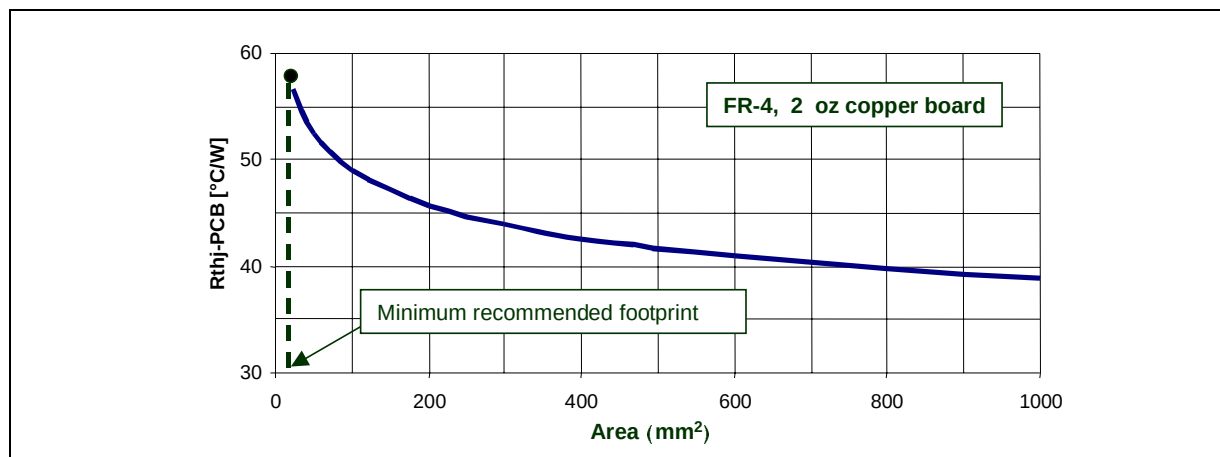
Figure 16: PowerSO-8™ internal structure



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Figure 17 shows a graph of $R_{THJ-PCB}$ versus drain pad area from minimum recommended footprint to 10cm^2 , for $t \leq 10\text{s}$ as power pulse:

Figure 17: $R_{THJ-PCB}$ versus drain pad area for PowerSO-8™



For the minimum recommended footprint (23mm^2) the thermal resistance value is about $R_{THJ-PCB} = 56.6$ $^{\circ}\text{C}/\text{W}$ and the maximum allowable power dissipation results:

$$P_D = \frac{\Delta T}{R_{THJ-PCB}} = \frac{125}{56.6} = 2.2\text{W} \quad (T_{JMAX} = 150^{\circ}\text{C}, T_C = 25^{\circ}\text{C})$$

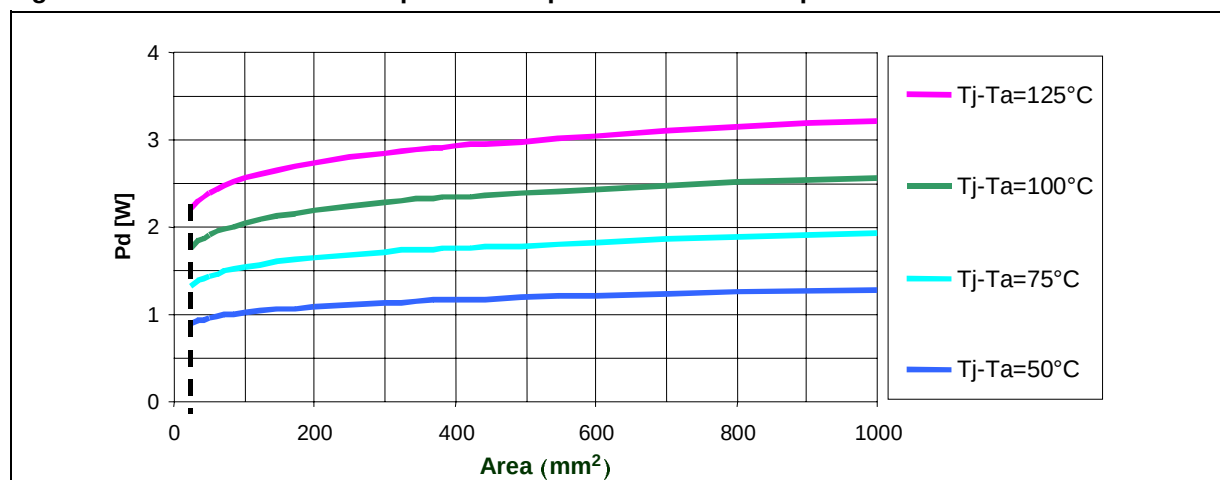
For a drain pad area of 1in^2 (about 600mm^2) we obtain:

$$R_{THJ-PCB} = 42^{\circ}\text{C}/\text{W} \Rightarrow P_D = \frac{\Delta T}{R_{THJ-PCB}} = 3\text{W}$$

that is 20% higher than that of the standard SO-8.

In the next figure the maximum allowable power dissipation as function of a PCB drain pad area for different $T_J - T_A$ values is shown:

Figure 18: Maximum allowable power dissipation versus drain pad area



8. PowerFLAT™ (5x5) and PowerFLAT™ (6x5)

PowerFLAT, in both (5x5) and (6x5) versions, depending on the package body size in (mm x mm), allows substantially bigger die capability with respect to the old-fashioned SO-8, still with reduced height and weight. This in turn translates into a remarkable board space reduction. Furthermore, the lower profile (1mm) allows higher operation frequency due to less inductance.

The leads are accommodated into the plastic body in such a way that a perfect co-planarity is assured. Also a better thermal impedance is achieved by means of the exposed pad that provides a thermal path from the die attached copper frame directly to the PCB.

The above features are exactly what designers demand in making their designs increasingly more efficient.

Not only is the PowerFLAT (5x5) smaller, but it also differs from PowerFLAT (6x5) in the way the pads are connected to the package. In fact, in PowerFLAT (5x5) the source terminals are on both sides while the drain coincides with the exposed back metal side only. The PowerFLAT (6x5) case is pin to pin compatible with a standard SO-8 package, it can house a larger die, and the exposed pad is connected to the drain as well.

Figure 19: PowerFLAT (5x5) and PowerFLAT (6x5)

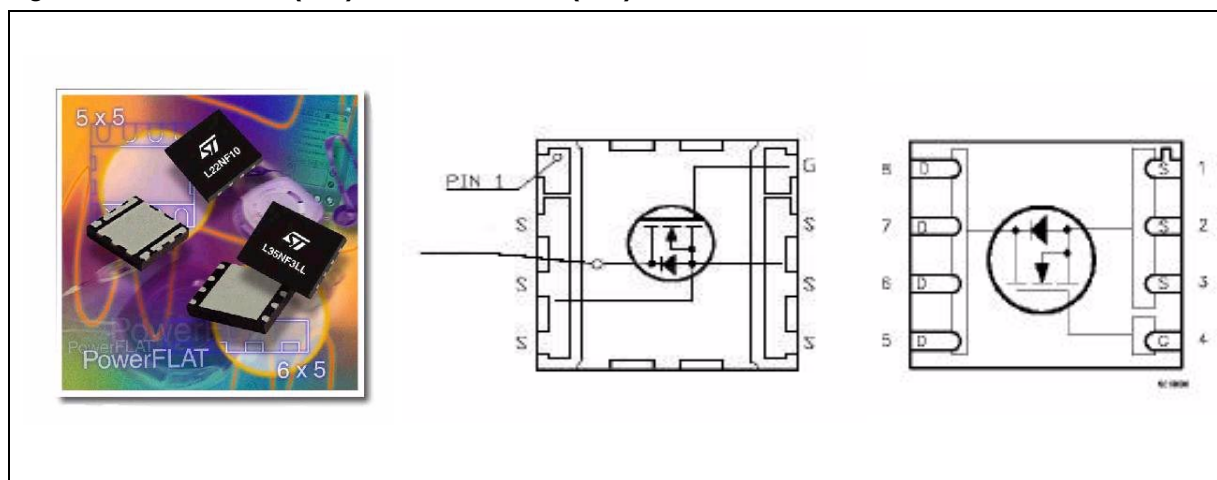
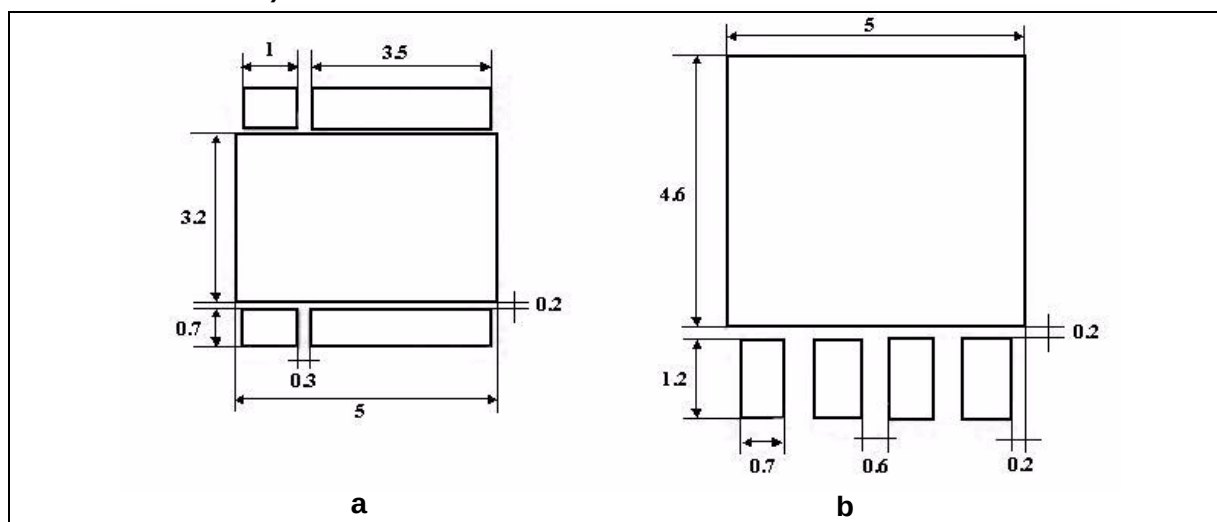


Figure 20 shows minimum recommended footprints for both types of PowerFLAT.

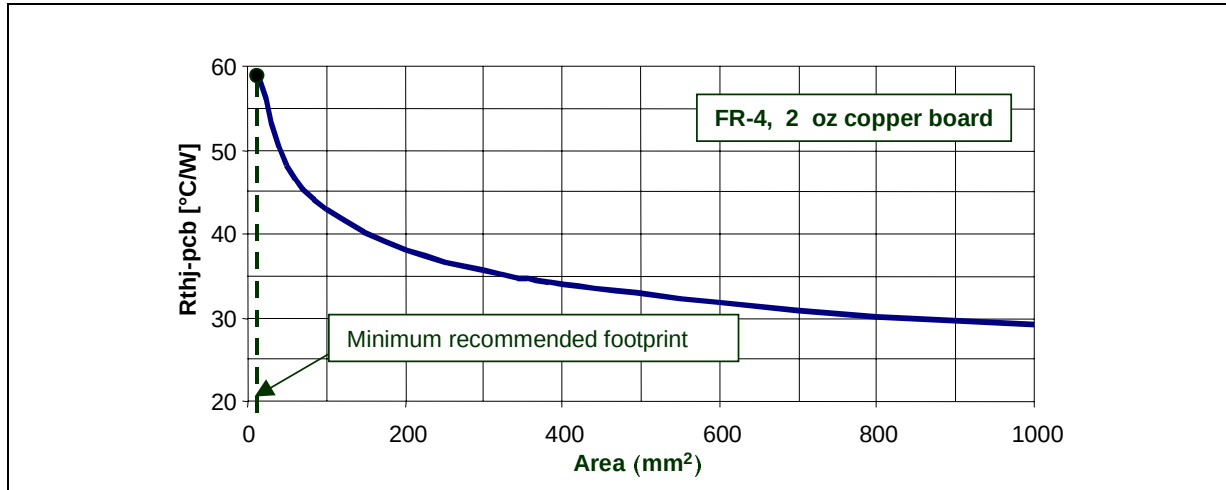
Figure 20: PowerFLAT (5x5) (a) and PowerFLAT (6x5) (b) minimum recommended footprints (all dimension are in mm)



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Figure 21 (obtained by measurements performed on PowerFLAT) shows the $R_{THJ-PCB}$ versus drain pad area from minimum recommended footprint to 10cm^2 , for $t \leq 10\text{s}$ as power pulse:

Figure 21: $R_{THJ-PCB}$ versus drain pad area for both types of PowerFLAT™



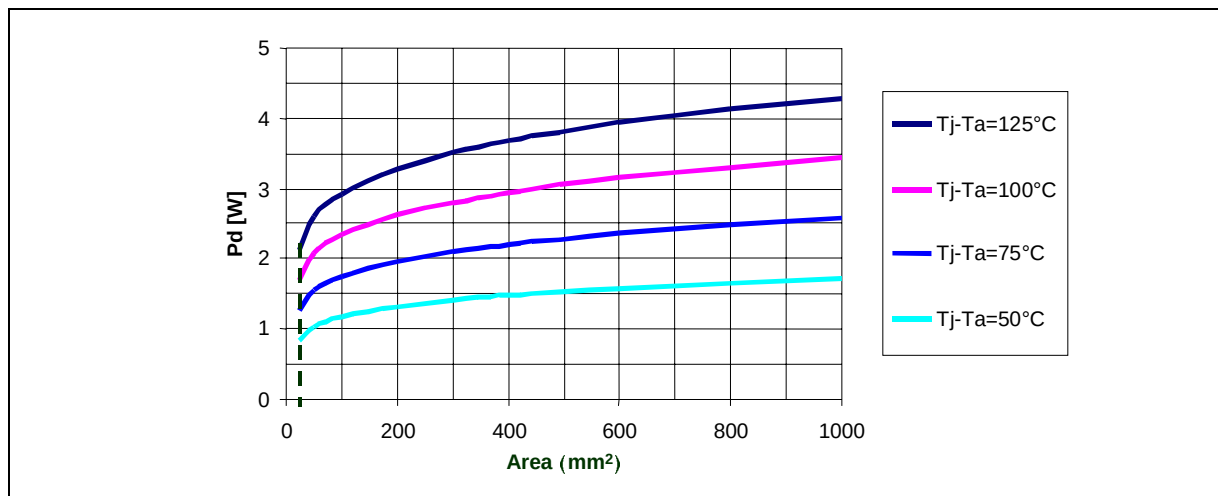
For the minimum recommended footprint the thermal resistance value is about $R_{THJ-PCB} = 60\text{ }^{\circ}\text{C/W}$ and the maximum allowable power dissipation results:

$$P_D = \frac{\Delta T}{R_{THJ-PCB}} = \frac{125}{60} = 2.1\text{W} \quad (T_{JMAX} = 150^{\circ}\text{C}, T_C = 25^{\circ}\text{C})$$

For a drain pad area of 1in^2 (about 600mm^2) we obtain:

$$R_{THJ-PCB} = 31.2^{\circ}\text{C/W} \Rightarrow P_D = \frac{\Delta T}{R_{THJ-PCB}} = 4\text{W}$$

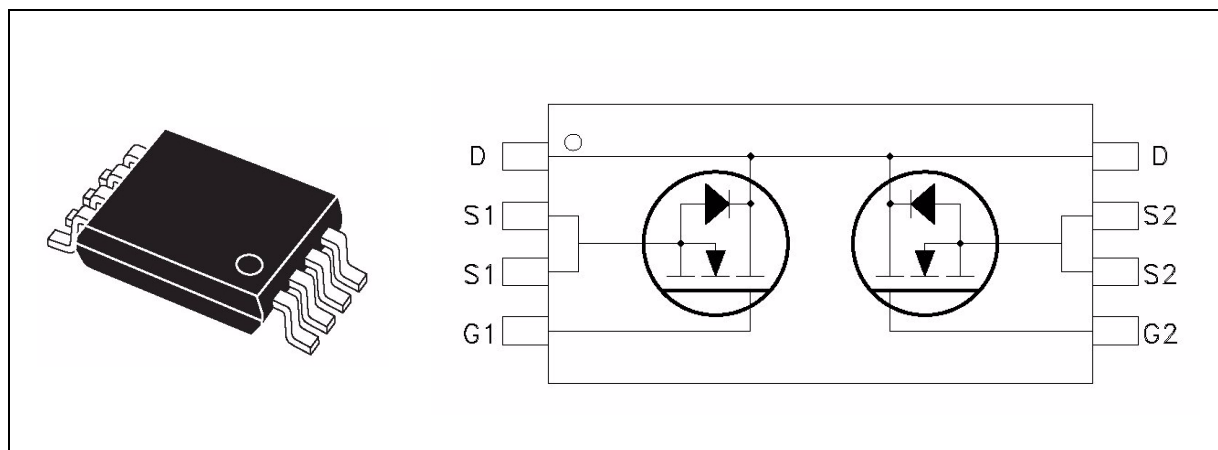
In the next figure the maximum allowable power dissipation as function of a PCB drain pad area for different $T_J - T_A$ values is shown:

Figure 22: Maximum allowable power dissipation versus drain pad area

9. TSSOP8

The new TSSOP8 power MOSFET package is the natural evolutionary response to the continuing demands of many markets for smaller packages. It has a smaller footprint and a lower profile than standard the SO-8 package, while maintaining low on-resistance and a good thermal performance. Furthermore TSSOP8 packages require approximately half the PCB area of a standard SO-8. It is available both in single die and/or in double die in common drain configuration.

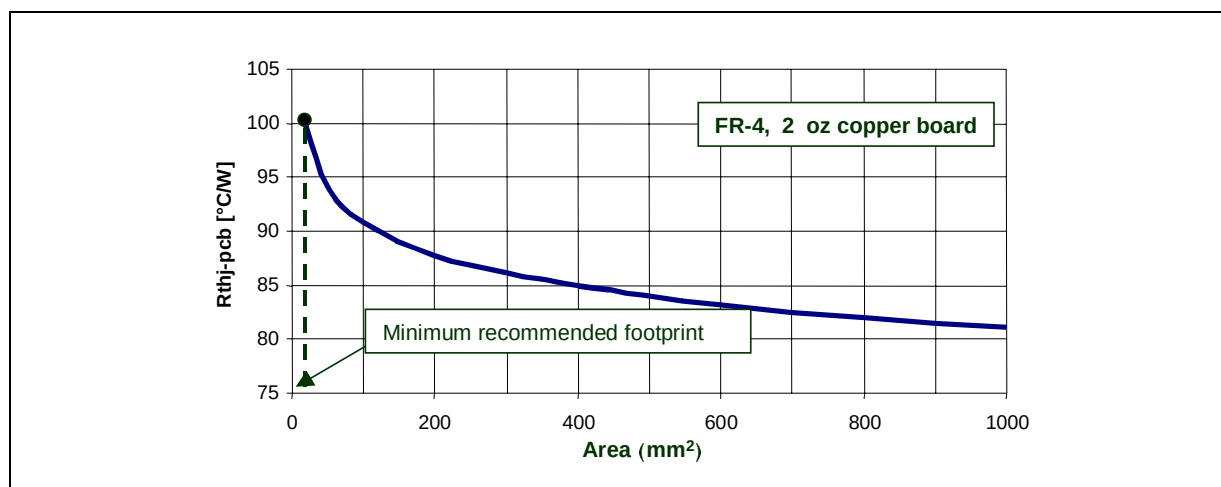
Figure 23 shows TSSOP8 and its internal schematic for dual configuration:

Figure 23: TSSOP8 package and its internal schematic

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Figure 24 shows the $R_{THJ-PCB}$ versus drain pad area from minimum recommended footprint to 10cm^2 , for $t \leq 10\text{s}$ as power pulse:

Figure 24: $R_{THJ-PCB}$ versus drain pad area for TSSOP8



For the minimum recommended footprint the thermal resistance value is about $R_{THJ-PCB} = 100\text{ °C/W}$ and the maximum allowable power dissipation results:

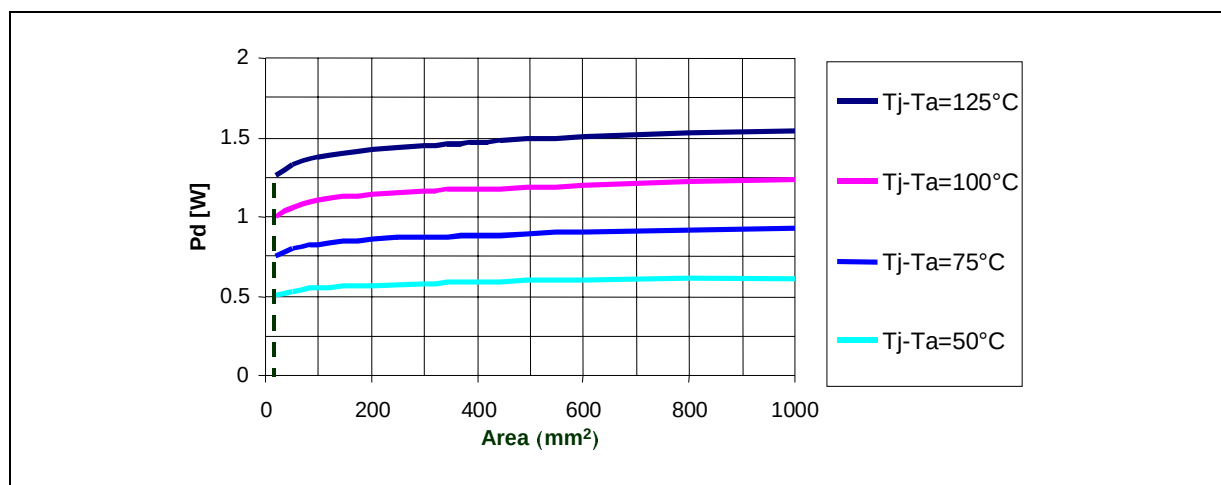
$$P_D = \frac{\Delta T}{R_{THj-PCB}} = \frac{125}{100} = 1.25\text{W} \quad (T_{JMAX} = 150^\circ\text{C}, T_C = 25^\circ\text{C})$$

For a drain pad area of 1in^2 (about 600mm^2) we obtain:

$$R_{THJ-PCB} = 83.5\text{ °C/W} \Rightarrow P_D = \frac{\Delta T}{R_{THJ-PCB}} = 1.5\text{W}$$

In the next figure the maximum allowable power dissipation as function of a PCB drain pad area for different T_J-T_A values is shown:

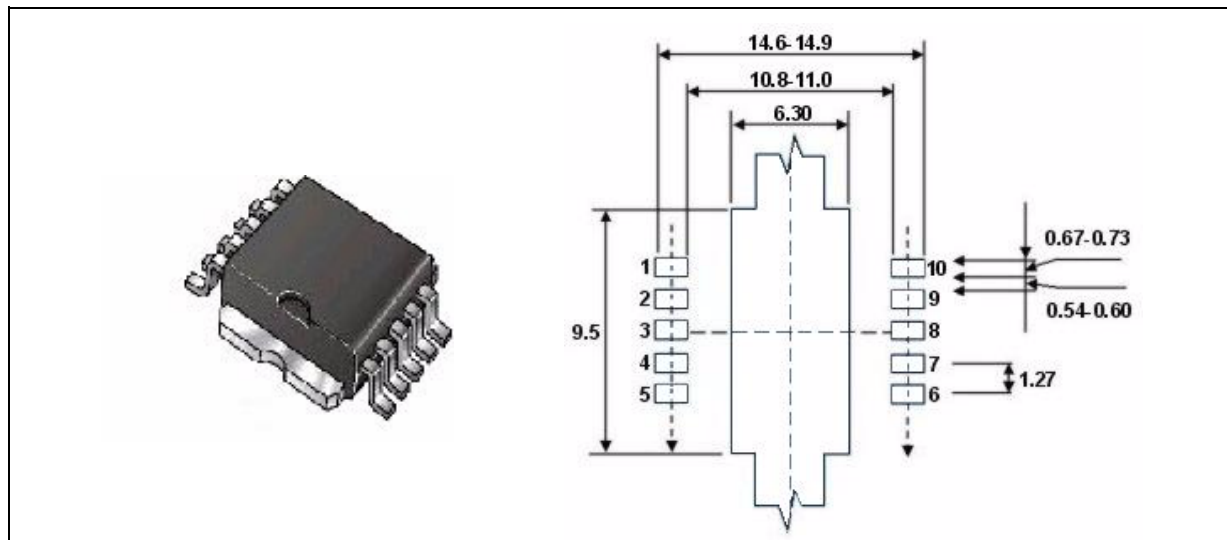
Figure 25: Maximum allowable power dissipation versus drain pad area



10. PowerSO-10™

Surface mounting packages, by their very nature are restricted to smaller footprints. Power devices need larger footprints to dissipate heat. PowerSO-10 is an optimized balance between these two conflicting requirements. Figure 26 shows PowerSO-10 with its minimum recommended footprint.

Figure 26: PowerSO-10™ package and its minimum recommended footprint (all dimensions are in mm)

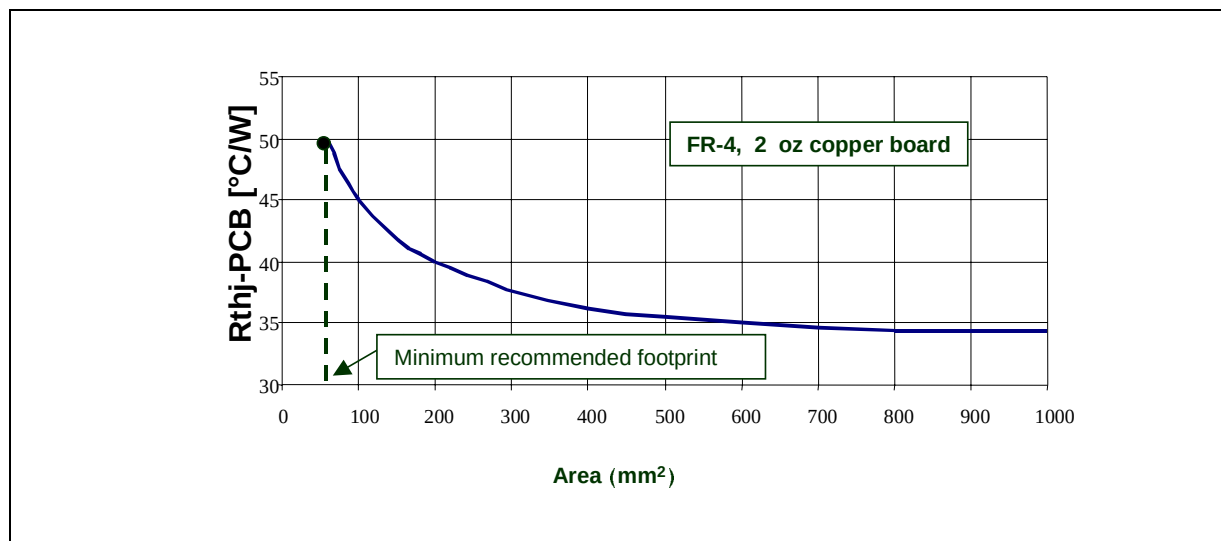


A 10-pin DIP package was manufactured also for use in intelligent power devices, which require many leads. Discrete can use high pin count packages to distribute the current through the power circuit.

The maximum die-size is the same as TO-220 and its derived versions, D²PAK and I²PAK. The lowering of the PowerSO-10 height results in about a 37% decrease in total volume of the package, while the spreader area remains large. Not only does this result in a lower package cost, but also from a high frequency standpoint, low height and less inductance are two big advantages.

The use of epoxy FR-4 boards is quite common in through-hole techniques; for surface mounting techniques, however, its poor thermal conduction means that it is not possible to benefit from the outstanding thermal performance of PowerSO-10. One way to improve the thermal conduction is the use of large heat spread areas at the copper layer of the PC board. This leads to a reduction of thermal resistance from 35-38°C/W for 3 to 6cm² on board heatsink (see figure 27).

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Figure 27: R_{THJ_PCB} versus drain pad area for PowerSO-10

For the recommended footprint (about 60mm²) the value is $R_{THJ-PCB} = 50^{\circ}\text{C/W}$ and the maximum allowable power dissipation results:

$$P_D = \frac{\Delta T}{R_{THJ-PCB}} = \frac{150}{50} = 3W \quad (T_{JMAX} = 175^{\circ}\text{C}, T_C = 25^{\circ}\text{C})$$

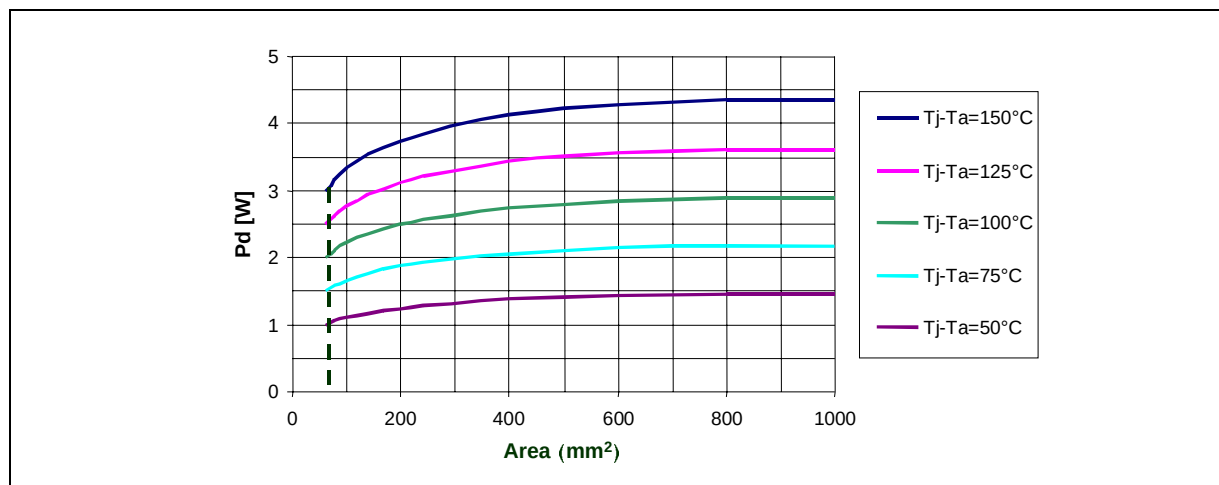
By increasing the area of the drain pad, the power dissipation can be increased. For a drain pad area of 1in² (about 600mm²) we obtain:

$$R_{THJ-PCB} = 35^{\circ}\text{C/W} \Rightarrow P_D = \frac{\Delta T}{R_{THJ-PCB}} = 4.3W$$

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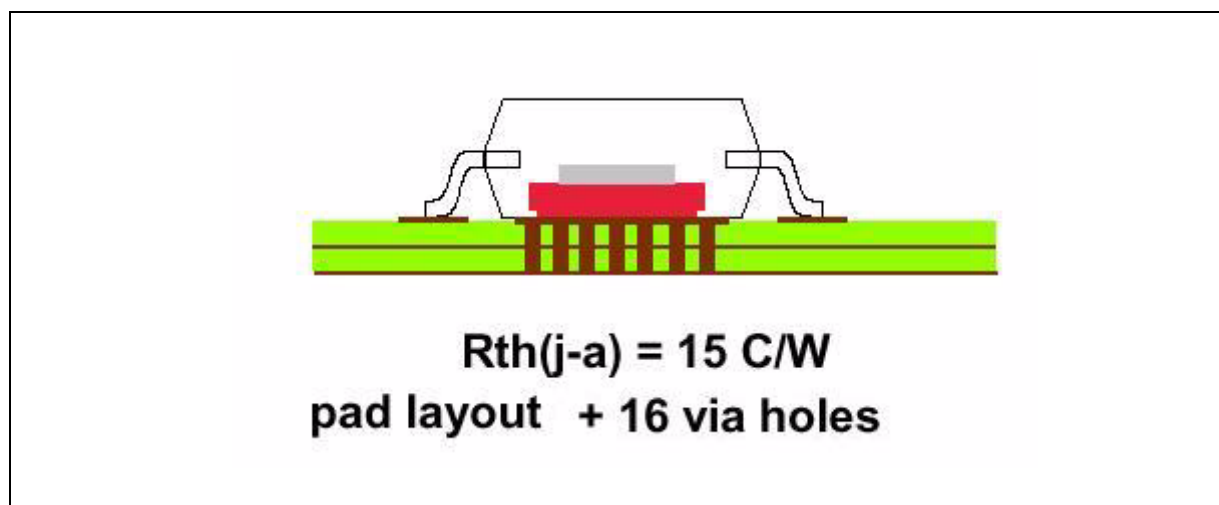
The next figure shows the maximum allowable power dissipation as function of a PCB drain pad area for different $T_J - T_A$ values.

Figure 28: Maximum allowable power dissipation versus drain pad area



Use of copper-filled through-holes with conventional FR-4 techniques increases the metallization and decreases thermal resistance accordingly. Using a configuration with 16 holes under the spreader of the package with a pitch of 1.8mm and a diameter of 0.7mm, the thermal resistance (junction - heats ink) can be reduced to 15 °C/W (see figure 29)

Figure 29: Mounting on FR-4 using copper-filled through holes for heat transfer



Apart from the thermal advantage, this solution allows the use of multi-layer boards. However, the limitations of this conventional material prevent its use in very high power, high current circuits.

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The thermal characteristics of PowerSO-10 are comparable with those of the D²PAK, as shown in the next table.

Table 1: Comparison between PowerSO-10™ and D2PAK

Comparison PowerSO-10 and TO-220 SMD-version

DESCRIPTION	TO-220 SMD-version	PowerSO-10	DELTA
Footprint Area in mm ²	203	141	-30%
Heat Spreader in mm ²	50 to 60	67	+10% to 30%
R _{th(j-c)} in °C/W	0.8	0.8	equal
Chip Size in mils ²	180x220	180x220	equal
Total Volume in mm ³	597	373	-37%
Package Height in mm	4.5	3.5	-22%

Steady-state thermal resistance (junction-case) studies show approximately 0.8°C/W for both PowerSO-10 and D²PAK, but PowerSO-10 exhibits 30% less footprint area than D²PAK. The test vehicle used is a MOSFET with a die-size of about 32,000 mils² (about 20.6mm²).

Furthermore, since PowerSO-10 has been designed solely to be an SMD, symmetry in the x- and y-planes gives the package excellent weight balance. Moreover, PowerSO-10 offers the unique opportunity to easily control the flatness and quality of the soldering process. Both the top and the bottom soldered edges of the package are accessible for visual inspection. PowerSO-10 is a package "designed for testability". Co-planarity between the substrate and the package can be easily verified.

11. SMD PACKAGES COMPARISON

Thermal performances for SMD packages are summarized in the following table:

Table 2: Thermal performances for SMD packages

Package	Package shaping area [mm ²]	Recommended Min. Footprint area [mm ²]	T _{JMAX} [°C]	R _{THJ-PCB} [°C/W] (*)	R _{THJ-PCB} [°C/W] (**)	P _D [W] (*)
D ² PAK	210	120	175	34.0	42.0	4.4
PowerSO-10	140	60	175	35.0	50.0	4.3
DPAK	80	45	175	50.0	62.0	3.0
PowerFLAT 5x5	25	15	150	31.2	60.0	4.0
PowerFLAT 6x5	30	23	150	31.2	60.0	4.0
SOT-223	50	15	150	38.0	56.6	3.3
PowerSO-8	30	23	150	42.0	56.6	3.0
SO-8	30	23	150	50.0	100	2.5
TSSOP8	20	15	150	83.5	100	1.5

(*) When mounted on 1 in² FR-4 board, 2 oz Cu, tp < 10s for small packages.

(**) When mounted on minimum recommended footprint.

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First of all we have to note that the maximum allowable power dissipation for the newest small packages (PowerFLAT and PowerSO-8) is quite similar to that for DPAK but require approximately half the PC board space. This advantage is more impressive if we note that the max die housed in PowerFLAT (6x5 version) is about 30% greater than those in DPAK. Also SOT-223 has a high thermal performance, but the max die housed is half that of those for DPAK and PowerSO-8.

Since several automotive applications require devices rated at 175 °C, up to now only the standard SMD packages (D²PAK, DPAK, PowerSO-10) are automotive graded. These packages have been designed to withstand the high stresses in under-hood applications.

12. SOLDERING PROFILE

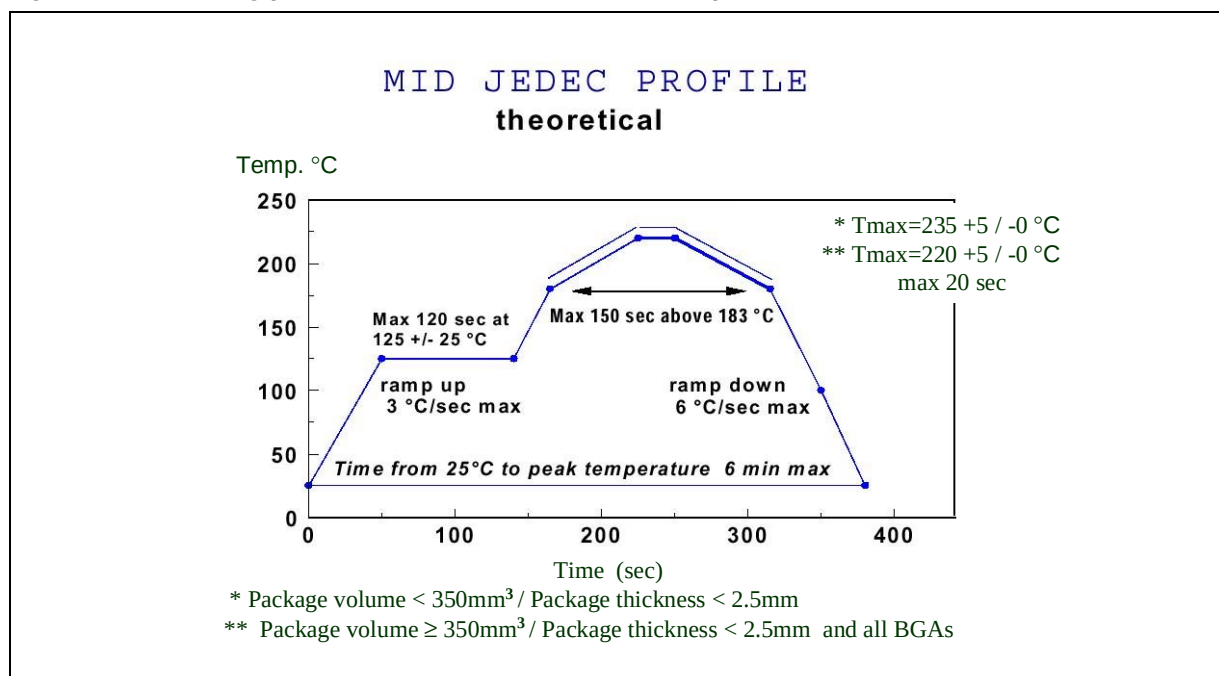
The most commonly used techniques for mounting SMD packages to the PCB are infrared and vapor phase reflow. These are preferred over wave soldering because this typically involves increased heating rate, higher temperatures and increased flux exposure.

The infrared reflow technique involves thermal energy supplied via lamps radiating at given wavelengths. Therefore, the amount of thermal energy absorbed varies with board size, component size, component orientation, and materials used. The surface temperature of the board is not uniform and the board edges tend to run 10°C to 20°C higher than the center.

The vapor phase reflow technique uses vapor from a boiling inert fluorocarbon liquid. The heat of condensation provides a thermal constraint dependent on the liquid selected. With essentially no temperature gradient across the surface of the board, component location design rules even for heating is not significant compared to infrared reflow.

The theoretical solder reflow temperature profile used, and the temperatures and time duration are shown in the next figure:

Figure 30: Soldering profile, recommended reflow oven profile



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Any solder temperature profile should be within these limits. The soldering process causes considerable thermal stress to a semiconductor component. This has to be minimized to ensure a reliable and extended lifetime of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, in order to minimize the thermal stress to which the devices are subject, the device should always be preheated (max 120sec at $125 \pm 25^{\circ}\text{C}$). Soldering a device without preheating can cause excessive thermal shock and stress that can result in damage to the device.

Voids pose a difficult reliability problem for large surface mount devices. Pockets of air under the package result in poor thermal contact and the resulting high thermal resistance leads to complete failure. Because of co-planarity problems, weight balance is critical.

The quality of the solder joints is very important for two reasons: firstly, poor quality solder joints result directly in poor reliability, and secondly, solder thickness significantly affects the thermal resistance. Thus a tight control of this parameter results in thermally efficient and reliable solder joints. Thermal conductivity in the region of 0.5°C/W can easily be lost through uneven solder and poor co-planarity of tabs and leads.

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APPENDIX A

Dean P. Neikirk

Emeritus Professor, Emeritus Cullen Trust for Higher Education Professorship in
Engineering
Department of Electrical and Computer Engineering
Cockrell School of Engineering
The University of Texas at Austin
Austin, TX 78712

Education:

Oklahoma State University (Physics and Mathematics; with Honors)	B.S.	1979
California Institute of Technology (Applied Physics)	M.S.	1981
California Institute of Technology (Applied Physics)	Ph.D.	1984

Professional Experience:

Assistant Professor, University of Texas at Austin, Jan. 1984 - Aug. 1988
Associate Professor, University of Texas at Austin, Sept. 1988- Aug. 1992
Full Professor, University of Texas at Austin, Sept. 1992-Jan. 2021
Associate Dean of Graduate Studies, Aug. 2014 – Jan. 2021
Emeritus Professor, Feb. 2021 - present

Honors and Awards:

- 1984 Marconi International Fellowship Young Scientist Award "for contributions to the development of millimeter wave integrated circuits especially in the areas of detectors and imaging arrays."
- Listed in the Second Edition of Who's Who in Frontiers of Science and Technology, 5th Edition of Who's Who in Technology Today, 1994 American Men & Women of Science; 1985 Outstanding Young Man of America, 1989 Outstanding Young Man of America; 7th Edition of Who's Who in Technology.
- 1984-85 Engineering Foundation Faculty Award, University of Texas at Austin Engineering Foundation Advisory Council.
- 1985-90 General Motors Foundation Centennial Teaching Fellowship, University of Texas at Austin.
- 1985-86 IBM Corporation Faculty Development Award
- 1986 National Science Foundation Presidential Young Investigator.

- 1987 Award for Outstanding Engineering Teaching by an Assistant Professor, College of Engineering, University of Texas at Austin.
- 1990-1992 Temple Foundation Endowed Faculty Fellowship (No. 1), University of Texas at Austin.
- 1992-present Cullen Trust for Higher Education Professorship in Engineering (No. 7), University of Texas.
- 1997 College of Engineering Award for Outstanding Teaching in the Department of Electrical and Computer Engineering, University of Texas at Austin.
- 2003 Department of Electrical and Computer Engineering Gordon T. Lepley IV Endowed Memorial Teaching Award, University of Texas at Austin.
- 2007 Lockheed Martin Aeronautics Company Award for Excellence in Engineering Teaching
 - each year since 1956, Lockheed Martin and its predecessor, has sponsored an award for excellence in engineering teaching to reward one College of Engineering faculty member for exceptional teaching. This prestigious award is given to a faculty member dedicating time and energy in abundance to teaching undergraduate and graduate students. As a result, his or her work leaves a mark of excellence on the entire College of Engineering. Nominations for this award are made by The University of Texas at Austin engineering students and faculty. Final selection is made by a committee composed the five most recent faculty recipients of the award and the student presidents of the Student Engineering Council (SEC) and the Graduate Engineering Council (GEC).
- 2015 Civitatis Award: The University of Texas at Austin Civitatis Award was established in 1997 to recognize outstanding faculty citizenship. The Civitatis Award is conferred upon a member of the faculty in recognition of dedicated and meritorious service to the University above and beyond the regular expectations of teaching, research, and writing. The award is made by the President upon the recommendation of the Faculty Council Executive Committee. Prof. Neikirk was nominated for the award for his “extensive, effective and distinguished service record to his department, college and [the] University of Texas.”

Vita for Dean P. Neikirk:

Dean P. Neikirk received the B.S. degree (1979) in physics from Oklahoma State University, and the M.S. (1981) and Ph.D. (1984) degrees in applied physics from the California Institute of Technology. He joined the faculty of The University of Texas at Austin in 1984, and is currently a Professor in the Department of Electrical and Computer Engineering, holding the Cullen Trust for Higher Education Professorship in Engineering (No. 7). Dr. Neikirk developed the first monolithic, high resolution focal plane detector array for use at wavelengths between 0.1 mm and 1 mm, and in 1984 received the Marconi International Fellowship Young Scientist Award "for contributions to the development of millimeter wave integrated circuits especially in the area of detectors and imaging arrays."

He has also been named a 1986 National Science Foundation Presidential Young Investigator.

Dr. Neikirk's research interests concentrated on the fabrication and modeling of electromagnetic and micromachined sensors and actuators. His work also included projects involving integrated circuit processing and the high frequency properties of transmission lines. His work concentrated on the use of advanced fabrication techniques, including silicon micromachining, for new device and sensor development. Dr. Neikirk developed the teaching laboratory for semiconductor device fabrication at The University of Texas at Austin, and was an active member of The University of Texas at Austin Microelectronics Research Center. Recently Dr. Neikirk's research project related to the development of new chemical sensors (an "electronic taste" sensor) was selected for a commercialization venture between the University of Texas and LabNow, Inc. Dr. Neikirk has also served as the Graduate Advisor of the Department of Electrical and Computer Engineering at UT-Austin, an Associate Chairman of the ECE Department, the Chair of the UT-Austin Graduate Assembly, the Chair of the UT-Austin Faculty Council, the Secretary of the General Faculty at UT-Austin, and as an Associate Dean of the University of Texas at Austin Graduate School.

Professional Societies:

Lifetime Senior Member, Institute of Electrical and Electronics Engineers
• Associate Editor for Solid State and VLSI Electronics, **IEEE Transactions on Education** (March 1991- Oct. 1994)

Commercialization of Technology:

Two companies have been founded based on technology developed by Dr. Neikirk's research group. In both cases the technology was developed at The University of Texas at Austin and licensed to start-ups.

From a University of Texas news release:

Firm commercializing University of Texas technology rounds up \$14 million venture capital investment (October 1, 2004)

AUSTIN, Texas—LabNow Inc. has received \$14 million in first-round venture investment for its point-of-care diagnostic system from the Soros Group, Austin Ventures and other investors.

The money will be used to develop the company's technology and to launch its initial product, CD4Now™, a point-of-care diagnostic tool for HIV/AIDS patients.

The device, which is based on technology developed at The University of Texas at Austin, quickly and accurately analyzes complex fluids such as blood.

Patents

1. US Patent 5,080,870: "Sublimating and Cracking Apparatus," Jan. 14, 1992; Inventors: B. G. Streetman, T. J. Mattord, D. P. Neikirk
2. US Patent 5,408,107: "Semiconductor Device Having Multiple Current-Voltage Curves and Zero-Bias Memory," April 18, 1995; Inventors: Dean P. Neikirk and Kiran Kumar Gullapalli
3. US Patent 6,589,779: "General signaling protocol for chemical receptors in immobilized matrices," July 8, 2003; Inventors: McDevitt; John T.; Anslyn; Eric V.; Shear; Jason B.; Neikirk; Dean P. Assignee: Board of Regents, The University of Texas System (Austin, TX)
4. US Patent 6,602,702: "Detection system based on an analyte reactive particle," August 5, 2003 Inventors: McDevitt; John T. (Austin, TX); Anslyn; Eric V. (Austin, TX); Shear; Jason B. (Austin, TX); Neikirk; Dean P. (Austin, TX)

Assignee: The University of Texas System (Austin, TX)

5. US Patent 6,649,403: "Method of preparing a sensor array," November 18, 2003
Inventors: McDevitt; John T. (Travis, TX); Anslyn; Eric V. (Austin, TX); Shear; Jason B. (Austin, TX); Neikirk; Dean P. (Travis, TX)
Assignee: Board of Regents, The University of Texas Systems (Austin, TX)
6. US Patent 6,680,206, "Sensor arrays for the measurement and identification of multiple analytes in solutions," January 20, 2004
Inventors: McDevitt; John T. (Travis, TX); Anslyn; Eric V. (Austin, TX); Shear; Jason B. (Austin, TX); Neikirk; Dean P. (Travis, TX)
Assignee: Board of Regents, The University of Texas Systems (Austin, TX)
7. US Patent 6,713,298, "Method and apparatus for the delivery of samples to a chemical sensor array," March 30, 2004
Inventors: McDevitt; John T. (Travis, TX); Anslyn; Eric V. (Travis, TX); Shear; Jason B. (Travis, TX); Neikirk; Dean P. (Travis, TX)
Assignee: Board of Regents, The University of Texas System (Austin, TX)
8. US Patent 6,908,770, "Fluid based analysis of multiple analytes by a sensor array," June 21, 2005
Inventors: McDevitt; John T. (Austin, TX); Anslyn; Eric V. (Austin, TX); Shear; Jason B. (Austin, TX); Neikirk; Dean P. (Austin, TX)
Assignee: Board of Regents, The University of Texas System (Austin, TX)
9. US Patent 7,022,517, "Method and apparatus for the delivery of samples to a chemical sensor array," April 4, 2006, filed: July 14, 2000
Inventors: McDevitt; John T. (Austin, TX); Anslyn; Eric V. (Austin, TX); Shear; Jason B. (Austin, TX); Neikirk; Dean P. (Austin, TX); Borich; Damon V. (Austin, TX)
Assignee: Board of Regents, The University of Texas System (Austin, TX)
10. US Patent 7,316,899, "Portable sensor array system," January 8, 2008, filed: January 31, 2001
Inventors: McDevitt; John T. (Austin, TX); Anslyn; Eric V. (Austin, TX); Shear; Jason B. (Austin, TX); Neikirk; Dean P. (Austin, TX)
Assignee: Board of Regents, The University of Texas System (Austin, TX)
11. US Patent 7,491,552, "Fluid based analysis of multiple analytes by a sensor array," February 17, 2009, filed: January 20, 2005
Inventors: McDevitt; John T. (Austin, TX); Anslyn; Eric V. (Austin, TX); Shear; Jason B. (Austin, TX); Neikirk; Dean P. (Austin, TX)
Assignee: Board of Regents, The University of Texas System (Austin, TX)
12. United States Patent 7,651,868, "Method and system for the analysis of saliva using a sensor array," January 26, 2010, Filed: December 13, 2004

Inventors: McDevitt; John T. (Austin, TX), Anslyn; Eric V. (Austin, TX), Shear; Jason B. (Austin, TX), Neikirk; Dean P. (Austin, TX), Christodoulides; Nick J. (Austin, TX)

Assignee: The Board of Regents of The University of Texas System (Austin, TX)

13. United States Patent 8,101,431, "Integration of fluids and reagents into self-contained cartridges containing sensor elements and reagent delivery systems," January 24, 2012, Filed: December 22, 2004

Inventors: McDevitt; John T. (Austin, TX), Ballard; Karri L. (Pflugerville, TX), Floriano; Pierre N. (Austin, TX), Christodoulides; Nick J. (Austin, TX), Neikirk; Dean (Austin, TX), Anslyn; Eric (Austin, TX), Shear; Jason (Austin, TX)

Assignee: Board of Regents, The University of Texas System (Austin, TX)

14. United States Patent 8,105,849, "Integration of fluids and reagents into self-contained cartridges containing sensor elements," January 31, 2012, Filed: December 22, 2004

Inventors: McDevitt; John T. (Austin, TX), Ballard; Karri L. (Pflugerville, TX), Floriano; Pierre N. (Austin, TX), Christodoulides; Nick J. (Austin, TX), Neikirk; Dean (Austin, TX), Anslyn; Eric (Austin, TX), Shear; Jason (Austin, TX)

Assignee: Board of Regents, The University of Texas System (Austin, TX)

15. United States Patent 8,257,967, "Method and system for the detection of cardiac risk factors," September 4, 2012, Filed: April 28, 2003

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16. United States Patent 9,291,586, "Passive wireless self-resonant sensor," March 22, 2016, Filing Date: May 5, 2013

Inventors: Neikirk, Dean P. (Austin, TX, US), Pasupathy, Praveenkumar (Austin, TX, US), Zhang, Sheng (Austin, TX, US), Leonhardt, Brad (Austin, TX, US), Ekerdt, John G. (Austin, TX, US), Korgel, Brian A. (Austin, TX, US), Holmberg, Vincent C. (Seattle, WA, US), Shipman, Catherine D. (Reston, TX, US), Bogart, Timothy D. (Oxford, GB), Chockla, Aaron (Chicago, IL, US)

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17. United States Patent 9,581,559, "Corrosion detection sensor embedded within a concrete structure with a diffusion layer placed over the sacrificial transducer," February 28, 2017, Filing Date: August 14, 2014

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15. T.R. Block, D. P. Neikirk, and B. G. Streetman, "MBE growth condition dependence of RHEED dampening and QW photoluminescence," Twelfth North American Conference on Molecular Beam Epitaxy, Ottawa, Canada, Oct. 12-14, 1992.
16. T.J. Mattord, D. P. Neikirk, A. Srinivasan, A. Tang, K. Sadra, Y.C. Shih, and B. G. Streetman, "Real time flux monitoring and feedback control of a valved arsenic source" Twelfth North American Conference on Molecular Beam Epitaxy, Ottawa, Canada, Oct. 12-14, 1992.
17. Y.C. Shih, D. P. Neikirk, and B. G. Streetman, "Effects of As flux on Si δ -doped GaAs," Twelfth North American Conference on Molecular Beam Epitaxy, Ottawa, Canada, Oct. 12-14, 1992.
18. Y. Kim and D. P. Neikirk, "Monolithically integrated optically interrogated pressure microsensor," **J. Acoust. Soc. Am.**, Vol. 92, No. 4 (pt. 2), October 1992, p. 2353.
19. O. Hartin, D. P. Neikirk, A. Anselm, and B. Streetman, "Memory Switching Simulation in Resonant Tunneling Devices," 1997 American Physical Society March Meeting, Kansas City, MO, March 17-21, Bulletin of the American Physical Society, Vol. 42, No. 1, 1997, p. 548.
20. O. Hartin and D. P. Neikirk, "Tight Binding Simulation of Memory Switching in Resonant Tunneling Devices," 1997 American Physical Society International Conference on Computational Physics, University of California, Santa Cruz, Aug. 25, 1997.

21. D. Neikirk, "Embedded Passive Sensors for State Monitoring," presented at NSF Workshop on Exploring the Uses of Autoadaptive Media in Geotechnical Earthquake Engineering, Austin, TX, January 10-12 2001.

22. Lavigne, John J.; Savoy, Steve; Best, Michael; Anslyn, Eric V.; Shear, Jason B.; McDevitt, John T.; Neikirk, Dean, "Toward the development of an 'electronic tongue'," Book of Abstracts, 219th ACS National Meeting, San Francisco, CA, March 26-30, 2000 (2000), AGFD-193.

23. Wood, Sharon; Neikirk, Dean, "Development of a passive sensor to detect cracks in welded steel construction," US-Japan Joint Workshop and Third Grantees Meeting, US-Japan Cooperative Research in Urban Earthquake Disaster Mitigation, Monbu-Kgagku-sho and The National Science Foundation, Seattle, August 15-16, 2001.

24. McCleskey, Shawn C.; Goodey, Adrian P.; Rodriguez, Marc D.; McDevitt, John T.; Anslyn, Eric V.; Neikirk, Dean P., "Development of a multi-component sensor array for the simultaneous detection of various analytes in solution," Abstracts of Papers, 222nd ACS National Meeting, Chicago, IL, United States, August 26-30, 2001.

D. Other Major Publications

V. Kesan and D. P. Neikirk, "Quantum Well Devices," **Microwaves and RF**, vol. 25, July 1986, pp. 93-97.

D. P. Neikirk, P. Cheung, M.S. Islam, and T. Itoh, "Optically Controlled Coplanar Waveguide Phase Shifters," **Microwave Journal**, Dec. 1989, pp. 77-88.

D. P. Neikirk, "Quantum Wells and Other Deep Subjects," **Discovery**, Vol. 11, No. 3, 1989, pp. 5-8.

S. M. Wentworth, J. M. Lewis, and D. P. Neikirk, "Antenna-Coupled Thermal Detectors of mm-Wave Radiation," **Microwave Journal**, Jan. 1993, pp. 94-103.

E. Book Chapter

D. B. Rutledge, D. P. Neikirk, and D. Kasilingam "Integrated- Circuit Antennas," in **Infrared and Millimeter Waves**, vol. 11, editor K.J. Button, 1984.

Nicolaos Christodoulides, Priya Dharshan, Jorge Wong, Pierre N. Floriano, Dean Neikirk and John T. McDevitt, "A Microchip-Based Assay for Interleukin-6," In: *Methods in Molecular Biology*, Volume 385: Microchip-Based Assay Systems, Humana Press, ISBN 978-1-58829-588-0 (Print) 978-1-59745-426-1 (Online), Copyright 2008, pages 131-144.

F. Technical Reports

C-K Tzuang, D. P. Neikirk, and T. Itoh, "Finite Element Analysis of Slow-Wave Schottky Contact Printed Lines," Microwave Laboratory Report No. 87-P-2, AFOSR Grant 86-0036, Feb., 1987.

D. P. Neikirk and T. Itoh, "Monolithic Phase Shifter Study," Microwave Laboratory Report No. 87-P-3, AFOSR Grant 86-0036, Jan., 1987.

V. P. Kesan and D. P. Neikirk, "Quantum Well Devices," Electrical Engineering Research Laboratory Report No. 87-P-8, Joint Services Electronics Program Research Contract AFOSR F49620-86-C-0045, August 7, 1987.

Stuart M. Wentworth and D. P. Neikirk, "High Frequency Characteristics of Tape Automated Bonding (TAB) Interconnects," Microwave Laboratory Report No. 87-P-7, August 26, 1987.

Stuart M. Wentworth and D. P. Neikirk, "Characterization of Tape Automated Bonding (TAB) Interconnects at High Frequency," Microwave Laboratory Report No. 87-P-9, October 23, 1987.

D. P. Neikirk and T. Itoh, "Monolithic Phase Shifter Study," Microwave Laboratory Report No. 90-P-1, Final Technical Report for AFOSR Grant 86-0036, Feb., 1990.

A. Mortazawi, D. Neikirk, and T. Itoh, "Microwave and millimeter wave oscillators and planar power combining structures for QWITT and Gunn diodes," Microwave Laboratory Report No. 90-P-4, Technical Report for ARO Grant DAAL03-88-K-0005 and JSEP Grant F49620-89-0044, Aug., 1990.

Oral Presentations

A. Professional Society Presentation

D. B. Rutledge and D. P. Neikirk, "Imaging Antenna Arrays," Invited Keynote Speakers, Sixth International Conference on Infrared and Millimeter Waves, Miami, Fl., Dec. 7-12, 1981.

D. P. Neikirk and D. B. Rutledge, "Advances in Microbolometers," Invited Keynote Speakers, Eighth International Conference on Infrared and Millimeter Waves, Miami, Fl., Dec. 12-17, 1983.

D. P. Neikirk, "Optically Controlled Coplanar Waveguide Millimeter Wave Phase Shifter," Tenth International Conference on Infrared and Millimeter Waves, Lake Buena Vista, Fl., Dec. 9-13, 1985.

D. P. Neikirk, "Picosecond Response of an Optically Controlled Millimeterwave Phase Shifter," Second Topical Meeting on Picosecond Electronics and Optoelectronics, Jan., 1987.

D. P. Neikirk, "Influence of Transit Time Effects on the Optimum Design and Maximum Oscillation Frequency of Quantum Well Oscillators," 12th International Conference on Infrared and Millimeter Waves, Dec. 14-18, 1987.

D. P. Neikirk, "Measurements of an Optically Controlled Coplanar Waveguide Phase-Shifter," 12th International Conference on Infrared and Millimeter Waves, Dec. 14-18, 1987.

D. P. Neikirk, "High Frequency Characterization of Tape-Automated Bonding Interconnects," 5th Annual Texas Regional Symposium, International Society of Hybrid Manufacturing, April 11, 1988.

D. P. Neikirk, "Time Dependent Simulation of the Quantum Well Injection Transit Time Diode," 13th International Conference on Infrared and Millimeter Waves, Dec. 5-9, 1988.

D. P. Neikirk, "Experimental Performance of a Periodically Illuminated Optically Controlled Coplanar Waveguide Phase Shifter," 13th International Conference on Infrared and Millimeter Waves, Dec. 5-9, 1988.

B. Invited Lectures

1. D. P. Neikirk, "Exotic Heterojunction Devices for Microwave Circuits," NSF Workshop on Future Research Opportunities in Electromagnetics, Arlington, TX., January 29-31, 1986.

2. D. P. Neikirk, "Optical Control of a Monolithic Millimeter Phase Shifter," ARO Workshop on Fundamental Issues in Millimeter and Submillimeter Waves, Los Angeles, Ca., Sept. 15-16, 1986.

3. Dean P. Neikirk, "Quantum Well Oscillators for Millimeter Wave Applications," 1987 Workshop on Compound Semiconductor Microwave Materials and Devices (WOCSEMMAD), Hilton Head Island, S.C., March 2-4, 1987.

4. S.M. Wentworth and D. P. Neikirk, "High Frequency Tape-Automated Bonding (TAB) Interconnect Characterization," IEEE 6th Annual VLSI and GaAs Packaging Workshop, Sept. 14-16, 1987.

5. D. P. Neikirk, "The quantum well injection transit time diode," Engineering Foundation Conference on Advanced Heterostructure Transistors, Keauhou-Kona, Hawaii, Dec. 5-10, 1988.
6. D. P. Neikirk, ""The High Frequency Characteristics of Tape Automated Bonding (TAB) Interconnects," presented to the Microelectronics and Computer Technology Corporation, April 19, 1989.
7. Dean P. Neikirk, "Impedance measurements of quantum well diodes for millimeter wave applications," 1990 Workshop on Compound Semiconductor Microwave Materials and Devices (WOCSEMMAD), San Francisco, CA., Feb. 12-14, 1990.
8. Dean P. Neikirk, "Twin-slot multi-layer substrate-supported antennas and detectors for terahertz imaging," First International Symposium on Space Terahertz Technology, University of Michigan, Ann Arbor, Mich., March 5-6, 1990.
9. Dean P. Neikirk, "Microwave and Millimeterwave Oscillators using Quantum Well Diodes," Joint IEEE MTT/ED Dallas Chapter meeting, Sept. 27, 1990.
10. Dean P. Neikirk, "Quantum Transport Simulations of Resonant Tunneling Diodes," 1991 Workshop on Compound Semiconductor Microwave Materials and Devices (WOCSEMMAD), Ft. Lauderdale, FL., Feb. 18-20, 1991.
11. Dean P. Neikirk, "The Application of Physics in Electrical Engineering (or is it Engineering in Physics?): Electromagnetics in Very High Frequency Semiconductor Devices," Physics Colloquium, Oklahoma State University, March 5, 1992.
12. D. P. Neikirk and B. G. Streetman, "MBE growth of multilayer heterostructures for photonic and high-speed electronic devices," Engineering Foundation Conference on High Speed Optoelectronic Devices and Circuits II, Banff, Alberta, Canada, Aug. 9-13, 1992.
13. L. T. Pillage, D. P. Neikirk, and R. Mercer, "Design automation techniques and algorithms for application specific electronic modules (ASEMs)," ARPA Electronic Packaging & Interconnect Principle Investigator Meeting, Marina del Ray, CA, Feb. 14-18, 1994.
14. D. P. Neikirk, "Micro-sensors - What happens when you make classical devices small?: Integrated Bolometric Radiation Detectors," Texas Instruments, Dallas, Texas, Oct. 20, 1994.
15. Dean P. Neikirk, "Micromachined sensors," Motorola Sensors Steering Committee, Albuquerque, New Mexico, March 28, 1995.
16. D. P. Neikirk, E. Tuncer, and B.-T. Lee, "The Use of Effective Internal Impedance Approximations in Lossy Transmission Line Modeling," *Progress in Electromagnetics*

Research Symposium PIERS 95, The University of Washington, Seattle, Washington, July 28, 1995.

17. D. P. Neikirk, M. S. Islam, and E. Tuncer, "Accurate Quasi-Static Modeling of Transmission Lines on Semiconducting Substrates," *Progress in Electromagnetics Research Symposium PIERS 95*, The University of Washington, Seattle, Washington, July 28, 1995.

18. D. P. Neikirk, "Impact of Finite Metal Conductivity on Inductance Extraction of Interconnects and Packages," Sematech meeting on Electrical Modeling Challenges Faced by Packaging Designers, Austin, Texas, Nov. 19, 1995.

19. D. P. Neikirk, "Micromachined Fabry-Perot Pressure Transducers," Hughes Research Laboratory, Malibu, California, Nov. 21, 1995.

20. D. P. Neikirk, "Classical Devices Made Small; or 'What's the big deal about little machines?'" , Manufacturing 2000, University of Texas at Austin, Feb. 23, 1996.

21. D. P. Neikirk, "Interconnect Inductance Modeling from DC to the Skin Effect Limit," Quad Designs, Camarillo, CA, July 10, 1996.

22. D. P. Neikirk, "Efficient Conductor Boundary Conditions in the dc to Skin Effect Limit," DARPA MAFET Program Review, Fairfax, VA, Oct. 27-31, 1997.

23. Micromachined Array-based Multi-analyte Chemical Sensors: Towards the Fabrication of an "Electronic Tongue" South, Texas Local Section of The Electrochemical Society Meeting, April 17, 1999.

24. D. P. Neikirk, "Resonant Chemical Surveillance Tags," IEEE Electron Device Chapter, Central Texas Section, September 25, 2008.

25. D.P. Neikirk, "Near Borehole Condition Sensing," Nanotechnology Conference and Trade Show - Nanotech 2009, Houston, TX May 3-7, 2009, Nanotech & Cleantech for Oil & Gas Session, (Session chair: Sean Murphy, Advanced Energy Consortium), May 5, 2009.

26. D.P. Neikirk, "Integrated Threshold Nanosensor Systems," Advanced Oil Consortium Microfabricated Sensors Workshop, Houston Research Center, Bureau of Economic Geology, University of Texas at Austin, September 8th-9th, 2010.

27. D. P. Neikirk, "Sensing systems for "harsh" environments," Engineering Challenges for Deepwater Drilling at the "U.S. Offshore Oil Exploration: Managing Risks to Move Forward," James A. Baker III Institute for Public Policy and PFC Energy, Rice University, Houston, TX, February 11, 2011.

C. Other Conference Presentations

Praveen Pasupathy, Mingxiang Zhuzhou, Shasi K. Munukutla, Dean P. Neikirk, and Sharon L. Wood, “Resonant Wireless Sensor Nets for Civil Infrastructure Health Monitoring,” 2009 National Science Foundation Division of Civil, Mechanical and Manufacturing Innovation (CMMI) Engineering Research and Innovation Conference, Honolulu, Hawaii, June 22-25, 2009.

Technical Consulting

Teltech Resource Network (1985-1993)
Ardex, Inc. (1986-88)
University and Polytechnic Grants Committee, Consultancy to examine Equipment Requirements for the Hong Kong University of Science and Technology, July, 1989
E. P. Hamilton Associates, (1987-90)
Burnett Company, Microwave Heating for Secondary Oil Recovery, July, 1990
Microelectronics and Computer Technology Corporation, June, 1990
Microelectronics and Computer Technology Corporation, Oct., 1994 - Sept., 1996
Baker-Hughes

University Committee Assignments

Departmental:

Graduate Student Financial Aid, Sept. 1984- Sept. 1987
Faculty Recruiting, Sept. 1984- Aug. 1985
Microelectronics Jr. Faculty Recruiting, Sept. 1985- Sept. 1987 (chairman)
ECE Safety Committee, Sept. 1985- Aug. 1993 (chairman, 1985-89)
ECE Electronics Shop Coordinating Committee, March 1986- Aug. 1993
Solid State Electronics Area Graduate Advisor, Aug. 1986- Aug. 89
ECE Space Allocation Committee, Sept. 1989-Aug. 1993 (chairman)
ECE Facilities Committee, Sept. 1993- Aug. 1996 (chairman)
ECE Areas Committee, Electromagnetics/Acoustics, Sept. 1993-present
ECE Ad Hoc Committee to Review the Undergraduate Curriculum, Jan. 1995- Aug. 1995
ECE World Wide Web Home Page Committee, Sept. 1995-Aug. 1996
ECE Ad Hoc Committee to Review the Undergraduate Curriculum, Jan. 1997- Aug. 1997
ECE Areas Committee, Materials and Quantum Electronics, Sept. 1993-present; chairman, Sept. 1996-present
Chair of ECE Graduate Studies Committee, May 1998-August 2006
ECE Chair's council, November 1999-2010
ECE Graduate Advisor, Sept. 1999- 2010
ECE Associate Chair, Sept. 2001-Dec. 2010
ECE peer Faculty Annual Review Committee, Sept. 2012-Aug. 2013

College:

Engineering Scholastic Appeals, Sept. 1984- Aug. 1985
Engineering Safety Committee, Sept. 1985- Aug. 1994 (chairman, Sept. 1989-Aug. 1994)

Aerospace Engineering Machine Shop, Sept. 1989-Aug. 1993
 College Annual Report Quality Team, Jan. 1994- Aug. 1994
 College Multimedia Committee, Sept. 1995-Aug. 2000
 Equal Opportunity in Engineering (EOE) Program, 1995-Dec. 1996
 Graduate Fellowship Review Committee, Sept. 2011-Aug. 2013

University:

Presidential Ad Hoc Committee on Research Infrastructure Enhancement, Jan. 1988 - Aug. 1994
 Research Safety Advisory Committee, Oct. 1991-present (chairman, Sept. 1996-1999)
 Ad Hoc Consultative Committee for the Selection of a Dean of the College of Engineering, Nov. 1995-May 1996
 Faculty Building Advisory Committee, Sept. 1995-Aug. 2000; Aug. 2003-Aug. 2004
 Ad Hoc Project Committee for Parking Garage # 4A, Sept. 1996-Aug. 2000
 Faculty Council, Sept. 1996-Aug. 2000; Sept. 2002 - Aug. 2004
 Faculty Advisory Committee on the Budget, Sept. 99 - Aug. 2000; Sept. 2008 – Aug. 2011 (vice chair Sept. 2009- Aug. 2010)
 Graduate Assembly, April 1997- Aug. 2000; Sept. 2001 - Aug. 2008
 Administrative sub-committee of GA, Sept. 1997-Aug. 1998; Sept. 2006-Aug. 2007
 Academic sub-committee of GA, Sept. 1998-Aug. 2000; Sept. 2001-Aug. 2006; Sept. 2007-Aug. 2008
 Chair, Graduate Assembly, 2004-2005
 Academy of Distinguished Teachers selection committee, academic year 1999-2000
 Outstanding Graduate Adviser selection committee, academic year 1999-2000
 Outstanding Graduate Coordinator selection committee, academic year 1999-2000
 Faculty Council, Sept. 2008 – Aug. 2012; Chair-elect Sept. 2009- Aug. 2010; Chair Sept. 2010- Aug. 2011; past chair: Sept. 2011-Aug. 2012
 Faculty Council Executive Committee, Sept. 2009 – Aug. 2012
 General Faculty Rules and Governance Committee, Sept. 2010 – Aug. 2015 (Chair, Sept. 2011 – Aug. 2013)
 Ad Hoc Consultative Committee for the Selection of a Dean of the Graduate School, Nov. 2012 – Sept. 2012
 Secretary of the General Faculty and Faculty Council, Sept. 2013 – Aug. 2015
 Committee on Undergraduate Degree Program review, Sept. 2013 – Aug. 2015
 Faculty Council Executive Committee, Sept. 2013 – Aug. 2015
 Faculty Committee on Committees, *ex officio* member, Sept. 2013 – Aug. 2015

UT System:

Task Force on Doctoral Programs and Post-Doctoral Experience, Spring-Fall 2006

University of Texas System Faculty Advisory Council, Sept. 2009- Aug. 2011

State of Texas:

Texas Higher Education Coordinating Board Graduate Education Advisory Committee (GEAC), September 1, 2015 - August 31, 2018.

Evidence of Teaching Effectiveness

Senior Design Projects:

Umer Yousafzai and Venuka Jayatilaka, Spring 1994

Chris Eiting and Sonny Gonzalez, Spring 1994

David Lee and David Onsongo, Fall 1996

Dave Pyle and Aruna Murthy, Spring 1999

Hitesh Mehta and Edward Zhu, Spring 1999, "Giving the electronic tongue a sense of good taste: image analysis tools and GUI"

Gus Espinosa and Donnie Garcia, Spring 1999, "Design and Implementation of a Computer Interfacing Circuit to Control LED's for use with a Chemical Sensor"

Natthanant Pon Skulkaew and Prem Nainani, Spring 2001, "PC-based data acquisition and wireless transmission system"

Matthew Andringa and Allen Hall, Spring 2001, "Non-Invasive RFID Weld Inspection"

Michael Amalfitano and Sapun Parekh, Spring 2002, "Output circuitry for a transmitter used in an Electronic Structural Surveillance system"

Kunal Patel and Jacy Little, Spring 2002, "Swept, high frequency oscillator to work in an Electronic Structural Surveillance (ESS) system"

Dong Pak, Spring 2002, "Automated image-processing software of an electronic chemical sensor"

Rajesh Nerlikar, Jonathan Solomon, Spring 2003, "Wireless Data Acquisition System for Bluetooth-enabled RFID Readers"

Nola Li, Judith Chen, Maria Huang, Fall 2003, "Design and build a tuning network for a swept frequency reader used in structural health analysis"

Tuenlap (Daniel) Chan, Imranul Islam, Derek Choi, Spring 2004, "Design and build an RFID Interrogator Receiver"

John McKee and Terence Man, Spring 2007, "Improved Corrosion Sensors"

Abdulaziz Beayeyz, Sravan Bhagavatula, Rahul Mitra, Shasi Munukutla, Spyder Spann, Fall 2009, "Portable Corrosion Detector"

Jonathan Pham, Po-Han Wu, Josh Schulte, Pritesh Solanki, Mesele Bedasa, Spring 2011- Fall 2011, "Multi-Sensor Robotics Platform"

Raymund Lee, Simon Chow, Connor Landy, Kevin Woo, and Anirudh Kashyap, Fall 2012-Spring 2013, "Variable Frequency RFID Tag and Reader"

Javier Chacon, Joshua Poncik, Joshua Orozco, Sebastian Salomon, Yongcong Zou, Fall 2013-Spring 2014, "Environmental Sensor Monitoring Network"

Organized Classes Taught:

EE 363M Introduction to Microwaves, Spring 1984, # 16455
 EE 396K VLSI Fabrication Techniques, Fall 1984, # 16255
 EE 379K Integrated Circuit Fabrication, Spring 1985, # 16055
 EE 396K VLSI Fabrication Techniques, Fall 1985, # 16275
 EE 379K Integrated Circuit Fabrication, Fall 1985, # 16070
 EE 396K VLSI Fabrication Techniques, Spring 1986, # 17680
 EE 379K Integrated Circuit Fabrication, Spring 1986, # 17450
 EE 396K VLSI Fabrication Techniques, Fall 1986, # 15245
 EE 379K Integrated Circuit Fabrication, Fall 1986, # 15020
 EE 396K VLSI Fabrication Techniques, Spring 1987, # 15205
 EE 379K Integrated Circuit Fabrication, Spring 1987, # 14970
 EE 396K VLSI Fabrication Techniques, Fall 1987, # 15010
 EE 440 Integrated Circuit Fabrication, Fall 1987, # 14545
 EE 363M Introduction to Microwaves, Spring 1988, # 14535
 EE 396K VLSI Fabrication Techniques, Spring 1988, # 14865
 EE 440 Integrated Circuit Fabrication, Spring 1988, # 14390
 EE 396K VLSI Fabrication Techniques, Fall 1988, # 15165
 EE 440 Integrated Circuit Fabrication, Fall 1988, # 14705
 EE 363M Introduction to Microwaves, Spring 1989, # 14525
 EE 396K VLSI Fabrication Techniques, Spring 1989, # 14855
 EE 396K VLSI Fabrication Techniques, Fall 1989, # 15165
 EE 440 Integrated Circuit Fabrication, Fall 1989, # 14705
 EE 363M Introduction to Microwaves, Spring 1990, # 14050
 EE 396K VLSI Fabrication Techniques, Spring 1990, # 14355, 14360
 EE 440 Integrated Circuit Fabrication, Spring 1990, # 13915, 13920
 EE 396K VLSI Fabrication Techniques, Fall 1990, # 14630, 14635
 EE 440 Integrated Circuit Fabrication, Fall 1990, # 14200, 14205
 EE 363M Introduction to Microwaves, Spring 1991, # 14365
 EE 396K VLSI Fabrication Techniques, Spring 1991, # 14660, 14665, 14670
 EE 440 Integrated Circuit Fabrication, Spring 1991, # 14220, 14225, 14230
 EE 396K VLSI Fabrication Techniques, Fall 1991, # 14865, 14860
 EE 440 Integrated Circuit Fabrication, Fall 1991, # 14425, 14430
 EE 363M Introduction to Microwaves, Spring 1992, # 14270
 EE 396K VLSI Fabrication Techniques, Spring 1992, # 14545, 14550, 14555
 EE 440 Integrated Circuit Fabrication, Spring 1992, # 14130, 14135
 EE 396K VLSI Fabrication Techniques, Fall 1992, # 15095, 15100, 15105
 EE 440 Integrated Circuit Fabrication, Fall 1992, # 14670, 14675
 EE 397K Microwave Devices, Spring 1993, # 14805
 EE 396K VLSI Fabrication Techniques, Fall 1993, # 14800, 14805, 14810
 EE 440 Integrated Circuit Fabrication, Fall 1993, # 14385, 14390
 EE 363M Introduction to Microwaves, Spring 1994, # 14370
 EE 396K VLSI Fabrication Techniques, Fall 1994, # 14365

EE 440 Integrated Circuit Fabrication, Fall 1994, # 13870
 EE 397K Electromagnetics in Packaging, Spring 1995, # 14555
 EE 396K VLSI Fabrication Techniques, Fall 1995, # 14765
 EE 440 Integrated Circuit Fabrication, Fall 1995, # 14260
 EE 397K Electromagnetics in Packaging, Spring 1996, # 14695
 EE 382M Simulation Methods in CAD/VLSI, Spring 1996, # 14500
 EE 396K VLSI Fabrication Techniques, Fall 1996, # 14535
 EE 440 Integrated Circuit Fabrication, Fall 1996, # 14090
 EE 382M Simulation Methods in CAD/VLSI, Spring 1997, # 14325
 EE 363M Introduction to Microwaves, Spring 1997, # 14120
 EE 396K VLSI Fabrication Techniques, Fall 1997, # 15315
 EE 440 Integrated Circuit Fabrication, Fall 1997, # 14820
 EE 363M Introduction to Microwaves, Spring 1998, # 14530
 EE 397K Microwave Devices, Spring 1998, # 14950
 EE 396K VLSI Fabrication Techniques, Fall 1998, # 15475
 EE 440 Integrated Circuit Fabrication, Fall 1998, # 14965
 EE 363M Introduction to Microwaves, Spring 1999, # 14825
 EE 397K Microwave Devices, Spring 1999, # 15260
 EE 396K VLSI Fabrication Techniques, Fall 1999, # 15340
 EE 440 Integrated Circuit Fabrication, Fall 1999, # 14820
 EE 363M Introduction to Microwaves, Spring 2000, # 14755
 EE 396K VLSI Fabrication Techniques, Fall 2000, # 15600
 EE 440 Integrated Circuit Fabrication, Fall 2000, # 15100
 EE 397K Micro-electromechanical Systems (MEMS), Spring 2001, #15170
 EE 396K VLSI Fabrication Techniques, Fall 2001, # 15725
 EE 440 Integrated Circuit Fabrication, Fall 2001, # 15230
 EE 397K Micro-electromechanical Systems (MEMS), Spring 2002, #15330
 EE 396K VLSI Fabrication Techniques, Fall 2002, # 16050
 EE 440 Integrated Circuit Fabrication, Fall 2002, # 15485
 EE 397K Microwave Devices, Spring 2003, # 15110
 EE 396K VLSI Fabrication Techniques, Fall 2003, # 15580
 EE 440 Integrated Circuit Fabrication, Fall 2003, # 15095
 EE 325 Electromagnetic Engineering, Spring 2004, # 14345
 EE 396K VLSI Fabrication Techniques, Fall 2004, # 16250
 EE 440 Integrated Circuit Fabrication, Fall 2004, # 15715
 EE 396K 26-Microelectromechanical Systems, Spring 2005, # 15690
 EE 396K VLSI Fabrication Techniques, Fall 2005, # 16455
 EE 440 Integrated Circuit Fabrication, Fall 2005, # 15930
 EE 396K VLSI Fabrication Techniques, Fall 2006, # 17040
 EE 440 Integrated Circuit Fabrication, Fall 2006, # 16430
 EE 325 Electromagnetic Engineering, Spring 2007, # 15765
 EE 396K VLSI Fabrication Techniques, Fall 2007, # 17425
 EE 440 Integrated Circuit Fabrication, Fall 2007, # 16770
 EE 396K-26 Microelectromechanical Systems, Spring 2008, # 16815
 EE 396K VLSI Fabrication Techniques, Fall 2008, # 17380
 EE 325 Electromagnetic Engineering, Spring 2009, # 16000

EE 396K-24 Microwave Devices, Spring 2010, # 16975
 EE 396K VLSI Fabrication Techniques, Fall 2010, # 17075, 17080, 17085, 17090
 EE 440 Integrated Circuit Fabrication, Fall 2010, # 16540, 16545, 16550, 16555
 EE 396K VLSI Fabrication Techniques, Fall 2011, # 17295, 17300, 17305, 17310
 EE 440 Integrated Circuit Fabrication, Fall 2011# 16760, 16765, 16770, 16775
 EE 396K 26-Microelectromechanical Systems, Spring 2012, #17070
 EE 396K VLSI Fabrication Techniques, Fall 2012, # 17185, 17190, 17195, 17200
 EE 440 Integrated Circuit Fabrication, Fall 2012, # 16640, 16645, 16650, 16665
 EE 363M Introduction to Microwaves, Spring 2013, # 16605
 EE 396K Ultra Large Scale Integrated Circuit Fabrication Techniques, Fall 2013, # 17425, 17430, 17435, 17440
 EE 440 Integrated Circuit Nanomanufacturing Techniques, Fall 2013, # 16790, 16795, 16800, 16805
 EE 396K-24 Microwave Devices. Spring 2014, #17440
 EE 396K Ultra Large Scale Integrated Circuit Fabrication Techniques, Fall 2014, #17525, 17530, 17535, 17540
 EE 440 Integrated Circuit Nanomanufacturing Techniques, Fall 2014, #16960, 16965, 16970, 16975
 EE 363M Microwave and Radio Frequency Engineering, Spring 2015, #16355
 EE 396K Ultra Large Scale Integrated Circuit Fabrication Techniques, Fall 2015, #16965, 16970, 16975
 EE 440 Integrated Circuit Nanomanufacturing Techniques, Fall 2015, #16480, 16485, 16490
 EE 363M Microwave and Radio Frequency Engineering, Spring 2016, #16550
 EE 396K Ultra Large Scale Integrated Circuit Fabrication Techniques, Fall 2016
 EE 440 Integrated Circuit Nanomanufacturing Techniques, Fall 2016
 EE 396K 26-Microelectromechanical Systems, Spring 2017
 EE 363M Microwave and Radio Frequency Engineering, Spring 2018, #15890
 EE 363M Microwave and Radio Frequency Engineering, Spring 2019, #16625
 EE 363M Microwave and Radio Frequency Engineering, Spring 2020, #16695

Continuing Education Courses Taught

"Microelectronics Fabrication - Chemical Aspects," with Isaac Trachtenberg, Continuing Engineering Studies, College of Engineering, The University of Texas at Austin, June 1-4, 1987.
 "Integrated Circuit Process & Design," with M. R. Mercer, Motorola short course, Continuing Engineering Studies, College of Engineering, The University of

Texas at Austin:

- Aug.-Sept., 1987
- Nov.-Dec., 1987
- Nov.-Dec., 1988
- March-April, 1989
- Aug.-Sept., 1989
- Nov.-Dec., 1989
- Feb.-March, 1990
- April, 1990
- Aug., 1990

"Integrated Circuit Processing and Design," with L. T. Pillage, Advanced Micro Devices short course, Continuing Engineering Studies, College of Engineering, The University of Texas at Austin:

- Oct.-Nov., 1990
- June-July, 1991

"Microelectronics Fabrication," for the Fellows of the Senior Service College Fellowship Program, Continuing Engineering Studies, College of Engineering, The University of Texas at Austin, yearly 1993-2003.