

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INERGY TECHNOLOGY, INC.,
Petitioner

v.

FORCE MOS TECHNOLOGY CO. LTD.,
Patent Owner

Inter Partes Review No. IPR2024-00093
U.S. Patent No. 7,629,634

PATENT OWNER'S RESPONSE
(37 CFR § 42.120)

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Patent Owner's Exhibit List

Exhibit No.	Description
2001	Transcript of Feb. 13, 2024 Deposition of David Kuan-Yu Liu, PhD in <i>Force MOS Technology Co., Ltd. v. ASUSTeK Computer, Inc.</i> , Case No. 2:22-cv-00460-JRG (E.D. Tex.)
2002	Declaration of David Kuan-Yu Liu, Ph.D., served on Jan. 30, 2024 in <i>Force MOS Technology Co., Ltd. v. ASUSTeK Computer, Inc.</i> , Case No. 2:22-cv-00460-JRG (E.D. Tex.)
2003	Defendant ASUSTeK Computer, Inc.'s Motion to Stay Pending Resolution of Inter Partes Reviews, filed on Nov. 30, 2023 as Dkt. No. 30 in <i>Force MOS Technology Co., Ltd. v. ASUSTeK Computer, Inc.</i> , Case No. 2:22-cv-00460-JRG (E.D. Tex.)
2004	Amended Docket Control Order, filed on Jan. 18, 2024 as Dkt. No. 35 in <i>Force MOS Technology Co., Ltd. v. ASUSTeK Computer, Inc.</i> , Case No. 2:22-cv-00460-JRG (E.D. Tex.)
2005	Cover pleading to Defendant ASUSTeK Computer, Inc.'s Invalidity Contentions, served on Jul. 18, 2024 in <i>Force MOS Technology Co., Ltd. v. ASUSTeK Computer, Inc.</i> , Case No. 2:22-cv-00460-JRG (E.D. Tex.)
2006	Excerpts from S. Gibilisco, Illustrated Dictionary of Electronics (2001) for "layer"
2007	Excerpts from J. Ruzyllo, Semiconductor Glossary (2d Ed. 2017) for "doping by ion implantation," "doping during material growth," "ion implantation"
2008	U.S. Patent No. 6,888,196 to Kobayashi
2009	Claim Construction Declaration of Dean Neikirk, Ph.D. (Corrected), as filed as Exhibit D to Dkt. No. 74 in <i>Alpha and Omega Semiconductor Limited, et al. v. Force MOS Technology Co. Ltd.</i> , Civ. No. 5:22-cv-05448 (N.D. Cal.)

Exhibit No.	Description
2010	Memorandum Order and Opinion (regarding claim construction), Dkt. No. 94 from <i>Alpha and Omega Semiconductor Limited et al v. Force MOS Technology Co., Ltd.</i> , Case No. 5:22-cv-05448-PCP (N.D. Cal.)
2011	Claim Construction Order, Dkt. No. 132 from <i>Force MOS Technology Co., Ltd. v. ASUSTeK Computer, Inc.</i> , Case No. 2:22-cv-00460-JRG (E.D. Tex.)
2012	Declaration of Dean Neikirk, Ph.D. in Support of Patent Owner's Response
2013	Curriculum Vitae of Dean Neikirk, Ph.D.
2014	Transcript of Aug. 22, 2024 Deposition of David Kuan-Yu Liu
2015	Zhang, Ruizhe, and Yuhao Zhang. "Power device breakdown mechanism and characterization: Review and perspective." <i>Japanese Journal of Applied Physics</i> 62.SC (2023): SC0806
2016	Additional Excerpts from Semiconductor Glossary
2017	Search results from scholar.google.com for article search “‘lateral contact layer’ MOSFET”
2018	Wang, Jingshan. High-Power Vertical GaN Electronic Devices Formed by Epitaxial Lift-Off. Diss. University of Notre Dame, 2018.
2019	Definition of “lateral” from https://www.merriam-webster.com/dictionary/lateral
2020	--Intentionally Not Used--
2021	Definition of “contact” from https://www.merriam-webster.com/dictionary/contact
2022	Definition of “contact” from https://www.lamresearch.com/technical-glossary/

Exhibit No.	Description
2023	Definition of “layer” from https://www.merriam-webster.com/dictionary/layer
2024	U.S. Patent No. 3,025,589 to Hoerni, “Method of manufacturing semiconductor devices”
2025	Definition of “layer” from https://dictionary.cambridge.org/us/dictionary/english/layer
2026	Suzuki, Kunihiro, A. Satoh, and T. Sugii. "Counter doping into uniformly and heavily doped channel region of sub-0.1 μm SOI MOSFETs." IEEE Electron Device Letters 17.1 (1996)
2027	U.S. Patent No. 4,315,781 to Henderson, “Method of controlling MOSFET threshold voltage with self-aligned channel stop”
2028	U.S. Patent No. 8,884,409 to Wong, “Wafer backside doping for thermal neutron shielding”
2029	Definition of “cover” from https://www.merriam-webster.com/dictionary/cover
2030	Excerpts of Sedra, Adel S., Microelectronic Circuits (5 th Ed. 2004)
2031	Excerpts of Williams, Principles and Elements of Power Electronics, ISBN 978-0-9553384-0-3 (2006)
2032	Sharma, R. S., and M. A. Peer. "Some Features of Avalanche Breakdown Phenomena Part 1: Transistors and Diodes." IETE Journal of Research 27.5 (1981): 178-184
2033	U.S. Patent No. 6,084,264 to Darwish, “Trench MOSFET having improved breakdown and on-resistance characteristics”
2034	U.S. Patent No. 6,545,315 to Hshieh et al., “Trench DMOS transistor having reduced punch-through”

Pursuant to 37 C.F.R. § 42.120, Patent Owner Force MOS Technology Co. Ltd. (“Patent Owner” or “Force MOS”) hereby submits its Patent Owner Response.

I. INTRODUCTION

The “lateral contact layer”—recited in the sole independent claim of the ’634 Patent—is the key improvement over the prior art identified by the ’634 Patent. Despite that, Petitioner proposes no construction for that term, and applies it to the prior art in an unclear and inconsistent manner. The term “lateral contact layer” is a coined term, whose meaning cannot be discerned simply from looking at its constituent words. Instead, its meaning can only be understood by reference to the specification, which discloses that it is a region of dopant which is implanted into sidewalls of the source contact trenches to have a P* dopant concentration.

Applying the appropriate construction of “lateral contact layer,” Petitioner’s grounds readily fail. Hirler does not have a P* layer, and its body amplification zone is not implanted into the sidewalls of a source contact trench, but rather is implanted into a broad region of the cell in which such a trench is subsequently etched. Shiraishi similarly does not disclose or suggest a P* layer, and its layer 14 is implanted broadly across the active region of the MOSFET, before any source contact trench is etched. And, in any event, Shiraishi does not disclose that its layer 14 covers the entire sidewalls of the source contact trench in the base layer, as required by Petitioner’s own construction. For the same reasons, combining

Shiraishi's layer 14 with Kobayashi would not render the lateral contact layer limitation obvious.

Hirler and Shiraishi also fail to satisfy limitation 1[a] of the '634 Patent. In particular, Hirler does not disclose an "epitaxial layer corresponding to said drain region." Petitioner makes no effort to show that Hirler's n- drift zone is necessarily created via epitaxy, and presents no obviousness arguments regarding epitaxy. Shiraishi fails to disclose limitation 1[a], which requires a specific series of layers disposed on top of each other (i.e. an epitaxial layer on top of a substrate, a base layer on top of the epitaxial layer, and a source layer on top of the base layer). In particular, Petitioner asserts that Shiraishi's layer 13 is the base layer, but Shiraishi's layer 14 is interposed between layer 13 and Shiraishi's source layer. For the same reasons, Petitioner's proposed combination of Kobayashi with Shiraishi's layer 14 fails to satisfy limitation 1[a]

Petitioner's obviousness theory for dependent claims 3-5 and 7-9 likewise fails. In particular, Petitioner assumes that the combinations would use tungsten plugs, and then identifies reasons why it would be obvious to use a barrier layer with tungsten plugs. However, because Hirler and Shiraishi disclose alternatives to tungsten plugs, Petitioner's obviousness theory is inadequate. Moreover, Petitioner disregards other ways to achieve the claimed benefits of a smooth top, i.e. the well-known technique of chemical mechanical planarization.

For all of these reasons, the Board should hold that all challenged claims are patentable.

II. OVERVIEW OF THE '634 PATENT

The '634 Patent relates to trench MOSFETs with source contact trenches, where each of the source contact trenches has a lateral contact layer at a sidewall thereof. Ex. 1001 ("'634 Patent"), Abstract. A trench MOSFET (metal-oxide-semiconductor field effect transistor) allows high current to pass through and for the channel to turn on or off using a low voltage. *Id.*, 1:11-17. The '634 Patent recognizes that, in a traditional trench MOSFET design, the sidewall of the source contact trench has no ohmic contact with the contact metal plug, which results in poor ruggedness performance of an Unclamp Inductive Switching (UIS) test. *Id.*, 1:35-38. In particular, when P base resistance from the channel to the source contact is too high, device destruction can occur. *Id.*, 1:38-42.

The '634 Patent addresses this problem in the prior art by implanting a P*-type lateral contact layer into parts of the sidewall of the source contact trenches, where P* has more doping than the P base layer, but less doping than the P+ base contact layer which is located at the bottom of the source contact trench. *Id.*, 2:1-11; Ex. 2012 ¶¶73-73. The '634 Patent describes optimizing the P*-type lateral contact layer doping concentration in order to achieve ohmic contact between the

P*-type layer and a contact metal plug without significantly increasing threshold voltage of the device. '634 Patent, 2:1-11.

III. OVERVIEW OF THE ASSERTED PRIOR ART

1. German Pat. Pub. No. DE 102004009083 (“Hirler”)

Hirler reference is directed the prior art’s problem of correctly setting the “depth of the contact zone” in trenched MOSFETs with trenched source contacts. Ex. 1006, [0003]. Hirler explains that, in the prior art, body contact zones were used to ensure good contact between the MOSFET’s source and body without helping avoid avalanche breakdown. *Id.*, [0002]. However, this required precision. If the contact zone was too shallow, it would not adequately clamp breakdown. *Id.*, [0003]. But, if the contact zone was too deep, breakdown voltage is reduced too much. *Id.* Thus, Hirler tries to address avalanche breakdown “without precisely defining the depth of the body contact zone.” *Id.*, [0007]; Ex. 2012 ¶104. It does this using a “body amplification zone” that “contains at least parts of the body contact zone.” Ex. 1006, [0008].

2. U.S. Patent Publication No. 2005/0029584 (“Shiraishi”)

Shiraishi attempt to improve the on-resistance and punch-through ruggedness of certain prior art trench MOSFETs. Ex. 1009 (Shiraishi), Abstract. Shiraishi explains that, in prior trench gate MOSFETs, the gate insulator of deep trench gates can increase capacitance. *Id.*, [0007], [0013]. Capacitance can be reduced by

narrowing the trench gates and reducing how far they penetrate into the drift layer. *Id.*, [0013]. However, making the gates too narrow can increase on-resistance. *Id.*, [0014]. And, making the trench gates too shallow can result in a short channel effect, resulting in punch-through (i.e., partial breakdown where the depletion region at the body-drift interface extends to connect to the depletion region at the source-body interface). *Id.*, [0014], [0080], [0085], Fig. 14; Ex. 2012 ¶106. Such punch-through could be prevented by increasing the dopant concentration of the entire body region, but that would significantly increase threshold voltage. Ex. 1009, [0015].

Shiraishi addresses these various problems by the introduction of a thin punch-through stopper layer (layer 14). Ex. 1009, [0081]. Layer 14 has the same doping type as the body, but is more strongly doped. *Id.*, [0080]. Layer 14 is located below the source layer and extends all the way, side-to-side between the gate trenches and source contact trenches. *Id.*, Fig. 9, [0080]-[0081], claim 22. The punch-through layer allows the channel to be shorter, permitting shallower gate trenches, thereby improving capacitance, without increased risk of punch-through. *Id.*

3. U.S. Patent Publication No. 2004/0021174 (“Kobayashi”)

Kobayashi is directed to an improved design for trench MOSFETs with trench source contacts. In such MOSFETs, a P⁺-type contact layer is formed at the bottom of the contact hole, but horizontal diffusion of that implant this can result

in increased dopant concentration in the channel region. Ex. 1008 (Kobayashi), [0014]-[0016]. This limits how much cell size may be reduced. *Id.*, [0014]. Kobayashi addresses this problem in two main ways. In the first method, Kobayashi ensures the depth of the source contact trench (and thus the depth of the P+ contact layer) is set precisely so it avoid being at the same depth as the depth where dopant concentration is the highest in the base layer. *Id.*, [0018]-[0019], [0025], Figs. 5A, 5B, 7C. As a result, impurities from the P+ base contact layer are less likely to leach into the channel region and increase threshold voltage. *Id.*, [0037]. In the second method, Kobayashi introduces a metal silicide layer around the source contact's bottom and sidewalls to suppress source contact resistance. *Id.*, [0022], [0070]-[0071], Figs. 10, 11A (element 15). Kobayashi also discusses a source metallization process where Tungsten plugs are added (*Id.*, Fig. 8A) followed by a planarization process (*Id.*, Fig. 8B), followed by back side metallization with aluminum (*Id.*, Fig. 8C). Ex. 2012 ¶106.

IV. LEVEL OF SKILL IN THE ART

Petitioner argues that a person of ordinary skill in the art (“POSITA”) would have “have a master’s degree in electrical engineering, and at least two years of relevant work experience in the field of integrated circuit design and manufacturing.” Pet., 15. For the purpose of this proceeding, Patent Owner does not dispute that characterization. Ex. 2012 ¶55.

V. CLAIM CONSTRUCTION

A. “lateral contact layer”

In its preliminary response in this IPR, Patent Owner argued that “lateral contact layer” should mean “a region of dopant which is implanted into sidewalls of the source contact trenches to have a dopant concentration between P and P+ (“P* doping”) for an N-channel MOSFET or between N and N+ (“N* doping”) in a P-channel MOSFET.” Paper No. 7 (Prelim. Resp.), 4-8. In the Board’s institution decision, the Board “preliminarily determine[d] that the phrase ‘lateral contact layer’ does not require ‘a dopant concentration between P and P+ (P* doping) for an N-channel MOSFET or between N and N+ (N* doping) in a P-channel MOSFET.’” Paper No. 13, 12-13. It also “preliminarily determine[d] that the phrase ‘lateral contact layer’ does not require ‘a region of dopant which is implanted into sidewalls of the source contact trenches.’” *Id.* Notably, the Board suggested that Patent Owner’s construction was improperly reading limitations into the claim from the specification (*id.*, 9), and indicated that the appropriate role of the specification was to provide “controlling definitions or context necessary to avoid ambiguities.” *Id.*

Patent Owner submits that the Board’s institution decision applies a claim construction standard that unduly restricts the role of the specification. In particular, in an IPR, the Board “us[es] the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. 282(b).” 37 C.F.R. §

42.100(b). The Federal Circuit’s canonical *en banc Phillips* decision sets forth that standard. *Phillips* provides that “[b]ecause the meaning of a claim term as understood by persons of skill in the art is often not immediately apparent, and because patentees frequently use terms idiosyncratically,” it is appropriate to look to various sources, including “the words of the claims themselves, the remainder of the specification, the prosecution history, and extrinsic evidence concerning relevant scientific principles, the meaning of technical terms, and the state of the art.” *Phillips v. AWH Corp.*, 415 F.3d 1303, 1314 (Fed. Cir. 2005).

In particular, the “claims ‘must be read in view of the specification, of which they are a part’”, as “the specification ‘is always highly relevant to the claim construction analysis” and “[u]sually, it is dispositive; it is the single best guide to the meaning of a disputed term.” *Id.*, 1315. *Phillips* specifically disapproved of prior decisions that had narrowly limited the role of the specification to “determining whether the specification excludes one of the meanings derived from the dictionary,” via “an explicit definition of the term different from its ordinary meaning,” or where the inventor “has disavowed or disclaimed scope of coverage, by using words or expressions of manifest exclusion or restriction, representing a clear disavowal of claim scope.” *Id.*, 1319. *Phillips* also specifically disapproved of “requiring that any definition of claim language in the specification be express.” *Id.*, 1321.

Further, the District Court in *Force MOS Technology Co., Ltd. v. ASUSTeK Computer, Inc.*, No. 2:22-cv-00460-JRG (E.D. Tex.) adopted the same construction of “lateral contact layer” that Force MOS proposes here. Ex. 2011, 49-50. Notably, in that proceeding, ASUSTeK Computer (the real-party-in-interest in this IPR), proposed that the term be construed as “requiring a region of dopant which is implanted into sidewalls of the source contact trenches, wherein implantation may occur before or after the source contact trenches are etched, the region to have a doping concentration between the base layer doping concentration and the base contact layer doping concentration.” Ex. 2011, 47. The Court’s opinion in the *ASUSTeK* case was in part based on Patent Owner’s submission of such construction in its preliminary response in this IPR. *Id.* 49. However, the Court also stated that it “agree[d] that the specification discloses implanting a P*-type lateral contact layer into the sidewall of the source contact trenches, where P* has more doping than the P base layer, but less doping than the P+ base contact layer which is located at the bottom of the source contact trench.” *Id.*, 48-49 (citing ’634 Patent, 2:1-11). Thus, the *ASUSTeK* decision confirms that it is appropriate to refer to the specification in construing “lateral contact layer.”

1. An express construction of “lateral contact layer” is necessary, as it is a coined term whose meaning can only be determined from the specification

An express claim construction of “lateral contact layer” is especially important because of the vague and inconsistent application of that term by Petitioner and its expert, who have advanced no express construction of that term. In particular, Petitioner’s expert concludes that Hirler disclosed a lateral contact layer because “the purpose of the body amplification zone is the same as the lateral contact layer—i.e., to achieve the intended avalanche breakdown voltage capability, without it being degraded through the turning on the of NPN parasitic bipolar transistor.” Ex. 1003 ¶73. As to Shiraishi, Petitioner’s expert opines that a “POSITA would understand that this [Shiraishi’s layer 14] acts as a lateral contact layer to prevent punch-through.” Ex. 1003 ¶107. But, neither of those discussions have any apparent relevance to the words of the phrase “lateral contact layer,” and instead appear to assume an entirely functional scope for “lateral contact layer.” Ex. 2012 ¶79. Moreover, punch-through and avalanche breakdown are different phenomena. Ex. 2012 ¶¶79, 160; Ex. 2031.

The relevant starting point to the claim construction analysis is whether the term “lateral contact layer” has an established ordinary meaning in the field. As Dr. Neikirk explains, “lateral contact layer” has no established meaning in the field, and instead is a coined term used by the patentee to refer to the invention of the

specification. Ex. 2012 ¶83. In particular, neither expert has previously heard the term “lateral contact layer” in the relevant field. *Id.*; Ex. 2014, 26:11-21. Nor does the term appear in relevant technical dictionaries or glossaries. Ex. 2012 ¶83 (citing Ex. 2016, 145-146). An articles search for “‘lateral contact layer’ MOSFET” in Google Scholar only returns only a single article, from well after the issuance of the ’634 Patent. That article also indicates their use of “lateral contact layer” as a coined term with a different meaning. Ex. 2012 ¶83; Ex. 2018 (referring to a layer that is planar and underneath another layer and a pair of ohmic contacts, i.e. a layer “extending from side to side”).

Because “lateral contact layer” is a coined term—i.e., a term lacking any plain or established meaning—under post-*Phillips* Federal Circuit precedent, its meaning should be interpreted based on the disclosures of the specification. *See Intervet Inc. v. Merial Ltd.*, 617 F.3d 1282, 1287 (Fed. Cir. 2010) (“[T]erms coined by the inventor are best understood by reference to the specification.”); *Indacon, Inc. v. Facebook, Inc.*, 824 F.3d 1352, 1357 (Fed. Cir. 2016) (“terms [that] have no plain or established meaning to one of ordinary skill in the art ... ordinarily cannot be construed broader than the disclosure in the specification”); *Iridescent Networks, Inc. v. AT&T Mobility, LLC*, 933 F.3d 1345, 1351 (Fed. Cir. 2019) (where term is a “coined term,” appropriate to “look first to the specification, followed by the

prosecution history, to determine the meaning of the term.”); *see also Irdeto Access, Inc. v. Echostar Satellite Corp.*, 383 F.3d 1295, 1300 (Fed. Cir. 2004).

Moreover, although Patent Owner does not believe the role of the specification is limited to explaining ambiguities, there are a number of potential ambiguities regarding “lateral contact layer” that would be apparent to a POSITA if they only considered the claim itself rather than the specification. One such ambiguity is the term “lateral” itself. For example, in semiconductors, “lateral” can refer to a structure that extends from one side of the device to another. Ex. 2012 ¶83 (citing Ex. 2018, 54; Ex. 2019). “Lateral” can also mean “of or relating to the side” or “situated on, directed toward, or coming from the side.” Ex. 2012 ¶¶83, 86 (citing Ex. 2019). Rather than the location of a structure, “lateral” in semiconductors can refer to having a lateral side-to-side current flow. Ex. 2013 ¶86 (citing Ex. 2016, 146).

A POSITA only considering the claim itself (rather than the specification) would also observe potential ambiguities regarding the word “contact.” In particular, in semiconductors, “contact” can refer to the state of physical contact. Ex. 2012 ¶87 (citing Ex. 2021). It can also refer to the state of electrical contact, such as ohmic contact or non-ohmic contact. *Id.* (citing Ex. 2016, 180). In addition to a state or condition, “contact” can refer structures (e.g. an “ohmic contact” can refer to a structure that has the condition of ohmic contact). *Id.* Additionally, there

are distinct metal structures called contacts, which are used to electrically interface parts of a semiconductor with a metal interconnect layer. *Id.* (citing '634 Patent, Title, Abstract, Figs. 1 (element 111), 2G (element 211), Ex. 2022).

Thus, a POSITA attempting to understand the meaning “lateral contact layer” in claim 1 without reference to the specification might recognize “contact” as referring to the metal contacts within the source contact trenches—suggesting the “lateral contact layer” fills those trenches, i.e., that it is part of the contact and covers the sidewalls of the source contact trench by filling the inside of those trenches. Ex. 2012 ¶88. Or, “lateral contact layer” could refer to a layer *contacting* the trenched source contacts. Or “contact” could also refer to the function of improving electrical contact. *Id.*

The term “layer” in “lateral contact layer” could also have potential ambiguities if a POSITA ignored the specification. Indeed, one common meaning of “layer” in semiconductors refers to a portion of a semiconductor device constituting a distinct material that has been deposited together as part of a single step in the semiconductor process, or resulting from a distinct process is applied across the surface of a semiconductor, and may be on top of or underneath other layers. Ex. 2012 ¶89 (citing Ex. 2023, Ex. 2024, 3:42-5:8). Such layers typically extend from side-to-side in a wafer, unless interrupted by other structures. *Id.*

Layer can also refer to a portion of the semiconductor formed during a particular step of the process, even if not deposited, such as a layer created by ion implantation. Ex. 2012 ¶¶90-91 (citing Ex. 2007, Ex. 1008, [0058]). Limitation 1[a] of claim 1 recites specific layers—“epitaxial layer,” “base layer,” the “source layer”—disposed on top of each other in order. But, the “lateral contact layer” is not recited in limitation 1[a]. Instead, it is mentioned in limitation 1.[g], and is recited as being located along or within another layer (i.e., the base layer).

Because claim 1 is an apparatus claim, a POSITA would expect certain structural properties to be reflected in the “lateral contact layer” such as to distinguish it from the other recited regions and layers in the claim. *See PPC Broadband, Inc. v. Corning Optical Commc'ns RF, LLC*, 815 F.3d 747, 752-53 (Fed. Cir. 2016) (different terms presumed to have different meanings). For example, based on the structure of the claim, the “base layer” occupies at least some of the same vertical depth as the “lateral contact layer.” ’634 Patent, cl. 1 (“sidewalls of said trenches *in said base layer* are covered by the lateral contact layer”). Thus, there must be some structural difference between the “lateral contact layer” and the “base layer” to disambiguate the two terms’ scopes and respect the patentee’s intentional choice to recite different terms. However, claim 1 provides no guidance what those differences are. Ex. 2012 ¶92. Similarly, a construction is needed to distinguish the “lateral contact layer” from the “base contact layer.” Both are recited

in claim 1 as being adjacent to the source contact trench. However, as they are different terms, they are presumed to have different meanings. Indeed, the patentee could easily have instead recited that the source contact trenches in the base layer are covered by a contact layer, but the text of the claim itself provides no clue regarding *how* the scope and meaning of lateral contact layer is different from the base contact layer. Relatedly, an express construction is needed to distinguish the admitted prior art of Fig. 1 of the '634 Patent, which depicts a base contact layer (108) and a base layer (105) adjacent to the sidewalls of the source contact trench. Ex. 2012 ¶93; '634 Patent, Fig. 1, 1:18-41.

2. “lateral contact layer” requires P* doping

The specification supports Patent Owner’s construction requiring P* doping. The '634 Patent’s “Summary of the Invention” describes a configuration of differently doped zones in a MOSFET of “the present invention” where the lateral contact layer is a doped region having a dopant concentration between P and P+:

According to the **present invention**, the silicon substrate, the epitaxial layer, and the source layer are N-type; the base layer and ***lateral contact layer P**** are P-type; and each of the source contact trenches further has a P+-type base contact layer at a bottom thereof and ***the lateral contact layer P* has less doping concentration than the P+ base contact layer at the source contact trench but higher doping concentration than P-base layer*** to achieve ohmic contact between the ***P*-type region, which is lower doping concentration than P+-type region***, and the

contact metal plug while threshold voltage V_{th} is not significantly affected by P*-type region

'634 Patent, 2:1-11 (emphasis added). Under Federal Circuit precedent, the use of the phrase “the present invention” creates a strong presumption of definitional language. *Verizon Servs. Corp. v. Vonage Holdings Corp.*, 503 F.3d 1295, 1308 (Fed. Cir. 2007) (“When a patent ... describes the features of the ‘present invention’ as a whole, this description functions as a disclaimer that limits the scope of the invention.”).

Moreover, the specification repeatedly and consistently refers to the layer contact layer as having P* doping, indicating that is required by the invention as a whole. '634 Patent, 3:55-61 (an “implantation procedure ... [is] carried out to form a P*-type lateral contact layer (209) at the sidewall of the source contact trench (224)”), 4:3-6 (“the P+-type base contact layer (208) has [a] higher doping concentration of BF₂ (boron fluoride) than the P*-type lateral contact layer (209).”). The figures also support that the lateral contact layer has P* doping— Figure 3B depicts region 209 as a P* doped region, which is distinct from the P-doped region 205 and the P+ doped region 208. *Id.*, Fig. 3B; *see also id.*, Fig. 2G. The fact that the lateral contact layer is defined by the P* doping concentration of the specification is also strongly inferred from claims 2 and 6 which recite “the lateral contact layer has less doping concentration than the base contact layer at bottom.” Ex. 2012 ¶97.

Those claims would make little sense unless “lateral contact layer” was a region defined by its doping concentration, but claim 1 provides no such clue.

The foregoing described doping configurations are focused on the example of an “N-channel MOSFET structure,” but the specification expressly provides that “by inverting the conductive type”—i.e. switching each P-type doping to N-type doping and vice-versa—“this invention is also applicable to a P-channel MOSFET structure.” *Id.*, 2:16-19, 4:47-50; *see* Ex. 1003 ¶¶85, 94 (discussing inverting conductive types). Thus, in a P-channel MOSFET, the lateral contact layer would have N* doping, i.e., a level of doping between N+ and N doping. *Id.*; *see* Pet., 65 (in annotated figure, acknowledging that a lateral contact layer in “p-channel MOSFET” would have “N* type” doping).

In the Board’s decision on institution, the Board concluded that a construction of lateral contact layer requiring P* doping would violate the doctrine against claim differentiation. In particular, the Board held that it would “render redundant dependent claims 2 and 6.” Paper No. 11, 11-12. However, “claim differentiation is a rebuttable presumption that may be overcome by a contrary construction dictated by the written description or prosecution history.” *Howmedica Osteonics Corp. v. Zimmer, Inc.*, 822 F.3d 1312, 1323 (Fed. Cir. 2016) (presumption overcome where “written description reveals only instances in which the claim language is satisfied

by” criteria of narrow construction); *Polymer Techs., Inc. v. HemCon, Inc.*, 672 F.3d 1350, 1358-59 (Fed. Cir. 2012) (en banc) (construction supported by specification);

Moreover, Patent Owner’s proposed construction would not render claims 2 and 6 redundant of claim 1. In particular, each of claim 2 and 6 recite limitations not required by claim 1 under Patent Owner’s construction. Claim 2 recites “the silicon substrate, the epitaxial layer, and the source layer are N-type; the base layer and lateral contact layer are P-type; and each of the source contact trenches further has a P-type base contact layer at a bottom thereof.” That is, claim 2 recites that the trenched MOSFET of claim 1 is an N-type (or N-channel) MOSFET. Ex. 2012 ¶96. Similarly, claim 6 recites, “the silicon substrate, the epitaxial layer, and the source layer are P-type; the base layer and lateral contact layer are N-type; and each of the source contact trenches further has a N-type base contact layer at a bottom thereof.” That is, claim 6 recites that the trenched MOSFET of claim 1 is a P-type (or P-channel) MOSFET. *Id.*

However, even under Patent Owner’s construction of “lateral contact layer,” the MOSFET of claim 1 can be a P-type *or* an N-type MOSFET. Thus, Patent Owner’s P* construction would not render claims 2 and 6 redundant. *Apple, Inc. v. Ameranth, Inc.*, 842 F.3d 1229, 1238 (Fed. Cir. 2016) (Federal Circuit “has declined to apply the doctrine of claim differentiation where the claims are not otherwise *identical* in scope.”) (emphasis added). Moreover, Patent Owner’s construction

would not necessarily render claim 2 and 6's recitation of "the lateral contact layer has less doping concentration than the base contact layer at bottom" to be redundant either. In particular, Patent Owner's construction of "lateral contact layer" does not necessarily require that the *base* contact layer have any particular doping concentration, only that the lateral contact layer has P* doping. Ex. 2012 ¶98.

3. "lateral contact layer" requires implantation into the sidewalls of an existent source contact trench

Additionally, the specification makes clear that the lateral contact layer is implanted into the sidewall of then-existing the source contact trenches. As Figures 2D and 2E of the '634 Patent demonstrate, the source contact trench 224 is first etched, and then the lateral contact layer is implanted into the sidewalls. '634 Patent, Figs. 2D, 2E, 3:41-61. Indeed, the '634 Patent explains that "FIGS. 3A and 3B are schematic sectional views for describing *ion implantation into a source contact trench of the present invention.*" *Id.*, 2:46-48 (emphasis added); *see also* Ex. 2001 (Liu Depo.), 44:21-24. Moreover, the detailed description explains that an "*implantation procedure ... [is] carried out to form a P*-type lateral contact layer (209) at the sidewall of the source contact trench.*" '634 Patent, 3:56-60 (emphasis added). The consistent and repeated description of the lateral contact layer being created by implantation into an existent source contact trench supports Patent Owner's construction. *See Nystrom v. TREX Co., Inc.*, 424 F.3d 1136, 1143(Fed.

Cir. 2005); *Phillips*, 415 F.3d at 1321 (“a claim term may be clearly redefined without an explicit statement of redefinition”) (quotation omitted).

In the decision on institution, the Board suggested that this would be reading in limitations from the specification. However, the words of the claim itself support Patent Owner’s construction. In particular, the claim recites both the term “region” and “layer” to refer to different structures in the MOSFET. ’634 Patent, cl. 1 (“drain region,” “body region,” “source region,” semiconductor region,” “lateral contact layer,” “base layer,” etc.). The use of different words indicate the terms have different meanings. *PPC Broadband*, 815 F.3d at 752-53. That is, a POSITA would presume that the “lateral contact *layer*” is not simply a “region” adjacent to the source contact trench. Ex. 2012 ¶120.

Thus, a POSITA would thus be motivated to look to meanings of “layer” that distinguish the “lateral contact *layer*” from a “region.” One such meaning is a “thin sheet of a substance.” Ex. 2025. This is consistent with the depiction of the lateral contact layer in the ’634 Patent, which depicts the lateral contact layer as being a relatively thin layer, spread over the source contact trench walls. ’634 Patent, Fig. 2G; *see also* Fig. 3B. This definition of layer—and the fact that the lateral contact layer is not merely a region present at the sidewalls—also informs the meaning of “covered.” In particular, it suggests that the “thin sheet” is “spread over” the sidewalls. Ex. 2012 ¶120 (citing Ex. 2029). However, as Dr. Neikirk explains, a

“thin sheet” cannot be “spread over” something that does not yet exist (i.e. sidewalls that have not yet been etched). *Id.* Moreover, as discussed in further detail below in connection with Petitioner’s grounds versus limitation 1[g], this is not a merely a manufacturing process detail, implanting dopant into the sidewalls of an existent source contact trench results in a structurally different device as opposed to devices where a region is doped before a trench is etched. *See infra* VI.A.2.b.1, VI.C.1.b.2.

Thus, the Board should construe “lateral contact layer” as “a region of dopant which is implanted into sidewalls of the source contact trenches to have a dopant concentration between P and P+ (‘P* doping’) for an N-channel MOSFET or between N and N+ (‘N* doping’) in a P-channel MOSFET.”

B. “the sidewalls of said trenches in said base layer are covered”

In the Petition, Petitioner, based on the prosecution history of the ’634 Patent, proposed that this term be construed as “the entire sidewalls of the said trenches in said base layer.” Pet., 18-19. Since then, two District Courts have likewise adopted the same construction as proposed by Petitioner. Ex. 2010, 6-9; Ex. 2011, 23. Accordingly, for the purpose of this proceeding, Patent Owner will apply Petitioner’s proposed construction. Moreover, an express construction of this term is necessary because, as discussed below, the structure that Petitioner identifies in Shiraishi as the “lateral contact layer” does not cover the *entire* sidewalls of the source contact trenches in the base layer. Ex. 2012 ¶102; *infra* VI.C.1.b.1.

**VI. PETITIONER HAS FAILED TO DEMONSTRATE THAT ANY
CHALLENGED CLAIM IS UNPATENTABLE**

A. Ground 1: Hirler Fails to Anticipate the Challenged Claims

1. Claim 1

**(a) 1[a]: Hirler Fails to Disclose an “*epitaxial* layer
corresponding to said drain region”**

Limitation 1[a] recites, *inter alia*, “an epitaxial layer corresponding to said drain region disposed on the top of said silicon substrate.” ’634 Patent, cl. 1. In addressing this limitation, the Petition merely quotes Hirler’s statement that “[t]he starting point is an n+ substrate 10 of silicon, an n- drift zone 11, p-body zone areas 12 as well as n+ source zone areas 13” and provides an annotated version of Hirler’s Fig. 2F, identifying the drain region as including layers 11 and 10. Pet., 23-24. Petitioner’s expert opines that Hirler’s “‘n- drift zone 11’ corresponds with ‘an epitaxial layer corresponding with a drain region.’” Ex. 1003 ¶66. However, neither the Petition nor Dr. Liu provide any explanation for *why* they believe that Hirler discloses an *epitaxial* layer corresponding to a drain region, or why n- drift zone 11 is an *epitaxial* layer. Indeed, Hirler itself does not use the word “epitaxial” or any variation of that word. Ex. 1005; Ex. 2012 ¶110.

An epitaxial layer is a semiconductor layer created via the process of epitaxy. Ex. 2012 ¶109 (citing Ex. 2016, 85 (“**epitaxial layer** a layer grown as a result of epitaxial deposition, or epitaxy ... **epitaxy** an ‘ordered deposition’; a process by

which thin layer of single crystal material is deposited on single-crystal substrate.”). Thus, to prove that Hirler anticipates this limitation, Petitioner is required to show that Hirler expressly discloses the recited “epitaxial layer corresponding with a drain region,” or that it is inherent in Hirler’s disclosure. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631 (Fed. Cir. 1987).

Hirler plainly does not expressly disclose an epitaxial layer corresponding with a drain region. Nowhere in Hirler is there a mention of “epitaxial,” “epitaxis,” or similar words. Ex. 2012 ¶110; Ex. 1006. Indeed, Hirler does not contain any description of how the “n- drift zone” was created. Rather, Hirler expressly states that its “starting point” has “an n+ substrate 10 of silicon [and] an n- drift zone 11.” Ex. 1006, [1018]. Hirler only discusses the details of fabrication *after* that starting point. Ex. 2012 ¶110.

Moreover, neither Petitioner nor its expert provides any explanation or analysis why a person of ordinary skill in the art would understand Hirler’s n- drift zone 11 is inherently or necessarily created by epitaxy (i.e., grown on top of an existing semiconductor wafer). Pet., 23-24; Ex. 1003 ¶66; Ex. 2012 ¶109. Similarly, the petition provides no explanation for why it contends that Hirler’s “n- drift zone 11” is necessarily an epitaxial layer. Pet., 23-24.

During Dr. Liu’s deposition, when first asked about Hirler’s disclosure of an *epitaxial* layer, he did not provide any explanation for his conclusions, and instead

argued that an epitaxial layer is obvious. Ex. 2014, 47:8-48:12. Of course, such an argument cannot sustain an anticipation ground. Nor can it sustain any obviousness grounds based on Hirler, as the Petition articulates no motivation to modify Hirler nor to combine it with another reference so as to use an epitaxial layer.

However, during redirect by Petitioner's counsel, Dr. Liu, for the first time, attempted to advance an inherency argument for this limitation. *Id.*, 164:16-165:20. The Board should not accept such late disclosed argument, as any inherency argument should be clearly disclosed in the Petition and Petitioner's expert's declaration. 37 C.F.R. § 42.104(b)(4), (5); *Spansion Inc., v. Macronix International Co., Ltd.*, IPR2014-01116, Paper 12, 9-10 (P.T.A.B. Dec. 22, 2014) (Petitioner must disclose factual basis for inherency argument in petition and accompanying evidence); *CommScope Inc. v. TQ Delta, LLC*, IPR2022-00809, Paper 31, 28 (P.T.A.B. Nov. 13, 2023) (holding that the Board will not consider an inherency argument not raised in Petition); *Cisco Systems, Inc. v. Capella Photonics, Inc.*, IPR2014-01276, Paper 40, 36 n.14 (P.T.A.B. Feb. 17, 2016).

Even if the Board were inclined to address Dr. Liu's tardy inherency theory, it also fails on the merits. "A party must ... meet a high standard in order to rely on inherency... the limitation at issue necessarily must be present, or the natural result of the combination of elements explicitly disclosed by the prior art." *PAR Pharmaceutical, Inc. v. TWI Pharmaceuticals, Inc.*, 773 F.3d 1186, 1195–1196 (Fed.

Cir. 2014). At his deposition, Dr. Liu argued that it would be impossible to create Hirler's more lightly doped n- drift zone layer on top of its more heavily doped n+ substrate layer other than via epitaxy. Ex. 2014 (Liu Depo.), 164:16-165:20. However, there are a number of ways that the configuration of an n- doped drift zone on top of an n+ substrate could have been created without epitaxial growth.

For example, Hirler's n- layer could be created by counter-doping the top portion of the more heavily doped n+ layer. Ex. 2012, ¶113. When asked about counter-doping at his deposition, Dr. Liu did not explain that Hirler *could not* have created the n- and n+ layers via counter doping, but rather that "it's not done" because it has disadvantageous mobility. Ex. 2014, 166:15-8. But that is not adequate to show inherency.

Alternatively, one could create Hirler's n- and n+ layers by starting with an n-doped substrate and creating the more heavily doped n+ portion of that substrate via back-side doping. Ex. 2012 ¶114. When asked about back-side doping at his deposition, Dr. Liu could not articulate any reason why back-side doping could not have created Hirler's arrangement of an n- layer on top of an n+ layer. Ex. 2014, 167:24-169:15.

Because Hirler does not expressly or inherently disclose an "*epitaxial* layer corresponding to said drain region," Petitioner's anticipation argument over Hirler fails.

(b) 1[g]: Hirler Fails to Disclose “the sidewalls of said trenches in said base layer are covered by the lateral contact layer”

As discussed above, the appropriate construction of the term “lateral contact layer” requires a region of dopant which is implanted into sidewalls of the source contact trenches to have a dopant concentration between P and P+ (“P* doping”) for an N-channel MOSFET or between N and N+ (“N* doping”) in a P-channel MOSFET. *Supra*, V.A.2. In Ground 1, Petitioner identifies this limitation as being satisfied by Hirler’s “body amplification zones” (19), it provides little explanation of that contention. Pet., 22, 26.

The petition itself merely notes that “body amplification zones” (19) is implanted and formed along the sidewalls of the contact trench that is in the base layer. Pet., 26. Petitioners’ expert merely adds that “the body amplification zone [is] located in the same position along the sidewalls of the contact trench” and “the purpose of the body amplification zone is the same as the lateral contact layer—i.e., to achieve the intended avalanche breakdown voltage capability, without it being degraded through the turning on the of NPN parasitic bipolar transistor.” Ex. 1003 ¶73.

But, the “lateral contact layer” is required to be on the source contact trench’s sidewalls by the language “the sidewalls of said trenches in said base layer are covered by the lateral contact layer.” Thus, the fact that Hirler has something located

in the same place does not make that something a “lateral contact layer” (otherwise the term “lateral contact layer” would be mere surplusage in the claim). And simply saying that Hirler’s body amplification zone “achieve[s] the intended avalanche breakdown voltage capability, without it being degraded through the turning on the of NPN parasitic bipolar transistor” is entirely functional. Many different structures can perform the same function, but that does not mean they satisfy a structural limitation that performs the same function—a structural limitation requires that the same structure appear in the prior art. Thus, the arguments in the Petition fail to give any meaningful explanation as to why Petitioner contends Hirler satisfies the “lateral contact layer” limitation.

For that reason alone, the Board should hold Petitioners have failed to meet their burden as to the Hirler ground—the rules require a Petitioner to disclose “how the challenged claim is to be construed,” “how the construed claim is unpatentable,” and “the relevance of the evidence to the challenged raised.” 37 C.F.R. § 42.104(b)(3)-(5). Petitioner’s cursory arguments fail even that low threshold.

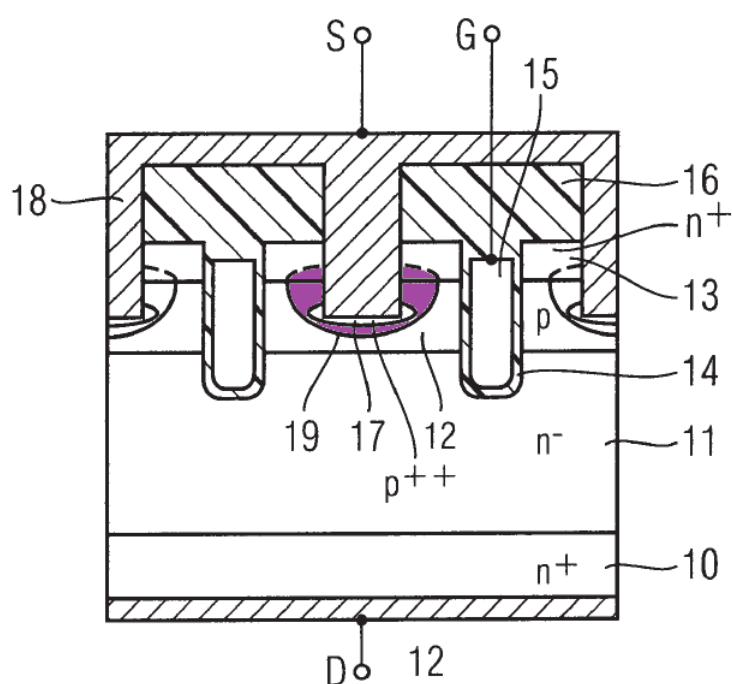
Additionally, Hirler’s “body amplification zone (19)” cannot satisfy the “lateral contact layer” for at least three reasons, and therefore Hirler cannot anticipate claim 1.

(1) Hirler’s “body amplification zone” is not implanted into the sidewalls of a source contact trench

First, Hirler’s “body amplification zone” is not a region of dopant resulting from implantation *into the sidewalls* of source contact trenches, as required by the proper construction of “lateral contact layer” (discussed above). Instead, Hirler’s “body amplification zone (19)” is implanted into the semiconductor material *before* the source contact trench or its sidewalls even exist. Ex. 2012, ¶119; Ex. 1006, [0012], [0034], Figs. 2C, 2D.

Moreover, Hirler fails to disclose limitation 1[g] even if the Board rejects Patent Owner’s proposed construction of “lateral contract layer” and instead adopts a plain and ordinary meaning construction. In particular, the claim recites that the “sidewalls of said trenches in said base layer are *covered* by the lateral *contact layer*.” As Dr. Neikirk explains, in context, “a POSITA would understand ‘cover[ed]’ as indicating more than simply any ‘region’ ‘being present ‘at’ the sidewalls, since that would fail to distinguish the base layer” (which, per the claim language, necessarily overlaps the same vertical depth range as the lateral contact layer). “Rather, a POSITA would understand ‘covered by the lateral contact layer’ as being consistent with a ‘thin sheet’ being ‘spread over’ the sidewalls.” Ex. 2012 ¶120; Ex. 2029, 2 (“cover ... 4 a: to spread over”); Ex. 2025 (“layer ... a thin sheet of substance”). As such, the side walls need to already exist at the time of the

creation of the lateral contact layer—a sheet cannot be spread over something that does not yet exist. Ex. 2012 ¶120. This is distinct from the broad implantation region of Hirler’s body amplification zones, which are implanted over a broad region of the semiconductor cell, prior to the source contact trenches being etched. Ex. 1006, [0030], Figs. 2C-2D; Ex. 2012 ¶119.



Ex. 1005 (Hirler), Ex. 2F (annotated)

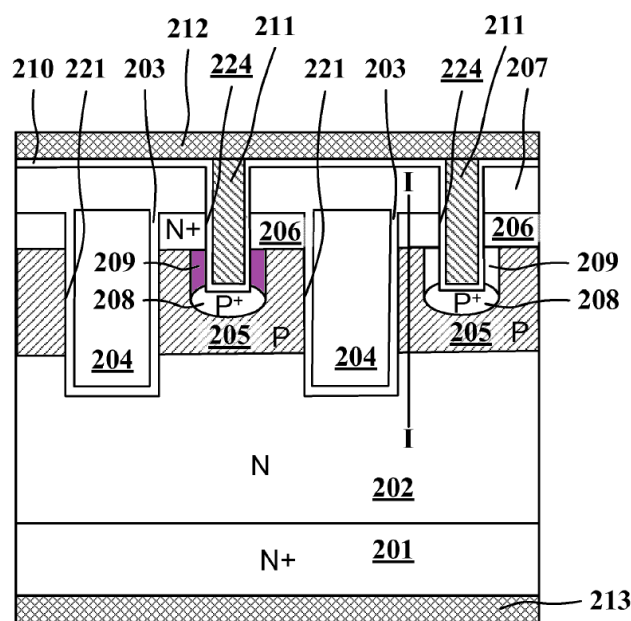


Fig. 2G

'634 Patent, Fig. 2G (annotated)

Indeed, these differences are more than mere variations in manufacturing processes—they reflect structurally different devices. As shown above in Figure 2F, Hirler’s body amplification zone 19 is a broadly diffused dopant **zone**, approaching the vicinity of the trench gates. Ex. 2012 ¶122; Ex. 1005, Fig. 2F; Ex. 1006, [0036] (mentioning that the body amplification zone’s “lateral extensions [can] reach the

vicinity of the channel in the area of the trench gates”). Such lateral extensions can increase threshold voltage, reducing the ability to improve cell density, exactly the situation the ’634 Patent tries to prevent. Ex. 2012 ¶122 (citing ’634 Patent, 2:10-11, 5:12-16, 5:27-29, Figs. 2G, 4). By contrast, the ’634 Patent’s lateral *contact layer* 209 is depicted as a thin layer—penetrating only slightly beyond the surface of the source contact’s sidewalls. ’634 Patent, Fig. 2G.

Thus, because Hirler’s body amplification zone is implanted into the semiconductor material *before* the source contact trench’s sidewalls exist, Hirler fails to disclose a lateral contact layer.

(2) Hirler’s “body amplification zone” does not have P* doping

Second, Hirler does not disclose that its body amplification zone 19 has P* doping.¹ As discussed above, as properly construed, “lateral contact layer” requires P* doping for N-channel MOSFETs (such as Hirler), which is a doping concentration between conventional P and P+ doping.

By contrast, Hirler consistently describes its “body amplification zone (19)” as having a “P+” level of doping concentration. Ex. 1006, [0030]; Ex. 1005, Figs.

¹ The P* portion of Force MOS’s construction (as opposed to the N* portion) is applicable to Hirler because Hirler is an N-channel MOSFET. Ex. 2012 ¶118, n.3; Ex. 1003 ¶75.

2C-2D. Plainly, P⁺ doping is not between P and P⁺. Ex. 2012 ¶123. Indeed, Petitioner has already admitted that P* is less heavily doped than P⁺ doping. Pet., 7; Ex. 1003 ¶29 (“Doping concentration P* is doped more heavily than P but less than P⁺.”).

Thus, because Hirler’s body amplification zone has P⁺ doping rather than P* doping, Hirler fails to disclose a lateral contact layer.

(3) Hirler does not necessarily disclose that its “body amplification zone” covers the *entire* sidewalls of the source contact trench

Lastly, Hirler fails to satisfy Petitioner’s construction of “the sidewalls of said trenches in said base layer are covered,” which requires that the lateral contact layer cover the “entire” sidewalls of the source contact trench in the base layer. Indeed, neither Petitioner nor its expert make any attempt to address whether Hirler’s body amplification zones satisfy their own construction requiring “entire” coverage. Pet., ¶124; Ex. 1003 ¶73.

Moreover, Hirler’s disclosures indicate that its body amplification zones do not necessarily cover the entire sidewalls of the source contact trenches. Ex. 2012 ¶124. This is demonstrated by Hirler’s disclosures that “the depth of the body reinforcement zones 19 ... can be controlled” and is “practically **not adjacent to the surface**” and that “the contact trench is etched so deep that it is driven into the body amplification zone 19.” *Id.*; Ex. 1006 (Hirler), [0030], [0035]. These disclosures

indicate that Hirler's body amplification zone is not practically adjacent to the surface (i.e. immediately below the source layer), but at some further depth. Moreover, Hirler's p-doped body amplification zone 19 is created by doping *through* an already n-doped source layer. Ex. 1006, [0030]; Ex. 1005, Fig. 2C. This would necessarily result in *some* degree of counter-doping of the source layer. Ex. 2012 ¶124.

Based on these disclosures, a POSITA would understand that, between the bottom of the N-doped source layer (where the N doping concentration would be the lowest) and the top of the P-doped body amplification zone 19, there would be a region of no net dopant. *Id.* And Hirler does not provide enough details to determine whether this no net dopant region is thick enough to mean that portions of the sidewalls are not covered by the body amplification zone 19 in the base layer. *Id.* Moreover, the simplified figures of Hirler would not be sufficient to resolve the issues raised by Hirler's written disclosures. *Id.* Thus, a person of ordinary skill in the art would not understand Hirler as necessarily disclosing that the "body amplification zone 19" covers the entire sidewalls in the base layer.

2. Claims 2, 6

Claims 2 and 6 depend from claim 1. '634 Patent, cls. 2, 6. Petitioner's arguments in Ground 1 for alleged anticipation of claims 2 and 6 are based on Petitioner's anticipation arguments for Ground 1, claim 1, which fail as discussed

above. Pet., 27, 28; *supra*, VI.A.1. Thus, Petitioner has not demonstrated that claims 2 and 6 are anticipated. Ex. 1012 ¶125.

B. Ground 2: Hirler in view of Kobayashi and the Knowledge of a POSITA Fail to Render Obvious the Challenged Claims

1. Lack of Motivation to Combine

Petitioner argues that “POSITA would have been motivated to combine the barrier metal layer disclosed in Kobayashi to the MOSFET disclosed in Hirler” because “barrier metal layer ... would help to promote the adhesion of the tungsten contact plug expressly taught in Hirler to the contact area” and “prevent ... fluorine from the deposition process of W [tungsten]” from “seeping into the underlying silicon surface.” Pet., 33.

However, that motivation to combine analysis is flawed because Hirler does not solely disclose tungsten plugs for its source contact trenches. Indeed, Hirler’s primary embodiment fills the source contact trenches with aluminum—Hirler discloses polycrystalline silicon or tungsten as additional alternatives. Ex. 1006, [0022], [0023]; Ex. 2012 ¶129. But, the Petition’s motivation to combine analysis assumes, without explanation, that a POSITA would select Hirler’s tungsten embodiment, and on that basis, identifies the use of tungsten as a motivation to use a barrier layer. Pet., 33. However, that violates the prohibition against “the hindsight combination of components selectively culled from the prior art to fit the parameters of the patented invention.” *Cheese Sys., Inc. v. Tetra Park Cheese and Powder Sys.,*

Inc., 725 F.3d 1341, 1352 (Fed. Cir. 2013) (quoting *ATD Corp. v. Lydall, Inc.*, 159 F.3d 534, 546 (Fed.Cir.1998)). Part of the motivation to combine is the motivation “to select particular elements” among the prior art. *See ATD Corp.*, 159 F.3d at 546.

That failure is plainly fatal to Petitioner’s arguments for claims 4 and 8 (and dependent claims 5 and 9)—which specifically recite the use of “tungsten” for the plugs. Moreover, that failure is fatal to Petitioner’s argument for claims 3 and 5 because the use of “tungsten” is the basis for the Petition’s motivation to use a barrier layer. Indeed, a POSITA would not envisage a need for a barrier layer if Hirler’s aluminum or polycrystalline silicon embodiments were instead selected for combination (and certainly neither Petitioner nor its expert provide any motivation to use a barrier layer with non-tungsten source contacts). Ex. 2012 ¶¶129, 130. Nor would a POSITA automatically conclude that tungsten is the only plausible implementation of Hirler—Hirler’s aluminum embodiment source contact provides at least some benefits over the tungsten embodiment, i.e., a simpler manufacturing process. *Id.*

Unlike the petition itself, Petitioner’s expert declaration does identify a motivation to use tungsten—that “CVD tungsten process is able to conformally fill contact holes with a high aspect ratio and produce a planar top surface.” Ex. 1003 ¶91. However, the Board should not consider those arguments because they are not mentioned in the Petition—doing so would thus violate the rules against

incorporation by reference. 37 C.F.R. § 42.6(a)(3). However, even if the Board did consider those arguments, they also fail. In particular, Dr. Liu’s assertions of good planarization and conformal filling by tungsten are conclusory—he cites no supporting documents. Ex. 1003 ¶91. And, he does not even render a specific opinion that tungsten is *better* than Hirler’s aluminum or polysilicon embodiments with respect to those properties. *Id.* Even if they were not as good as tungsten at planarization, such good planarization could be readily achieved by the well-known technique of chemical mechanical planarization (CMP). Ex. 2012 ¶131. Moreover, Hirler’s polysilicon embodiment is plainly adequate to conformally fill Hirler’s source contact trenches, as polysilicon is equally capable of conformally filling similar trenches (e.g. gate trenches). Ex. 2012 ¶132; Ex. 1008, [0009].

Additionally, both Petitioner and its expert fail to address the significant differences in structure and purpose between the Hirler and Kobayashi references. In particular, the Hirler and Kobayashi references are diametrically opposed references that teach away from each other’s approach. Ex. 2012 ¶127. In particular, the primary goal of Hirler is to avoid having to “precisely defin[e] the depth of the body contact zone [i.e., the strongly doped implant at the bottom of source contact trenches].” *Id.*; Ex. 1005 (Hirler), [0007]. By contrast, the focus of Kobayashi is to do exactly that, i.e., to precisely define the depth of the base contact layer to ensure that it is at a depth different from the depth of peak dopant concentration in the base

layer. *Id.*, [0018]-[0019], [0025], Figs. 5A, 5B, 7C; Ex. 2012 ¶127. These contradictory disclosures are directly relevant to the proposed combination, as Petitioner proposes combining components of the structure of Kobayashi's source contact trenches with Hirler's source contact trenches.

Even if the Board determines these disclosures do not rise to "teaching away," these differences in structure and purpose still lead to a conclusion of non-obviousness. *See Rembrandt Wireless Tech., LP v. Samsung Elecs. Co. Ltd.*, 853 F.3d 1370, 1379-80 (Fed. Cir. 2017); *Apple Inc. v. Samsung Elecs. Co., Ltd.*, 839 F.3d 1034, 1051 n.15 (Fed. Cir. 2016) (en banc); *Arctic Cat v. Bombardier Recreational Products*, 876 F.3d 1350, 1360 (Fed. Cir. 2017). Accordingly, a POSITA would not be motivated to select those references for combination. *WBIP, LLC v. Kohler Co.*, 829 F.3d 1317, 1337 (Fed. Cir. 2016) ("Whether a skilled artisan would be motivated to make a combination includes whether he would select particular references in order to combine their elements.").

2. Claims 3-5, 7-9

Claims 3-5 and 7-9 all depend indirectly from claim 1. '634 Patent, cls. 3-5, 7-9. Petitioner's arguments in Ground 2 for alleged obviousness of claims 3-5 and 7-9 are based on Petitioner's arguments that Hirler anticipates claim 1, which fail as discussed above. Pet., 29-32 (citing to Ground 1). Petitioner offers no argument or evidence that Kobayashi cures any of the deficiencies of Hirler identified above with

respect to claim 1. That is, because Petitioner has failed to demonstrate that Hirler discloses each limitation of claim 1, Petitioner's obviousness arguments in Ground 2 for claims 3-5 and 7-9 fail for the same reasons discussed above for claim 1 in Ground 1. *See supra*, VI.A.1.

(a) “barrier metal layer and a plurality of contact metal plugs”

Additionally, claim 3 recites “a barrier metal layer and a plurality of contact metal plugs.” Claims 4-5 depend, directly or indirectly, from claim 3. Claim 7 recites “a barrier metal layer and a plurality of contact metal plugs.” Claims 8-9 depend, directly or indirectly, from claim 3. Thus, claims 3-5 and 7-9 all recite “a barrier metal layer and a plurality of contact metal plugs.”

As discussed above (*supra* VI.B.1), Petitioner fails to provide an adequate motivation to combine Hirler and Kobayashi to have “a barrier metal layer and a plurality of contact metal plugs,” which is recited in claims 3 and 7, from which claims 4-5 and 8-9 respectively depend. Nor do they provide an adequate motivation to use “tungsten” for the “contact metal plug,” as recited in claims 4 and 8. Accordingly, Petitioner's obviousness theory for claims 3-5 and 7-9 fails.

C. Ground 3: Shiraishi Fails to Anticipate the Challenged Claims

1. Claim 1

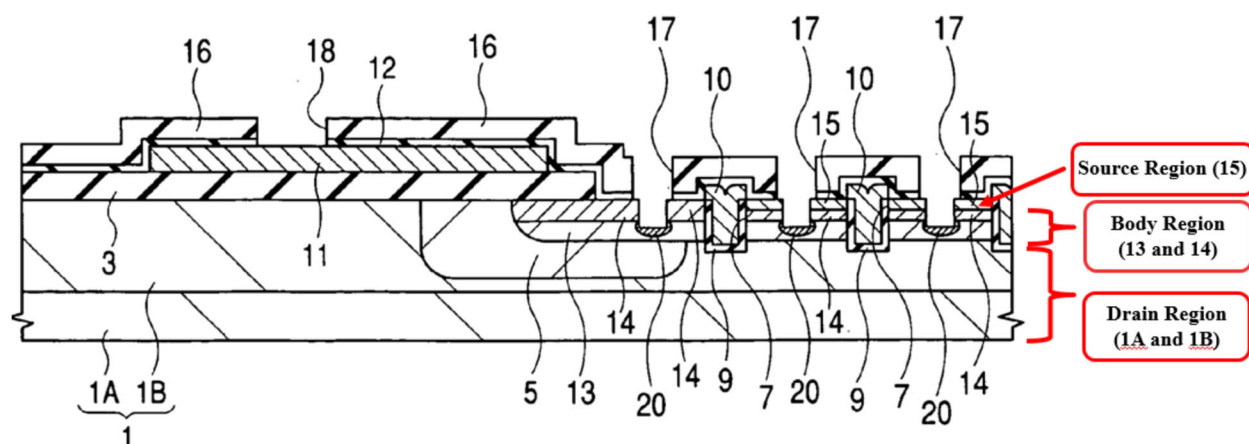
a) 1[a]: Shiraishi Fails to Disclose “a source layer corresponding to said source region disposed on the top of said base layer”

The Petition identifies the claimed epitaxial layer as corresponding to Shiraishi’s layer 1B and the source layer as corresponding to Shiraishi’s layer 15. Pet., 38. The Petition does not mention the “base layer,” but instead identifies Shiraishi’s layer 13 as corresponding to a “body layer,” which is not recited in the claim. *Id.* However, Petitioner’s expert’s declaration identifies Shiraishi’s layer 13 as corresponding to the claimed “base layer.” Ex. 1003 ¶100.²

Notably, this claim limitation requires a specific order of layers: a source layer disposed on top of a base layer, which is disposed on top of an epitaxial layer. However, this immediately runs into a problem with Petitioner’s theory: the location of layer 14 of Shiraishi.³ As Petitioner’s own figures show, layer 14 of Shiraishi interposes layer 13 (the alleged base layer) and source layer 15:

² Shiraishi also refers to layer 13 as the “second semiconductor layer” or “p⁻ type semiconductor region 13.” Ex. 1009, [0072].

³ Shiraishi also refers to layer 14 as the “fifth semiconductor layer” or “p-type semiconductor region 14.” Ex. 1009, [0073].



Pet., 38 (annotating Shiraishi’s Fig. 8); Ex. 1003 ¶98; *see also* Ex. 1009, [0073] (stating that “n+type semiconductor region [] 15” is formed “over the p-type semiconductor region 14”). Thus, according to Petitioner’s mapping of limitations, Shiraishi does not disclose a source layer corresponding to said source region *disposed on the top of said base layer*, because Shiraishi’s source layer 15 is instead disposed on the top of layer 14. Ex. 2012 ¶138.

Confusingly, Petitioner’s annotation of Shiraishi’s Fig. 8 identifies both layers 13 and 14 as the “body region,” despite the claim reciting a “base layer corresponding to said body region,” and despite Petitioner not identifying Shiraishi’s layer 14 as part of the claimed base layer. Pet., 38; Ex. 1003 ¶98. Because the claim recites the “base layer corresponding to said body region,” it is inconsistent with the claim’s text to identify both layers 13 and 14 of Shiraishi as the body region but to identify layer 13 alone as the “base layer.” Ex. 2012 ¶137.

Moreover, it would be inappropriate to include layer 14 as part of the body region or base layer because a POSITA would understand that the “body” region of

a MOSFET is the region where the channel is formed when the gate is in an “ON” state. Ex. 2012 ¶138. But, Shiraishi only identifies layer 13 (not layer 14) as being the “channel layer” or “acting as a base.” *Id.*; Ex. 1009 (Shiraishi), [0072]-[0073], [0080], [0084]. By contrast, layer 14 is identified in Shiraishi as a “punch-through stopper layer,” not a base layer, body region, or channel region. *Id.*; *id.*, [0073], [0081]. Thus, layer 14 of Shiraishi is not part of the body region or base layer. Indeed, neither Petitioner nor its expert provides any analysis to the contrary.

Thus, because Shiraishi’s layer 14 is disposed underneath the source layer, Shiraishi fails to disclose the specific structure of limitation 1[a], which requires “a source layer corresponding to said source region disposed on the top of said base layer.”

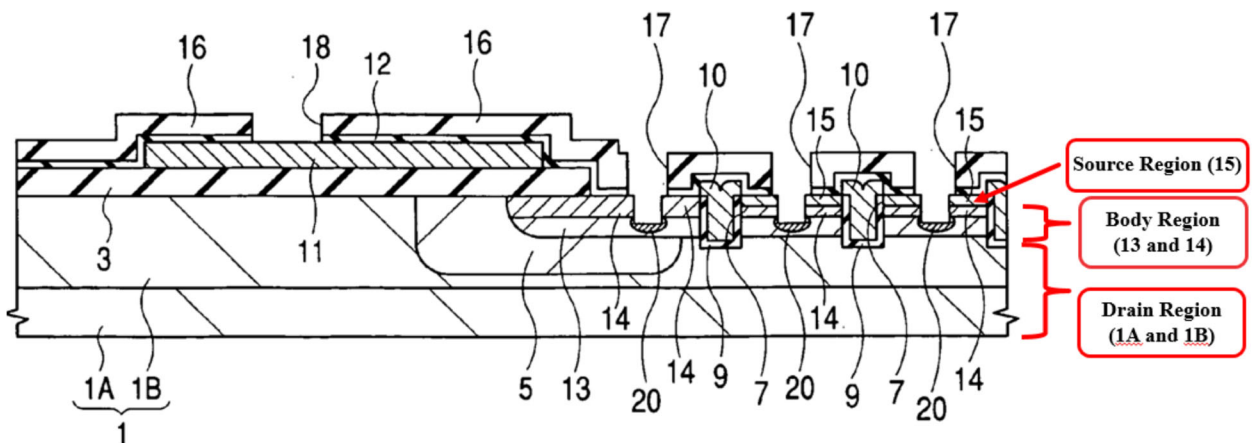
b) 1[g]: Shiraishi Fails to Disclose a “lateral contact layer” as Properly Construed

As discussed above, the appropriate construction of the term “lateral contact layer” requires a region of dopant which is implanted into sidewalls of the source contact trenches to have a dopant concentration between P and P+ (“P* doping”) for an N-channel MOSFET, or between N and N+ (“N* doping”) in a P-channel MOSFET. *Supra*, III.A. In Ground 3, Petitioner identifies this limitation as being satisfied by Shiraishi’s “additional semiconductor layer (14).” Pet., 40, Ex. 1003 ¶¶95, 107. However, Shiraishi’s “additional semiconductor layer (14)” cannot

satisfy the “lateral contact layer” limitation as properly construed for at least three reasons.

(1) Shiraishi’s layer 14 does not cover the sidewalls of the source contact trench in said base layer

As discussed in limitation 1[a], Petitioner solely identifies Shiraishi’s layer 13 as the claimed base layer. Pet., 48; Ex. 1003 ¶100. In limitation 1[g], Petitioner identifies Shiraishi’s layer 14 as the claimed “lateral contact layer.” However, Shiraishi’s layer 14 is disposed on top of layer 13, under source layer 15:



Pet., 38 (annotating Shiraishi’s Fig. 8); Ex. 1003 ¶98; *see also* Ex. 1009, [0073] (stating that “n+type semiconductor region [] 15” is formed “over the p-type semiconductor region 14”). Indeed, layer 14 is created on top of layer 14 by adding additional dopant to layer 13. Ex. 1009, [0073]. But, this arrangement creates an obvious problem: limitation 1[g] requires “the sidewalls of said trenches *in said base layer* are covered by the lateral contact layer.” ’634 Patent, cl. 1. Because

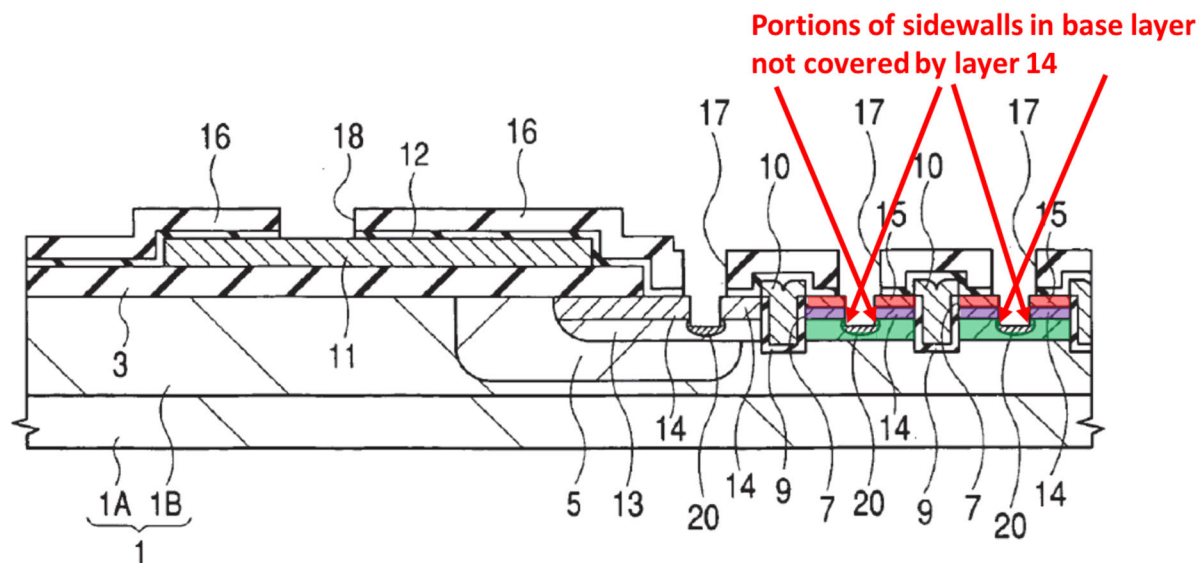
Shiraishi's layer 14 is located *above* the base layer (layer 13), layer 14 cannot cover the sidewalls *in the base layer*.

As discussed in limitation 1[a], Petitioner includes a confusing annotation of Shiraishi's figure 8 that identifies layers 13 and 14 as corresponding to the body region, but that is inconsistent with the claim text of "said body region disposed on the top of said epitaxial layer" and Petitioner's identification as layer 13 as the base layer. Because Petitioner did not identify layer 14 as part of the base layer in the petition, Petitioners should be foreclosed from making any argument that claim 14 is part of the base layer. 35 U.S.C. § 312(a)(3); 37 C.F.R. § 42.104(b)(3)-(5).

However if the Board allowed the Petitioner to pursue a theory that Shiraishi's layer 13 and layer 14 could be considered, together, to constitute a "base layer," that theory would also fail to satisfy limitation 1[g]. In particular, that argument would be inconsistent with Petitioner's own construction, which requires the lateral contact layer cover the "entire" sidewalls of the source contact trench in the base layer. Pet., 19. Neither Petitioner nor its expert advance any explanation that Shiraishi's layer 14 covers the entire sidewalls of the source contact trenches in the base layer. Pet., 55-56; Ex. 1003 ¶107.

Moreover, Shiraishi's figures plainly show there is not "entire" coverage of the sidewalls in the base layer, i.e., there are portions of the sidewalls in the base

layer (i.e. the depth-wise extent of layer 13, green) not covered by the alleged lateral contact layer (layer 14, purple):



Ex. 1009 (Shiraishi), Fig. 8 (annotated) (layer 15 in red, layer 14 in purple, layer 13 in green)



Magnified and cropped version of above annotated Ex. 1009, Fig. 8

Ex. 2012 ¶142 (annotating Ex. 1009, Fig. 8).

That the coverage of the sidewalls by layer 14 is less than “entire” in the base layer is also consistent with Shiraishi’s written description. Indeed, nothing in Shiraishi discloses layer 13 being entirely replaced or coextensive with layer 14 such that the entire sidewalls would be covered by layer 14. Ex. 2012 ¶143. Rather, Shiraishi describes only “*localized* formation of the p-type semiconductor region 14 *inside* the p– type semiconductor region 13.” Ex. 1009, [0081].⁴ Indeed, layer 14 is disclosed to be a thin layer of “about 0.1 to about 0.4 μm .” Ex. 2012 ¶143 (citing Ex. 1009, claim 22). By contrast layer 13 extends down to about 0.9 μm from the semiconductor surface (0.1 μm less than the 1 μm deep gate trenches). *Id.* (citing Ex. 1009 (Shiraishi), [0083]). Thus, all of Shiraishi’s written disclosures indicate that layer 13 is considerably thicker than layer 14. *Id.* Accordingly, if the claimed “base layer” were considered to be Shiraishi’s layers 13 and 14 together, layer 14 does not cover the “entire” sidewalls of the source contact trenches in the base layer, as required by Petitioner’s construction.

Because Shiraishi does not disclose a “lateral contact layer” covering the entire sidewalls in the base layer, it does not satisfy limitation 1[g].

⁴ Because Shiraishi’s sidewalls layer 13 and 14 can be created by the same mask, they can only be differentiated in the depth-wise direction. Ex. 2012 ¶143, n.5 (citing Ex. 1009 (Shiraishi), [0073]).

(2) Shiraishi's layer 14 is not implanted into the sidewalls of a source contact trench

Shiraishi's layer 14 is not a "lateral contact layer" because it is not a region of dopant resulting from implantation *into the sidewalls* of source contact trenches, as required by the proper construction of "lateral contact layer" (discussed above). Rather, Shiraishi's layer 14 is implanted across the entire active region of the semiconductor surface *prior* to the sidewalls of a source contact trench existing. Ex. 2012 ¶146 (citing Ex. 1009 (Shiraishi), Figs. 6-7, [0073]-[0074]). Thus, Shiraishi does not disclose a region of dopant which is *implanted into sidewalls* of the source contact trenches.

And, even if the Board does not adopt Patent Owner's construction of "lateral contact layer," as discussed above in connection with the Hirler reference, it is compelled by the ordinary meaning of "sidewalls of said trenches in said base layer are *covered* by the lateral *contact layer*" in the context of claim 1. In particular, simply examining the language of the claim, a POSITA would not understand sidewalls being "cover[ed]" by a "layer" as being satisfied by the simple presence of a region at the sidewalls—that would not distinguish the "lateral contact layer" from the claimed "base layer." Ex. 2012 ¶147. Rather, a POSITA would understand "covered by the lateral contact layer" as being consistent with a "thin sheet" being "spread over" the sidewalls. *Id.* (citing Exs. 2025, 2029). Because a sheet cannot

be spread over something that does not yet exist, this would require the side walls to be etched before the lateral contact layer is created. *Id.*

Indeed, these differences are more than a mere variation in manufacturing processes—they reflect structurally different devices, as shown in the following annotated figures:

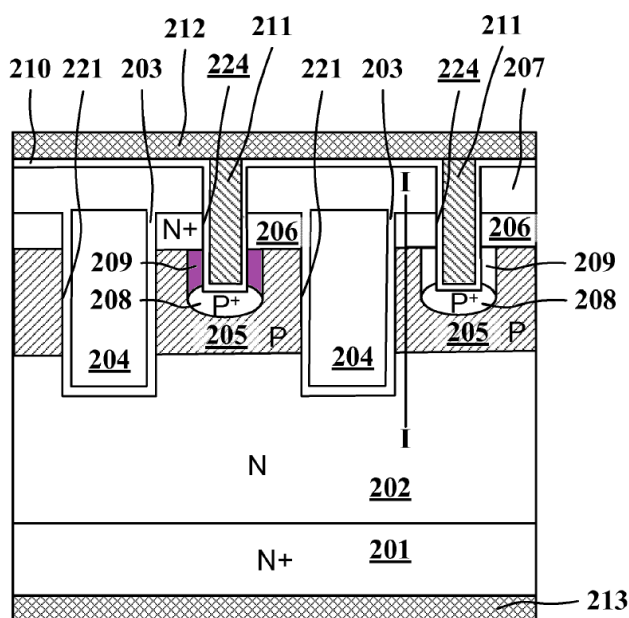
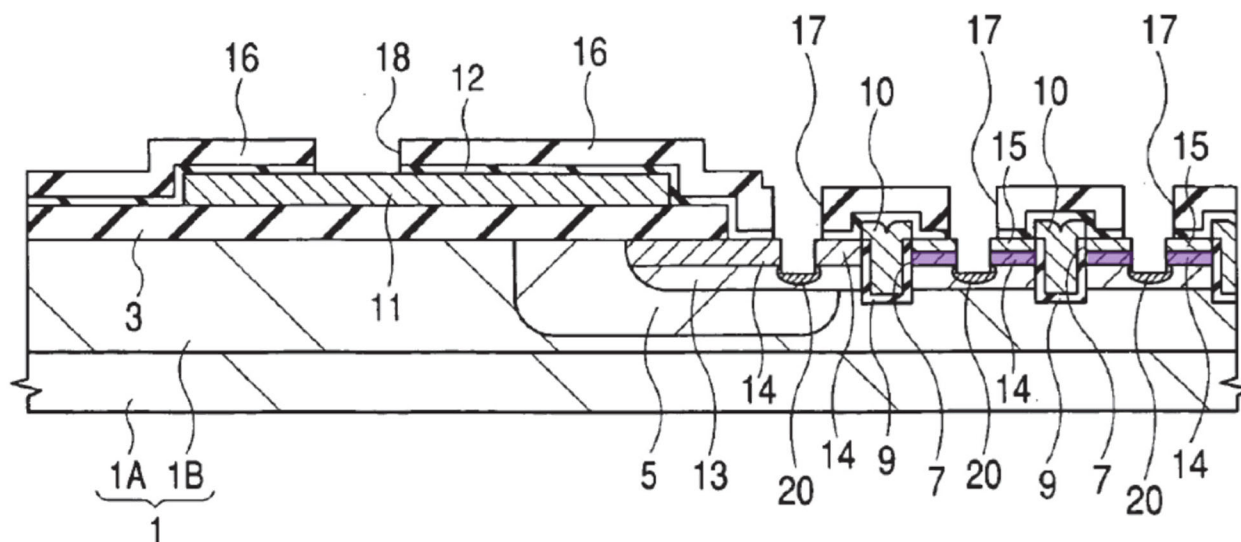


Fig. 2G

'634 Patent, Fig. 2G (annotated)



Ex. 1009 (Shiraishi), Fig. 8 (annotated)

As shown, Shiraishi's technique's for creating layer 14 (i.e., ion implantation across nearly the entire active region of the device's transistors) spreads layer 14 over layer 13, rather than the sidewalls of the source contact trench. As a result, Shiraishi's layer 14 contacts the gate oxide—increasing doping in the channel region. Ex. 2012 ¶149 (citing Ex. 1009 (Shiraishi), [0073], Figs. 5-6, 8). The increased doping of the channel region would increase threshold voltage—exactly the situation the '634 Patent seeks to avoid. *Id.* (citing '634 Patent, 2:10-11, 5:12-16, 5:27-29, Figs. 2G, 4).

Thus, Shiraishi does not satisfy limitation 1[g] because its “layer 14” is not implanted into the sidewalls of a source contact trench.

(3) Shiraishi's layer 14 does not have P* doping

As discussed above, “lateral contact layer,” as properly construed, requires P* doping—a level of doping between conventional P and P+ doping.⁵ Petitioner and its expert fail to identify any evidence demonstrating that Shiraishi's additional semiconductor layer (14) has P* doping. Pet., 55-56; Ex. 1003 ¶107. Indeed, Shiraishi does not describe its semiconductor layer 14 as having doping between P and P+.

Shiraishi does disclose that semiconductor layer 14 “can be doped such that the impurity concentration is less than that of the p+ base contact layer 20 but higher than the p-type body layer 13.” Ex. 1009, [0075]. However, Shiraishi's layer 13 has “p-” (P minus) doping, i.e. light doping which has lower doping concentration than conventional “P” doping. Ex. 2012 ¶¶59, 150 (citing Ex. 1009, [0072]-[0073]). Thus, the disclosure that layer 14 has greater doping than layer 13 does not necessarily imply that layer 14 has P* doping. *Id.* Indeed, layer 14 is a punch-through stopper—Shiraishi does not disclose calibrating layer 14's doping to balance

⁵ The P* portion of Force MOS's construction (as opposed to the N* portion) is applicable to Shiraishi because Shiraishi is an N-channel MOSFET. Ex. 2012 ¶145, n.6; Ex. 1003 ¶¶109-110.

reduced contact resistance against increased threshold voltage. *Id.* (citing Ex. 1009, [0073], [0080]).

Moreover, Shiraishi discloses an aggregate implantation dose of 8×10^{12} ions / cm^2 for layer 14. Ex. 2012 ¶150 (citing Ex. 1009, [0073]). That dose is the same order of magnitude as the 5×10^{12} ions/ cm^2 dose that creates layer 13. *Id.* By contrast, the '634 Patent gives an exemplary range for the dose to create P* doping of 1×10^{14} to $4 \times 10^{14} \text{ cm}^{-2}$ —two orders of magnitude larger than the dose used for Shiraishi's layer 14. *Id.* (citing '634 Patent, 3:58). Because Shiraishi's layers 13 and 14 are created with doses of the same order of magnitude, and because Shiraishi calls layer 13 a "P-" layer, a POSITA would not conclude that layer 14 has P* doping. *Id.* Petitioner and its expert wholly fail to address any of Shiraishi's disclosures regarding implantation dose.

Thus, because Shiraishi does not disclose P* doping, it fails to satisfy limitation 1[g].

2. Claim 2

Claim 2 depends from claim 1. '634 Patent, cl. 2. Petitioner's arguments in Ground 3 for alleged anticipation of claim 2 are based on Petitioner's anticipation arguments for Ground 3, claim 1, which fail as discussed above. Pet., 41-42; *supra*, IV.C.1. Thus, Petitioner has not demonstrated that claim 2 is anticipated. Ex. 1012 ¶151.

D. Ground 4: Shiraishi in view of Kobayashi and the Knowledge of the POSITA Fail to Render Obvious the Challenged Claims

1. Lack of Motivation to Combine

Like Petitioner’s motivation to combine theory for Hirler and Kobayashi in Ground 2, Petitioner seeks to combine Shiraishi with Kobayashi to render obvious the “barrier metal layer and a plurality of contact metal plugs” recited in claims 3 and 7, as well as the additional limitations of claims 4 and 8.

Petitioner’s motivation to combine theory for this ground is similarly inadequate. In particular, the Petition again assumes, without explanation, that a POSITA would be motivated to select *tungsten* plugs in the combination (Pet., 47-48), even though Shiraishi teaches filling its source contact trenches with aluminum (Ex. 1009, [0076], Fig. 9 (element 22)). As discussed in ground 2, that violates the prohibition against “the hindsight combination of components selectively culled from the prior art to fit the parameters of the patented invention,” as part of the motivation to combine is the motivation “to select particular elements” among the prior art. *Supra* VI.B.1. *Cheese Sys., Inc.*, 725 F.3d at 1352; *ATD Corp.*, 159 F.3d at 546. That failure is plainly fatal to Petitioner’s arguments for claims 4 and 8—which specifically recite the use of “tungsten” for the plugs. Moreover, that failure is also fatal to Petitioner’s argument for claims 3 and 5 because Petitioner relies on the use of tungsten in particular to motivate use of a barrier layer. Pet., 48; Ex. 2012 ¶¶154.

The Petition does argue that Kobayashi discloses that contact metal plugs, in general, are beneficial. In particular, the Petition cites Kobayashi's disclosure that:

In the first embodiment, the W 17 is filled in the contact hole 12 as a plug. On the W 17, the source electrode 18 is formed. Therefore, the source electrode 18 finally has a flat surface. Accordingly, the resistance component of the source electrode 18 can be reduced. In addition, the source electrode 18 having a flat surface assures a wide contact area in wire bonding or clip bonding carried out for the surface so that a total on-resistance after mounting can be reduced.

Ex. 1008, [0066] (cited by Pet., 47-48). However, that is only a motivation for the use of a two-stage process (i.e. filling the source contact trenches in one step, planarizing, and then depositing the source contact metal layer). Ex. 2012 ¶154; Ex. 1008, [0066], [0062] (describing tungsten etch back after filling contact trenches). Thus, Petitioner's "flat surface" argument is not an argument to use *tungsten* instead of Shiraishi's aluminum. *Id.* Indeed, it is not even an argument to use *plugs* at all, because one could apply the same two-stage process to an open-cell topology that is incompatible with plugs, such as the stripe topology of Shiraishi's Fig. 11. Ex. 2012 ¶154 (citing Ex. 1009, Fig. 11). And, again, Petitioner fails to explain why conventional techniques, such as chemical mechanical planarization (CMP), would be inadequate for creating a smooth top. *Id.*

Like Ground 2, Petitioner's expert again improperly presents additional theories—not recited in the Petition—touting purported benefits of tungsten. Ex.

1003 ¶112. The Board should reject such theories again for the same reasons in Ground 2. *Supra* VI.B.1. In particular, as in Ground 2, they violate the Board's rule against incorporation by reference, are conclusory assertions without supporting documents, and fail to explain why tungsten would be better than aluminum or why good planarization could be readily achieved by the well-known technique of CMP. Ex. 2012 ¶131, 154.

Moreover, Petitioner and its expert ignore the significant differences in structure and purpose between Shiraishi and Kobayashi. Indeed, they are diametrically opposed references that both teach away from each other. Kobayashi is specifically focused on avoiding the leaching of dopants into the channel region, and the resulting increase of threshold voltage. Ex. 2012 ¶153; Ex. 1008 (Kobayashi) 174, [0014]-[0019], [0025], [0037], Figs. 5A, 5B, 7C. By contrast, as discussed, Shiraishi is specifically focused on its punch-through stopper layer which introduces additional dopants laterally throughout the body region between the trench gates and the source trenches so as to reduce punch through, i.e., the focus of Shiraishi is to intentionally do what Kobayashi specifically seeks to avoid. Ex. 2012 ¶153; Ex. 1009 (Shiraishi), Fig. 9, [0080]-[0081]. These contradictory disclosures are directly relevant to the proposed combination, as Petitioner proposes combining components of the structure of Kobayashi's source contact trenches with Shiraishi's source contact trenches. Even if the Board determines these disclosures do not rise

to “teaching away,” these differences in structure and purpose would still lead to a conclusion of non-obviousness. *See Rembrandt Wireless Tech*, 853 F.3d at 1379-80; *Apple*, 839 F.3d at 1051 n.15; *Arctic Cat*, 876 F.3d at 1360. Accordingly, a POSITA would not be motivated to select those references for combination. *WBIP*, 829 F.3d at 1337 (“Whether a skilled artisan would be motivated to make a combination includes whether he would select particular references in order to combine their elements.”).

Thus, the petition fails to identify a motivation to combine Shiraishi with Kobayashi to use plugs, little less tungsten plugs.

2. Claims 3-9

Claims 3-9 all depend directly or indirectly from claim 1. '634 Patent, cls. 3-9. Petitioner's obviousness arguments in Ground 4 for alleged obviousness of claims 3-9 are based on Petitioner's arguments that Shiraishi anticipates claim 1, which fail as discussed above. Pet., 42-46 (citing to Ground 3). In Ground 4, Petitioner offers no argument or evidence that Kobayashi or the knowledge of a POSITA cures any of the deficiencies of Shiraishi identified above with respect to claim 1. That is, because Petitioner has failed to demonstrate that Shiraishi discloses each limitation of claim 1, Petitioner's obviousness arguments in Ground 4 for claims 3-9 fail for the same reasons discussed above for claim 1 in Ground 3. *See supra* VI.C.1.

3. Claims 3-5, 7-9: “barrier metal layer and a plurality of contact metal plugs” and “the contact metal plug is Tungsten”

As discussed above (*supra* VI.D.1), Petitioner fails to provide an adequate motivation to combine Shiraishi and Kobayashi to have “barrier metal layer and a plurality of contact metal plugs,” which is recited in claims 3 and 7, from which claims 4-5 and 8-9 respectively depend. Nor do they provide an adequate motivation to use “tungsten” for the “contact metal plug,” as recited in claims 4 and 8. Accordingly, Petitioner’s obviousness theory for claims 3-5 and 7-9 fails. Ex. 2012 ¶156.

E. Ground 5: Kobayashi in view of Shiraishi and the Knowledge of the POSITA Fail to Render Obvious the Challenged Claims

1. Lack of Motivation to Combine

Petitioner argues that a POSITA would combine Shiraishi’s punch-through stopper layer 14 with Kobayashi “to optimize the MOSFET and prevent punch-through.” Pet., 63; Ex. 1003 ¶¶167-168. Petitioner’s theory suffers from several fatal flaws.

(a) Petitioner fails to demonstrate that Kobayashi would benefit from a punch-through stopper layer

First, Petitioner articulates no reason to believe that Kobayashi’s MOSFET would benefit from a punch-through stopper layer (i.e. that it suffers from punch-through). *Id.* At his deposition, Petitioner’s expert could not identify a portion of

his declaration offering an opinion that Kobayashi suffered from punch-through. *See* Ex. 2014, 93:18-94:14 (instead noting that “It's all a different degree and how you want to incrementally optimize your device and -- without sacrificing any of the parameters”).

Indeed, in attempting to optimize a MOSFET's design, such as by increasing the cell density (i.e., reducing cell pitch, as discussed in Kobayashi), there are a variety of obstacles that can be limiting, including on-resistance, threshold voltage, avalanche breakdown, latch-up, and gate capacitance. Ex. 2012 ¶160. Even if breakdown were a limiting factor, punch through breakdown does not apply to every MOSFET design—the limiting form of breakdown can be avalanche breakdown, Zener breakdown, or punch-through. *Id.* Petitioner's expert, at his deposition, stated “you don't want the breakdown voltage to be undermined by other means of breakdown ... you want to live to 120 years and you don't want -- you don't want any other things, you know, reckless driving or reckless drinking to undermine your lifespan” Ex. 2014, 96:8-97:12. Using that analogy, not every MOSFET will benefit from 120 years of punch-through ruggedness if its lifespan is going to end at 30 due to Zener breakdown or avalanche breakdown.

Because not every MOSFET benefits from improved punch-through ruggedness, Petitioner's failure to articulate a reason why Kobayashi's MOSFET would benefit from reduced punch-through is fatal to its theory. Moreover, even if

punch-through were a problem, Petitioner articulates no reason to specifically select Shiraishi for combination, given that there were other ways known in the art to avoid punch-through. Ex. 2012 ¶161 (citing Exs. 2033, 2034).

(b) Petitioner’s combination directly violates Kobayashi’s express teaching and purpose

Second, Petitioner ignores that Shiraishi and Kobayashi are diametrically opposed references that teach away from each other, as discussed in ground 4. *See supra* VI.D.1. In particular, as discussed, the primary purpose of Kobayashi is specifically focused on the problem of avoiding the increased threshold caused by leaching of dopants into the channel region. Ex. 2012 ¶153, 159; Ex. 1008 (Kobayashi) 174, [0014]-[0019], [0025], [0037], [0065], [0073] Figs. 5A, 5B, 7C. However, Shiraishi’s punch-through stopper layer introduces additional dopants laterally throughout the cell between the trench gates and the source trenches so as to reduce punch through. Ex. 2012 ¶¶153, 159; Ex. 1009 (Shiraishi), Fig. 9, [0073], [0080]-[0081]. Indeed, like Shiraishi, in Petitioner’s proposed combination of Shiraishi and Kobayashi the punch-through layer extends laterally all the way to the gate. Pet., 64-65; Ex. 2012 ¶159. Thus, Petitioner’s proposed combination would combine Kobayashi with Shiraishi in a manner expressly taught away by Kobayashi.

Even if the Board determines these disclosures do not rise to “teaching away,” these differences in structure and purpose would still lead to a conclusion of non-

obviousness. *See Rembrandt Wireless Tech*, 853 F.3d at 1379-80; *Apple.*, 839 F.3d at 1051 n.15; *Arctic Cat*, 876 F.3d at 1360. Indeed, it is well established that combinations that would defeat the basic objective of one of the references or render it inoperable for its intended purpose are unlikely. *In re Ratti*, 270 F.2d 810, 813 (CCPA 1959); *In re Gordon*, 733 F.2d 900, 902 (Fed. Cir. 1984); *Trivascular, Inc. v. Samuels*, 812 F.3d 1056, 1068 (Fed. Cir. 2016). Modifying Kobayashi to have region of increased dopant in its channel would defeat Kobayashi's basic objective and render it inoperable for the purpose of having reduced threshold voltage compared to the prior art. Ex. 2012 ¶159.

(c) Petitioner articulates no reason why a POSITA would be motivated to combine Kobayashi with Shiraishi such that the punch-through-stopper layer covered the “entire” sidewalls in the base layer

Third, even if there were a motivation to combine Kobayashi with Shiraishi, Petitioner articulates no reason to combine Kobayashi with Shiraishi such that the punch-through layer covered the “entire” sidewalls of Kobayashi's source contact trenches in the base layer, as required by Petitioner's construction. Pet., 19. Indeed, the only argument that Petitioner advances is its contention that Shiraishi itself “expressly teaches a lateral contact layer along the entire sidewalls of the contact trench in the base layer that serves as ‘a punch-through stopper layer.’” Pet., 63; Ex. 1003 ¶167.

However, as discussed in ground 3, Shiraishi's punch-through stopper layer 14 does not cover the entire sidewalls of its source contact trenches in the base layer. *Supra* VI.C.1.b (citing Ex. 2012 ¶¶142-143, 1009, Fig. 8, [0081], [0083], cl. 22). Moreover, as discussed, Kobayashi teaches away from any increased dopants in the channel region. Ex. 2012 ¶¶164, 166; Ex. 1008, [0065], [0073] ("since the base contact layer is not present on the side wall of the contact, the source layer resistance is never increased."). And, Shiraishi teaches that layer 14 should be much thinner than layer 13, and thus a POSITA would not be motivated to cover the entire sidewalls of Kobayashi with layer 14 (displacing Kobayashi's base layer). Ex. 2012 ¶¶143, 165. Thus, Petitioner articulates no motivation to combine Kobayashi with Shiraishi in a manner that would satisfy its own construction of "the sidewalls of said trenches in said base layer."

2. Claim 1

- c) **1[a]: The proposed combination of Kobayashi and Shiraishi Fails to Satisfy "a base layer corresponding to said body region disposed on the top of said epitaxial layer" and/or "a source layer corresponding to said source region disposed on the top of said base layer"**

In Ground 5, Petitioner argues that it would be obvious to modify Kobayashi to add Shiraishi's punch-through stopper layer 14, underlying Kobayashi's source layer and overlaying Kobayashi's P-type base layer, except for where interrupted by the gate and source trenches. Pet., 63-65.

Because this combination uses Shiraishi's punch-through stopper layer 14 in the same place in Kobayashi as in Shiraishi, Petitioner's theory for this ground suffers from all the same deficiencies as discussed in connection with limitation 1[a] in Ground 3 (alleged anticipation over Shiraishi). *Supra* VI.C.1.a.

In particular, in the proposed combination, because Shiraishi's punch-through stopper layer is disposed between Kobayashi's source layer and base layer (Pet., 64, 65), the proposed combination fails to satisfy limitation 1[a]'s requirement that the "source layer ... [be] disposed on the top of said base layer." *See supra* VI.C.1.a; Ex. 2012, ¶¶137, 138, 163. Indeed, neither Petitioner nor its expert articulates any reason that, in the proposed combination, Shiraishi's punch-through stopper layer would be considered to be part of the MOSFET's base layer (instead of being its own separate layer). Pet., 62-65; Ex. 1003 ¶¶164-170. To the contrary, as discussed, Shiraishi does not describe the punch-through stopper layer as part of the base layer or body of a MOSFET, and describes the channel being formed in a different layer. *See supra* VI.C.1.a (citing Ex. 2012 ¶138; Ex. 1009, [0072]-[0073], [0080]-[0081], [0084]). Thus, the Kobayashi-Shiraishi combination would fail to satisfy limitation 1[a] for the same reasons as Shiraishi alone.

a) 1[g]: Petitioner Fails to Show that Kobayashi or Shiraishi Disclose or Suggest “the sidewalls of said trenches in said base layer are covered by the lateral contact layer”

Because the proposed combination of Petitioner’s ground 5 uses Shiraishi’s punch-through stopper layer 14, in the same place in Kobayashi as it is located in Shiraishi, Petitioner’s theory for this ground suffers from all the same deficiencies as discussed in connection with limitation 1[g] in Ground 3 (alleged anticipation over Shiraishi). *Supra* VI.C.b.

First, because, in the proposed combination, Shiraishi’s punch-through stopper layer (the alleged lateral contact layer) is disposed *above* Kobayashi’s base layer (Pet., 64, 65), the proposed combination fails to satisfy limitation 1[g]’s requirement that the “the sidewalls of said trenches *in said base layer* are covered by the lateral contact layer.” *See supra* VI.C.1.b.1; Ex. 2012, ¶¶137, 138, 163. And, as mentioned, neither Petitioner nor its expert articulates any reason that, in the proposed combination, Shiraishi’s punch-through stopper layer would be considered to be within the combined MOSFET’s base layer, as Shiraishi does not describe the punch-through stopper layer as part of the base layer or body. *See supra* VI.C.1.a. (citing Ex. 2012 ¶138; Ex. 1009, [0072]-[0073], [0080]-[0081], [0084]).

Moreover, as discussed above, Shiraishi’s layer 14 does not cover the entire sidewalls in Shiraishi. *Supra* VI.C.1.b.1. And, as discussed (*supra* VI.E.1), even if

Shiraishi's layer 14 were considered to be in the combined MOSFET's base layer, there is no motivation to combine Shiraishi's punch-through stopper layer with Kobayashi such that the punch-through stopper layer would cover the "entire" sidewalls in the base layer (i.e. to make Shiraishi's thin layer 14 thick enough to cover the entire sidewalls of Kobayashi's base layer). Ex. 2012 ¶164. Thus, the proposed combination would not satisfy Petitioner's own construction of "the sidewalls of said trenches in said base layer."

Furthermore, as discussed, Shiraishi's punch-through stopper layer does not have P* doping (or N* doping). *See supra* VI.C.1.b.3. Petitioner's obviousness combination relies on Shiraishi's punch-through stopper layer for satisfying the "lateral contact layer," and Petitioner articulates no reason to modify the doping of that punch-through stopper layer in the combination with Kobayashi. Pet., 55-56; Ex. 1003 ¶¶145-147. Accordingly, the proposed combination would not satisfy the appropriate construction of "lateral contact layer," which requires P* doping.

Finally, as discussed, Shiraishi's punch-through stopper layer 14 is not implanted into the sidewalls of an existing source contact trench. *See supra* VI.C.1.b.2. Petitioner's obviousness combination relies on Shiraishi's punch-through stopper layer for satisfying the "lateral contact layer," and Petitioner articulates no reason to modify the structure of that layer or the process for its creation in the proposed combination with Kobayashi. Pet., 64-65; Ex. 1003 ¶¶165-

170. To the contrary, Petitioner depicts the proposed combination as having the punch-through stopper layer being spread over the base layer (rather than the sidewalls of the source contact trench), and extending laterally along the entire portion of the cell that is not displaced by the source or gate trenches. Pet., 64-65. Accordingly, the proposed combination would not satisfy the appropriate construction of “lateral contact layer,” which requires implantation into an existing source contact trench.

3. Claims 2-9

Claims 2-9 all depend, directly or indirectly, from claim 1 of the '634 Patent. Because claim 1 is not rendered obvious over Kobayashi in view of Shiraishi, for the reasons discussed above (*supra* VI.E.2), claims 2-9 are also not obvious. Ex. 2012 ¶¶167-168.

(a) Claims 3-5, 7-9: “barrier metal layer and a plurality of contact metal plugs”

Claim 3 recites “The trenched MOSFET of claim 2, wherein further comprises a barrier metal layer and a plurality of contact metal plugs.” Similarly, claim 7 recites “wherein further comprises a barrier metal layer and a plurality of contact metal plugs.” Claims 4-5 depend from claim 3, and claims 8-9 depend from claim 7. '634 Patent, cls. 3-5, 7-9.

As discussed in the Ground 4, Petitioner and Dr. Liu fail to articulate an adequate motivation to combine Shiraishi and Kobayashi to use tungsten metal

plugs. *Supra* VI.D.1. Moreover, in ground 5—with Kobayashi as the primary reference—Dr. Liu and Petitioner simply seem to assume that the combination would use Kobayashi’s metal plugs (rather than, for example, the continuous metal trench embodiment of Shiraishi’s Fig. 11), without explanation. Pet., 58, 62-66; Ex. 1003 ¶¶165-169. Thus, Petitioner’s motivation to combine arguments in this ground fail due to lack of disclosure. 35 U.S.C. § 312(a)(3). Even if they were permitted to rely on the theories for using tungsten plugs presented in Ground 4, Petitioner’s arguments for Ground 5, claims 3-5 and 7-9 would fail for the same reasons as Ground 4. *See supra* VI.D.1, VI.D.3.

VII. CONCLUSION

For the above reasons, Patent Owner requests that Board hold that all challenged claims are patentable.

Date: September 16, 2024

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Certificate of Service 37 C.F.R. § 42.6(e)

The undersigned certifies that on September 16, 2024, I will cause true and correct copies of the foregoing Patent Owner's Response, and all associated exhibits or appendices referred to therein, to be served electronically upon the following attorneys who have consented to service via email. Paper 18.

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