

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INERGY TECHNOLOGY, INC.,
Petitioner

v.

FORCE MOS TECHNOLOGY CO. LTD.,
Patent Owner

Inter Partes Review No. IPR2024-00093
U.S. Patent No. 7,629,634

DECLARATION OF DEAN NEIKIRK, PH.D.
IN SUPPORT OF PATENT OWNER'S RESPONSE

TABLE OF CONTENTS

I.	INTRODUCTION	3
II.	BACKGROUND AND QUALIFICATIONS	4
III.	COMPENSATION	8
IV.	MATERIALS CONSIDERED	8
V.	UNDERSTANDING OF LEGAL PRINCIPLES	10
A.	Claim Construction	10
B.	Invalidity Based on Prior Art	11
1.	Prior Art	11
2.	Anticipation.....	14
3.	Obviousness	16
VI.	LEVEL OF ORDINARY SKILL IN THE ART	20
VII.	BACKGROUND OF TRENCHED MOSFETS	21
VIII.	BACKGROUND OF THE '634 PATENT	33
IX.	CLAIM CONSTRUCTION	36
A.	“lateral contact layer” ('634 Patent, cl. 1).....	36
B.	“the sidewalls of said trenches in said base layer” ('634 Patent, cl. 1).....	51
X.	THE CHALLENGED CLAIMS OF THE '634 PATENT ARE NOT ANTICIPATED AND ARE NOT RENDERED OBVIOUS	53
A.	Overview of the Prior Art Relied Upon for the '634 Patent	53
1.	German Patent Publication No. DE 102004009083 (“Hirler”)	53
2.	U.S. Patent Publication No. 2004/0021174 (“Kobayashi 174”).....	53
3.	U.S. Patent Publication No. 2005/0029584 (“Shiraishi”)	54
B.	Claims 1-2 and 6 of the '634 Patent Are Not Anticipated by Hirler ..	56
1.	Claim 1	56
2.	Claims 2 and 6.....	66
C.	Claims 3-5 and 7-9 Are Not Obvious over Hirler in View of Kobayashi 174.....	66
1.	Lack of Motivation to Combine in Manner Claimed	66
2.	Claim 3-5, 7-9	70

D.	Claims 1 and 2 Are Not Anticipated by Shiraishi.....	71
1.	Claim 1	71
2.	Claim 2	81
E.	Claims 3-9 Are Not Obvious over Shiraishi in View of Kobayashi 174	81
1.	Lack of Motivation to Combine.....	82
2.	Claims 3-9	83
F.	Claims 1-9 Are Not Obvious over Kobayashi 174 in View of Shiraishi.....	84
1.	Lack of Motivation to Combine.....	85
2.	Claim 1	88
3.	Claims 2 and 6.....	90
4.	Claims 3-5 and 7-9	91
XI.	CONCLUSION.....	92

I. INTRODUCTION

1. I have been retained by Patent Owner Force Mos Technology Co. Ltd. (“Patent Owner” or “ForceMOS”) in this *inter partes* review proceeding number IPR2024-00093 (“IPR”), filed by Petitioner Inergy Technology, Inc. (“Inergy” or “Petitioner”). I understand that this IPR proceeding involves U.S. Patent No. 7,629,634 (the ’634 patent) and that the challenged claims are claims 1-9 (the “Challenged Claims”).

2. I have been asked to provide my objective, independent analysis of the ’634 patent in view of the asserted prior art references cited in the Petition and to provide my opinion regarding the allegations in the Petition, as well as the supporting opinions of Dr. David Kuan-Yu Liu.

3. I have based my opinions on the information available to me as of the date of this declaration. I understand that additional information may become available after this declaration is submitted. If I become aware of additional information following my submission of this declaration I may, if I am permitted, offer additional opinions (including by amending and/or supplementing this declaration) taking into account such new information.

4. I am not currently, nor have I ever been, an employee of Force MOS. I received no compensation for this declaration beyond my normal hourly compensation based on my time actually spent working on this IPR. I will not

receive any added compensation based on the outcome of this IPR, any other IPR, or any other proceeding involving the '634 patent.

II. BACKGROUND AND QUALIFICATIONS

5. My qualifications are most accurately reflected in my curriculum vitae, which is Exhibit 2013. The following is a brief summary of some of my relevant experience and qualifications.

6. I have over 40 years of experience in electronic devices and systems, including the methods used to fabricate integrated circuits and devices.

7. I received a B.S. degree in 1979 in physics from Oklahoma State University, and an M.S. degree and a Ph.D. degree in 1981 and 1984, respectively, in applied physics from the California Institute of Technology.

8. Each of my academic degrees involved significant studies in solid state physics, semiconductor devices, electrical engineering, electronic systems, electromagnetics, optics, radio frequency systems, and antennas. For example, courses relating to these fields that I took include two years of study in electromagnetics and optics, one year of study in solid state and semiconductor physics, as well as four years of graduate research in electronic devices, antenna design, antenna fabrication, microwave systems, and optical systems. My Ph.D. thesis was on the design and fabrication of high frequency electromagnetic detectors and imaging arrays, including research on integrated-circuit fabrication, antennas,

sensors, and packaging. I designed and fabricated the first monolithic integrated-circuit imaging array for use at wavelengths in the far infrared (sometimes referred to as the terahertz) region of the electromagnetic spectrum. This research work required the fabrication, testing, and field placement of devices with many output channels, presenting a significant challenge (at that time) in packaging. I personally developed packages for my devices, and personally performed the packaging itself. At that time the most common method of connection made use of wirebonding, which I personally performed.

9. I am currently a Life Senior Member of the Institute of Electrical and Electronics Engineers (“IEEE”). From March 1991 to October 1994, I served as an Associate Editor for the IEEE publication called “IEEE Transactions on Education.” I also served as a member of the Editorial Board on the IEEE Transactions on Microwave Theory and Techniques in the 1990-2000 timeframe.

10. I have almost 40 years of experience on the faculty of the University of Texas at Austin. My work as a professor began in 1984, when I joined the University of Texas at Austin as an assistant professor. In 1988, I became an associate professor, and became a full professor in 1992.

11. My research over the last forty years has concentrated heavily in the areas of electromagnetics, microwave engineering, microelectronics, semiconductor devices, integrated circuit (IC) fabrication, and new sensors. This research work has

been funded by many agencies, focusing on the fabrication and modeling of semiconductor devices, electromagnetic devices and detectors, chemical sensors, temperature sensors, proximity sensors, and pressure sensors, as well as research on the high frequency properties of transmission lines, RF devices, and infrared to terahertz detectors for use in focal plane imaging arrays. My research related to the development of new chemical sensors (an “electronic taste” sensor) was selected for a commercialization venture between The University of Texas and two outside startup companies.

12. Over the years, I have also taught a variety of electrical engineering courses at the University of Texas. These include Integrated Circuit Fabrication, VLSI Fabrication Techniques, Ultra Large Scale Integrated Circuit Fabrication Techniques, Integrated Circuit Nanomanufacturing Techniques, Electromagnetics in Packaging, Simulation Methods in CAD/VLSI, Micro-Electromechanical Systems, Electromagnetic Engineering, and Microwave and Radio Frequency Engineering. I have also taught several continuing education courses in these fields.

13. In 1985, I established the Microelectronics Fabrication Teaching Laboratory at The University of Texas at Austin, which continues to this day to provide undergraduate and graduate students with hands-on experience in integrated circuit fabrication. I have taught many courses in integrated-circuit fabrication, microwave devices, integrated circuit packaging, electromagnetics, computer aided

design methods for circuit simulation, sensors of all sorts, and microelectromechanical systems.

14. I conducted research with students and research scientists in the Microelectromagnetics Research Group in the Microelectronics Research Center at The University of Texas at Austin for 37 years. For over ten years, I also served as the Graduate Advisor of the Department of Electrical and Computer Engineering at the University of Texas at Austin, as well as serving for over five years as an Associate Chairman of the Electrical and Computer Engineering Department at The University of Texas at Austin. I also served as Associate Dean of Graduate Studies from 2014 to 2021.

15. In addition to my work at The University of Texas at Austin, I have done part-time consulting work since 1984 as an independent consultant to the industry for technical projects and as a technical expert in legal cases. I am a senior member of the IEEE. Through my work on sensors, electronic systems, and innovations in other related fields, I have been named an inventor on 17 U.S. patents. These are summarized in my curriculum vitae.

16. As a result of my professional education and experience, I am qualified to render opinions in the areas of semiconductors and their fabrication, and in particular, the subject matter of the patents-in-suit.

III. COMPENSATION

17. I am being compensated as an expert witness in this case at my standard hourly rate in addition to out-of-pocket expenses. I have received no additional compensation for my work on this matter and my compensation does not depend, and has not ever depended in any way, on my opinion as expressed in this matter, in any testimony that I may give, or on the outcome of this matter. I am not and have never been employed by Force MOS. I have no financial stake in Force MOS, the ‘634 Patent, or the outcome of this IPR or any other matter involving the ‘634 Patent.

IV. MATERIALS CONSIDERED

18. In formulating my opinions, I have relied upon my training, knowledge and experience that are relevant to the ‘634 Patent. I have also considered the ‘634 Patent and its file history, Petition (“Pet.”) and attached exhibits, the Patent Owner preliminary response, the Board’s decision on institution, the asserted prior art references, and the declaration of Dr. Liu and the materials cited therein. In addition to the materials cited elsewhere in this declaration, I have also considered the following:

Exhibit No.	Description
1017	Memorandum Order and Opinion (regarding claim construction), Dkt. No. 94 from <i>Alpha and Omega Semiconductor Limited et al v. Force MOS Technology Co., Ltd.</i> , Case No. 5:22-cv-05448-PCP (N.D. Cal.)
2006	Illustrated Dictionary of Electronics (Excerpts)
2007	Semiconductor Glossary (Excerpts)
2008	U.S. Patent No. 6,888,196 (Kobayashi 196 Patent)

2011	Claim Construction Order, Dkt. No. 132 from <i>Force Mos Technology Co., Ltd. v. ASUSTeK Computer, Inc.</i> , Case No. 2:22-cv-00460-JRG (E.D. Tex.)
2014	Transcript of Aug. 22, 2024 Deposition of David Kuan-Yu Liu
2015	Zhang, Ruizhe, and Yuhao Zhang. "Power device breakdown mechanism and characterization: Review and perspective." <i>Japanese Journal of Applied Physics</i> 62.SC (2023): SC0806
2016	Additional Excerpts from Semiconductor Glossary
2017	Search results from scholar.google.com for article search “‘lateral contact layer’ MOSFET”
2018	Wang, Jingshan. High-Power Vertical GaN Electronic Devices Formed by Epitaxial Lift-Off. Diss. University of Notre Dame, 2018.
2019	Definition of “lateral” from https://www.merriam-webster.com/dictionary/lateral
2021	Definition of “contact” from https://www.merriam-webster.com/dictionary/contact
2022	Definition of “contact” from https://www.lamresearch.com/technical-glossary/
2023	Definition of “layer” from https://www.merriam-webster.com/dictionary/layer
2024	U.S. Patent No. 3,025,589 to Hoerni, “Method of manufacturing semiconductor devices”
2025	Definition of “layer” from https://dictionary.cambridge.org/us/dictionary/english/layer
2026	Suzuki, Kunihiro, A. Satoh, and T. Sugii. "Counter doping into uniformly and heavily doped channel region of sub-0.1 μm SOI MOSFETs." <i>IEEE Electron Device Letters</i> 17.1 (1996)
2027	U.S. Patent No. 4,315,781 to Henderson, “Method of controlling MOSFET threshold voltage with self-aligned channel stop”
2028	U.S. Patent No. 8,884,409 to Wong, “Wafer backside doping for thermal neutron shielding”
2029	Definition of “cover” from https://www.merriam-webster.com/dictionary/cover
2030	Excerpts of Sedra, Adel S., <i>Microelectronic Circuits</i> (5 th Ed. 2004)
2031	Williams, <i>Principles and Elements of Power Electronics</i> , ISBN 978-0-9553384-0-3 (2006)

2032	Sharma, R. S., and M. A. Peer. "Some Features of Avalanche Breakdown Phenomena Part 1: Transistors and Diodes." IETE Journal of Research 27.5 (1981): 178-184
2033	U.S. Patent No. 6,084,264 to Darwish, "Trench MOSFET having improved breakdown and on-resistance characteristics"
2034	U.S. Patent No. 6,545,315 to Hshieh et al., "Trench DMOS transistor having reduced punch-through"

V. UNDERSTANDING OF LEGAL PRINCIPLES

19. I am not an attorney. I have been asked to provide opinions on the validity of the Asserted Claims of the Patents-in-Suit from the perspective of a POSITA.

A. Claim Construction

20. I have been provided certain legal principles relating to the construction of patent claims. I understand that "claim construction" is the interpretation of the meaning of patent claims. I understand that words of a claim are generally given their ordinary and customary meaning, which is the meaning the term or phrase would have to a person of ordinary skill in the art at the time of the invention. I understand that both intrinsic and extrinsic evidence can be used to assist in understanding the meaning of a claim. Intrinsic evidence includes the claim language, language in other claims of the patent, the specification, and the prosecution record. I further understand that, unless required by the claim language or specification, claims should generally not be limited to embodiments in the specification, including preferred embodiments. I understand that extrinsic

evidence, which consists of all evidence external to the patent and prosecution history including expert and inventor testimony, dictionaries, and learned treatises, may also be relevant to claim construction.

B. Invalidity Based on Prior Art

21. I understand that each claim of an issued patent is presumed to be valid. A party challenging the validity of a patent claim must present clear and convincing evidence to overcome the presumption of validity.

1. Prior Art

22. I understand that a patent or other publication must first qualify as prior art before it can be used to invalidate a patent claim.

23. I understand that a U.S. or foreign patent qualifies as prior art to an asserted patent if the date of issuance of the patent is prior to the invention of the asserted patent. I further understand that a printed publication, such as an article published in a magazine, academic journal, conference proceedings, or trade publication, or U.S. or foreign published patent application qualifies as prior art to an asserted patent if the date of publication is prior to the invention of the asserted patent.

24. I understand that a U.S. or foreign patent qualifies as prior art to an asserted patent if the date of issuance of the patent is more than one year before the priority date of the asserted patent. I further understand that a printed publication,

such as an article published in a magazine, academic journal, conference proceedings, or trade publication, or U.S. or foreign published patent application constitutes prior art to an asserted patent if the publication occurs more than one year before the priority date of the asserted patent.

25. I understand that, absent an assertion by the patentee otherwise, the date of invention is the filing date of the patent. I understand that a U.S. patent qualifies as prior art to the asserted patent if the application for that patent was filed in the United States before the invention of the asserted patent.

26. I understand that a system or device qualifies as prior art to the asserted patent if it was known or used in the United States prior to the invention of the asserted patent. I further understand that a system or device qualifies as prior art to the asserted patent if it was in public use or on sale in the United States more than one year prior to the priority date of the asserted patent.

27. I understand that if a device was used by others in this country before the date of the invention, or if it was in public use in this country more than one year before the effective date of application, the device qualifies as prior art. I understand that, under either scenario, for a non-patentee's use to qualify as prior art, the purported use must have been available to the public. I understand that the following factors may be helpful in analyzing whether there was a public use: (1) the nature of the activity that occurred in public; (2) the public access to and knowledge of the

public use; and (3) whether there was any confidentiality obligation imposed on persons who observed the use. I further understand that where a non-patentee's public use puts all the claimed features of an invention in the public's possession, this cannot be negated by evidence that other, unclaimed aspects of the non-patentee's device were not publicly available. Conversely, I understand that for a non-patentee's uses to constitute prior art, that use must have placed each of the claimed features of an invention in the public's possession. And, I understand that a non-patentee's secret or confidential uses do not invalidate later-filed patents.

28. I understand that a patent claim may be anticipated where, before the invention thereof, the invention was made in this country by another inventor who had not abandoned, suppressed, or concealed it. I further understand that when the non-patentee's invention's "inner workings" are the essence of the invention, it is those "inner workings" that must not be suppressed or concealed in order for the invention to constitute prior art.

29. I also understand that prior art can include work by a prior inventor if that prior inventor: (1) conceived of the claimed invention before the conception date of the patentee, (2) was reasonably diligent in reducing the invention to practice from just prior to the conception date of the patentee, and (3) has not abandoned, suppressed or concealed the invention.

30. I understand that to qualify as prior art, a reference must contain an enabling disclosure that allows one of ordinary skill to practice the claims without undue experimentation.

31. I understand that documents and materials that qualify as prior art can be used to invalidate a patent claim as anticipated or as obvious.

32. I understand that invalidity must be shown by clear and convincing evidence. Furthermore, I understand that clear and convincing evidence means that it is highly probable that the fact is true.

2. Anticipation

33. I understand that, pursuant to 35 U.S.C. § 102, a claim of a patent is invalid for anticipation if, among other things, any of the following is true: (i) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for patent, (ii) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country more than one year prior to the date of the application for patent in the United States, or (iii) the invention was described in another's United States patent or published patent application which issued from a patent application filed in the United States before the invention by the applicant for patent.

34. I understand that, once the claims of a patent have been properly construed, the second step in determining anticipation of a patent claim requires a comparison of the properly construed claim language to the prior art on a limitation-by-limitation basis.

35. I understand that a prior art reference “anticipates” an asserted claim, and thus renders the claim invalid, if all elements of the claim are disclosed in that prior art reference, either expressly or inherently (i.e., necessarily present), arranged in the same way as in the claim. I understand that, for inherent anticipation, it is required that the missing descriptive material is necessarily present in the prior art reference.

36. I understand that to anticipate an asserted claim, an allegedly anticipatory prior art reference has to have an enabling disclosure. I understand an enabling disclosure describes the claimed invention in sufficient detail to enable a person of ordinary skill in the art to carry out the claimed invention.

37. I understand that a patent is anticipated if, before such invention thereof, the invention was made in this country by another inventor who had not abandoned, suppressed, or concealed it.

38. A patent claim is also anticipated if there is clear and convincing proof that, more than one year before the priority date of the patent, the claimed invention was: in public use or on sale in the United States; patented anywhere in the world;

or described in a printed publication anywhere in the world. This is called a statutory bar.

39. I have written this declaration with the understanding that anticipation must be shown by clear and convincing evidence. I understand that clear and convincing evidence means that it is highly probable that the fact is true.

3. Obviousness

40. I understand that even if a patent is not anticipated, it is still invalid pursuant to 35 U.S.C. § 103 if the differences between the claimed subject matter and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person of ordinary skill in the pertinent art (henceforth, a “POSITA” or “POSITA”).

41. I understand that a POSITA provides a reference point from which the prior art and claimed invention should be viewed. This reference point prevents one from using his or her own insight or hindsight in deciding whether a claim is obvious.

42. I also understand that an obviousness determination includes the consideration of various factors such as (1) the scope and content of the prior art, (2) the differences between the prior art and the Asserted Claims, (3) the level of ordinary skill in the pertinent art, and (4) the existence of secondary considerations (also called objective indicia of non-obviousness).

43. I understand that the test of obviousness is whether the claimed invention, as a whole, would have been obvious to one of ordinary skill in the art as of the date of the invention in light of the prior art.

44. I understand that a claim is not proved obvious merely by demonstrating that each of the elements was independently known in the prior art. I understand that most, if not all, inventions rely on building blocks long since uncovered, and claimed discoveries, almost of necessity, will likely be combinations of what is already known. I understand that it is important to identify whether a reason existed at the time of the invention that would have prompted a person of ordinary skill in the art in the relevant field to combine the known elements in the way the claimed invention does. I understand that the use of hindsight must be avoided when considering whether the alleged invention would have been obvious to the person of ordinary skill in the art. In assessing obviousness, I have been instructed to consider the distortion caused by hindsight bias, guard against slipping into the use of hindsight, be cautious of arguments that rely upon after-the-fact reasoning, and avoid the temptation to read into the prior art the teachings of the invention in issue.

45. I understand that secondary considerations of non-obviousness (also known as objective indicia of non-obviousness) may include: (1) a long felt but unsolved need; (2) commercial success; (3) unexpected results; (4) industry praise;

(5) licensing; and (6) copying by others. I also understand that there must be a relationship or nexus between any such secondary considerations and the claimed invention. I further understand that contemporaneous and independent invention by others is a secondary consideration supporting an obviousness determination.

46. I understand that any secondary consideration must bear a nexus to the claimed invention. Where the offered secondary consideration actually results from something other than what is both claimed and novel in the claim, there is no nexus to the merits of the claimed invention. I further understand that the patentee bears the burden of demonstrating that the relevant secondary indicia is attributable to the claimed invention, as opposed to other economic and commercial factors unrelated to the technical quality of the patented subject matter. I understand that a nexus is presumed where the secondary considerations are tied to a particular product which: (i) embodies the claimed invention and (ii) is coextensive with the claimed invention. In analyzing whether a product is coextensive with the claimed invention, I understand that there is no requirement for a perfect correspondence between the claims and the product, and that the presumption of a nexus can still apply when unclaimed features present in the product amount to nothing more than additional insignificant features.

47. I further understand that, as a safeguard against hindsight bias, all secondary considerations of non-obviousness must be considered prior to reaching an obviousness conclusion.

48. I understand that an obviousness evaluation can be based on a combination of multiple prior art references. I understand that the prior art references themselves may provide a suggestion, motivation, or reason to combine, but other times the nexus linking two or more prior art references can be based on the ordinary understandings available to a POSITA. I further understand that obviousness analysis recognizes that market demand, rather than scientific literature, often drives innovation, and that a motivation to combine references may be supplied by the direction of the marketplace.

49. It is further my understanding that a proper obviousness analysis focuses on what was known or obvious to a POSITA, not just the patentee. Accordingly, I understand that any need or problem known in the field of endeavor at the time of invention and addressed by the patent can provide a reason for combining the elements in the manner claimed.

50. I understand that whether a prior art reference “teaches away” from the claimed invention is a fact to be considered in determining obviousness. I understand that it is improper to combine references where the references teach away from their combination. However, I understand that the nature of the teaching is highly relevant

and must be weighed in substance – a known or obvious composition does not become patentable simply because it has been described as somewhat inferior to some other product for the same use. Furthermore, I understand that the prior art’s mere disclosure of more than one alternative does not constitute a teaching away from any of those alternatives because such disclosure does not criticize, discredit, or otherwise discourage the solution claimed.

51. For an obviousness combination, obviousness must be proven by clear and convincing evidence such that a POSITA at the time of the alleged invention would have had a reason (or reasons) for combining the teachings of those prior art references to achieve the claimed invention, and that same POSITA would have had a reasonable expectation of success from combining those teachings.

VI. LEVEL OF ORDINARY SKILL IN THE ART

52. My opinions herein are based from my standpoint of a person of ordinary skill in the art at the time of invention of the ‘634 Patent, which I refer herein as a “POSITA.”

53. I understand that, for the purposes of proceeding, the ‘634 Patent is entitled to a priority date no later than February 23, 2008, the filing date of the application leading to the ‘634 Patent (U.S. Pat. Appl. No. 12/036,243).

54. I understand that Petitioner and its expert Dr. Liu have proposed that a POSITA “would have earned a Master’s degree in electrical engineering, and at least

two years of relevant work experience in the field of integrated circuit design and manufacturing.” Pet. at 15; Ex. 1003 ¶ 57.

55. I have applied Petitioner’s proposed level of skill for my analysis. At the relevant time frame, I was a person of more than ordinary skill in the art during the relevant timeframe. However, I worked with and managed many people who fit the characteristics of the POSITA, and I am familiar with their level of skill.

VII. BACKGROUND OF TRENCHED MOSFETS

56. The ‘634 Patent is directed to improvements in the field of trench MOSFETs. ‘634 Patent, Title, Abstract, 1:5-67. In connection with my analysis and opinions herein, I will provide a brief description of the background of Trenched MOSFETs. This background information is based on my knowledge and experience, but such background information regarding MOSFETs, including trench MOSFETs can be found in various publications. *See, e.g.*, Baliga, B. Jayant, Fundamentals of Power Semiconductor Devices, 2019, ISBN 978-3-319-93988-9 (“Baliga Fundamentals”); Lutz, Josef, et al. "Semiconductor power devices." 2018, ISBN 978-3-319-70917-8 (“Lutz”); R. K. Williams, et al. "The Trench Power MOSFET: Part I—History, Technology, and Prospects," in IEEE Transactions on Electron Devices, vol. 64, no. 3, pp. 674-691, March 2017 (“Williams”).

57. There are two primary types of transistors. A transistor is a semiconductor device that can act as a switch or amplifier. The first is the Bipolar Junction Transistor (BJT) and the second is the Field Effect Transistor (FET). Transistors have three (or more) terminals—the outputs/inputs of the transistor—which typically include gate, source and drain terminals. In a transistor, changing the voltage of the gate terminal (or base current) allows varying the flow of charge (e.g., current) between the source (or emitter) and drain (or collector) (e.g., turning “on” or “off” the current flow). In a Field Effect Transistor (FET) the region of a transistor where charge can flow between the source and drain is called the “channel” region. In general, MOSFETs often offer faster switching speeds, lower conduction losses, and simpler drive circuitry compared to other types of transistors.

58. Pure semiconductor material (e.g., silicon) has a conductivity which is greater than insulators (e.g., oxides) but less than conductors (e.g., metals). However, the conductivity of regions of semiconductors can be increased by adding “doping.” Doping is the process of introducing impurities into semiconductor material (e.g., silicon) to affect its electrical properties. N-type semiconductors are created by doping a semiconductor with an electron donor element (e.g., phosphorus or arsenic). N refers to the negative charge of an electron. P-type semiconductors are created by doping a semiconductor with an electron acceptor element (e.g., boron or gallium). P refers to the positive charge of a hole—a hole is quasiparticle denoting

the lack of an electron at a position where one could exist in an atom or atomic lattice.

59. Thus, N-type and P-type doping introduce additional charge carriers (e.g., electrons or holes) and permit designers of transistor devices to control the flow of charge. For example, at a junction of P-type and N-type semiconductor materials (a so called p-n junction), current can only readily pass in one direction when forward biased—i.e., electrons pass from the N-type to the P-type material (and notional “current” goes in the opposite direction since current is the direction of positive charge, and electrons are negatively charged. A number of conventions have been adopted in the industry for referring to different magnitudes of doping. N⁺ doping is used to refer to material which has been more highly doped with electron donor impurities than N-type doping, while N⁻ doping is used to refer to material which is more lightly doped with electron donor impurities. Similarly, P⁺ doping is used to refer to material which has been more highly doped with electron acceptor impurities than P-type doping, while P⁻ doping is used to refer to material which is more lightly doped with electron acceptor impurities.

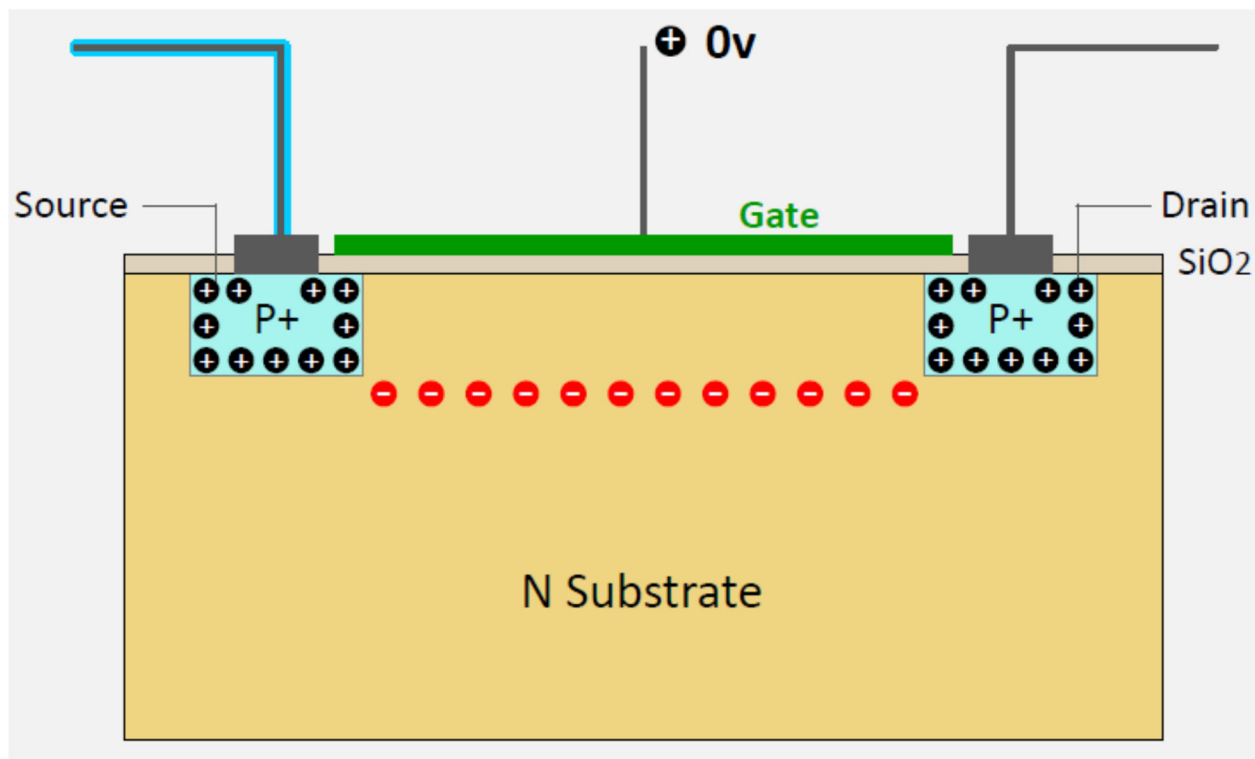
60. The term “MOSFET” refers to a metal–oxide–semiconductor field-effect transistor. In MOSFETs, a gate (originally made of metal) is physically separated from the rest of the device via an insulative “oxide” layer (i.e., the “gate

oxide”).¹ The voltage applied to the gate terminal controls the flow of charge in the channel region by using the “field effect”—i.e., the electric field created by the gate voltage attracts or repels charge carriers in or near the channel region. *Id.* In “N-Channel MOSFETs” the channel region charge carriers are electrons, while in “P-Channel MOSFETs,” the charge carriers are holes. *Id.* Some MOSFETs—called “depletion mode MOSFETs”—are designed so that charge will always flow in the channel unless a voltage is applied at the gate. Other MOSFETs—called “enhancement mode MOSFETs”—are designed so that charge will only flow in the channel when a voltage is applied at the gate. The following exemplary figures depict the operation of a P-Channel enhancement mode MOSFET.

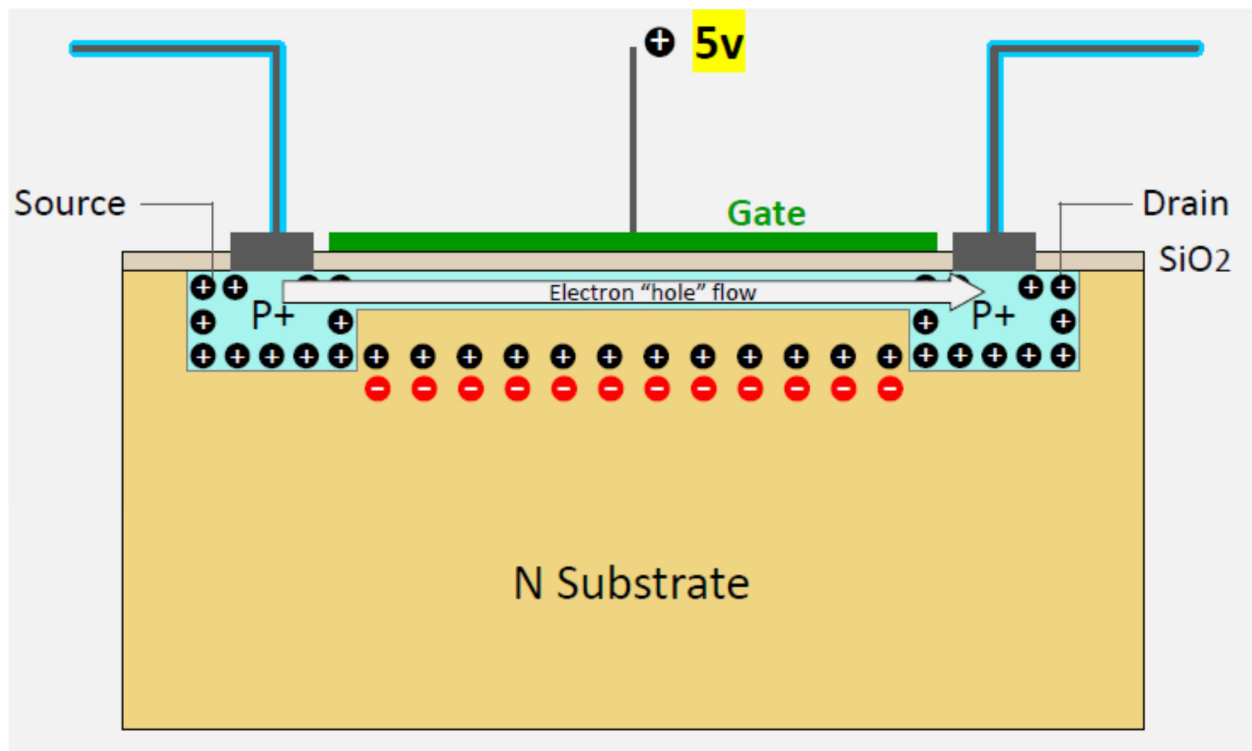
61. In the first figure, because this is a P-channel MOSFET, we have source and drain regions which are positively doped, to create a surplus of holes—positive charge carriers, whereas the body of the MOSFET has been negatively doped, creating a surplus of electrons—negative charge carriers. Because no voltage is applied to the gate terminal there is no change in the carriers in the N substrate,

¹ Subsequent MOSFET devices have used different materials for the gate, particularly polysilicon—silicon crystal which is grown to be composed of many smaller crystals—as opposed to the monocrystalline silicon typically used for semiconductor devices. Despite no longer using metal for the gate, the term MOSFET has continued to be applied in the industry for such devices because they operate by the same mechanism as the original MOSFETs.

and hence charge flow is “blocked” by the p-n junctions formed between the source and substrate and the drain and substrate of this enhancement mode device.



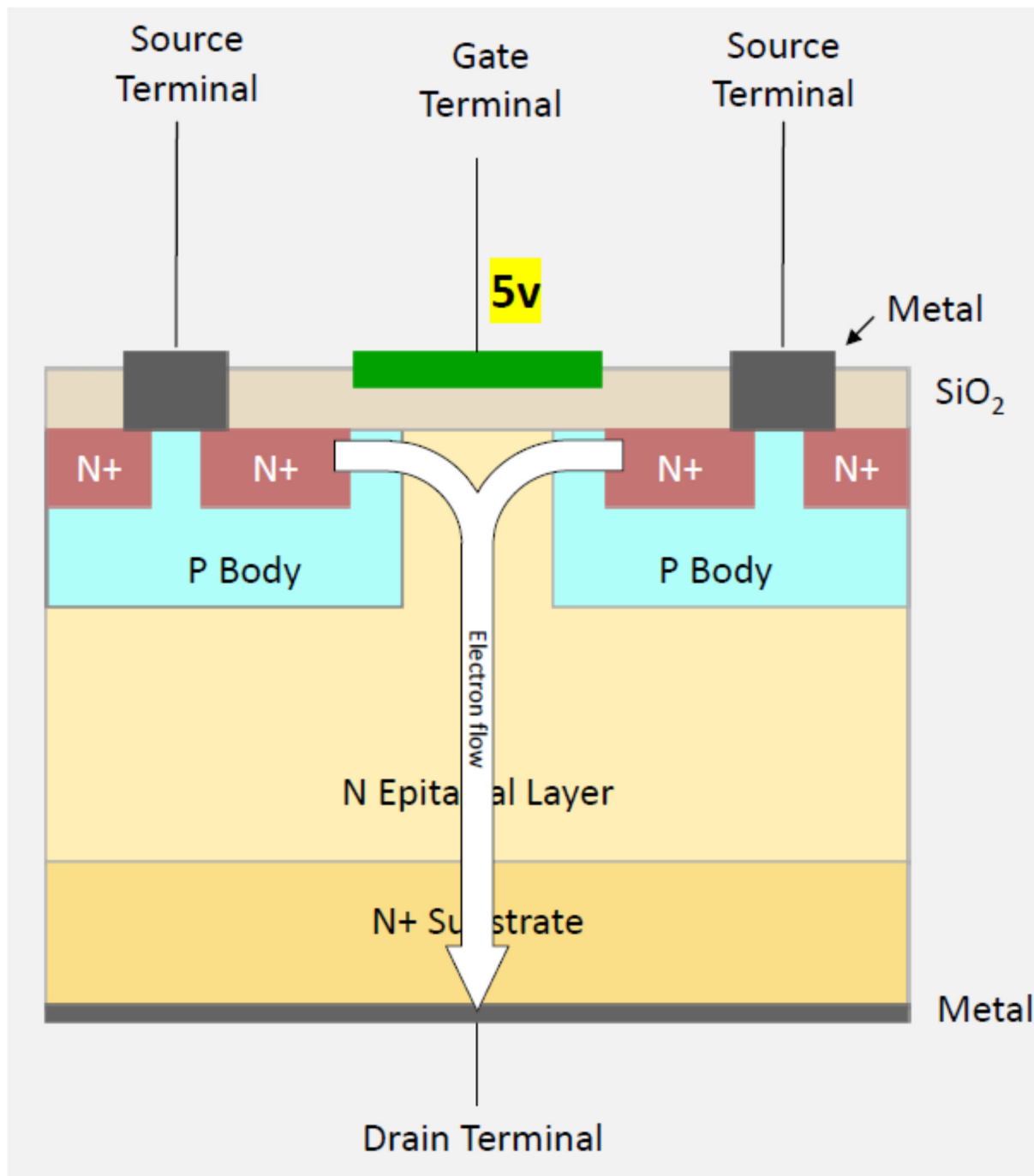
62. In the next figure, we see that a voltage has been applied to the gate terminal. This repels electrons from the region below the gate, leaving behind positive carriers and, as a result, below the channel region a depletion region (a region where substrate charge carriers have been forced away) is formed. Holes are attracted towards the gate into the channel region, creating a channel (also called an “inversion layer”) between the source and drain—a layer of holes near the gate between the two P+ regions. The channel carriers (holes) are the same as the carrier in the P+ source and drain regions. As a result, holes can flow (i.e., current) from source to drain.



63. If the gate voltage is removed, the device will return to its prior state (as illustrated in the first figure). Similar figures could illustrate the operation of N-Channel or depletion mode MOSFETs). For example, in an “N-Channel” MOSFET, the doping of each region would be reversed, and, electrons instead of holes would flow from source to drain when a channel is formed (and thus current would flow from drain to source). In a depletion-mode MOSFET, the channel region would typically have the same doping as the source and drain regions, and the channel would be present when there is no gate voltage, but the channel region would be depleted (preventing charge flow) when a voltage is applied to the gate. *Id.*

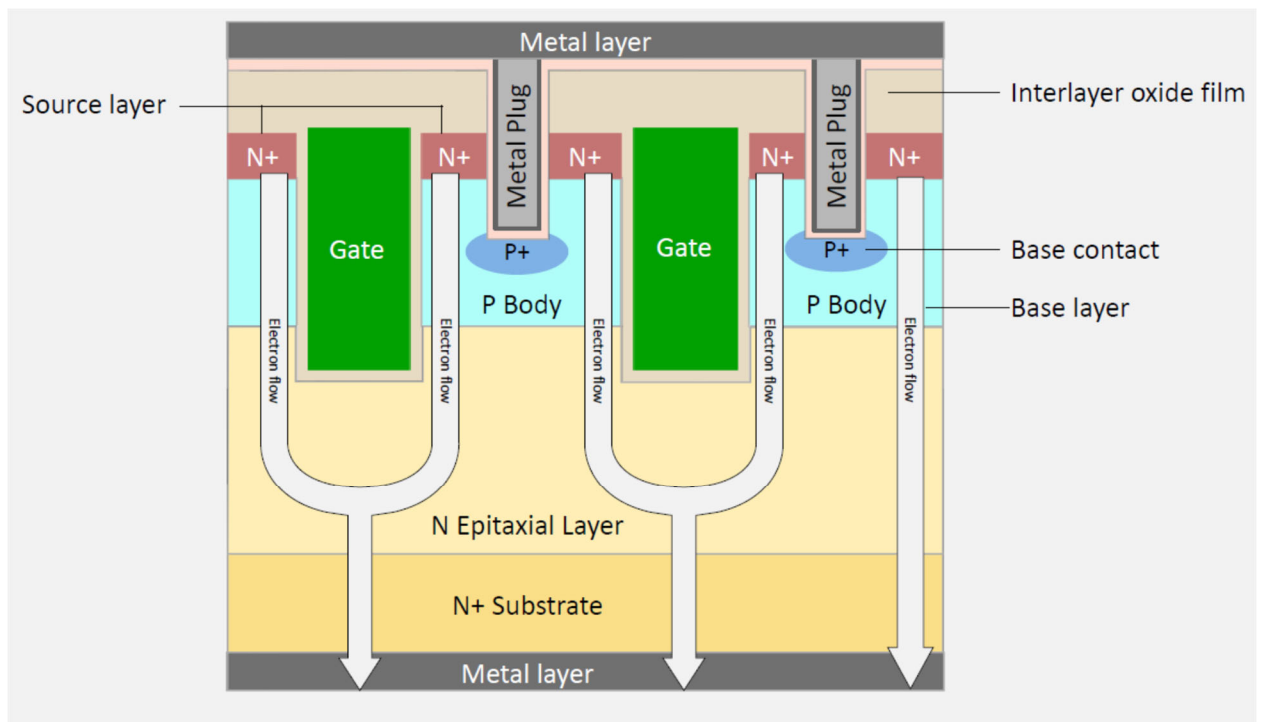
64. The above figures illustrate a lateral planar MOSFET, the original type of MOSFET—where the gate, source and drain are in a planar relationship, and the

channel runs from source to drain along that plane. To increase the current carrying capability for devices such as power MOSFETs, other designs used vertical drain electrodes (i.e., with the source and gate electrodes on the top of the chip and the drain electrode on the bottom of the chip). By using a vertical drain, the MOSFET can increase density, improving current-handling capacity and reducing $R_{DS(on)}$ (discussed below). Note that in this device the channel is not formed in the “substrate” as it is in the lateral planar MOSFET, since the substrate is now part of the drain. The source and drain still must be doped oppositely from the channel region, which is often called the “body” in the vertical MOSFET. A MOSFET with a vertical drain configuration is illustrated in the following figure:



65. Trench MOSFETs present a further improvement on the vertical drain MOSFET, by including trenches for the gate material (e.g., gate trenches). As a result, the channels form vertically along the sides of the gates. Accordingly, a

trench gate MOSFET essentially makes a chip conduct the current vertically from one surface to the other, permitting packing millions of trenches on a chip. As a result, it allows for much smaller cell pitch (and hence higher cell density), thus providing further improved current-handling capacity and reduced $R_{DS(on)}$. The following figure illustrates a trench MOSFET also having source trenches filled with metal.



66. A number of properties are important to the function and performance of MOSFETs, particularly trench MOSFETs. One of the most important properties is on-state resistance, or $R_{DS(on)}$, which is the resistance when the MOSFET is in the ON state (i.e., charge flow is occurring). Subject to other constraints, MOSFET designers generally want to minimize $R_{DS(ON)}$ because such resistance results in

conduction losses, harming the efficiency of the device (e.g., everything else being equal, a higher $R_{DS(on)}$ will result in unwanted energy usage and heat generation). MOSFETs are often compared by on-resistance-area ($R_{DS(on)} \cdot A$), as generally the larger the chip size (surface area) of the MOSFET the smaller the ON resistance. Thus, a MOSFET design with a better on-resistance-area can fit a smaller $R_{DS(on)}$ in the same package size as a device with worse on-resistance area and a higher $R_{DS(on)}$. Thus, on-resistance-area is a way for comparing MOSFET designs independent of the particular package. *Id.* $R_{DS(on)}$ performance of a MOSFET can often be improved (i.e., lowered) by increasing device density.

67. Another important property of MOSFETs is called “threshold voltage” (“ V_{th} or $V_{GS(th)}$ ”), which is the minimum voltage at the gate where the device switches between the “ON” and “OFF” states (e.g. in an enhancement mode MOSFET, the voltage where the channel forms and meaningful charge flow can occur). The threshold voltage is between gate and “body”, but since the body is normally electrically connected to the source, the gate voltage is also usually given relative to the source. A high threshold voltage can be disadvantageous for a number of reasons. For example, if the design of a MOSFET has a threshold voltage which is too high, it can reduce switching speed, and even potentially render the MOSFET unusable for low-voltage situations by being above the supply voltage (e.g., the voltage of the device’s battery).

68. Another important property is referred to as “parasitic capacitance.” In particular, capacitance is the ability of a material to store an electrical charge. In the context of a MOSFET, particularly power MOSFETs, parasitic capacitance is important because it can result in switching losses—efficiency power losses that increase as switching speed increases. In essence, these effective capacitors within the MOSFET require energy to fill to allow the MOSFET to switch between OFF and ON states, but the energy in such capacitors is dissipated without useful activity when such state switching occurs. Unlike the conductive losses from higher RDS(on), parasitic capacitances are often made worse by increasing device density.

69. Another important property of MOSFETs are parasitic structures. Parasitic structures are interactions of parts of a MOSFET (e.g., doped regions) other than the desired operation of controlling the drain-to-source charge flow using gate voltage. In particular, the structure of MOSFETs often include multiple P-N and/or N-P junctions that can interact to form other transistors, particularly a parasitic “BJT” or bipolar junction transistor within a MOSFET. A BJT is a transistor formed by P-N-P or N-P-N arrangement of doped regions, where the amount of current supplied to the “base” terminal (physically connected to the middle doped region, e.g., the body in the vertical MOSFET) controls current flow between a collector on one end of the NPN/PNP and an emitter on the other end. *Id.*

70. Related to the parasitic BJT is the phenomena of “avalanche breakdown” of a MOSFET. In the condition of avalanche breakdown, high drain-source voltages (e.g., transient voltages at turn-off that occur due to inductive loads or spike voltages) cause electrons to obtain sufficient kinetic energy to collide with atoms in the semiconductor lattice, ionizing those atoms to create holes and additional free electrons (i.e., impact ionization). Those released free electrons can, in turn, collide with other atoms in the lattice to create further holes and further free electrons, potentially resulting in an avalanching amount of charge flow. Breakdown voltage (BVDSS) refers to the reverse-bias drain to source voltage that will result in avalanche breakdown and avalanche current—even when the gate voltage would otherwise be in an “OFF” state and the channel is off. In this condition, referred to as the “breakdown region,” a small increase in drain-source voltage creates an exponential increase in current flow. In particular, when the drain-to-source voltage becomes high enough, the parasitic BJT (also called parasitic NPN) is turned on (i.e., a type of latch-up or short circuit), and a positive feedback mechanism of thermal runaway occurs where increasing temperature causes increasing current flow (even if VDSS is brought back under BVDSS). This can easily result in device destruction. Avalanche ruggedness is a property of MOSFETs that reflects the amount of avalanche current or avalanche energy a MOSFET can withstand prior to device destruction.

71. Each of these properties is important to the design and operation of a MOSFET, the applications a MOSFET is suitable for use in, and the operation of an electrical device using the MOSFET.

VIII. BACKGROUND OF THE '634 PATENT

72. The '634 patent is derived from U.S. Application Number 12/036,243, which was filed on February 23, 2008. The '634 Patent relates to trench MOSFETs with source contact trenches, where each of the source contact trenches has a lateral contact layer at a sidewall thereof. Ex. 1001 ('634 Patent), Abstract. In particular, the invention provides "a lateral contact layer in the MOSFET for avalanche improvement." *Id.* at 1: 6-8.

73. A trench MOSFET (metal-oxide-semiconductor field effect transistor) allows high current to pass through and for the channel to turn on or off using a low voltage. *Id.* at 1:11-17. The '634 Patent recognizes that, in a traditional trench MOSFET design, the sidewall of the source contact trench has no ohmic contact (due to low doping of the P base) with the contact metal plug, which results in poor ruggedness performance during Unclamp Inductance Switching tests. '634 Patent at 1:35-38. When P base resistance from the channel to the contact metal plug is high enough, device destruction can occur. *Id.* at 1:38-42.

74. The '634 Patent addresses the problem of the prior art by applying the P*-type lateral contact layer to parts of the sidewall of the source contact trench,

where the P* has less doping than the P+ base contact layer which is located at the bottom of the source contact trench. '634 Patent at 2:1-11. The '634 Patent describes optimizing the P*-type lateral contact layer doping concentration by having the ohmic contact to the barrier metal layer/the contact metal plug without significantly increasing threshold voltage of the device. *Id.* In comparison, the sidewall of a source contact trench in a prior art MOSFET has no ohmic contact with the contact metal plug. *Id.* at 1:35-38.

75. Figure 2G of the '634 Patent is reproduced below. It shows an N+-type silicon substrate (201), an N-type epitaxial layer (202), a P-type base layer (205), and an N+-type source layer (206). The gate trench (221) reaches the N-type epitaxial layer (202) through the N+-type source layer (206) and the P-type base layer (205). It is covered by the interlayer oxide film (207).

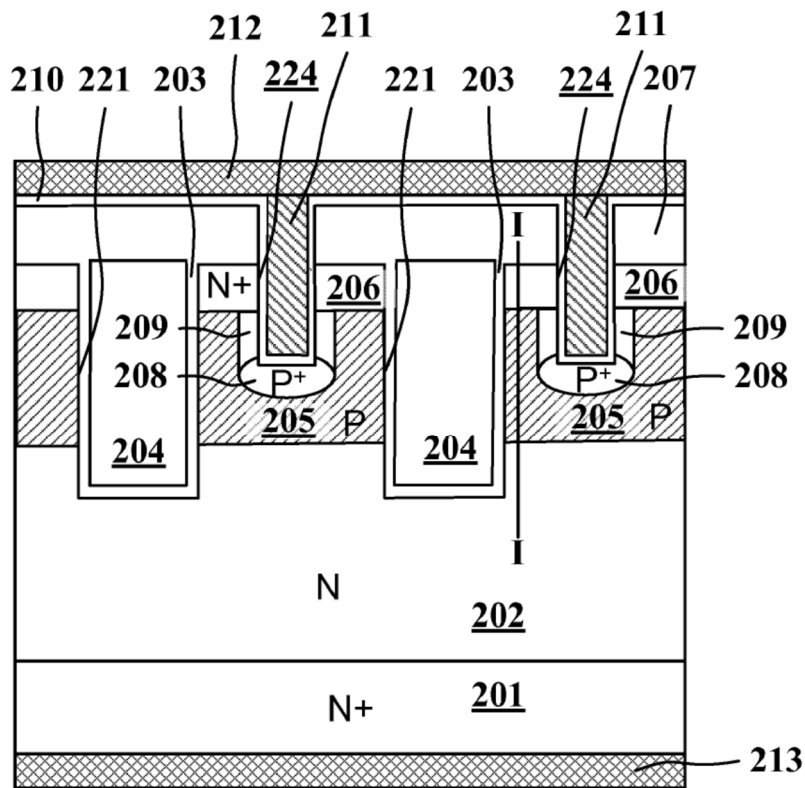


Fig. 2G

76. The source contact trenches (224) reach the P-type base layer (205) through the interlayer oxide film (207) and the N+-type source layer (206). The source contact trenches are covered by the front metal layer (212). The N-type epitaxial layer (202) forms the drain region of the trench MOSFET. The N-type trench gates (204) form the gate region of the trench MOSFET. The N+-type source layer (206) forms the source region of the trench MOSFET. The P-type base layer (205) forms the body region of the trench MOSFET.

77. The interlayer oxide film (207) is formed between the front metal layer (212) and the trench gates (204), providing insulation. The contact metal plugs

(211) penetrate through the interlayer oxide film (207) to contact the front metal layer (212). The P⁺-type base contact layer (208) is at the bottom of the source contact trenches (224). The P^{*}-type lateral contact layer (209) is at the sidewall of the source contact trenches (224). The P^{*}-type lateral contact layer (209) doping concentration is optimized to have ohmic contact to the barrier metal layer (210) and the contact metal plug (211) without significantly increasing the Threshold Voltage of the device, causing higher R_{ds}.

78. The optimized lateral contact layer doping provides good ohmic contact to the sidewall of the source contact, thus reducing the base resistance R_p between the channel and the source contact trench. This allows a higher I_{av} and a lower R_p. *Id.* at 2:23-34. The trenched MOSFET may use a Ti/TiN or Co/TiN barrier metal layer and a plurality of contact metal plugs made of Tungsten. *Id.* at 2:12-15. Though an N-channel MOSFET structure is disclosed, the conductors may be inverted for a P-channel MOSFET. *Id.* at 5:47-52.

IX. CLAIM CONSTRUCTION

A. “lateral contact layer” (’634 Patent, cl. 1)

79. In this proceeding, Petitioner and its expert have been unclear and inconsistent in how they have applied the term “lateral contact layer.” In particular, they have advanced no express construction of that term. Petitioner’s expert concluded that Hirler disclosed a lateral contact layer because “the purpose of the

body amplification zone is the same as the lateral contact layer—i.e., to achieve the intended avalanche breakdown voltage capability, without it being degraded through the turning on the of NPN parasitic bipolar transistor.” Ex. 1003 ¶ 73. With respect to Shiraishi, Petitioner’s expert opines that a “POSITA would understand that this region acts as a lateral contact layer to prevent punch-through.” Ex. 1003 ¶ 107. However, neither of those discussions have any apparent relevance to the words of the phrase “lateral contact layer,” but instead appear to assume an entirely functional scope for “lateral contact layer.” Nor are they even the same—the punch-through effect refers to the condition where, due to increased drain voltage, the depletion region at the body-drift p-n junction reaches toward the depletion region around the source region, reducing the potential barrier between them. Although related, punch-through is distinct from turning on avalanche breakdown or turning on the NPN parasitic. Ex. 2015 (Zhang, Ruizhe, and Yuhao Zhang. "Power device breakdown mechanism and characterization: Review and perspective." Japanese Journal of Applied Physics 62.SC (2023): SC0806) at 2-4.

80. By contrast, I understand that, in the preliminary response in this IPR, Patent Owner argued that “lateral contact layer” should mean “a region of dopant which is implanted into sidewalls of the source contact trenches to have a dopant concentration between P and P+ (“P* doping”) for an N-channel MOSFET or between N and N+ (“N* doping”) in a P-channel MOSFET.” Paper No. 7 (Prelim.

Resp.) at 4-8. I also understand that the District Court in *Force Mos Technology Co., Ltd. v. ASUSTeK Computer, Inc.*, No. 2:22-cv-00460-JRG (E.D. Tex.) adopted the same construction. Ex. 2011 at 49-50. Notably, in that proceeding, ASUSTeK Computer (who I understand is a real-party-in-interest in this IPR), proposed that the term be construed as “requiring a region of dopant which is implanted into sidewalls of the source contact trenches, wherein implantation may occur before or after the source contact trenches are etched, the region to have a doping concentration between the base layer doping concentration and the base contact layer doping concentration.” Ex. 2011 at 47. I understand that that Court’s opinion in the *ASUSTeK* case was in part based on Patent Owner’s submission of such construction in its preliminary response in this IPR. *Id.* 49. However, the Court also stated that it “agree[d] that the specification discloses implanting a P*-type lateral contact layer into the sidewall of the source contact trenches, where P* has more doping than the P base layer, but less doping than the P+ base contact layer which is located at the bottom of the source contact trench.” *Id.* at 48-49 (citing ‘634 Patent at 2:1-11).

81. Because of the parties’ differences in position regarding claim scope, and because of the unclear and apparently inconsistent meanings of “lateral contact layer” applied by Petitioner and its expert, and because of the term’s lack of ordinary meaning in the field (as discussed below), it is my opinion that a construction of “lateral contact layer” is necessary to address the issues in this IPR.

82. I understand that, in the Board’s institution decision in this IPR, the Board “preliminarily determine[d] that the phrase ‘lateral contact layer’ does not require ‘a dopant concentration between P and P+ (P* doping) for an N-channel MOSFET or between N and N+ (N* doping) in a P-channel MOSFET.’” Paper No. 13 at 12. I also understand that the Board “preliminarily determine[d] that the phrase ‘lateral contact layer’ does not require ‘a region of dopant which is implanted into sidewalls of the source contact trenches.’” Paper No. 13 at 13. I respectfully disagree with the Board’s preliminary constructions, and I believe that the construction proposed by Patent Owner, and adopted by the Court in the *ASUSTeK* case, is the appropriate construction of “lateral contact layer.”

83. As a threshold issue, it is my opinion that the term “lateral contact layer” has no established meaning in either the field of trenched MOSFETs or the field of semiconductors more generally. Instead, it is my opinion that “lateral contact layer” is a coined term used by the patentee for referring to the novel invention disclosed in the specification. Prior to my work on Force MOS matters, I had never heard the term “lateral contact layer” used in connection with MOSFETs or BJTs in the relevant time period (e.g., prior to 2008). Nor does the term appear in relevant technical dictionaries or glossaries. *See, e.g.,* Ex. 2016 (Semiconductor Glossary) at 145-146 (no definition of “lateral contact layer”). Running an articles search for “‘lateral contact layer’ MOSFET” in Google Scholar (scholar.google.com), only

returns only a single article, from well after the issuance of the ‘634 Patent: Wang, Jingshan. High-Power Vertical GaN Electronic Devices Formed by Epitaxial Lift-Off. Diss. University of Notre Dame, 2018. Ex. 2017 (google scholar search result). Moreover, rather than demonstrating an established ordinary meaning, the Wang article also indicates that the authors were using “lateral contact layer” as a coined term. In particular, the author of the Wang article use the phrase “1 μm highly doped n-GaN lateral contact layer” to refer a layer (of a diode) that is planar and underneath another layer and a pair of ohmic contacts (as opposed to the to a layer to the side of something else). Ex. 2018 (Wang article) at p. 54, *available at* https://curate.nd.edu/articles/thesis/High-Power_Vertical_GaN_Electronic_Devices_Formed_by_Epitaxial_Lift-Off/24825441/1/files/43666500.pdf. That is, the Wang article uses “lateral” in “lateral contact layer” in the sense of “extending from side to side” rather than “of or relating to the side,” which are two different potential definitions of “lateral.” See Ex. 2019 (<https://www.merriam-webster.com/dictionary/lateral>). Based on my experience, the Wang article is only one example of the use of the word “lateral” in this manner in the field of semiconductors.

84. I understand in the Institution Decision, the Board stated:

The specification may provide controlling definitions or context necessary to avoid ambiguities, but only as needed and not at the expense of the actual claim

language. Context for avoiding ambiguities is not on the table, because Patent Owner does not contend that the phrase “lateral contact layer” is ambiguous, and we discern no ambiguity in that term on this record. Prelim. Resp. 4–8.

We find especially significant, on the point of ambiguity, that Patent Owner admits that the plain and ordinary meaning of “‘layer’ on its own is quite broad, meaning ‘a region having unique electrical properties (e.g., n layer).’” *Id.* at 5. Against that backdrop, we are hard pressed to discern any ambiguity in the meaning of the term “lateral contact layer,” which plainly indicates a lateral contact region having unique electrical properties. Patent Owner does not explain why the word “layer” in the claim phrase “lateral contact layer” should be read to convey a different and narrower meaning than “‘layer’ on its own.” *Id.*

Paper No. 13 at 9-10 (case citations omitted).

85. As the relevant law of claim construction has been explained to me by counsel, it is not my understanding that the role of a patent’s specification in claim construction is limited solely to “provid[ing] controlling definitions or context necessary to avoid ambiguities.” However, even if it were, I do believe that Patent Owner’s construction of “lateral contact layer” is needed to provide context necessary avoid potential ambiguities that could arise to a POSITA that did not consider the specification of the ‘634 Patent in informing the appropriate construction of “lateral contact layer.”

86. First, as discussed above with regards to the “Wang” article, there is a potential ambiguity with respect to the term “lateral” in “lateral contact layer” (if

one were not to refer to the specification of the ‘634 Patent). One meaning of “lateral” is “of or relating to the side.” Ex. 2019 (<https://www.merriam-webster.com/dictionary/lateral>). Another meaning is “situated on, directed toward, or coming from the side.” *Id.* These meanings are consistent with the specification of the ‘634 Patent, where the “lateral contact layer” is located on the sidewalls of the source contact trenches in the base layer. ‘634 Patent at 1:65-67, 3:55-65, Fig. 2G (element 209), cl. 1. However, another meaning of “lateral” is “extending from side to side.” Ex. 2019 (<https://www.merriam-webster.com/dictionary/lateral>). As discussed above, that is how “lateral” is used in the term “lateral contact layer,” in the Wang article (the only article returned by searching “‘lateral contact layer’ MOSFET” in Google Scholar). Indeed, similar to the structure of the diode in the Wang article, lateral MOSFETs are a well-known type of MOSFET to those of skill in the art. However, lateral MOSFETs are referred to as *lateral* because they are predominantly a lateral, surface-effect device having side-to-side current flow, rather than vertical current flow. *See* Ex. 2016 (Semiconductor Glossary) at 146 (“**lateral transistor** a bipolar transistor (BJT), typically p-n-p, in which current flows across the base in the direction parallel to the wafer surface ...”). Thus, this is another sense of “lateral” in the field (side-to-side current flow, rather than the relationship between structures).

87. The side-to-side current flow sense of “lateral” in “lateral MOSFET” also relates to a potential ambiguity in the word “contact.” In the field of semiconductors, “contact” can refer to the state of physical contact (i.e., two structures in the semiconductor are arranged to touch each other). Ex. 2021 (<https://www.merriam-webster.com/dictionary/contact>) at 1 (“union or junction of surfaces.”); *see also* Ex. 2016 (Semiconductor Glossary) at 139 (“junction in semiconductor materials and devices a region in which two materials featuring different work functions are brought to contact”). “Contact” can also refer to the state of electrical contact, such as ohmic contact (i.e., having a linear current-voltage relationship consistent with Ohm’s law, such as between metals), or non-ohmic contact (i.e., having non-linear current-voltage curves, such as a p-n junction). Ex. 2016 (Semiconductor Glossary) at 180 (ohmic contact). However, in addition to the state or condition of having contact, “contact” can also refer to a structure having that state, thus “ohmic contact” can refer to a structure that has the condition of ohmic contact, and “non-ohmic contact” can refer to a structure that has the condition of non-ohmic contact. Another sense of “contact” is to refer to distinct structures (often metal) used to electrically interface parts of a semiconductor with a metal interconnect layer, typically through a hole in an insulative layer, e.g., the trench source contacts of the ‘634 Patent. Ex. 1001, Title, Abstract, Figs. 1 (element 111), 2G (element 211); Ex. 2022

(<https://www.lamresearch.com/technical-glossary/>) (“CONTACT the conductive connection between the transistor and the first interconnect layer”).

88. In my opinion, if a POSITA were to attempt to understand the meaning of claim 1’s “lateral contact layer” without reference to the specification of the ‘634 Patent, these various meanings of “contact” could create a potential ambiguity. For example, a POSITA would recognize that “contact” could refer to the metal contacts within the source contact trenches—potentially suggesting that the “lateral contact layer” is part of the filling of those trenches, i.e., part of the contact and covering the sidewalls of the source contact by filling such trenches. Or, a POSITA could understand “lateral contact layer” as referring to a layer *contacting* the trenched source contacts. A POSITA would also recognize that “contact” could also refer to a functional purpose, i.e., the sense of a layer for improving electrical contact.

89. There is also a potential ambiguity with respect to the term “layer” in “lateral contact layer” if one were not to refer to the specification of the ‘634 Patent. As an initial issue, the term “layer” in semiconductors most typically refers to a portion of a semiconductor device constituting a distinct material that has been deposited together as part of a single step in the semiconductor process, or resulting from a distinct process is applied across the surface of a semiconductor, and may be on top of or underneath other layers. *See, e.g.,* Ex. 2023 (<https://www.merriam-webster.com/dictionary/layer>) (“one thickness, course, or fold laid or lying over or

under another”); Ex. 2024 (U.S. Patent No. 3025589 at 3:42-5:8). Because semiconductors typically use the planar process, such layers typically extend from side-to-side in the wafer, except where they are interrupted by other processes (e.g., etched trenches, which may be filled with conductive material to form contacts), or where a mask has been used to limit a process to only a portion of the plane. *Id.* The result of the planar process is a cross-section that typically looks somewhat like geological strata.

90. However, reading claim 1 of the ‘634 Patent, it would be apparent to the POSITA that the term “lateral contact layer” is not using “layer” in the sense of a planar layer of material formed during a step of the semiconductor process. Indeed, the structure and organization of claim 1 draws a clear contrast between the layers recited in limitation 1.a (i.e., the “epitaxial layer,” the “base layer,” the “source layer”), which are disposed on top of each other in a specific order and the “lateral contact layer,” which is only mentioned in limitation 1.g, and is recited as being located *within* another layer (i.e., the base layer). Given this, and the nature of the planar process, a POSITA reviewing the claim text (without reference to the specification) would not understand “lateral contact layer” as likely indicating a layer of material physically deposited together at the same time.

91. Another sense of “layer” in semiconductors refers to a portion of the semiconductor formed during a particular step of the process, even if not deposited.

Ex. 2007 (Semiconductor Glossary definition of layer). Thus, “ion” implantation can create a “source layer” in a semiconductor device, even though the semiconductor material that makes up that source layer was already deposited before the ion implantation procedure. *Id.*; *see, e.g.*, Ex. 1008 (Kobayashi 174), [0058]. However, given that the claims of the ‘634 Patent are apparatus claims, a POSITA would expect the “lateral contact layer” to be some structure in the MOSFET that is created as a step in the semiconductor process that is structurally reflected in the final device. Moreover, a POSITA would recognize that claim 1 of the ‘634 Patent recites various “layer[s]” and “region[s],” and that a POSITA would believe that using the term “layer” (as opposed to region) would likely be an intentional choice, such as consistent with the common dictionary definition of “layer” as a “thin sheet of a substance.” Ex. 2025 (<https://dictionary.cambridge.org/us/dictionary/english/layer>). Given the various potentially relevant meanings of “layer,” a POSITA would naturally turn to the specification to understand the scope and meaning of “lateral contact layer.”

92. Another potential ambiguity relating to “lateral contact layer” that would be apparent to a POSITA without referring to the specification, is that interpreting the phrase as simply being a layer lateral to (to the sides of) the source contact trenches would fail to distinguish the claimed “lateral contact layer” from the claimed “base layer.” In particular, claim 1 of the ‘634 Patent recites “a plurality

of source contact trenches ... extending downwardly through said source layer to a portion of said base layer.” Thus, the base layer is, to some degree, necessarily lateral to the source contacts. However, the claim’s choice to introduce the “lateral contact layer” as another term, separate from the “base layer,” indicates that the “lateral contact layer” is something different from the “base layer,” but the text of the claim itself provides no clue *how* the scope and meaning of lateral contact layer is different from the base layer.

93. Similarly, in my opinion, an affirmative construction of “lateral contact layer” is needed to distinguish claim 1 from the admitted prior art in the specification of the ‘634 Patent. In particular, as indicated by comparing Fig. 1 of the ‘634 Patent (admitted prior art) and Fig. 2G, the only difference between the admitted prior art and the embodiment of Fig. 2G is the presence of element 209, the lateral contact layer, in Fig. 2G. However, notably, admitted prior art Fig. 1 of the ‘634 Patent does have *a* layer lateral to the source contact trenches, contacting the source contacts, i.e., base layer 105. ‘634 Patent, Fig. 1. In my opinion, a POSITA reading the ‘634 Patent would reject a construction of “lateral contact layer” as simply being any layer lateral to (to the side of) the source contact trenches because that construction would fail to distinguish the admitted prior art of Fig. 1.

94. Moreover, in my opinion, a construction of “lateral contact layer” is needed to distinguish the “lateral contact layer” from the “base contact layer.” In

particular, it is clear from the text of claim 1 of the ‘634 Patent that both the “lateral contact layer” and the “base contact layer” cover portions of the source contact trenches. However, the recitation of the separate terms “lateral contact layer” and “base contact layer” would indicate to a POSITA that those terms have different meanings—if not, the patentee could easily have instead recited that the source contact trenches in the base layer are covered by *a* contact layer. Again, however, the text of the claim itself provides no clue *how* the scope and meaning of lateral contact layer is different from the base contact layer.

95. I also understand that, in the institution decision, the Board stated:

Furthermore, claims 2 and 6 depend from claim 1, and both expressly specify that “the lateral contact layer has less doping concentration than the base contact layer at bottom.” Ex. 1001, 6:22–23, 6:36–37. Claims 2 and 6 show that the patentee knew how to use words in a claim to impose a dopant concentration limitation on the lateral contact layer, but included no such language in claim 1.⁷ *See id.* at 6:15, 6:22–23, 6:36–37 (claims 1, 2, and 6).

Patent Owner does not address the principle of claim differentiation, under which “limitations stated in dependent claims are not to be read into the independent claim from which they depend.” To be clear, on this record, we discern no distinction, and the parties identify none, between the dopant concentration limitation that Patent Owner contends is present in claim 1, and the dopant concentration limitations specified in claims 2 and 6. The doctrine of claim differentiation “is at its strongest ‘where,’” as here, “the limitation sought to be ‘read into’ an independent claim already appears in a dependent claim.” On this record, therefore, we preliminarily determine that Patent Owner requests a

construction of the term “lateral contact layer” that renders redundant dependent claims 2 and 6.

Paper No. 13 at 11-12 (case citations omitted).

96. Respectfully, I disagree with the Board’s apparent conclusion that Patent Owner’s proposed construction would render claims 2 and 6 redundant of claim 1. In particular, each of claim 2 and 6 recite limitations that are plainly not required by claim 1 under Patent Owner’s construction. In particular, claim 2 recites “the silicon substrate, the epitaxial layer, and the source layer are N-type; the base layer and lateral contact layer are P-type; and each of the source contact trenches further has a P-type base contact layer at a bottom thereof.” That is, claim 2 recites that the trenched MOSFET of claim 1 is an N-type MOSFET.² Similarly, claim 6 recites “the silicon substrate, the epitaxial layer, and the source layer are P-type; the base layer and lateral contact layer are N-type; and each of the source contact trenches further has a N-type base contact layer at a bottom thereof.” That is, claim 6 recites that the trenched MOSFET of claim 1 is a P-type MOSFET. However, even under Patent Owner’s construction of “lateral contact layer,” claim 1 does not

² An N-Type MOSFET, also called an n-channel MOSFET or NMOS, use the field effect to induce an n region (the channel) in an ON state, whereas the channel region is p-type (due to doping) during an OFF state. By contrast, a P-type MOSFET (or p-channel MOSFET or PMOS) induces a p region (the channel) in an ON state, whereas the channel region is n-type (due to doping) during an OFF state. Thus, an N-type MOSFET will have P-type doped body / base layer, and a P-type MOSFET will have an N-type doped body / base layer. In each, the source and drain regions or layers will be of opposite doping as the body / base layer.

require that the MOSFET be a P or N type MOSFET. Indeed, Patent Owner's construction of "lateral contact layer" is expressly consistent with either N-type or P-type MOSFETs.

97. Claims 2 and 6 of the '634 Patent also recite "the lateral contact layer has less doping concentration than the base contact layer at bottom." As a threshold issue, it is my opinion that a POSITA would understand the reference to "doping concentration" in claims 2 and 6 as a strong indication that the defining property of claim 1's "lateral contact layer" is its doping concentration—but such doping concentration is not recited in claim 1. Thus, a POSITA would naturally turn to the specification to understand the "doping concentration" required by the "lateral contact layer."

98. Moreover, I do not believe that Patent Owner's construction of "lateral contact layer" would render redundant the language of claim 2 and 6 that "the lateral contact layer has less doping concentration than the base contact layer at bottom." In particular, Patent Owner's construction of "lateral contact layer" does not require that the *base* contact layer have any particular doping concentration—it does not mention the base contact layer at all. Nor do I believe that the term "base contact layer" is necessarily limited to P⁺ doping (for N-channel MOSFETs) or N⁺ doping (for P-channel MOSFETs). Thus, Patent Owner's construction—requiring P* or N* doping for the lateral contact layer—would not render claim 2 and 6's requirement

that the “base contact layer” have a higher doping concentration than the lateral contact layer to be redundant.

99. Accordingly, I believe the appropriate construction of “lateral contact layer” to be “a region of dopant which is implanted into sidewalls of the source contact trenches to have a dopant concentration between P and P+ (“P* doping”) for an N-channel MOSFET or between N and N+ (“N* doping”) in a P-channel MOSFET.” *See* ‘634 Patent, 2:1-11, 4:3-6, Figs. 3B, 2G.

B. “the sidewalls of said trenches in said base layer” (‘634 Patent, cl. 1)

100. I understand that Petitioner and its expert have argued that “the sidewalls of said trenches in said base layer” should be construed to mean “entire sidewalls of said trenches in said base layer.” Pet. at 17-19; Ex. 1003 ¶¶ 60-62. In particular, they argue that the applicant, during prosecution, disclaimed coverage other than of the entire sidewalls as part of an examiner interview where the examiner asserted the Kobayashi reference (U.S. Patent No. 6,888,196, Ex. 2008), whose published patent application is Exhibit 1008. *Id.* (citing Ex. 1002 at 27, 29). They also argue that the specification of the ‘634 Patent similarly requires coverage of the entire sidewalls. Ex. 1003 ¶ 60 (citing ‘634 Patent at 1:33-35, 1:43-45, 5:9-12, Figs. 1, 2G).

101. I also understand that two District Courts have likewise construed the same or similar claim language of the ‘634 Patent as requiring that the lateral contact

layer cover the entire sidewalls in the base layer, based on similar arguments. Ex. 1017 at 6-9; Ex. 2011 at 23.

102. I understand that, in the Board’s institution decision in this IPR, the Board determined that “no express construction of that term is necessary to resolve whether to institute review.” Paper No. 13 at 8. I believe that a construction of this term is necessary in this IPR, particularly to address Petitioner’s Ground No. 3 (alleged anticipation by Shiraishi), Ground No. 4 (alleged obvious over Shiraishi in view of Kobayashi) and Ground No. 5 (alleged obvious over Kobayashi in view of Shiraishi). In particular, as discussed in further detail below, neither Shiraishi nor Kobayashi disclose or suggest an alleged “lateral contact layer” as covering the entire sidewalls of the source contact trenches in the base layer.

103. Accordingly, for the purposes of this declaration, I have applied Petitioner’s proposed construction of “the sidewalls of said trenches in said base layer” should be construed to mean “entire sidewalls of said trenches in said base layer,” i.e., that the lateral contact layer (whose construction is discussed above) must cover the entire sidewalls of the portions of the source contact trenches that are in the base layer.

X. THE CHALLENGED CLAIMS OF THE '634 PATENT ARE NOT ANTICIPATED AND ARE NOT RENDERED OBVIOUS

A. Overview of the Prior Art Relied Upon for the '634 Patent

1. German Patent Publication No. DE 102004009083 (“Hirler”)

104. The Hirler reference is dedicated to the problem of setting the “depth of the contact zone” in trench MOSFETs with trench source contacts. Ex. 1006 (Hirler), [0003]. Hirler describes that, in avoiding avalanche breakdown due to the intrinsic NPN parasitic bipolar transistor in such MOSFETs, it was known that a body contact zone helps ensure adequate contact between the source and body without causing a voltage drop. *Id.*, [0002]. But, if the contact zone is too shallow it will not effectively clamp the breakdown, while if the contact zone that is too deep, there will be too much reduction in breakdown voltage. *Id.* at [0003]. Thus, Hirler attempts to address avalanche breakdown “without precisely defining the depth of the body contact zone.” *Id.* at [0007]. It does this by including a “body amplification zone” that “contains at least parts of the body contact zone.” *Id.* at [0008].

2. U.S. Patent Publication No. 2004/0021174 (“Kobayashi 174”)

105. Kobayashi 174 is directed to improving prior art designs of trench MOSFETs where the P⁺-type contact layer is formed at the bottom of the contact hole, the impurity (i.e. dopant) concentration in a channel region is increased by lateral or horizontal diffusion, which limits how much cell size may be reduced. Ex. 1008 (Kobayashi 174), [0014]-[0016]. Additionally, it attempts to address the

problem of adequately filling contact holes in a single step of front side metallization with aluminum without causing an irregular surface profile of the source metal layer. *Id.* at [0013]. Kobayashi 174 addresses these problems in two main ways. In the first method, Kobayashi ensures the depth of the source contact trench (and thus the location of the implantation of the P+ contact layer) is set to a precise depth which is different from the depth in the base layer where dopant concentration is the highest. *Id.* at [0018]-[0019], [0025], Figs. 5A, 5B, 7C. As a result, impurities from the P+ base contact layer (which is injected into the bottom of the contact trench before metallization) are less likely to leach into the channel region and increase threshold voltage. *Id.* at [0037]. In the second method, Kobayashi introduces a metal silicide layer around the source contact's bottom and sidewalls to suppress source contact resistance. *Id.* at [0022], [0070]-[0071], Figs. 10, 11A (element 15). Kobayashi also discusses a source metallization process where Tungsten plugs are added (*Id.*, Fig. 8A) followed by a planarization process (*Id.*, Fig. 8B), followed by back side metallization with aluminum (*Id.*, Fig. 8C).

3. U.S. Patent Publication No. 2005/0029584 (“Shiraishi”)

106. Shiraishi is directed to improving on-resistance and reducing punch-through of trench MOSFETs. Ex. 1009 (Shiraishi), Abstract. Shiraishi identifies a problem with prior trench gate MOSFETs in that the gate insulator of deep trench gates may increase capacitance. *Id.*, [0007], [0013]. This capacitance may be

addressed by narrowing the trench gates and reducing the extent of penetration of the gate trenches into the drift layer. *Id.* at [0013]. However, making the trench gates too narrow can increase on-resistance, and making the trench gates—and thus the interface between the body and drift regions—too shallow can result in a short channel effect, resulting in depletion in the channel layer and punch-through (i.e., partial breakdown as depletion region located at the body-drift layer interface extends to connect to the depletion region at the source-body interface as V_{ds} increases). *Id.* at [0014], [0080], [0085], Fig. 14. Shiraishi notes that, although punch-through could be mitigated by increasing the doping concentration throughout the body region, that would result in significantly increased threshold voltage. *Id.* at [0015]. Shiraishi attempts to address these problems by the introduction of a thin punch-through stopper layer, having the same doping type as the body but a higher degree of doping, located immediately at a depth immediately below the source layer, and that extends laterally between the gate trenches and source contact trenches. *Id.*, Fig. 9, [0080]-[0081], claim 22. The punch-through stopper layer allows the channel to be shorter, allowing the gate trench bottoms and body-drift interface located at a shallower depth, thereby improving capacitance. *Id.*

B. Claims 1-2 and 6 of the '634 Patent Are Not Anticipated by Hirler

107. Petitioner contends, and Dr. Liu opines, that claims 1-2 of the '634 Patent are anticipated by the Hirler reference (DE 102004009083). As set forth below, I disagree.

1. Claim 1

- a) [1.a]. “a semiconductor region having a drain region, a body region and a source region, comprising, a silicon substrate, an epitaxial layer corresponding to said drain region disposed on the top of said silicon substrate, a base layer corresponding to said body region disposed on the top of said epitaxial layer, and a source layer corresponding to said source region disposed on the top of said base layer;”*

108. In my opinion, the cited disclosures do not demonstrate that Hirler anticipates limitation 1.a of the '634 Patent.

109. In particular, Dr. Liu opines that the claimed “epitaxial layer corresponding to said drain region” is disclosed by Hirler’s “n- drift zone 11.” Liu Declaration, ¶ 66. An epitaxial layer refers to a semiconductor layer created via the process of epitaxy. Ex. 2016 (Semiconductor Glossary) at 85 (“**epitaxial layer** a layer grown as a result of epitaxial deposition, or epitaxy ... **epitaxy** an ‘ordered deposition’; a process by which thin layer of single crystal material is deposited on single-crystal substrate.”). However, Dr. Liu provides no explanation or analysis why he concludes that a person of ordinary skill in the art would understand Hirler’s n- drift zone 11 as inherently or necessarily being a layer created by epitaxy (i.e.,

grown on top of an existing semiconductor wafer). Similarly, the petition provides no explanation for why it contends that Hirler’s “n- drift zone 11” is necessarily an epitaxial layer. Pet. at 23-24.

110. Indeed, nowhere in Hirler is there a mention of “epitaxial” or “epitaxis” or similar words. Moreover, Hirler does not contain any description of how the “n- drift zone” was created. To the contrary, Hirler expressly states that its “starting point” has “an n+ substrate 10 of silicon [and] an n- drift zone 11,” and then only discusses manufacturing steps *after* that starting point. Ex. 1006, [0018]; Ex 1005, Figs. 1A, 2A. Accordingly, in my opinion, Hirler does not expressly disclose that n- drift zone is an epitaxial layer. I understand anticipation requires a showing that each element is expressly or inherently present in the limitation. However, Dr. Liu’s report makes no effort to articulate any reason why Hirler’s n- drift zone 11 must inherently be an epitaxial layer. I also note that Dr. Liu has not articulated any obviousness theory with respect to Hirler and the “epitaxial layer” limitation. Accordingly, in my opinion, Dr. Liu has failed to demonstrate that Hirler anticipates or otherwise renders invalid limitation 1.a.

111. For the purposes of disclosure, in connection with an infringement report in the *Force MOS v. ASUSTek* district court litigation, I opined that all components of limitation 1.a are necessary for the operation of a trench MOSFET at the relevant time period in that litigation (i.e., for a lawsuit filed in November

2022 and addressing products sold potentially up to six years before that). In the modern MOSFET market, commercial trench power MOSFETs are almost invariably produced from pre-doped epi-wafers provided by substrate vendors (i.e., an already existing doped epitaxial wafer and substrate are provided to the semiconductor fab). However, I am not aware of the same being *necessarily* true at the time of Hirler (February 2004) or the filing date of the ‘634 Patent in February of 2008.

112. I understand that, during redirect during Dr. Liu’s deposition, Dr. Liu, for the first time, attempted to advance an inherency argument for this limitation, arguing that Hirler’s “n- drift zone” must be created by epitaxy, because he argues that it would be impossible to otherwise create a more lightly doped layer on top of a more heavily doped layer. Ex. 2014 (Liu Depo.) at 164:16-165:20 (“it’s not going to be possible to implant, to make an implant substrate on the bottom and then a layer with actually lighter doping layer on top”). In my opinion, even if Petitioner is allowed to rely on such a theory, Dr. Liu’s new inherency argument is without merit. In particular, there are a number of ways that the configuration of an n- doped drift zone on top of an n⁺ substrate could have been created without epitaxial growth.

113. Another alternative way for creating an N- layer on top of an N⁺ layer (as disclosed in Hirler)—without epitaxy—would be to use “counter-doping.” Counter-doping is the process of introducing dopants of the opposite type to an

already doped region of semiconductor material. *See, e.g.*, Ex. 2026 (Suzuki, Kunihiro, A. Satoh, and T. Sugii. "Counter doping into uniformly and heavily doped channel region of sub-0.1 μm SOI MOSFETs." IEEE Electron Device Letters 17.1 (1996)) at 1-3, Ex. 2027 (U.S. Patent No. 4,315,781, Fig. 1c, 3:64-4:13). As applied to Hirler, the N- epitaxial layer could be created by counter-doping via a process where, on the top (i.e., front side) of an N⁺ doped silicon substrate, P-type dopants are introduced, such as via diffusion or ion implantation. *See id.* (both examples of creating a more lightly doped layer on top of a more heavily doped layer via counter-doping). The introduction of P-type dopants has the effect of reducing the net number of negative charge carriers (e.g., from N⁺ to N⁻). Controlling the depth of such a procedure and the degree of counter-doping could ensure that an N- drain layer remains on the front side, while an N⁺ is present on the backside.

114. One alternative way for creating an N- layer on top of an N⁺ layer (as disclosed in Hirler)—without epitaxy—would be to use “backside doping.” That is, in a separate doping step from the doping procedure used to create the N- drain layer (and prior to backside metallization), introducing heavy N doping into the bottom (or backside) of the substrate using diffusion or ion implantation. *See* Ex. 2028 (U.S. Patent No. 8,884,409 at 3:35-4:8). Controlling the depth of such a procedure and the degree of backside doping (e.g., by diffusion time and/or implant dose) could

ensure that an N- drain layer remains on the front side, while an N+ is present on the backside.

115. Accordingly, in my opinion, Hirler neither expressly nor inherently discloses all of the limitations of limitation 1.a. of claim 1 of the '634 Patent.

b) [1.g]. “wherein the sidewalls of said trenches in said base layer are covered by the lateral contact layer”;

116. In my opinion, the cited disclosures do not demonstrate that Hirler anticipates limitation 1.g of the '634 Patent.

117. As a threshold issue, it is unclear what, if any, construction Dr. Liu has applied in analyzing limitation 1.g. As discussed, Dr. Liu expressly addresses construing the phrase “sidewalls of said trenches in said base layer,” but not the phrase “lateral contact layer.” In his analysis of limitation 1.g against Hirler, Dr. Liu opines that “body amplification zone located in the same position along the sidewalls of the contact trench” and “the purpose of the body amplification zone is the same as the lateral contact layer—i.e., to achieve the intended avalanche.” Ex. 1003 ¶ 73. But, in my opinion, the lateral contact layer of claim 1 is required to be on the sidewalls of the contact trench by the language “the sidewalls of said trenches in said base layer are covered by.” Thus, in claim 1 of the '634 Patent, the lateral contact layer must be present at the sidewalls of the source contact trench in the base layer, but a structure is not a “lateral contact layer” simply because it is so located there (as otherwise an unaltered base layer would likewise satisfy the term). Moreover,

in my opinion, that Hirler’s body amplification zone helps “achieve the intended avalanche breakdown voltage capability, without it being degraded through the turning on the of NPN parasitic bipolar transistor” is entirely functional—it says nothing to indicate it meets the plain meaning of any of the words of the phrase “lateral contact layer.”

118. Moreover, I understand that Force MOS has proposed “a region of dopant which is implanted into sidewalls of the source contact trenches to have a dopant concentration between P and P+ (“P* doping”) for an N-channel MOSFET or between N and N+ (“N* doping”) in a P channel MOSFET.”³ As discussed above, I believe that is the correct construction. In my opinion, Hirler does not satisfy that construction, or the plain and ordinary meaning of “lateral contact layer” for two reasons.

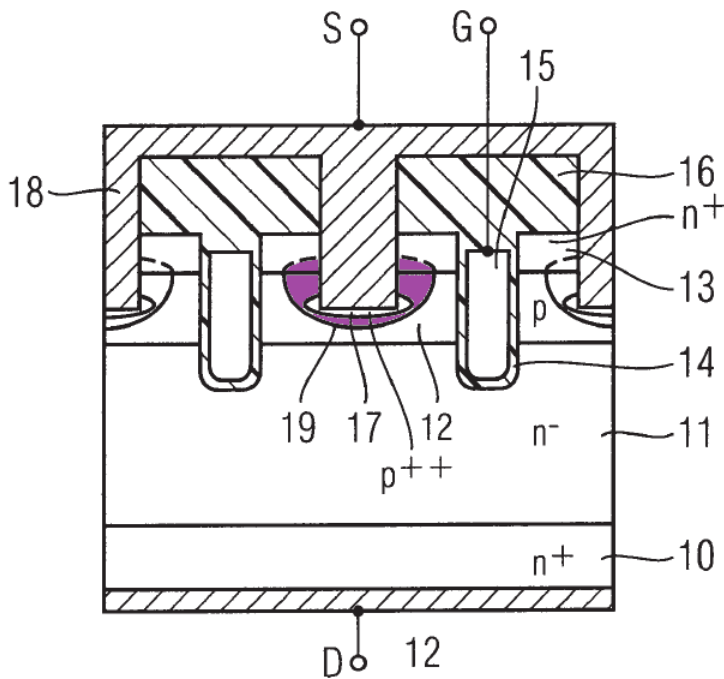
119. First, Hirler’s “body amplification zone 19” (which Dr. Liu equates to the claimed “lateral contact layer”), is created by ion implantation *before* Hirler’s contact trenches are etched. Ex. 1006 (Hirler), [0030], Figs. 2C-2D. Thus, Hirler does not disclose a region of dopant which is *implanted into sidewalls* of the source contact trenches. This is required by Force MOS’s proposed construction, discussed

³ Hirler’s embodiment that Dr. Liu analyzes is an N-channel MOSFET. *See* Ex. 1003, ¶ 75 (citing Hirler, Fig. 2F, [0018]). Thus I focus on N-Channel MOSFETs in my analysis of claim 1.

above, and thus Hirler cannot satisfy “lateral contact layer” under Force MOS’s construction.

120. Moreover, even if Force MOS’s construction is not adopted, it is compelled by the ordinary meaning of “sidewalls of said trenches in said base layer are *covered* by the lateral *contact layer*” in the context of claim 1. In particular, in context, a POSITA would understand “cover[ed]” as indicating more than simply a “region” “being present “at” the sidewalls, since that would fail to distinguish the base layer (or the prior art of Fig. 1 of the ‘634 Patent). Rather, a POSITA would understand “covered by the lateral contact layer” as being consistent with a “thin sheet” being “spread over” the sidewalls, which would require a process where the sidewalls already exist at the time of the creation of the lateral contact layer (a sheet cannot be spread over something that does not yet exist). *See* Ex. 2029 (<https://www.merriam-webster.com/dictionary/cover>) (“cover ... 4 a: to spread over”); Ex. 2025 (<https://dictionary.cambridge.org/us/dictionary/english/layer>) (“layer ... thin sheet of a substance.”).

121. Moreover, in my opinion, this distinction is more than a mere difference in manufacturing methods but reflects substantively different structures. As shown in Fig. 2F of Hirler, the result of implanting the body amplification zone before etching the trenches is to create an expansive doped *region*:



Ex. 1005 (Hirler), Ex. 2F (annotated)

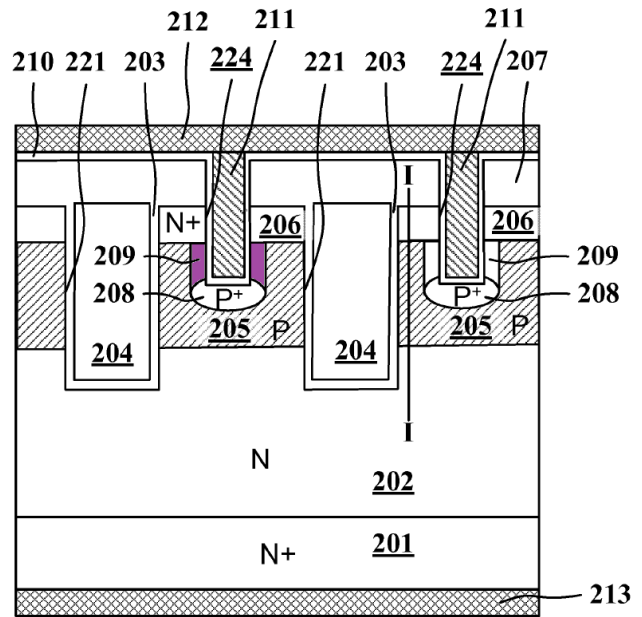


Fig. 2G

Ex. 1001 ('634 Patent), Fig. 2G (annotated)

122. Thus, by using Hirler's technique for creating body amplification zone 19 (implantation and then annealing/diffusion) results in the "lateral extensions" of the zone "reach[ing] the vicinity of the channel in the area of the trench gates 14, 15 after subsequent annealing/diffusion steps." Ex. 1006 (Hirler), [0036], claim 5; *compare id.*, Fig. 2F with '634 Patent, Fig. 2G. A POSITA would understand that such step would risk increased P dopant concentration in the channel area, which would harm threshold voltage, particularly if the gate trench masks were not well aligned with the mask used to create the body amplification zone. This issue would be exacerbated as a MOSFET designer tried to increase cell density of the MOSFET.

Such an increase of threshold voltage is exactly the situation the '634 Patent tries to avoid. Ex. 1001 ('634 Patent) at 2:10-11, 5:12-16, 5:27-29, Figs. 2G, 4.

123. Second, the cited disclosures of Hirler also do not demonstrate that Hirler satisfies Force MOS's proposed construction of "lateral contact layer" because Hirler discloses that "body amplification zone 19" has "P+" doping rather than "P*" doping. Ex. 1006 (Hirler), [0030]; *see also* '634 Patent at 2:1-8 ("lateral contact layer P* has less doping concentration than [] P+"). Also, in my opinion, a POSITA applying the plain and ordinary meaning of "lateral contact layer," as informed by the specification, would similarly interpret this limitation as requiring "P*" doping (which Hirler's body amplification zone 19 does not have). Indeed, the '634 Patent repeatedly emphasizes the use of P* doping in the sidewalls in distinguishing from the prior art. '634 Patent, 2:1-11, 3:55-65.⁴

124. Additionally, in my opinion, the cited disclosures fail to demonstrate that Hirler satisfies Limitation 1.g if "sidewalls of said trenches in said base layers" is construed to require coverage of the "entire" sidewalls with the lateral contact

⁴ Although the '634 Patent provides a numeric range for the dose used to create P* doping of 1×10^{14} to $4 \times 10^{14} \text{ cm}^{-2}$ ('634 Patent, 3:58), this cannot be directly compared to Hirler's disclosure of a doping concentration of 1×10^{16} to $1 \times 10^{18} \text{ cm}^{-3}$ (Hirler at [0031]). As demonstrated by the different units, a dose is distinct from doping concentration, as the doping concentration depends on both the dose and other properties (e.g. the time and temperature of any diffusion/annealing steps).

layer. Dr. Liu cites to no express disclosure in Hirler that states that the body amplification zone covers the entire sidewalls of the source contact trench. Ex. 1003 ¶ 73. To the contrary, Hirler teaches that “the depth of the body reinforcement zones 19 created by implantation can be controlled” and that “body amplification zone 19” is “practically not adjacent to the surface” and that “the contact trench is etched so deep that it is driven into the body amplification zone 19.” Ex. 1006 (Hirler), [0030], [0035]. Moreover, the body amplification zone 19 is created by doping *through* an already doped source layer. *Id.*; *id.*, [0030]; Ex. 1005, Fig. 2C,. This would necessarily result in *some* degree of counter-doping of the source layer. Based on the disclosures of Hirler, between the bottom of the N-doped source layer (where the N doping concentration would be the lowest) and the top of the P-doped body amplification zone 19 a person of ordinary skill would understand and expect there to be a region of no net dopant. Whether this region would be significant enough to conclude that there is a portion of the sidewalls in the base layer without a lateral contact layer would require additional details that are not supplied by Hirler. Thus, in my opinion, a person of ordinary skill in the art would not understand Hirler as necessarily disclosing that the “body amplification zone 19” covers the entire sidewalls in the base layer. I understand Dr. Liu relies on the simplified drawing of Hirler’s figures in support of his conclusion (Ex. 1003, ¶ 73 (citing Ex. 1005, Fig. 2F)), but, in my opinion, a person of skill in the art would interpret those figures in

light of the written description as not necessarily disclosing that the entire sidewalls of Hirler's contact trench in the base layer being covered by body amplification zone 19.

2. Claims 2 and 6

125. Claims 2 and 6 depend from Claim 1 of the '634 Patent and thus requires all of the limitations of claim 1. Because claim 1 is not anticipated by Hirler for the reasons discussed above, in my opinion, claims 2 and 6 are also not anticipated by Hirler.

C. Claims 3-5 and 7-9 Are Not Obvious over Hirler in View of Kobayashi 174

126. Dr. Liu opines that claim 3 of the '634 Patent is rendered obvious by the Hirler reference (DE 102004009083) (Exs. 1005, 1006) combined with the Kobayashi 174 reference (US2004/0021174) (Ex. 1008). As set forth below, I disagree.

1. Lack of Motivation to Combine in Manner Claimed

127. As a threshold issue, Dr. Liu ignores that Hirler and Kobayashi 174 are diametrically opposed references that both teach away from each other. As discussed, the primary focus of Hirler (and its body amplification zone) is to avoid having to "precisely defin[e] the depth of the body contact zone [i.e., the strongly doped implant at the bottom of source contact trenches]." Ex. 1005 (Hirler) at [0007]. By contrast, the focus of Kobayashi 174 is to do exactly that, i.e., precisely

define the depth of the base contact layer (the strongly doped implant at the bottom of the source contact trenches) such that it is at a depth different from the depth where dopant concentration is the highest in the base layer. *Id.* at [0018]-[0019], [0025], Figs. 5A, 5B, 7C. This is directly relevant to the purposes of the combination, as Dr. Liu proposes combining components of the structure of Kobayashi 174's source contact trenches with Hirler's source contact trenches. Given the diametrically opposed goals and disclosures of Hirler and Kobayashi 174, in my opinion, a person of ordinary skill in the art would not select those references for combination.

128. Moreover, Dr. Liu's motivation to combine analysis is brief, only identifying as a motivation to add Kobayashi 174's barrier metal layer to Hirler "promote the adhesion of the tungsten contact plug of Hirler to the contact area of the source contact trenches. Ex. _1003 ¶ 90. Dr. Liu says these were "known" concepts in the art, but cites no sources other than Kobayashi itself. *Id.* ¶ 91. Indeed, Dr. Liu does not cite any particular field of art in this discussion. In particular, Dr. Liu cites no evidence that tungsten was widely used for *source contact trenches* in *trenched MOSFETs*. To the extent he is opining about a broader field of art than *trenched MOSFETs with trenched source contacts*, he provides no analysis why use of tungsten in other devices is relevant to device of Hirler. I understand that

Defendant bears the burden of proof on this issue and that such conclusory testimony carries no weight.

129. Also, in Dr. Liu's motivation to combine analysis, he assumes that the plugs would be made of tungsten in opining that barrier layer would be obvious. *Id.* ¶ 91. However, Hirler identifies aluminum as its primary embodiment for filling the contact trenches, with tungsten or polycrystalline silicon identified as alternatives. Ex. 1006 (Hirler), [0022]-[0023]. However, Dr. Liu identifies no motivation to *select* Hirler's Tungsten stopper embodiment, from the various embodiments disclosed in Hirler, for combination with Kobayashi 174, even though the selection of Tungsten is the basis for Dr. Liu's motivation to combine to use Kobayashi 174's barrier layer. In my opinion, particularly as of the filing date of the '634 Patent, a person of ordinary skill in the art would not immediately envisage a need for a barrier layer if aluminum or polycrystalline silicon were selected. And, Hirler's aluminum embodiment source contact provides at least some benefits over the tungsten embodiment, i.e., it can be accomplished by a simpler procedure with less steps (a single aluminization step that fills the source contact trenches and also provides the source contact metal layer). Ex. 1006 (Hirler), [0022].

130. As Dr. Liu himself notes, a barrier layer may be used to create a barrier to prevent gases sometimes used in the deposition of tungsten from etching the silicon (Ex. 1003, ¶ 82, 92), and thus a barrier layer is not necessarily required when

depositing aluminum on silicon. I note that Dr. Liu provides no other motivation for a barrier layer other than in connection with tungsten deposition, and thus provides no motivation to use a barrier layer if tungsten is not selected (which Dr. Liu has not identified a motivation for). Thus, in my opinion, Dr. Liu has not provided an adequate explanation of a motivation to combine the references in the manner claimed.

131. Although Dr. Liu mentions that “good planarization” is important (Ex. 1003 ¶ 91) and suggests that tungsten is needed to provide good planarization, he provides no citation or explanation that good planarization could not be achieved with Hirler’s aluminum or polysilicon embodiments. Indeed, it was well known in the field of semiconductor manufacturing to use chemical mechanical planarization (or polishing, both referred to as CMP) to ensure good planarization, particularly after a deposition step. *See, e.g.*, Ex. 2016 (semiconductor glossary) at 40 (“**Chemical-Mechanical Planarization, CMP** increased force mechanical interactions between polishing pads and the patterned wafer surface enhanced by the chemically reactive slurry; a combination of chemical etching and abrasive polishing carried out for the purpose of surface planarization through the removal of excess material ...”). Dr. Liu provides no analysis why Hirler’s embodiments using aluminum or polysilicon for the source trenches could not be adequately planarized by CMP.

132. Dr. Liu also notes that “CVD tungsten process” is able to conformally fill contact holes with a high aspect ratio, but fails to explain or provide any reasoning why Hirler’s alternative embodiments are unable to conformally fill contact holes, even as manufacturing processes scale to smaller dimensions. Ex. 1003 ¶ 91. In particular, Kobayashi uses polysilicon (aka polycrystalline silicon) for filling its gate trenches (Ex. 1008, [0009]), indicating that polycrystalline silicon is equally capable of conformally filling trenches in manufacturing processes where one might use tungsten for contacts.

2. Claim 3-5, 7-9

133. Claims 3-5 and 7-9 all depend, directly or indirectly from claim 1 of the ’634 Patent. Thus they require all of the limitations of claim 1. In Dr. Liu’s obviousness analysis for claims 3-5 and 7-9 in his “Hirler in View of Kobayashi 174” obviousness ground, Dr. Liu relies solely on his anticipation analysis comparing claims 1 and 2 of the ’634 Patent with Hirler for his conclusion that Hirler in View of Kobayashi 174 satisfies claims 1, 2 and 6. Ex. 1003 ¶¶ 81, 85. That is, Dr. Liu does not offer any opinion that combining Kobayashi 174 with Hirler would satisfy any of the limitations of claims 1 or 2 differently than he opines with respect to Hirler alone. Because Dr. Liu offers no opinion that Kobayashi 174 cures any of the deficiencies I identify above in Dr. Liu’s comparison of claims 1 and 2 to Hirler, in my opinion, Dr. Liu fails to demonstrate that claim 3 is obvious for the same

reasons I discuss above regarding Dr. Liu’s anticipation analysis of Hirler versus claims 1 and 2 of the ’634 Patent.

134. Moreover, as discussed above, a POSITA would not be motivated to select Hirler and Kobayashi or combine them in the manner claimed. In particular, claim 3 recites “The trenched MOSFET of claim 2, wherein further comprises a barrier metal layer and a plurality of contact metal plugs.” Claims 4-5 depend, directly or indirectly, from claim 3. Claim 7 recites “wherein further comprises a barrier metal layer and a plurality of contact metal plugs.” Claims 8-9 depend, directly or indirectly, from claim 7. Thus, claims 3-5 and 7-9 all require “wherein further comprises a barrier metal layer and a plurality of contact metal plugs.” As discussed above, Petitioner and Dr. Liu fail to articulate an adequate motivation to combine Hirler and Kobayashi 174 to use metal plugs.

D. Claims 1 and 2 Are Not Anticipated by Shiraishi

135. Dr. Liu opines that claims 1-2 of the ’634 Patent are anticipated by the Shiraishi reference (US20050029584). As set forth below, I disagree.

1. Claim 1

a) [1.a]. “a semiconductor region having a drain region, a body region and a source region, comprising, a silicon substrate, an epitaxial layer corresponding to said drain region disposed on the top of said silicon substrate, a base layer corresponding to said body region disposed on the top of said epitaxial

layer, and a source layer corresponding to said source region disposed on the top of said base layer;”

136. In my opinion, the cited disclosures do not demonstrate that Shiraishi anticipates limitation 1.a of the '634 Patent.

137. In my opinion, Dr. Liu's application of Shiraishi is inconsistent with claimed structure of claim 1 of '634 Patent. Claim 1 recites three distinct semiconductor layers: “an epitaxial layer corresponding to said drain region disposed on the top of said silicon substrate, a base layer corresponding to said body region disposed on the top of said epitaxial layer, and a source layer corresponding to said source region disposed on the top of said base layer.” '634 Patent, cl. 1. That is, a source layer on top of a base layer corresponding to the body region, and the base layer on top of the epitaxial layer. Only at the sidewalls and the bottom of the source contact trench are there other layers (the lateral contact layer and the source contact layer). *Id.*; *see also* '634 Patent, Fig. 2G. However, Dr. Liu reads the claimed 3 layers onto 4 distinct layers of Shiraishi that extend completely throughout the semiconductor material between the source contact trenches and gate trenches. Ex. 1003, ¶¶ 97-103 (mapping Shiraishi's layers 13 and 14 onto the “body region”, but not stating which claimed layer that layer 14 corresponds to). Moreover, the claim recites that the “base layer correspond[s] to said body region,” thus it would be incorrect to map layers 13 and 14 of Shiraishi onto the body region but to only map layer 13 onto the “base layer.” '634 Patent, cl. 1.

138. Furthermore, it is well understood that in MOSFETs, the body region contains the region where the channel is formed when the gate is in an “ON” state (and where the channel is absent where the gate is in an “OFF” state). *See, e.g.*, Ex. 2030 (Sedra, Adel S., *Microelectronic Circuits* (5th Ed. 2004)) at 236-238 (§ 4.1.1). However, Shiraishi only identifies layer 13 (not layer 14) as being the “channel layer” or “acting as a base.” Ex. 1009 (Shiraishi), [0072]-[0073], [0080], [0084]. By contrast, layer 14 is identified in Shiraishi as a “punch-through stopper layer,” not a base layer, body region, or channel region. *Id.* at [0073], [0081]. This indicates that layer 14 of Shiraishi is not part of the body region or base layer. Indeed, Dr. Liu provides no analysis to the contrary. However, layer 14 of Shiraishi is interposed between the source layer (15) and the base layer (13), which is inconsistent with the specific structure of limitation 1.a, which requires “a source layer corresponding to said source region disposed on the top of said base layer.”

139. Thus, in my opinion, Dr. Liu has not demonstrated that Shiraishi discloses a MOSFET with layers arranged in a manner that satisfies limitation 1.a.

b) [1.g]. “wherein the sidewalls of said trenches in said base layer are covered by the lateral contact layer”;

140. In my opinion, the cited disclosures do not demonstrate that Shiraishi anticipates limitation 1.g of the ’634 Patent.

141. As discussed above, in connection with limitation 1.a, Dr. Liu identifies only Shiraishi’s layer 13 as corresponding to the “base layer,” despite identifying

Shiraishi's layers 13 and 14 together as corresponding to the claimed "body region." Ex. 1003 ¶¶ 97-103. In limitation 1.g, Dr. Liu identifies Shiraishi's layer 14 as the "lateral contact layer." Ex. 1003 (Liu Declaration), ¶¶ 107. Thus, plainly Dr. Liu's theory for limitation 1.g. fails, because as shown in Shiraishi's figures, the alleged lateral contact layer (i.e., Shiraishi's layer 14) is not *in* the alleged base layer (i.e., Shiraishi's layer 13) but rather on top of the alleged base layer (i.e., layer 13)—thus no portions of the sidewalls would be covered by the "lateral contact layer" in the "base layer" as required by the claim.

142. Moreover, even if Petitioner were allowed to articulate a theory that Shiraishi's layer 13 and layer 14 could be considered to together constitute a single "base layer," that would be inconsistent with the construction requiring lateral contact layer cover "entire" sidewalls of the trench in the base layer. Dr. Liu provides no explanation why Shiraishi satisfies Petitioner's own construction of "sidewalls of said trenches in said base layer" requiring that the lateral contact layer cover the "entire" side wall in the base layer. Indeed, Shiraishi's own figures plainly indicate that there are portions of the base layer (i.e., portions of layer 13 below layer 14) adjacent to the sidewalls, i.e., portions of the sidewalls in the base layer not covered by the alleged lateral contact layer:

stopper layer 14 is a thin layer of “about 0.1 to about 0.4 μm .” *Id.*, claim 22. By contrast the layer 13 extends down to about 0.9 μm from the semiconductor surface (0.1 μm less than the 1 μm deep gate trenches). Ex. 1009 (Shiraishi), [0083]. Thus, the written disclosures indicate that layer 13 is considerably thicker than layer 14. Accordingly, if the “base layer” were layers 13 and 14 together, it would not satisfy Petitioner’s construction of “sidewalls of said trenches in said base layer” requiring that the lateral contact layer cover the “entire” side wall in the base layer.

144. Turning to “lateral contact layer” itself, it is unclear what, if any, construction of that term Dr. Liu has applied in analyzing limitation 1.g. Instead, Dr. Liu simply states in a conclusory manner that “Shiraishi discloses and the POSITA would understand that this region acts as a lateral contact layer to prevent punch-through.” Ex. 1003 ¶ 107. However, there is no apparent connection between the words of the phrase “lateral contact layer” and the function of “prevent[ing] punch-through.”

resist film at the time of forming the p– type semiconductor region 13”). Because the mask controls the dimensions from the top-view plane, Shiraishi’s disclosures of *distinct* layers 13 and 14 can only be the result of processes that cause layer 14 to be implanted at a different depth than layer 13, and thus there must be some source contact trench sidewall adjacent to layer 13 in Shiraishi (i.e., as shown in Shiraishi’s figures).

145. Moreover, I understand that Force MOS has proposed “a region of dopant which is implanted into sidewalls of the source contact trenches to have a dopant concentration between P and P+ (“P* doping”) for an N-channel MOSFET or between N and N+ (“N* doping”) in a P channel MOSFET.”⁶ In my opinion, Shiraishi does not satisfy that construction or the plain and ordinary meaning of “lateral contact layer” for at least two reasons.

146. First, Shiraishi’s layer 14 is implanted across the entire active region of the semiconductor surface *prior* to the sidewalls of a source contact trench existing. Ex. 1009 (Shiraishi), Figs. 6-7, [0073] (“dopant ions (for example B) having the p-type conductivity may be implanted into the n- type single crystal silicon layer 1B at a concentration in the order of 3×10^{12} ions/cm², thereby forming a p-type semiconductor region (fifth semiconductor layer) 14”), [0074] (“the insulating film 16, the silicon oxide film 12, and the substrate 1 are etched, thereby forming contact grooves (a second groove part) 17”). Thus, Shiraishi does not disclose a region of dopant which is *implanted into sidewalls* of the source contact trenches. This is required by Force MOS’s proposed construction (discussed above), and thus Shiraishi cannot satisfy that construction.

⁶ Shiraishi’s embodiment that Dr. Liu analyzes is an N-channel MOSFET. See Liu Declaration, ¶ 140 (citing Shiraishi, [0067], [0073]). Thus I focus on N-Channel MOSFETs in my analysis.

147. Moreover, even if Force MOS's construction is not adopted, as discussed above in connection with the Hirler reference, it is compelled by the ordinary meaning of "sidewalls of said trenches in said base layer are *covered* by the lateral *contact layer*" in the context of claim 1. In particular, in context, a POSITA would understand "cover[ed]" as indicating more than simply a region "being present at" the sidewalls, since that would fail to distinguish the base layer (or the prior art of Fig. 1 of the '634 Patent). Rather, a POSITA would understand "covered by the lateral contact layer" as being consistent with a "thin sheet" being "spread over" the sidewalls, which would require a process where the sidewalls already exist at the time of the creation of the lateral contact layer (a sheet cannot be spread over something that does not yet exist). See Ex. 2029 (<https://www.merriam-webster.com/dictionary/cover>) ("cover ... 4 a: to spread over"); Ex. 2025 (<https://dictionary.cambridge.org/us/dictionary/english/layer>) ("layer ... thin sheet of a substance.").

148. Moreover, in my opinion, this is more than a mere difference in manufacturing methods but results in a substantively different structure, as shown in the following annotated figures:

the gate and increases dopant in the area between the source and the drain where the channel forms. Ex. 1009 (Shiraishi), [0073], Figs. 5-6, 8. The resulting increased dopant near the gate and in the channel area would result in an increase of threshold voltage, which is exactly the situation the '634 Patent wants to avoid. Ex. 1001 ('634 Patent) at 2:10-11, 5:12-16, 5:27-29, Figs. 2G, 4.

150. Second, Dr. Liu provides no identification or explanation why Shiraishi's layer 14 has P* doping. The '634 Patent recites that: "[a]ccording to the present invention, the silicon substrate, the epitaxial layer, and the source layer are N-type; the base layer and lateral contact layer P* are P-type; and each of the source contact trenches further has a P⁺-type base contact layer at a bottom thereof and the lateral contact layer P* has less doping concentration than the P⁺ base contact layer at the source contact trench but higher doping concentration than P-base layer." Ex. 1001 ('634 Patent) at 2:1-8. Because Shiraishi's layer 13 is "P-" doping (i.e., weakly doped with positive dopants), Shiraishi's disclosure that layer 14 has a higher doping concentration than layer 13 does not necessarily imply that Shiraishi's layer 14 has P* doping. Ex. 1009 (Shiraishi), [0073]. Indeed, Shiraishi does not disclose calibrating the doping of layer 14 to balance reduced resistance at the source contact-base layer interface (thereby reducing avalanche) with threshold voltage, but rather layer 14 is primarily designed to act as a punch-through stopper (i.e., to prevent the depletion regions of the source and drain from connecting in the channel region).

Id., [0073], [0080]. Reduction of base resistance is only a secondary consideration in Shiraishi. *Id.*, [0084]. Moreover, Shiraishi discloses that layer 13 is created by a dose of “ 5×10^{12} ions/cm²” (*id.*, [0073]), and layer 14 is created by an additional dose of “ 3×10^{12} ions/cm²” (*id.*), for a net dose of 8×10^{12} ions/cm² for layer 14. Notably, the fact that layer 13 and layer 14 are created with doses of the same order of magnitude, and that Shiraishi calls layer 13 a “P-” layer, demonstrates that layer 14 does not have P* doping. By contrast, the ’634 Patent gives an exemplary range for the dose to create P* doping of 1×10^{14} to 4×10^{14} cm⁻² (’634 Patent, 3:58), which is a dose two orders of magnitude larger than the dose used for Shiraishi’s layer 14. Accordingly, in my opinion, Shiraishi does not disclose P* doping.

2. Claim 2

151. Claim 2 depends from Claim 1 of the ’634 Patent, and thus requires all of the limitations of claim 1. Because claim 1 is not anticipated by Shiraishi for the reasons discussed above, in my opinion, claim 2 is also not anticipated by Shiraishi.

E. Claims 3-9 Are Not Obvious over Shiraishi in View of Kobayashi 174

152. Dr. Liu opines that claims 3-9 of the ’634 Patent are rendered obvious by the Shiraishi reference in view of Kobayashi 174 (US20040021174). As set forth below, I disagree.

1. Lack of Motivation to Combine

153. As a threshold issue, Dr. Liu ignores that Shiraishi and Kobayashi 174 are diametrically opposed references that both teach away from each other. Kobayashi 174 is specifically focused on avoiding the leaching of dopants into the channel region, and the resulting increase of threshold voltage. Ex. 1008 (Kobayashi) 174, [0014]-[0019], [0025], [0037], Figs. 5A, 5B, 7C. By contrast, as discussed, Shiraishi is specifically focused on its punch-through stopper layer which introduces additional dopants laterally throughout the cell between the trench gates and the source trenches so as to reduce punch through, i.e., the focus of Shiraishi is to intentionally do what Kobayashi 174 specifically seeks to avoid. Ex. 1009 (Shiraishi), Fig. 9, [0080]-[0081]. Given the diametrically opposed goals and disclosures of Shiraishi and Kobayashi 174, in my opinion, a person of ordinary skill in the art would not select those references for combination.

154. Dr. Liu only provides brief statements in support of his conclusion that one would be motivated to combine Shiraishi with Kobayashi 174 in the manner claimed by claim 3. Ex. 1003 ¶¶ 112-116. Indeed, his reasoning is largely the same as the reasoning he provides for combining Hirler and Kobayashi 174 for claim 3, and fails for the same reasons discussed above for that ground. In particular, “smooth top surface” is a benefit whenever source contact trenches are filled and planarized as a separate step prior to source metallization, it is not a benefit

specifically related to using plugs. That is, the source metal top layer will have a smooth top surface as long as there is a planarization procedure before it is applied. Thus, the benefit of a smooth top surface would equally apply to any process where a metal deposition to fill the source contact trenches is followed by a planarization procedure prior to source metallization, even for designs which intrinsically lack plugs, such as Shiraishi's open-cell stripe topology, which has continual metal trenches. Ex. 1009 (Shiraishi), Figure 11. Dr. Liu provides no explanation for why there would be a motivation to select a topology compatible for plugs rather than one of the topologies disclosed in Shiraishi which are incompatible with plugs (e.g., a stripe topology of Ex. 1009 (Shiraishi), Fig. 11), provides that such trenches are filled and planarized before metallization. Nor does Dr. Liu provide any explanation why use of a CMP planarization would be inadequate to create a smooth top surface. Thus, in my opinion, Dr. Liu has not provided an adequate explanation of a motivation to combine the references in the manner claimed.

2. Claims 3-9

155. Claims 3-9 all depend, directly or indirectly, from claim 1 of the '634 Patent. Thus they require all of the limitations of claim 1. In Dr. Liu's analysis for claims 3-9 in his Shiraishi in View of Kobayashi 174 obviousness ground, Dr. Liu relies solely on his anticipation analysis comparing claim 1 of the '634 Patent with Shiraishi for his conclusion that Shiraishi in View of Kobayashi 174 satisfies claim

1. Ex. 1003, ¶¶ 112, 119. That is, Dr. Liu does not offer any opinion that combining Kobayashi 174 with Shiraishi would satisfy any of the limitations of claim 1 differently than he opines with respect to Shiraishi alone. Because Dr. Liu offers no opinion that Kobayashi 174 cures any of the deficiencies I identify above in Dr. Liu's comparison of claim 1 to Shiraishi, in my opinion, Dr. Liu fails to demonstrate that any of claims 3-9 are obvious for the same reasons I discuss above regarding Dr. Liu's anticipation analysis of Shiraishi versus claim 1 of the '634 Patent.

156. Additionally, claim 3 recites "The trench MOSFET of claim 2, wherein further comprises a barrier metal layer and a plurality of contact metal plugs." Claims 4-5 depend, directly or indirectly, from claim 3. Claim 7 recites "wherein further comprises a barrier metal layer and a plurality of contact metal plugs." Claims 8-9 depend, directly or indirectly, from claim 3. Thus, claims 3-5 and 7-9 all require "wherein further comprises a barrier metal layer and a plurality of contact metal plugs." As discussed above, Petitioner and Dr. Liu fail to articulate an adequate motivation to combine Shiraishi and Kobayashi 174 to use metal plugs.

F. Claims 1-9 Are Not Obvious over Kobayashi 174 in View of Shiraishi

157. Dr. Liu opines that claims 1-(of the '634 Patent are rendered obvious by the Kobayashi 174 reference in view of the Shiraishi reference. As set forth below, I disagree.

1. Lack of Motivation to Combine

158. As discussed in connection with the obviousness ground of Shiraishi in view of Kobayashi 174, Shiraishi and Kobayashi 174 are diametrically opposed references that teach away from each other, and it is my opinion that a person of ordinary skill in the art would thus not select them for combination.

159. Dr. Liu opines that a person of skill in the art would have been motivated to combine Kobayashi 174 with Shiraishi's punch-through stopper layer 14. Ex. 1003 ¶¶ 164-170. As presented in Shiraishi (and shown in Dr. Liu's diagram of the proposed combination, Ex. 1003 ¶ 169, annotating Kobayashi's Fig. 5A), Shiraishi's punch-through stopper layer 14 is a layer that extends the entire width between the gate oxide and the source contact trench sidewalls. However, that approach is expressly taught away as disadvantageous by Kobayashi 174. In particular, Kobayashi expressly teaches avoiding having increased doping concentration on the source contact trench sidewalls because it can increase on resistance and potentially threshold voltage (if allowed to diffuse). Ex. 1008 (Kobayashi 174), [0065] (disclosing that "diffusion layer 14 for the base contact is not present on the side wall of the contact hole 12" because "if a part of the source diffusion layer 14 is diffused to the side wall of the contact hole 12, the source-contact resistance is increased to result in an increase in on-resistance" and if "[t]he impurity ... is further diffused to the channel region, [it would] result[] in an increase

in V_t .”), [0073] (“because the base contact layer is not present on the side wall of the contact, the source layer resistance is never increased.”). Thus, Dr. Liu and Petitioner proposed combining Kobayashi 174 with Shiraishi in a manner expressly taught away by Kobayashi 174.

160. Moreover, although Dr. Liu says there would be a motivation to avoid punch through, Dr. Liu identifies no reason why Kobayashi 174’s MOSFET has punch through issues which are not already adequately addressed by Kobayashi 174’s design. Nor does Dr. Liu provide any analysis explaining that punch through would be a significant limiting criteria in attempting to improve the cell density (i.e., reducing cell pitch) of Kobayashi 174’s designs as opposed to other obstacles (e.g., on-resistance, threshold voltage, avalanche breakdown, latch-up, gate capacitance, etc.). Indeed, it is well-known in the art of MOSFET that some designs have the limiting form of breakdown be avalanche breakdown, others have Zener breakdown, and others have punch-through. Ex. 2031 (Williams, Principles and Elements of Power Electronics, ISBN 978-0-9553384-0-3 (2006)) at 54. Not every power MOSFET design will have punch-through as a limiting form of breakdown. *See, e.g.,* Ex. 2032 (Sharma, R. S., and M. A. Peer. "Some Features of Avalanche Breakdown Phenomena Part 1: Transistors and Diodes." IETE Journal of Research 27.5 (1981): 178-184)) at 181 (describing that whether punch-down voltage is lower or higher than avalanche breakdown voltage can depend on factors including

transistor structure and operating temperature). Dr. Liu provides no reason to believe that Kobayashi 174's design is one that would benefit from a punch-through stopper layer. And, as discussed above, there are obvious downsides to implementing Shiraishi's punch-through stopper layer (i.e., increased channel resistance due to increased dopants in the channel region).

161. Moreover, there were other ways known in the art to avoid punch-through. *See, e.g.*, Ex. 2033 (US6084264A), Abstract, Figs. 3, 10, 4:62-5:17 (junction between the N drain region and the P-epitaxial layer extends between the N+ substrate and a sidewall); Ex. 2034 (US6545315B2) at Figs. 4, 8, 4:8-29, 4:48-5:27 (reducing punch-through by using patterned trench mask to prevent dopant from leaching leach out of the p-body, and by depositing a layer of undoped polysilicon followed by a layer of doped polysilicon when forming gate). That is, Dr. Liu provides no reasoned analysis why a person of skill in the art would be seeking to avoid punch through in Kobayashi's design, nor why a person of skill in the art would turn to Shiraishi's system to address any punch-through problem that may arise. Given that Kobayashi expressly teaches away from techniques—such as Shiraishi's layer 14—that would introduce additional dopant into the channel region, if punch-through were a problem with Kobayashi's MOSFET, a POSITA would look to other ways to reduce punch-through, of which, there were many known.

2. Claim 1

162. In Dr. Liu's proposed combination of Kobayashi 174 in view of Shiraishi, Dr. Liu proposes to modify Kobayashi 174 to use the distinct, separate "punch-through stopper layer" (layer 14) of Shiraishi. Thus, this proposed combination would have the same faults with respect to limitations 1.a and 1.g that I identify above in Dr. Liu's anticipation grounds for Shiraishi against claim 1.

163. In particular the use of Shiraishi's stopper layer 14 across the entire semiconductor material between the gate and source layer is inconsistent with the specific structure of layers and regions recited in limitation 1.a, which recites "source layer corresponding to said source region disposed on the top of said base layer." And, as discussed above, Dr. Liu's identification of the "lateral contact layer" as Shiraishi's layer 14 and the claimed "base layer" as Kobayashi's "base layer 9" is inconsistent with limitation 1.g (which requires the "lateral contact layer" to be present at the sidewalls *in the base layer*); and (3) Dr. Liu identifies no disclosure or motivation in either of the references to use P* doping (or N* doping for a P-Channel MOSFET) for a layer at the source contact trench sidewalls, as required by limitation 1.g.

164. As to limitation 1.g., Dr. Liu opines that the combination of Kobayashi 174 in View of Shiraishi would have the lateral contact layer cover the "entire" sidewalls of the source contact trench, as required by Petitioner's construction of

“sidewalls of said trenches in said base layer.” Ex. 1003 ¶ 167. But, there is no disclosure of such “entire” coverage in either reference, and Dr. Liu provides no motivation for combining Kobayashi 174 in View of Shiraishi in this manner. The only reason that Dr. Liu identifies for this is his contention that “Shiraishi expressly teaches a lateral contact layer along the entire sidewalls of the contact trench.” *Id.* But, as discussed above in the Shiraishi anticipation ground for claim 1, Shiraishi expressly discloses its punch-through stopper layer 14 as relatively thin and not penetrating the full depth of layer 13, leaving layer 13 (and its low “P-” doping concentration) existing adjacent to the source contact trench sidewalls beneath layer 14. *See, e.g.*, Ex. 1009 (Shiraishi), Fig. 9, [0083], claim 22. And, as discussed, Shiraishi’s figures expressly show portions of the sidewalls of the source contact trenches which are in the base layer (i.e., which are adjacent to layer 13) but not covered by the alleged lateral contact layer (i.e., which are not part of layer 14). *Id.*, Figs 8, 9. And, as discussed, Kobayashi entirely teaches away from any increased dopants in the channel region (as would be introduced by Shiraishi’s layer 14), due to the resulting increase of threshold voltage. Ex. 1008 (Kobayashi 174), [0065], [0073].

165. Moreover, it is important in Shiraishi that layer 13 have significant depth beyond layer 14, as layer 13 provides the channel region adjacent to the gate and increasing layer 13’s doping would increase threshold voltage. Ex. 1009

(Shiraishi), [0072], [0080]. Thus, combining Shiraishi with Kobayashi 174 to have Shiraishi's punch through layer 14 along the "entire" depth of the source contact trench's sidewalls would be inconsistent with Shiraishi's teachings.

166. Combining Shiraishi and Kobayashi to have "entire" coverage of the sidewalls with Shiraishi's layer 14 would also be inconsistent with Kobayashi's teachings. Indeed, as discussed above in the motivation to combine section, Kobayashi expressly teaches avoiding having increased doping concentration on the source contact trench sidewalls. Instead, Kobayashi addresses the issue of increased contact resistance at the sidewalls (and thus NPN latching and avalanche) by its embodiment which forms silicide 15. Ex. 1008 (Kobayashi 174), [0070]-[0071]. As part of this process, instead of implanting P-type dopants into the source contact trench sidewalls of the Kobayashi's NMOSFET, Kobayashi 174 implants Arsenic ions (an N-type dopant) into the source contact trench sidewalls. *Id.*, [0069], Fig. 9B. Thus both Shiraishi and Kobayashi expressly teach against combining in a manner that would have Shiraishi's punch-through stopper layer 14 take up the entire sidewalls of the source contact trench in the base layer.

3. Claims 2 and 6

167. Claims 2 and 6 depend from Claim 1 of the '634 Patent and thus requires all of the limitations of claim 1. Because claim 1 is not rendered obvious

over Kobayashi 174 in view of Shiraishi for the reasons discussed above, in my opinion, claims 2 and 6 are also not rendered obvious.

4. Claims 3-5 and 7-9

168. Claims 3-5 and 7-9 all depend, directly or indirectly, from claim 1 of the '634 Patent. Thus claims 3-5 and 7-9 requires all of the limitations of claim 1. Because claim 1 is not rendered obvious over Kobayashi 174 in view of Shiraishi for the reasons discussed above, in my opinion, claims 3-5 and 7-9 are also not rendered obvious.

169. Additionally, claim 3 recites “The trench MOSFET of claim 2, wherein further comprises a barrier metal layer and a plurality of contact metal plugs.” Claims 4-5 depend, directly or indirectly, from claim 3. Claim 7 recites “wherein further comprises a barrier metal layer and a plurality of contact metal plugs.” Claims 8-9 depend, directly or indirectly, from claim 3. Thus, claims 3-5 and 7-9 all require “wherein further comprises a barrier metal layer and a plurality of contact metal plugs.” Additionally, as discussed in the prior argument where Shiraishi is the primary reference and Kobayashi 174 is the secondary reference, Petitioner and Dr. Liu fail to articulate an adequate motivation to combine Shiraishi and Kobayashi 174 to use metal plugs. Indeed, in the ground with Kobayashi 174 as the primary reference, Dr. Liu and Petitioner simply seem to assume that the combination would use Kobayashi’s metal plugs (rather than, for example,

Shiraishi's continuous metal trench embodiment), without explanation. Ex. 1003 ¶¶ 165-169.

XI. CONCLUSION

170. I currently hold the opinions that I have expressed in this declaration. However, my analysis may continue, and I may acquire or receive additional information or insights that may result in revised or supplemental observations or opinions.

171. I understand this declaration will be used as evidence in a contested case before the PTAB.

172. I declare that all statements made herein on my own knowledge are true and that all statements made on information and belief are believed to be true, and further, that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 or Title 18 of the United State Code, and that such willful false statements may jeopardize the validity of the '634 Patent..

I declare under penalty of perjury that the foregoing is true and correct.

Executed: September 12, 2024



Dr. Dean Neikirk