
High-Power Vertical GaN Electronic Devices Formed by Epitaxial Lift-Off**Jingshan Wang****Publication Date**

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HIGH-POWER VERTICAL GAN ELECTRONIC DEVICES FORMED BY
EPITAXIAL LIFT-OFF

A Dissertation

Submitted to the Graduate School
of the University of Notre Dame
in Partial Fulfillment of the Requirements
for the Degree of

Doctor of Philosophy

by

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July 2018

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HIGH-POWER VERTICAL GAN ELECTRONIC DEVICES FORMED BY EPITAXIAL LIFT-OFF

Abstract

by

Jingshan Wang

GaN and related materials have become one of the most promising material systems for high efficiency power electronics due to their unique material properties, such as a high critical electrical field, large band gap, high electron saturation velocity, large electron mobility, and high thermal conductivity compared with alternatives, such as Si, GaAs and SiC. However, the actual performance of many lateral GaN devices has fallen short of expectations, including large ideality factors, the inability to achieve avalanche breakdown, dynamic on-state resistance, current collapse, and hysteresis in FETs. Unlike other power device options, most GaN devices are built on lattice-mismatched non-native substrates such as sapphire or SiC because of the high cost and limited availability of bulk GaN substrates. These foreign substrates result not only in large dislocation densities, but also limited thermal conductance for heat removal. This work focuses on the development of several GaN power device concepts, such as Schottky diodes and p-n diodes for high efficiency power switching applications, made possible by vertical device architectures. The prospects for, and benefits of, fabrication processing using epitaxial lift-off (ELO) using band gap selective photoelectrochemical (PEC) etching techniques are also examined.

Vertical devices are advantageous for power applications because they can utilize thick low-doped drift layers to achieve higher breakdown voltages. This leads to

smaller die sizes than comparable lateral devices. On the other hand, vertical devices are more sensitive to the presence of threading dislocations and thus must be made on high quality bulk GaN substrates for best performance. ELO technology has the potential to allow cost-effective device production using native GaN substrates through substrate re-use, as well as to improve thermal performance of devices by eliminating the thermal resistance associated with conventional substrates by enabling direct thermal and electrical bonding. To investigate vertical GaN devices and the potential benefits of ELO processing, Schottky diodes and p-n junction diodes have been fabricated and tested. The Schottky device results suggests that ELO processing could potentially improve device performance for devices on non-native substrates. In addition, to realize high-voltage, high-current vertical GaN-on-GaN power diodes and surmount the limitations of mesa-isolated power diodes, we developed a new vertical p-n diode design with ion-implantation edge termination (ET), sputtered SiN_x passivation and back-side cathode contacts. The measured devices exhibit a breakdown voltage (V_{br}) exceeding 1.68 kV, with differential specific on resistances (R_{on}) of 0.15 mΩ·cm². A Baliga's figure-of-merit (BFOM) of 18.8 GW/cm² is obtained; this is among the highest reported BFOMs for GaN homoepitaxial p-n diodes. These devices also exhibit near-ideal scaling with area, enabling currents as high as 12 A for a 1 mm diameter device. To investigate the effect of ELO processing on devices on bulk GaN substrates, a comparison study was performed on the devices after lift-off processing (after transfer to a Cu carrier wafer) and nominally-identical control devices (on a bulk GaN substrate and without the buried release layer). The results show that ELO-processed devices have nearly identical electrical performance—and improved thermal performance—compared to devices on full-thickness GaN substrates. In addition to these high power diodes, vertical GaN MESFETs have been designed and simulated, and functional devices have been obtained.

CONTENTS

FIGURES	iv
TABLES	x
ACKNOWLEDGMENTS	xi
CHAPTER 1: INTRODUCTION	1
1.1 GaN material system for power electronics	2
1.2 GaN vertical devices for power switching applications	4
1.3 Epitaxial lift-off (ELO) for GaN based materials	7
1.4 Motivation and outline of this work	8
CHAPTER 2: THIN-FILM GAN SCHOTTKY DIODES FORMED BY EPI- TAXIAL LIFT-OFF FROM SAPPHIRE SUBSTRATES	11
2.1 Introduction	11
2.1.1 Overview of GaN Schottky diodes	12
2.1.2 Overview of wavelength-selective PEC etching for GaN-based ELO	12
2.2 GaN Schottky diode fabrication process	14
2.3 Comparison of GaN Schottky diodes performance before and after ELO	15
2.3.1 Current-voltage characteristics of GaN Schottky diodes before and after ELO	17
2.3.2 Schottky diode temperature dependence	17
2.3.3 Schottky barrier height extraction	20
2.3.4 Trap and doping effects	21
2.3.5 Physical interpretation	25
2.4 Conclusion	25
CHAPTER 3: VERTICAL GAN P-N DIODES ON BULK GAN SUBSTRATES	27
3.1 Overview of GaN p-n diodes	27
3.2 Pd/Ni/Au on p-GaN ohmic contact with low contact resistance	30
3.2.1 Surface treatment	31
3.2.2 Thermal annealing	32
3.2.3 CTLM test	34
3.3 Vertical p-n diodes on bulk GaN substrates with ion-implanted isolation	34

3.3.1	Device structure and fabrication process	34
3.3.2	Ion-implantation process design and simulation	36
3.3.3	Sputtered SiN _x passivation	41
3.3.4	Device performance and physical interpretation	43
3.3.5	Comparison of GaN p-n diode performance between simulation and measurement	45
3.4	Conclusion	49
CHAPTER 4: THE IMPACT OF EPITAXIAL LIFT-OFF ON VERTICAL GAN P-N DIODES FROM BULK GAN SUBSTRATES		51
4.1	Overview of ELO on GaN p-n diodes	51
4.2	Epitaxial lift-off mesa isolated GaN p-n diodes from bulk GaN substrates	52
4.2.1	Device structure and fabrication process—mesa-isolated devices	52
4.2.2	Device performance and physical interpretation	53
4.2.3	Impact on carrier concentrations	56
4.3	Epitaxial lift-off ion-implantation isolated vertical p-n diodes from GaN substrates	56
4.3.1	Device structure and fabrication process—implant isolated de- vices	56
4.3.2	ELO p-n diode electrical performance	60
4.3.3	ELO p-n diode thermal performance	61
4.4	GaN p-n diodes on reclaimed substrate	63
4.5	Conclusion	64
CHAPTER 5: CONCLUSIONS AND FUTURE WORK		68
5.1	Summary, overview, and conclusion	68
5.2	Future work	69
5.2.1	Device design and simulation of GaN vertical MESFETs for high-power applications	69
5.2.1.1	Vertical GaN MESFET design and simulation	70
5.2.1.2	Basic physical models and equations	70
5.2.1.3	Effect of electric-field dependent mobility	74
5.2.1.4	Current-voltage characteristics and device optimization	75
5.2.2	Fabrication process design for vertical GaN MESFETs	77
5.2.2.1	Self-aligned source process	77
5.2.2.2	MESFET I-V characteristics	77
5.2.3	Further efforts—MESFETs	80
5.2.3.1	Optimization of via hole ICP-RIE process	82
5.2.3.2	Ion-implanted isolation	82
5.2.3.3	Device analysis	83
5.2.4	Further efforts—diodes	83
BIBLIOGRAPHY		84

FIGURES

1.1	Various power electronics applications as a function of the required rated current and voltage. [1]	3
1.2	Theoretical limits of R_{on} as a function of V_{br} for major semiconductor options. The contours shown reflect the Baliga figure of merit for each material.	4
1.3	Dynamic load line and switching trajectory for a power switching device. The dynamic load line is an example only; the details strongly depend on external circuitry, parasitic device impedances, and mode of operation. [2]	5
2.1	Schematic structure of Schottky diode (a) before and (b) after ELO processing.	13
2.2	Wavelength-selective PEC etch configuration used for the epitaxial lift-off process. (a) Schematic diagram of PEC etch processing. (b) High-angle annular dark-field (HAADF) image showing pseudomorphic InGaN release layer. (This HAADF figure is from Ref.[3])	14
2.3	Images of lifted-off GaN films and Schottky diodes. (a) Top-side view showing mechanical support metallization after lift-off; (b) view between sapphire substrate and detached GaN/Schottky diodes. UV illumination was used to highlight the yellow-green luminescence on the lifted-off film; (c) & (d) top view of Schottky diodes after bonding to a support substrate and removing the metal mechanical support layer by selective etching.	16
2.4	Semi-log plot of typical room-temperature I-V characteristics for a typical GaN Schottky diode before and after lift-off processing. The insets show details near the origin in a semi-log scale, as well as the I-V characteristics on a linear scale.	18
2.5	Semi-log plot of the reverse-bias I-V characteristics as a function of temperature for GaN Schottky diodes before and after epitaxial lift-off processing. Inset: reverse current density at -15 V (545 kV/cm) vs. temperature.	19
2.6	Semi-log plot of the forward-bias I-V characteristics as a function of temperature for GaN Schottky diodes before and after epitaxial lift-off processing.	20

2.7	Plot of the Norde function over bias and temperature, to facilitate barrier height extraction.	22
2.8	Cyclic I-V measurement, scan rate of 1 V/s.	23
2.9	Measured C-V characteristics (a) before ELO and (b) after ELO processing. In both cases, no frequency dispersion is observed, and no significant differences are seen before or after ELO.	24
2.10	Schematic illustration of possible mechanism for the performance improvement in ELO-processed GaN Schottky diodes. The red arrow denotes the ideal thermionic Schottky current contribution, while the blue arrows illustrate the leakage paths. The leakage paths include a vertical component along dislocations, and a lateral component in the InGaN release layer quantum well and the n^+ GaN buffer. Elimination of these two layers, and replacement of them with an insulating bond and carrier wafer, eliminates this leakage mechanism.	26
3.1	The doping profiles extracted the slope of $1/C^2$ and SIMS.	30
3.2	CTLM tests for p-type GaN/Pd/Ni/Au (30/20/50 nm, without annealing) ohmic contacts (on CTLM patterns with 30 μm inner diameter) and n-type GaN/Ti/Al/Ni/Au (30/100/50/50 nm without annealing). (a) Measured current-voltage characteristics with gaps from 3 to 22 μm . (b) Measured total resistance versus gap spacing for p-GaN contacts. $4.2 \times 10^{-5} \Omega\cdot\text{cm}^2$ specific contact resistance and 10 $\text{k}\Omega/\square$ sheet resistance were extracted from this CTLM test. (c) Measured current-voltage characteristics with 3 to 22 μm gaps for n-GaN contact test. (d) Measured total resistance versus gap spacing. $3.3 \times 10^{-6} \Omega\cdot\text{cm}^2$ specific contact resistance was extracted from this CTLM test.	35
3.3	(a) Cross-sectional schematic and (b) top view of a fabricated p-n diode with ion-implanted ET and SiN_x passivation.	37
3.4	Detail of ET structure and SRIM simulation of a triple energy implant for a partially compensated ET. The implant-induced defect concentration is smaller than the Mg doping (blue dashed line) from 440-470 nm in the p-GaN with the highest ion-implantation energy of 220 keV, leading to partial compensation layer thickness, t_p , of 30 nm.	39
3.5	(a) Computed electric-field distribution showing where the electric field peaks occur in devices with SiN_x passivation for the optimal case. (b) Electric field profile along the ET (red arrow in (a)) for different t_p . Balanced electric field peaks (blue curve) are obtained when t_p is close to the optimum.	40

3.6	Measured I-V characteristics of GaN p-n diodes with 8 μm drift layer (155 μm diameter). (a) Comparison of reverse I-Vs and V_{br} of p-n diodes without passivation, with sputtered SiN_x , and with PECVD SiN_x . Both sputtered SiN_x and PECVD SiN_x increase the V_{br} equally, consistent with a dielectric field distribution model. (b) Comparison of forward I-Vs and R_{on} for p-n diodes without passivation, with sputtered SiN_x , and with PECVD SiN_x . At 3.6 V, R_{on} is 0.25, 0.25 and 0.41 $\text{m}\Omega\cdot\text{cm}^2$ for these diodes, respectively. Compared with PECVD, sputtered SiN_x results in less compromise of the on-state performance.	42
3.7	Electric-field distribution for vertical p-n diode structures with SiN_x . (a)-(c) shows ET designs for several t_p values. When the thickness of the partially compensated layer is small (a), the electric field peaks at the corner of the p^+ GaN/ n^- GaN drift layer and the edge of the implant. When $t_p = 40$ nm (b), the electric field peaks are spread between the p^+ / p^- (partially compensated)/ n^- GaN corner and the corner of ET/ p^- / n^- GaN. When $t_p = 80$ nm, the electric field peaks at the corner of the ET/ p^- / n^- . The case shown in (b) $t_p = 40$ nm, results in the highest V_{br} . In devices without SiN_x surface passivation, similar trends are seen, except that the absence of the surface passivation leads to enhancement of the peak at the top surface of the etched ET ring as shown in (d).	44
3.8	Measured I-V characteristics of GaN p-n diodes with 8 μm drift layer as a function of device area. (a) Reverse I-Vs, showing that the breakdown voltage V_{br} is not affected by device area; (b) Forward I-Vs on semi-log scale, showing that device area does not affect the forward current density. The increase in SRH current for small devices suggests a modest edge-related recombination current; (c) Forward-bias pulsed I-V on large diodes. Currents as high as 12 A are carried by 1 mm diameter devices at 4 V.	46
3.9	Simulated electrical performance of diodes. (a) Forward I-V characteristics, (b) ideality factor, n , and (c) R_{on} of diodes with and without SiN_x passivation. Diodes with and without SiN_x have the same turn on voltage 3.1 V (at 100 A/ cm^2), R_{on} , and have $n = 2.0$ at low current levels, dropping to $n = 1.4$ at turn on before rising again due to series resistance.	47
3.10	V_{br} vs. t_p from simulation and measurement for devices both with and without SiN_x . The highest measured V_{br} occurred at 40 nm and 30 nm with and without passivation, respectively, only slightly offset from the simulation curves.	48

3.11	I-V performance of measured and simulated GaN pn diodes. (12 μm drift layer, 155 μm diameter, $t_p = 40\text{ nm}$) From the measurement, 1680 V V_{br} and 0.15 $\text{m}\Omega\cdot\text{cm}^2$ R_{on} (at 5 V) are obtained. Both the simulated and measured diodes have the same turn-on voltage of 3.1 V at 100 A/cm^2	49
3.12	Benchmark of R_{on} vs. V_{br} for reported power GaN p-n diodes. The blue stars are the results obtained for diodes in this work with 8 μm drift layers, while red stars indicate devices with 12 μm drift layers. Performance approaching the fundamental limits of GaN (assuming an electron mobility of 1470 cm^2/Vs and critical electric field of 3.9 MV/cm [4]) with a simple device and ET design has been achieved.	50
4.1	Schematic structure of thin-film GaN p-n diodes fabricated on GaN substrates. (a) Schematic structure of as-fabricated p-n diode after deposition of the encapsulating metal support layer. (b) Schematic structure of p-n diode after lift-off processing and remounting on an insulating carrier wafer. (c) Top view of an as-fabricated diode. (d) 1/4 of 2 inch wafer with metal support top layer (left) and substrate (right) after ELO.	54
4.2	Typical device ($40 \times 40\ \mu\text{m}^2$) electrical performance before and after ELO. (a) & (b) Measured I-V of as-fabricated and after-ELO p-n diode on a linear scale and a semi-log scale respectively. (c) Schematic structure of the physical interpretation explaining the increased series resistance after ELO. (d) Measured I-V from a recent vertical ion-implantation isolated p-n diode with backside n-GaN contact comparing with the I-Vs of mesa-isolated diodes. (e) Ideality factor and specific on resistance of the vertical p-n diode with implantation based isolation for devices fabricated using the same device structure as the mesa-isolated diodes.	57
4.3	Typical measured device capacitance-voltage (C-V) performance before and after ELO. (a) Measured C-V of as-fabricated and after ELO p-n diodes (b) Doping concentrations extracted from measured C-V of p-n diodes.	58
4.4	(a) Heterostructure of the ELO devices. The control sample has the same epitaxial layers, except the InGaN release layer. (b) Schematic cross-section of p-n diode after lift-off and bonding to the carrier. (c) View of GaN substrate and detached GaN p-n diode film after lift-off under UV illumination. (d) Top view of fully transferred GaN p-n diodes.	59
4.5	(a) & (b) Measured reverse and forward I-V characteristics of ELO and control p-n diodes. (c) & (d) Ideality factor n and differential R_{on} of ELO and control devices.	62
4.6	C-V performance of ELO and control devices.	63

4.7	Schematic illustration of pulsed I-V characterization approach for assessing thermal performance of pn junctions.	64
4.8	(a) DC I-V vs. temperature for the ELO devices. (b) Temperature-voltage characteristics for selected current densities, as extracted from the temperature-dependent I-V. (c) Representative pulsed I-V for ELO device for several pulse base voltages larger than the turn on voltage. (d) Temperature vs. power density lines for ELO and control devices. The thermal resistance is extracted from the slopes of these lines. . .	65
4.9	(a) Electroluminescence intensity vs. wavelength for a 160 μm ring contact p-n diode with different bias currents; the inset shows a device with light emission. (b) The device temperature extracted from the electroluminescence peaks vs. applied power for control and ELO devices.	66
4.10	Tests of devices fabricated on a re-used/reclaimed substrate. (a) Measured current-voltage characteristics of typical GaN vertical p-n junction diodes on prime bulk GaN substrate and on a reclaimed substrate, validating that device performance on epi-ready prime and reclaimed/reused substrates is nearly indistinguishable.[5] (b) Comparison of ideality factor and specific on resistances of diodes on prime GaN substrate and reclaimed substrate.	67
5.1	Structure of the vertical MESFET evaluated here. (a) Cross-section of the baseline MESFET structure simulated in TCAD. (b) Dimensions and doping parameters for the baseline MESFET design. Half of the device is shown (as simulated in TCAD); the device is symmetric about the right-hand edge of the figure.	71
5.2	Electric field distribution in the vertical MESFET, as simulated with Sentaurus TCAD.	73
5.3	Simulated I-V performance of the GaN MESFET. (a) $I_D - V_{GS}$ characteristics and transconductance g_m on a linear scale, (b) $I_d - V_{GS}$ transfer characteristics on a semi-log scale, (c) $I_D - V_{DS}$ characteristics at V_{DS} from 0 V to 15 V, and (d) breakdown characteristics. . . .	76
5.4	GaN MESFET performance as a function of key design variables. (a) Impact of the channel width on the output characteristics; (b) dependence of breakdown voltage on channel width; (c) influence of the drift layer thickness on the output characteristics; (d) drift layer thickness dependence of the breakdown characteristics; (e) impact of the channel length and thickness on the output characteristics; (f) dependence of the output characteristics on drift layer doping.	78
5.5	Vertical GaN MESFETs. (a) Schematic structure of GaN MESFET, (b) Top view of a typical GaN MESFET after fabrication, (c) Fabrication process flow for the vertical GaN MESFETs.	79

5.6	SEM images of fabricated MESFETs after the self-aligned source process and gate metallization.	80
5.7	Comparison between I-V characteristics for MESFETs from measurement and TCAD simulation. (a) Measured $I_d - V_{ds}$ family of curves, and (b) simulated $I_d - V_{ds}$ family of curves. (c) Measured $I_d - V_{gs}$ and g_m , and (d) simulated $I_d - V_{gs}$ and g_m for $V_{ds} = 5V$. (e) Measured $I_d - V_{gs}$ and (f) simulated $I_d - V_{gs}$ for V_{ds} from 1 V to 5 V.	81
5.8	SEM pictures of MESFET (a) after via hole etching, and (b) after pad metalization.	82

TABLES

2.1	COMPARISON OF BARRIER HEIGHTS AND IDEALITY FACTORS OVER TEMPERATURE FOR SCHOTTKY DIODES BEFORE AND AFTER ELO PROCESSING	22
3.1	SURFACE TREATMENT TESTS FOR P-GaN/Ni/Au OHMIC CONTACTS	32
3.2	ANNEALING TESTS FOR Ni/Au (20/50 NM) AND Pd/Ni/Au (30/20/50 NM) ON P-GaN OHMIC CONTACTS	33

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CHAPTER 1

INTRODUCTION

While developing clean alternative energy sources is essential for sustainability, in addition it is also critically important that the available energy is used as efficiently as possible. One area that is especially promising for improved efficiency is in power converters. These devices for DC to DC, AC to AC, or AC to DC (and visa-versa) converters are ubiquitous and span a wide range of scales and applications, from consumer products such as chargers for mobile phones to industrial motor drives for elevators and industrial process control and automation. For large-scale applications of power converters, even modest improvements in efficiency can produce significant power savings. However, implementing these functions with conventional device technologies is not especially efficient so far. To put this in perspective, it has been estimated that more than 10% of all electricity is lost during power conversion; this amount of lost power is more than 10 times the world's current supply of renewable energy[6]. Thus improving the efficiency of power converters could make a significant impact on overall energy usage. Further, this approach helps sustainable development without requiring extensive and challenging lifestyle changes. The goal of this project is to make contributions in this area, by exploring high performance GaN-based power device designs, as well as the potential for producing these devices economically.

High-power applications such as industrial motor drives may offer the best opportunity for new approaches, since conventional technologies face some of the most severe technical limitations. To address this, we are investigating the use of GaN-

based devices with vertical structures, since vertical structures offer fundamental performance and economic advantages. Despite these advantages, the vertical configurations proposed in this work have not been thoroughly explored. As of the start of this study, very limited data was available on the potential performance of devices of this type (see e.g. GaN vertical p-n diodes on GaN substrates[7][8][9], GaN VHFETs [10][11][12] or GaN MOSFETs [13][14][15]). Therefore a key goal of this work is to develop a better understanding of these devices through both numerical simulations as well as experimental demonstrations.

1.1 GaN material system for power electronics

Power electronics applications are typically classified into categories based on the required drive current and voltage as shown in Figure 1.1. On the other hand, to choose the most suitable material for each application, the specific on resistance and breakdown voltage are used as two basic device parameters to evaluate the material system. Baliga's figure of merit (BFOM), shown in Figure 1.2, is the most popular metric for this estimation. For a one-sided abrupt p-n or Schottky junction, the specific on resistance R_{on} for a given breakdown voltage V_{br} can be estimated from [16]

$$R_{on} = \frac{4V_{br}^2}{\epsilon\mu E_c^3}, \quad (1.1)$$

where ϵ is the permittivity, μ is the electron mobility, and E_c is the critical electric field for the material. This relationship assumes that there is a one-dimensional (1D) abrupt junction in a uniformly doped semiconductor.[16] Inspection of both Figure 1.1 and Figure 1.2 shows that GaN and SiC are among the most promising material systems for high power switching applications, with BFOMs exceeding that of GaAs and Si. Ga₂O₃ is another interesting material for high power devices that is currently being developed, but at present this material system is just beginning to

be explored.[17][18] The limit line for diamond looks very good as well, but diamond has significant material growth, fabrication, and device design challenges.

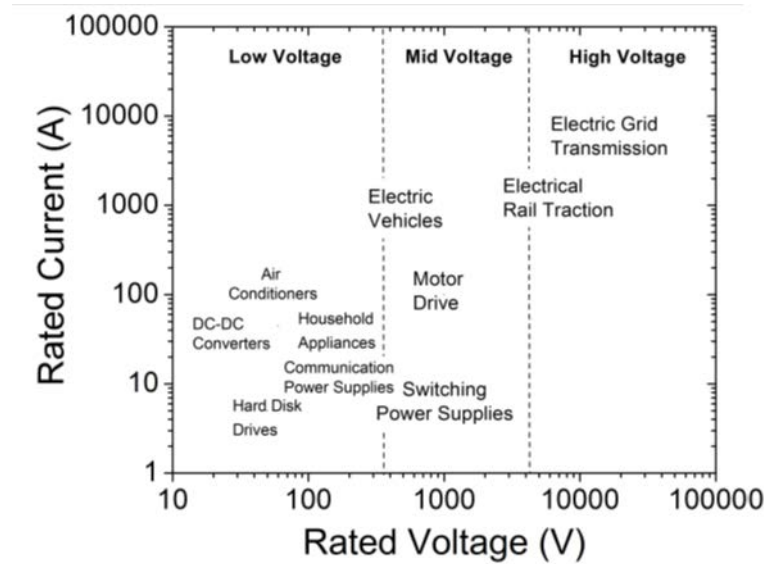


Figure 1.1. Various power electronics applications as a function of the required rated current and voltage. [1]

Power conversion electronics generally require a power diode or transistor along with passive components. High power switch devices must sustain high currents in the on-state and withstand high voltages in the off-state as shown in Figure 1.3. To be efficient, the switch needs to have a low on-resistance and be able to switch quickly between on and off states to minimize device power dissipation. Unfortunately, as of this writing, the demonstrated power switching performance of both current GaN and SiC devices lags behind their respective material limit lines. For GaN, the mobility and critical field are dependent on the dislocation density, and thus depend on the substrate quality. It is reported that the mobility in GaN grown on GaN substrates is

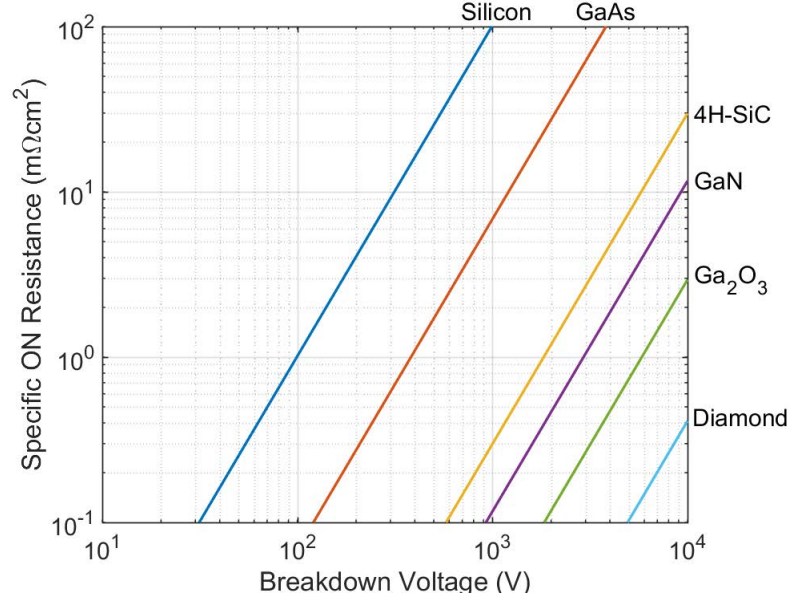


Figure 1.2. Theoretical limits of R_{on} as a function of V_{br} for major semiconductor options. The contours shown reflect the Baliga figure of merit for each material.

significantly higher than that of GaN on sapphire or SiC substrates due to the lower dislocation density.[19][20]

1.2 GaN vertical devices for power switching applications

As is well known, the unique material properties of GaN and related III-N semiconductors, such as a high critical electrical field, large band gap, high saturation electron velocity, good electron mobility, and high thermal conductivity, have made the GaN material system one of the most promising material systems for high-performance optoelectronics as well as power electronics.[21][22] However, the actual performance of many lateral (planar) GaN devices has fallen short of the ultimate performance expected from consideration of fundamental material parameters despite the inherent material advantages of GaN. These performance discrepancies, including effects such as large ideality factors, higher-than-expected reverse saturation currents,

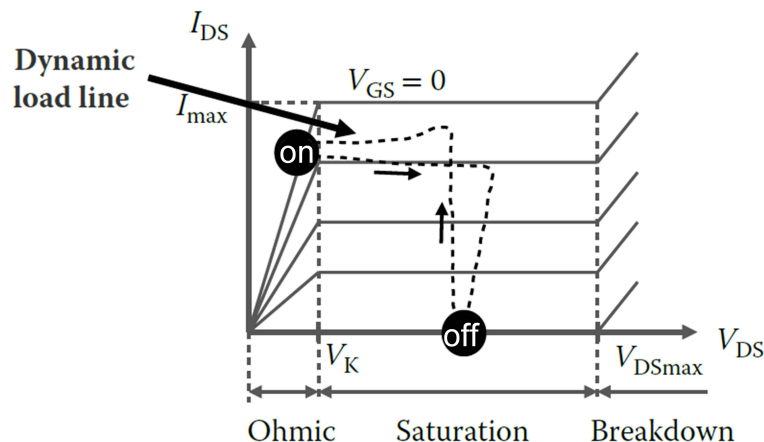


Figure 1.3. Dynamic load line and switching trajectory for a power switching device. The dynamic load line is an example only; the details strongly depend on external circuitry, parasitic device impedances, and mode of operation. [2]

and the inability to support avalanche currents in diodes,[23][24] and the presence of surface- and/or buffer-related effects such as dynamic on-state resistance, current-collapse, and hysteresis in FETs, [25][26] have thus far limited the applications that can be addressed using GaN electronics. In contrast to Si and SiC devices, the majority of GaN devices for power electronics are realized on foreign substrates such as Si and SiC. The root cause of this is related to the difficulty associated with growing large diameter freestanding GaN substrates. Therefore, historically, the development of GaN devices has been on foreign substrates with a lattice constant in the neighborhood of GaN, such as SiC and sapphire. The use of lattice-mismatched non-native GaN substrates (driven by the high cost and limited availability of native GaN substrates) also results not only in large dislocation densities (typically on the order of 10^9 cm^{-2}) but also limits the thermal conductance for through-substrate heat removal.[27][28] Since power devices are often thermally limited, the die size is set by power dissipation and thermal resistance considerations, rather than by current

density limitations.[29][30] Consequently both the thermal and electronic properties play critical roles in power device design.

In addition to its attractive BFOM, GaN and related materials have another special material property: polarization. Because of their wurtzite crystal structure, nitride heterojunctions (e.g. AlGaN/GaN or InGaN/GaN) are characterized by polarization-induced fixed charges at the interfaces.[31] This polarization charge is given by $\rho = -\nabla \cdot P$, where ρ is the fixed charge density and P is the material polarization vector. In III-N materials, P is directed along the c crystal axis, so at abrupt heterojunctions a sheet of fixed charge results. This charge can induce a two dimensional electron gas (2DEG) at the interface.[32] In fact, this is the fundamental basis for the high charge density electron channel in high mobility GaN-based HEMTs.[1][32][33] While HEMTs have been enormously successful for RF power applications, there are two main shortcomings in these lateral structures for high-power applications. One is large chip sizes in designs for high power applications because the breakdown voltage of these devices mainly depends on the spacing between the drain and gate.[34] Another issue is that the peak electric field is located close to the surface, allowing interaction with the significant density of surface states present there.[35] The impact of these surface traps includes suppression of the on current, leading to effects such as dynamic R_{on} [36], knee walkout[37], and current collapse[38]. Using thick passivation layers and multiple metal field plates to distribute the field along the gate-to-drain spacing allows this issue to be mitigated to some degree, but comes at a cost of significant process complexity and increased R_{on} . However, for higher voltage applications, vertical geometry devices can be a better choice, offering the possibility of both a better field distribution as well as allowing the peak electric field to be moved away from the surface. A vertical design also offers economic benefits as a result of reduced chip size as well as high working voltage from the use of a thick low-doped drift layer.

1.3 Epitaxial lift-off (ELO) for GaN based materials

There is a wide range of possible applications for epitaxial lift-off with GaN. For optoelectronics, epitaxial lift-off can reduce the parasitic substrate optical absorption to improve the light extraction for deep-UV LEDs. For emerging applications, epitaxial lift-off may provide a path to flexible III-V electronics/optoelectronics for wearables and medical applications. Of more importance for the work described here, epitaxial lift-off is especially promising for improving the performance and economics of GaN-based power electronics. The performance of vertical power devices can benefit from the reduced electrical access resistance made possible by removal of the substrate through ELO processing. In addition, by removing the substrate and mounting the device directly on a heat sink, the thermal resistance can also be reduced. This enables smaller die sizes, improving the device economics. For example, an analysis using a 2D coupled electro-thermal model indicated that lift-off based vertical FETs supplying 100 amps and 1500 volts could be approximately 31% of the size of devices on full-thickness native GaN substrates for the equivalent thermal resistance and junction temperature[39]. Therefore, 3 times as many die per wafer could be obtained, dramatically lowering cost. In addition, ELO enables re-use of the host substrate (after epitaxial layer removal, the substrate remains intact and can be used for subsequent epitaxial growths). Thus, substrate re-use enables high-cost native GaN substrates with low dislocation densities to be used to generate multiple wafers of epitaxial material, showing a significant economic effect. To achieve these strategic advantages, epitaxial lift-off with GaN requires large-area lift-off with high yield, and no compromise in device performance.

There are well established processes for epitaxial lift off of As and P based materials. More than 5 times substrate reuse has been demonstrated, and these processes have been demonstrated industrially for up to 6 inch wafers.[40][41] However, it is more challenging in nitrides because of the lack of highly-selective, fast etches and

lattice-matched release layers. Lift-off processing of GaN films has been demonstrated by several techniques, including laser lift-off[42], selective etching of release layers[43][44][45], substrate removal by grinding or etching[46], and band gap selective photoelectrochemical (PEC) etching techniques[47][48]. Although laser lift-off is widely used to separate LED devices from sapphire substrates, this process can reduce yield due to cracking of the epitaxial material and is not currently compatible with native GaN substrates due to absorption of the laser wavelengths in the substrate. In this work, a band gap selective PEC technique is explored.[3] An InGaN release layer with band gap well separated from GaN was used. A high-power LED-based light source with peak irradiance at a photon energy below the band gap of GaN was used to ensure that optical absorption occurred primarily in the InGaN release layer. Also, a GaN wafer was utilized as an optical filter to truncate emission tails from the LEDs. Potassium hydroxide (KOH) was used as the electrolyte for high etch rate. To speed the lift-off of large-area films, cross-shaped perforations were defined photolithographically and non-selective PEC etching (using above-band gap illumination with a broadband Hg arc lamp) was performed to etch through the GaN layers and expose the InGaN release layer to the electrolyte.

1.4 Motivation and outline of this work

This work focuses on device development for a series of vertical GaN power devices including Schottky diodes, p-n diodes, and metal-semiconductor-field-effect-transistors (MESFETs) for high efficiency power switching applications, and the benefit to these devices that ELO processing can provide.

As an exploration of the potential of ELO processing to enhance device performance, Chapter 2 presents a comparative study of thin film GaN Schottky diodes formed with and without ELO processing on sapphire substrates. We find that the ELO processing does not result in any detectable degradation of the GaN based

material quality; on the contrary, the leakage current and device electrical characteristics are improved after ELO processing, with improved ideality factor and greatly reduced reverse leakage currents and no significant change in Schottky barrier height. A physical mechanism that is consistent with the experimental observations is the elimination of dislocation-related leakage paths in the devices processed by ELO. The approach described here may be beneficial for GaN-based electronic and optoelectronic devices over a wide range of applications, while also providing a potential route to reuse of low-dislocation native GaN substrates.[49][39][3]

To reach GaN's full potential for high-power switching applications, vertical GaN-on-GaN p-n junctions were studied. As bipolar devices, pn diodes are ideal for studying the impact of processing on material quality or defects, since bipolar devices are very sensitive to recombination centers. For improving device performance and scalability, vertical p-n diodes with ion-implantation edge termination (ET) and sputtered SiN_x passivation with performance approaching the fundamental material limit of GaN have been explored; this work is described in Chapter 3. Vertical power p-n diodes with thick n⁻ GaN drift layers and back-side contacts on bulk GaN substrates have been designed, simulated, and demonstrated experimentally. Ion-implantation isolation and sputtered SiN_x passivation technologies were developed to provide high breakdown voltages over 1.68 kV, while at the same time achieving very low specific on resistances of approximately 0.15 mΩ·cm² thanks to the optimized p-GaN ohmic contacts. With nearly ideal scalability of the optimized devices[50][51], current drive capability as high as 12 A at 4 V has been achieved with 1 mm diameter devices.[52]

To further study the effect of ELO processing on devices on bulk GaN substrates, vertical GaN p-n diodes lifted-off from GaN substrates and transferred to Cu carriers/heat sinks and nominally-identical GaN-on-GaN control devices are compared in Chapter 4. Measurement of the forward current-voltage (I-V) characteristics, breakdown voltages and capacitance-voltage (C-V) characteristics shows that the ideality

factor, turn on voltage, breakdown voltage and C-V are unchanged by the ELO process, suggesting that defect generation due to ELO is not significant. The most significant change in device performance is the increased R_{on} ; this is attributable to the unoptimized Ti/Au contact to the N-face cathode. The thermal properties have also been evaluated. ELO devices exhibit thermal resistance of approximately $8.5 \text{ mK}\cdot\text{cm}^2/\text{W}$, which is approximately 30% less than that for GaN-on-GaN control devices. These results demonstrate that epitaxial lift-off can be used with native GaN substrates, and that it can also improve performance. It may also provide a path to economical deployment of GaN-based power devices.[53][54][55]

Chapter 5 describes the conclusion and possible directions for future work. We developed high performance GaN Schottky diodes and p-n diodes for power switching applications and successfully demonstrated use of the ELO process to improve the device performance and reduce the economic cost. While the focus of the work reported here is on pn junction diodes, power FETs are another very important device to explore. As a step in this direction, we present the design and simulation of vertical GaN power MESFETs. Working devices have been demonstrated experimentally, and the measured characteristics (e.g. I-V measurements) are shown in Chapter 5. Suggestions for possible future work include the further development of GaN FETs for high power applications, and demonstration of these FETs using ELO to improve performance.

CHAPTER 2

THIN-FILM GAN SCHOTTKY DIODES FORMED BY EPITAXIAL LIFT-OFF FROM SAPPHIRE SUBSTRATES

The impact of ELO processing on material quality and device performance has been assessed by starting with thin film GaN Schottky diodes on sapphire substrates. GaN Schottky diodes are a relatively mature device technology and have enabled the first demonstration of GaN devices formed by ELO using band gap selective photoenhanced wet etching of an InGaN release layer.

2.1 Introduction

As noted in Chapter 1, epitaxial lift-off (ELO) is a process technology that enables epitaxial layers to be separated from the original host substrate after growth and transferred to a new carrier wafer. If done successfully, important economic as well as device performance benefits could be obtained, especially for vertical devices on bulk GaN substrates. However, at present, high quality bulk GaN substrates are difficult to obtain and costly, and even epitaxial growth conditions on these substrates are still under investigation. To evaluate the potential of ELO processing for GaN power devices, while work continues to develop bulk GaN technology, ELO from conventional sapphire substrates has been investigated. To date, ELO processing of GaN films has been demonstrated by several techniques, such as lift-off, selective etching of release layers, substrate removal, and band gap selective PEC etching techniques[56][57]. In this work, a band gap selective PEC technique has been used.[3] In general, group-III nitrides can be effectively etched using PEC methods, although they are notoriously

difficult to etch in conventional wet etchants. The ELO approach investigated here uses an InGaN release layer that can be selectively etched using photoenhanced wet etching. Above-band gap illumination is used to generate electron-hole pairs in the semiconductor material. Band gap-selective etching of specific layers within an epitaxial structure can be accomplished by illuminating with wavelengths that absorb only within the layers of interest (i.e. InGaN in this work).

2.1.1 Overview of GaN Schottky diodes

Schottky diodes are unipolar devices which means only one type of charge carrier is responsible for current transmission. In Schottky diodes, the metal-semiconductor work function difference serves as the “blocking junction,” in contrast to the p-n junction in semiconductor p-n diodes. With n-doped material, only electrons participate in the current flow. Compared with a p-n diode, the turn-on voltage is smaller because the metal-semiconductor work function difference is typically smaller than the built-in voltage for a p-n structure. On the other hand, the breakdown voltage of Schottky diodes is typically smaller than for p-n diodes due to the high field at the metal-semiconductor surface. For high-frequency power applications, Schottky diodes are advantageous because they lack minority charge storage effects that can lead to switching loss[58][59]. Therefore, GaN Schottky diodes are potentially attractive for high frequency applications.

2.1.2 Overview of wavelength-selective PEC etching for GaN-based ELO

Wavelength selective GaN ELO offers several important advantages over other ELO methods, including the potential for substrate reuse, low processing-induced stress, control of film thickness by well-controlled epitaxial growth, and compatibility with bulk GaN substrates.[56][57][3] Figure 2.1 illustrates schematically the Schottky diodes used for ELO evaluation. The device structure includes an undoped pseudo-

morphic InGaN release layer ($< 0.1 \mu\text{m}$ thick to retain crystal quality), below the active layers to facilitate lift-off. Diodes were first fabricated on the as-grown epitaxial layers, followed by PEC wet etching to lift off the completed devices. Processing was performed on quarters of 100 mm diameter wafers. As shown in Figure 2.2 (a), the epitaxial lift-off process used was a wavelength-selective wet-chemical PEC etch based on the use of a high-power LED-based UV light source with peak irradiance at a photon energy below the band gap of GaN to ensure that the optical absorption occurred primarily in the InGaN release layer. The PEC lift-off process was performed in a KOH solution, with the sample acting as the anode; a Pt wire served as the cathode of the resulting electrochemical cell. The UV illumination drives the electrochemical dissolution reaction. The sample is illuminated through the substrate (i.e., from the back) to facilitate undercut etching of the InGaN release layer. After epitaxial lift-off, the thin-film device layers were bonded to a Si carrier wafer using SU-8, and the copper support layer was removed by selective wet-chemical etching[3].

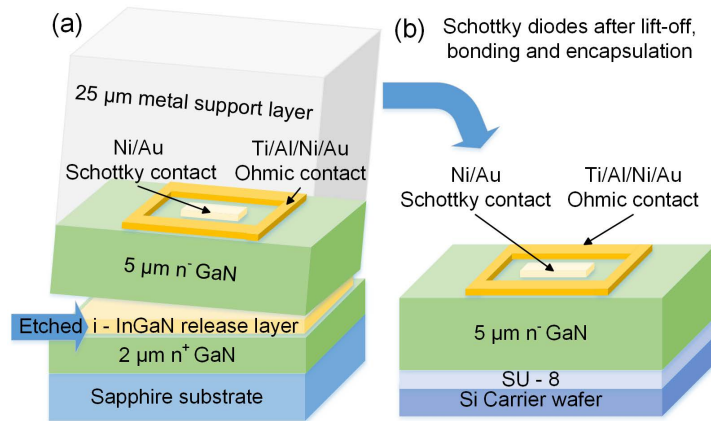


Figure 2.1. Schematic structure of Schottky diode (a) before and (b) after ELO processing.

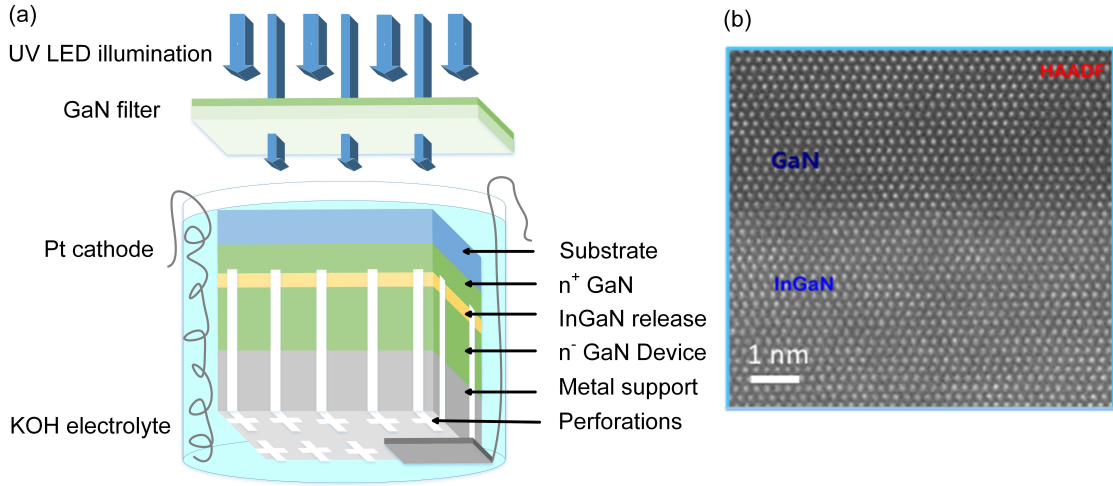


Figure 2.2. Wavelength-selective PEC etch configuration used for the epitaxial lift-off process. (a) Schematic diagram of PEC etch processing. (b) High-angle annular dark-field (HAADF) image showing pseudomorphic InGaN release layer. (This HAADF figure is from Ref.[3])

2.2 GaN Schottky diode fabrication process

For the Schottky diodes reported here, the diodes were fabricated first and tested, and then the ELO process and carrier wafer mounting were performed and the devices tested again to screen for any changes. The details of the fabrication and lift-off processes are described here. Metal Organic Chemical Vapour Deposition (MOCVD) was used to grow the device layer structure, including a $2\ \mu\text{m}$ thick n^+ GaN buffer layer (Si, $3 \times 10^{18}\ \text{cm}^{-3}$), a 90 nm undoped pseudomorphic InGaN release layer ($<0.1\ \mu\text{m}$ thick to retain crystal quality), and a $5\ \mu\text{m}$ n^- GaN device layer (Si, nominally $2 \times 10^{17}\ \text{cm}^{-3}$ on sapphire by collaborators at Qorvo, Inc. (J. Xie, E. Beam). The planar Schottky diodes were metallized with Ti/Al/Ni/Au (30/100/50/50 nm) ohmic contacts. To get good electrical ohmic contact, a thermal anneal at $750\ ^\circ\text{C}$ for 3 min-

utes in N_2 was performed. After ohmic contact formation, Ni/Au Schottky contacts were evaporated on the sample to complete the devices. They were then tested (I-V, C-V, variable-temperature I-V) to establish the “as fabricated” performance of the devices. Prior to lift-off, devices were encapsulated in a thick metal support layer for handling. This 25 micron electroplated metal handle layer provided masking for perforation etching as well as mechanical support for the thin device layers during handling after lift-off as shown in Figure 2.3 (a). For this demonstration, the ELO process was performed by our collaborators at Microlink Devices, Inc. For the band gap selective PEC process, a high-power LED-based light source with a peak wavelength several LED FWHMs (full width at half maximum) above the GaN absorption edge was used for the illumination through the substrate. Concentrated KOH electrolyte and a Pt cathode were used. 1 or 2 mm cross-shaped perforations were used to speed up the release. Under the conditions used here, it took approximately 6 hours to release a film using a 3×3 mm perforation pitch. Figure 2.3(b) shows the successful ELO of one-quarter of a 4 inch wafer; $5 \mu\text{m}$ of GaN remains after the lift-off process. After ELO, the metal-backed film was bonded to a carrier wafer using SU-8 photore-sist. The top-side metal handle layer was removed by selective wet chemical etching as shown in Figure 2.3(c) and (d). The selective wet etchants gave good selectivity against GaN as well as both the Schottky and ohmic metals.

2.3 Comparison of GaN Schottky diodes performance before and after ELO

Material characterization, including Atomic force microscopy (AFM) of the sur-faces, cross-sectional Transmission electron microscopy (TEM) of the epitaxial layers, X-ray diffraction (XRD) and reciprocal-space mapping, and scanning electron micro-scope (SEM) examination of the films before and after lift-off have all been performed by our collaborators at MicroLink, and were found to be virtually unchanged by ELO processing.[3] For example, after lift-off, the samples grown on sapphire before and

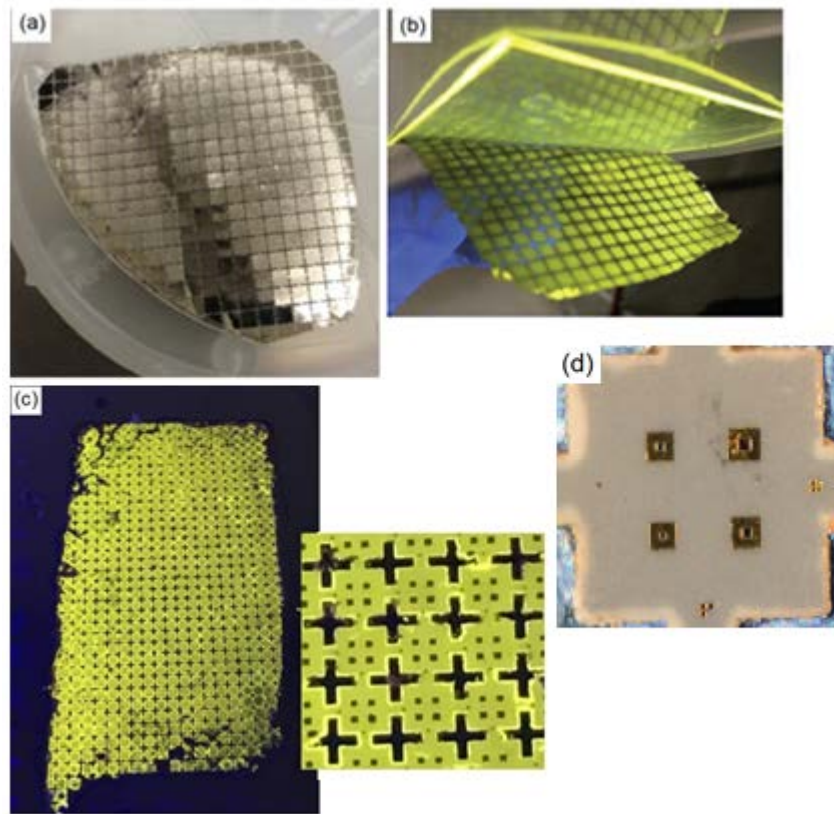


Figure 2.3. Images of lifted-off GaN films and Schottky diodes. (a) Top-side view showing mechanical support metallization after lift-off; (b) view between sapphire substrate and detached GaN/Schottky diodes. UV illumination was used to highlight the yellow-green luminescence on the lifted-off film; (c) & (d) top view of Schottky diodes after bonding to a support substrate and removing the metal mechanical support layer by selective etching.

after ELO showed similar X-ray diffraction peak broadening values, 170 and 200 arc-sec, respectively. These measurement results all indicate that ELO processing did not degrade the material quality. In this section, we will focus on the electrical impacts of the ELO processing. Fabricated diodes were tested immediately after fabrication before metal encapsulation, as well as after the lift-off and bonding process. This work has been previously reported in [49].

2.3.1 Current-voltage characteristics of GaN Schottky diodes before and after ELO

Figure 2.4 shows a typical set of room-temperature current-voltage (I-V) characteristics for the same device with a $40 \times 40 \mu\text{m}^2$ active area before and after epitaxial lift-off. The spacing between anode and cathode contacts is $10 \mu\text{m}$. The turn-on voltage is consistent with the theoretical expectation of 1.0 V for a Ni/Au Schottky contact on GaN if the work function of Ni and the electron affinity of n-type GaN are 5.1 and 4.1 eV, respectively[60][61]. For a reverse bias voltage of -15 V (corresponding to an average depletion-region electric field of 545 kV/cm (at -15 V) as estimated from numerical simulation of Poisson's equation for the device structure in Figure 2.1), the measured reverse current density is 7.2×10^{-2} and $4.0 \times 10^{-3} \text{ A/cm}^2$ for devices before and after ELO processing, respectively. Under forward bias, the as-fabricated devices exhibit two distinct regions: a leaky low-bias region for biases below 0.4 V, and a more ideal diode region at higher biases. In contrast, the leaky low-bias region is eliminated in the characteristics measured after lift-off, as shown in the upper-right inset of Figure 2.4.

2.3.2 Schottky diode temperature dependence

To obtain additional insight into the physics underpinning these results, variable temperature characterization and modeling of these GaN Schottky diodes has been performed. For the measurements reported here, the temperature was set using the

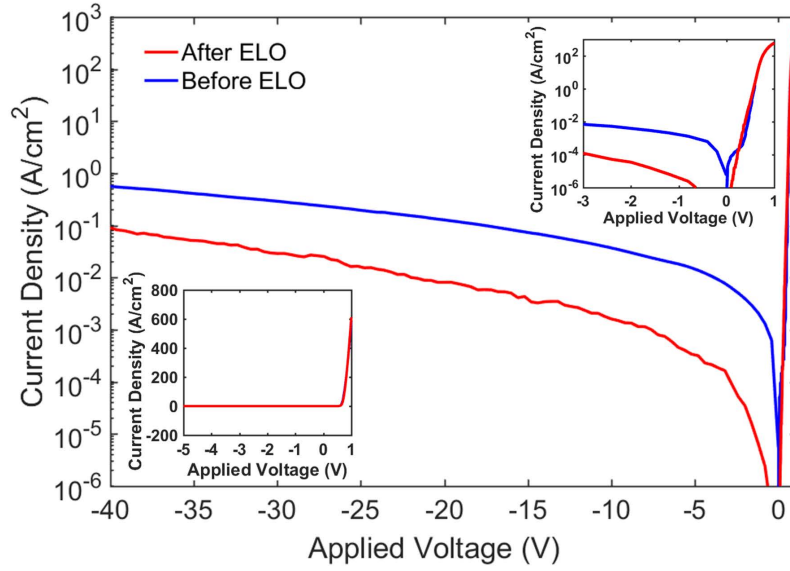


Figure 2.4. Semi-log plot of typical room-temperature I-V characteristics for a typical GaN Schottky diode before and after lift-off processing. The insets show details near the origin in a semi-log scale, as well as the I-V characteristics on a linear scale.

chunk of a variable-temperature wafer probe station. The measured reverse-bias I-V characteristics over temperature of as-fabricated and ELO-processed GaN Schottky diodes are shown in Figure 2.5.

For the full range of temperatures evaluated ($-25\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$), the reverse current is lower for devices after ELO processing than the as-fabricated devices. For ideal Schottky diodes, the characteristics are expected to be dominated by thermionic emission, although other phenomena such as field-assisted tunneling through the barrier and trap-assisted and thermionic generation in the depletion region may contribute to deviation from these expectations[62][63]. For ideal devices dominated by thermionic emission,

$$I = I_O \left[\exp \left(\frac{qV}{nkT} \right) - 1 \right] \quad (2.1)$$

$$I_O = AA^{**}T^2 \left(\frac{-q\phi_B}{kT} \right) \quad (2.2)$$

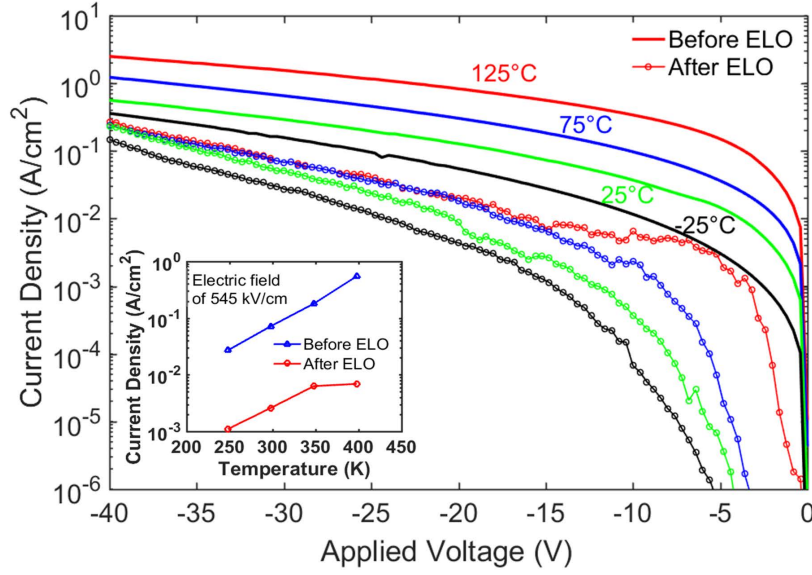


Figure 2.5. Semi-log plot of the reverse-bias I-V characteristics as a function of temperature for GaN Schottky diodes before and after epitaxial lift-off processing. Inset: reverse current density at -15 V (545 kV/cm) vs. temperature.

where ϕ_B is the Schottky barrier height, k is the Boltzmann constant, n is the ideality factor, I_O is the reverse saturation current, A is the Schottky contact area and A^{**} is the effective Richardson constant. As shown in the inset of Figure 2.5, the reverse current density at 545 kV/cm is much lower after ELO, and exhibits significantly reduced temperature dependence.

The measured I-V vs. temperature characteristics under forward bias are shown in Figure 2.6. As can be seen, the turn-on voltage increases as the temperature is reduced, as expected for thermionic emission. In addition, the ELO-processed devices have a modestly higher turn-on voltage than the as-fabricated devices, and also exhibit a much lower leakage current density, reaching the measurement noise floor ($\sim 3 \times 10^{-9}$ A/cm²) for the -25 °C case at voltages below 0.25 V. Effectively, Figure 2.6 shows that the ELO process eliminated the excess forward bias leakage

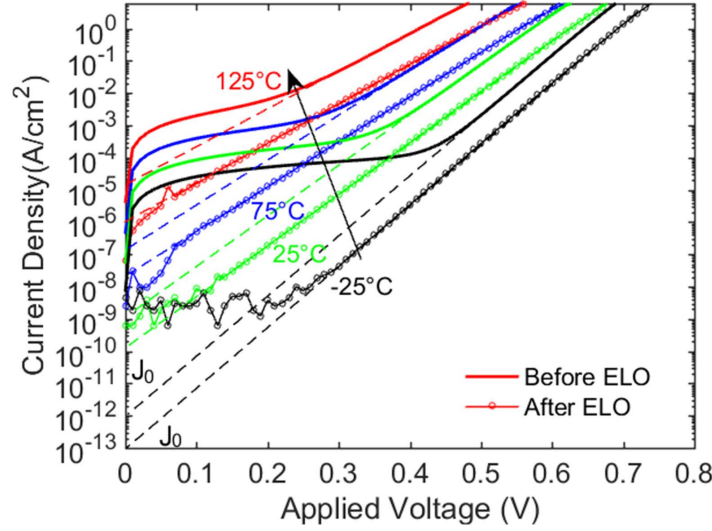


Figure 2.6. Semi-log plot of the forward-bias I-V characteristics as a function of temperature for GaN Schottky diodes before and after epitaxial lift-off processing.

current that is evident in the as-fabricated device measurement results.

2.3.3 Schottky barrier height extraction

The ideality factor and ϕ_B can be extracted from the intercepts and slopes of the linear part of the characteristics in Figure 2.6. The ideality factor improved from 1.12-1.18 before ELO processing to 1.04-1.10 after ELO processing, and the ϕ_B for both pre- and post-ELO devices is close to the theoretical value obtained from the difference between the Ni workfunction and GaN electron affinity[64][65], as shown in Table 2.1. As an additional check, the modified Norde method was applied to extract ϕ_B since the extrapolated I_O from the I-V vs. temperature plot can be unreliable for small applied voltages or if there is appreciable recombination current or series resistance[66]. The Norde function $F(V)$, defined by[67]

$$F(V) = \frac{V}{2} - \frac{kT}{q} \ln \left(\frac{I}{AA^{**}T^2} \right), \quad (2.3)$$

is plotted in Figure 2.7. The applied voltage V_O corresponding to the minimum of the Norde function can be used to extract ϕ_B using[68]

$$\phi_B = F(V_O) + \frac{V_O}{2} - \frac{kT}{q}. \quad (2.4)$$

For ELO-processed diodes, as shown in Figure 2.7, $F(V)$ depends linearly on V for low voltage except for the $V < 0.25$ V region at -25 °C where the true device current is obscured by the measurement noise floor. However, the as-fabricated diodes exhibit leaky low-bias regions. This contributes to the additional minima in $F(V)$ observed for $V \leq 0.1$ V in Figure 2.7, thus should not be considered when extracting V_0 . For large V , $F(V)$ approaches a straight line with slope of $1/2$ as expected from Equation 2.3. Table 2.1 compares the ideality factors and extracted barrier heights for diodes before and after lift-off over temperature. As shown in Table 2.1, the barrier height values agree well with the theoretical expectations for Ni/GaN contacts across both methods used and the full temperature range evaluated, and the ideality factors are well behaved, suggesting the diode behavior is nearly ideal. It should be noted that for the data in Figures 2.5, 2.6, 2.7, the self-heating of the device is estimated to be below 0.5 K from estimates of thermal conductivity of the substrates and the low power dissipation in the devices.

2.3.4 Trap and doping effects

Cyclic I-V measurement with a voltage sweep rate of 1 V/s and cyclic C-V measurement with a voltage sweep rate of 0.2 V/s were performed to look for hysteresis as a signature of trapping in the devices. As shown in Figure 2.8, a small amount of I-V hysteresis was apparent in the as-fabricated devices; this disappeared after ELO processing. For the C-V measurements (not shown), no hysteresis was found in either case. The C-V characteristics were also used to validate the doping concentration

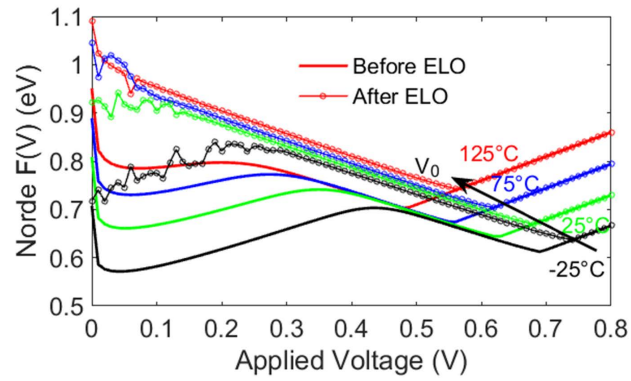


Figure 2.7. Plot of the Norde function over bias and temperature, to facilitate barrier height extraction.

TABLE 2.1

COMPARISON OF BARRIER HEIGHTS AND IDEALITY FACTORS
OVER TEMPERATURE FOR SCHOTTKY DIODES BEFORE AND
AFTER ELO PROCESSING

	T(°C)	n	ϕ_B I-V (eV)	ϕ_B Norde (eV)
Before ELO	125	1.18	0.99	0.99
	75	1.16	0.89	0.90
	25	1.13	0.91	0.95
	-25	1.12	0.87	0.96
After ELO	125	1.10	0.99	0.99
	75	1.08	0.99	1.00
	25	1.05	0.91	0.95
	-25	1.04	0.94	1.00

in the epitaxial layers,[69][70] with a geometric edge correction applied due to the small device area.[71][72] The obtained doping concentration was found to be uniform through the depletion layer thickness and unchanged before and after ELO processing, with a value of approximately $2.5 \times 10^{17} \text{ cm}^{-3}$. In addition, variable-frequency C-V measurements from 2 kHz through 1 MHz were performed before and after ELO processing. As expected for Schottky diodes, no frequency dispersion was observed, and no significant differences between the C-V characteristics before and after ELO processing could be discerned. These observations suggest that ELO processing does not have a discernible impact on bulk material properties or trap generation, but does reduce the leakage current.

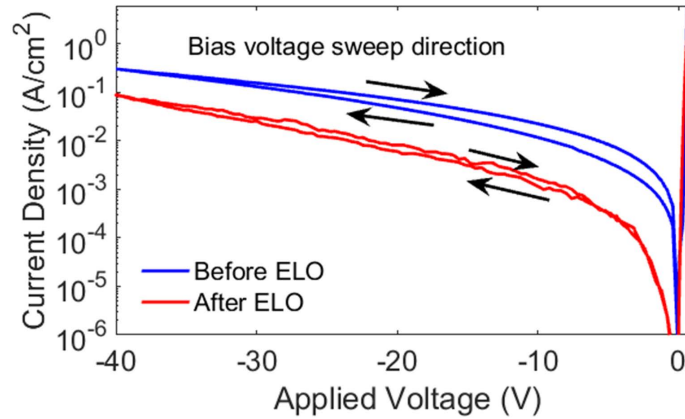


Figure 2.8. Cyclic I-V measurement, scan rate of 1 V/s.

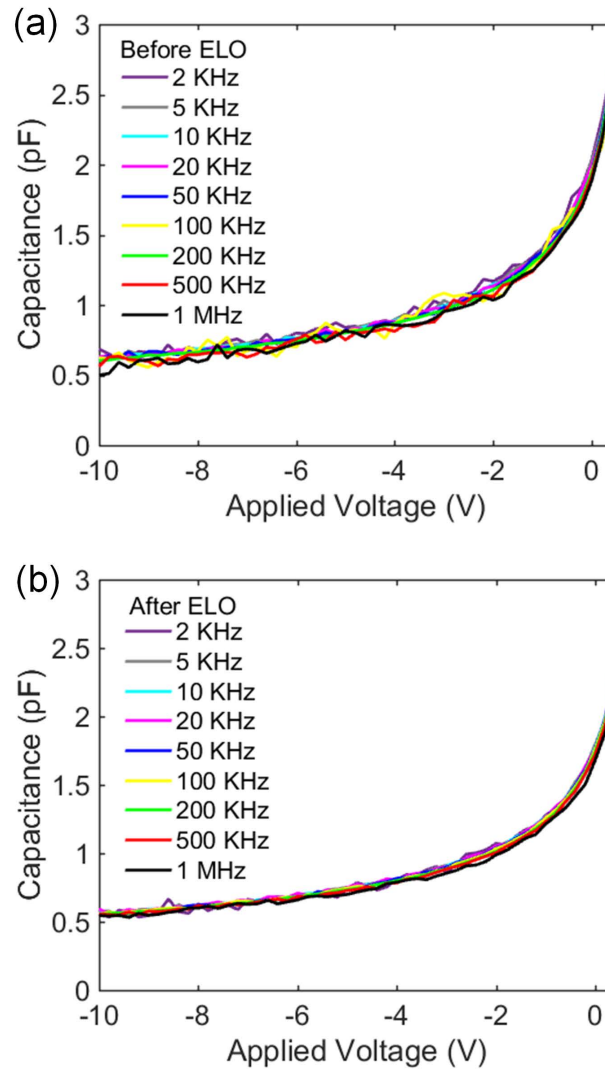


Figure 2.9. Measured C-V characteristics (a) before ELO and (b) after ELO processing. In both cases, no frequency dispersion is observed, and no significant differences are seen before or after ELO.

2.3.5 Physical interpretation

As noted above, the fabricated Schottky diodes exhibit substantially reduced leakage after lift-off processing in both reverse and low forward bias conditions. On the other hand, the Schottky barrier height is found to be constant, while the ideality factor improves after lift-off. Figure 2.10 illustrates schematically a proposed mechanism to explain these observations. These GaN-based epitaxial films, grown on sapphire, contain a high density of dislocations. Vertical leakage current paths associated with dislocations having screw character have been observed previously.[73][74] In the case of the Schottky diodes fabricated here, these conductive dislocations form shunt paths through the devices. These are shown, for illustration purposes, as the dashed gray vertical lines in Figure 2.10. For the devices before ELO processing, these dislocations pass through the n^- GaN Schottky layer, through the InGaN release layer, and into the n^+ GaN buffer. This heavily-doped buffer and the quantum well associated with the InGaN release layer can provide a low-resistance lateral current path between the vertical dislocations, as illustrated with the blue arrows in Figure 2.10 (a). In contrast, for the ELO-processed devices the release layer and n^+ buffer are removed, eliminating this lateral path connecting the dislocation shunt paths. These leakage paths are thus disconnected by the insulating carrier wafer bond, eliminating the leakage path. As a consequence, the devices after epitaxial lift-off show more nearly ideal characteristics, as illustrated by the curved red arrows in Figure 2.10.

2.4 Conclusion

This work resulted in the first demonstration of GaN Schottky diodes fabricated using a large-area epitaxial lift-off process. The process is capable of lifting off large areas—one quarter of 100 mm wafers was demonstrated here. Critically, the devices before and after liftoff exhibit the same Schottky barrier heights with no discernible

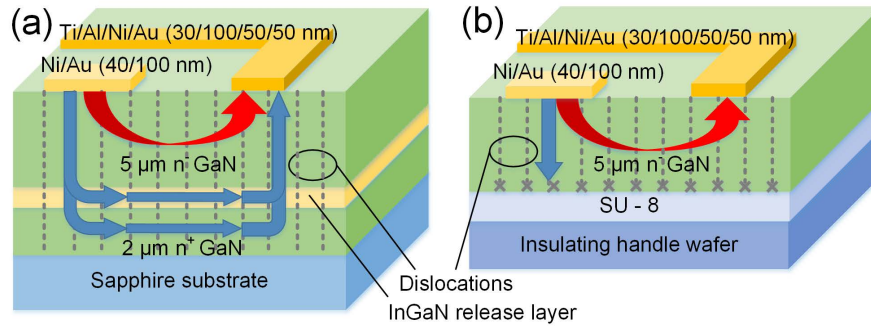


Figure 2.10. Schematic illustration of possible mechanism for the performance improvement in ELO-processed GaN Schottky diodes. The red arrow denotes the ideal thermionic Schottky current contribution, while the blue arrows illustrate the leakage paths. The leakage paths include a vertical component along dislocations, and a lateral component in the InGaN release layer quantum well and the n^+ GaN buffer. Elimination of these two layers, and replacement of them with an insulating bond and carrier wafer, eliminates this leakage mechanism.

device or material quality degradation. In fact, the device performance is improved by liftoff, likely due to elimination of dislocation-related leakage paths through the buffer and release layers. Thus this study suggests that epitaxial liftoff may enable new levels of GaN-based device performance and economics, including vertical GaN devices on high thermal conductivity substrates, substrate re-use for low cost devices, and flexible GaN-based electronics and optoelectronics.

CHAPTER 3

VERTICAL GAN P-N DIODES ON BULK GAN SUBSTRATES

3.1 Overview of GaN p-n diodes

As discussed in Chapter 1, vertical GaN power devices based on bulk GaN substrates are promising for delivering high breakdown voltage, low power loss, and fast switching performance due to the exceptional material properties of GaN.[75][76][77][78] As a result, GaN devices are attractive for their potential for high performance and efficiency as well as their potential reduction of the size and weight of power supplies and converters.[78][79][80] While GaN-based HEMTs grown on foreign substrates have been very successful for RF applications, progress has been more limited for diodes and FETs intended for higher voltage levels. For GaN diodes in particular, there are several challenges. First, vertical devices such as diodes are sensitive to high defect densities [81]; extended defects such as dislocations can act as shunt paths, while point defects can act as recombination centers. Both can seriously compromise pn junction performance. Another challenge arises from the difficulty in fabricating high quality p-GaN ohmic contacts with low resistance, which is essential for achieving high performance, efficiency, and reliability of bipolar GaN devices [82].

Despite these challenges, recently, vertical GaN power p-n diodes with record high Baliga's figure of merit (BFOM) and critical electric field have been demonstrated (see e.g.,[7][8][9][83][84][4][85][86][87][88][89]). In addition to the value of p-n diodes in circuit applications, they are also an excellent vehicle for fundamental study of semiconductor material quality. However, in order to achieve the best performance (and

thus allow the most direct study of the material quality), the fabrication processing and structure design, such as p-GaN ohmic contact, isolation process, junction termination extension (JTE), and surface passivation need to be developed and optimized. In this chapter, efforts in this direction are discussed.

For the p-n diodes in this work, the p-type GaN was doped with Mg and n-type GaN was doped with Si. All samples were grown using an Aixtron close-coupled showerhead (CCS) metal-organic chemical vapor deposition (MOCVD) reactor using TMGa, TMIIn, NH₃, Si₂H₆ and Cp₂Mg precursors for Ga, In, N, Si and Mg sources, respectively, by our collaborators at Qorvo. Compared to Schottky diodes such as those described in Chapter 2, p-n diodes have lower reverse current and can more easily be designed to achieve high breakdown voltage. However, p-n junctions have larger forward voltage drops, and also exhibit minority charge storage effects that can limit their frequency of operation.

For p-n junctions, the expected current-voltage characteristics can be expressed as[84][70]

$$J = J_{d0} \left(e^{qV_a/kT} - 1 \right) + J_{SHRr0} \left(e^{qV_a/2kT} - 1 \right) + J_{r0} \left(e^{qV_a/kT} - 1 \right) \quad (3.1)$$

where the first term represents the diffusion current J_d , the second term is the Shockley-Read-Hall (SRH) recombination current density J_{SHRr} inside the depletion region, and the third term is the band-to-band radiative recombination current density J_r . For an ideal diode, the ideality factor n from the diffusion and radiative components should be 1, while the n for the SRH-related term should be 2. J_{d0} , J_{SHRr0} , and J_{r0} represent the bias insensitive terms. The applied voltage, V_a ($V_a = V - JR_s$) is the applied voltage over the intrinsic junction, and R_s is the total specific series resistance (extends to the junction) of the diode. The pre-factor for the radiative recombination current, J_r inside the depletion region, is expressed as:

$J_{r0} = 2qbn_i^2W$, where n_i is the intrinsic carrier concentration in GaN, W is the width of the depletion region, and b is the radiative recombination coefficient of GaN. Based on the value of b (i.e. $b = 0.47 \times 10^{-10} \text{ cm}^3/\text{s}$ at $T = 300 \text{ K}$ and $n = 1 \times 10^{18} \text{ cm}^{-3}$) reported in [90], J_r is negligible compared with the other two current components for these devices in the voltage range examined here.

Capacitance-voltage (C-V) profiling is an important tool to confirm the effective junction doping profiles[7][84]. For abrupt p^+/n^- junctions, the doping profile can be extracted from $1/C^2$ [70], using

$$N_d = \left| \frac{-2}{q\epsilon_s A^2 \left(\frac{d(1/C^2)}{dV} \right)} \right|, \quad (3.2)$$

and

$$W = \frac{\epsilon_s A}{C}, \quad (3.3)$$

where N_d is the doping concentration, W is the depletion width and ϵ_s is the dielectric constant of GaN.

To achieve high breakdown voltage, a lightly-doped drift layer is essential. A doping concentration of $1.0\text{-}1.5 \times 10^{16} \text{ cm}^{-3}$ is needed to achieve breakdown voltage in the 1.5-2 kV range. In this work, the doping concentration measured for the drift layer in our structures by both capacitance-voltage measurement as well as secondary-ion mass spectrometry (SIMS) as shown in Figure 3.1. As can be seen in Figure 3.1, our crystal growth collaborators have successfully achieved n-type doping of approximately $1.0\text{-}1.2 \times 10^{16} \text{ cm}^{-3}$. This doping is sufficiently low to enable breakdown voltages $> 1500 \text{ V}$.

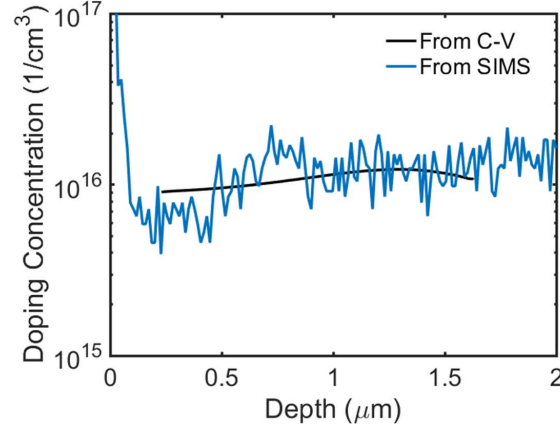


Figure 3.1. The doping profiles extracted the slope of $1/C^2$ and SIMS.

3.2 Pd/Ni/Au on p-GaN ohmic contact with low contact resistance

Although the GaN material system has become one of the most promising options for power electronics and high-performance optoelectronics, low-resistance ohmic contacts remains a challenging issue for further improvement of the overall performance and reliability of GaN devices. For n-type GaN, Ti-, Al- and Mo- based metalization schemes have been demonstrated to form good quality ohmic contacts with low specific contact resistances in the range from $\sim 10^{-5}$ to $\sim 10^{-8} \Omega \cdot \text{cm}^2$. [91][92] However, p-type contacts remain challenging. This has led to an intense effort to develop contact materials and strategies, such as metal alloys[93][94][95], metal oxides and carbon nanotubes[96][97], interband tunneling structures[98], as well as surface and thermal treatments[99][100]. A review of contacts to p-GaN can be found in Ref[82]. However, despite significant effort, it is still difficult to achieve high quality ohmic contact ($< \approx 10^{-4} \Omega \cdot \text{cm}^2$) to p-type GaN because of two main impediments. The first results from the difficulty in achieving high hole concentrations in p-GaN ($\geq 10^{18} \text{ cm}^{-3}$) because of the large activation energy of the Mg acceptors ($\sim 0.17 \text{ eV}$) and the tendency to form Mg-H complexes. The second complication arises from the

absence of appropriate metals or conducting oxides with work functions larger than that of p-type GaN (a work function of $\sim 7.5\text{eV}$ would be desired, as estimated from GaN's 3.4 eV bandgap and 4.1 eV electron affinity).[101] As part of the process development work for p-n junction diodes, low-resistance Ni/Au and Pd/Ni/Au ohmic contacts have been developed for p-GaN.

3.2.1 Surface treatment

Pre-metallization surface treatment and thermal treatment after contact metal deposition are two important processes for forming p-GaN ohmic contacts. In terms of pre-treatments, both acid and caustic solutions, such as HCl, HF, $(\text{NH}_4)_2\text{S}$ and KOH have been used for p-GaN surface treatment to remove the thin surface oxide and other impurities on the surface of p-GaN and provide benefits from shifting the surface Fermi level. [102][100][103]

For the contact process optimization effort performed here, each of these solutions, and selected sequential combinations, were evaluated for creating ohmic contacts on MOCVD grown p-GaN with moderate Mg doping. For this surface pretreatment study, Ni/Au contact metallization was used. Table 3.1 lays out the combinations that have been evaluated. In Table 3.1, “Step 1” denotes treatment performed before lithography to define the p-GaN ohmic contact, while “Step 2” denotes the surface treatment right before the sample is loaded into the evaporator for contact deposition. Circular transfer length method (CTLTM) patterns with 30 μm inner contact diameter and Ni/Au (20/50 nm) p-GaN ohmic contact metallization were used to compare these surface treatments. All of the acid and caustic solutions studied improved the contacts relative to a “no treatment” condition. The best recipe—shown in bold type in Table 3.1—consisted of using BHF and diluted HCl surface treatments both before lithography and immediately before metallization.

TABLE 3.1

SURFACE TREATMENT TESTS FOR P-GaN/Ni/Au OHMIC
CONTACTS

Step 1	Step 2	$R_{sh}(k\Omega/\square)$	$\rho_c(\Omega \cdot cm^2)$
BHF & HCl	BHF & HCl	11	1.0×10^{-4}
BHF & HCl	$(NH_4)_2S$	13	1.3×10^{-4}
BHF & HCl	KOH	11	4.2×10^{-4}
KOH	$(NH_4)_2S$	12	1.6×10^{-4}
BHF & HCl	w/o	12	2.0×10^{-4}
w/o	w/o	N/A	5.3×10^{-2}

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3.2.2 Thermal annealing

Thermal treatment is another key process for p-GaN ohmic contact formation. It has been suggested that post-metallization anneals may assist in removal of hydrogen atoms bonded with Mg, as well as the formation of conductive metal oxides on the surface of p-GaN.[99][104] In this work, thermal annealing tests using circular transfer length method (CTLTM) test structures for both Ni/Au (20/50 nm) and Pd/Ni/Au (30/20/50 nm) metallizations were compared.[104][93][95][94] In addition, it has previously been suggested that the presence of O_2 in the anneal ambient could be beneficial for low contact resistance.[104][99] Air, N_2/O_2 mixtures, and pure N_2 were compared; no improvement with added O_2 was observed for the process conditions explored here. For the annealing condition comparisons reported here, a duration of 1 minute and N_2 ambient was selected. Table 3.2 shows that Pd/Ni/Au without annealing gave the lowest contact resistance, $4.2 \times 10^{-5} \Omega \cdot cm^2$, and a sheet-

resistance of $10 \text{ k}\Omega/\square$. This specific contact resistance is approximately ten times lower than for un-annealed Ni/Au contacts, and five times better than Ni/Au contacts annealed at 750°C (the optimum temperature for Ni/Au contacts in Table 3.2). For the Pd-based contacts, when the annealing temperature is higher than 600°C , the I-Vs from CTLM test are not linear, preventing accurate extraction of the sheet resistance and contact resistance. For all of these samples, the optimum 2-step BHF/HCl surface treatment process was used.

TABLE 3.2
ANNEALING TESTS FOR Ni/Au (20/50 NM) AND Pd/Ni/Au (30/20/50
NM) ON P-GaN OHMIC CONTACTS

T	$R_{sh}(k\Omega/\square)$	$R_{sh}(k\Omega/\square)$	$\rho_c(\Omega \cdot cm^2)$	$\rho_c(\Omega \cdot cm^2)$
	Ni/Au	Pd/Ni/Au	Ni/Au	Pd/Ni/Au
w/o	11	10	4.2×10^{-4}	4.2×10^{-5}
400°C	12	12	4.5×10^{-4}	1.8×10^{-3}
500°C	13	13	2.3×10^{-4}	2.6×10^{-3}
600°C	13	13	2.1×10^{-4}	1.7×10^{-2}
700°C	12	N/A	1.8×10^{-3}	N/A
750°C	10	N/A	2.0×10^{-4}	N/A
800°C	11	N/A	1.5×10^{-3}	N/A

3.2.3 CTLM test

To verify the quality of the ohmic contacts provided using the optimal recipe in Table 3.2, the measured I-V and total resistance versus gap spacing is shown in Figure 3.2 (a) and (b). Linear I-V characteristics and a good fit to the resistance vs. gap characteristics confirm that a high-quality ohmic contact has been achieved. This is a promising ohmic contact compared with other metal alloys ohmic contact on p-GaN with moderate carrier concentration.[101][94] For comparison, equivalent measurement results for n-type contacts are also shown in Figure 3.2 (c) and (d).

3.3 Vertical p-n diodes on bulk GaN substrates with ion-implanted isolation

As an initial step of exploring vertical GaN p-n diodes, mesa isolated devices on bulk GaN were studied first [105]. The results showed that mesa isolated devices exhibit excess leakage currents that compromise device performance as shown in section 4.2. To avoid mesa sidewall related leakage currents and the complications (e.g. field plates, etc.) required to terminate the junction fields in a mesa isolated structure[7][84], fully vertical p-n diodes with backside cathode contact and an ion-implantation based edge termination with SiN_x surface passivation layer have been investigated. In this section, we demonstrate high performance GaN p-n junction diodes on bulk GaN substrates with high-voltage and high-current capability.[50][51][52]

3.3.1 Device structure and fabrication process

The epitaxial layers were grown by MOCVD on 2 inch diameter native GaN substrates. Figure 3.3 depicts the device structures that have been evaluated. From the bottom to the top, the epi-layers consist of a 1 μm thick n-type GaN buffer layer doped with Si with a concentration of $2 \times 10^{18} \text{ cm}^{-3}$, a lightly doped n-type GaN drift layer (doping concentration of $1 \times 10^{16} \text{ cm}^{-3}$) with thickness from 8 to 12 μm ,

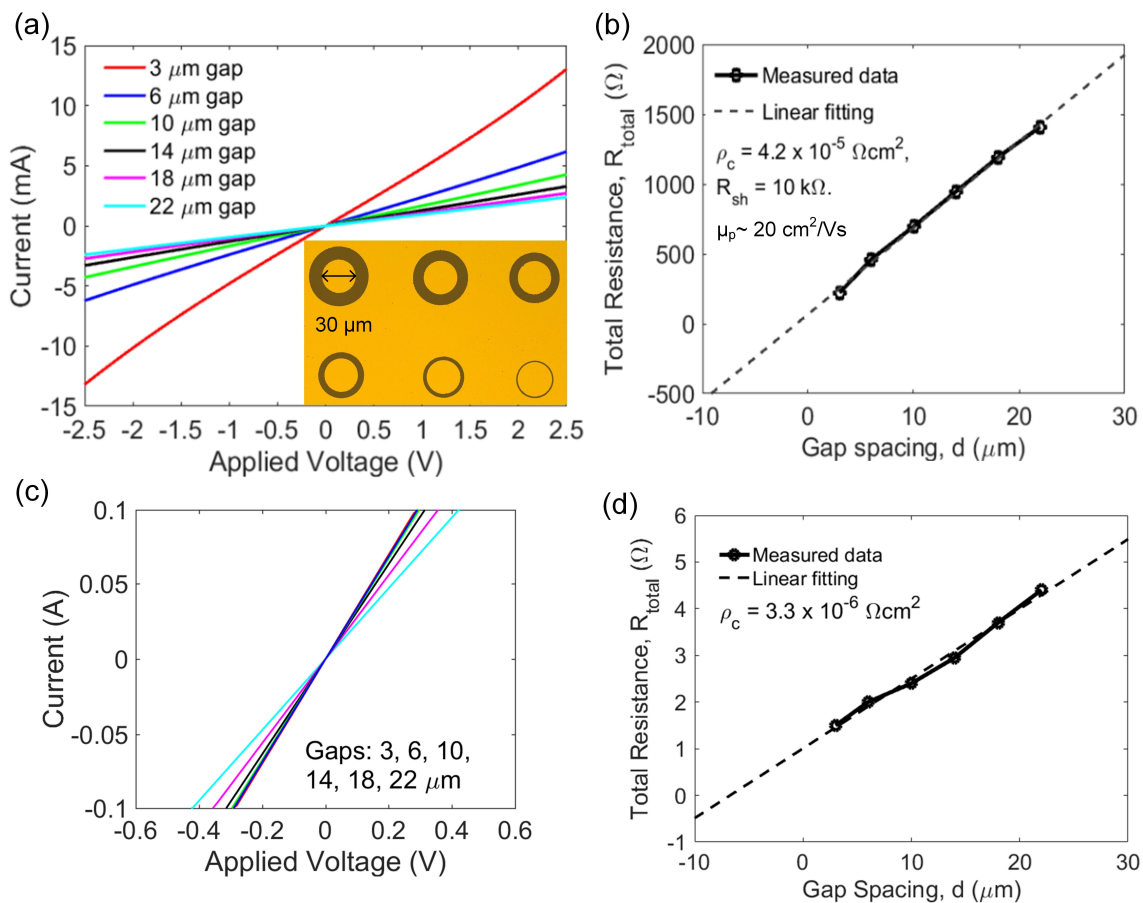


Figure 3.2. CTLM tests for p-type GaN/Pd/Ni/Au (30/20/50 nm, without annealing) ohmic contacts (on CTLM patterns with 30 μm inner diameter) and n-type GaN/Ti/Al/Ni/Au (30/100/50/50 nm without annealing). (a) Measured current-voltage characteristics with gaps from 3 to 22 μm . (b) Measured total resistance versus gap spacing for p-GaN contacts. $4.2 \times 10^{-5} \Omega\text{cm}^2$ specific contact resistance and 10 $\text{k}\Omega/\square$ sheet resistance were extracted from this CTLM test. (c) Measured current-voltage characteristics with 3 to 22 μm gaps for n-GaN contact test. (d) Measured total resistance versus gap spacing. $3.3 \times 10^{-6} \Omega\text{cm}^2$ specific contact resistance was extracted from this CTLM test.

a 450 nm p^+ GaN layer, doped with a Mg concentration of $3 \times 10^{19} \text{ cm}^{-3}$, and a 20 nm heavily doped p^{++} GaN layer (Mg concentration $> 10^{19} \text{ cm}^{-3}$) to facilitate ohmic contacts.

The fabrication process used is outlined below. First, the ohmic contact to the n-GaN was formed on the back-side of the GaN wafer; a Ti/Al/Ni/Au (30/100/50/100 nm) metal stack was used. For the p-type contact, Ni/Au (20/500 nm) was used. A fairly thick Au top layer was used to reduce probe resistance on large devices[106]). The anode metal patterns were made circular to avoid field concentration from corners at high voltages. The diodes were isolated using a N damage implant, and also include a single-stage junction termination ring to improve the breakdown [8]. The isolation and termination was formed by first etching a ~ 160 nm deep and $20 \mu\text{m}$ wide ring into the p-GaN layer at a distance of $50 \mu\text{m}$ from the edge of the p-contact metallization. This ring acts to diffuse the lateral extent of the junction termination. After etching, a photoresist implant mask (AZ1813, $1.6 \mu\text{m}$ thick) is defined to protect the metallization from the implant. A $5 \mu\text{m}$ margin beyond the metal edge was used to ensure the implant did not encroach on the device's active area. Device fabrication was then completed with a nitrogen triple implant. The details of the implant and the design of the edge termination structure will be discussed in the next two subsections. Finally, the device was covered by 250 nm of sputtered SiN_x for surface passivation.

3.3.2 Ion-implantation process design and simulation

Achieving high breakdown voltages requires low-doped drift layers, in the case of the structures evaluated here, approximately $1 \times 10^{16} \text{ cm}^{-3}$. In addition, however, the high fields at the edge of the active region must also be managed. This is the role of junction edge termination (ET) structures. In a well-designed ET, the electric field can be diminished which prevents the onset of localized impact ionization and

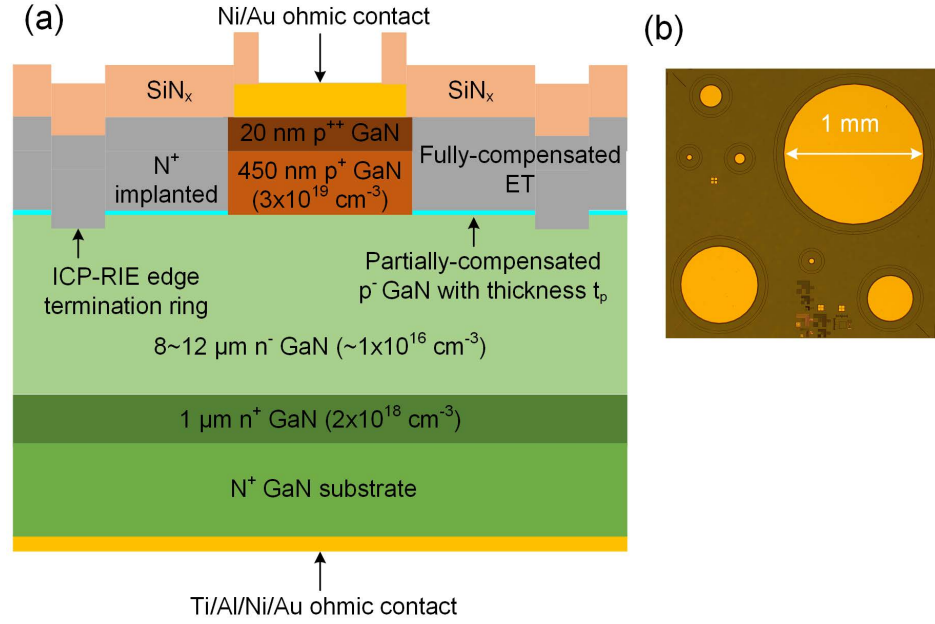


Figure 3.3. (a) Cross-sectional schematic and (b) top view of a fabricated p-n diode with ion-implanted ET and SiN_x passivation.

avalanche breakdown along the device periphery. Effective termination schemes are well developed for mature high power semiconductor systems such as Si, GaAs and SiC; these typically rely on tailoring the lateral doping profile in the devices, and are implemented using diffusion or implantation. Unfortunately, p-type doping of GaN by implant and diffusion is difficult, and so other approaches are required. Implantation-based isolation has been studied in the GaN material system using N^+ , Ar^+ , O^+ , H^+ , He^+ , F^+ , Mg^+ , Kr^+ , and Zn^+ ions. [8][107][108][109] As can be seen, most of these implant recipes are either inert (Ar, N, He, Kr) or form deep levels or complexes (O, H, Zn). Compensated regions formed from ion implantation [8][108], beveled oxide field plates [9][7], and other structures [110][111] have been reported to create ETs in GaN power devices. In this work, we used N^+ ion implantation to form a damage-based edge termination.

For ET designs of the type investigated here, the top p-type layer is compensated

by implant damage, leading to a nominally insulating layer that can distribute the field laterally by fringing. To compensate for the “block doping” profile in the device, a flat defect density profile from the surface of the p-GaN to nearly the bottom of this layer is needed. For the work shown here, triple nitrogen implants were used to create the compensated region. A simulation of defect density versus depth, calculated using Stopping and Range of Ions in Matter (SRIM),[112] is shown in Figure 3.4. For the 450/20 nm p⁺/p⁺⁺ GaN epitaxial anode layers in our devices, energies of 30, 100, and 220 keV at doses of $3.3 \times 10^{12} \text{ cm}^{-2}$, $6.7 \times 10^{12} \text{ cm}^{-2}$ and $1.2 \times 10^{13} \text{ cm}^{-2}$, respectively, were found to result in an approximately flat profile. The superposition of these implants results in a constant number of defects ($\sim 4 \times 10^{20} \text{ cm}^{-2}$) to a depth of 300 nm, followed by a gradual tailing off at greater depths. Using this triple ion-implantation recipe, the implant profile is expected to fully compensate the top 440 nm of the structure (i.e. the defect density exceeds the Mg concentration to this depth), leaving approximately 30 nm of p-type GaN partially compensated. This remaining p-GaN layer can help to distribute the electric field laterally and to increase the voltage at which impact ionization occurs.[8] By adjusting the highest ion implantation energy, the range of the implant (and thus the thickness of the partially compensated layer, t_p (light blue region in Figs. 3.3 and 3.4), can be fine-tuned to achieve the highest breakdown voltage.

To study the effect implantation conditions and surface dielectric passivation have on device breakdown, the device structure with an 8 μm drift layer was simulated numerically using Synopsys Technology Computer-Aided Design (TCAD). To explore the design space for the ET, the thickness of the partially compensated p-type GaN layer, t_p , was varied over the range from 0 to 80 nm. Figure 3.5 shows the lateral electric field for several partial-compensation thicknesses, t_p . When the p-GaN layer is fully compensated ($t_p = 0 \text{ nm}$, red curve), the electric field peaks at the corner formed by the metallurgical junction and the edge of the implant. The inclusion of

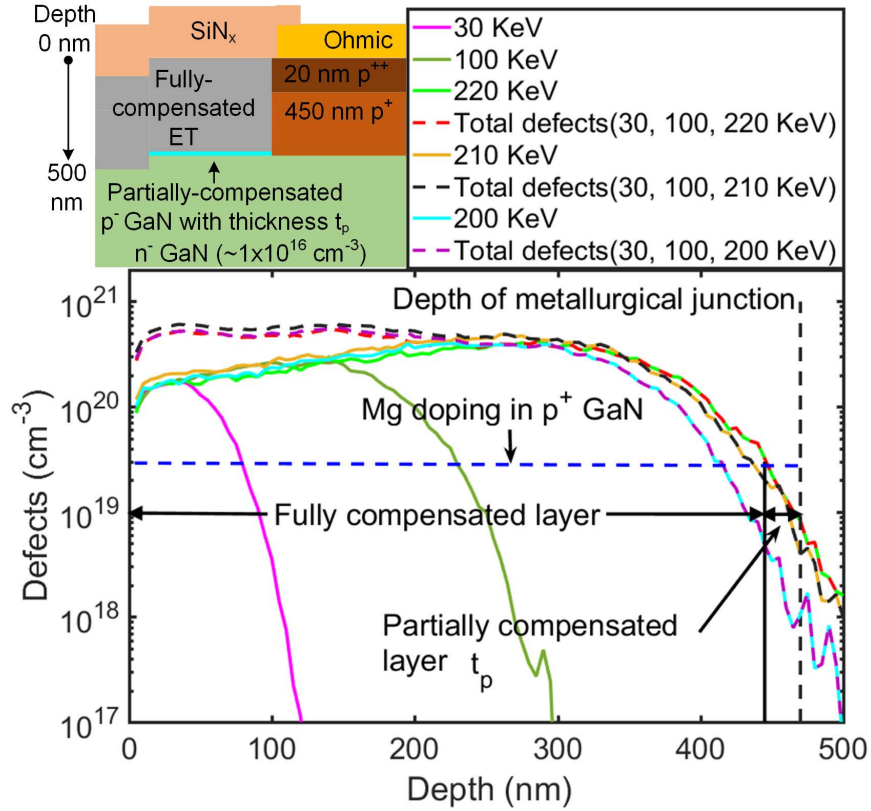


Figure 3.4. Detail of ET structure and SRIM simulation of a triple energy implant for a partially compensated ET. The implant-induced defect concentration is smaller than the Mg doping (blue dashed line) from 440-470 nm in the p-GaN with the highest ion-implantation energy of 220 keV, leading to partial compensation layer thickness, t_p , of 30 nm.

a partially-compensated layer between the anode region and the shallow ring etch results in a second peak in the field that increases the breakdown voltage. As t_p approaches the optimum value ($t_p = 40$ nm, blue curve), the electric field peaks are evenly spread between the edge of the anode region and the transition to the fully-depleted region due to the edge termination etch ring. When t_p is larger than optimal ($t_p = 80$ nm, green curve), the partially-compensated region is not depleted in reverse bias and the electric field peaks prematurely at the edge where the device becomes fully depleted. This approach is conceptually similar to the Reduced Surface Field

(RESURF) approach, except in this case the surface field tailoring is done through partial depletion of a buried layer.

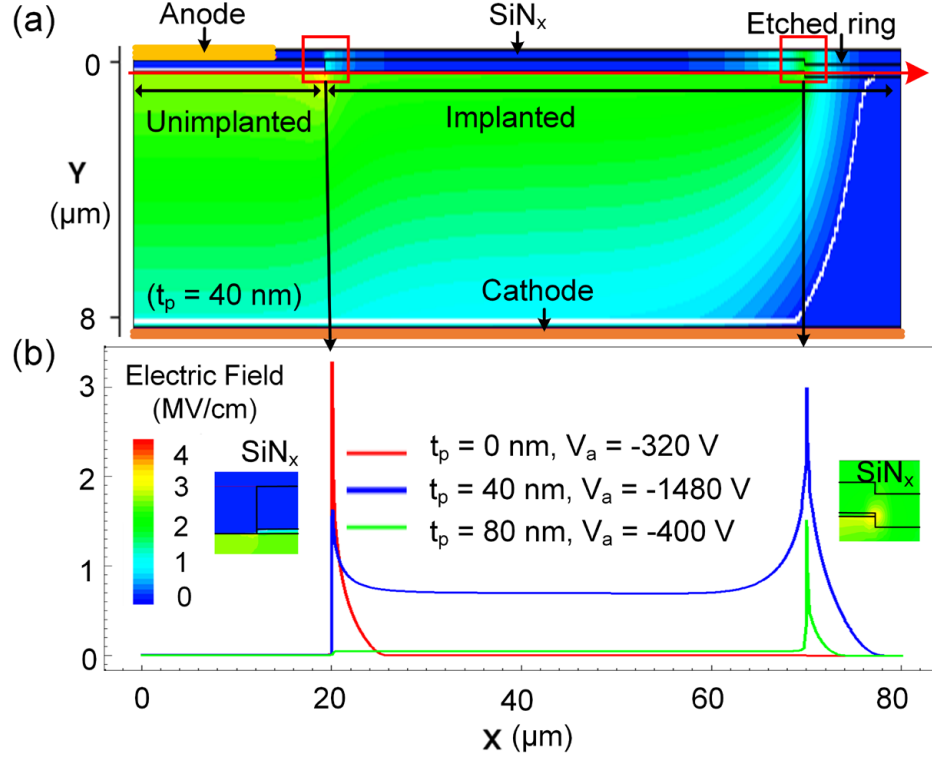


Figure 3.5. (a) Computed electric-field distribution showing where the electric field peaks occur in devices with SiN_x passivation for the optimal case. (b) Electric field profile along the ET (red arrow in (a)) for different t_p . Balanced electric field peaks (blue curve) are obtained when t_p is close to the optimum.

As can be seen from Figure 3.5, the thickness of the partially-compensated layer, t_p , significantly impacts the electric field distribution within the device, and thus the V_{br} . From a series of simulations like that shown in Figure 3.5 with t_p varied, the

breakdown voltage as a function of t_p was obtained and is shown in Figure 3.6; the highest V_{br} achieved (defined in simulation as the bias at which the peak field in the device reaches 3.3 MV/cm) is 1.48 kV for a t_p of 40 nm.

3.3.3 Sputtered SiN_x passivation

The inclusion of a surface passivation layer is well known to be useful for enhancing the breakdown of devices, both due to termination of surface states as well as moderating the permittivity contrast along the device surface. However, it has been observed that the on-state characteristics of n-type GaN Schottky diodes can be compromised if SiN_x or SiO₂ deposited by plasma-enhanced chemical vapor deposition (PECVD) is used;[113] it is speculated that hydrogen present during the deposition process may de-activate the Mg acceptors through the formation of Mg-H complexes.[113] As an alternative, sputtered SiN_x was found not to compromise the forward characteristics while also not increasing the reverse leakage current with respect to the unpassivated n-type Schottky diodes.[114] In this work, sputtered SiN_x was evaluated as the passivation for implant-isolated planar p-n junction diodes (i.e. on a p-type GaN surface as shown in Figure 3.5). A comparison of the current voltage characteristics of diodes without passivation and with either PECVD SiN_x or sputtered SiN_x is shown in Figure 3.6 for devices with an 8 μ m thick drift layer. As shown in Figure 3.6(a), both PECVD and sputtered SiN_x improve the breakdown voltage compared t_p the unpassivated case. However, as shown in Figure 3.6(b), the forward on-resistance is increased for PECVD passivation, while sputtered SiN_x is nearly identical to the unpassivated case.

As discussed in section 3.3.2, when t_p is close the optimum, a “balanced” electric field (e.g. $t_p = 40$ nm in Figure 3.5(b) and Figure 3.7(b)) can be obtained near the partially compensated region. In devices without SiN_x surface passivation, similar trends are seen, except that the absence of the surface passivation leads to enhance-

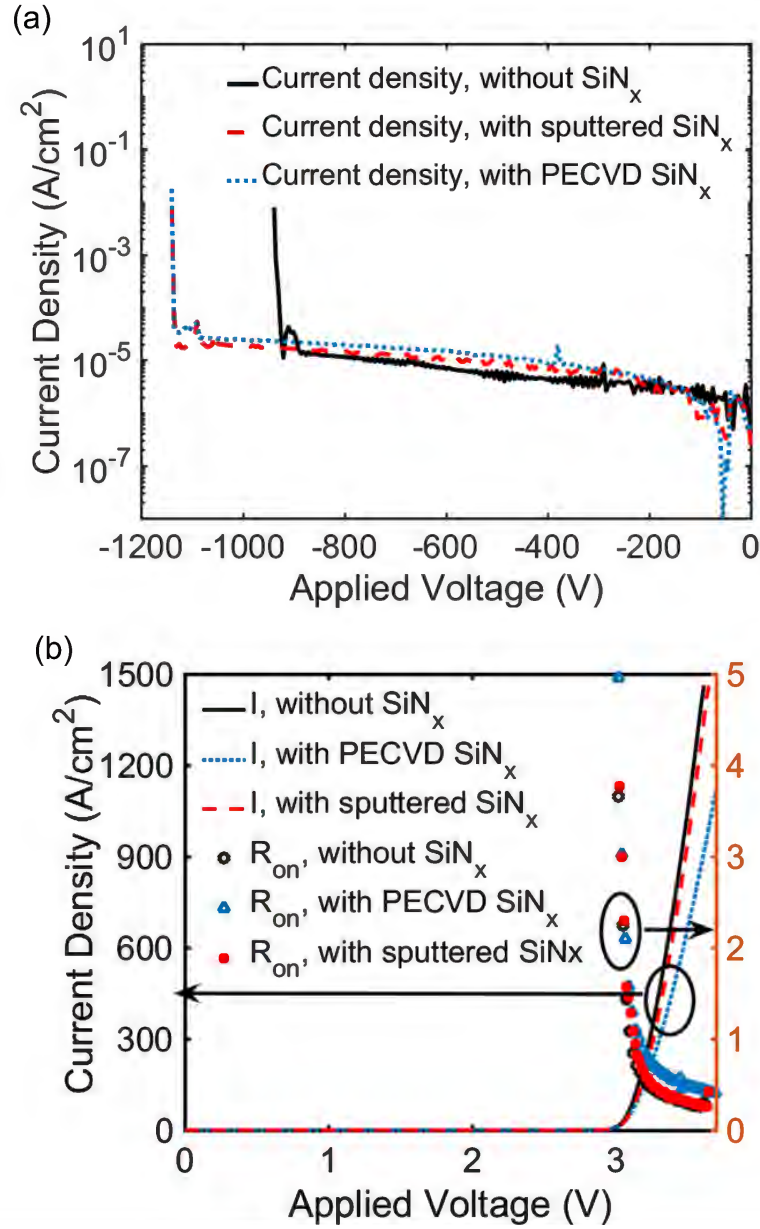


Figure 3.6. Measured I-V characteristics of GaN p-n diodes with 8 μm drift layer (155 μm diameter). (a) Comparison of reverse I-Vs and V_{br} of p-n diodes without passivation, with sputtered SiN_x , and with PECVD SiN_x . Both sputtered SiN_x and PECVD SiN_x increase the V_{br} equally, consistent with a dielectric field distribution model. (b) Comparison of forward I-Vs and R_{on} for p-n diodes without passivation, with sputtered SiN_x , and with PECVD SiN_x . At 3.6 V, R_{on} is 0.25, 0.25 and 0.41 $\text{m}\Omega\cdot\text{cm}^2$ for these diodes, respectively. Compared with PECVD, sputtered SiN_x results in less compromise of the on-state performance.

ment of the peak at the top surface of the etched ET ring, (Figure 3.7(d)) reducing the breakdown voltage. This indicates (as suggested by the simulation results) that the primary mechanism of passivation-related breakdown enhancement in this case is through dielectric field control, rather than surface state modification or other effects.

3.3.4 Device performance and physical interpretation

A critical issue for power devices is device area scalability. To evaluate scalability, devices with diameters from 70 μm up to 1 mm were fabricated and tested. For the devices reported here, the measured breakdown voltages were found to be independent of the size of the diodes, as shown in Figure 3.8(a). The apparent increase in reverse leakage current density for small devices at low bias voltages is an artifact from the measurement noise floor and the current/area normalization. The lack of an area dependence suggests that the device edges are playing an insignificant role in limiting the breakdown voltage. In forward bias as shown in Figure 3.8(b), the devices exhibit near-ideal behavior for current densities spanning 13 orders of magnitude. Below 2 V, the diode current is too low to be measured. For applied voltages from 2 V to approximately 2.5 V, the extracted ideality factor n is 2.1, indicating SRH recombination dominated operation. In this regime, a small area dependence can be seen, suggesting that the diode perimeter contributes modestly to the SRH recombination. Above approximately 2.5 V, the ideality factor shows a transition from 2.1 down to approximately 1.18 at 3 V, signifying the diode diffusion current (with ideality factor of 1) overwhelms the SRH current in this region. A turn-on voltage of 3.1 V (at 100 A/cm²) is measured, as expected given the bandgap of GaN. Above the turn-on voltage, n rises due to the diode series resistance. As can be seen in Figure 3.8(b), the current density scales almost perfectly with junction area (thus yielding identical current densities) in the on-state.

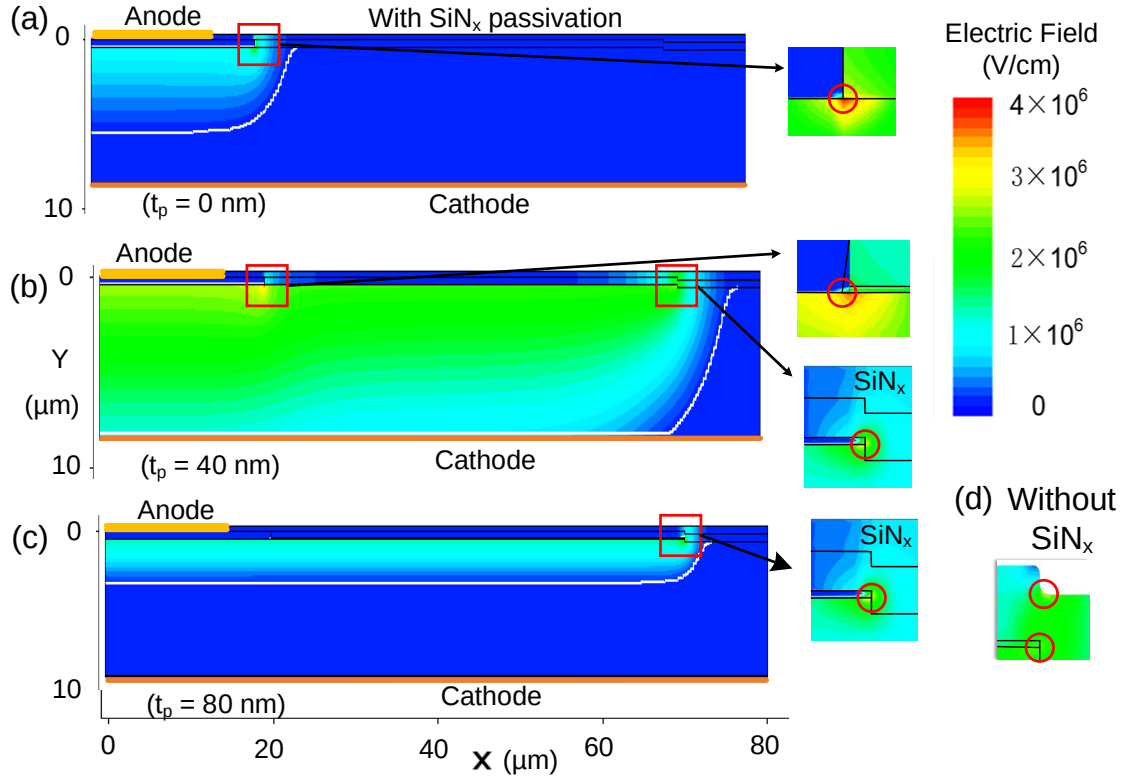


Figure 3.7. Electric-field distribution for vertical p-n diode structures with SiN_x. (a)-(c) shows ET designs for several t_p values. When the thickness of the partially compensated layer is small (a), the electric field peaks at the corner of the p⁺ GaN/ n⁻ GaN drift layer and the edge of the implant. When $t_p = 40$ nm (b), the electric field peaks are spread between the p⁺ /p⁻(partially compensated)/n⁻ GaN corner and the corner of ET/p⁻/n⁻ GaN. When $t_p = 80$ nm, the electric field peaks at the corner of the ET/p⁻/n⁻. The case shown in (b) $t_p = 40$ nm, results in the highest V_{br} . In devices without SiN_x surface passivation, similar trends are seen, except that the absence of the surface passivation leads to enhancement of the peak at the top surface of the etched ET ring as shown in (d).

To evaluate the ultimate current-carrying capability of these structures, pulsed I-V measurements were performed on the larger-sized devices. To limit the effects of self-heating during measurements, 500 μ s pulses and a pulse period of 500 ms was used during the measurement. The sample was also mounted on a thermal probe station chuck with the surface actively held at 25 °C. As shown in Figure 3.8(c), the current in a 1 mm diameter diode can reach 12 A at 4 V. No apparent degradation with additional measurement sweeps was observed. As of this writing, this represents a state of the art result for forward current and reverse blocking voltage.

3.3.5 Comparison of GaN p-n diode performance between simulation and measurement

To help to understand and optimize these GaN p-n diodes, Sentaurus TCAD and SRIM software packages were used to simulate the vertical p-n diode with ion-implanted ET. Due to the radially symmetric structure of the p-n diodes, a 2D simulation of half of the structure of the device could be performed, based on the structure shown in Figure 3.3. Figure 3.9 shows the simulated I-V characteristics. The simulated I-V in forward bias shows a 3.1 V turn on voltage (at 100 A/cm²), in good agreement with experiment. In addition the linear-scaled I-V characteristics show that the effect of series resistance is well captured by the simulations. To explore the design space for the ET, the thickness of the partially compensated p-type GaN p⁻ layer, t_p , was scanned over a range from 0 to 80 nm to optimize the breakdown voltage [8]. As an approximation to the smooth decrease in the damage profile with increasing depth (e.g. Figure 3.4), the doping concentration of the partially compensated p⁻ GaN was set to be constant, at 10 percent of that from the p⁺ layer, following the treatment in [8]. Both the simulated and measured results showed that the thickness of t_p did not affect the forward I-V characteristics. Figure 3.6 showed the SiN_x passivation effect on the electrical performance of diodes. As expected,

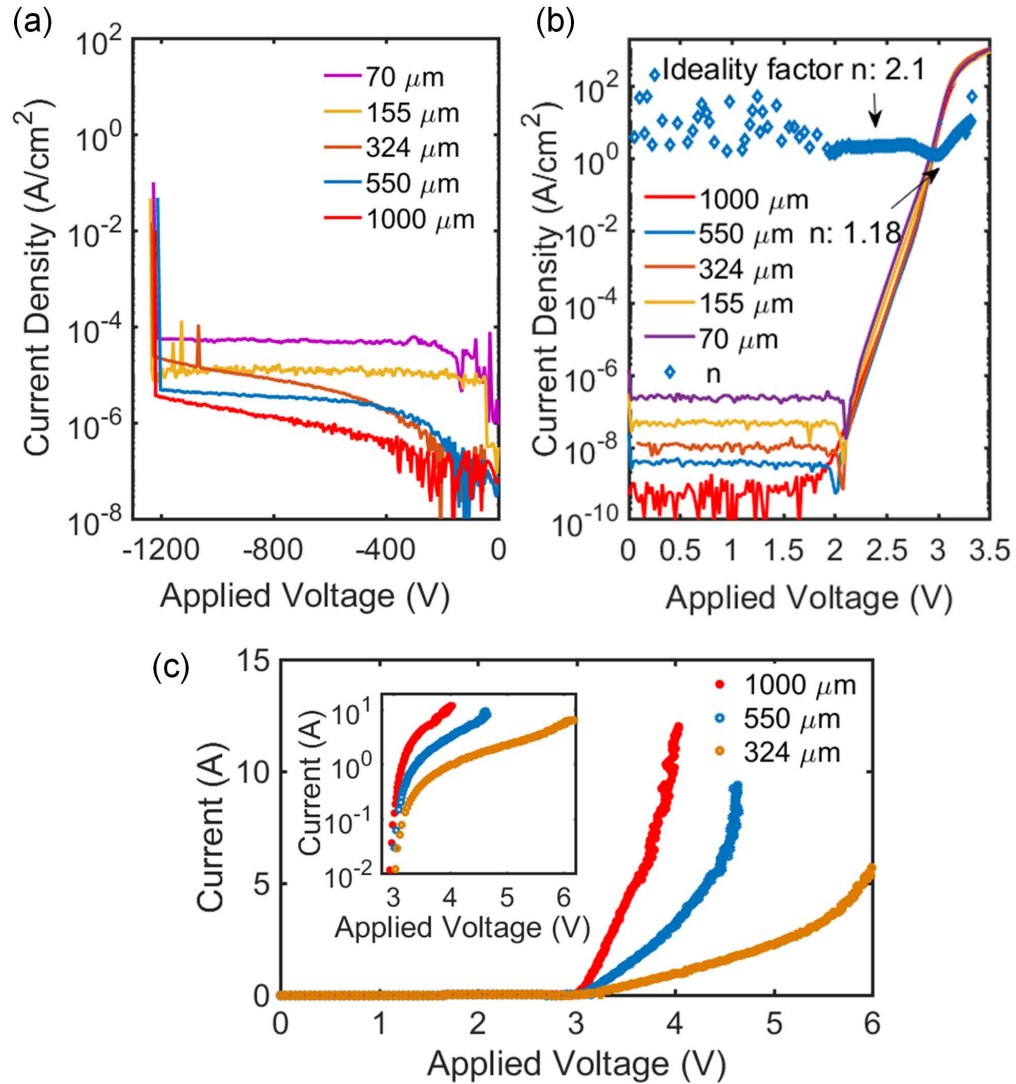


Figure 3.8. Measured I-V characteristics of GaN p-n diodes with 8 μm drift layer as a function of device area. (a) Reverse I-Vs, showing that the breakdown voltage V_{br} is not affected by device area; (b) Forward I-Vs on semi-log scale, showing that device area does not affect the forward current density. The increase in SRH current for small devices suggests a modest edge-related recombination current; (c) Forward-bias pulsed I-V on large diodes. Currents as high as 12 A are carried by 1 mm diameter devices at 4 V.

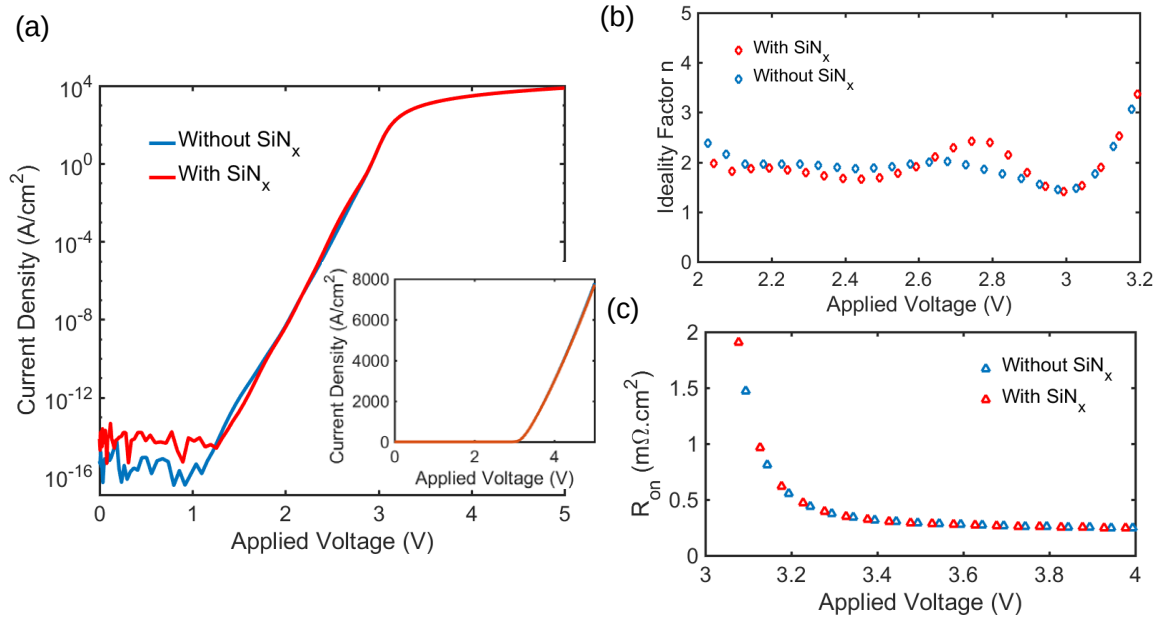


Figure 3.9. Simulated electrical performance of diodes. (a) Forward I-V characteristics, (b) ideality factor, n , and (c) R_{on} of diodes with and without SiN_x passivation. Diodes with and without SiN_x have the same turn on voltage 3.1 V (at 100 A/cm²), R_{on} , and have $n = 2.0$ at low current levels, dropping to $n = 1.4$ at turn on before rising again due to series resistance.

an ideality factor $n \sim 2$ is obtained at low currents, with n dropping (to ~ 1.4) at higher current levels. Small changes in ideality factor (n) were observed with surface passivation; devices with SiN_x passivation have a slightly better n in the low-injection regime due to reduced surface recombination. However, it has a significant impact on the breakdown voltage. The highest V_{br} (defined in simulation as the bias at which the peak field in the device reaches 3.3 MV/cm) is projected to occur for t_p of 40 nm and 30 nm for devices with and without SiN_x, respectively. To confirm these predictions, diodes with different t_p were fabricated and characterized. A comparison of simulated and measured breakdown voltage is shown in Figure 3.10. The highest measured V_{br} occurred for t_p of 40 nm and 30 nm (with and without SiN_x respectively),

in good agreement with the simulation. Experimentally, diodes with sputtered SiN_x passivation and $t_p = 40$ nm exhibited a breakdown voltage of 1220 V, only modestly below the simulation prediction.

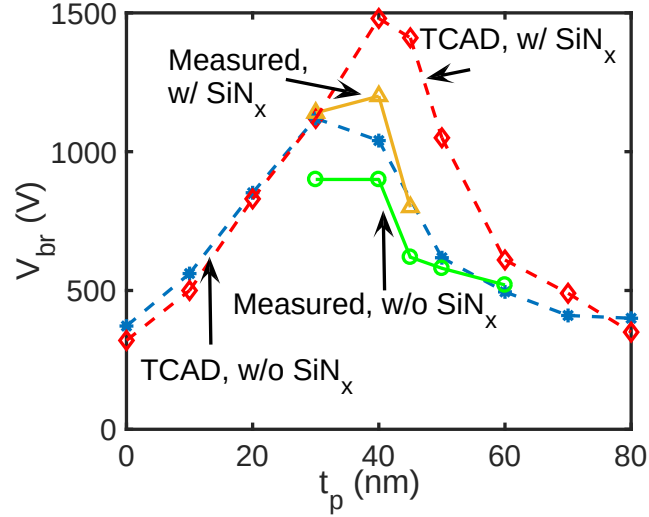


Figure 3.10. V_{br} vs. t_p from simulation and measurement for devices both with and without SiN_x . The highest measured V_{br} occurred at 40 nm and 30 nm with and without passivation, respectively, only slightly offset from the simulation curves.

In addition to the 8 μm drift layer devices shown above, a thicker 12 μm drift layer was also evaluated through simulation and experiment in order to achieve higher breakdown voltages. As shown in Figure 3.11, measurement and simulation for these devices exhibit turn-on voltages of 3.1 V, and the measured R_{on} of $0.15 \text{ m}\Omega\cdot\text{cm}^2$ is within $0.02 \text{ m}\Omega\cdot\text{cm}^2$ of the prediction from simulation. Measured breakdown voltages of 1680 V are obtained, in good agreement with the simulation projected breakdown of 1730 V. These results correspond to a BFOM of $18.8 \text{ GW}/\text{cm}^2$, among the best

GaN diodes reported to date.

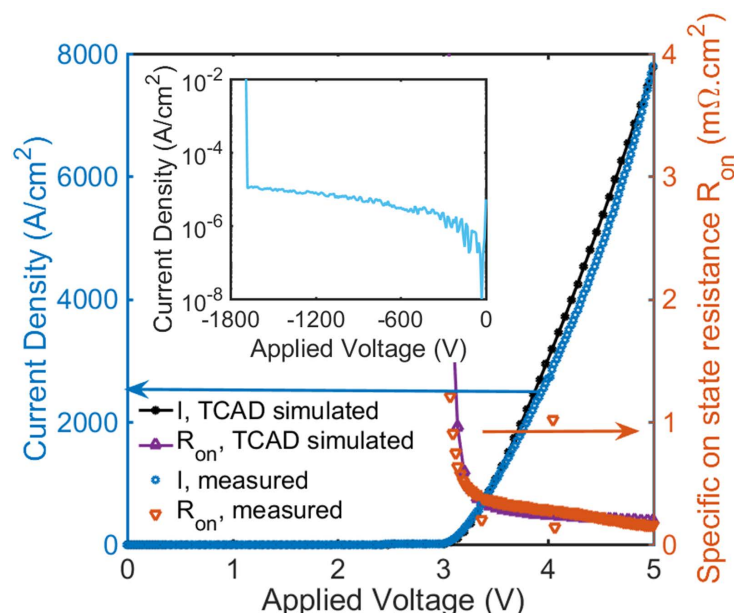


Figure 3.11. I-V performance of measured and simulated GaN pn diodes. ($12\ \mu\text{m}$ drift layer, $155\ \mu\text{m}$ diameter, $t_p = 40\ \text{nm}$) From the measurement, $1680\ \text{V}$ V_{br} and $0.15\ \text{m}\Omega\cdot\text{cm}^2$ R_{on} (at $5\ \text{V}$) are obtained. Both the simulated and measured diodes have the same turn-on voltage of $3.1\ \text{V}$ at $100\ \text{A}/\text{cm}^2$.

3.4 Conclusion

Well behaved vertical p-n diodes with optimized ion-implantation ET, sputtered SiN_x passivation, and etched isolation ring have been demonstrated. A comparison of these results to the state of the art is presented in Figure 3.12. As can be seen, the highest performance devices presented here are close to the fundamental limits for GaN, and compare favorably with the state of art. A high BFOM of $18.8\ \text{GW}/\text{cm}^2$ is obtained for these vertical GaN-on-GaN p-n diodes, and the scalability

of the devices to large areas, high current densities, and large absolute currents is demonstrated. The high performance attained with a single-step ET without field plates offers advantages for cost and yield, as well as reduction in parasitic capacitance for switching applications. With this device design and fabrication process demonstrated, exploration of the performance benefits possible from ELO processing is considered in Chapter 4.

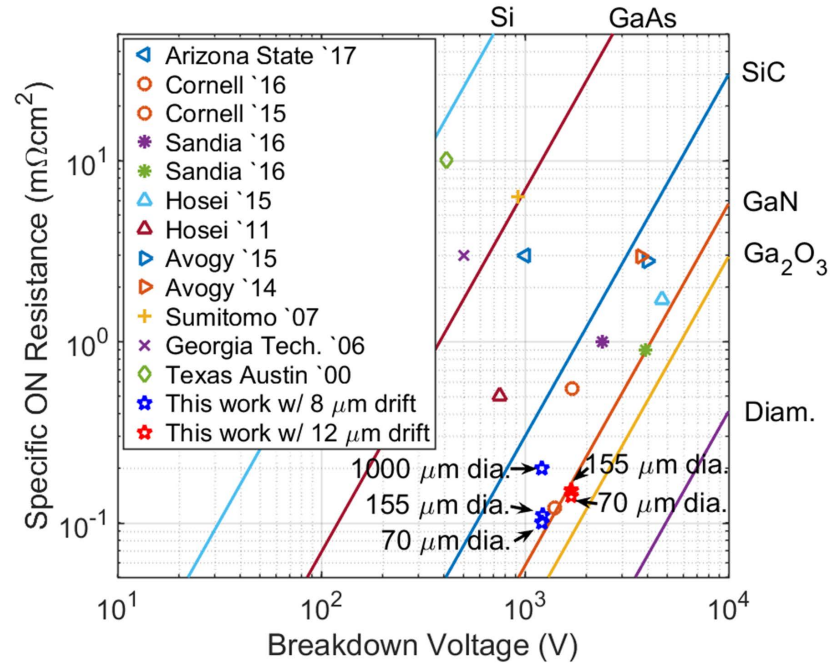


Figure 3.12. Benchmark of R_{on} vs. V_{br} for reported power GaN p-n diodes. The blue stars are the results obtained for diodes in this work with 8 μm drift layers, while red stars indicate devices with 12 μm drift layers. Performance approaching the fundamental limits of GaN (assuming an electron mobility of $1470 \text{ cm}^2/\text{Vs}$ and critical electric field of 3.9 MV/cm [4]) with a simple device and ET design has been achieved.

CHAPTER 4

THE IMPACT OF EPITAXIAL LIFT-OFF ON VERTICAL GAN P-N DIODES FROM BULK GAN SUBSTRATES

4.1 Overview of ELO on GaN p-n diodes

There is a wide range of possible applications for epitaxial lift-off with GaN, including optoelectronics, emerging devices, flexible electronics/optoelectronics for wearables and medical applications. Of more importance for this study, epitaxial lift-off is especially promising for power electronics. The performance of power devices can benefit from the removal of the substrate through ELO processing. For vertical devices, removal of substrate enables the reduced electrical access. In addition, by removing the substrate and mounting the device directly on a heat sink, the thermal resistance can also be reduced. ELO enables re-use of the host substrate and smaller die sizes, improving the device economics. To obtain these benefits, epitaxial lift-off with GaN requires large-area lift-off with high yield, and no compromise in device performance. It is challenging in nitrides because of the lack of highly-selective, fast etches and lattice-matched release layers. Lift-off processing of GaN films has been demonstrated by several techniques. In this work, band gap selective PEC etching techniques was used to build vertical GaN p-n diodes. In this chapter, the prospects and potential impact of ELO processing on p-n diodes on bulk GaN substrates are explored experimentally.

The performance of many GaN-based devices has fallen short of expectations, in part because of the effects of material defects originating from the use of non-native

substrates. However, recent demonstrations of high-performance devices on bulk GaN substrate appear very promising. The use of epitaxial lift-off has the potential to allow cost-effective device production using native GaN substrates by reuse of the (quite costly) substrate. In Chapter 2, thin-film GaN Schottky diodes were fabricated on sapphire substrates, and the impact of ELO processing was evaluated. In Chapter 3, we demonstrated high quality GaN p-n junction diodes on bulk GaN substrates. In this chapter, we take the device design and fabrication processes developed in Chapter 3 and apply them to evaluate the impact of ELO processing on these low-dislocation devices. [105][54]

4.2 Epitaxial lift-off mesa isolated GaN p-n diodes from bulk GaN substrates

To evaluate the impact and benefits of ELO for GaN power diodes, several device designs and process flows were explored. Although mesa-etched devices are known to suffer from increased sidewall-related leakage and reduced breakdown compared to devices with more sophisticated ET designs, they do provide a simple way to evaluate the impact of ELO processing in material quality. Consequently, as a first study, mesa-isolated devices were fabricated and subjected to ELO processing.

4.2.1 Device structure and fabrication process—mesa-isolated devices

The epitaxial layers for mesa-isolated devices were grown on bulk GaN substrates for low threading dislocation density ($\sim 10^6 \text{ cm}^{-2}$) using MOCVD by our collaborators at Qorvo. The layer structure is shown schematically in Figure 4.1 (a). A thin 500 nm n-type drift layer ($N_d = 1 \times 10^{17} \text{ cm}^{-3}$) was used to allow high junction fields to be achieved under modest applied voltages so that any field-sensitive defects could be more easily identified. For this first demonstration of p-n diodes lifted-off from bulk GaN substrates, a simple mesa-isolated device design was used. The process flow consisted of first defining the mesa with photolithography and etching the

mesa by ICP-RIE in BCl_3/Cl_2 to a depth of just over $1\ \mu\text{m}$. Then n-type ohmic contacts (Ti/Al/Ni/Au, 30/100/50/50 nm) were deposited on the exposed n^+ GaN, and annealed at 750°C in N_2 for 1 minute. Device fabrication was completed by depositing Pd/Ni/Au contacts on the mesa surface. The devices were then tested (I-V, temperature dependence, C-V) to establish a pre-ELO processing performance baseline. The ELO process was then performed by our collaborators at MicroLink. The ELO process begins with deposition of a thick metal support layer ($\sim 25\ \mu\text{m}$, mainly copper) applied by electroplating over the entire wafer surface. This metal film was patterned with cross-shaped perforations, followed by a PEC wet etch process using KOH solution to etch vertically through the n^+ GaN epitaxial layers to the release layer. Broadband UV illumination from an unfiltered Hg arc lamp was used to drive this non-selective wet etch process. The function of these cross-shaped perforations is to provide access to the InGaN release layer for the etch chemistry during the subsequent lateral selective wet etching ELO process. The use of perforations (on a 1-2 mm pitch) reduces the time required to lift off large areas and enables the ELO process to be scaled up to arbitrary wafer sizes. After ELO, the lifted-off layers were transferred and bonded to a semi-insulating Si carrier wafer using SU-8 as illustrated schematically in Figure 4.1(b). Epitaxial lift-off of large area samples ($\geq 1/4$ of a 2" wafer) was performed successfully from bulk GaN substrates, as shown in Figure 4.1(d).

4.2.2 Device performance and physical interpretation

So that any effects of ELO processing can be clearly identified, devices were tested both before and after lift-off processing. As shown in Figure 4.2 (a) and (b), functional p-n junctions were achieved (both before and after lift-off). The ideality factor was largely unchanged by the lift-off processing, ranging from 2.1-2.3 for currents below the onset of series resistance roll-over. The turn-on voltage (defined as

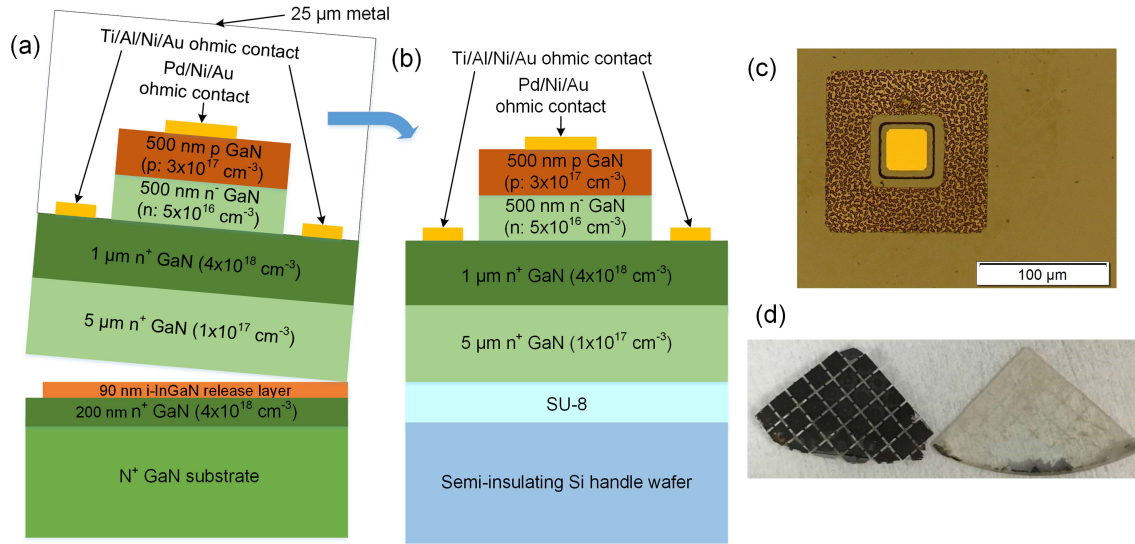


Figure 4.1. Schematic structure of thin-film GaN p-n diodes fabricated on GaN substrates. (a) Schematic structure of as-fabricated p-n diode after deposition of the encapsulating metal support layer. (b) Schematic structure of p-n diode after lift-off processing and remounting on an insulating carrier wafer. (c) Top view of an as-fabricated diode. (d) 1/4 of 2 inch wafer with metal support top layer (left) and substrate (right) after ELO.

the voltage needed to produce a current density of 100 A/cm^2) is 3.08 V before lift off and 3.40 V after lift off.

From the forward biased I-Vs, one can see that additional series resistance and additional low-voltage leakage is present in the devices after ELO processing. The increase in series resistance can be understood by noting that the cathode current is carried by a much thinner layer after ELO, compared to the as-fabricated devices. Figure 4.2 (c) illustrates this schematically. Prior to lift-off, the cathode current can flow through the parallel combination of the n⁺ cathode contact layer, the InGaN release layer, and the full n-type GaN substrate. On the other hand, after lift-off, only the 1 μm highly doped n-GaN lateral contact layer and the 5 μm n-GaN buffer layer remains. This leads to a larger extrinsic series resistance.

In terms of the leakage currents, one can see in Figure 4.2(b) that the reverse current at high voltage is unaffected by ELO; for an example, $J \sim 10^{-3} \text{ A/cm}^2$ at -100 V both before and after ELO. This is leakier than expected for high quality GaN p-n junctions. From an area scaling study of the reverse current vs. area, we observed the devices are perimeter-limited, indicating that the leakage is dominated by the mesa sidewalls rather than the material quality. SEM inspection (not shown) also revealed surface contamination that was more severe after ELO, suggesting residual encapsulation metal may be degrading the surface leakage.

From the inset of Figure 4.2(b), one can see that the ELO process did not change the ideality factor very much, suggesting the material quality was not compromised, but the series resistance and mesa sidewall leakage limited the device performance. These extrinsic factors may be compromising device performance; using backside contacts in a fully vertical configuration (to avoid lateral current spreading), in combination with more effective junction edge termination is a natural approach to eliminate these effects. To verify this idea, devices with back-side contacts and ion implantation isolation were fabricated on the same device structure as the previously described mesa devices. A N triple implant designed to compensate the surface p-type layer with lattice defects was used. The black curves in Figure 4.2 (d) present the measured I-V for a device of this type while red and blue are for mesa-isolated devices before and after ELO respectively. The implant edge termination reduced the leakage by more than 3 orders of magnitude ($1000\times$). In addition, the series resistance was also reduced, and the turn on voltage became approximately 2.9 V. As shown in Figure 4.2 (e), the ideality factor was 2 for small applied voltages (up to 2.75 V) in the SRH recombination current domain, but reduced to 1.2 above the turn on voltage, as expected due to the onset of diffusion and/or radiative recombination in a high-quality diode. This provides concrete evidence for the need to use more sophisticated processes (such as those developed in Chapter 3) for achieving material-limited

performance in GaN diodes.

4.2.3 Impact on carrier concentrations

To confirm that ELO processing does not affect the effective junction doping profiles (e.g., through formation of shallow defect states or added impurities), the capacitance-voltage characteristics of the mesa-isolated diodes were measured. Figure 4.3 shows a typical measured characteristic, as well as a plot of $1/C^2$ vs. depletion depth[7][84]. As shown in Figure 4.3, the doping concentration is essentially the same before and after lift-off, with a drift-layer doping of 4 to $5 \times 10^{16} \text{ cm}^{-3}$, in reasonable agreement with the doping density target by our crystal growth collaborators. As can be seen in Figure 4.3, no significant impact of lift-off and handing processing can be seen.

4.3 Epitaxial lift-off ion-implantation isolated vertical p-n diodes from GaN substrates

To avoid the mesa sidewall related leakage currents and associated complications described above, fully vertical p-n diodes with backside cathode contacts and an ion-implantation-based edge termination with SiN_x surface passivation layer have been investigated using the processes described in Chapter 3. These improved devices were evaluated with and without ELO processing. In addition, further exploration of the benefits of ELO on GaN diodes for power switching applications, including thermal effects, has been performed.

4.3.1 Device structure and fabrication process—implant isolated devices

The device design for the implant-isolated vertical p-n junctions consists of an n^+ GaN buffer, 90 nm pseudomorphic InGaN release layer, and n^+ cathode layer, followed by a 12 μm thick drift layer ($\text{Si}: 1 \times 10^{16} \text{ cm}^{-3}$) and 450 nm/20 nm p^+/p^{++}

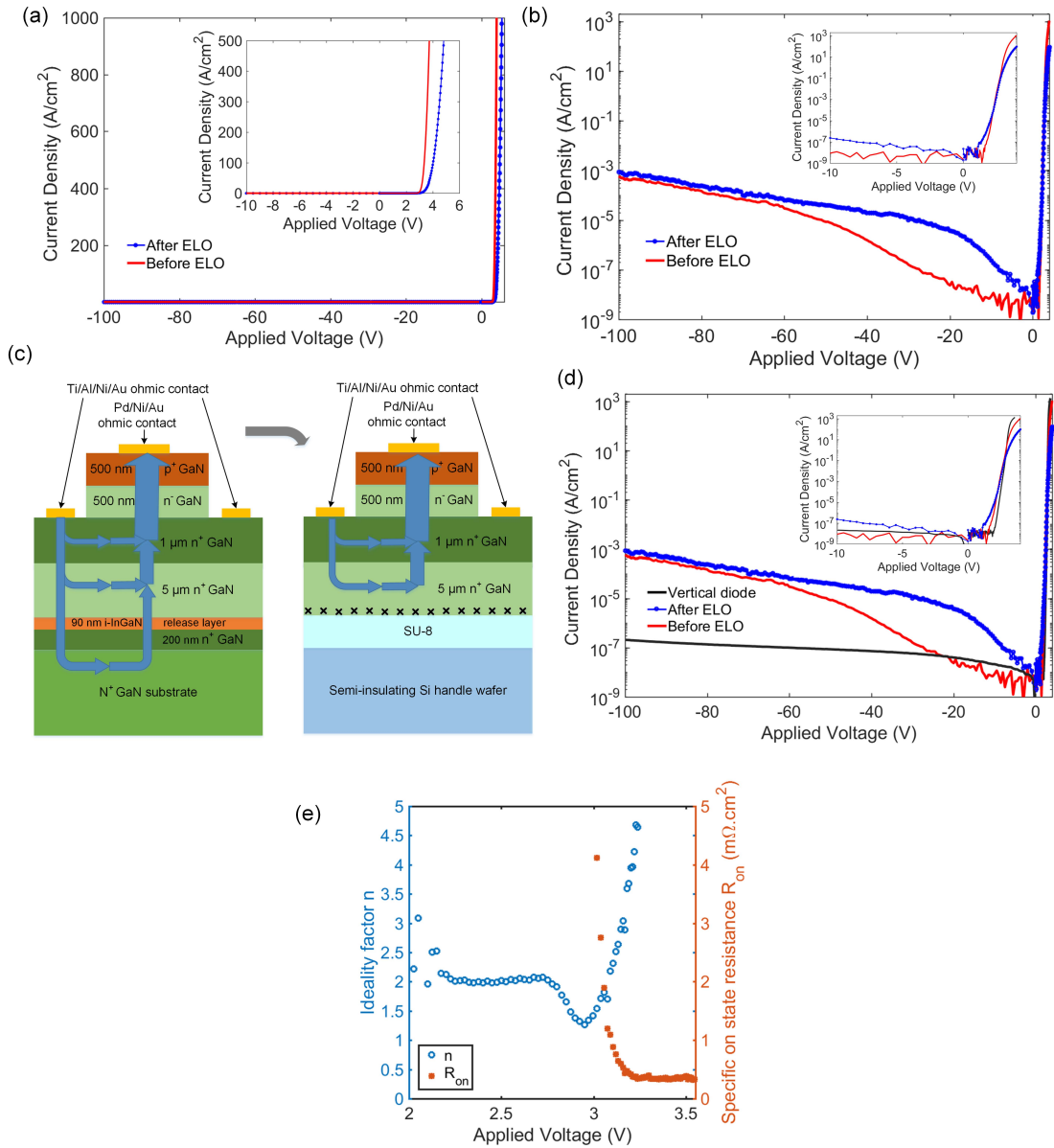


Figure 4.2. Typical device ($40 \times 40 \mu\text{m}^2$) electrical performance before and after ELO. (a) & (b) Measured I-V of as-fabricated and after-ELO p-n diode on a linear scale and a semi-log scale respectively. (c) Schematic structure of the physical interpretation explaining the increased series resistance after ELO. (d) Measured I-V from a recent vertical ion-implantation isolated p-n diode with backside n-GaN contact comparing with the I-Vs of mesa-isolated diodes. (e) Ideality factor and specific on resistance of the vertical p-n diode with implantation based isolation for devices fabricated using the same device structure as the mesa-isolated diodes.

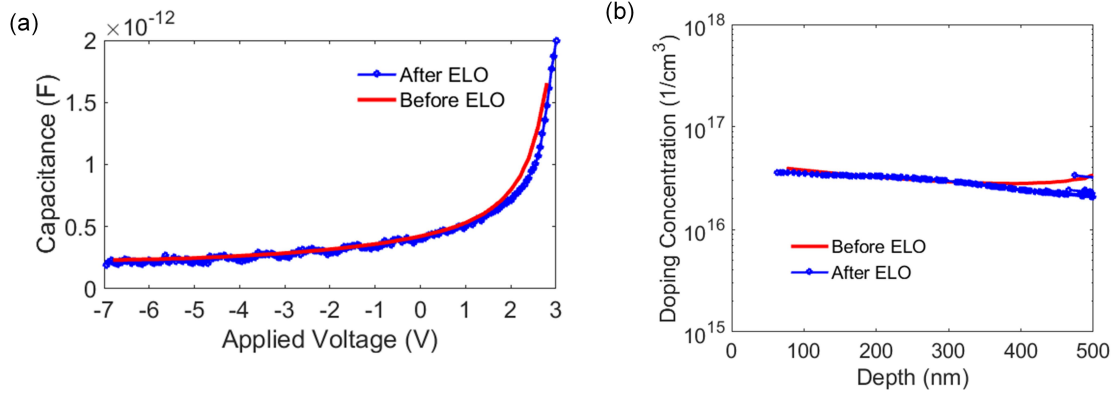


Figure 4.3. Typical measured device capacitance-voltage (C-V) performance before and after ELO. (a) Measured C-V of as-fabricated and after ELO p-n diodes (b) Doping concentrations extracted from measured C-V of p-n diodes.

anode layer grown by MOCVD on a 2 inch n^+ bulk GaN substrate (Figure 4.4(a)). For comparison, a nominally-identical control but without the buried InGaN release layer was also grown. Vertical GaN p-n diodes were fabricated in parallel on both the ELO and control structures. P-GaN ohmic contacts with low resistance were obtained using the two-step surface treatment and thermal annealing of evaporated Ni/Au (20/500 nm) contacts as described in Chapter 3. A 0.5 μm thick Au top layer was used on the anode contacts to reduce probe resistance on large devices. A triple nitrogen implant and a shallow trench etch (Figure 4.4(b)) were designed to create fully-compensated (gray) and partially-compensated (light blue) edge termination regions for device isolation. The top surface of the devices was passivated with sputter-deposited SiN_x . After completion of the top-side device fabrication, a 25 μm thick metal support layer was electroplated on the top surface. The device layers were then lifted off using large-area PEC ELO processing [54]. The PEC ELO process is performed in a KOH solution, with the sample acting as the anode, and a Pt wire as the cathode of the resulting electrochemical cell. A high-power LED-based UV light source shining through the substrate from the back acts to drive the electrochemical

dissolution reaction. The peak irradiance of the UV light is at a photon energy below the bandgap of GaN to ensure that optical absorption occurs primarily in the InGaN release layer. The back side of the ELO devices was then metallized using evaporated Ti/Au (40/100 nm), and the lifted off thin device film was bonded to a metallized Cu carrier using nanosilver paste [115](Figure 4.4(d)). After bonding to the copper carrier, the top support metalization was removed in selective wet chemical etching. For the control sample, a conventional Ti/Al/Ni/Au (30/100/50/50 nm) metallization on the back of the wafer was used.

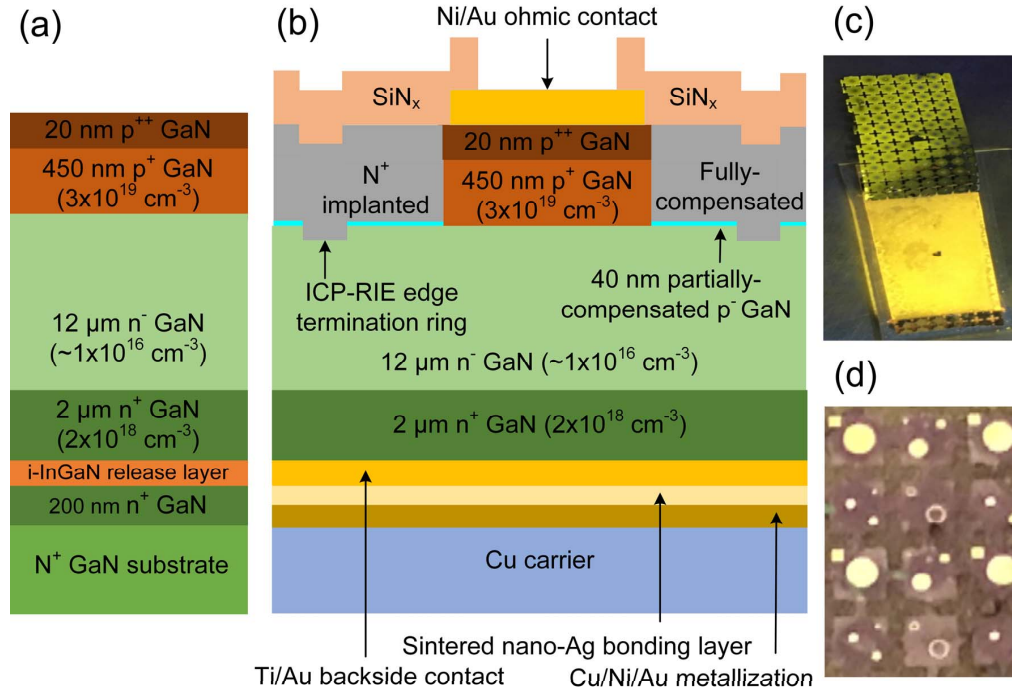


Figure 4.4. (a) Heterostructure of the ELO devices. The control sample has the same epitaxial layers, except the InGaN release layer. (b) Schematic cross-section of p-n diode after lift-off and bonding to the carrier. (c) View of GaN substrate and detached GaN p-n diode film after lift-off under UV illumination. (d) Top view of fully transferred GaN p-n diodes.

4.3.2 ELO p-n diode electrical performance

Figure 4.5 shows measured characteristics of representative control and ELO devices. As can be seen, the devices after ELO have nearly identical electrical performance to those on full-thickness GaN substrates. In the reverse-bias region, when the reverse voltage is smaller than 700 V, the leakage current shown in Figure 4.5(a) is too small to be measured (measurement noise floor). For larger reverse voltage, the reverse current rises gradually, before an abrupt breakdown at approximately 1.3 kV. The ELO p-n diode exhibits a V_{br} of 1.30 kV, within 30 V of the control sample's V_{br} of 1.33 kV. In forward bias, below 2 V, the diode current of both the ELO and control diodes is below the measurement noise floor. For applied voltages from 2 V to approximately 2.5 V, the extracted ideality factor n is approximately 2.0 for both the control and ELO devices, indicating SRH recombination dominated operation. Above approximately 2.5 V, the ideality factor shows a transition from 2 down to approximately 1.54 and 1.48 at 3 V for the ELO and control samples respectively. This indicates that the diode diffusion current (with ideality factor of 1) plays a significant role in this region. A turn-on voltage of 3.1 V (at a current density of 100 A/cm²) is measured for both cases, as expected given the bandgap of GaN. Also, above the turn-on voltage, n rises due to the diode series resistance. A differential R_{on} of 0.50 m Ω ·cm² and 0.20 m Ω ·cm²(at 5 V) was measured for the ELO and control samples respectively. As can be seen in Figure 4.5, the most significant difference between the ELO and control devices is the increased R_{on} of the ELO device. This is attributable to the unoptimized Ti/Au contact to the N-face cathode. The measured capacitance-voltage characteristics are nearly the same for both device structures, as shown in Figure 4.6. This indicates that the ELO process does not have a discernible impact on bulk dopants or impurities, or trap generation. The nearly identical ideality factor, breakdown, forward turn-on performance and capacitance characteristics suggest that ELO of bipolar GaN devices can be achieved without introducing defects

or compromising device electrical performance.

4.3.3 ELO p-n diode thermal performance

A potentially valuable feature of band-gap selective PEC etching ELO processing is that it offers the possibility to maintain fully coherent single-crystal material from the bulk substrate through the device epitaxial layers, while at the same time providing a route to reduce the thermal resistance by removal the device layers from the substrate and mounting the device directly on a heat sink to reduce the thermal resistance. In this work, both pulsed I-Vs[116][117] and optical electroluminescence methods[118] were developed to estimate the thermal resistance of ELO and GaN-on-GaN p-n diodes.

Figure 4.7 show the schematic illustration of the pulsed I-V measurement method used here. To change the device temperature, self-heating at several quiescent bias points (V_{dc}) was used. To allow the diode characteristics to be measured without the measurement impacting the temperature, a pulsed I-V sweep, with 500 μ S pulses and period of 500 mS was used. Figure 4.8 shows the measured pulsed I-V and the extracted thermal resistance of these diodes. To calibrate the measurement, DC swept I-Vs at temperatures from 0 °C-100 °C (Figure 4.8(a)) were measured to obtain the relationship between junction temperature and applied voltage (T-V lines in Figure 4.8(b)). For a specific current density, such as 10, 40 and 100 A/cm², the temperature sensitive voltages (i.e., the bias voltage required to establish the specified current) can extracted for different quiescent biases (Figure 4.8(c)). Using the linear fits to the T-V plots in Figure 4.8(b), the junction temperature for diodes self-heated at different quiescent biases can be obtained. This can then be converted to effective thermal resistance. Figure 4.8(d) shows a comparison of control and ELO devices. The ELO devices exhibit a thermal resistance of 8.5 mK·cm²/W, which is approximately 30% lower than that of the GaN-on-GaN control devices.

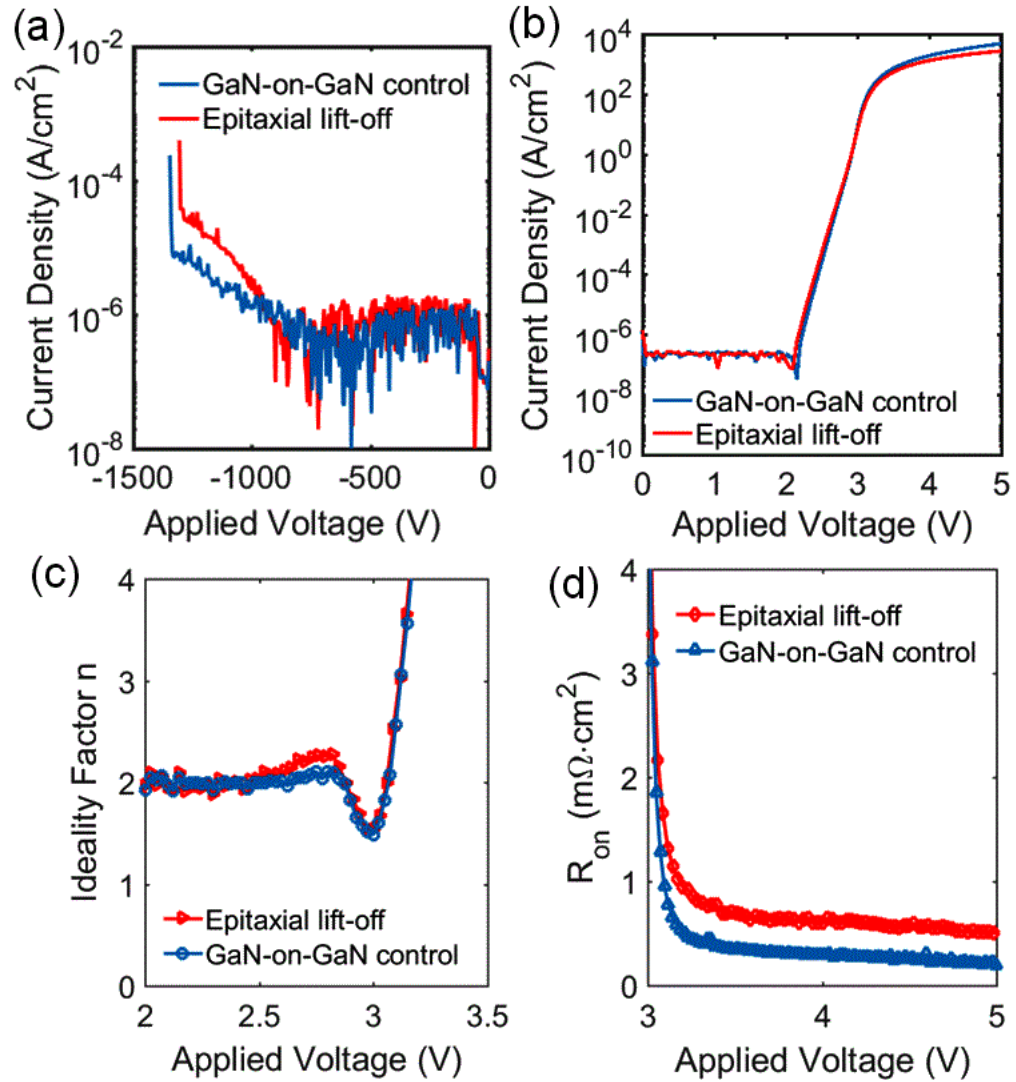


Figure 4.5. (a) & (b) Measured reverse and forward I-V characteristics of ELO and control p-n diodes. (c) & (d) Ideality factor n and differential R_{on} of ELO and control devices.

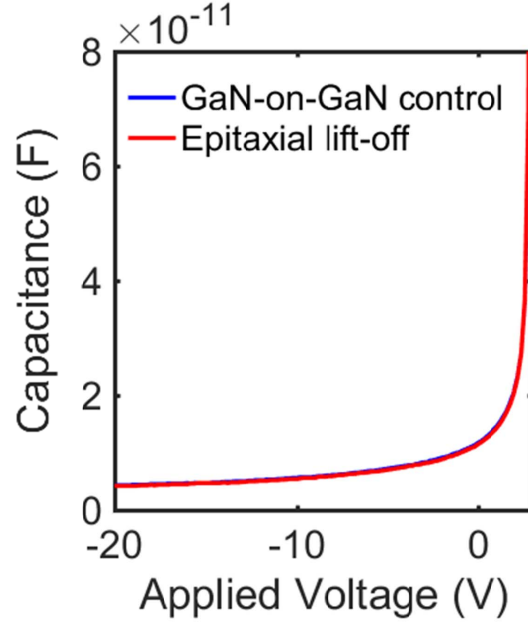


Figure 4.6. C-V performance of ELO and control devices.

Optical electroluminescence measurements were also performed to estimate the thermal resistance. As shown in Figure 4.9, the peak electroluminescence wave length was measured as a function of forward-bias power. In this case, devices with ring-shaped anode contacts were used to improve the light extraction. The junction temperature was then extracted by using the variation of bandgap with temperature.[119] An extracted thermal resistance of $9.4 \text{ mK}\cdot\text{cm}^2/W$ for the ELO devices was obtained, which is also approximately 30% less than that of the GaN-on-GaN control devices. This result is consistent with the observation as estimated by pulsed I-V method.

4.4 GaN p-n diodes on reclaimed substrate

Another key advantage of selective PEC etching with a pseudomorphic InGaN release layer is that it offers the potential to make devices on bulk GaN substrates

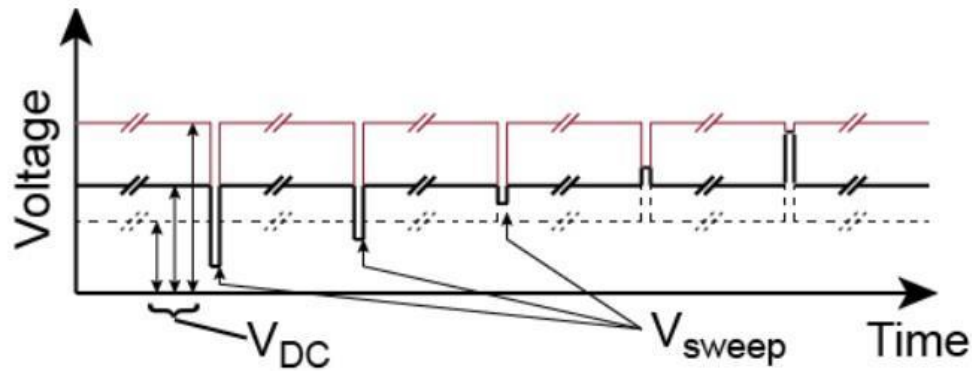


Figure 4.7. Schematic illustration of pulsed I-V characterization approach for assessing thermal performance of pn junctions.

with low dislocation densities, and then to remove the device layers from the host substrate non-destructively. Due to the high cost of bulk GaN substrates, preserving and reusing the substrates is critical to achieve favorable economics. Toward this end, the reuse of bulk GaN substrates after lift-off has recently been demonstrated by fabricating p-n junctions on re-used substrates. The results are shown in Figure 4.10. The fabrication process included ELO from the bulk GaN substrate, repolishing the substrate by our collaborators at Sumitomo Electric (50 μm material was removed during polishing), growth of new epitaxial layers, and p-n diode fabrication and testing. The I-V characteristics of vertical p-n diodes on the re-used substrate were not compromised, demonstrating for the first time an effective method to improve the economics of vertical devices on bulk GaN. This work has been previously reported in [5].

4.5 Conclusion

High performance vertical GaN p-n diodes fabricated using ELO by band gap selective PEC wet etching from bulk GaN substrates and bonded on Cu carrier wafers

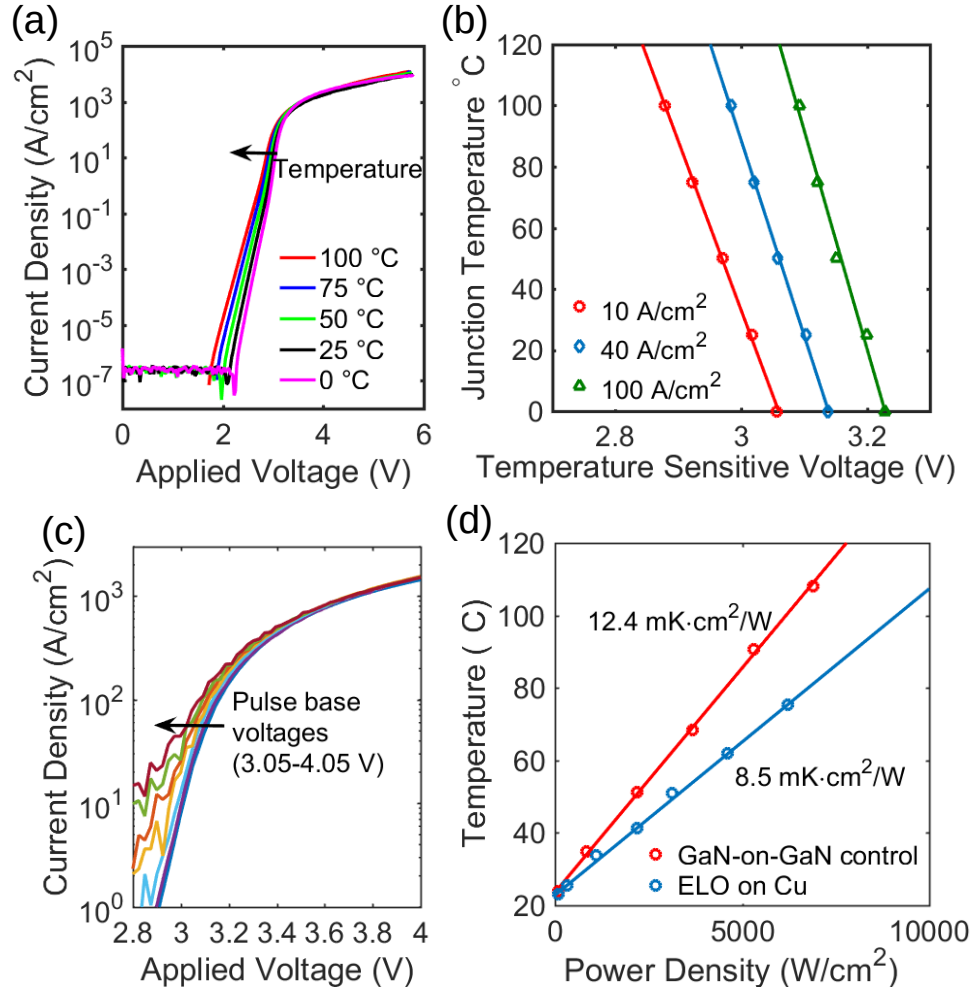


Figure 4.8. (a) DC I-V vs. temperature for the ELO devices. (b) Temperature-voltage characteristics for selected current densities, as extracted from the temperature-dependent I-V. (c) Representative pulsed I-V for ELO device for several pulse base voltages larger than the turn on voltage. (d) Temperature vs. power density lines for ELO and control devices. The thermal resistance is extracted from the slopes of these lines.

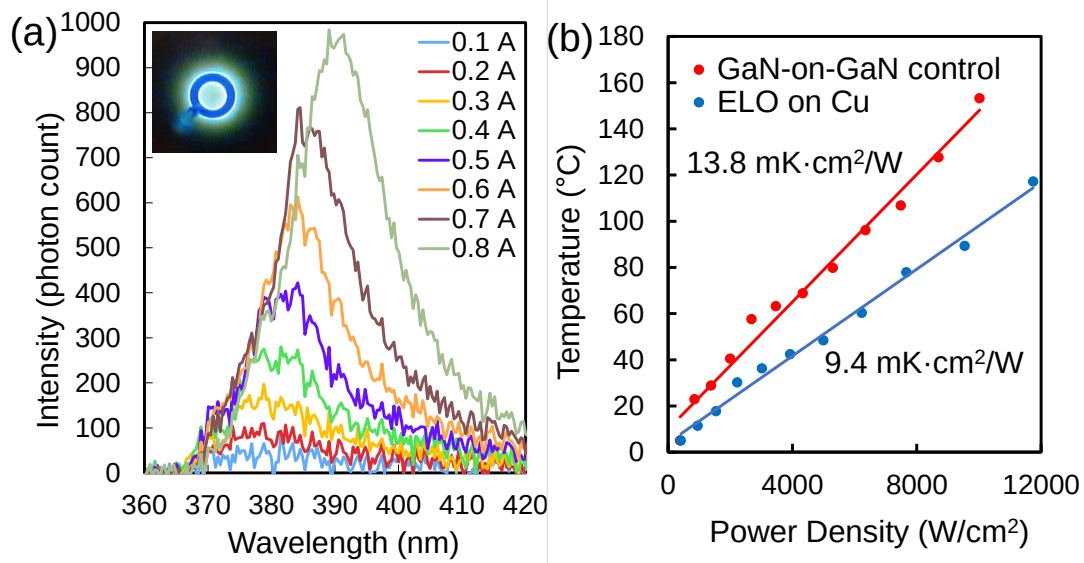


Figure 4.9. (a) Electroluminescence intensity vs. wavelength for a 160 μm ring contact p-n diode with different bias currents; the inset shows a device with light emission. (b) The device temperature extracted from the electroluminescence peaks vs. applied power for control and ELO devices.

were demonstrated. The p-n diodes in the work obtained high V_{br} up to 1.3 kV with low R_{on} of 0.5 $\text{m}\Omega\cdot\text{cm}^2$ R_{on} (giving a Baliga figure of merit of 3.38 GW/cm^2). Compared with the GaN-on-GaN control diodes, the electrical performance was nearly unchanged, while the thermal resistance is improved more than 30%. We find that ELO of bipolar GaN devices can be achieved without introducing defects or compromising device electrical performance, and improved thermal performance is also achieved. Epitaxial lift-off of vertical GaN-on-GaN diodes opens the possibility of GaN-based thin-film optoelectronics, power electronics, and flexible electronics/optoelectronics for wearables and medical applications. Furthermore, a comparison of vertical GaN p-n diodes on reclaimed substrates vs. a prime substrate shows that substrate reuse should be possible to improve the economics of vertical GaN devices.

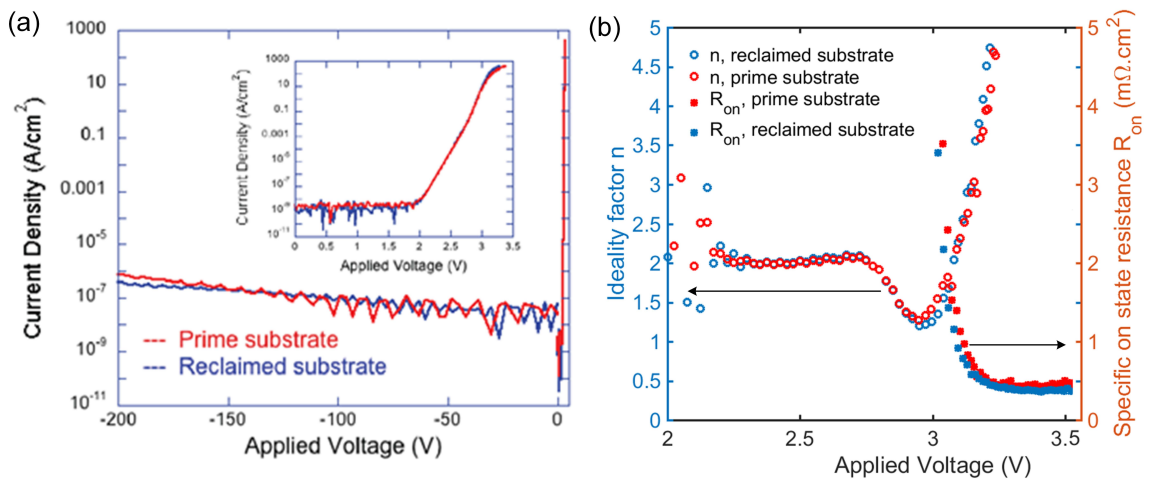


Figure 4.10. Tests of devices fabricated on a re-used/reclaimed substrate.
 (a) Measured current-voltage characteristics of typical GaN vertical p-n junction diodes on prime bulk GaN substrate and on a reclaimed substrate, validating that device performance on epi-ready prime and reclaimed/reused substrates is nearly indistinguishable.[5] (b) Comparison of ideality factor and specific on resistances of diodes on prime GaN substrate and reclaimed substrate.

CHAPTER 5

CONCLUSIONS AND FUTURE WORK

5.1 Summary, overview, and conclusion

As noted earlier, GaN electronics is extremely promising for enabling future generations of efficient power electronics due to the innate material properties of GaN. For this vision to become reality, however, an economically and technically viable path to low-defect-density GaN-on-GaN devices must be found. In this thesis, one promising pathway has been explored, including study of Schottky and pn junctions. As discussed in Chapter 3, the low threading dislocation density possible on native GaN substrates enables high breakdown voltages. However, these substrates are expensive; to mitigate this challenge, epitaxial lift-off with GaN using band gap selective photoelectrochemical etching was evaluated. ELO from non-native substrates was examined in Chapter 2; nearly ideal (ideality factor < 1.1) GaN Schottky diodes were achieved using ELO, demonstrating that the ELO processing need not damage the material quality. Process enhancements to improve p-n diode device performance were studied, including backside n-GaN ohmic contact and ion-implantation ET strategies. Diodes fabricated with this improved process have resulted in breakdown voltages as high as 1680 V, low specific on resistance ($0.15 \text{ m}\Omega\cdot\text{cm}^2$), and near ideal forward current voltage performance ($n \approx 2$ in the SHR recombination domain and $n = 1.2$ in the diffusion current domain), as described in Chapter 3. These device design and process improvements were applied to pn junctions subjected to ELO processing and the ideality factor, turn on voltage, breakdown voltage and C-V

are found to be unchanged by the ELO process. On the other hand, ELO devices exhibit an improved thermal resistance of approximately $8.5 \text{ mK}\cdot\text{cm}^2/\text{W}$, which is approximately 30% less than that for GaN-on-GaN control devices. In addition to these technical benefits, reuse of bulk GaN substrates was demonstrated in Chapter 4. Taken together these results suggest that ELO may provide a path to performance improvement as well as economical deployment of GaN-based power devices.

5.2 Future work

Diodes were used as the main focus of this work because they provide a convenient “window” into the impact and potential benefits of ELO for GaN power electronics. For real systems, however, three-terminal devices such as FETs are needed. While not a focus of the work reported here, vertical GaN MESFETs for high efficiency power switching were also designed and simulated. An initial fabrication run of MESFETs was completed and functional FETs were obtained. However, several opportunities for improvement were identified to improve device performance. Future work will focus on optimizing the fabrication process and performing additional detailed analysis of vertical GaN MESFETs.

5.2.1 Device design and simulation of GaN vertical MESFETs for high-power applications

Lateral GaN JFETs[120][121],(also called a gate injection transistors (GIT))[122] and HEMTs [123][124] have been explored for their use as power devices. However, the performance and reliability of these devices have fallen short of expectations. Challenges for lateral devices such as these include significant dynamic on-state resistance, current-collapse, and the inability to support avalanche breakdown,[125] as well as the need for a large device area that leads to high cost. To address these issues, vertical device structures provide a promising alternative.[126] In a vertical device,

the high-field regions can be internal to the device—away from the surface—eliminating the effects of surface states. In addition, since the field is vertical instead of horizontal, high voltages can be accommodated by making the layers thicker, rather than requiring a large device layout as in lateral devices.[13][127]

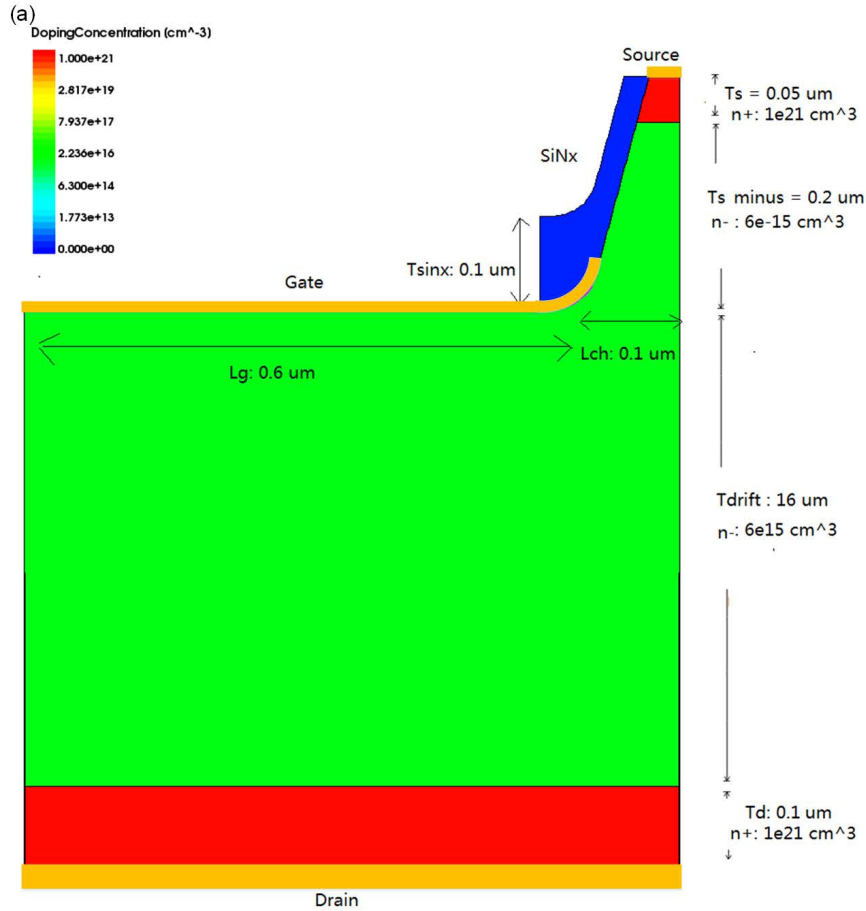
5.2.1.1 Vertical GaN MESFET design and simulation

As a test vehicle to evaluate the prospects for ELO applied to a transistor, a vertical MESFET has been chosen for study. While vertical JFETs should offer the additional benefits of isolating the active region from the surface and allowing enhancement-mode operation to be achieved more easily, JFETs require selective-area p-type doping, which is extremely challenging with GaN; the Schottky contact MESFET allows these complications to be avoided.[126][128] A 2D schematic structure of half of a vertical GaN MESFET is shown in Figure 5.1. This design represents an initial baseline design. Ni/Au Schottky contacts, as discussed in Chapter 2, are used as the gate, and Ti/Al/Ni/Au metallization is assumed for the source and drain ohmic contacts. This GaN MESFET structure in TCAD consists of n-type epitaxial layers. The drift layer is 16 μm in thickness with nominal doping concentration of $6 \times 10^{15} \text{ cm}^{-3}$, grown on an n^+ drain contact layer (shown in Figure 5.1 as the substrate). On the top of this drift layer is an n^+ layer to enable low-resistance source ohmic contacts.

5.2.1.2 Basic physical models and equations

In the numerical simulations used for the design and performance projections of the vertical MESFETs, diffusion and drift current, avalanche breakdown, high-field saturation mobility and lattice temperature effects were included in the TCAD calculations.

For devices intended for high voltage applications, a fundamental limit is imposed



(b)

Symbo	Definition	Value
T_s	source n+ thickness	0.05 μm
T_{drift}	drift layer thickness	16 μm
$T_{s\ minus}$	channel length	0.2 μm
L_{ch}	half-width of channel	0.1 μm
L_g	width of gate contact	0.6 μm
L	width of half VMESFET	0.7 μm
N_{n+}	n+ source and drain contact doping	$1 \times 10^{21} / \text{cm}^3$
N_d	drift layer doping	$6 \times 10^{15} / \text{cm}^3$
T_{SiNx}	thickness of SiNx passivation	0.1 μm

Figure 5.1. Structure of the vertical MESFET evaluated here. (a) Cross-section of the baseline MESFET structure simulated in TCAD. (b) Dimensions and doping parameters for the baseline MESFET design. Half of the device is shown (as simulated in TCAD); the device is symmetric about the right-hand edge of the figure.

by the onset of avalanche breakdown. In a MESFET with uniform drift layer doping as shown in Figure 5.1, the peak electric field occurs at the Schottky contact. Thus the breakdown voltage V_b can be estimated using

$$V_b = \frac{\epsilon_s E_c^2}{2q} \frac{1}{N_d} \quad (5.1)$$

where ϵ_s is the permittivity of GaN, N_d is the doping in n-type drift layer, E_c is the critical electric field and q is the electron charge. Figure 5.2 shows the computed electric field distribution in the device. The peak of the electric field occurs at the gate/drift layer Schottky junction, as expected. In practice, the source “fin” will be fabricated using inductively coupled plasma reactive ion etching (ICP-RIE) to expose the n⁻ layer for the gate Schottky contact. Typical GaN ICP-RIE processes result in angled sidewalls. In TCAD, the sidewall of the source region was designed with a slope angle of 15 degrees to approximate the actual structure expected after ICP-RIE.

To design an enhancement-mode (normally-off) or depletion-mode (normally-on) MESFET, the threshold voltage can be estimated using the built-in potential ψ_{bi} and the pinch-off potential ψ_p . [70],

$$V_{th} = \psi_{bi} - \psi_p, \quad (5.2)$$

where ψ_{bi} is determined from the Schottky barrier height ϕ_B and doping using $\psi_{bi} = \phi_B - kT \ln \left(\frac{N_c}{N_d} \right)$, and $\psi_p = \frac{qN_d L^2}{2\epsilon_s}$ (k is the Boltzmann constant, L is the channel length, and N_c is effective density of states in the conduction band of GaN). For the Ni/Au Schottky contact used in this work, the Schottky barrier height ϕ_B is 1.0 V as reported in [49]. Enhancement-mode devices are preferred as switching devices for the convenience of circuit applications, although depletion-mode MESFETs can often supply higher drain current, I_d .

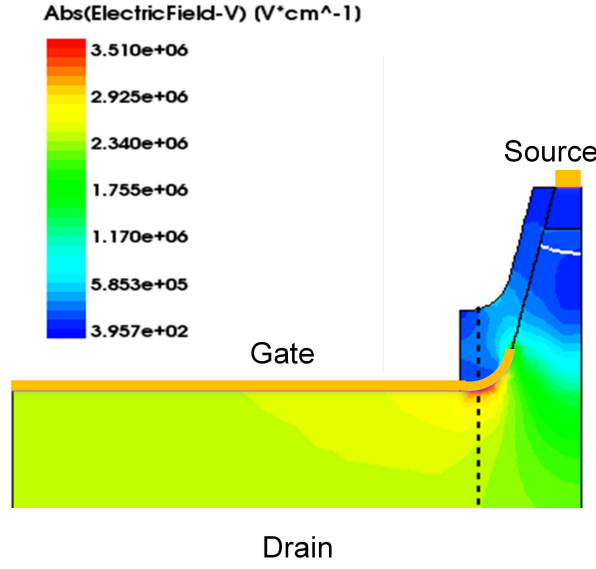


Figure 5.2. Electric field distribution in the vertical MESFET, as simulated with Sentaurus TCAD.

For MESFETs, drain current is dependent on the doping of the drift layer and the dimensions of the channel. Considering an equation for a conventional lateral structure: [129]

$$I_D = \frac{zq\mu N_d W_{ch}}{L} \left\{ V_D - \frac{2}{3\sqrt{\psi_p}} [(\psi_{bi} + V_D - V_G)^{\frac{3}{2}} - (\psi_{bi} - V_G)^{\frac{3}{2}}] \right\}, \quad (5.3)$$

where L is the channel length, W_{ch} is the channel width, z is the thickness of the 2D structure in the direction which is perpendicular to the XY plane, and μ is the electron mobility of GaN (a constant mobility $v = \mu E$ is assumed for this simplified analysis). Equation 5.3 indicates that increasing N_d , W_{ch} , and/or decreasing L can increase the drain current.

To map the structure in Figure 5.1 to the terms in Eq. 5.3, we note that L_{ch} in the vertical structure is half of the channel width W_{ch} in Eq. 5.3; the sum of $T_{s,minus}$ and T_{drift} (the distance from the source to the drain vertically) is the channel length

of L in Eq. 5.3; and N_d is the channel doping (the doping of the drift layer) for both cases. Other parameters in the vertical structure, for example L_g and T_d , have relatively minor effects on the simulation results.

For vertical MESFETs, the simulated results indicate that the thickness of the drift layer T_{drift} (in Figure 5.1) is another critical parameter which needs to be optimized for a vertical MESFET design that is not captured by the simple model in Eq. 5.3. A large thickness is desirable to increase the breakdown voltage, but this leads to increase the on-state resistance. The thickness is also coupled to the threshold voltage, and because of the non-ideal gate control electrostatics in this geometry, this can lead to significant shifts in V_{th} with drain voltage (sometimes called drain induced barrier lowering, DIBL). In the design process, the thickness and the doping concentration of the drift layer need to be optimized to tune the breakdown voltage V_{br} , the threshold voltage V_{th} and the drain current I_d .

5.2.1.3 Effect of electric-field dependent mobility

Although the model in Eq. 5.3 is valuable, it omits some important considerations that are critical for power devices. In order to achieve application-relevant currents, multiple source fingers are needed (e.g., the Advanced Research Projects Agency-Energy (ARPA-E) program supporting this work had a device target of 100 A on-current with 1500 V breakdown). Consequently, we have expanded the simulation domain to include multiple gate and source fingers, and have also incorporated electric-field dependent mobility, saturation velocity, and self-heating effects in the simulations. This allows for a more realistic estimate of on-current densities, and thus a more accurate estimate of the device area required to support a specific drain current target. For the simulations reported here, the electron mobility was modeled

using

$$\mu(T, N) = \mu_{min} \left(\frac{T}{300} \right)^{\beta_1} + \frac{(\mu_{max} - \mu_{min}) \left(\frac{T}{300} \right)^{\beta_2}}{1 + \left[\frac{N}{N_{ref} \left(\frac{T}{300} \right)^{\beta_3}} \right]^{\alpha (T/300)^{\beta_4}}}. \quad (5.4)$$

where T is the temperature, and $\mu_{max}, \mu_{min}, \beta_1, \beta_2, \beta_3, \beta_4$, and α are parameters extracted from, and calibrated against, experimental reports.[130][131][132]

5.2.1.4 Current-voltage characteristics and device optimization

Figure 5.3 shows the simulated I-V characteristics of the baseline vertical GaN MESFET design. The threshold voltage is about 1 V; for $V_{GS} > 1.3$ V, the gate starts to conduct, due to the Schottky gate contact. At $V_{GS} = 1.3$ V, the knee voltage in the common-source output curves is approximately 3 V (though the poor output saturation makes it difficult to determine the knee voltage unambiguously). The specific on resistance is $1.8 \text{ m}\Omega \cdot \text{cm}^{-2}$, while the breakdown voltage is approximately 800 V.

Some of the critical parameters of the MESFETs have been explored through simulations; examples of the observed dependencies are shown in Figure 5.4. The channel width is a significant parameter for device performance; as shown in Figure 5.4(a) and (b), a channel width of 300 nm can support a high drain current density I_d while still providing a breakdown voltage as high as 600 V. Although a device with a 200 nm channel width can support a higher breakdown voltage, the on state resistance is larger than that for a 300 nm channel width device, and it is much harder to fabricate such an aggressively scaled device (i.e. lithography and alignment are especially difficult due to the 15 degree side wall of the channel after ICP-RIE). As shown in Figure 5.4(c), I_d decreases as the thickness of the drift layer is increased. On the other hand, the breakdown voltage increases with the thickness of the drift layer until the drift layer is larger than the maximum depletion width (13 μm for

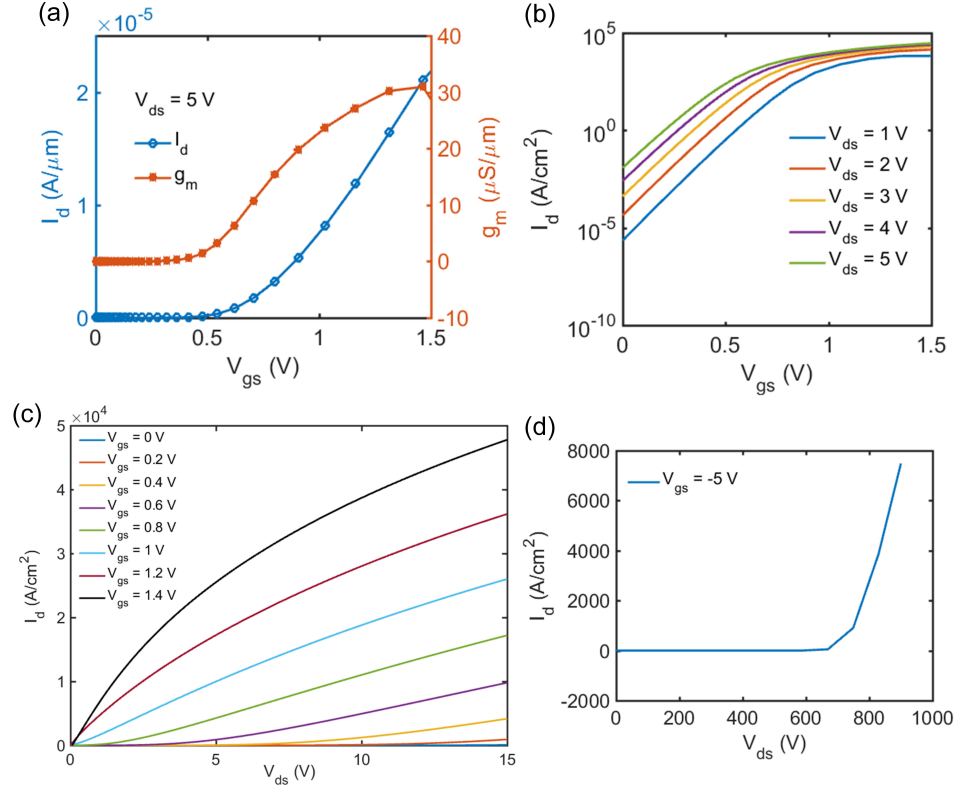


Figure 5.3. Simulated I-V performance of the GaN MESFET. (a) $I_D - V_{GS}$ characteristics and transconductance g_m on a linear scale, (b) $I_D - V_{GS}$ transfer characteristics on a semi-log scale, (c) $I_D - V_{DS}$ characteristics at V_{DS} from 0 V to 15 V, and (d) breakdown characteristics.

the doping level used here) as illustrated in Figure 5.4(d). As can be seen, in Figure 5.4(e) and (f), both the channel length and the doping of the drift layer, N_d , can affect I_d significantly. As shown in Figure 5.4(e) and (f), I_d increases as the channel length is decreased or as the doping of the drift layer N_d increases. As expected, this results in the traditional trade-off between low on-resistance (high N_d) and high breakdown voltage (low N_d). In addition, however, the channel length is also limited by the ability to fabricate suitable source fins, while the lower limit on drift layer doping is set by MOCVD growth kinetics. All of these effects must be considered during the device design and optimization in order to realize a functional device with

desirable performance.

5.2.2 Fabrication process design for vertical GaN MESFETs

Based on these simulations, a preliminary device fabrication run of vertical GaN MESFETs was performed, as shown in Figure 5.5 (a) and (b). The fabrication process flow is shown in Figure 5.5 (c). Ni/Au Schottky contacts have been used for the gate, and Ti/Al/Ni/Au ohmic contacts were used for both the source and drain, just as for the Schottky diodes in Chapter 2. To facilitate the small source finger contacts, a self-aligned electron-beam lithography process was used. With the GaN ICP-RIE recipe used here, a sidewall slope of approximately 15° was obtained.

5.2.2.1 Self-aligned source process

As discussed above, the channel width of the MESFET has a significant effect on the device electrical performance. One critical issue for vertical FETs is to fabricate channels with small width, so that the threshold voltage is positive. For this initial study, we did the source metalization before GaN ICP-RIE and included an extra top metal layer of Ni to serve as an etch mask for the channel definition dry etch process. This both reduces the number of fabrication steps, as well as avoids mis-alignment of the source contact to the source/channel fin. The self-aligned source process provides accurate and controllable source definition. Lithography for the gate was then aligned to the source metal, resulting in the structures as shown in Figure 5.6.

5.2.2.2 MESFET I-V characteristics

The current-voltage characteristics of the fabricated vertical GaN MESFETs were measured. Figure 5.7 shows a comparison of the measured I-V performance for a typical MESFET (with 350 nm channel width) and a TCAD simulation. As shown in Figure 5.7(a) and (b), the drain current I_d increases with both gate voltage V_{gs} and

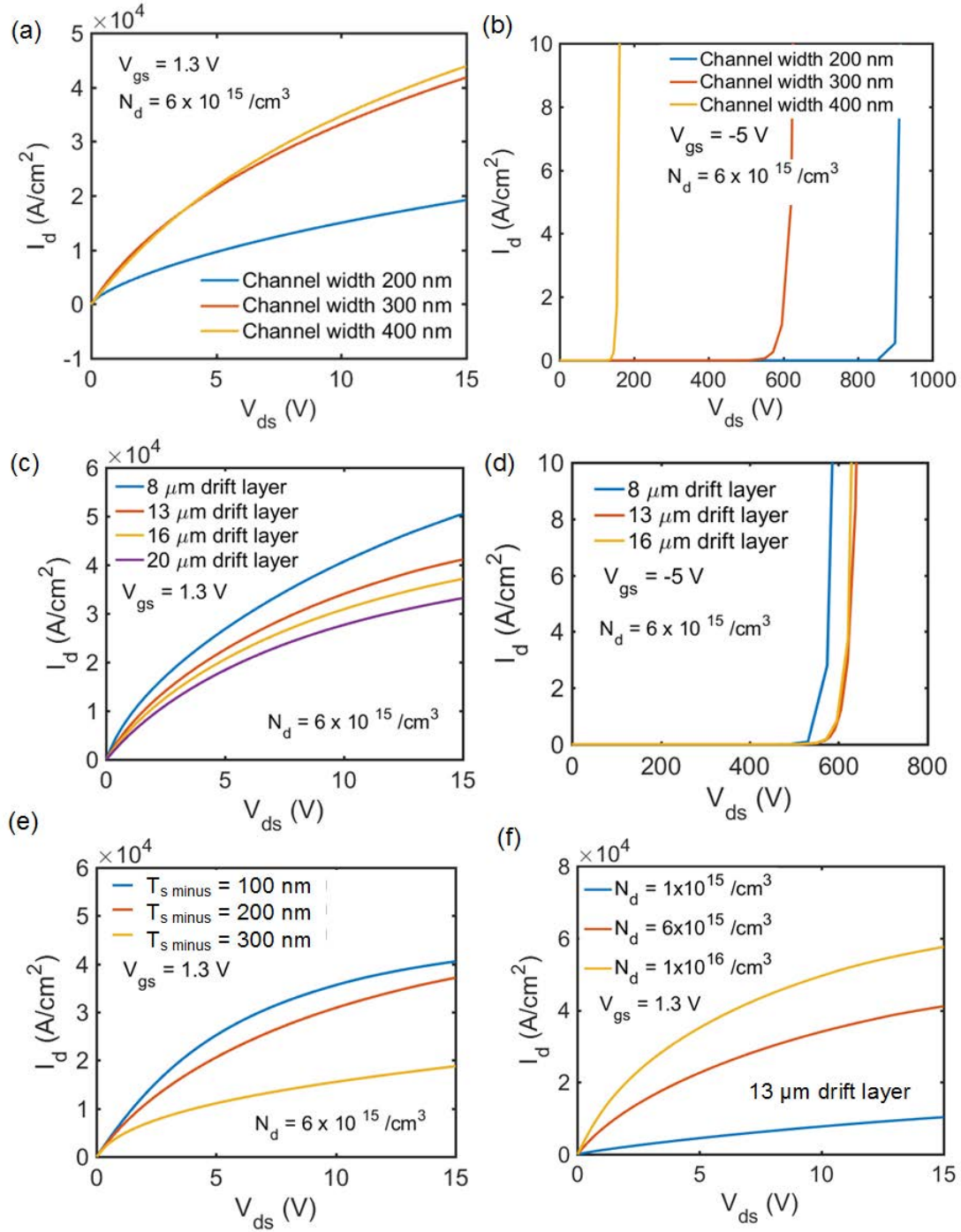


Figure 5.4. GaN MESFET performance as a function of key design variables. (a) Impact of the channel width on the output characteristics; (b) dependence of breakdown voltage on channel width; (c) influence of the drift layer thickness on the output characteristics; (d) drift layer thickness dependence of the breakdown characteristics; (e) impact of the channel length and thickness on the output characteristics; (f) dependence of the output characteristics on drift layer doping.

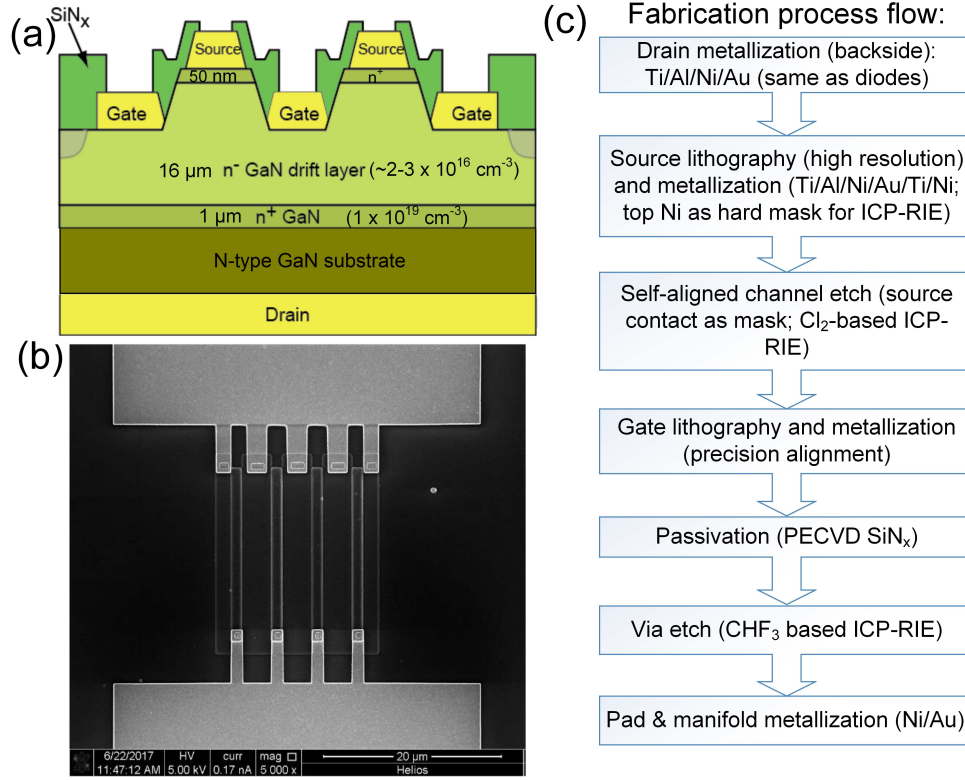


Figure 5.5. Vertical GaN MESFETs. (a) Schematic structure of GaN MESFET, (b) Top view of a typical GaN MESFET after fabrication, (c) Fabrication process flow for the vertical GaN MESFETs.

V_{ds} , showing basic FET operation. The measured knee voltage on the $I_d - V_{ds}$ curve at $V_{gs} = 1$ V is about 3.5 V, in good agreement with simulation. However, the current densities do not align as well as expected. Through the $I_d - V_{gs}$ curve shown in Figure 5.7(c), we see the threshold voltage V_t for the measured MESFET is approximately -3 V, and thus a depletion mode FET. At $V_{ds} = 5$ V, the transconductance g_m ($g_m = \frac{dI_{d,sat}}{dV_{gs}}$) has its maximum value 7 $\mu\text{S}/\mu\text{m}$ at 0 V. For comparison, the TCAD simulations in Figure 5.7(d) show an enhancement-mode MESFET ($V_t = +0.5$ V) with a maximum g_m value of 25 $\mu\text{S}/\mu\text{m}$ at V_{gs} 1.3 V. In the semi-log $I_d - V_{GS}$ plots shown in Figure 5.7(e) and (f), we see the shifts of V_t with drain voltages. DIBL is extracted[133] to be 150 mV/V from the measurement, which is bigger than the

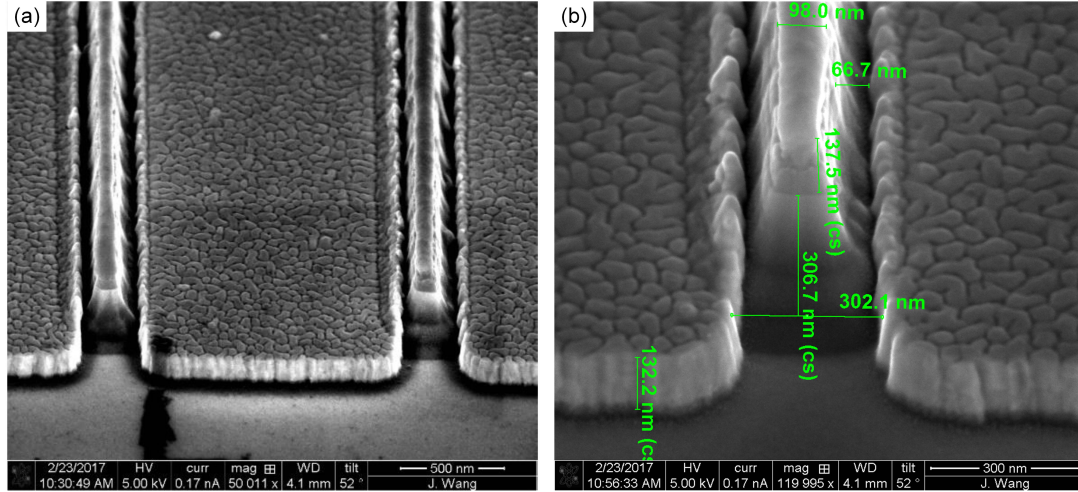


Figure 5.6. SEM images of fabricated MESFETs after the self-aligned source process and gate metallization.

TCAD simulation of 75 mV/V. These results indicate that while the devices show basic functionality, they do not have the degree of gate electrode control expected. This could be due to doping or thickness deviations from the intended design, or fabrication nonidealities. Additional analysis of the epitaxial material (e.g. SIMS profiling, etc.) is needed to clarify these effects. Further breakdown measurement and device performance study is also needed to fully characterize and analyze these devices.

5.2.3 Further efforts—MESFETs

As noted above, an initial effort towards developing an ELO-compatible transistor was initiated. While basic device operation was achieved, there are a number of areas for potential follow-on work.

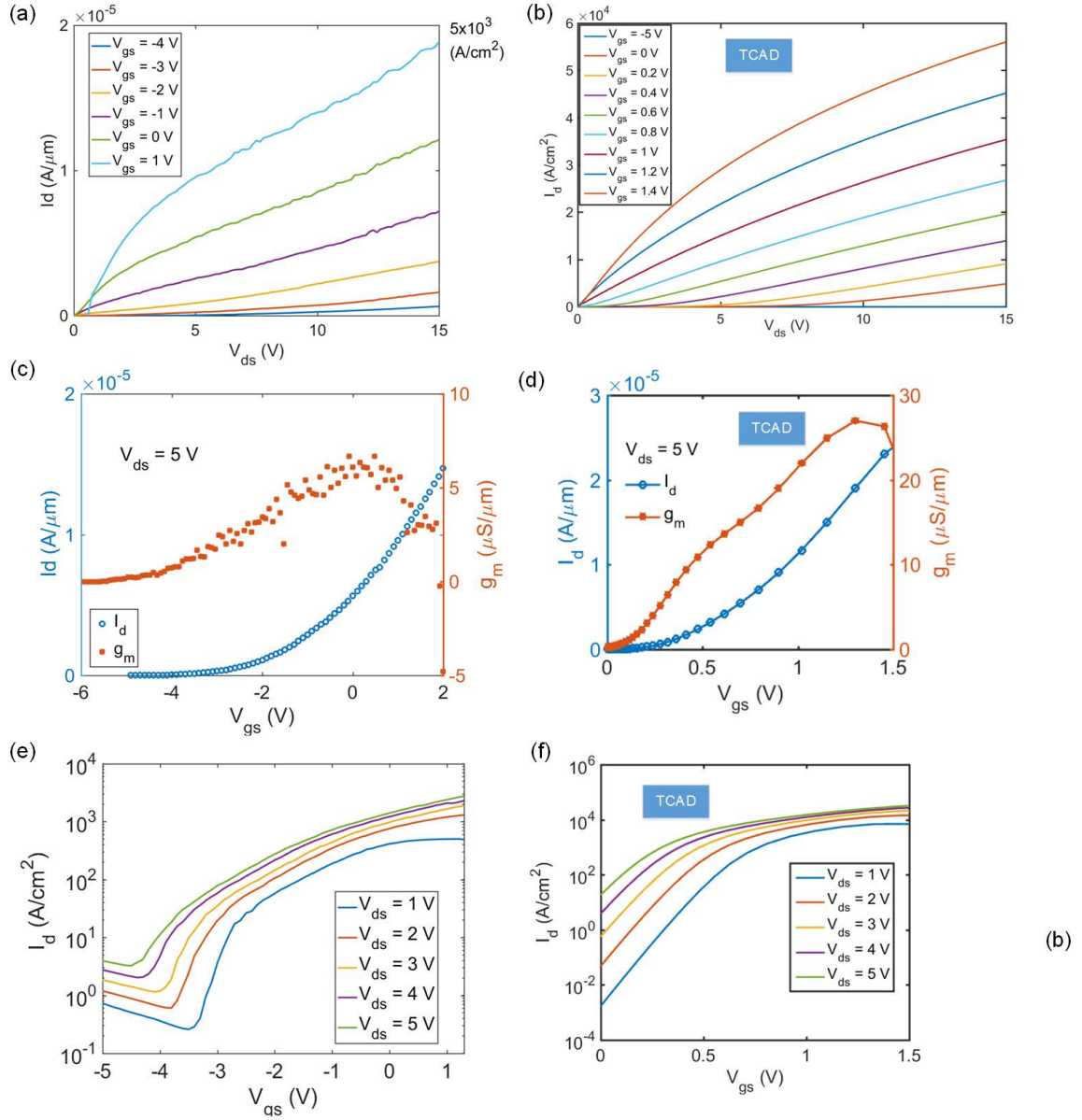


Figure 5.7. Comparison between I-V characteristics for MESFETs from measurement and TCAD simulation. (a) Measured $I_d - V_{ds}$ family of curves, and (b) simulated $I_d - V_{ds}$ family of curves. (c) Measured $I_d - V_{gs}$ and g_m , and (d) simulated $I_d - V_{gs}$ and g_m for $V_{ds} = 5$ V. (e) Measured $I_d - V_{gs}$ and (f) simulated $I_d - V_{gs}$ for V_{ds} from 1 V to 5 V.

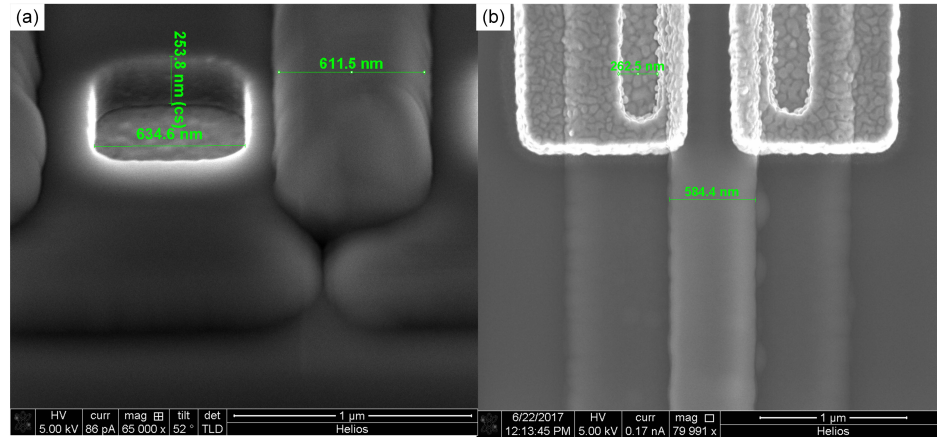


Figure 5.8. SEM pictures of MESFET (a) after via hole etching, and (b) after pad metalization.

5.2.3.1 Optimization of via hole ICP-RIE process

In the initial batch of devices, it was suspected that the via hole contacts were not always in good contact. As can be seen in Figure 5.8, the metal may be discontinuous at the via hole edges due to the vertical sidewalls formed using the CHF_3 based SiN_x ICP-RIE recipe. To solve this problem, the CHF_3 based ICP-RIE could be optimized to achieve more gently sloped sidewalls for better metal step edge coverage, through the use of higher pressure and reduced mask selectivity.

5.2.3.2 Ion-implanted isolation

For the first fabrication run of vertical GaN MESFETs, no device isolation or junction termination was used. A junction termination implant similar to that developed in Chapter 3 could be added to the process flow. Inclusion of a MESFET junction termination would lower the gate-edge fields by the combination of nitrogen implantation isolation and by trench etching through part of the drift layer. In this way, a box-like isolation structure is created, surrounding each MESFET with an insulating dielectric. This is expected to improve the gate-drain breakdown characteristics.

5.2.3.3 Device analysis

As noted in section 5.2.2, the measured results do not match the simulated results very well. Possible reasons for the observed discrepancy are fabrication process deviations, source via hole etch issues, and mismatch between the actual and intended epitaxial structure (thickness and doping). Additional analysis, by simulating variations of the design, could be useful to identify the key issues. Finally, fabrication and demonstration of the devices both on-wafer and after ELO would be valuable to augment the demonstrations of lifted-off diodes.

5.2.4 Further efforts—diodes

Although discrete diodes with BFOM comparable to the state of the art were developed and demonstrated, additional effort in this area could also be beneficial for power systems. Areas for improvement include exploration of more sophisticated ET structures (e.g. multi-stage ETs, different surface passivations and surface treatments, or more complex implants) for higher voltage operation. For many applications, 3 kV breakdown is needed. Another area for further study is thermal performance. Although an improvement on copper carriers was observed, a quantitative analysis of interfacial thermal resistance was not performed. Also, the potential benefits of ultra-high thermal conductivity substrates, such as diamond, could be a valuable area for further exploration. And finally, the prospects for ultra-thin flexible GaN electronics, made possible by ELO, could be an interesting area for additional exploration.

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