

Technical Glossary

A B C D E F G H I J K L M N O P Q R S T U V W X Y Z

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μm
see **micron**

3D IC
an integrated circuit (IC) formed by stacking wafers and/or dies vertically (three-dimensional) and connecting them electrically using through-silicon vias

3D NAND
a device architecture in which memory cells are arranged vertically (three-dimensional), rather than horizontally (planar) to increase memory bit density

components in a semiconductor device

CONFORMAL

a term used to describe uniform coverage of a layer of material over pre-existing topography; thickness of the layer remains the same everywhere on the surface of the feature

CONTACT

the conductive connection between the transistor and the first interconnect layer

higher electrical conductivity (faster) than aluminum interconnect

COPPER OVERBURDEN

excess copper deposited on top of the wafer after filling vias and trenches; later removed using chemical-mechanical planarization (CMP)

CRITICAL DIMENSION (CD)

a dimension that must be precisely fabricated to ensure proper device performance and/or yield

CVD

see **chemical vapor deposition**

D

DAMASCENE

a technique of forming conductive connections (wiring) between circuits by inlaying conductive materials, such as copper, into insulating layers

DEEP SILICON ETCHING

an anisotropic (directional) plasma etch process that creates high aspect ratio (tall and narrow) features in silicon; applications include MEMS devices and TSV structures