

Counter Doping into Uniformly and Heavily Doped Channel Region of Sub 0.1 μm SOI MOSFET's

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Abstract— We proposed counter doping into a heavily and uniformly doped channel region of SOI MOSFET's. This enabled us to suppress the short channel effects with proper threshold voltage V_{th} and to eliminate parasitic edge or back gate transistors. We derived a model for V_{th} as a function of the projected range, R_p and dose, Φ_D , of the counter doping, and showed that V_{th} is invariable even when the as-implanted counter doping profile redistributes. Using this technology, we demonstrated a V_{th} roll-off free 0.075 μm - L_{Geff} nMOSFET with low off-state current.

I. INTRODUCTION

A N SOI MOSFET provides low power operation due to its negligible junction capacitance. However, we must also realize superb short channel immunity with a low V_{th} and eliminate edge or back-gate transistors to suppress stand-by current [1]. To suppress the short channel effects, retrograde channel doping technology was developed [2]. However, the tradeoff between good short-channel immunity and a low V_{th} has not been sufficiently overcome in deep submicron gate length region. Using a thin-film SOI substrate with a thickness t_{Si} , and doping it with an ion implantation with a dose ϕ_B followed by sufficient thermal process, we can precisely obtain a uniformly and heavily doped substrate with a doping concentration $N_B = \phi_B/t_{Si}$. We showed that counter doping into this substrate (Fig. 1) satisfied above all demands for the low-power operation.

II. RESULTS AND DISCUSSION

In order to design the proposed SOI MOSFET's, we modeled threshold voltage and its stability against thermal processing.

Considering the arbitrarily counter doping profile $N_D(x)$ as shown in Fig. 1, we solved 1-D Poisson equation and found that the threshold voltage is given by

$$V_{th} = V_{FB} + 2\phi_F + \frac{Q_{B0}}{C_{Ox}} \left[\sqrt{1 + \frac{2R_p}{W_0} \left(\frac{Q_D}{Q_{B0}} \right)} - \frac{Q_D}{Q_{B0}} \right]$$

where

$$R_p = \frac{\int_0^\infty x N_D(x) dx}{\int_0^\infty N_D(x) dx}. \quad (1)$$

V_{FB} is the flat band voltage, C_{Ox} is gate capacitance per gate area, Q_{B0} and W_0 are depleted charge density and depletion

width without counter doping, respectively, and they are given by

$$V_{FB} = -\frac{k_B T}{q} \ln \left(\frac{N_{Dpoly} N_B}{n_i^2} \right) - \frac{Q_{ss}}{C_{Ox}}$$

$$\phi_F = \frac{k_B T}{q} \ln \left(\frac{N_B}{n_i} \right), \quad W_0 = \sqrt{\frac{2\epsilon_{Si}(2\phi_F)}{q N_B}}$$

$$Q_{B0} = q N_B W_0, \quad Q_D = q \Phi_D, \quad (2)$$

where k_B is the Boltzmann constant, T is the absolute temperature, q is the electron charge, N_{Dpoly} is the doping concentration of gate, Q_{ss} is the surface charge density, and n_i is the intrinsic carrier concentration. In the derivation process, all the counter dopants are assumed to be activated, and the region where the counter dopants are introduced is shallower than the depletion width. When Q_D is zero, that is, when there is no counter doping, (1) reduces to the V_{th} of conventional bulk MOSFET's [3] as is expected. Note that V_{th} is a function of R_p and Φ_D . Since Φ_D is constant if out diffusion is negligible, V_{th} is stable if R_p is invariable during thermal processing.

Assuming a Gaussian as-implanted counter doping profile, we derived models for redistributed profile and R_p during thermal processing given by

$$N_D(x, t) = \frac{\Phi_D}{\sqrt{2\pi(2Dt + \Delta R_p^2)}} \left[\exp \left[-\frac{(R_{p0} - x)^2}{2(2Dt + \Delta R_p^2)} \right] + \exp \left[-\frac{(R_{p0} + x)^2}{2(2Dt + \Delta R_p^2)} \right] \right] \quad (3)$$

$$R_p(t) = R_{p0} \operatorname{erf} \left[\frac{R_{p0}}{\sqrt{2(2Dt + \Delta R_p^2)}} \right] + \sqrt{\frac{2(2Dt + \Delta R_p^2)}{\pi}} \exp \left[-\frac{R_{p0}^2}{2(2Dt + \Delta R_p^2)} \right] \quad (4)$$

where R_{p0} is the R_p of the as-implanted profile. The diffusion profile of (3) consists of two Gaussian profiles instead of one which is the diffusion profile in an infinite plane. The two Gaussians profile is the results of the boundary condition at the gate oxide/Si substrate interface which is assumed to be $dN_D/dx = 0$. D is the diffusion coefficient of counter doped impurity and that of Sb in [4] was used.

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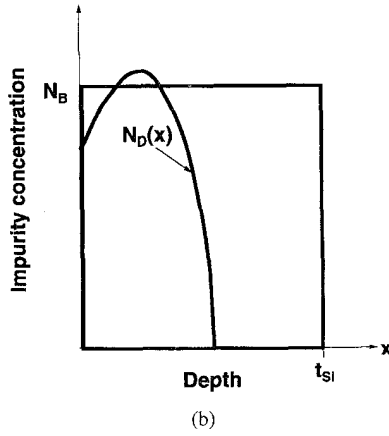
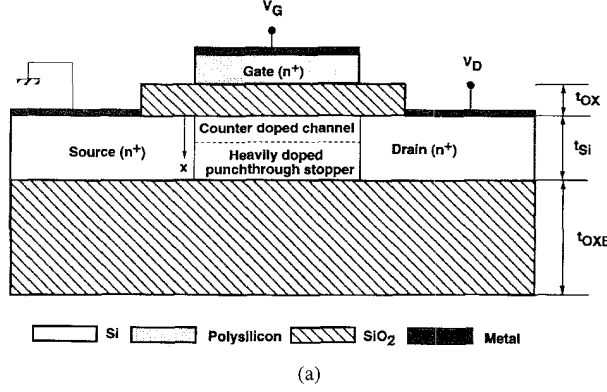


Fig. 1. (a) Proposed SOI nMOSFET. The channel region is first doped with B and subsequently enough annealed, resulting in a uniformly and heavily doped p^+ substrate with a doping concentration of N_B . Then, counter doping $N_D(x)$ was then introduced at the surface region by Sb ion implantation. It is a partial depleted device. (b) Schematic doping profile perpendicular to the channel.

Assuming $R_p - R_{p0}$ is small, the V_{th} variation during thermal processing ΔV_{th} is derived from (1) given by

$$\Delta V_{th} = \frac{Q_D}{C_{ox}} \frac{(R_p - R_{p0})}{W_0} \frac{1}{\sqrt{1 + \frac{2R_{p0}}{W_0} \left(\frac{Q_D}{Q_{B0}} \right)}}. \quad (5)$$

ΔV_{th} is then proportional to $R_p - R_{p0}$ for small $R_p - R_{p0}$.

R_p does not vary if $2(2Dt + \Delta R_p^2)$ is smaller than R_{p0}^2 as shown by Fig. 2, even when the as-implanted profile redistributes, that is, $2(2Dt + \Delta R_p^2)$ changes from its initial value. Therefore, we can define the critical time t_c for R_p variation as

$$t_c = \frac{R_{p0}^2}{2D} \left[1 - 2 \left(\frac{\Delta R_p}{R_{p0}} \right)^2 \right]. \quad (6)$$

In order to verify our model and demonstrate predicted superb short channel immunity with low off-state current, we fabricated sub $0.1\text{-}\mu\text{m}$ SOI MOSFET's using direct electron beam lithography.

After forming a 15-nm -thick SiO_2 layer by dry oxidation, B was ion implanted into a 100-nm -thick SOI substrate with 20 keV and a dose of $2 \times 10^{13}\text{ cm}^{-2}$, and then it was annealed at 1000°C for 60 min in dry nitrogen atmosphere, resulting in an uniformly doped substrate with N_B of 2×10^{18}

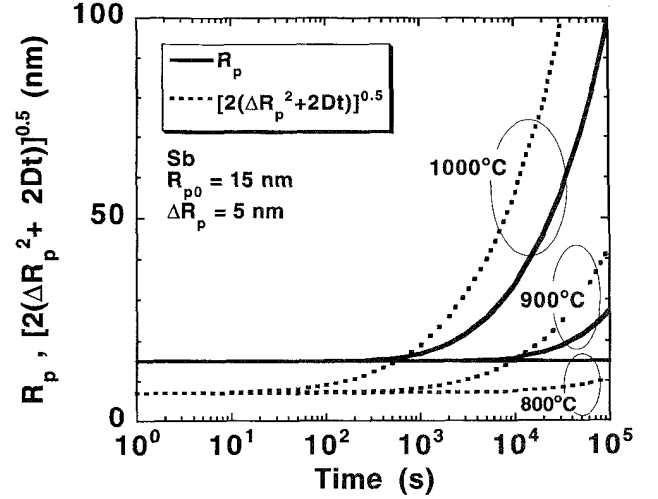


Fig. 2. Dependence of R_p on annealing time. R_p does not change if $2(2Dt + \Delta R_p^2)$ is smaller than R_{p0}^2 . The critical time, which provides $R_{p0}^2 = 2(2Dt + \Delta R_p^2)$, is 10 min for 1000°C , 2.8 h for 900°C , and more than a day for 800°C .

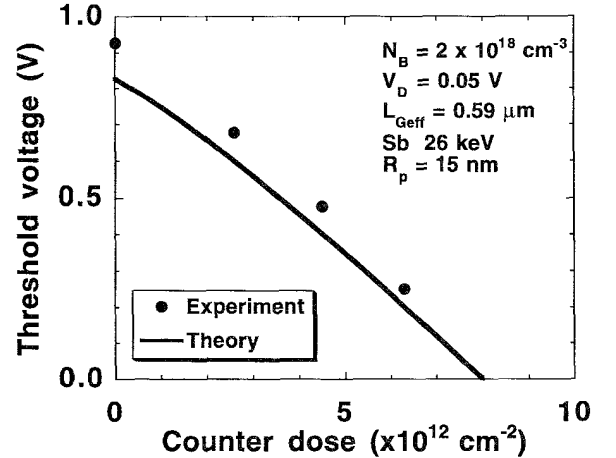


Fig. 3. Comparison between theory and experiment of dependence of V_{th} on counter dose. V_{th} is determined as the gate voltage at which $I_{DLG} = 1\text{ }\mu\text{A}\mu\text{m}$ where the device length $W = 10\text{ }\mu\text{m}$.

cm^{-3} . Then, a counter doping with Sb at 26 keV and various doses was done after removing the top oxide layer. A 4-nm -thick gate oxide was produced at 900°C , and conventional MOSFET process was followed. 1000°C for 5 s annealing was done to activate impurities in the source/drain regions. We evaluated the effective gate length of the device with split-CV measurement [5].

Using $R_p = R_{p0} = 15\text{ nm}$ and $\Delta R_p = 5\text{ nm}$ for as-implanted Sb data [6], we obtained good agreement between theory of (1) and experiment as shown in Fig. 3, although the device were subjected to thermal processing: 900°C for 10 min (gate oxidation), 800°C for 2 h (SiO_2 CVD), and 1000°C for 5 s (source/drain activation annealing). Q_{ss} is assumed to be zero. The stability of V_{th} against thermal processing is well explained by Fig. 2 in which t_c at each process temperature is much longer than the time the samples were thermal treated in the experiment.

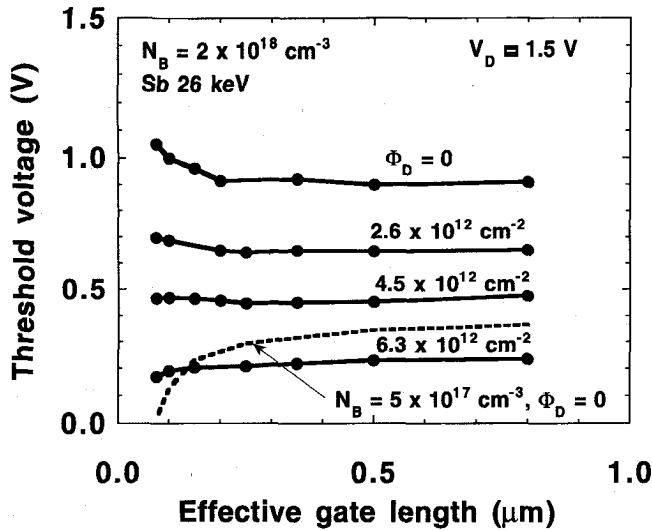


Fig. 4. Experimental dependence of threshold voltage on gate length with various counter doses, Φ_D .

Fig. 4 shows the dependence of V_{th} on gate length with various counter dose, Φ_D . We obtained a low V_{th} of 0.2 V and roll-off free characteristics down to L_{Geff} of 0.075 μm using a counter dose of $6.3 \times 10^{12} \text{ cm}^{-2}$. If we use a uniform channel doping concentration N_B of $5 \times 10^{17} \text{ cm}^{-3}$, we can adjust a proper threshold voltage, but suffer significant short channel effects in the deep submicron gate length region. The device also showed no “hump” in the subthreshold region, which means the elimination of parasitic transistors despite no introduction of channel-stop doping [1]. This is attributed to

the uniform and high back ground doping. The subthreshold swing of the device was 90 mV/decade at $V_D = 1.5 \text{ V}$ and its value was independent of gate length.

III. CONCLUSION

We proposed counter doping into a uniformly and heavily doped SOI substrate, which enabled us to adjust proper V_{th} while holding superb short channel immunity and to eliminate parasitic edge or back gate transistors without introducing channel cut doping. We also developed a model for V_{th} of this device, showed its stable characteristics against thermal processing, and verified its validity. We demonstrated roll-off free V_{th} characteristics down to 0.075 μm - L_{Geff} with a value of 0.2 V.

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