

Inergy Technology, Inc. (Petitioner)
v.
Force MOS Technology Co. Ltd. (Patent Owner)

Patent 7,629,634

Case IPR2024-00093

Patent Owner's Demonstratives

FORCEMOS Ex. 2036
Inergy v. Force MOS, IPR2024-00093

Agenda

1. Introduction to the '634 Patent

2. Claim construction

- “sidewalls of said trenches in said base layer are covered”
- “lateral contact layer”

3. Hirler Grounds

- Ground 1 - Anticipation - Claim 1
- Ground 2 - Obviousness in view of Kobayashi - Claim 3

4. Shiraishi Grounds

- Ground 3 - Anticipation - Claim 1
- Ground 4 - Obviousness in view of Kobayashi - Claim 3

5. Shiraishi and Kobayashi Grounds

- Ground 5 – Obviousness – Claims 1 and 3

Introduction to the '634 Patent

Problem:

bottom. The sidewall of source contact trench has no ohmic contact (due to low doping concentration of P base) with the contact metal plug resulting in poor ruggedness performance during UIS (Unclamp Inductance Switching) test. A parasitic

Ex. 1001 ('634 Patent) at 1:35-38 (cited by Paper 25 at 3)

Improvement:

According to the present invention, the silicon substrate, the epitaxial layer, and the source layer are N-type; the base layer and lateral contact layer P* are P-type; and each of the source contact trenches further has a P⁺-type base contact layer at a bottom thereof and the lateral contact layer P* has less doping concentration than the P⁺ base contact layer at the source contact trench but higher doping concentration than P-base layer to achieve ohmic contact between the P*-type region, which is lower doping concentration than P⁺-type region, and the contact metal plug while threshold voltage V_{th} is not significantly affected by P*-type region.

Ex. 1001 ('634 Patent) at 2:1-11 (cited by Paper 25 at 3)

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

See Paper 25 (POR) at 3-4

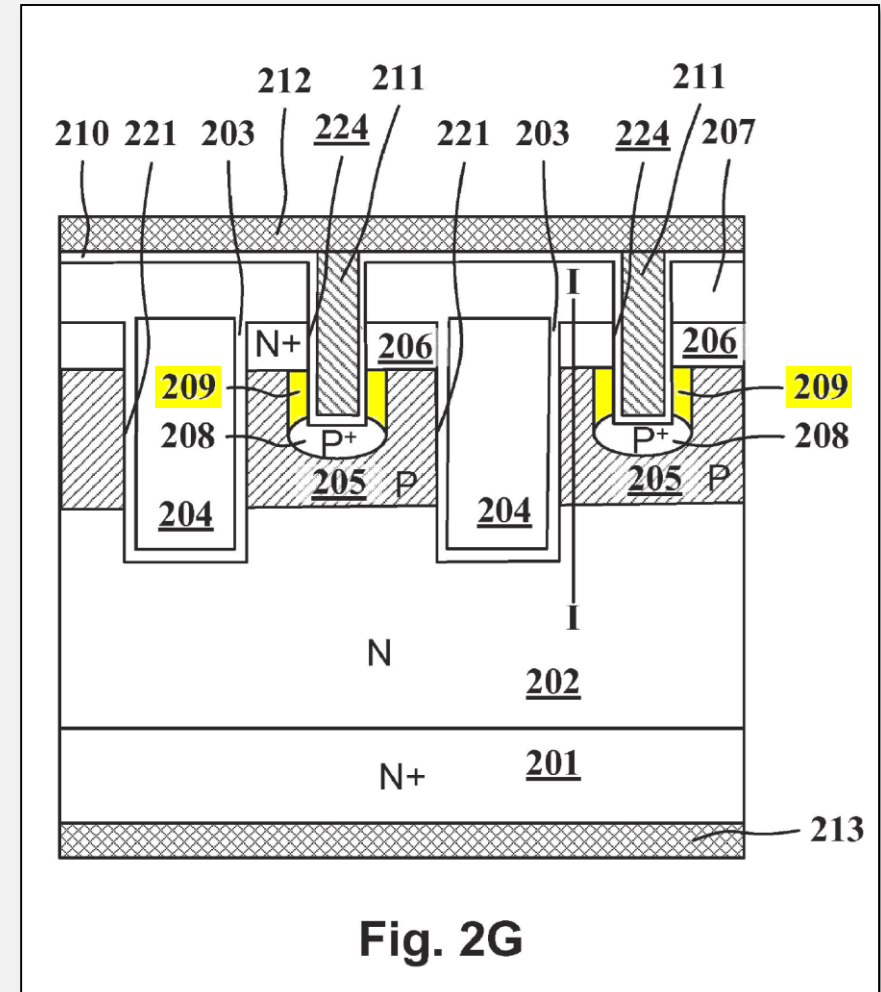


Fig. 2G

Ex. 1001 ('634 Patent) Fig. 2G
(cited by Paper 25 at 20)

Claim Construction

Claim Construction: “sidewalls of said trenches in said base layer”

Claim Term	Patent Owner’s Proposed Construction:	Petitioner’s Proposed Construction:
“sidewalls of said trenches in said base layer”	the <u>entire</u> sidewalls of the said trenches in said base layer	the <u>entire</u> sidewalls of the said trenches in said base layer

Paper 1 (Pet.) at 18-19

Paper 25 (POR) at 21

In the Petition, Petitioner, based on the prosecution history of the ’634 Patent, proposed that this term be construed as “the entire sidewalls of the said trenches in said base layer.” Pet., 18-19. Since then, two District Courts have likewise adopted the same construction as proposed by Petitioner. Ex. 2010, 6-9; Ex. 2011, 23. Accordingly, for the purpose of this proceeding, Patent Owner will apply Petitioner’s proposed construction. Moreover, an express construction of this term

Paper 25 (POR) at 21

Claim Construction: “lateral contact layer”

Claim Term	Patent Owner’s Proposed Construction:	Petitioner’s Proposed Construction:
“lateral contact layer”	a region of dopant which is implanted into sidewalls of the source contact trenches to have a dopant concentration between P and P+ (“P* doping”) for an N-channel MOSFET or between N and N+ (“N* doping”) in a P-channel MOSFET.	no express construction required

Paper 7 (Prelim. Resp.) at 4-8
Paper 25 (POR) at 7-21

Paper 27 at 1-21

Claim Construction: “lateral contact layer”

“lateral contact layer” is a Coined Term Without an Established Ordinary Meaning

Patent Owner’s Expert’s Unrebutted Testimony:

83. As a threshold issue, it is my opinion that the term “lateral contact layer” has no established meaning in either the field of trench MOSFETs or the field of semiconductors more generally. Instead, it is my opinion that “lateral contact layer” is a coined term used by the patentee for referring to the novel invention disclosed in the specification. Prior to my work on Force MOS matters, I had never heard the term “lateral contact layer” used in connection with MOSFETs or BJTs in the relevant time period (e.g., prior to 2008). Nor does the term appear in relevant technical dictionaries or glossaries. *See, e.g., Ex. 2016 (Semiconductor Glossary) at*

Ex. 2012 (Niekirk Decl.) at ¶83 (cited by Paper 25 at 11)

Unrebutted Expert Testimony that “lateral contact layer” Needs Construction to Avoid Potential Ambiguities: Ex. 2012 ¶¶ 85-94

Claim Construction: “lateral contact layer”

“lateral contact layer” Requires P* Doping

'634 Patent:

According to the present invention, the silicon substrate, the epitaxial layer, and the source layer are N-type; the base layer and lateral contact layer P* are P-type; and each of the source contact trenches further has a P⁺-type base contact layer at a bottom thereof and the lateral contact layer P* has less doping concentration than the P⁺ base contact layer at the source contact trench but higher doping concentration than P-base layer to achieve ohmic contact between the P*-type

Ex. 1001 ('634 Patent) at 2:1-9 (cited by Paper 25 at 15-16)

“When a patent ... describes the features of the ‘present invention’ as a whole, this description limits the scope of the invention.”

Verizon Servs. Corp. v. Vonage Holdings Corp., 503 F.3d 1295, 1308 (Fed. Cir. 2007)

Claim Construction: “lateral contact layer”

Claim Differentiation Does Not Apply—at Most Weak Presumption

'634 Patent:

2. The trench MOSFET of claim 1, wherein the silicon substrate, the epitaxial layer, and the source layer are N-type; the base layer and lateral contact layer are P-type; and each of the source contact trenches further has a P-type base contact layer at a bottom thereof, and the lateral contact layer has less doping concentration than the base contact layer at bottom.

Ex. 1001 ('634 Patent) at claim 2 (cited by Paper 25 at 18)

6. The trench MOSFET of claim 1, wherein the silicon substrate, the epitaxial layer, and the source layer are P-type; the base layer and lateral contact layer are N-type; and each of the source contact trenches further has a N-type base contact layer at a bottom thereof, and the lateral contact layer has less doping concentration than the base contact layer at bottom.

Ex. 1001 ('634 Patent) claim 6 (cited by Paper 25 at 18)

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Claim Construction: “lateral contact layer”

“lateral contact layer” Requires Implantation Into Sidewalls of Source Contact Trenches

’634 Patent:

FIGS. 3A and 3B are schematic sectional views for describing ion implantation into a source contact trench of the present invention; and

Ex. 1001 (’634 Patent) at 2:46-48 (cited by Paper 25 at 19)

tact trench (224). Referring to FIGS. 2E and 3B, thereafter, another implantation procedure of BF₂ with angle ranging from 45 to 80 degree respective to the surface of the epitaxial layer (202) and dose ranging from 1E14 to 4E14 cm⁻², and another activation by heat treatment are carried out to form a P*-type lateral contact layer (209) at the sidewall of the source contact trench (224) and corresponding to the P-type

Ex. 1001 (’634 Patent) at 3:55-61 (cited by Paper 25 at 19)

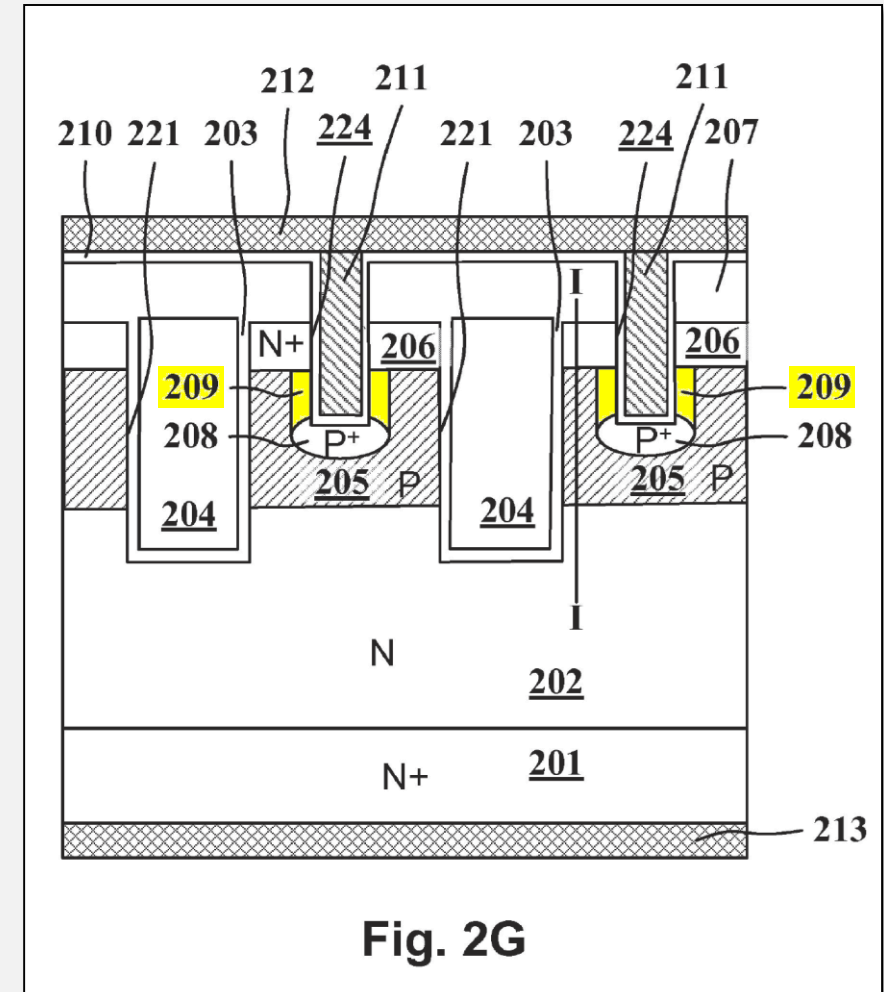


Fig. 2G

Ex. 1001 (’634 Patent) Fig. 2G
(cited by Paper 25 at 20)

Hirler v. Claim 1

Grounds 1 & 2

Hirler v. Claim 1 (grounds 1 & 2)

Hirler does not disclose “epitaxial layer” of limitation 1[a]

Petitioner’s Expert’s Conclusory Opinion:

66. Specifically, Hirler discloses “The starting point is an n+ substrate **10** of silicon, an n- drift zone **11**, p-body zone areas **12** as well as n+ source zone areas **13**.” Ex. 1006 at [0018], [0001]; Ex. 1005 at Fig. 1A, Fig. 2F. The POSITA would understand that Hirler’s Figure 2F (copied below with color annotations) shows a MOSFET with the drain region oriented at the bottom of the figure and layered as claimed, wherein (1) the “n+ substrate **10** of silicon” corresponds with “a silicon substrate,” (2) the “n- drift zone **11**” corresponds with “an epitaxial layer corresponding with a drain region,” (3) the “p-body zone areas **12**” corresponds with “a base layer corresponding to a said body region,” and (4) “n+ source zone areas **13**” corresponds with “a source layer corresponding to said source region” as provided in Claim 1 of the ’634 Patent. Ex. 1006 at [0018]; Ex. 1005 at Fig. 1A, Fig. 2F.

Ex. 1003 (Liu Decl.) at ¶66 (cited by Paper 25 at 22)

Patent Owner’s Expert’s Unrebutted Testimony:

110. Indeed, nowhere in Hirler is there a mention of “epitaxial” or “epitaxis” or similar words. Moreover, Hirler does not contain any description of how the “n- drift zone” was created. To the contrary, Hirler expressly states that its “starting point” has “an n+ substrate 10 of silicon [and] an n- drift zone 11,” and then only discusses manufacturing steps after that starting point. Ex. 1006, [0018]; Ex 1005, Figs. 1A, 2A. Accordingly, in my opinion, Hirler does not expressly disclose that n- drift zone is an epitaxial layer. I understand anticipation requires a showing that

Ex. 2012 (Niekirk Decl.) at ¶110 (cited by Paper 25 at 22)

113. Another alternative way for creating an N- layer on top of an N+ layer (as disclosed in Hirler)—without epitaxy—would be to use “counter-doping.”

Ex. 2012 (Niekirk Decl.) at ¶113 (cited by Paper 25 at 25)

114. One alternative way for creating an N- layer on top of an N+ layer (as disclosed in Hirler)—without epitaxy—would be to use “backside doping.” That is,

Ex. 2012 (Niekirk Decl.) at ¶114 (cited by Paper 25 at 25)

Hirler v. Claim 1 (grounds 1 & 2)

Petitioner's Argument that Hirler's "Successively Provided" Language Demonstrates an "Epitaxial Layer" Fails

1. Improper new reply argument: Hirler's claim 1 and "successively provided" argument not presented in Petition or expert declaration
2. Based solely on attorney argument
3. No evidence or argument why "successively provided" necessarily requires thin layer of single crystal material deposited on substrate

Hirler v. Claim 1 (grounds 1 & 2)

Hirler Does Not Disclose Limitation 1[g]’s “lateral contact layer” — Body Amplification Zone is Not P* Doped

Hirler:

[0030] In accordance with **Fig. 2C**, p⁺ implantation body amplification zones **19** are now implanted through the source zone areas **13**. In this case, a

Ex. 1006 (Hirler) at ¶0030 (cited by Paper 25 at 30)

Petitioner’s Expert:

29. The ‘634 Patent describes the lateral contact layer (209) as being doped to P*-type, the base contact layer (208) at the bottom of the source contact trench is P+-type, and the body of the MOSFET (205) is P-type. Ex. 1001 at 3:50-56, 3:65-4:6, 5:9-15. Doping concentration P* is doped more heavily than P but less than P+. *Id.*

Ex. 1003 (Liu Decl.) at ¶29 (cited by Paper 25 at 31)

Patent Owner’s Expert:

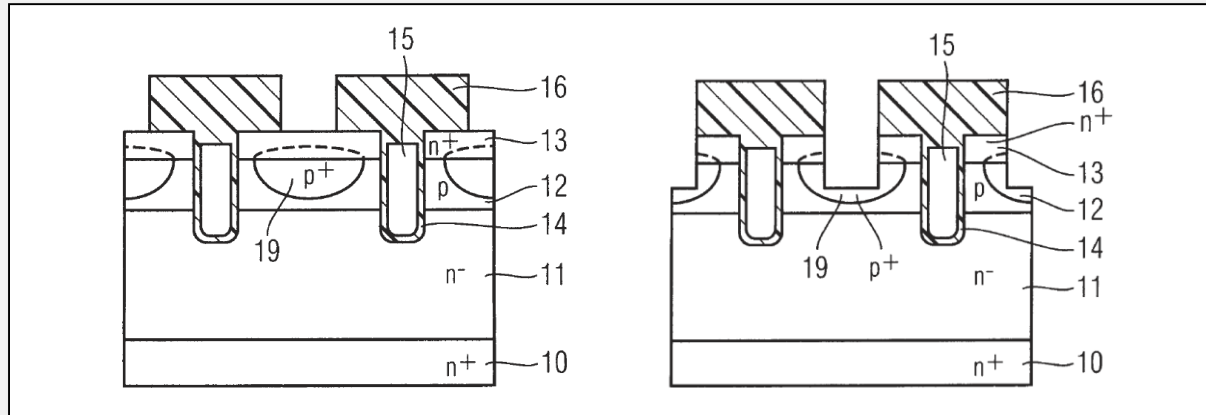
123. Second, the cited disclosures of Hirler also do not demonstrate that Hirler satisfies Force MOS’s proposed construction of “lateral contact layer” because Hirler discloses that “body amplification zone 19” has “P+” doping rather than “P*” doping. Ex. 1006 (Hirler), [0030]; *see also* ‘634 Patent at 2:1-8 (“lateral contact layer P* has less doping concentration than [] P+”). Also, in my opinion, a

Ex. 2012 (Nie Kirk Decl.) at ¶123 (cited by Paper 25 at 31)

Hirler v. Claim 1 (grounds 1 & 2)

Hirler Does Not Disclose Limitation 1[g]'s “lateral contact layer” — Body Amplification Zone Is Not Implanted *Into* A Source Contact Trench

Hirler:



Ex. 1005 (Hirler) at Fig. 2C and 2D (cited by Paper 25 at 28)

[0030] In accordance with **Fig. 2C**, **p⁺ implantation body amplification zones 19** are now implanted through the source zone areas 13. In this case, a photoresist layer (not drawn) serving to etch the silica layer 16 can serve as an additional masking layer. The body amplification zones 19 are implanted (cf. **Fig. 2E**) with the body contact zones 17 already explained on the basis of **Fig. 1D** and **Fig. 1E** after insertion of the contact trench (cf. **Fig. 2D**). **The contact trench is etched so deep that it is driven into the body amplification zone 19.** The body amplification zone 19 is practically not adjacent to the

Ex. 1006 (Hirler) at ¶0030 (cited by Paper 25 at 29)

Patent Owner's Expert's Unrebutted Testimony:

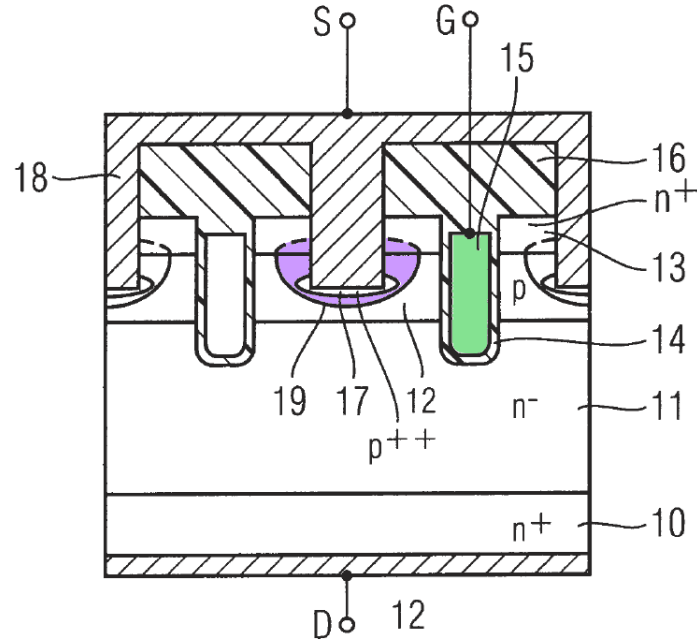
119. First, Hirler's "body amplification zone 19" (which Dr. Liu equates to the claimed "lateral contact layer"), is created by ion implantation *before* Hirler's contact trenches are etched. Ex. 1006 (Hirler), [0030], Figs. 2C-2D. Thus, Hirler does not disclose a region of dopant which is *implanted into sidewalls* of the source contact trenches. This is required by Force MOS's proposed construction, discussed above, and thus Hirler cannot satisfy "lateral contact layer" under Force MOS's construction.

Ex. 2012 (Nie Kirk Decl.) at ¶119 (cited by Paper 25 at 28)

Hirler v. Claim 1 (grounds 1 & 2)

The Differences in Hirler's Body Amplification Zone's Implantation are Structural

Hirler:



Ex. 1005 (Hirler) at Fig. 2F (cited by Paper 25 at 29)

[0036] In addition, the implantation of the body amplification zones 19 can be adjusted in such a manner that the lateral extensions reach the vicinity of the channel in the area of the trench gates 14, 15 after subsequent

Ex. 1006 (Hirler) at ¶0036 (cited by Paper 25 at 29)

Patent Owner's Expert's Unrebutted Testimony:

121. Moreover, in my opinion, this distinction is more than a mere difference in manufacturing methods but reflects substantively different structures. As shown

. . .

compare id., Fig. 2F with '634 Patent, Fig. 2G. A POSITA would understand that such step would risk increased P dopant concentration in the channel area, which would harm threshold voltage, particularly if the gate trench masks were not well aligned with the mask used to create the body amplification zone. This issue would be exacerbated as a MOSFET designer tried to increase cell density of the MOSFET. Such an increase of threshold voltage is exactly the situation the '634 Patent tries to avoid. Ex. 1001 ('634 Patent) at 2:10-11, 5:12-16, 5:27-29, Figs. 2G, 4.

Ex. 2012 (Niekirk Decl.) ¶¶121-122 (cited by Paper 25 at 29-30)

Combination of Hirler and Kobayashi v. Claim 3

The trench MOSFET of claim 2, wherein further comprises a barrier metal layer and a plurality of contact metal plugs.

Ground 2

Combination of Hirler and Kobayashi v. Claim 3 (ground 2)

Petitioner's Obviousness Theory Assumes, Without Explanation, Selection of Hirler's Tungsten Contact Embodiment

Hirler:

[0022] In accordance with **Fig. 1E** then a metallization **18** of for example **aluminum** is applied, which contacts the contact zones **17** and the source zone areas **13**. This metallization **18** forms a source connection S. On the side of the substrate facing away from the drift zone **11**, an unspecified metallization of, for example, **aluminum** is applied, which forms a drain connection D. The gate electrodes **15** form a gate connection G. A structure similar to the one described above is known from DE 102 34 996.7.

[0023] The trench can also be filled with a conductive stopper made of, for example, **polycrystalline silicon** or **tungsten**. The aluminum metallization is then applied to said stopper.

Ex. 1006 (Hirler) at ¶¶0022-0023 (cited by Paper 25 at 33)

Petition's Obviousness Theory:

Second, the POSITA would have been motivated to combine the **barrier metal layer** disclosed in Kobayashi to the MOSFET disclosed in Hirler. In general, a POSITA would know that the use of a **barrier metal layer**, made of materials such as Ti and TiN, would help to **promote the adhesion of the tungsten contact plug expressly taught in Hirler** to the contact area. Ti and TiN also serve as a barrier layer to **prevent** unwanted elements, such as **fluorine from the deposition process of W**, seeping into the underlying silicon surface, which would degrade the performance of the transistor. Thus, the POSITA would be motivated to apply a known solution (the barrier layer) to a known problem (unwanted seeping of fluorine into the silicon surface) to yield predictable results. Ex. 1003 at ¶¶ 90-93.

Paper 1 (Pet.) at 33

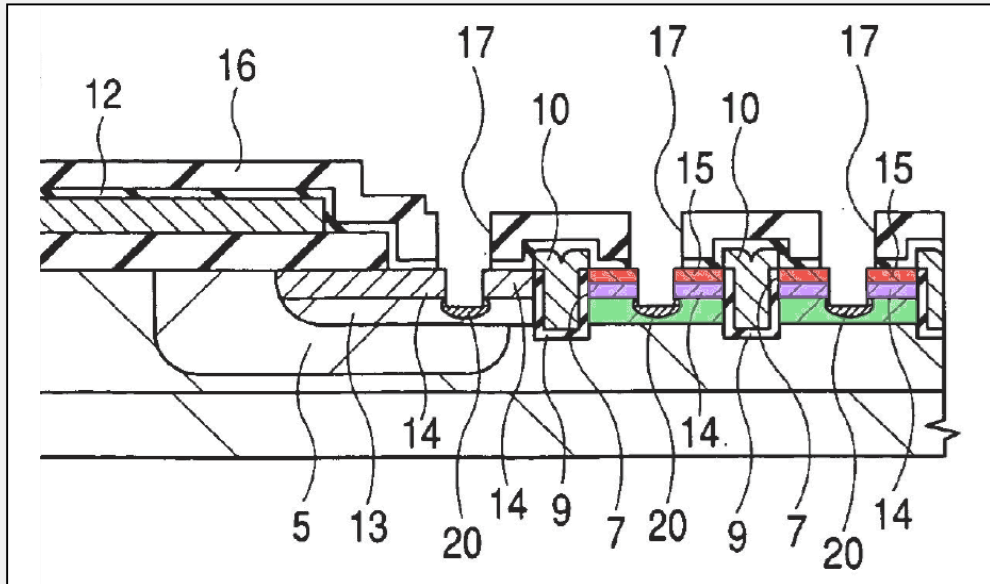
Shiraishi v. Claim 1

Grounds 3 & 4

Shiraishi v. Claim 1 (grounds 3 & 4)

Shiraishi Does Not Disclose 1[a]’s “source layer ... disposed on the top of said base layer”

Shiraishi:



Ex. 1009 (Shiraishi) at Fig. 8 (cropped) (cited by Paper 25 at 39)

resulting in an increase in the ON-resistance. Accordingly, the p-type semiconductor region 14 may be locally higher in impurity concentration than the p type semiconductor region 13, and is formed inside the p-type semiconductor region 13 without raising the impurity concentration of the p-type semiconductor region 13, thereby causing the p-type semiconductor region 14 to function as a punch-through stopper layer. By so doing, the occurrence of punch through can be

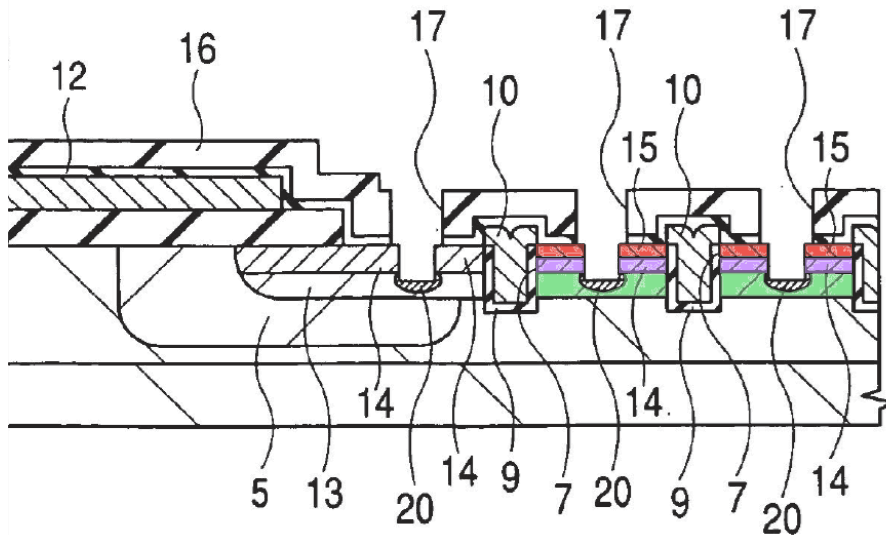
Patent Owner’s Expert’s Unrebutted Testimony:

138. Furthermore, it is well understood that in MOSFETs, the body region contains the region where the channel is formed when the gate is in an “ON” state (and where the channel is absent where the gate is in an “OFF” state). *See, e.g.*, Ex. 2030 (Sedra, Adel S., *Microelectronic Circuits* (5th Ed. 2004)) at 236-238 (§ 4.1.1). However, Shiraishi only identifies layer 13 (not layer 14) as being the “channel layer” or “acting as a base.” Ex. 1009 (Shiraishi), [0072]-[0073], [0080], [0084]. By contrast, layer 14 is identified in Shiraishi as a “punch-through stopper layer,” not a base layer, body region, or channel region. *Id.* at [0073], [0081]. This indicates that layer 14 of Shiraishi is not part of the body region or base layer. Indeed, Dr. Liu provides no analysis to the contrary. However, layer 14 of Shiraishi is interposed between the source layer (15) and the base layer (13), which is inconsistent with the specific structure of limitation 1.a, which requires “a source layer corresponding to said source region disposed on the top of said base layer.”

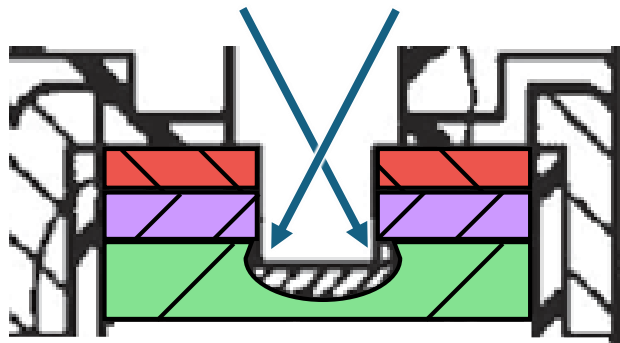
Shiraishi v. Claim 1 (grounds 3 & 4)

Shiraishi Does Not Disclose Limitation 1[g]’s “lateral contact layer”—Layer 14 Does Not Cover Entire Sidewalls in Base Layer

Shiraishi:



Portions of sidewalls in base layers not covered by layer 14



Patent Owner’s Expert’s Unrebutted Testimony:

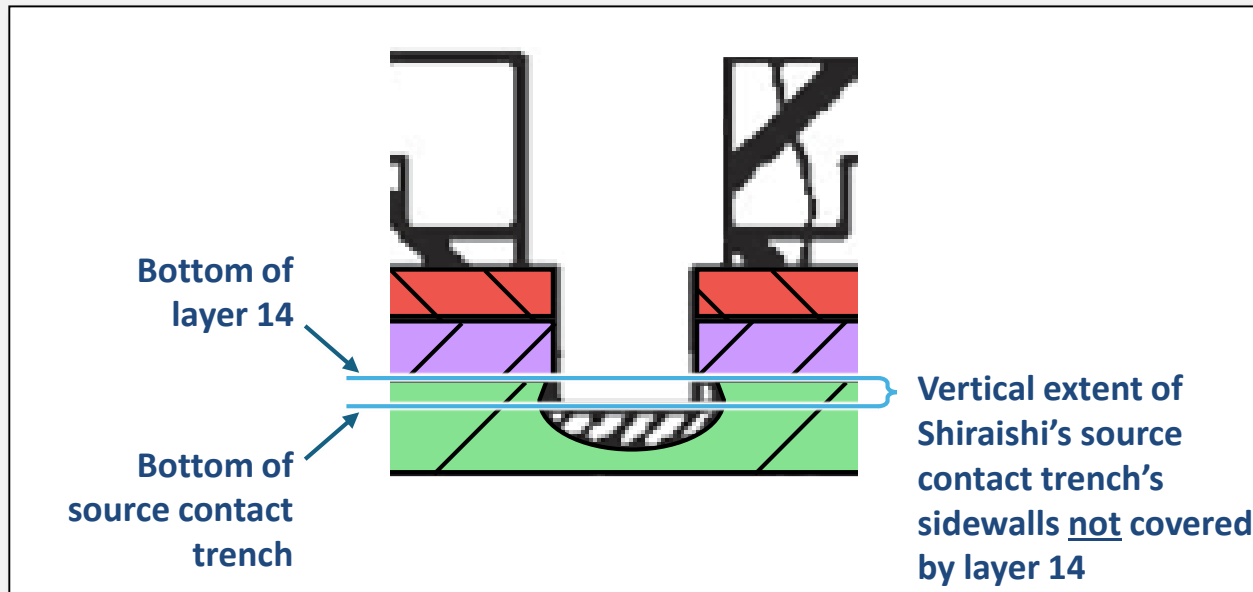
contact layer cover “entire” sidewalls of the trench in the base layer. Dr. Liu provides no explanation why Shiraishi satisfies Petitioner’s own construction of “sidewalls of said trenches in said base layer” requiring that the lateral contact layer cover the “entire” side wall in the base layer. Indeed, Shiraishi’s own figures plainly indicate that there are portions of the base layer (i.e., portions of layer 13 below layer 14) adjacent to the sidewalls, i.e., portions of the sidewalls in the base layer not covered by the alleged lateral contact layer:

Ex. 2012 (Niekirk Decl.) at ¶142 (cited by Paper 25 at 43)

Shiraishi v. Claim 1 (grounds 3 & 4)

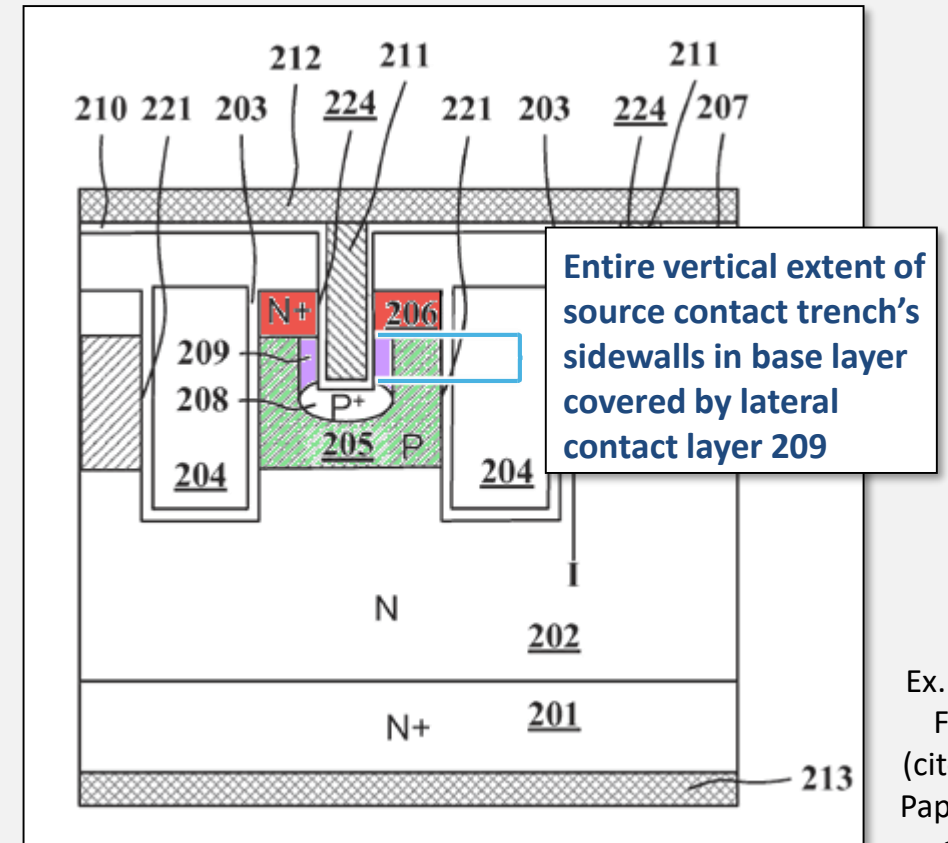
Petitioner's Reply Argument That layer 14 Covers Entire Sidewalls in Base Layer Contradicts '634 Patent

Shiraishi:



Ex. 1009 (Shiraishi) at FIG.8 (cropped and annotated (cited by Paper 28 at 21))

'634 Patent:



Ex. 1001
Fig. 2g
(cited by
Paper 28
at 21)

“sidewalls ... in said base layer” = sidewalls in vertical extent of base layer (e.g. top of layer 14 to bottom of trench)

Shiraishi v. Claim 1 (grounds 3 & 4)

Shiraishi Does Not Disclose Limitation 1[g]’s “lateral contact layer” — No Teaching That layer 14 Has P* Doping

Shiraishi:

[0073] Subsequently, by use of a photo resist film patterned by photolithographic techniques as a mask, dopant ions (for example B) having the p-type conductivity may be implanted into the n⁻ type single crystal silicon layer 1B at a concentration in the order of 3×10^{12} ions/cm², thereby forming a p-type semiconductor region (fifth semiconductor layer) 14 higher in impurity concentration than the p⁻type semiconductor region 13. The photo mask uses in patterning

Ex. 1009 (Shiraishi) at ¶0073 (cited by Paper 25 at 49)

Patent Owner’s Expert’s Unrebutted Testimony:

150. Second, Dr. Liu provides no identification or explanation why Shiraishi’s layer 14 has P* doping. The ’634 Patent recites that: “[a]ccording to the present invention, the silicon substrate, the epitaxial layer, and the source layer are N-type; the base layer and lateral contact layer P* are P-type; and each of the source contact trenches further has a P⁺-type base contact layer at a bottom thereof and the lateral contact layer P* has less doping concentration than the P⁺ base contact layer at the source contact trench but higher doping concentration than P-base layer.” Ex. 1001 (’634 Patent) at 2:1-8. Because Shiraishi’s layer 13 is “P” doping (i.e., weakly doped with positive dopants), Shiraishi’s disclosure that layer 14 has a higher doping concentration than layer 13 does not necessarily imply that Shiraishi’s layer 14 has P* doping. Ex. 1009 (Shiraishi), [0073]. Indeed, Shiraishi does not disclose

Shiraishi v. Claim 1 (grounds 3 & 4)

Shiraishi Does Not Disclose Limitation 1[g]’s “lateral contact layer” — Layer 14 Is Not Implanted Into A Source Contact Trench

Shiraishi:

[0073] Subsequently, by use of a photo resist film patterned by photolithographic techniques as a mask, dopant ions (for example B) having the p-type conductivity may be implanted into the n⁻ type single crystal silicon layer 1B at a concentration in the order of 3×10^{12} ions/cm², thereby forming a p-type semiconductor region (fifth semiconductor layer) 14 higher in impurity concentration than the p⁻type semiconductor region 13. The photo mask uses in patterning

Ex. 1009 (Shiraishi) at ¶0073 (cited by Paper 25 at 45)

Patent Owner’s Expert’s Unrebutted Testimony:

146. First, Shiraishi’s layer 14 is implanted across the entire active region of the semiconductor surface *prior* to the sidewalls of a source contact trench existing.

Ex. 1009 (Shiraishi), Figs. 6-7, [0073] (“dopant ions (for example B) having the p-type conductivity may be implanted into the n⁻ type single crystal silicon layer 1B at a concentration in the order of 3×10^{12} ions/cm², thereby forming a p-type semiconductor region (fifth semiconductor layer) 14”), [0074] (“the insulating film 16, the silicon oxide film 12, and the substrate 1 are etched, thereby forming contact grooves (a second groove part) 17”). Thus, Shiraishi does not disclose a region of dopant which is *implanted into sidewalls* of the source contact trenches. This is required by Force MOS’s proposed construction (discussed above), and thus Shiraishi cannot satisfy that construction.

Ex. 2012 (Niekirk Decl.) at ¶146 (cited by Paper 25 at 45)

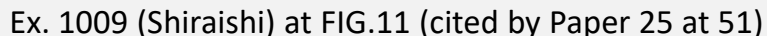
Combination of Shiraishi and Kobayashi v. Claim 3

The trench MOSFET of claim 2, wherein further comprises a barrier metal layer and a plurality of contact metal plugs.

Ground 4

Petitioner Failed to Articulate Any Reason for Selecting Plugs

Patent Owner's Expert's Unrebutted Testimony:



Ex. 2012 (Niekirk Decl.) at ¶154 (cited by Paper 25 at 51)

Combination of Kobayashi and Shiraishi v. Claim 1

Ground 5

Combination of Kobayashi and Shiraishi v. Claim 1 (ground 5)

No Articulated Reason Why Kobayashi Would Benefit from Shiraishi's Punch-Through Stopper Layer

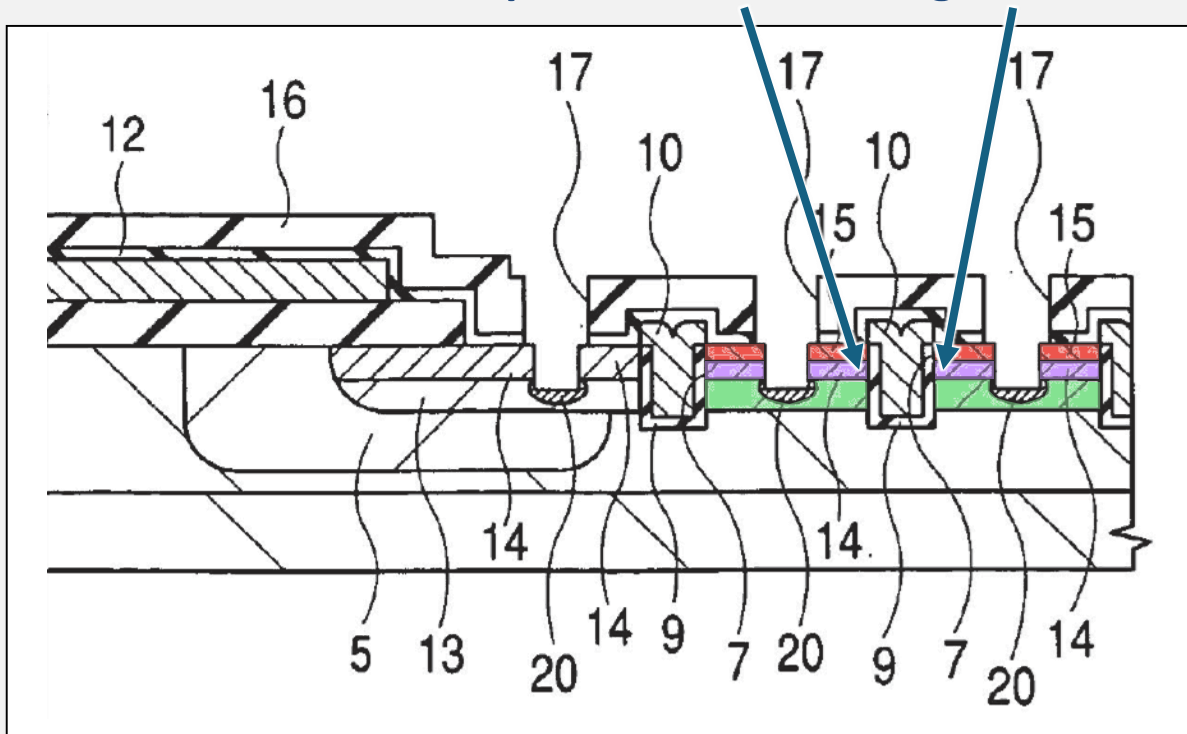
160. Moreover, although Dr. Liu says there would be a motivation to avoid punch through, Dr. Liu identifies no reason why Kobayashi 174's MOSFET has punch through issues which are not already adequately addressed by Kobayashi 174's design. Nor does Dr. Liu provide any analysis explaining that punch through would be a significant limiting criteria in attempting to improve the cell density (i.e., reducing cell pitch) of Kobayashi 174's designs as opposed to other obstacles (e.g., on-resistance, threshold voltage, avalanche breakdown, latch-up, gate capacitance, etc.). Indeed, it is well-known in the art of MOSFET that some designs have the limiting form of breakdown be avalanche breakdown, others have Zener breakdown, and others have punch-through. Ex. 2031 (Williams, Principles and Elements of

Ex. 2012 (Niekirk Decl.) at ¶160 (cited by Paper 25 at 55)

Combination of Kobayashi and Shiraishi v. Claim 1 (ground 5)

Shiraishi's Punch-Through Stopper Layer Conflicts With Kobayashi's Purpose

Shiraishi adds dopants to channel region



Ex. 1009 (Shiraishi), Fig. 8 (cropped and annotated) (cited by Paper 1 at 40)

Kobayashi is Directed to Avoiding Increased Threshold Voltage from Addition of Dopants to Channel Region

Specifically, when the P⁺-type contact layer is formed at the bottom of the contact hole, the impurity concentration in a channel region is increased by lateral or horizontal diffusion. Therefore, a threshold voltage (V_t) is increased. In order to prevent the increase of V_t, it is necessary to widen the space between the trench gate and the contact. As a consequence, miniaturization of the cell can not be achieved. Since the

Ex. 1008 (Kobayashi) at ¶10014 (cited by Paper 25 at 56)

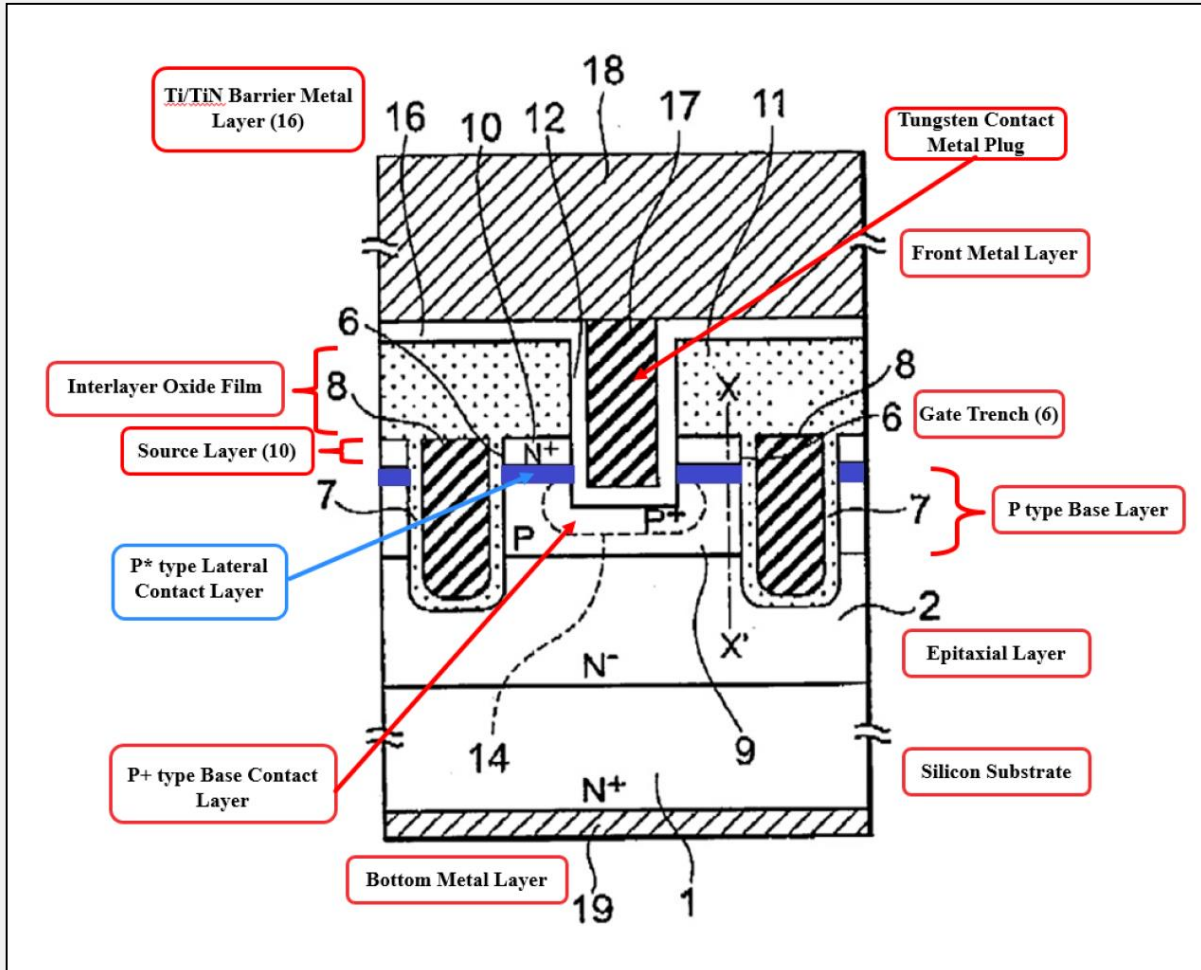
[0037] According to this invention, the contact is formed to the depth different from the peak depth of the impurity concentration of the base layer. Thus, it is possible to suppress an influence upon a channel region by the impurity of the base contact layer formed at the bottom of the contact and to reduce the cell size without increasing V_t. Furthermore, since the base contact layer is not present on the side wall of the contact, a source layer resistance is not increased. Furthermore, it is possible to flatten the surface of the source electrode and to decrease a bonding resistance.

Ex. 1008 (Kobayashi) at ¶10037 (cited by Paper 25 at 56)

Combination of Kobayashi and Shiraishi v. Claim 1 (ground 5)

No Motivation to Combine to Cover Entire Sidewalls in the Base Layer as Required by Limitation 1[g]

Petitioner's Proposed Combination:



Ex. 1009 (Shiraishi) at Fig. 5A (Annotated) (cited by Paper 1 at 64)

Patent Owner's Expert's Unrebutted Testimony:

165. Moreover, it is important in Shiraishi that layer 13 have significant depth beyond layer 14, as layer 13 provides the channel region adjacent to the gate and increasing layer 13's doping would increase threshold voltage. Ex. 1009 (Shiraishi), [0072], [0080]. Thus, combining Shiraishi with Kobayashi 174 to have Shiraishi's punch through layer 14 along the "entire" depth of the source contact trench's sidewalls would be inconsistent with Shiraishi's teachings.

Ex. 2012 (Niekirk Decl.) at ¶165 (cited by Paper 25 at 58, 61-62)

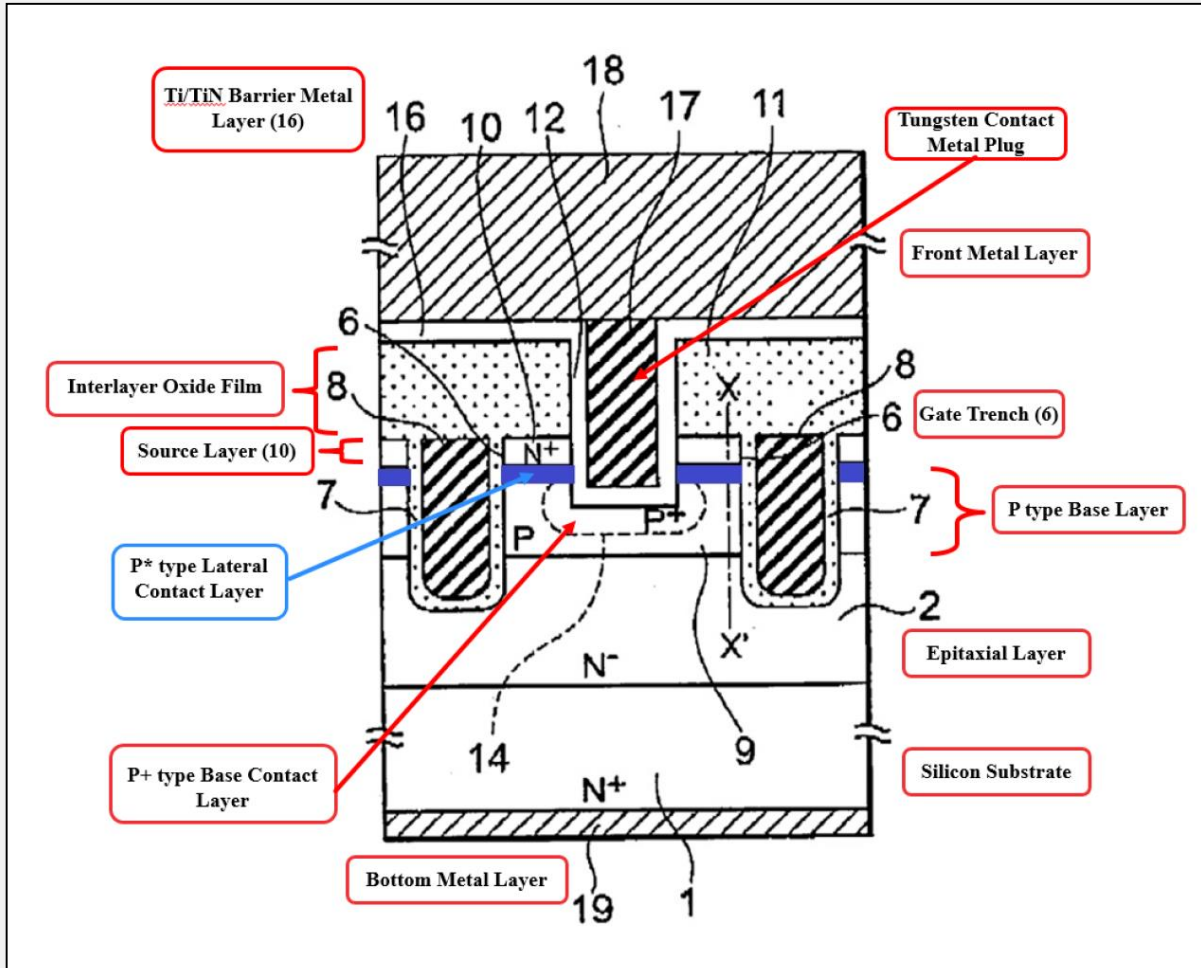
166. Combining Shiraishi and Kobayashi to have "entire" coverage of the sidewalls with Shiraishi's layer 14 would also be inconsistent with Kobayashi's teachings. Indeed, as discussed above in the motivation to combine section, Kobayashi expressly teaches avoiding having increased doping concentration on the source contact trench sidewalls. Instead, Kobayashi addresses the issue of increased

Ex. 2012 (Niekirk Decl.) at ¶166 (cited by Paper 25 at 61-62)

Combination of Kobayashi and Shiraishi v. Claim 1 (ground 5)

Proposed Combination Does Not Satisfy 1[a] or 1[g] For Same Reasons as Shiraishi

Petitioner's Proposed Combination:



Ex. 1009 (Shiraishi) at Fig. 5A (Annotated) (cited by Paper 1 at 64)

Patent Owner's Expert's Unrebutted Testimony:

163. In particular the use of Shiraishi's stopper layer 14 across the entire semiconductor material between the gate and source layer is inconsistent with the specific structure of layers and regions recited in limitation 1.a, which recites "source layer corresponding to said source region disposed on the top of said base layer." And, as discussed above, Dr. Liu's identification of the "lateral contact layer" as Shiraishi's layer 14 and the claimed "base layer" as Kobayashi's "base layer 9" is inconsistent with limitation 1.g (which requires the "lateral contact layer" to be present at the sidewalls in the base layer); and (3) Dr. Liu identifies no disclosure or motivation in either of the references to use P* doping (or N* doping for a P-Channel MOSFET) for a layer at the source contact trench sidewalls, as required by limitation 1.g.

Ex. 2012 (Nie Kirk Decl.) at ¶163 (cited by Paper 25 at 59, 61-62)

Combination of Kobayashi and Shiraishi

v.

Claim 3

The trench MOSFET of claim 2, wherein further comprises a barrier metal layer and a plurality of contact metal plugs.

Ground 5

Combination of Kobayashi and Shiraishi v. Claim 3 (ground 5)

*No motivation to use plugs in Petition
and thus suffers from same issues as Shiraishi vs. claim 3*