Paper No. _____

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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Inergy Technology, Inc.,

Petitioner

v.

Force Mos Technology Co., Ltd.,

Patent Owner

Patent No. 7,812,409

Issue Date: October 12, 2010

Title: TRENCH MOSFET WITH CELL LAYOUT, RUGGEDNESS, TRUNCATED CORNERS

Inter Partes Review No. IPR2024-00094

PETITION FOR *INTER PARTES* REVIEW OF CLAIMS 1-6 OF U.S. PATENT NO. 7,812,409 UNDER 35 U.S.C. §§ 311-319 AND 37 C.F.R. § 42.100 *ET. SEQ.*

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EXHIBIT LIST

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1001	U.S. Patent No. 7,812,409 (the "'409 Patent" or "Patent-in-Suit")
1002	File History for the U.S. Patent No. 7,812,409
1003	Declaration of Dr. David Liu
1004	Curriculum Vitae of Dr. David Liu
1005	U.S. Patent No. 6,888,196, Kobayashi ("Kobayashi")
1006	U.S. Patent No. 5,763,914, Hshieh et al ("Hshieh")
1007	Kikkawa, T. et al, "A Quarter-Micrometer Interconnection Technology Using a TiN/Al-Si-Cu/TiN/Al-Si-Cu/TiN/Ti Multilayer Structure," IEEE Transactions on Electron Devices, Vol. 40, No. 2, February 1993 ("Kikkawa")
1008	Declaration of Dr. Sylvia D. Hall-Ellis
1009	Complaint, *Force Mos Technology, Co. Ltd. v. Asustek Computer, Inc.*, No. 2:22-cv-00460 (E.D. Tex.)
1010	First Amended Complaint, *Force Mos Technology, Co. Ltd. v. Asustek Computer, Inc.*, No. 2:22-cv-00460 (E.D. Tex.)
1011	U.S. Patent No. 6,541,818 to Pfirsch et al. ("Pfirsch")
1012	Kim, Sang-Gi et al., "Trench Corner Rounding Technology Using Hydrogen Annealing for Highly Reliable Trench DMOSFETs," International Symposium on Power Semiconductor Devices and ICs (ISPSD), May 22-25, 2000, Toulouse France
1013	Curriculum Vitae of Dr. Sylvia D. Hall-Ellis
1014	Attachment 1A MARC Record

EXHIBIT NUMBER	DESCRIPTION
1015	Attachment 1B Library of Congress Authorities sh 85042254
1016	Attachment 1C Library of Congress Authorities sh 85099890
1017	Attachment 1D OCLC
1018	Docket Control Order, *Force Mos Technology, Co. Ltd. v. Asustek Computer, Inc.*, No. 2:22-cv-00460 (E.D. Tex.)

LIST OF CHALLENGED CLAIMS

Claim 1	
1[preamble]	A trenched semiconductor power device comprising a plurality of trenched gates surrounding a plurality of transistor cells formed in a semiconductor substrate, wherein:
1[a]	wherein: said trenched gates surrounding said transistor cells as closed cells constituting substantially square-shaped cells with rounded corners;
1[b]	each of said closed cells further includes a circular trench contact disposed substantially in a central portion of said closed cells, penetrating through a source region surrounding said trenched gates and extending into a body region encompassing said source region;
1[c]	said circular trench contact comprises a hole opened from a top surface of said semiconductor substrate and is filled with a contact metal plug
1[d]	wherein sidewalls of said hole are surrounded by and in contact said source and body regions
1[e]	and said circular trench contact is separate from said trenched gates with said source region and body region disposed between a gate oxide lining of said trenched gates and all circumferential points of the circular trench contact;
1[f]	and said contact metal plug connected to a source metal disposed on top of said circular trench contact.
Claim 2	
The trenched semiconductor power device of claim 1 further comprising: a contact resistance reduction metal layer composed of a titanium (Ti) layer disposed above a top surface said contact metal plug and below a bottom surface of said source metal for reducing a contact resistance between said contact metal plug and said source metal.	
Claim 3	
The trenched semiconductor power device of claim 1 wherein: said contact metal plug disposed in said hole of said circular trench contact further comprising a Ti/TiN/W metal plug.	

Claim 4	
The trenched semiconductor power device of claim 1 wherein: said source metal disposed on top of and in contact with a top surface of said metal plug further comprising a layer composed of aluminum alloys including alloys of AlCu or AlSiCu.	
Claim 5	
The trenched semiconductor power device of claim 1 wherein: a diameter of a top surface of said circular trench contact is smaller than 1.0 micrometer.	
Claim 6	
6[preamble]	A trenched semiconductor power device comprising a plurality of trenched gates surrounding a plurality of transistor cells formed in a semiconductor substrate, wherein:
6[a]	said trenched gates surrounding said transistor cells as closed cells constituting substantially square-shaped cells with truncated corners;
6[b]	each of said closed cells further includes a circular trench contact hole disposed substantially in a central portion of said closed cells with a diameter of a top surface of said circuit trench contact less than 1.0 micrometer, penetrating through source regions surrounding said trenched gates and extending into body regions encompassing said source regions;
6[c]	said circular trench contact comprises a hole opened from a top surface of said semiconductor substrate
6[d]	wherein sidewalls of said hole are surrounded by and in contact with said source and body regions and
6[e]	said circular trench contact and is separate from said trenched gates with said source region and body region disposed between a gate oxide lining of said trenched gate and all circumferential points of the circular trench contact; and
6[f]	said circular trench contact hole is filled with a metal plug composed of a Ti/TiN/W plug to contact said source and body regions and
6[g]	said metal plug contacting a source metal disposed on top of said metal plug wherein said source metal layer composed of Ti/AlCu or Ti/AlSiCu alloys.

I. INTRODUCTION

Petitioner, Inergy Technology, Inc. ("Inergy" or "Petitioner"), respectfully requests institution of an *inter partes* review (IPR) and cancellation of claims 1-6 ("the Challenged Claims") of U.S. Patent No. 7,812,409 (the "'409 Patent") (Ex. 1001). The challenged claims generally relate to a trenched semiconductor device wherein the layout includes trenched gates surrounding transistor cells as closed cells with truncated or rounded corners. As detailed in this Petition, the claimed configurations were well-known in the relevant art prior to the '409 Patent.

II. MANDATORY NOTICES

A. Real Parties-in-Interest (37 C.F.R. § 42.8(b)(1))

Inergy Technology, Inc., Asustek Computer, Inc., and Panjit International Inc. are the real parties-in-interest.

B. Related Matters (37 C.F.R. § 42.8(b)(2))

The '409 Patent is currently the subject of litigation brought by Force Mos Technology Co., Ltd. ("Force Mos" or "Patent Owner") against Asustek Computer, Inc. in *Force Mos Technology, Co. Ltd. v. Asustek Computer, Inc.*, No. 2:22-cv-00460 (E.D. Tex.) (the "EDTX Force Mos Action"). The complaint and first amended complaint in the EDTX Force Mos Action are attached as Exs. 1009, 1010, respectively. The asserted patents in the EDTX Force Mos Action also include U.S. Patent Nos. 7,629,634 and 7,847,346. (*See* Ex. 1010 ¶¶ 49, 64, 73.) Force Mos Technology Co., Ltd. is also involved in another litigation in *Alpha and*

Omega Semiconductor Limited et al v. Force MOS Technology Co., Ltd., No. 4:22-cv-05448-HSG (N.D. Cal.) involving U.S. Patent Nos. 7,629,634; 7,847,346; and 7,646,058—but not the '409 Patent. Petitioner is not aware of any other pending judicial or administrative matter that would affect, or be affected by, a decision in this proceeding.

C. Lead and Back-Up Counsel (37 C.F.R. § 42.8(b)(3))

For purposes of this Petition, the following attorneys are lead and back-up counsel for Petitioner:

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D. Service Information (37 C.F.R. § 42.8(b)(4))

For purposes of this Petition, Petitioner consents to electronic service by email at: mackenzie.martin@bakermckenzie.com.

E. Payment of Fees (37 C.F.R. § 41.103)

Petitioner authorizes the United States Patent and Trademark Office (USPTO) to charge the fees set forth in 37 C.F.R. § 42.15(a) for this Petition, and any additional fees that might be due, to Deposit Account No. 13-0480 (Attorney Docket No. 10148110-51064583). This Petition meets the fee requirements of 35 U.S.C. § 312(a)(1).

III. REQUIREMENTS FOR IPR UNDER 37 C.F.R. § 42.104

A. Grounds for Standing (§ 42.104(a))

Petitioner certifies that the ’409 Patent is available for IPR and that Petitioner is not barred or estopped from requesting an IPR that challenges the claims of the ’409 Patent on the grounds identified in this Petition.

B. Identification of Challenge and Statement of Precise Relief Requested for Each of the Challenged Claims (§ 42.104(b))

Petitioner respectfully requests that IPR of the Challenged Claims (i.e., claims 1-6 of the ’409 Patent) be instituted and that each of the Challenged Claims be held unpatentable and canceled based on the following grounds:

No.	Claims	Ground	Reference(s)
1	1, 3-5	Pre-AIA 102	Unpatentable under pre-AIA 35 U.S.C. § 102(b) as anticipated by U.S. Patent No. 6,888,196 B2 to Kobayashi (“Kobayashi”)

2	2, 6	Pre-AIA 103	Unpatentable under pre-AIA 35 U.S.C. § 103 as obvious over Kobayashi in view of Kikkawa, T. et al, "A Quarter-Micrometer Interconnection Technology Using a TiN/Al-Si-Cu/TiN/Al-Si-Cu/TiN/Ti Multilayer Structure," IEEE Transactions on Electron Devices, Vol. 40, No. 2, February 1993 ("Kikkawa")
3	5	Pre-AIA 103	Unpatentable under pre-AIA 35 U.S.C. § 103 as obvious over Kobayashi in view of the knowledge of a person of skill in the art ("POSITA")
4	1, 3-5	Pre-AIA 103	Unpatentable under pre-AIA 35 U.S.C. § 103 as obvious over Kobayashi in view of U.S. Patent No. 5,763,914, Hshieh et al ("Hshieh")
5	2, 6	Pre-AIA 103	Unpatentable under pre-AIA 35 U.S.C. § 103 as obvious over Kobayashi in view of Kikkawa and Hshieh
6	5	Pre-AIA 103	Unpatentable under pre-AIA 35 U.S.C. § 103 as obvious over Kobayashi in view of Hshieh and the knowledge of a person of skill in the art ("POSITA")

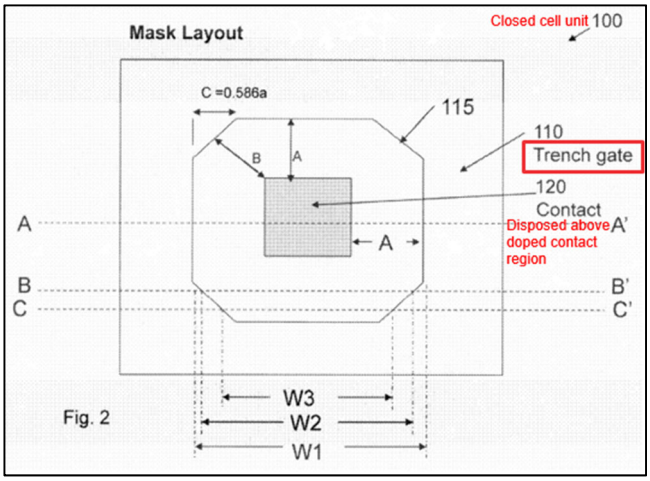
This Petition, supported by the declaration of Dr. David Liu (Ex. 1003), the prior art (Exs. 1005-1007), and other exhibits filed herewith, demonstrate that there is a reasonable likelihood that Petitioner will prevail with respect to one or more, if not all, of the Challenged Claims. *See* 35 U.S.C. § 314(a).

IV. THE '409 PATENT

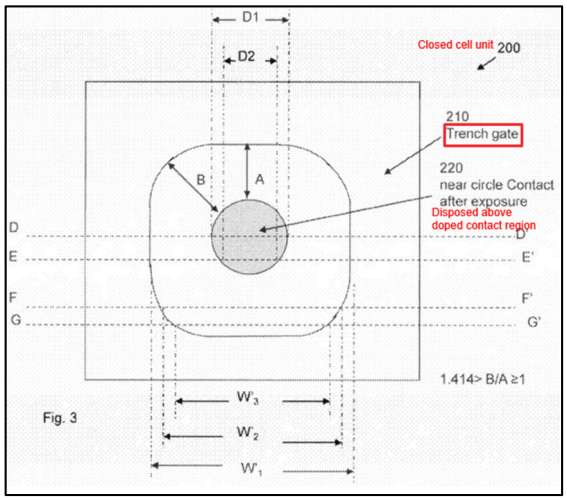
A. The '409 Patent

The '409 Patent is generally directed to a trenched semiconductor power device. Ex. 1001, 1:7—13. The '409 Patent admits that, at the time of filing, trenched semiconductor power devices already existed in products and disclosures. *Id.*, 1:14—17.

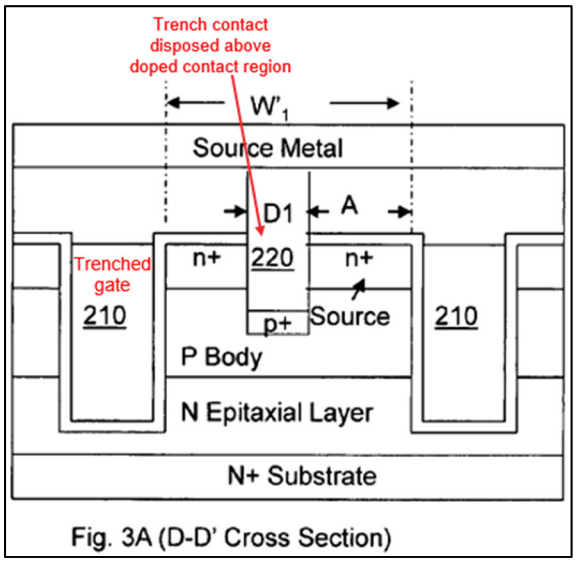
The trenched semiconductor power device described in the ’409 Patent has a main body component—i.e., a “closed cell unit” 200/100 of a MOSFET device including trenched gate 210/110 surrounding a metal contact 220/120 disposed above a doped contact region, as shown below in (annotated) Figures 2-3 and 3A of the ’409 Patent. *Id.*, 4:4—7.



’409 Patent, Figure 2 (annotated)



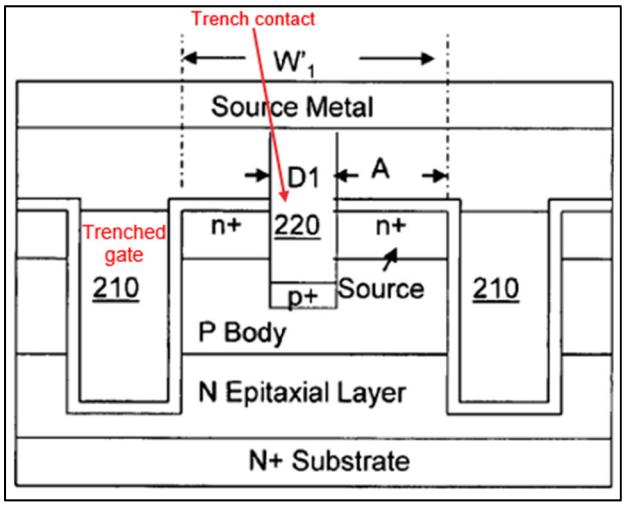
’409 Patent, Figure 3 (annotated)



’409 Patent, Figure 3A (annotated)

The closed cells are designed to have substantially square-shaped cells with truncated corners as shown in Figure 2. *Id.*, 4:57—62. "The truncated corners are formed by design layout not process." *Id.*, 4:57—62, Fig. 2 (showing the mask layout). Then, the truncated corners (as shown in the mask layout of Figure 2) naturally become rounded during exposure during lithography. *Id.* ("It is by nature that [the] truncated corners in [the] layout as that shown in FIG. 2 . . . [become] rounded as shown in FIG. 3."). Similarly, the square contact 120, as shown in the mask layout in Figure 2, naturally becomes a circular shaped contact 220, as shown in Figure 3, during exposure. *Id.*, 4:53—57.

As shown in Figure 3A (annotated below), the circular trench contact 220 is "extended into the body region through the source region of the closed semiconductor power cell [and is] in contact with a p+ contact dopant region disposed immediately below the trench contact [220]." *Id.*, 4:27—33, Fig. 3A.



'409 Patent, Figure 3A (annotated)

Accordingly, the sidewalls of the trench source-body contact 220 are in contact with the source and body regions. *Id.*, 4:27—33, Fig. 3A. Furthermore, the circular trench contact 220 is disposed a distance away from a gate oxide lining of said trench gate from all circumferential points of the circular trench contact with the source and body regions disposed between the gate oxide lining and all circumferential points of the circular trench contact. *Id.*, 4:27—33, Figs. 3, 3A.

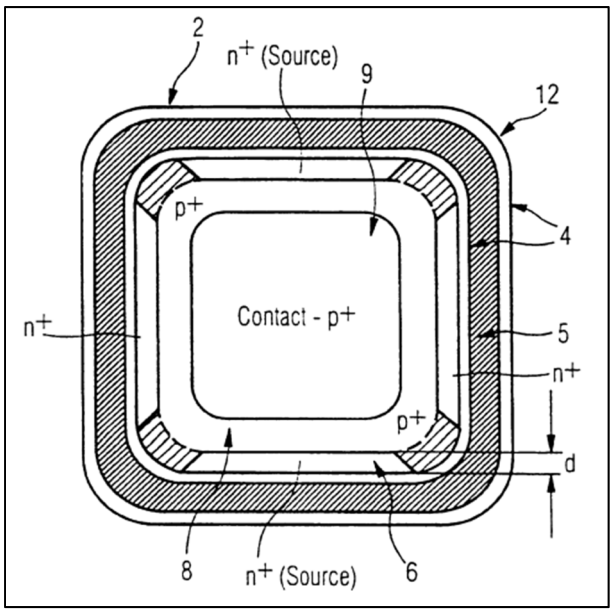
The circular trench contact 220 is filled with a contact metal plug connected to the source metal. *Id.*, Figure 3A; 5:26—27; *see also id.* Fig. 1C.

B. The '409 Patent File History

U.S. Patent Application No. 11/633,366 (the "'366 Application"), titled "TRENCH MOSFET WITH CELL LAYOUT, RUGGEDNESS, TRUNCATED CORNERS," was filed on December 4, 2006, and issued as the '409 Patent on October 12, 2010. Ex. 1001 at 1; Ex. 1002 at p. 350. The '366 Application was filed with 18 original claims and listed Fu-Yuan Hshieh as the inventor. Ex. 1001 at 1; Ex. 1002 at p. 350. In response to an Examiner's Action mailed October 6, 2008 for Election and Restriction, the Applicant withdrew claims 14-18 relating to methods for making semiconductor devices. Ex. 1002 at p. 331.

The application received a first office action dated January 26, 2009, rejecting all pending claims on the basis of anticipation and obviousness. *Id.* at 309. On April 15, 2009, the Applicant amended the pending claims to include (1)

a square shaped closed cell with rounded corners in amended claim 1 and with truncated corners in amended claim 13 (now claim 6); and (2) a circular trench contact hole disposed in the center of the closed cells. *Id.* at p. 302. This amendment was made to overcome the Pfirsh reference (U.S. Patent No. 6,541,818), which Applicant admitted disclosed "a closed cell with square trench gate with rounded corner [2] and square contact with rounded corner [9] . . . ." *Id.* at p. 302 (emphasis added). The Pfirsh top view is provided below for reference.



Pfirsh Fig. 2

The application received a second and final office action dated July 15, 2009, rejecting all pending claims on the basis of indefiniteness and obviousness. *Id.* at 275. On October 14, 2009, the Applicant submitted a Request for Continued Examination and amended the pending claims to include a circular trench contact disposed at a distance away from a gate oxide lining of a trench gate from all

circumferential points of the circular trench contact in claim 1 and claim 13 (now claim 6). *Id.* at 253. This amendment was made to overcome the Pfirsh reference (U.S. Patent Pub. No. 2022/0006703) in view of the Iman reference (U.S. Patent No. 6,867,083).

The application received a third and final office action dated January 10, 2010, rejecting all pending claims on the basis of obviousness. *Id.* at 237. On April 2, 2010, the Applicant amended the pending claims to include (1) a circular trench contact comprising a hole opened from a top surface of a semiconductor surface, sidewalls surrounded by and in contact source and body regions, and source and body regions disposed between the hole and trenched gates in amended claim 1; and (2) a contact resistance reduction metal layer disposed above a contact metal plug and below a bottom surface of a source metal in claim 5 (now claim 2). *Id.* at 222. This amendment was made to overcome the Pfirsh reference (U.S. Patent Pub. No. 2022/0006703) in view of the Blanchard reference (U.S. Patent No. 6,621,107). *Id.* at 227. On August 5, 2010, the examiner issued a Notice of Allowance and Fees Due, and the ’409 Patent issued on October 12, 2010. *Id.* at p. 207.

On October 12, 2018, the ’409 Patent expired due to non-payment of maintenance fee. *Id.* at 197. Four years later, on July 12, 2022, the Applicant submitted a Petition for Acceptance of Delayed Payment of Maintenance Fees. *Id.*

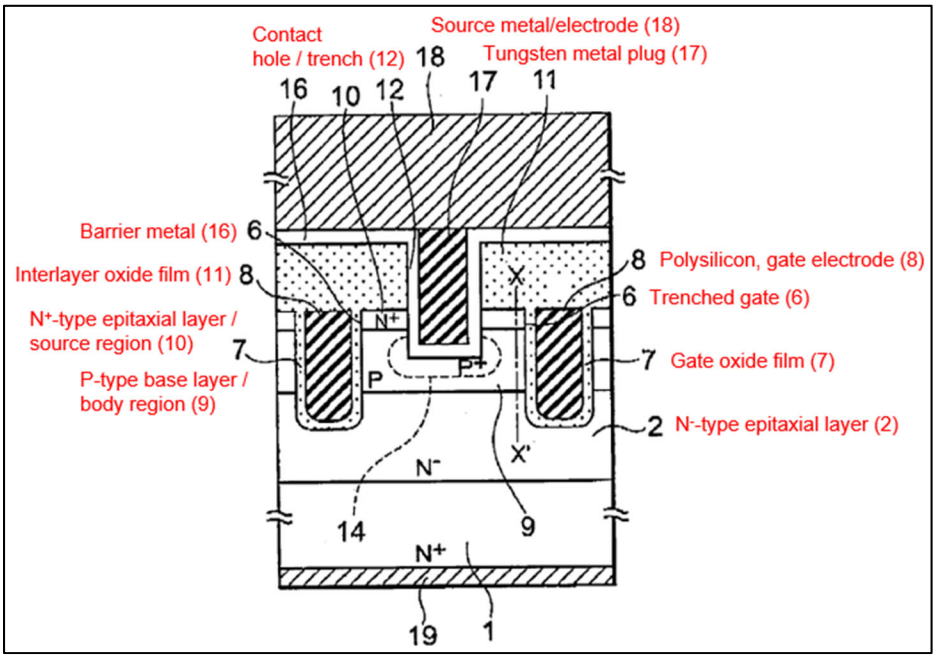
at 180. Applicant had failed to pay the 7.5 year maintenance fee which the last day to pay was October 12, 2018. *Id.* at 197. This petition was dismissed on October 12, 2022 for failure to meet the petition requirements. *Id.* at 168. On October 28, 2022, the Applicant submitted a second Petition for Acceptance of Delayed Payment of Maintenance Fees. *Id.* at 121. This petition was also dismissed on December 14, 2022 for failure to meet the petition requirements as well as non-payment of the 11.5 Year maintenance fee which was due no later than October 12, 2022. *Id.* at 109. On February 14, 2023, the Applicant submitted a third Petition for Acceptance of Delayed Payment of Maintenance Fees. *Id.* at 94. This petition was also dismissed on March 17, 2023 for failure to meet the petition requirements as well as non-payment of the 11.5 Year maintenance fee which was due no later than October 12, 2022. *Id.* at 23. On February 14, 2023, the Applicant submitted a fourth Petition for Acceptance of Delayed Payment of Maintenance Fees. *Id.* at 6. This petition was granted on May 24, 2023.

V. OVERVIEW OF THE PRIOR ART

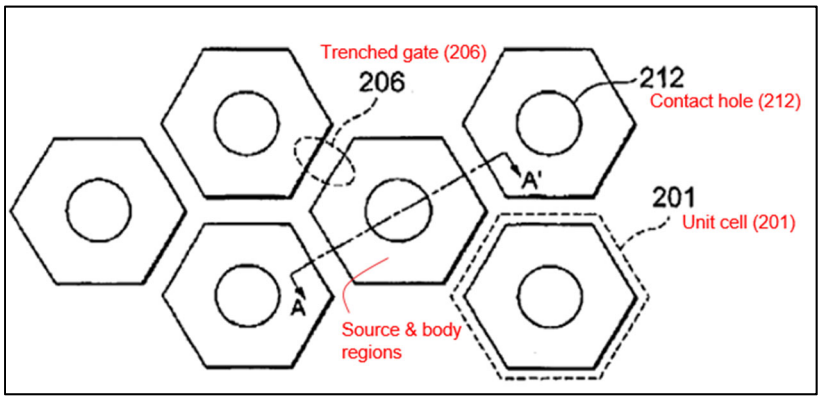
A. U.S. Patent No. 6,888,196 ("Kobayashi")

U.S. Patent No. 6,888,196 to Kobayashi ("Kobayashi") issued on May 3, 2005. Ex. 1005. Kobayashi is prior art at least under pre-AIA 35 U.S.C. § 102(b). Kobayashi was not considered during the prosecution of the '409 Patent.

Kobayashi Figure 3 (annotated) and Figure 4A (annotated) are included below for reference.



Kobayashi, Figure 3 (Annotated)

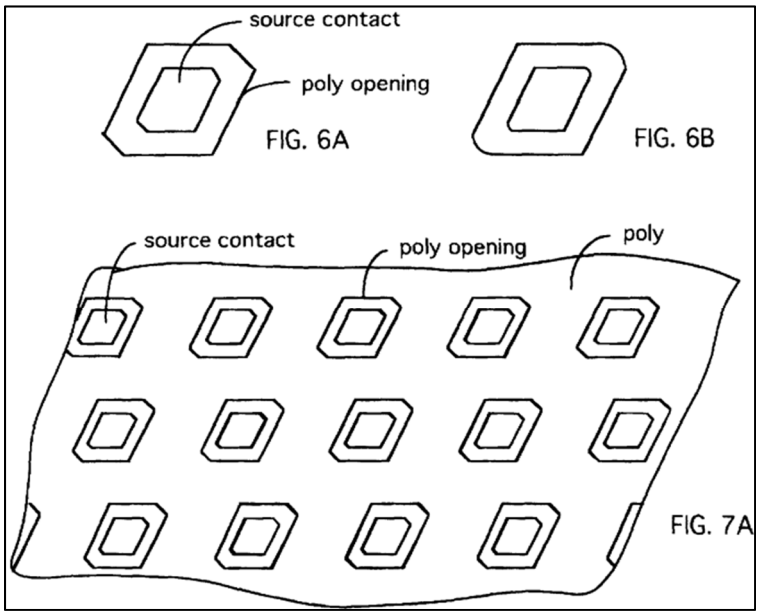


Kobayashi Fig. 4A (annotated)

Like the '409 Patent, Kobayashi discloses a trenched semiconductor power device. *Id.*

B. U.S. Patent No. 5,763,914 ("Hshieh")

U.S. Patent No. 5,763,914 to Hshieh et al. ("Hshieh") was issued on June 9, 1998. Ex. 1006. Hshieh is prior art at least under pre-AIA 35 U.S.C. § 102(b). Hshieh was not considered during the prosecution of the '409 Patent. Hshieh Figures 6A, 6B, and 7A are included below for reference.



Hshieh, Figures 6A, 6B, 7A

Like the '409 Patent, Hshieh discloses trenched semiconductor power devices. Ex. 1006.

C. Kikkawa

"A Quarter-Micrometer Interconnection Technology Using a TiN/Al-Si-Cu/TiN/Al-Si-Cu/TiN/Ti Multilayer Structure," by Kikkawa, T. et al, IEEE Transactions on Electron Devices, Vol. 40, No. 2 ("Kikkawa") was published and made publicly available in or around January-February 1993. Ex. 1007; Ex. 1008. Specifically, on its face, Kikkawa is part of "IEEE TRANSACTIONS ON

ELECTRON DEVICES," which is "A PUBLICATION OF THE IEEE ELECTRON DEVICES SOCIETY." Ex. 1007 at 1. The "IEEE TRANSACTIONS ON ELECTRON DEVICES is published monthly by the Institute of Electrical and Electronics Engineers, Inc." Ex. 1007 at 2. The date on the face of the publication is "February 1993" and the copyright is also 1993. Ex. 1007 at 1-2. *See Hulu v. Sound View Innovations, LLC*, IPR2018-01039, Paper 29 at 9 (PTAB Dec. 20, 2019) (precedential). In addition, expert testimony establishes that Kikkawa had been received, indexed, and cataloged by subject matter in multiple ways around or shortly after January 26, 2023. Ex. 1008; *see also Samsung Elecs. Co. v. Infobridge Pte. Ltd.*, 929 F.3d 1363, 1369 (Fed. Cir. 2019). Therefore, Kikkawa is prior art under at least pre-AIA 35 U.S.C. § 102(b). Kikkawa was not considered during the prosecution of the '409 Patent.

Like the '409 Patent, Kikkawa describes structures for semiconductor devices. *Id.*

VI. LEVEL OF ORDINARY SKILL IN THE ART

Petitioner submits that a person of ordinary skill in the art ("POSITA") of the subject matter of the '409 Patent at the filing date of the '409 Patent would have a master's degree in electrical engineering, and at least two years of relevant work experience in the field of integrated circuit design and manufacturing. Ex. 1003 ¶ 52.

VII. CONSTRUCTION OF THE CLAIMS

In *inter partes* review proceedings, a claim of a patent is "construed using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. § 282(b)." 37 C.F.R. § 42.100(b). Claim terms are generally given their "ordinary and customary meaning that the term would have to a person of ordinary skill in the art." *Duncan Parking Techs., Inc. v. IPS Grp., Inc.*, 914 F.3d 1347, 1364 (Fed. Cir. 2019).[1] Because the meaning of a claim term as understood by a POSITA is often not immediately apparent, and because patentees frequently use terms idiosyncratically, the court looks to "those sources available to the public that show what a person of skill in the art would have understood disputed claim language to mean." *Phillips v. AWH Corp.*, 415 F.3d 1303, 1314 (Fed. Cir. 2005) (en banc). Those sources include the "intrinsic evidence of record, i.e., the patent itself, including the claims, the specification and, if in evidence, the prosecution history." *Vitronics Corp. v. Conceptronic*, 90 F.3d 1576, 1582 (Fed. Cir. 1996).

Specifically, "the specification may reveal an intentional disclaimer, or disavowal, of claim scope by the inventor. In that instance as well, the inventor

[1]A person of ordinary skill in the art is a hypothetical person who is presumed to have known the art "before the effective filing date of the claimed invention." 35 U.S.C. § 103. This person is considered one "of ordinary creativity, not an automaton." *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 420 (2007).

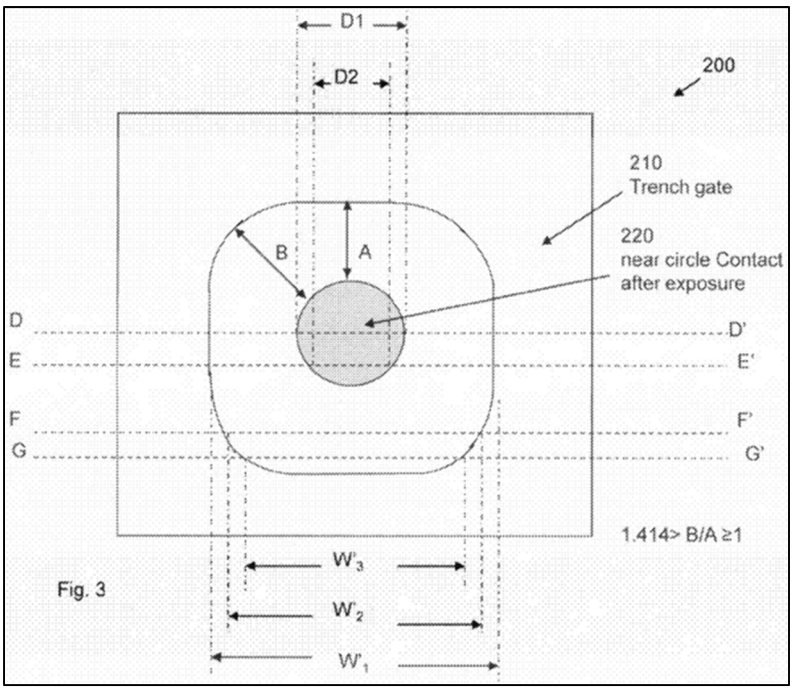
has dictated the correct claim scope, and the inventor's intention, as expressed in the specification, is regarded as dispositive." *Phillips*, 415 F.3d at 1316 (citing *SciMed Life Sys., Inc. v. Advanced Cardiovascular Sys., Inc.*, 242 F.3d 1337, 1343-44 (Fed. Cir. 2001)). If the specification discusses prior art, "[c]laims cannot be construed as encompassing the prior art that was distinguished in the specification . . . ." *Kinik Co. v. ITC*, 362 F.3d 1359, 1365 (Fed. Cir. 2004) (citing *SciMed*, 242 F.3d at 1343-44); *see Akeva LLC v. Nike, Inc.*, 817 Fed. Appx. 1005, 1009-1010 (Fed. Cir. 2020) (finding the patentee had disclaimed the embodiment of the prior art disclosed in the specification "given the patent's disparagement of conventional fixed rear sole shoes" and the patent's following characterization of the invention as removable or rotatable sole shoes).

Additionally, for *inter partes* review, claims are construed only to the extent necessary to resolve an underlying controversy. *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co. Ltd.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (internal citations omitted).

A. "Rounded corners" (claim 1)

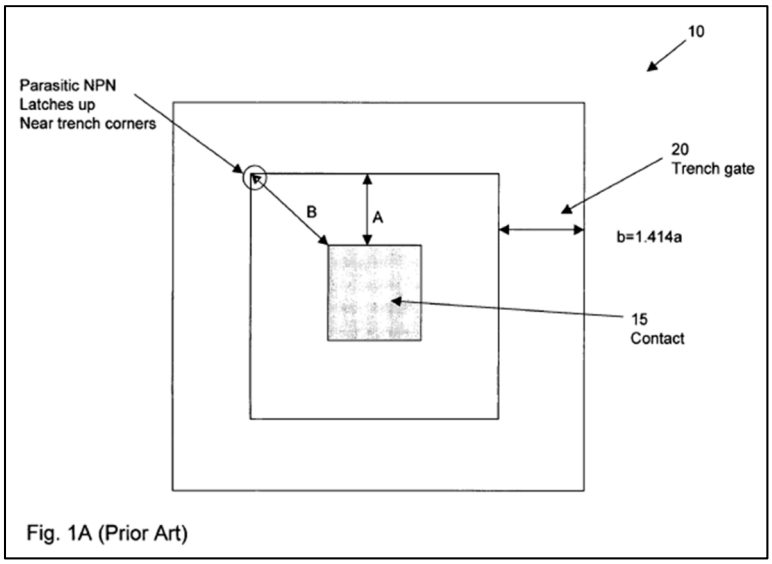
The term "rounded corners" should be construed as "corners that are truncated by design layout and then rounded." This construction is supported by the specification and file history of the '409 Patent. Ex. 1003 ¶ 55. In particular, the '409 Patent only describes rounded corners in one context—with respect to

Figure 3 (shown below). Ex. 1001, 2:10-20; 4:53-64. In addition, during prosecution of the ’409 Patent, the Applicant characterized the “rounded corners in the amended claim 1” as “structural features . . . shown in Fig. 3” of the ’409 Patent. Ex. 1002 at 302. As described in the ’409 Patent, in order to form the “rounded corners” in Figure 3, *truncated corners are first formed by design layout*. Ex. 1001, 2:10-20; 4:53-64. Then, the *truncated corners become rounded* after exposure during photolithography. *Id*.



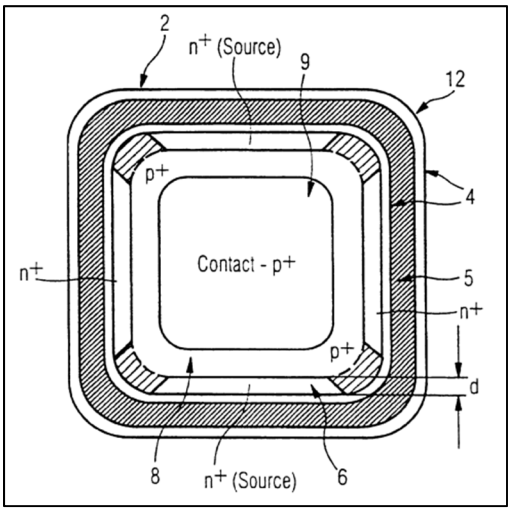
<u>’409 Patent Figure 3</u>

The ’409 Patent also admits that its Figure 1A (shown below) is prior art. Figure 1A is a mask layout of a trench gate that is designed to be square shaped. It is well known in the art that corners become somewhat rounded as a natural/incidental result of lithography. Ex. 1003 ¶ 56.



<u>'409 Patent Figure 1A (Admitted Prior Art)</u>

Further, during prosecution, the Applicant amended claim 1 (which is also the current claim 1) by adding the "rounded corners" to distinguish the closed cells of the Pfisrch reference, shown below. Specifically, Applicant distinguished claim 1 from Pfirsch "which has a closed cell with ***square trench gate with rounded corner*** . . . as shown in Fig. 2 . . . in Pfirsch." Ex. 1002 at 302 (emphasis added).

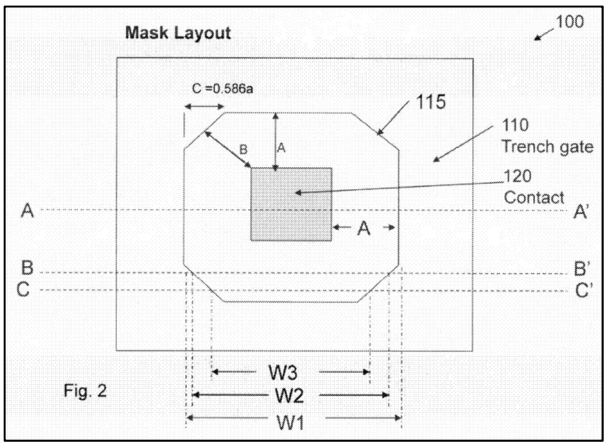


<u>Pfirsh Fig. 2</u>

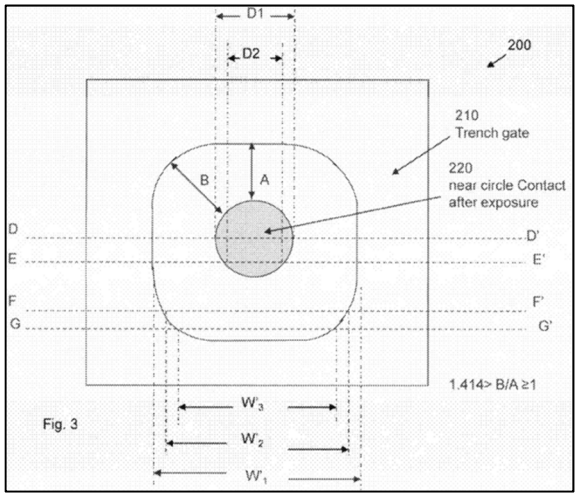
Accordingly, the "rounded corners" in claim 1 of the '409 Patent cannot mean a naturally or incidentally rounded corner of a trench gate that was designed to be square. Instead, the term "rounded corners" refers to the truncated and subsequently rounded design of Figure 3. As a result, the "rounded corners" of claim 1 should be construed as "corners that are truncated by design layout and then rounded." *See Kinik*, 362 F.3d at 1365; *SciMed*, 242 F.3d at 1341.

B. "Truncated corners" (claim 13)

The term "truncated corners" should be construed as "corners that are truncated by design layout." This construction is supported by the specification and file history of the '409 Patent. Ex. 1003 ¶ 59. In particular, the '409 Patent only describes truncated corners with respect to Figures 2 and 3 (shown below).



'409 Patent, Figure 2



'409 Patent, Figure 3

Ex. 1001, 2:10-20; 4:53-64. In addition, during prosecution of the '409 Patent, the Applicant characterized the "truncated corners in the amended claim 13" as "structural features . . . shown in Fig. 3" of the '409 Patent. Ex. 1002 at 302. As described in the '409 Patent, in order to form the rounded corners in Figure 3, truncated corners are first formed by the mask design layout of Figure 2. Ex. 1001, 2:10-20; 4:53-64. "The truncated corners are formed by design layout not process." Ex. 1001, 4:57-58.

As discussed above, the admitted prior art and prior art that was distinguished by Applicant during prosecution include trench gates that are designed to be square and become rounded or changed during the lithography process. Accordingly, "truncated corners" in the '409 Patent cannot refer to corners of a square layout that are incidentally or naturally altered or truncated. Instead, "truncated corners" refers to the truncated design described in relation to Figures 2-3. As a result, the "truncated corners" of claim 13 should be construed as "corners that are truncated by design layout." *See Kinik*, 362 F.3d at 1365; *SciMed*, 242 F.3d at 1341.

VIII. CLAIM-BY-CLAIM EXPLANATION OF GROUNDS FOR UNPATENTABILITY

Pre-AIA Section 102 of the United States patent law provides that "[a] person shall be entitled to a patent unless —

…

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of the application for patent in the United States," 35 U.S.C. § 102(b) (Pre-AIA). A claim is anticipated if "a prior art reference [] disclose[s] each and every element of the claim, either explicitly or inherently." *ADASA Inc. v. Avery Dennison Corp.*, 55 F.4th 900, 910 (Fed. Cir. 2022) (citing *Eli Lilly & Co. v. Zenith Goldline Pharms., Inc.*, 471 F.3d 1369, 1375 (Fed. Cir. 2006)). While the disclosed claim elements must be "arranged or combined in the same way as the claim," the reference need not used the same terms to describe these claims. *In re Gleave*, 560 F.3d 1331, 1334 (Fed. Cir. 2009) (internal citations omitted).

Pre-AIA Section 103 provides that "if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art." 35 U.S.C. § 103(a) (Pre-AIA). The Supreme Court's decision in *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398 (2007) sets forth the standard for determining obviousness under 35 U.S.C. § 103, which is based on an analysis of several factual inquiries as set forth in *Graham v. John Deere Co. of Kansas City*, 383 U.S. 1, 17-18 (1966): (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) when available, evidence such as

commercial success, long-felt but unsolved needs, and failure of others. *KSR Int'l*, 550 U.S. at 407, 419.

The Court emphasized that an "expansive and flexible approach" should be used when determining obviousness. *KSR Int'l*, 550 U.S. at 415. The Court identified several rationales and principles, including the following: (1) if a work is available in one field of endeavor, and design incentives and other market forces can prompt variations of it (either in the same field or a different one), and a person of ordinary skill can implement a predictable variation, the variation is obvious; (2) if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its application is beyond his or her skill; (3) the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results; (4) if the improvement is nothing more than the predictable use of prior art elements according to their established functions, it is likely obvious, among others. *Id*. at 416–17. "Often, it will be necessary for a court to look to interrelated teachings of multiple patents; the effects of demands known to the design community or present in the marketplace; and the background knowledge possessed by a person having ordinary skill in the art, all in order to determine whether there was an apparent

reason to combine the known elements in the fashion claimed by the patent at issue." *Id.* at 418.

A. <u>Ground 1: Claims 1, 3–5 are unpatentable under pre-AIA 35 U.S.C. § 102(b) as anticipated by Kobayashi</u>.

Claims 1–6 of the '409 Patent are unpatentable under pre-AIA 35 U.S.C. § 102(b) as anticipated by Kobayashi. The following discussion is fully supported by the Declaration of Dr. David Liu. Ex. 1003 ¶¶ 62—82.

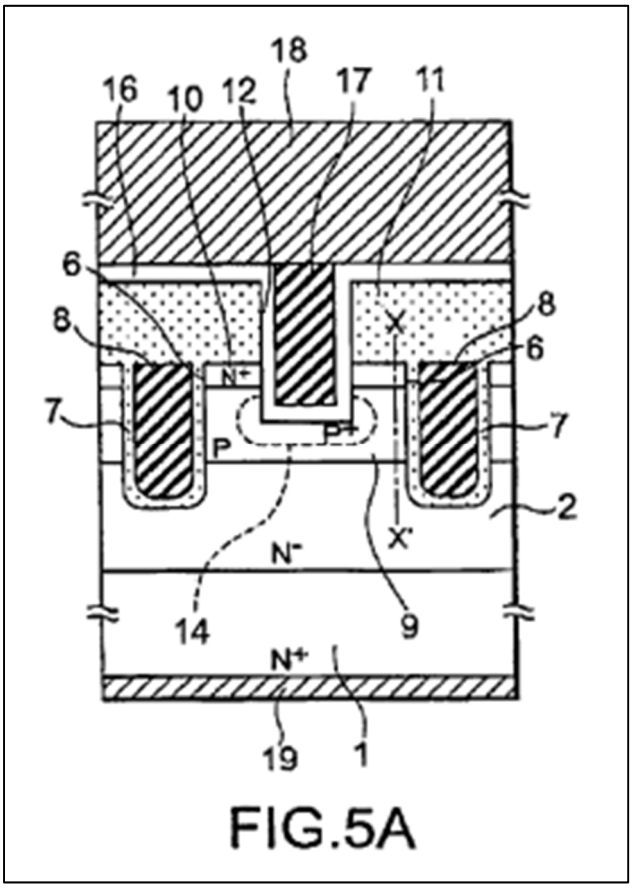
1. Claim 1

Kobayashi discloses and anticipates every limitation of claim 1.

a. 1 [preamble]: "A trenched semiconductor power device comprising a plurality of trenched gates surrounding a plurality of transistor cells formed in a semiconductor substrate, wherein:"

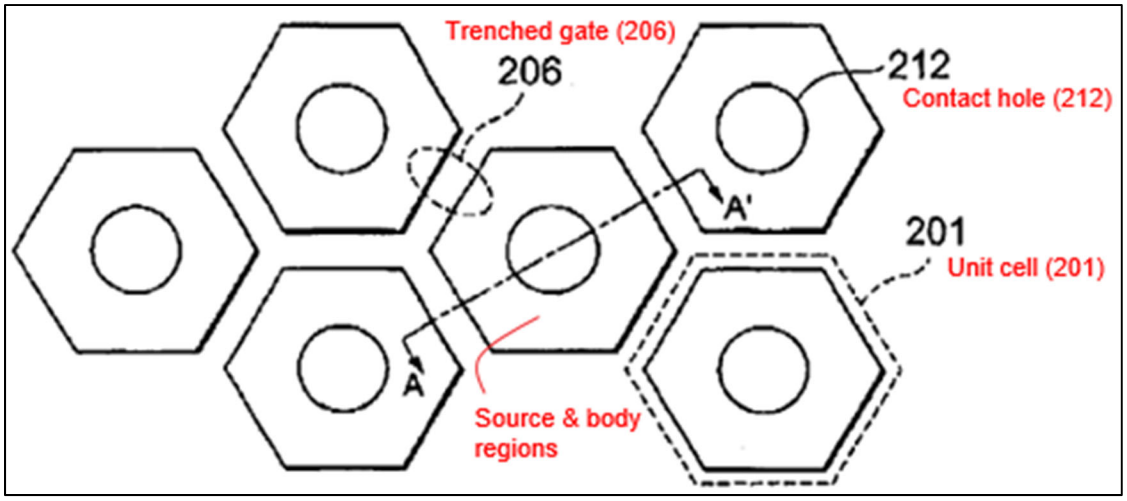
To the extent the preamble is limiting, it is disclosed in Kobayashi, which discloses a trenched semiconductor power device comprising a plurality of trenched gates surrounding a plurality of transistor cells formed in a semiconductor substrate. For example, Kobayashi discloses "[a] vertical MOSFET (or a UMOSFET) comprising: a semiconductor layer (1, 2, 9, 10) having first and second surfaces opposite to each other and a pair of trenches (6) formed on the first surface . . . ." Ex. 1005, 4:12—15, Fig. 5A (depicting a unit cell). Kobayashi also describes trenched gates ("trench gates (8) formed in the pair of trenches") surrounding the transistor cells formed in a semiconductor substrate ("a unit cell

formed in a region of the semiconductor layer surrounded by the pair of trench gates"). *Id.*, 4:12—19.



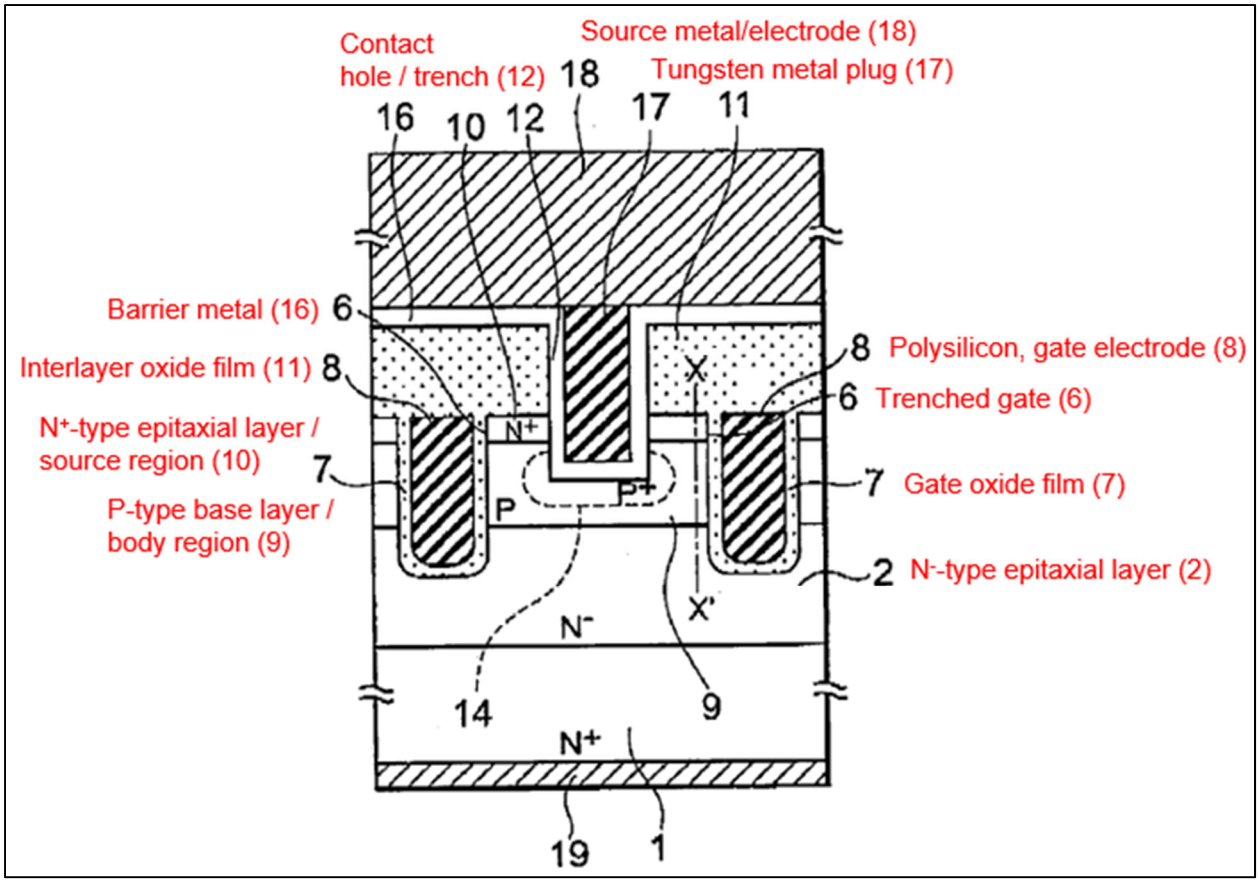
Kobayashi Figure 5A

As shown in Kobayashi's Figure 4A (depicted below with color annotations), a plurality of unit cells separated by a plurality of trenches are disclosed. Specifically, the "unit cells [201] in each figure can be defined as structural units separated by trenches [206] where gate electrodes are to be formed. At the centers of the unit cells [201] contact holes [212] are disposed, respectively." *Id.*, 6:29—37.



Kobayashi, Figure 4A (annotated)

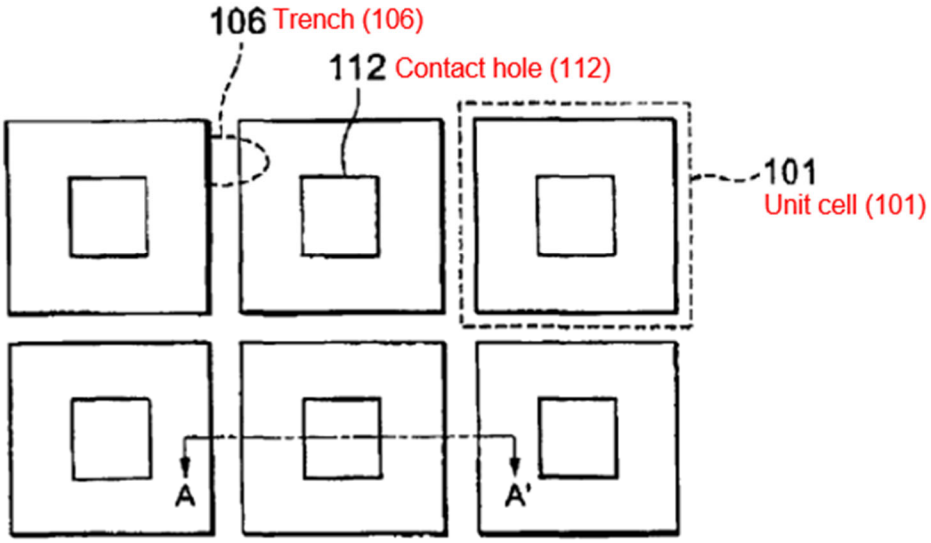
Referring back to the unit cell of Figure 5A (depicted below with color annotations), "[a] combination of the substrate 1 and the layers 2, 9, and 10 constitutes a silicon layer having silicon surface opposite to each other. In each of trenches 6 reaching the N^--type epitaxial layer 2 through the P-type base layer 9, a gate oxide film 7 and a polysilicon 8 are filled." *Id.*, 6:51—56.



Kobayashi, Figure 5A (annotated)

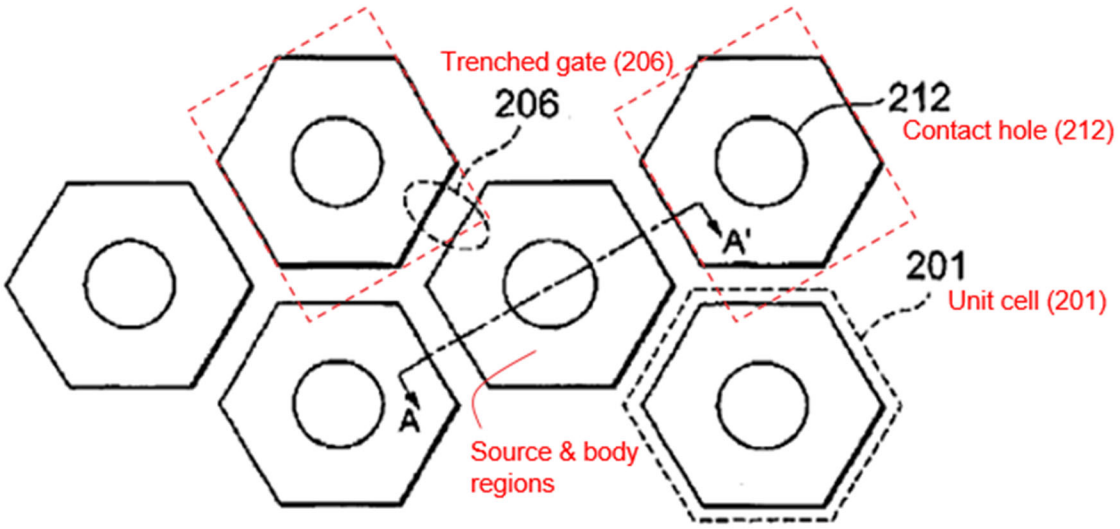
b. 1[a]: "said trenched gates surrounding said transistor cells as closed cells constituting substantially square-shaped cells with rounded corners;"

Element 1[a] is disclosed by Kobayashi. As depicted below in Kobayashi's Figure 3A (annotated), "a plurality of ***square cells*** are arranged in a matrix." Ex. 1005, 6:26—27 (emphasis added).



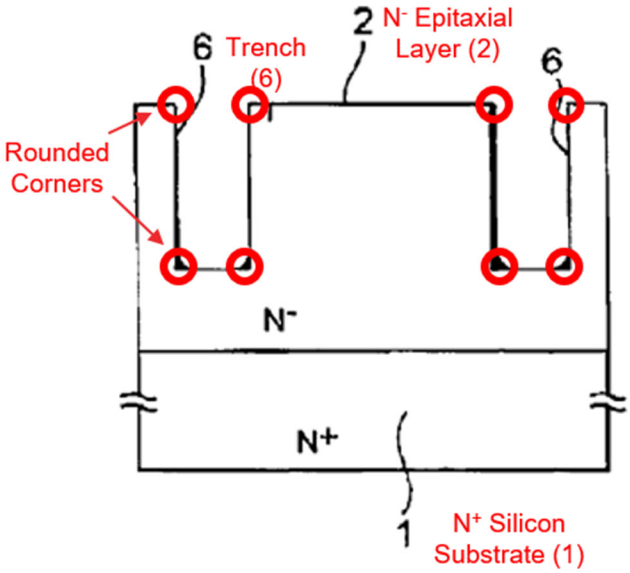
Kobayashi, Figure 3A (annotated)

Furthermore, as shown below in Kobayashi's Figure 4A (annotated), Kobayashi discloses "a plurality of hexagonal cells"—i.e., substantially square cells with truncated corners. Ex. 1005, 6:30; Ex. 1003 ¶ 68.



Kobayashi, Figure 4A (annotated)

Kobayashi's Figure 6C further discloses that the MOSFETs disclosed are made with a process where the "corners of each trench 6 at the bottom are rounded [and] corners of each trench 6 at an opening portion may also be rounded." Ex. 1005, 7:57—8:4; Ex. 1003 ¶ 69.



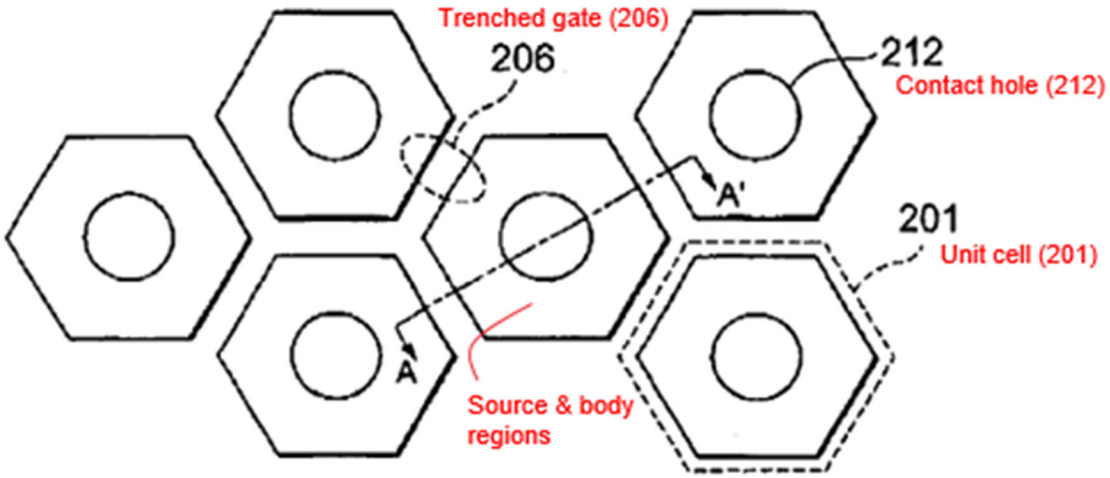
Kobayashi, Figure 6C (annotated)

Accordingly, Kobayashi discloses closed cells that are substantially square shaped with corners that are truncated by design layout and then rounded. Ex. 1003 ¶ 70.

c. 1[b]: "each of said closed cells further includes a circular trench contact disposed substantially in a central portion of said closed cells, penetrating through a source region surrounding said trenched gates and extending into a body region encompassing said source region;"

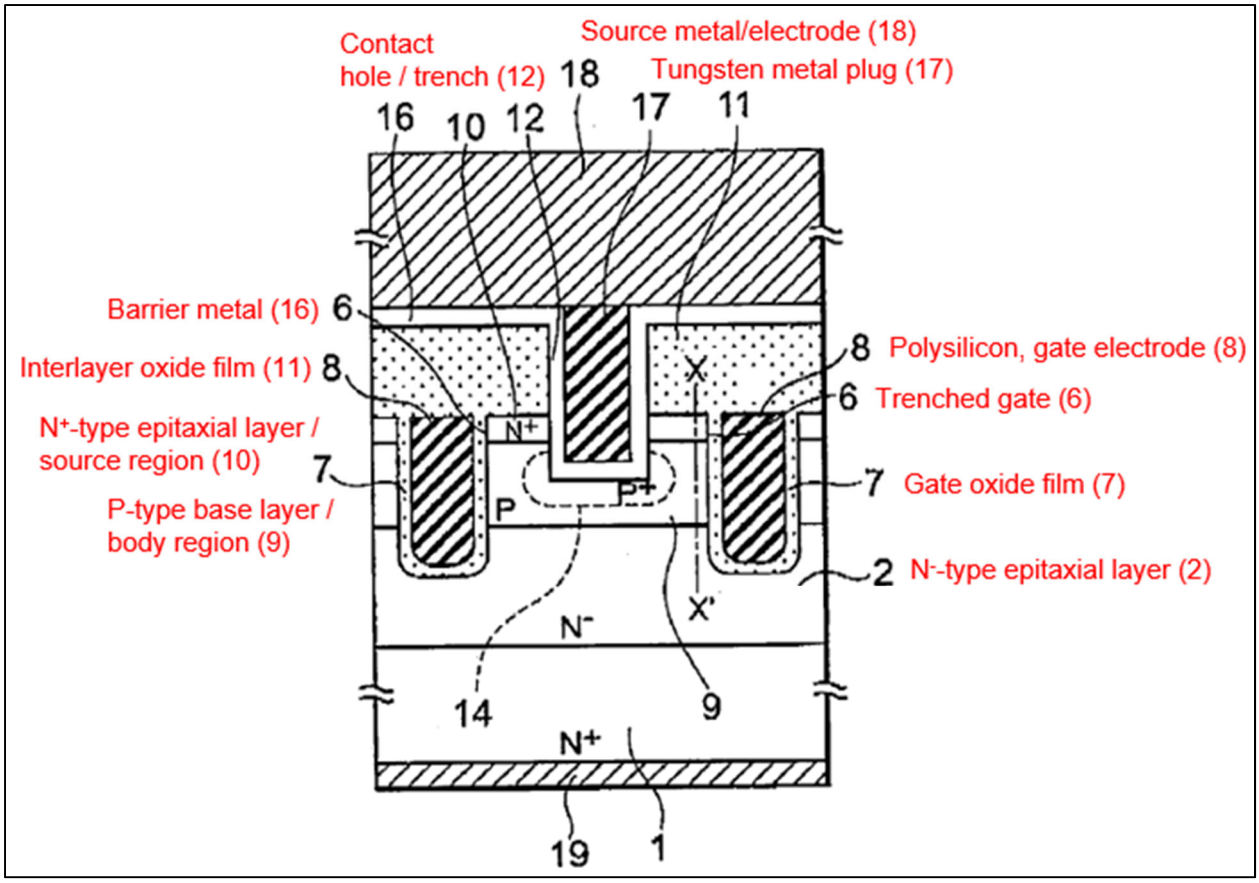
Element 1[b] is disclosed in Kobayashi. As described in Kobayashi, each closed cell includes a circular trench contact 212. Ex. 1005, 6:29—39. As shown

below in Kobayashi's Figure 4A (annotated), the circular trench contact 212 is disposed substantially in a central portion of the closed cell 201.



Kobayashi, Figure 4A (annotated)

Further, as described in Kobayashi, a trench contact 12 "is formed to reach the P-type base layer 9 through the N^+-type source layer 10." Ex. 1005, 6:58—60. As shown below in Figure 5A (annotated), the circular trench contact 12 penetrates through a source region 10 surrounding trenched gates 6. Ex. 1005, 6:46—67.



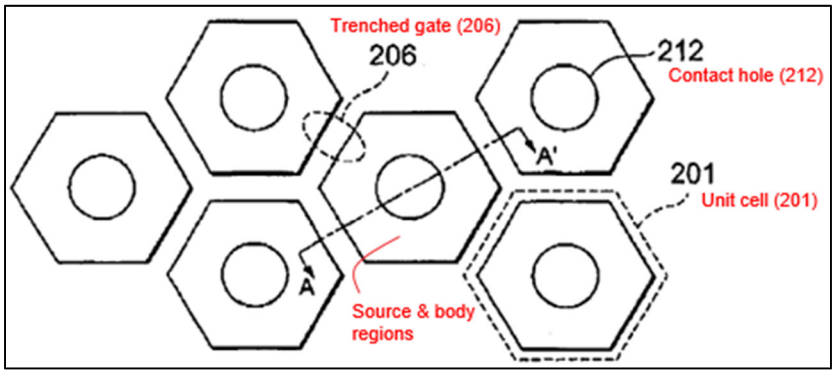
Kobayashi, Figure 5A (annotated)

Moreover, the trench contact 12 extends into a P-type base layer 9—i.e., body region. Ex. 1005, Fig. 5A. Finally, the P-type base layer 9 (body region), encompasses the source region 10. *Id.*, 6:46—67, Fig. 5A.

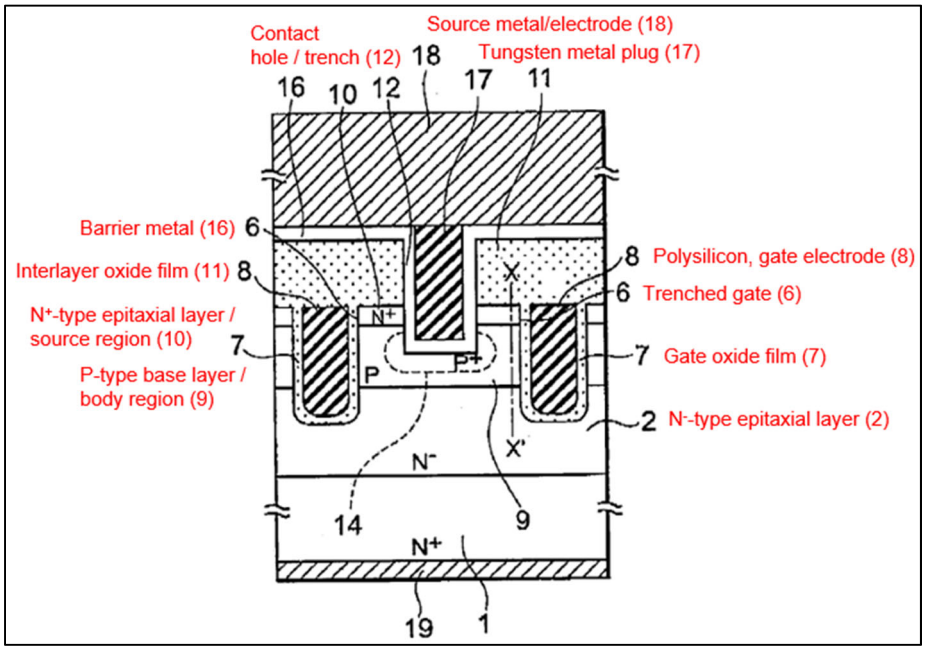
d. 1[c]: "said circular trench contact comprises a hole opened from a top surface of said semiconductor substrate and is filled with a contact metal plug"

Element 1[c] is disclosed in Kobayashi. As shown below in Kobayashi's Figures 4A and 5A (annotated), the circular trench contact is "a contact hole 12 having a predetermined length formed to reach the P-type base layer 9 through the N^+-type source layer 10" from a top surface. *Id.*, 6:58-60. Furthermore, as

described in Kobayashi, the contact hole 12 is filled with a contact metal plug, tungsten 17. Ex. 1005, 6:61-67, Fig. 5A.



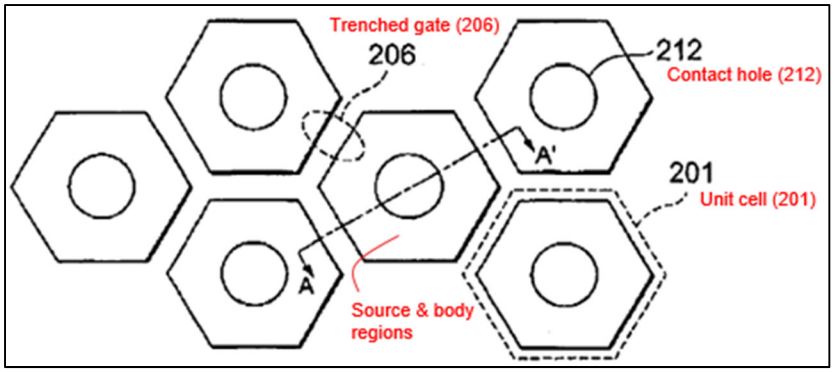
Kobayashi, Figure 4A (annotated)



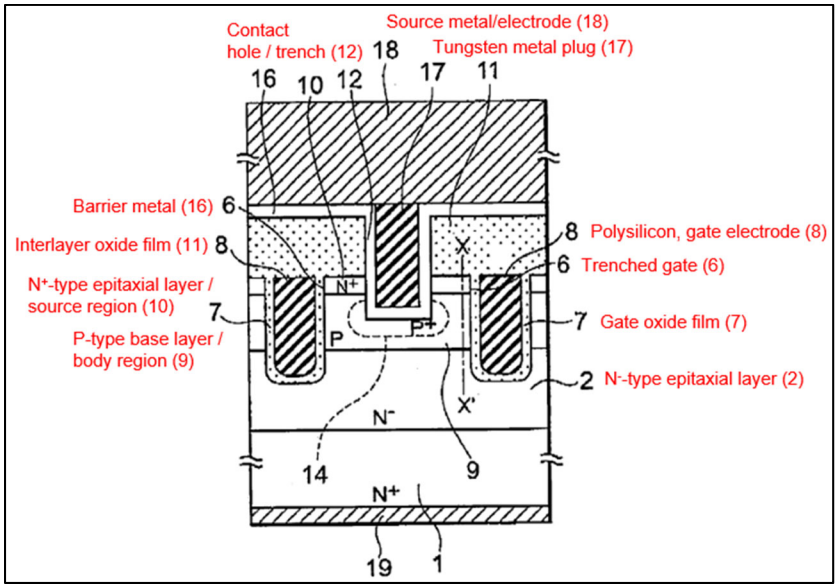
Kobayashi, Figure 5A (annotated)

e. 1[d]: "wherein sidewalls of said hole are surrounded by and in contact said source and body regions"

Element 1[d] is disclosed in Kobayashi. As shown below in Kobayashi's Figures 4A and 5A (annotated), the sidewalls of contact hole 12 are surrounded by and in contact with the source 10 and body 9 regions.



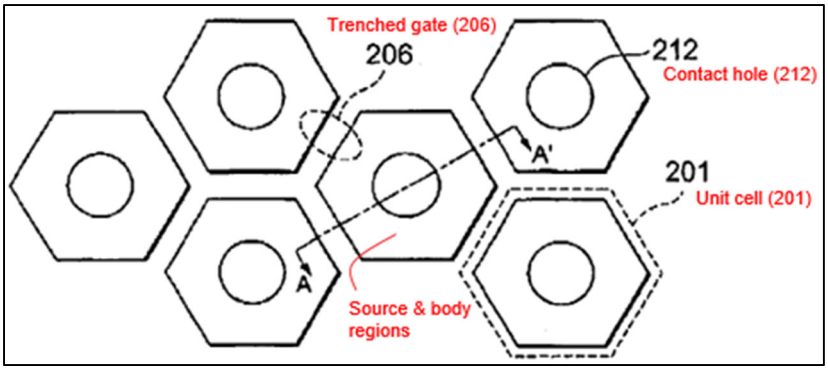
Kobayashi, Figure 4A (annotated)



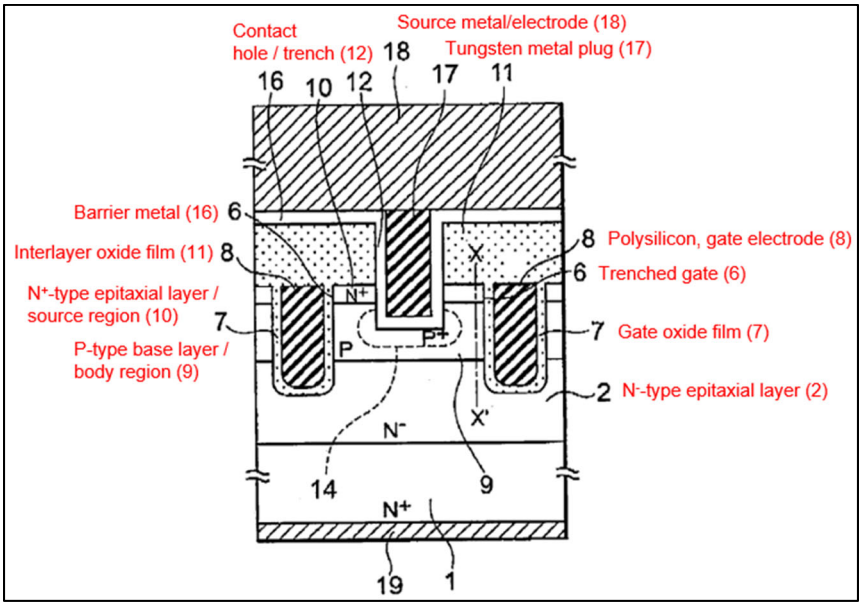
Kobayashi, Figure 5A (annotated)

f. 1[e]: "and said circular trench contact is separate from said trenched gates with said source region and body region disposed between a gate oxide lining of said trenched gates and all circumferential points of the circular trench contact;"

Element 1[e] is disclosed in Kobayashi. As shown below in Kobayashi's Figures 4A and 5A (annotated), the contact hole 12 is separate from trenched gates 6 with source 10 and body 9 regions disposed between a gate oxide film 7 of said trenched gates and all circumferential points of the contact hole 12.



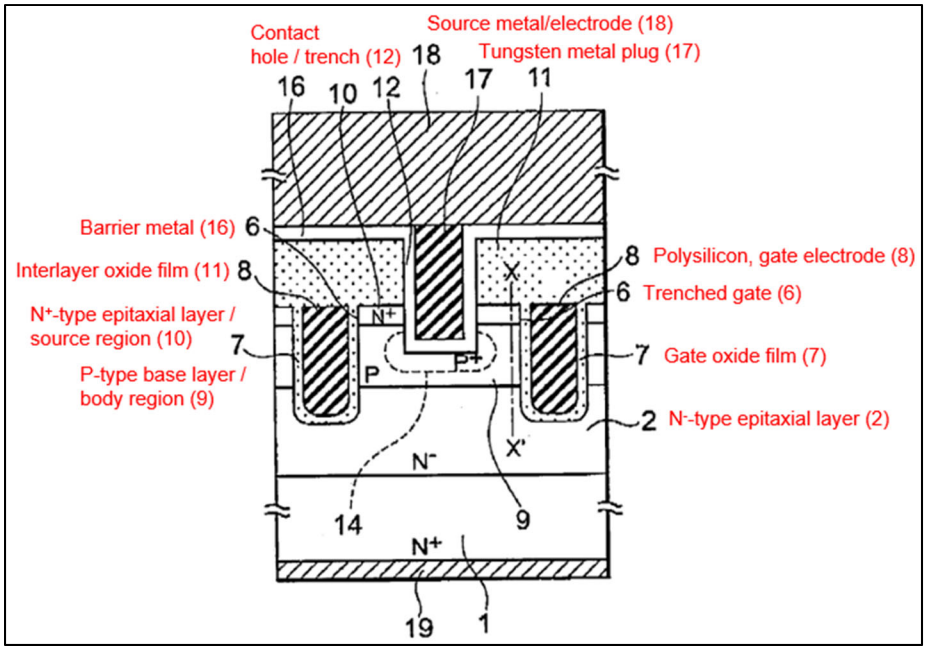
Kobayashi, Figure 4A (annotated)



Kobayashi, Figure 5A (annotated)

g. 1[f]: "and said contact metal plug connected to a source metal disposed on top of said circular trench contact."

Element 1[f] is disclosed in Kobayashi. As shown below in Kobayashi's Figure 5A (annotated), "on the surface of the [tungsten plug] 17 and the barrier metal 16, a source electrode 18 is formed." Ex. 1005, 6:64—67.

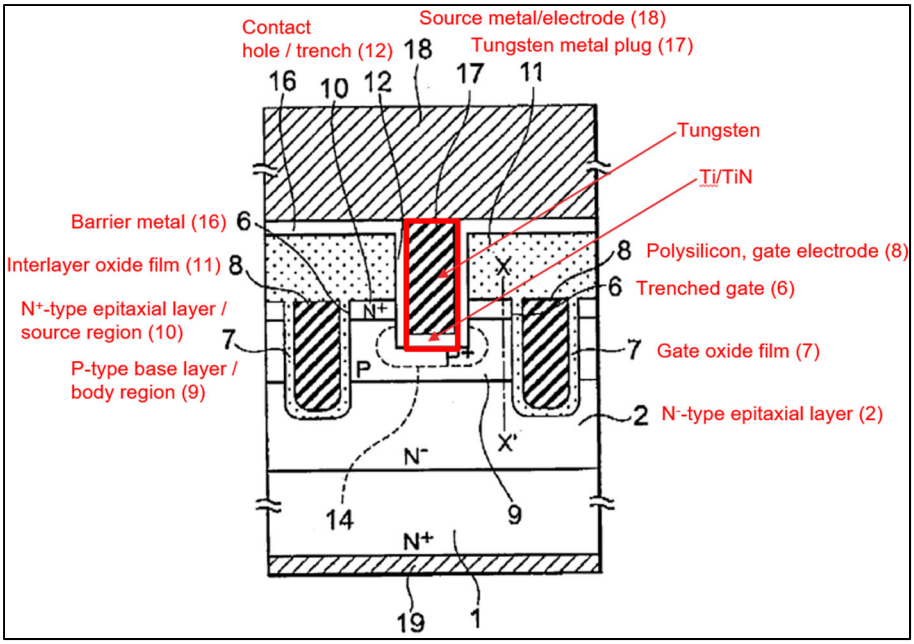


Kobayashi, Figure 5A (annotated)

2. Claim 3

a. "The trenched semiconductor power device of claim 1 wherein: said contact metal plug disposed in said hole of said circular trench contact further comprising a Ti/TiN/W metal plug."

Claim 3 is disclosed in Kobayashi. As discussed above and shown below in Kobayashi's Figure 5A (annotated), a contact metal plug 17 is disposed in a circular trench contact 12 (*see* § VIII.A.1.c—d). Kobayashi further discloses W (Tungsten) deposited on top of Ti (Titanium) and TiN (Titanium Nitride) within the circular trench contact. Ex. 1005, 9:30—33.

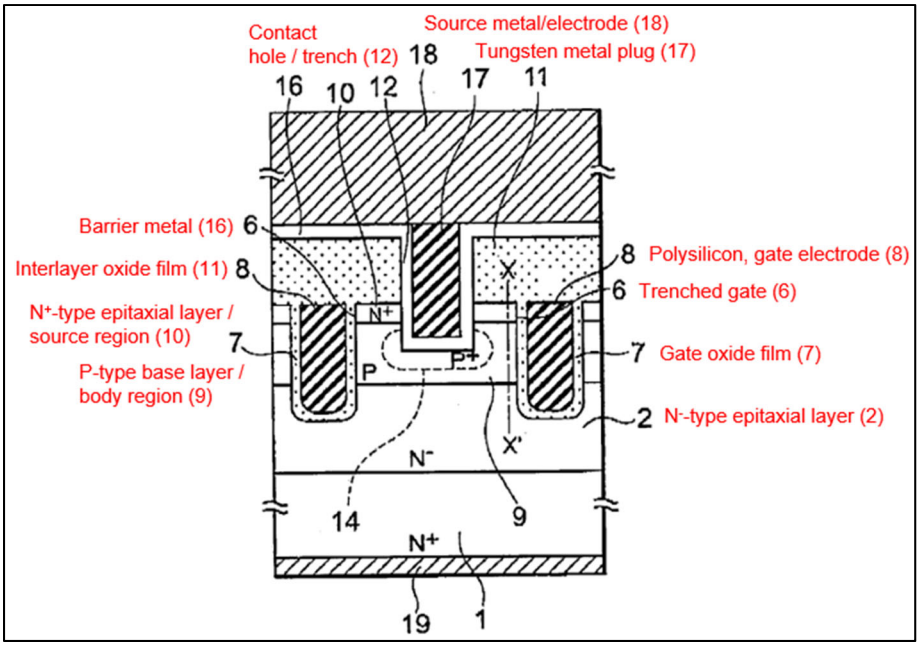


Kobayashi, Figure 5A (annotated)

3. Claim 4

a. "The trenched semiconductor power device of claim 1 wherein: said source metal disposed on top of and in contact with a top surface of said metal plug further comprising a layer composed of aluminum alloys including alloys of AlCu or AlSiCu."

Claim 4 is disclosed in Kobayashi. As discussed above and shown below in Kobayashi's Figure 5A (annotated), a source metal 18 is disposed on top of a circular trench contact 12 (see § VIII.A.1.g). Kobayashi further discloses that "AlSi (aluminum silicon) or AlSiCu (aluminum copper silicon) is deposited by sputtering to form the source electrode 18." Ex. 1005, 9:36—38.



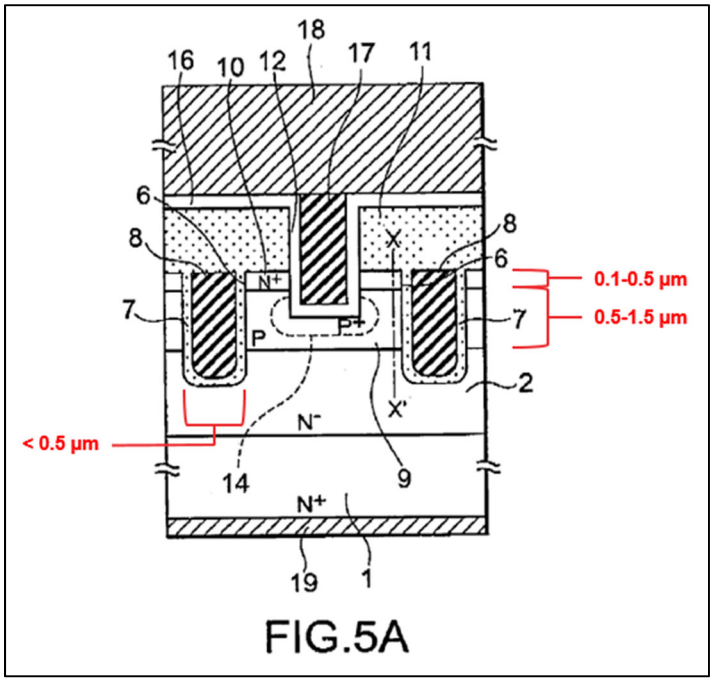
Kobayashi, Figure 5A (annotated)

4. Claim 5

a. "The trenched semiconductor power device of claim 1 wherein: a diameter of a top surface of said circular trench contact is smaller than 1.0 micrometer."

Claim 5 is disclosed in Kobayashi. As discussed above and shown below in Kobayashi's Figure 5A (annotated), a circular trench contact is disclosed (*see supra* § VIII.A.1.c). Kobayashi further discloses in relation to trench 6 that "it is possible to obtain the trench width not greater than 0.5 µm." Ex. 1005, 7:49—50. Kobayashi also discloses that N^+ source layer 10 has a depth of 0.1-0.5 µm and that the P base layer 9 has a depth of 0.5-1.5 µm. *Id.*, 7:19-21 (explaining that Figs. 6A-6D, 7A-7D, and 8A-8C describe the method of producing the MOSFET in Fig.

5A); 8:21-46. When considering the relative proportions[2] of the MOSFET of Figure 5A, the diameter of the circular trench contact is approximately the same as the width as the trench 6. Ex. 1003 ¶ 81. Accordingly, Kobayashi discloses that it is possible to obtain a circular trench contact width/diameter not greater than 0.5 µm. A width of 0.5 µm is less than what is required by the claim (which requires a diameter smaller than 1.0 µm), and so this limitation is also met.



Kobayashi, Figure 5A (annotated)

B. Ground 2: Claims 2 and 6 are unpatentable under pre-AIA 35 U.S.C. § 103 as obvious over Kobayashi in view of Kikkawa.

[2]Other than regions 18 and 1, which are specially annotated with "≈" to indicate that those regions extend further than depicted, the rest of the drawing is drawn to relative scale. Ex. 1003 ¶ 81.

Claim 2 of the ’409 Patent is unpatentable under pre-AIA 35 U.S.C. § 103 as obvious over Kobayashi in view of Kikkawa, T. et al, “A Quarter-Micrometer Interconnection Technology Using a TiN/Al-Si-Cu/TiN/Al-Si-Cu/TiN/Ti Multilayer Structure,” IEEE Transactions on Electron Devices, Vol. 40, No. 2, February 1993 (“Kikkawa”). The following discussion is fully supported by the Declaration of Dr. Liu. Ex. 1003 ¶ 83.

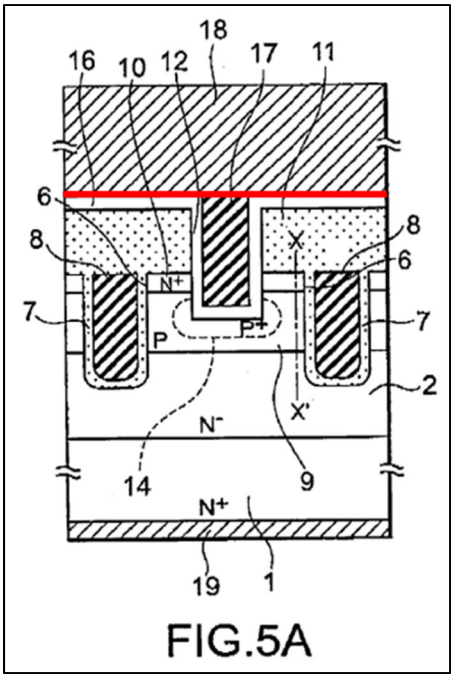
1. Claim 2

a. “The trenched semiconductor power device of claim 1 further comprising: a contact resistance reduction metal layer composed of a titanium (Ti) layer disposed above a top surface said contact metal plug and below a bottom surface of said source metal for reducing a contact resistance between said contact metal plug and said source metal.”

Claim 2 would have been obvious to a POSITA at the time of the filing of the ’409 Patent based on Kobayashi in view of Kikkawa. Specifically, claim 2 depends from claim 1, and claim 1 is disclosed by Kobayashi for the reasons provided above. *See supra* § VIII.A.1. Further, as discussed above, Kobayashi discloses a contact metal plug 17 connected to a source metal 18 disposed on top of a circular trench contact 12 (*see supra* § VIII.A.1.g). As shown in Kobayashi’s Figure 5A (annotated) below, Kobayashi teaches a metal layer (source metal layer 18) disposed above a top surface of the contact metal plug. Ex. 1005 6:61—65;

see also supra § VIII.A.3 (explaining that the source metal layer 18 can be made of AlSiCu / AlCu).

Kikkawa teaches that it was well known in the art at least by the time of the filing of the ’409 Patent that an AlCu / AlSiCu metal layer could have a bottom layer made of titanium (e.g., Ti or TiN) designed as both an electro- and stress-migration-resistant interconnection structure. Ex. 1007 at 4. This would yield a lower contact resistance over time (relative to *not* having a Ti or TiN bottom layer) when the device undergoes electro-migration stress, which also would have been appreciated by a POSITA at the time of the filing of the ’409 Patent. Ex. 1003 ¶ 85. A POSITA would have been motivated to combine the teachings of Kobayashi and Kikkawa to include a titanium layer disposed below the bottom surface of the source metal (and therefore above the top surface of the contact metal plug) for the reasons discussed below in § VIII.B.3. Ex. 1003, ¶ 86; *see also* Ex. 1005, Fig. 5A (annotated to show the position of the titanium layer in the combination with Kikkawa).



Kobayashi, Figure 5A (annotated)

2. Claim 6

Kobayashi discloses and anticipates every limitation of claim 6.

a. 6 [preamble]: "A trenched semiconductor power device comprising a plurality of trenched gates surrounding a plurality of transistor cells formed in a semiconductor substrate, wherein:"

To the extent the preamble of claim 6 is limiting, it is disclosed in Kobayashi. *See supra* § VIII.A.1.a.

b. 6[a]: "said trenched gates surrounding said transistor cells as closed cells constituting substantially square-shaped cells with truncated corners"

Element 6[a] is disclosed by Kobayashi. *See supra* § VIII.A.1.b (explaining that Kobayashi discloses closed cells that are substantially square shaped with corners that are truncated by design layout).

c. 6[b]: "each of said closed cells further includes a circular trench contact hole disposed substantially in a central portion of said closed cells with a diameter of a top surface of said circuit trench contact less than 1.0 micrometer, penetrating through source regions surrounding said trenched gates and extending into body regions encompassing said source regions"

Element 6[b] is disclosed in Kobayashi. *See supra* §§ VIII.A.1.c.

d. 6[c]: "said circular trench contact comprises a hole opened from a top surface of said semiconductor substrate"

Element 6[c] is disclosed in Kobayashi. *See supra* § VIII.A.1.d.

e. 6[d]: "wherein sidewalls of said hole are surrounded by and in contact said source and body regions"

Element 6[d] is disclosed in Kobayashi. *See supra* § VIII.A.1.e.

f. 6[e]: "said circular trench contact is separate from said trenched gates with said source region and body region disposed between a gate oxide lining of said trenched gates and all circumferential points of the circular trench contact"

Element 6[e] is disclosed in Kobayashi. *See supra* § VIII.A.1.f.

g. 6[f]: "said circular trench contact hole is filled with a metal plug composed of a Ti/TiN/W plug to contact said source and body regions"

Element 6[f] is disclosed in Kobayashi. *See supra* §§ VIII.A.1.d, VIII.A.1.e., and VIII.A.2.

h. 6[g]: "said metal plug contacting a source metal disposed on top of said metal plug wherein said source

metal layer composed of Ti/AlCu or Ti/AlSiCu alloys."

Element 6[g] would have been obvious to a POSITA at the time of the filing of the '409 Patent based on Kobayashi in view of Kikkawa. *See supra* §§ VIII.A.1.g, VIII.A.3, VIII.B.1. *See also infra* § VIII.B.3.

3. Combining Kobayashi and Kikkawa

As discussed above, the combination of Kobayashi and Kikkawa discloses all elements of claims 2 and 6 (*see supra* §§ VIII.B.1, VIII.B.2). For the reasons discussed below, it would have been obvious to a POSITA before the effective filing date of the '409 Patent to combine Kobayashi and Kikkawa to arrive at the trenched semiconductor power device of claims 2 and 6, rendering those claims invalid under 35 U.S.C. § 103.

a. Kobayashi, Kikkawa, and the '409 Patent are analogous art seeking to solve similar problems.

1. Same field of endeavor

The '409 Patent, Kobayashi, and Kikkawa are all directed to semiconductor structures and therefore are analogous art since they are in the same field of endeavor. Specifically, the '409 Patent relates to "the cell structure, device configuration and fabrication process of power semiconductor devices." Ex. 1001, 1:7-9. Kobayashi similarly relates to "a vertical MOSFET (Metal Oxide Semiconductor Field Effect Transistor) reduced in cell size . . . and a method of producing the same." Ex. 1005, 1:7-12–6. And Kikkawa relates to a "new

interconnection structure using a . . . multilayer conductor . . . for DRAM." Ex. 1007 at 3.

2. Pertinent to the same problems within the prior art.

Additionally, the '409 Patent, Kobayashi, and Kikkawa are all directed to solutions to similar problems with semiconductor devices (including high power devices), such as, designing for electro- and stress-migration resistant (and therefore contact resistance when undergoing electro-migration stress) interconnection structures. The '409 Patent claims a titanium metal layer "for reducing a contact resistance between said contact metal plug and said source metal." Similarly, Kobayashi discloses a Ti and TiN barrier metal layer below the source metal, which serves the purpose of electro-migration resistance. Ex. 1003 ¶ 99. Kikkawa similarly discloses that problems with electro-migration and contact resistance are improved by using Ti and TiN barrier layers on an AlSiCu metal layer in a semiconductor structure. Ex. 1007 at 4.

Accordingly, the Kobayashi and Kikkawa references are analogous art which may be combined to render claims 2 and 6 obvious, both because these references are in the same field of endeavor as claims 2 and 6 of the '409 Patent and because these references are reasonably pertinent to the problems addressed by the inventors of the '409 Patent. *Smartdoor Holdings, Inc. v. Edmit Indus., Inc.*, 707, 708 F. App'x 705 (Fed. Cir. 2017).

b. Known benefits of combining the teachings of Kobayashi and Kikkawa

A POSITA before the effective filing date of the ’409 Patent would have recognized several benefits of combining Kobayashi and Kikkawa as described in this Petition, and therefore would have been incentivized to do so. For example, it was well known to a POSITA that adding a titanium (Ti) or titanium nitride (TiN) layer to the bottom of Kobayashi’s source metal layer would improve the reliability of the metal layer through the reduction of stress-induced electro-migration, which would also result in reduced contact resistance between metal layers and also reinforce the mechanical strength of the source metal layer. Ex. 1007 at 4; Ex. 1003 ¶101.

c. Rationales for combining Kobayashi and Kikkawa

A POSITA before the effective filing date of the ’409 Patent would have been motivated to combine Kobayashi and Kikkawa with a reasonable expectation of success, for several reasons.

1. Express teaching

First, Kikkawa expressly teaches that problems with electro-migration and contact resistance are improved by using Ti and TiN barrier layers on an AlSiCu metal layer in a semiconductor structure. Ex. 1007 at 4; Ex. 1003 ¶ 103. The addition of the TiN / Ti layers (as disclosed by Kikkawa) to the source metal of Kobayashi would further achieve the aim set out by Kikkawa. *Id.* As

demonstrated by Kobayashi and Kikkawa, the source metal layer, metal plug, and barrier or intermediate TiN / Ti layers are all known, conventional, familiar elements to a POSITA. Ex. 1003 ¶ 103. Therefore, there is "teaching, suggestion, or motivation to combine known elements" in the prior art itself. Even though such teaching or suggestion is not required to prove obviousness, the presence of such teaching or suggestion is a strong indicator of obviousness. *KSR Int'l.*, 550 U.S. at 415, 418; *ThermoLife Int'l, LLC v. Myogenix Corp.*, No. 13cv651 JLS (MDD), 2016 U.S. Dist. LEXIS 129181, at *10 (S.D. Cal. Sept. 21, 2016) (citing *KSR Int'l*, 550 U.S. at 418).

2. Use of known techniques to improve similar devices in the same way

Second, combining Kobayashi and Kikkawa requires nothing more than the use of known techniques to improve similar devices in the same way. Kobayashi and Kikkawa are in the same field of endeavor, i.e. semiconductor structures. Both Kobayashi and Kikkawa disclose that there are known methods for interconnection and other metal layers within semiconductor structures. Ex. 1005, 9:30-53; Ex. 1007 at 3-4. Kobayashi and Kikkawa discloses similar devices, as both are directed to semiconductor structures and layers. E.g., Ex. 1005, 9:30-53; Ex. 1007 at 3-4; Ex. 1003 ¶ 104. Similar to the '409 Patent, which claims that its titanium (Ti) layer reduces contact resistance between a contact metal plug and a source metal (Ex. 1001, claims 2, 6), Kikkawa teaches that TiN / Ti layer below an

AlSiCu layer improves electro-migration and contact resistance in an interconnection structure of a semiconductor. Ex. 1007 at 4. Further, Kikkawa's TiN / Ti layer resides in a location proximate to the AlSiCu that makes its addition to Kobayashi a natural fit and common sense choice. Ex. 1005 at Fig. 5A; Ex. 1007 at Fig. 1; Ex. 1003 ¶ 104. Adding Kikkawa's TiN / Ti layer to Kobayashi's source metal (AlSiCu layer) applies a known technique to realize a minor and commonplace modification. *Ignite USA, LLC v. CamelBak Prods., LLC*, 709 F. App'x 1010, 1015 (Fed. Cir. 2017) (affirming PTAB decision holding that "obvious design choices" well known to a POSITA would include shape or size changes such as "increasing the width of the opening and changing the shape or size of the spring."); *Bristol-Myers Squibb Co. v. Teva Pharm. USA, Inc.*, 752 F.3d 967, 973 (Fed. Cir. 2014) (finding it obvious to make a "minor modification" to a chemical compound disclosed in prior art to arrive at a claimed invention); Ex. 1003 ¶ 104. Therefore, combining Kobayashi and Kikkawa requires only known techniques to improve similar devices in the same way.

3. Applying a known technique to a known device ready for improvement to yield predictable results

Third, the combination of Kobayashi and Kikkawa applies a known technique to a known device ready for improvement to yield predictable results. As discussed above, adding Kikkawa's TiN / Ti layer to Kobayashi's source metal (AlSiCu layer) applies a known technique or method to a known structure which is

ready for improvement (as expressly taught by Kikkawa). Ex. 1003 ¶ 105. The combination would have had a reasonable expectation of success and/or a predictable result, that is, to improve electro-migration (which also reduces contact resistance). *Id.*

4. Combining familiar elements according to known methods to yield predictable results

Fourth, combining Kobayashi and Kikkawa requires nothing more than combining familiar elements according to known methods to yield predictable results. As demonstrated by Kobayashi and Kikkawa, the source metal layer, metal plug, and barrier or intermediate TiN / Ti layers are all known, conventional, familiar elements to a POSITA. Ex. 1003 ¶ 106. As discussed above, adding Kikkawa's TiN / Ti layer to Kobayashi's source metal (AlSiCu layer) uses a known method to realize a minor modification. *See Ignite USA, LLC*, 709 F. App'x at 1015; *Bristol-Myers Squibb Co.*, 752 F.3d at 973; Ex. 1003 ¶ 106. The combination would have had a reasonable expectation of success and/or a predictable result, for example, to improve electro-migration and therefore reduce contact resistance. Ex. 1003 ¶ 106.

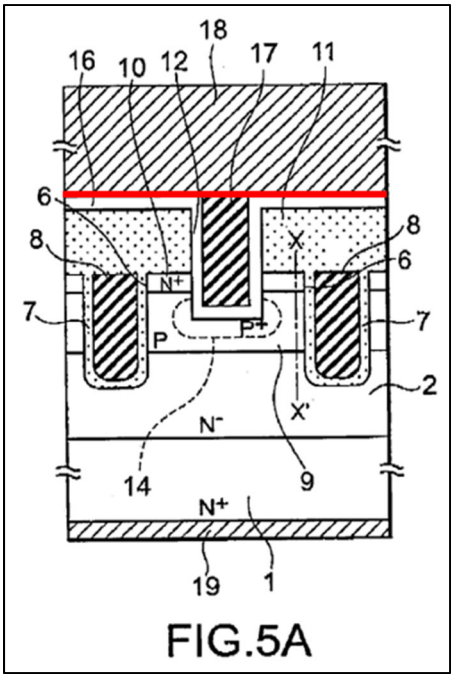
5. Known work in the field

Kobayashi discloses known work in the field of semiconductor structures. A POSITA would have been prompted to modify Kobayashi in view of Kikkawa for use in the same field based on design incentives or other market forces, and the

modification would have been predictable to a POSITA. Both Kobayashi and Kikkawa are directed to semiconductor structures. As discussed above, there are several design incentives for adding Kikkawa's TiN / Ti barrier layers into Kobayashi's design. *Id.* ¶ 106. In addition, a POSITA designing a semiconductor structure would naturally seek to improve electro-migration and contact resistance, where possible. Ex. 1003 ¶ 107; Ex. 1001 claims 2, 6; Ex. 1007 at 3-4. Thus, a POSITA considering Kobayashi would have been prompted to modify Kobayashi in view of Kikkawa. Ex. 1003 ¶ 107. Implementing a TiN / Ti barrier layer on the bottom of Kobayashi's source metal layer using known methods of design would have been within the skill of a POSITA. *Id.*

d. The combination of Kobayashi and Kikkawa

The combination of Kobayashi and Kikkawa renders obvious claims 2 and 6, as illustrated below in a hypothetical diagram based on Kobayashi's Figure 5A with the addition of the TiN / Ti layer for improving electro-migration and contact resistance disclosed in Kikkawa. Ex. 1003 ¶ 108.



Kobayashi, Figure 5A (annotated)

This case is similar to *Nanya Tech. Corp., et al. v. Lone Star Silicon Innovations LLC*, where the PTAB invalidated claims directed to a MOS semiconductor with a trenched gate. IPR2018-00063, Paper 25, Final Written Decision at 6-7, 22-35 (PTAB May 15, 2019) (*dismissed as moot Lone Star Silicon Innovations, LLC v. Nanya Tech. Corp.*, 810 Fed. Appx. 878, 879 (Fed. Cir. 2020)). There, Petitioner presented both anticipation and obviousness grounds based on each of three primary references. *Nanya* at 7-8. Citing to figures in the prior art, the Board held that the Petitioner had "persuasively map[ped]" the elements of each challenged claim, such that the claims were anticipated and/or obvious to the POSITA. *See*, *e.g.*, *id.* at 24-25. Further, the Board found the challenged claims obvious, because "any missing details in [the prior art] . . .

would have been 'conventional' and, thus, fully within the grasp of an ordinarily skilled artisan." *Id.* at 34 (internal citations omitted).

The combination of Kobayashi and Kikkawa is also similar to the proposed combination in *Micron Tech., Inc. v. Lone Start Silicon Innovations LLC*, where the Board agreed with Petitioner's expert that the proposed combination "is merely the use of known technique that improves similar devices . . . in the same way . . . to yield predictable results." IPR2017-01562, Paper 30, Final Written Decision at 35 (PTAB Dec. 13, 2018) (*aff'd Lone Star Silicon Innovations LLC v. Iancu*, 813 F. App'x 512 (Fed. Cir. 2020)) (internal quotations and citations omitted).

Based on reasons explained above, a POSITA would have found it obvious to combine Kobayashi and Kikkawa. *See KSR Int'l*, 550 U.S. at 415-18; *Micron Tech.*, IPR2017-01562, Paper 30 at 35; *Lone Star Silicon Innovations LLC*, 813 F. App'x 512; *Nanya*, IPR2018-00063, Paper 25 at 6-7, 22-35.

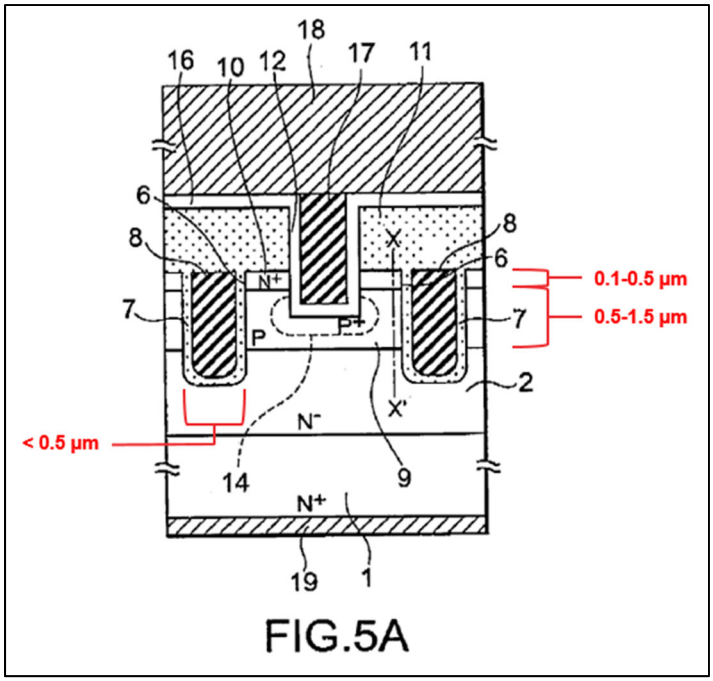
C. Ground 3: Claim 5 is unpatentable under pre-AIA 35 U.S.C. § 103 as obvious over Kobayashi and the knowledge of a POSITA.

1. Claim 5

a. "The trenched semiconductor power device of claim 1 wherein: a diameter of a top surface of said circular trench contact is smaller than 1.0 micrometer."

As discussed above in § VIII.A.4, claim 5 is disclosed in Kobayashi. To the extent the Board disagrees that the "diameter of a top surface of said circular trench contact is smaller than 1.0 micrometer," is explicitly disclosed, this claim

element would have been obvious to a POSITA based on the disclosure of Kobayashi and the knowledge of a POSITA. When considering the relative proportions of the MOSFET of Figure 5A (annotated below), a POSITA would have understood that the diameter of the circular trench contact is approximately the same as the width as the trench 6 (which Kobayashi teaches can be a width less than 1.0 µm). Ex. 1005, 7:34-55; Ex. 1003 ¶ 110. In addition, a POSITA would understand several design considerations that would result in a diameter of less than 1 µm. For example, a POSITA would consider the need to minimize the overall width of the cell and minimize the width of the source contact trench for purposes of an easier subsequent filling of the source contact trench without having voids or unwanted variations in the topography. Ex. 1003 ¶ 111. Accordingly, a POSITA would have understood that the diameter/width of the circular contact trench is less than 1.0 µm. *Id.*; *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. at 421; *Nanya*, IPR2018-00063, Paper 25 at 6-7, 22-35.



Kobayashi, Figure 5A (annotated)

D. Ground 4: Claims 1, 3—5 are unpatentable under pre-AIA 35 U.S.C. § 103 as obvious over Kobayashi in view of Hshieh.

Claims 1, 3-5 of the '409 Patent are unpatentable under at least pre-AIA 35 U.S.C. § 103 as obvious over Kobayashi in view of Hshieh. The following discussion is fully supported by the Declaration of Dr. Liu. Ex. 1003 ¶ 116.

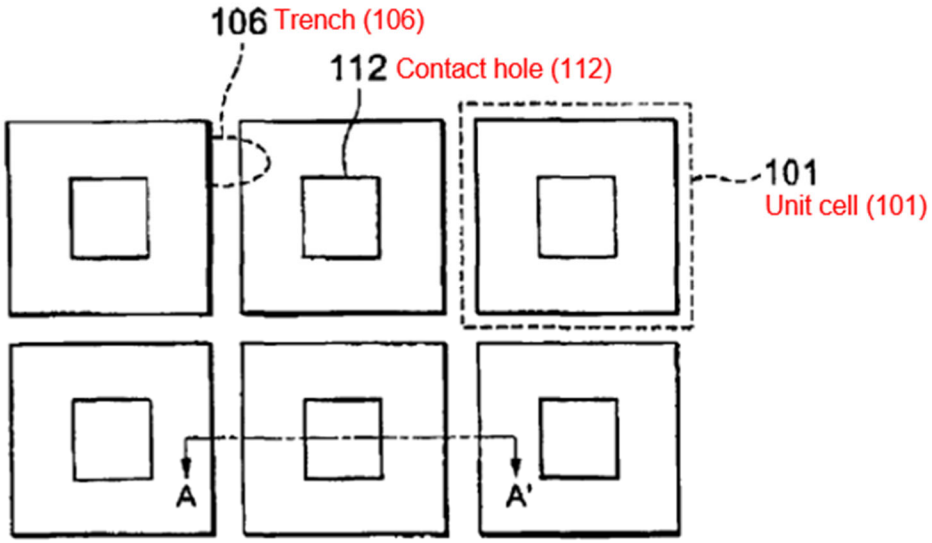
1. Claim 1

a. 1 [preamble] : "A trenched semiconductor power device comprising a plurality of trenched gates surrounding a plurality of transistor cells formed in a semiconductor substrate, wherein:"

To the extent the preamble of claim 1 is limiting, it is disclosed in Kobayashi. *See supra* § VIII.A.1.a.

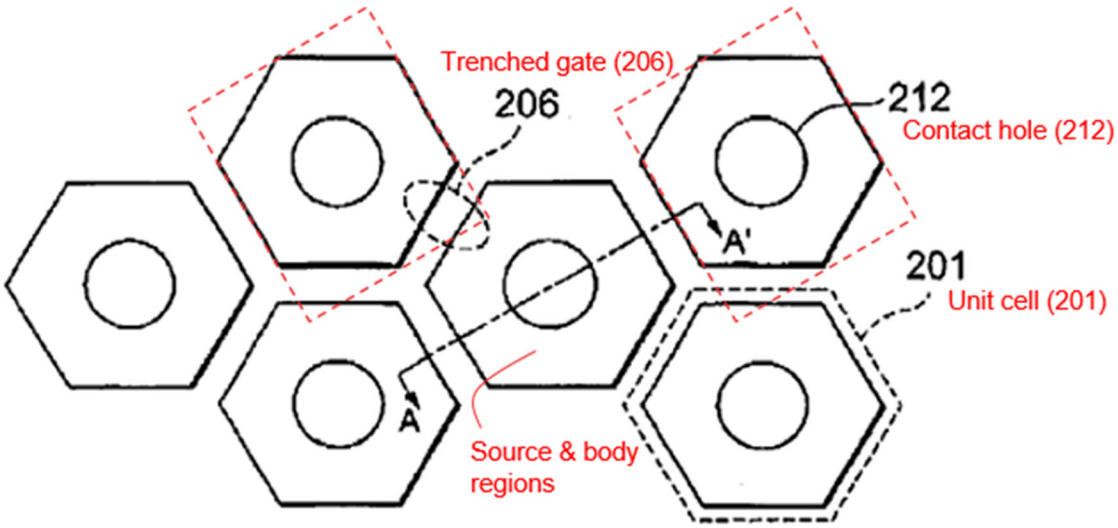
b. 1[a]: "said trenched gates surrounding said transistor cells as closed cells constituting substantially square-shaped cells with rounded corners;"

Element 1[a] is disclosed by Kobayashi combined with Hshieh. As depicted below in Kobayashi's Figure 3A (annotated), "a plurality of ***square cells*** are arranged in a matrix." Ex. 1005, 6:26—27 (emphasis added).



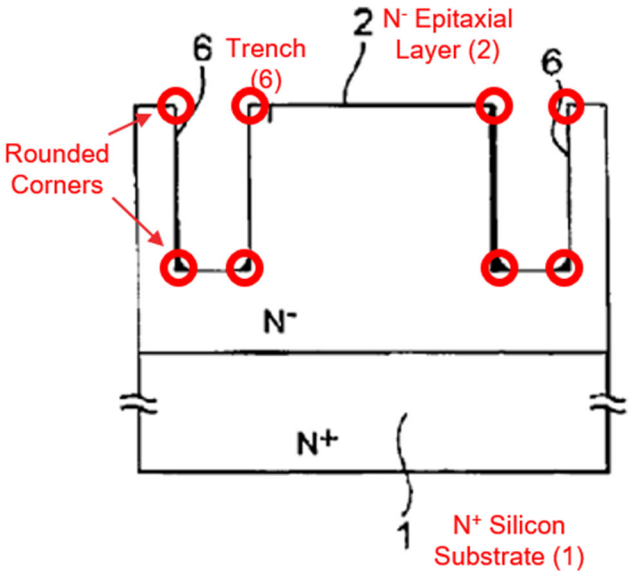
<u>Kobayashi, Figure 3A (annotated)</u>

Furthermore, as shown below in Kobayashi's Figure 4A (annotated), Kobayashi discloses "a plurality of hexagonal cells"—i.e., substantially square cells with truncated corners. Ex. 1005, 6:30; Ex. 1003 ¶ 119.



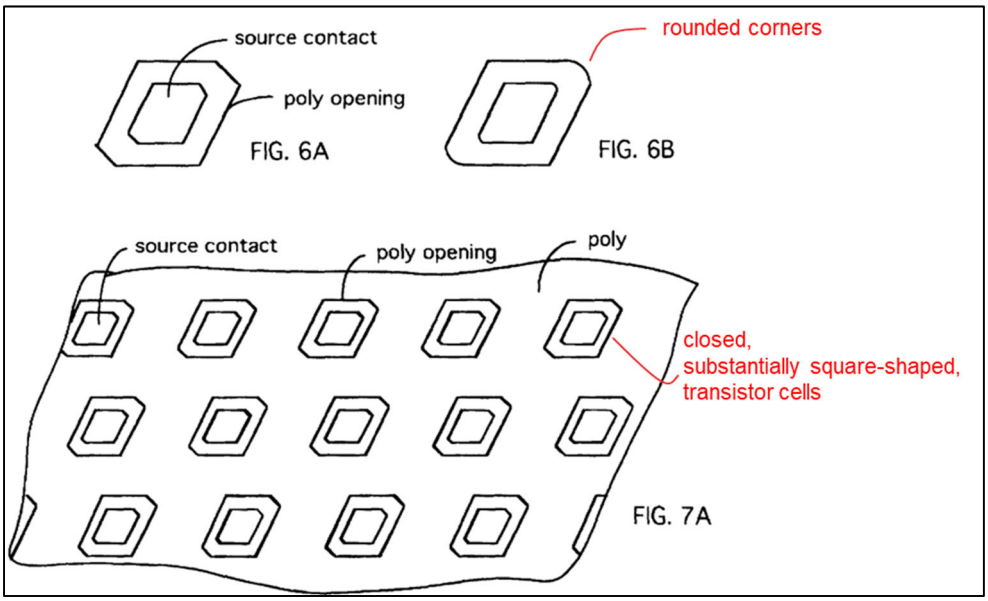
Kobayashi, Figure 4A (annotated)

Kobayashi's Figure 6C further discloses that the MOSFETs disclosed are made with a process where the "corners of each trench 6 at the bottom are rounded [and] corners of each trench 6 at an opening portion may also be rounded." Ex. 1005, 7:57—8:4; Ex. 1003 ¶ 120.



Kobayashi, Figure 6C (annotated)

Moreover, Hshieh discloses rounding the corners of transistor cells. Ex. 1006, 5:3-28; Ex. 1003 ¶ 121. As shown below in Hshieh Figure 6A—7A (annotated below), Hshieh's transistor cells are closed cells constituting cells with multiple truncated and rounded corners.



Hshieh, Figure 6A—7A (annotated)

Accordingly, Kobayashi discloses closed cells that are substantially square shaped with corners that are truncated by design layout, and Kobayashi and Hshieh disclose that the corners of the closed cells can be rounded (and the benefits for doing so). Ex. 1003 ¶ 122. As discussed below in § VIII.D.5, it would have been obvious to combine Kobayashi's square shaped cells that are truncated by design layout with Hshieh's rounded corners to arrive at element 1[a] of claim 1. Ex. 1003 ¶ 122.

c. 1[b]: "each of said closed cells further includes a circular trench contact disposed substantially in a central portion of said closed cells, penetrating through a source region surrounding said trenched gates and extending into a body region encompassing said source region;"

Element 1[b] of claim 1 is disclosed in Kobayashi. *See supra* § VIII.A.1.c.

d. 1[c]: "said circular trench contact comprises a hole opened from a top surface of said semiconductor substrate and is filled with a contact metal plug"

Element 1[c] of claim 1 is disclosed in Kobayashi. *See supra* § VIII.A.1.d.

e. 1[d]: "wherein sidewalls of said hole are surrounded by and in contact said source and body regions"

Element 1[d] of claim 1 is disclosed in Kobayashi. *See supra* § VIII.A.1.e.

f. 1[e]: "and said circular trench contact is separate from said trenched gates with said source region and body region disposed between a gate oxide lining of said trenched gates and all circumferential points of the circular trench contact;"

Element 1[e] of claim 1 is disclosed in Kobayashi. *See supra* § VIII.A.1.f.

g. 1[f]: "and said contact metal plug connected to a source metal disposed on top of said circular trench contact."

Element 1[f] of claim 1 is disclosed in Kobayashi. *See supra* § VIII.A.1.g.

2. Claim 3

a. "The trenched semiconductor power device of claim 1 wherein: said contact metal plug disposed in said hole of said circular trench contact further comprising a Ti/TiN/W metal plug."

Claim 3 is disclosed in Kobayashi. *See supra* § VIII.A.2.

3. Claim 4

a. "The trenched semiconductor power device of claim 1 wherein: said source metal disposed on top of and in contact with a top surface of said metal plug further comprising a layer composed of aluminum alloys including alloys of AlCu or AlSiCu."

Claim 4 is disclosed in Kobayashi. *See supra* § VIII.A.3.

4. Claim 5

a. "The trenched semiconductor power device of claim 1 wherein: a diameter of a top surface of said circular trench contact is smaller than 1.0 micrometer."

Claim 5 is disclosed in Kobayashi. *See supra* § VIII.A.4.

5. Combining Kobayashi and Hshieh

As discussed above, the combination of Kobayashi and Hshieh discloses all elements of claims 1, 3-5 (*see* §§ VIII.D.1—4). For the reasons discussed below, it would have been obvious to a POSITA before the effective filing date of the '409 Patent to combine Kobayashi and Hshieh to arrive at the trenched semiconductor power device of claims 1, 3-5, rendering those claims invalid under 35 U.S.C. § 103.

a. Kobayashi, Hshieh, and the '409 Patent are analogous art seeking to solve similar problems.

1. Same field of endeavor

The '409 Patent, Kobayashi, and Hshieh are all directed to semiconductor structures and therefore are analogous art since they are in the same field of endeavor. Specifically, the '409 Patent relates to "the cell structure, device

configuration and fabrication process of power semiconductor devices." Ex. 1001, 1:7-9. Kobayashi similarly relates to "a vertical MOSFET (Metal Oxide Semiconductor Field Effect Transistor) reduced in cell size . . . and a method of producing the same." Ex. 1005, 1:7-12–6. And Hshieh relates to a "power transistor cell[s] supported on a semiconductor substrate." Ex. 1006, Abstract.

2. Pertinent to the same problems within the prior art.

Additionally, the '409 Patent, Kobayashi, and Hshieh are all directed to solutions to similar problems with semiconductor devices (including high power devices), such as, vulnerabilities with respect to corners of square cells. It is known that the corners of the square cells tend to induce higher peak electric fields, which would lead to a low avalanche breakdown voltage, which is undesirable. The '409 Patent describes problems in the prior art relating to square cell configurations with sharp corners as causing low avalanche current and reduced device ruggedness due to the parasitic N+PN latches near the corners. Ex. 1001 1:15-62; Ex. 1003 ¶ 133. Similarly, Kobayashi discloses rounding corners of trenches in square cells. Ex. 1005, 7:57-8:4; Ex. 1003 ¶ 133. In doing so, Kobayashi refers to a paper by Sang-Gi Kim et al, which discusses the benefits of trench corner rounding leading to higher breakdown voltage and lower leakage current. These are the same benefits discussed in the '409 Patent. Ex. 1005, 7:57-8:4, Ex. 1003 ¶ 133; Ex. 1012. Hshieh similarly discloses the problems of

vulnerable punch-through weak points in the corners of square cell, also due to undesirable higher peak electric field being reached at the corners. Ex. 1006, 2:19-39; Ex. 1003 ¶ 133.

Accordingly, the Kobayashi and Hshieh references are analogous art which may be combined to render claims 1, 3-5 obvious, both because these references are in the same field of endeavor as claims 1, 3-5 of the ’409 Patent and because these references are reasonably pertinent to the problems addressed by the inventors of the ’409 Patent. *Smartdoor Holdings, Inc. v. Edmit Indus., Inc.*, 707, 708 F. App’x 705 (Fed. Cir. 2017).

b. Known benefits of combining the teachings of Kobayashi and Hshieh

A POSITA before the effective filing date of the ’409 Patent would have recognized several benefits of combining Kobayashi and Hshieh as described in this Petition, and therefore would have been incentivized to do so. For example, it was well known to a POSITA that rounding the corners of square (or substantially square) cells in semiconductor structures had several advantages. Ex. 1006, 2:19-39; Ex. 1003 ¶ 135; Ex. 1005, 7:57-8:4.

c. Rationales for combining Kobayashi and Hshieh

A POSITA before the effective filing date of the ’409 Patent would have been motivated to combine Kobayashi and Hshieh with a reasonable expectation of success, for several reasons.

1. Express teaching

First, Hshieh expressly teaches advantages for rounding the corners of square or substantially square-shaped cells. Ex. 1006, 5:3-17, Figs. 6A-8B; Ex. 1003 ¶ 137. Combining the rounded corners (as disclosed by Hshieh) with the truncated corners disclosed in Kobayashi would further achieve the aim set out by Hshieh. Ex. 1003 ¶ 137. As demonstrated by Kobayashi and Hshieh, the square-shaped cells, their corners, and methods of truncating, blunting, and rounding the corners, are all known, conventional, familiar elements to a POSITA. Ex. 1003 ¶ 137. Therefore, there is "teaching, suggestion, or motivation to combine known elements" in the prior art itself. Even though such teaching or suggestion is not required to prove obviousness, the presence of such teaching or suggestion is a strong indicator of obviousness. *KSR Int'l.*, 550 U.S. at 415, 418; *ThermoLife Int'l, LLC v. Myogenix Corp.*, No. 13cv651 JLS (MDD), 2016 U.S. Dist. LEXIS 129181, at *10 (S.D. Cal. Sept. 21, 2016) (citing *KSR Int'l*, 550 U.S. at 418).

2. Use of known techniques to improve similar devices in the same way

Second, combining Kobayashi and Hshieh requires nothing more than the use of known techniques to improve similar devices in the same way. Kobayashi and Hshieh are in the same field of endeavor, i.e. semiconductor structures. Both Kobayashi and Hshieh disclose that there are known methods for addressing problems with sharp corners in closed cells within semiconductor structures. Ex.

1005, 9:30-53; Ex. 1006, 2:19-39. Kobayashi and Hshieh disclose similar devices, as both are directed to semiconductor structures and closed cell layouts. E.g., Ex. 1005, Fig. 4A, 7:57-8:4; Ex. 1006, Figs. 6A-8B; Ex. 1003 ¶ 138. Similar to the '409 Patent, which seeks to address known difficulties that are pronounced at the corners of trenches in closed cell layouts, Hshieh teaches that rounding the corners of such devices has advantages. Ex. 1006, 5:3-17, Figs. 6A-8B; Ex. 1003 ¶ 138. Further, Hshieh's rounding is provided to corners of substantially square cells, which makes its combination with Kobayashi a natural fit and common sense choice. Ex. 1005 at Fig. 5A; Ex. 1006 at Figs. 6A-8B; Ex. 1003 ¶ 138. Adding Hshieh's rounding of corners to Kobayashi's truncated corners of a closed cell layout applies a known technique to realize a minor and commonplace modification. *Ignite USA, LLC v. CamelBak Prods., LLC*, 709 F. App'x 1010, 1015 (Fed. Cir. 2017) (affirming PTAB decision holding that "obvious design choices" well known to a POSITA would include shape or size changes such as "increasing the width of the opening and changing the shape or size of the spring."); *Bristol-Myers Squibb Co. v. Teva Pharm. USA, Inc.*, 752 F.3d 967, 973 (Fed. Cir. 2014) (finding it obvious to make a "minor modification" to a chemical compound disclosed in prior art to arrive at a claimed invention); Ex. 1003 ¶ 138. Therefore, combining Kobayashi and Hshieh requires only known techniques to improve similar devices in the same way.

3. Applying a known technique to a known device ready for improvement to yield predictable results

Third, the combination of Kobayashi and Hshieh applies a known technique to a known device ready for improvement to yield predictable results. As discussed above, adding Hshieh's rounding of corners to Kobayashi's truncated corners of a closed cell layout applies a known technique or method to a known structure which is ready for improvement (as expressly taught by Hshieh). Ex. 1003 ¶ 139. The combination would have had a reasonable expectation of success and/or a predictable result, that is, to improve electro-migration and contact resistance. *Id.*

4. Combining familiar elements according to known methods to yield predictable results

Fourth, combining Kobayashi and Hshieh requires nothing more than combining familiar elements according to known methods to yield predictable results. As demonstrated by Kobayashi and Hshieh, the square-shaped cells, their corners, and methods of truncating, blunting, and rounding the corners, are all known, conventional, familiar elements to a POSITA. Ex. 1003 ¶ 140. As discussed above, adding Hshieh's rounding of corners to Kobayashi's truncated corners of a closed cell layout uses a known method to realize a minor modification. *See Ignite USA, LLC*, 709 F. App'x at 1015; *Bristol-Myers Squibb Co.*, 752 F.3d at 973; Ex. 1003 ¶ 140. The combination would have had a

reasonable expectation of success and/or a predictable result, for example, to improve electro-migration and contact resistance. Ex. 1003 ¶ 140.

5. Known work in the field

Kobayashi and Hshieh disclose known work in the field of semiconductor structures. A POSITA would have been prompted to modify Kobayashi in view of Hshieh for use in the same field based on design incentives or other market forces, and the modification would have been predictable to a POSITA. Both Kobayashi and Hshieh are directed to semiconductor structures. As discussed above, there are several design incentives for adding Hshieh's rounding of corners to Kobayashi's truncated corners of a closed cell layout. *Id.* ¶ 141. In addition, a POSITA designing a semiconductor structure would naturally seek to eliminate known problems at the corners of closed cells, where possible. *Id.*; Ex. 1005, Fig. 4A, 7:57-8:4; Ex. 1006, Figs. 6A-8B; 5:3-17. Thus, a POSITA considering Kobayashi would have been prompted to modify Kobayashi in view of Hshieh. Ex. 1003 ¶ 141. Rounding the truncated corners of closed cell layouts using known methods of design would have been within the skill of a POSITA. *Id.*

d. The combination of Kobayashi and Hshieh

Accordingly, the combination of Kobayashi and Hshieh renders claims 1, 3-5 obvious as described in § VIII.D.1.b.

This case is also similar to *Nanya Tech. Corp., et al. v. Lone Star Silicon Innovations LLC* and *Micron Tech., Inc. v. Lone Start Silicon Innovations LLC*, which cases are explained above. *See supra* § VIII.B.3.d. Based on reasons explained above, a POSITA would have found it obvious to combine Kobayashi and Hshieh. *See KSR Int'l*, 550 U.S. at 415-18; *Micron Tech., Inc.*, IPR2017-01562, Paper 30 at 35; *Lone Star Silicon Innovations LLC*, 813 F. App'x 512; *Nanya Tech. Corp.*, IPR2018-00063, Paper 25 at 6-7, 22-35.

E. Ground 5: Claims 2, 6 are unpatentable under pre-AIA 35 U.S.C. § 103 as obvious over Kobayashi, Hshieh, and Kikkawa.

Claims 2, 6 of the '409 Patent are unpatentable under pre-AIA 35 U.S.C. § 103 as obvious over the Kobayashi, Hshieh, and Kikkawa. The following discussion is fully supported by the Declaration of Dr. Liu. Ex. 1003 ¶¶ 144—155.

1. Claim 2

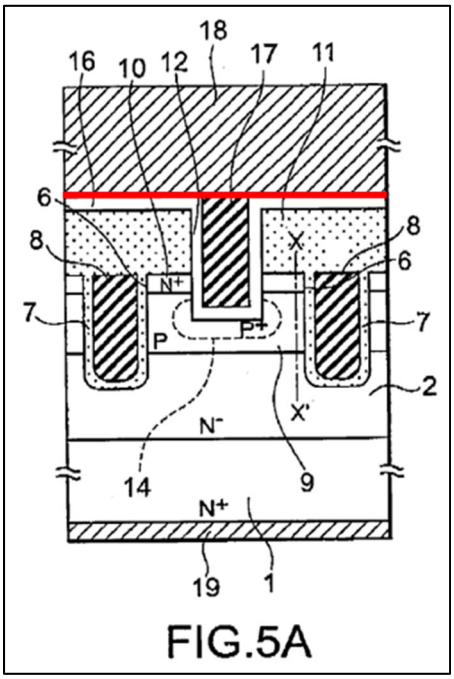
a. "The trenched semiconductor power device of claim 1 further comprising: a contact resistance reduction metal layer composed of a titanium (Ti) layer disposed above a top surface said contact metal plug and below a bottom surface of said source metal for reducing a contact resistance between said contact metal plug and said source metal."

Claim 2 would have been obvious to a POSITA at the time of the filing of the '409 Patent based on Kobayashi in view of Kikkawa and Hshieh. Specifically, claim 2 depends from claim 1, and claim 1 is disclosed by Kobayashi in view of Hshieh for the reasons provided above. *See supra* § VIII.D.1. Further, as

discussed above, Kobayashi discloses a contact metal plug 17 connected to a source metal 18 disposed on top of a circular trench contact 12 (see supra § VIII.A.1.g). As shown in Kobayashi's Figure 5A (annotated) below, Kobayashi teaches a metal layer (source metal layer 18) disposed above a top surface of the contact metal plug. Ex. 1005 6:61—65; *see also supra* § VIII.A.3 (explaining that the source metal layer 18 can be made of AlSiCu / AlCu).

Kikkawa teaches that it was well known in the art at least by the time of the filing of the '409 Patent that an AlCu / AlSiCu metal layer could have a bottom layer made of titanium (e.g., Ti or TiN) designed as both an electro- and stress-migration-resistant interconnection structure. Ex. 1007 p. 4. This would result in a lower contact resistance over time (relative to *not* having a Ti or TiN bottom layer) when the device undergoes electro-migration stress, which also would have been appreciated by a POSITA at the time of the filing of the '409 Patent. Ex. 1003 ¶ 85. A POSITA would have been motivated to combine the teachings of Kobayashi and Hshieh for the reasons described above. *See supra* § VIII.D.5. A POSITA would have further been motivated to combine Kobayashi and Hshieh with Kikkawa to include a titanium layer disposed below the bottom surface of the source metal (and therefore above the top surface of the contact metal plug) for the reasons discussed in §§ VIII.B.3. Ex. 1003 ¶ 146; *see also* Ex. 1005, Fig. 5A

(annotated to show the position of the titanium layer in the combination with Kikkawa).



Kobayashi, Figure 5A (annotated)

2. Claim 6

Claim 6 would have been obvious to a POSITA at the time of the filing of the ’409 Patent based on Kobayashi in view of Kikkawa and Hshieh.

a. 6 [preamble]: “A trenched semiconductor power device comprising a plurality of trenched gates surrounding a plurality of transistor cells formed in a semiconductor substrate, wherein:”

To the extent the preamble of claim 6 is limiting, it is disclosed in Kobayashi. *See supra* § VIII.A.1.a.

b. 6[a]: “said trenched gates surrounding said transistor cells as closed cells constituting substantially square-shaped cells with truncated corners”

Element 6[a] is disclosed by Kobayashi combined with Hshieh. *See supra* § VIII.D.1.b.

c. 6[b]: "each of said closed cells further includes a circular trench contact hole disposed substantially in a central portion of said closed cells with a diameter of a top surface of said circuit trench contact less than 1.0 micrometer, penetrating through source regions surrounding said trenched gates and extending into body regions encompassing said source regions"

Element 6[b] is disclosed in Kobayashi. *See supra* §§ VIII.A.1.c, VIII.A.4.

d. 6[c]: "said circular trench contact comprises a hole opened from a top surface of said semiconductor substrate"

Element 6[c] is disclosed in Kobayashi. *See supra* § VIII.A.1.d.

e. 6[d]: "wherein sidewalls of said hole are surrounded by and in contact said source and body regions"

Element 6[d] is disclosed in Kobayashi. *See supra* § VIII.A.1.e.

f. 6[e]: "said circular trench contact is separate from said trenched gates with said source region and body region disposed between a gate oxide lining of said trenched gates and all circumferential points of the circular trench contact"

Element 6[e] is disclosed in Kobayashi. *See supra* § VIII.A.1.f.

g. 6[f]: "said circular trench contact hole is filled with a metal plug composed of a Ti/TiN/W plug to contact said source and body regions"

Element 6[f] is disclosed in Kobayashi. *See supra* §§ VIII.A.1.d, VIII.A.1.e., and VIII.A.2.

h. 6[g]: "said metal plug contacting a source metal disposed on top of said metal plug wherein said source metal layer composed of Ti/AlCu or Ti/AlSiCu alloys."

Element 6[g] is obvious in view of Kobayashi combined with Hshieh and Kikkawa. *See supra* §§ VIII.A.1.g, VIII.A.3, VIII.B.1, VIII.B.3, VIII.D.5.

F. Ground 6: Claim 5 is unpatentable under pre-AIA 35 U.S.C. § 103 as obvious over Kobayashi in view of Hshieh and the knowledge of a POSITA.

1. Claim 5

a. "The trenched semiconductor power device of claim 1 wherein: a diameter of a top surface of said circular trench contact is smaller than 1.0 micrometer."

Claim 5 depends from claim 1, and claim 1 is obvious over Kobayashi and Hshieh for the reasons provided above. *See supra* § VIII.D.1. Further, "wherein: a diameter of a top surface of said circular trench contact is smaller than 1.0 micrometer" would have been obvious to a POSITA based on the disclosure of Kobayashi and the knowledge of a POSITA. *See supra* § VIII.C; *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. at 421; *Nanya*, IPR2018-00063, Paper 25 at 6-7, 22-35.

IX. THE BOARD SHOULD INSTITUTE IPR

A. The asserted grounds are neither excessive nor redundant.

The six unpatentability grounds asserted herein are not excessive. *See, e.g.*, *Favored Tech Corp. v. P2i Ltd.*, IPR2020-01198, Paper 9 at 48 (Jan. 27, 2021) (instituting review and holding that asserting five distinct grounds (with no more

than three references per ground, and seven references in total) was not excessive) (distinguishing *Adaptics Ltd. v. Perfect Company*, IPR2018-01596, Paper 20 at 19 (PTAB Mar. 6, 2019)). The present Petition asserts only six grounds of unpatentability. Grounds 1 and 4 challenge claims 1, 3-5; Grounds 2 and 5 challenge claims 2 and 6; and Grounds 3 and 6 challenge only claim 5. Further, only Grounds 2, 4-6 assert more than one reference, while Ground 1 asserts Kobayashi, and Ground 3 asserts Kobayashi and the knowledge of a POSITA. Additionally, only three total references are asserted. Accordingly, the Petition is far from the "hundreds of possible combinations" of *Adaptics*. *See Favored Tech Corp.*, Paper 9 at 48.

Nor are the six grounds redundant. Ground 4 is not redundant of Ground 1 at least because Ground 4 is based on 35 U.S.C. § 103, while Ground 1 is based on 35 U.S.C. § 102. Ground 5 (based on Kobayashi, Hshieh, and Kikkawa) is not redundant of Ground 2 (based on Kobayashi and Kikkawa) because they rely on different prior art combinations. Likewise, Ground 6 is not redundant of Ground 3, as they rely on different prior art combinations. Thus, Grounds 1-6 are asserted with particularity such that discretionary denial of the petition would be improper.

B. The petition applies different art than that considered by the Office during prosecution of the '409 Patent, and so the PTAB should not exercise its discretion under 35 U.S.C. § 325(d).

None of the references cited in this Petition were presented to or cited by the Examiner during prosecution of the '409 Patent. The PTAB uses a two-part framework to determine whether to exercise its discretion under 35 U.S.C. § 325(d):

> (1) determining whether the same or substantially the same art previously was presented to the Office or whether the same or substantially the same arguments previously were presented to the Office; and (2) if either condition of [the] first part of the framework is satisfied, [determining] whether the petition has demonstrated that the Office erred in a manner material to the patentability of challenged claims.

Snap Inc. v. SRK Technology LLC, IPR2020-00820, Paper 15 at 19-20 (PTAB Oct. 21, 2020) (internal quotations omitted) (citing *Advanced Bionics, LLC v. Med-El Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 at 8 (PTAB Feb. 13, 2020) (precedential) ("*Advanced Bionics*")). Under the *Advanced Bionics* framework, the PTAB considers the non-exclusive "*Becton, Dickinson*" factors. *Becton, Dickinson & Co. v. B. Braun Melsungen AG*, IPR2017-01586, Paper 8 at 17-18 (PTAB Dec. 15, 2017) (precedential as to Section III.C.5, first paragraph) (footnote omitted) ("*Becton, Dickinson*"). Specifically, factors (a), (b), and (d) below relate to determining whether the same or substantially the same art previously was presented to the Office or whether the same or substantially the same arguments previously were presented to the Office. *Advanced Bionics* at 20. Factors (a), (b), and (d) are as follows:

> (a) the similarities and material differences between the asserted art and the prior art involved during examination; (b) the cumulative nature of the asserted art and the prior art evaluated during examination; . . . (d) the extent of the overlap between the arguments made during examination and the manner in which petitioner relies on the prior art;

Becton, Dickinson at 17-18.

Because Petitioner relies on references and arguments that are not the same (nor substantially the same) as those previously presented to the Office, there is no need to consider whether the Office erred in a material manner in step two of the *Advanced Bionics* framework. *Snap* at 28. Specifically, Kobayashi, Kikkawa, and Hshieh were not considered during original prosecution of the '409 Patent.

Further, the disclosures of these references are not substantially similar to the prior art evaluated by the examiner. For example, Kobayashi discloses truncating the corners of cells in trenched MOSFETs before rounding the corners, and further discloses a circular contact for the source trench contact. Ex. 1005, 6:29—39; Ex. 1003 ¶¶ 68, 71-73. Similarly, Hshieh discloses truncating the corners of cells in trenched MOSFETs. Ex. 1006, 5:3-28, Figure 6A—7A; Ex. 1003 ¶ 121. In addition, Kikkawa discloses teaches an AlCu / AlSiCu metal layer could have a bottom layer made of titanium (e.g., Ti or TiN) designed as both an electro- and stress-migration-resistant interconnection structure. Ex. 1007 p. 4; Ex. 1003 ¶ 85.

These references are therefore not the same (and are not substantially the same) than those considered by the Examiner during prosecution. *See Samsung*

Electronics Co., Ltd. v. Immersion Corp., IPR2018-01469, Paper 10 at 11-12 (PTAB March 7, 2019). In addition, the combinations and arguments presented herein are entirely different than any considered by the examiner during prosecution of the '409 Patent. *Samsung Electronics* at 13-14. For these reasons, Petitioner requests that the Board does not use its discretion to deny institution.

C. The *Fintiv* factors do not weigh against institution.

As explained above in Section VIII, this Petition presents compelling evidence of unpatentability, which alone warrants institution. Director Vidal, Memorandum, "Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation," at 9 (June 21, 2022) ("In summary, the PTAB will not deny institution of an IPR [] under *Fintiv* (i) when a petition presents compelling evidence of unpatentability . . . ."). Here, the grounds are straightforward and explain how Kobayashi anticipates, or how Kobayashi combined with Kikkawa and/or Hshieh render obvious <u>all</u> of the challenged claims. This evidence leads to a conclusion that one or more of the claims are unpatentable, and so the Board must decline to exercise discretion under § 314(a). *Id*.

In addition, a "holistic view" of the six *Fintiv* factors demonstrates that the Board should institute this petition. *Apple v. Fintiv*, IPR2020-00019, Paper 11 at 6 (PTAB Mar. 20, 2020) (precedential). There is only one parallel district court

litigation that involves the subject patent here (the EDTX Force Mos Action), and Petitioner is not a party to this action.

1. Factor 1 - Stay of parallel district court litigation

No party has requested a stay of litigation, and so this factor is neutral. *Fintiv*, Paper 15 at 12 (PTAB May 13, 2020) (informative).

2. Factor 2 - Proximity of the district court's trial date

This petition is being filed in October 2023, and so a final written decision ("FWD") should issue around April 2025. Petitioner is not involved in the EDTX Force Mos Action, there is no district court trial date (or projected trial date) that applies to Petitioner, and so this factor favors institution.

To the extent the Board considers the time to trial in the EDTX Force Mos Action (which does not involve Petitioner), this also does not merit discretionary denial of the Petition. The first amended complaint in the EDTX Force Mos Action included, for the first time on March 7, 2023, the '409 Patent. *See* Ex. 1010 at 7. As of March 2023, the median time to trial in the Eastern District of Texas was 19 months.[3] This would result in a trial occurring in October 2023, which is six (6) months earlier than the expected FWD. However, the EDTX Force Mos Action is still in the early stages. The parties in that case have not yet exchanged

[3] *See* "United States District Courts — National Judicial Caseload Profile," *https://www.uscourts.gov/sites/default/files/data_tables/fcms_na_distprofile0331.2023.pdf* (last accessed October 27, 2023).

proposed terms for claim construction nor filed *Markman* briefs; the court has not issued a *Markman* order; expert discovery has not begun; and substantial work remains before trial. *See* Ex. 1018. Accordingly, this factor favors institution or is neutral. *RingCentral, Inc. v. Estech Systems, Inc.*, IPR2021-00574, Paper 13 at 11–12 (PTAB Oct. 6, 2021).

3. Factor 3 - Investment in parallel proceedings

This factor favors institution because Petitioner is not involved in the parallel proceedings. In addition, the district court has not issued substantive orders related to the '409 Patent nor any claim construction orders. The EDTX Force Mos Action is still in the early stages. The parties in that case have not yet exchanged proposed terms for claim construction nor filed *Markman* briefs; the court has not issued a *Markman* order; expert discovery has not begun; and substantial work remains before trial. *See* Ex. 1018. Accordingly, this factor weighs favors institution, as the PTAB's institution can streamline the EDTX Force Mos Action. *Fintiv*, Paper 15 at 9-12.

4. Factor 4 - Overlap between the issues

Petitioner agrees not to pursue invalidity challenges in any district court case based on the same or substantially the same grounds relied upon in this Petition, and so this factor favors institution. Vidal Memorandum at 7-8.

5. Factor 5 - Petitioner is not the defendant in the parallel proceeding

This factor favors institution (or is neutral) because Petitioner is not the defendant in the parallel proceeding and is not an affiliate or subsidiary thereof. *Fintiv*, Paper 15 at 13-14. In addition, Petitioner has agreed not to pursue invalidity challenges in any district court case based on the same or substantially the same grounds relied upon in this Petition.

6. Factor 6 - Merits of Petitioner's challenge

This factor favors institution because the merits are strong, as discussed above. *Fintiv*, Paper 11 at 14–16.

X. CONCLUSION

For the foregoing reasons, Petitioner respectfully asks that *inter partes* review of the '409 Patent be instituted and claims 1-6 of the '409 Patent be cancelled.

Respectfully submitted,

Dated: October 27, 2023

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CERTIFICATE OF COMPLIANCE

I hereby certify that this brief complies with the type-volume limitations of 37 C.F.R. § 42.24, because it contains 13,079 words (as determined by the Microsoft Word word-processing system used to prepare the brief), excluding the parts of the brief exempted by 37 C.F.R. § 42.24.

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CERTIFICATE OF SERVICE

I hereby certify that on October 27, 2023, I caused a true and correct copy of the foregoing materials:

- Petition for *Inter Partes* Review of U.S. Patent No. 7,812,409 under 35 U.S.C. § 311-319 and 37 C.F.R. § 42.100 *Et Seq.*
- Exhibits 1001 – 1018
- Power of Attorney

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