

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Inergy Technology, Inc.,

Petitioner

v.

Force Mos Technology Co., Ltd.,

Patent Owner

Case No. IPR2024-00094

Patent No. 7,812,409

DECLARATION OF DAVID KUAN-YU LIU, Ph.D.

I, Dr. David Liu, declare and state as follows:

I. INTRODUCTION

1. I have been retained by Inergy Technology, Inc. (“Inergy” or “Petitioner”) as an independent expert in this *inter partes* review before the Patent Trial and Appeal Board (“PTAB”) of the United State Patent and Trademark Office. I am not an employee of Inergy or of any affiliate or subsidiary of Inergy.

2. I have been engaged to provide my opinions as to whether certain references disclose, teach, or suggest the features cited in the claims of U.S. Patent No. 7,812,409 (the ’409 Patent) and whether the claims of the ’409 Patent are unpatentable as anticipated or obvious.

3. I am being compensated at \$550.00 per hour for non-testifying work and \$600.00 per hour for testifying work, including reimbursement for reasonable and necessary out-of-pocket expenses incurred in connection to my engagement. My compensation is based solely on the amount of time that I devote to this proceeding and is in no way contingent on the nature of my findings, the presentation of my findings in testimony, or the outcome of this or any other proceeding. I have no other financial interest in this proceeding.

4. My opinion and the bases for my opinions are set forth below.

II. EDUCATIONAL BACKGROUND, PROFESSIONAL EXPERIENCE, AND OTHER QUALIFICATIONS

5. I have personal knowledge or have developed knowledge of these technologies based upon education, training, or experience, of the matters set forth herein.

6. My curriculum vitae ("CV") is attached hereto as Exhibit 1004 and provides an accurate identification of my background and experience. Among other things, my CV includes a list of my issued patents and publications for at least the last 30 years. My curriculum vitae also includes information about my expert witness experience, with case numbers where available. Below is a short summary of my professional qualifications:

7. I received a Bachelor of Science in Electrical Engineering from the University of California, Berkeley, in 1983. I received a Master of Science and Ph.D. degrees in Electrical Engineering from Stanford University in 1985 and 1989, respectively.

8. I worked on a novel Conductivity Modulated Power MOSFET for my Ph.D. thesis. The novel device uses a trench injector to facilitate an optimal tradeoff between the breakdown voltage and ON-Resistance of a Power MOSFET (Vertical DMOS) through the use of a minority carrier injector.

9. From 1989 to 1992, I was a member of technical staff at Texas Instruments, Inc. At Texas Instruments, my job responsibilities included process integration,

device modeling, high-voltage CMOS process integration, and investigating novel source-side injection mechanisms for Flash EPROM channel hot-electron programming.

10. From 1992 to 1995, I was a member of the technical staff at Advanced Micro Devices, Inc. (AMD) where I was a key contributor in optimizing Flash cell and periphery devices in AMD's CMOS-based 0.5um and 0.35um Flash EPROM technology. My job responsibilities at AMD also included process integration, device modeling, and development of triple-well process technology for accommodate x-decoder transistors and high voltage transistors for negative gate erase operation. While at AMD, I was awarded a Spotlight Award for developing a method of manufacturing a self-aligned source (SAS) etch for a NOR flash memory.

11. I spent the next five years of my career in managerial and director roles at several California-based semiconductor companies. I was responsible for increasing yield and for leading teams of engineers working to develop next-generation memory devices.

12. In 2000, I co-founded Progressant Technologies in Fremont, California. Progressant Technologies developed IP for negative differential resistance transistor technology and was eventually acquired by Synopsys, Inc.

13. From 2000 to 2004, I was a Senior Manager at Xilinx, Incorporated, where I was responsible for developing nonvolatile memory process technology for flash and CPLD product applications, as well as advanced CMOS process technology (specifically 75nm CMOS technology node, a half node version between 90nm and 65nm).

14. From 2004 to 2007, I was a Senior Scientist at Maxim Integrated Products where I was responsible for developing Embedded Non-volatile Memory process technology for Power Management product applications.

15. Since 2007, I have served as a technical consultant where I have provided expert advice regarding Flash memory technology, CMOS process technology, and semiconductor device physics.

16. I am not now, and have never been an employee of the Petitioner.

III. DOCUMENTS AND REFERENCES CONSIDERED

17. I have reviewed and considered the following documents:

Exhibit No.	Citation
1001	U.S. Patent No. 7,812, 409 (the "'409 Patent")
1002	File History of the '409 Patent
1005	U.S. Patent No. 6,888,196, Kobayashi ("Kobayashi")
1006	U.S. Patent No. 5,763,914, Hshieh et al ("Hshieh")
1007	Kikkawa, T. et al, "A Quarter-Micrometer Interconnection Technology Using a TiN/Al-Si-Cu/TiN/Al-Si-Cu/TiN/Ti Multilayer Structure," IEEE Transactions on Electron Devices, Vol. 40, No. 2, February 1993 ("Kikkawa")
1009	Complaint, <i>Force Mos Technology, Co. Ltd. v. Asustek Computer, Inc.</i> , No. 2:22-cv-00460 (E.D. Tex.)

Exhibit No.	Citation
1010	First Amended Complaint, <i>Force Mos Technology, Co. Ltd. v. Asustek Computer, Inc.</i> , No. 2:22-cv-00460 (E.D. Tex.)
1011	U.S. Patent No. 6,541,818 to Pfirsch et al. ("Pfirsch")
1012	Kim, Sang-Gi et al., "Trench Corner Rounding Technology Using Hydrogen Annealing for Highly Reliable Trench DMOSFETs," International Symposium on Power Semiconductor Devices and ICs (ISPSD), May 22-25, 2000, Toulouse France

IV. APPLICABLE LEGAL STANDARDS

18. I am not an attorney, but I have been instructed in and applied the law as described in this section.

19. It has been explained to me that a claim must be properly construed in order to be compared to prior art. My opinions regarding how a POSITA would have understood the meaning of the claims of the '409 Patent are below in Section X.

20. It has been explained to me that a claim is anticipated under Pre-AIA Section 102(b) if a prior art reference discloses each and every element of the claim, either explicitly or inherently. I understand that while the disclosed claim elements must be arranged or combined in the same way as the claim, the reference need not used the same terms to describe these claims.

21. It has also been explained to me that a claim is unpatentable for obviousness if the differences between the subject matter sought to be patented and

the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a PO.

22. I understand that the standard for determining obviousness is based on an analysis of several factual inquiries, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) when available, evidence such as commercial success, long-felt but unsolved needs, and failure of others.

23. I understand that several rationales and principles may be employed to show obviousness, including the following: (1) if a work is available in one field of endeavor, and design incentives and other market forces can prompt variations of it (either in the same field or a different one), and a person of ordinary skill can implement a predictable variation, the variation is obvious; (2) if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its application is beyond his or her skill; (3) the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results; (4) if the improvement is nothing more than the predictable use of prior art elements according to their established functions, it is likely obvious, among others.

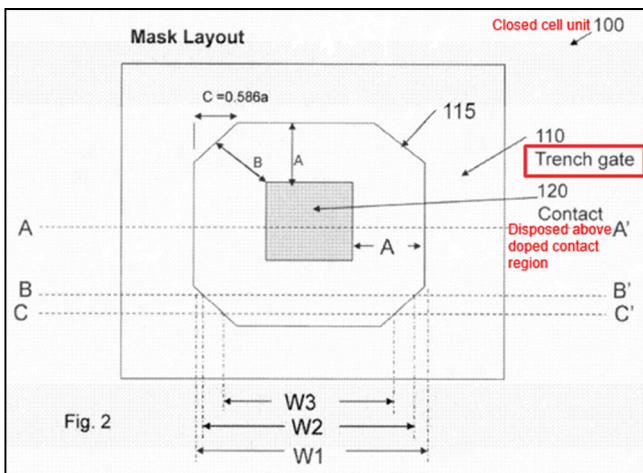
24. I also understand that when looking into interrelated teachings of multiple references, there must be a motivation to combine for the POSITA to combine the prior art references to arrive at the claimed subject matter.

25. I understand that considerations to determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent-at-issue include the effects of demands known to the design community or present in the marketplace and the background knowledge possessed by a POSITA.

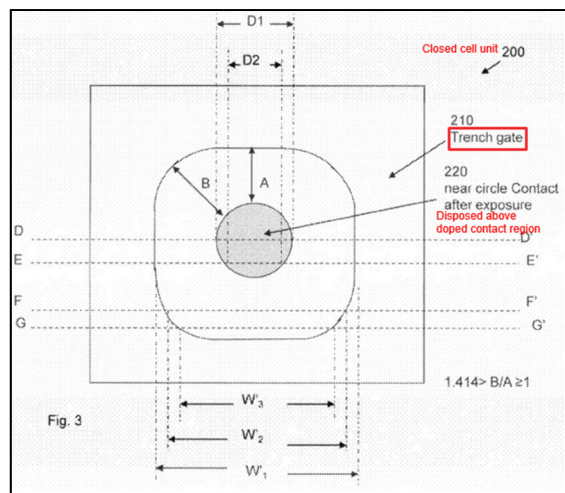
V. THE '409 PATENT

26. The '409 Patent relates to a trenched semiconductor power device. Ex. 1001, 1:7—13 (“This invention relates generally to the cell structure, device configuration and fabrication process of power semiconductor devices.”). The '409 Patent states in the “Description of the Related Art” that trenched semiconductor power devices already existed in products and disclosures. *Id.*, 1:14—17.

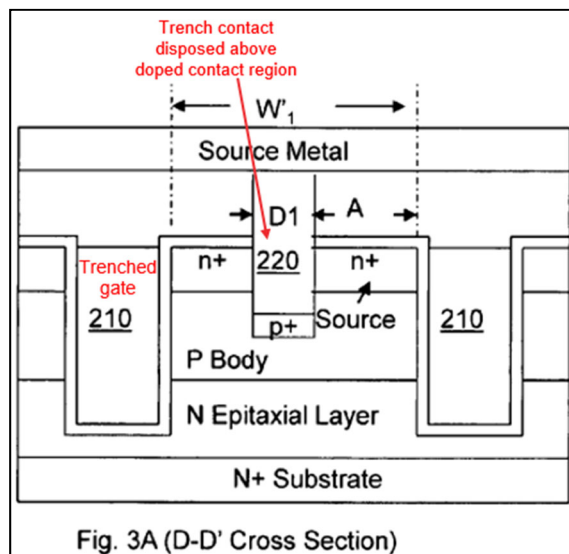
27. The '409 Patent discloses a trenched semiconductor power device with a “closed cell unit” 200/100 of a MOSFET device, which includes a trenched gate 210/110 surrounding a metal contact 220/120. The metal contact 220/120 is disposed above a doped contact region, as shown below in (annotated) Figures 2-3 and 3A of the '409 Patent. *Id.*, 4:4—7.



'409 Patent, Figure 2 (annotated)



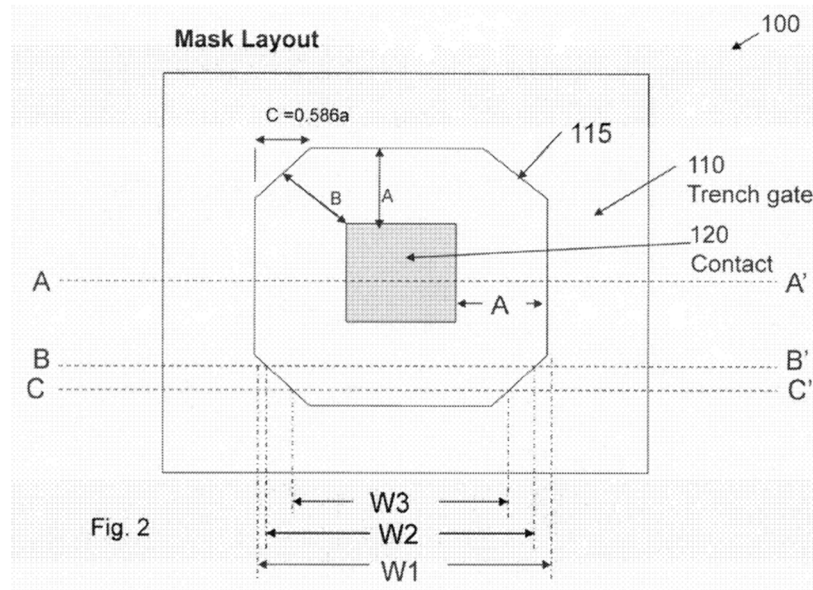
'409 Patent, Figure 3 (annotated)



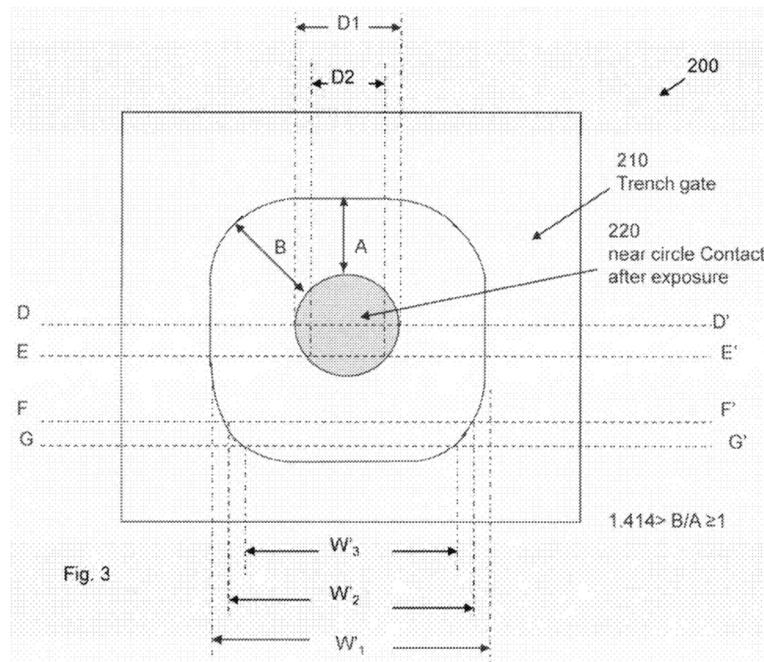
'409 Patent, Figure 3A (annotated)

28. The '409 Patent discloses closed cells designed with substantially square-shaped cells with truncated corners. *Id.*, 4:57—62; Fig. 2. The “truncated corners are formed by design layout not process.” *Id.* (showing the mask layout). During lithography, the truncated corners naturally become rounded from exposure. *Id.* (“It is by nature that truncated corners in layout as that shown in

FIG. 2 and becomes rounded as shown in FIG. 3.”). Figure 3 also shows that the square contact 120 (Fig. 2) naturally becomes a circular shaped contact 220 (Fig. 3) after exposure. *Id.*, 4:53—57.

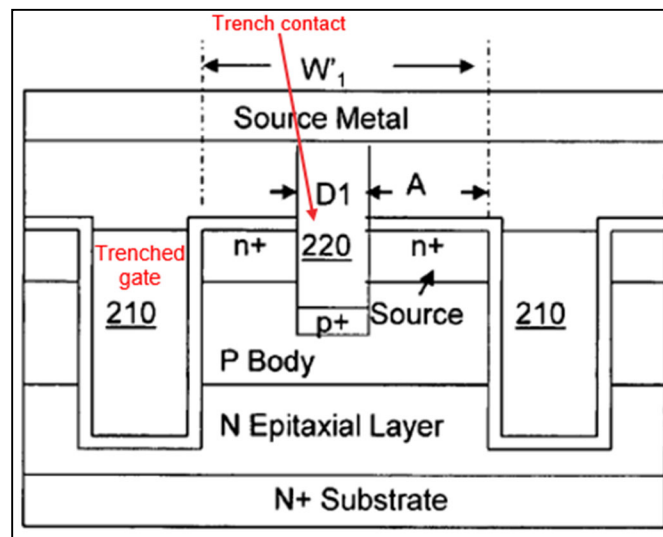


'409 Patent, Figure 2



'409 Patent, Figure 3

29. The '409 Patent discloses a circular trench contact 220 that is “extended into the body region through the source region of the closed semiconductor power cell” and is “in contact with a p⁺ contact dopant region disposed immediately below the [circular] trench contact.” *Id.*, 4:25—33, Fig. 3A. Meanwhile, the trenched gates 210 and the gate oxide lining of the trenched gates 210 are disposed at a distance away from the circular trench contact 220. *Id.* The source and body regions are disposed between the gate oxide lining and all circumferential points of the circular trench contact 220. *Id.* The source and body regions are in contact with the circular trench contact 220. *Id.*



'409 Patent, Figure 3A (annotated)

30. Finally, the circular trench contact 220 is filled with a contact metal plug that is connected to a source metal. *Id.*, Figure 3A; 5:26—27; *see also id.* Fig. 1C.

VI. STATE OF THE ART

31. At the effective filing date of the '409 Patent, December 4, 2006, a POSITA would know that the development of MOSFET, and specifically Power MOSFET, focuses on the tradeoff between minimizing the ON-Resistance and maximizing the breakdown voltage capability, for a given device area.

32. The key evolutionary advancement of the MOSFET involves going from a planar DMOS (Double-Diffused MOS) to a trench MOSFET, where the gate and its associated channel of the transistor is folded vertically onto a trench into the silicon. While the use of trench Power MOSFET reduces the ON-Resistance significantly through the reduction of the JFET component, the dopant profile optimization of the body region and the drift region continues to be the key feature in this optimization effort.

33. However, even for well-designed doping profiles in the drift region (N-region) and the body region (P-region) in an N-channel MOSFET that minimize the channel resistance (R_{ch}) and achieve a target avalanche breakdown voltage strength, the breakdown voltage capability could nonetheless be degraded due to the phenomena of punch-through of the body region between the drain and the source.

34. This punch-through behavior comes from the existence of a parasitic bipolar transistor (N-P-N) that forms between the drift region (collector of the N-P-

N bipolar transistor), P-base region (base of the NPN bipolar transistor), and the N⁺ source region (emitter of the NPN bipolar transistor). Any current that is generated from the reverse biased P-N junction (the junction between drift region and the body region) can trigger the lowering of the barrier between the drain and source of the transistor in the off-state, through the turning on of the base emitter junction of the parasitic bipolar transistor, and causes premature breakdown or conduction of the device even before the target avalanche breakdown voltage is reached.

35. Thus, while most of the work in the field at this time focused on optimizing the doping profiles of the body region and the drift region, a significant portion of the said efforts also focused on the doping profile around the source/body contact in order to generate a low resistive ohmic contact to connect both the N⁺ source and the P- body of the transistor.

36. With the further evolution of using a trenched source contact to contact both the source region and the P body region, the doping profiles of the body surrounding both the sides and the bottom of the trench have significant impact on the resistivity of the ohmic contacts required to connect both the source and the body.

37. Given that all these device design consideration were taken into account at the time of the '409 patent application (December 4, 2006) there were

additional process and layout efforts being made to remove or alleviate any geometrical features that could magnify the detrimental effects that lead to premature punch-through breakdown of the device. An area of improvement was identified to be the elimination of sharp features at the corner of the device, either in planar direction or in the vertical direction, since it is known that sharp corner features tend to reach a higher peak electric field for a given sustained voltage.

VII. THE FILE HISTORY OF THE '409 PATENT

38. When the '409 Patent was filed as a patent application, original claims 1 and 13 (which eventually became the current claims 1 and 6, respectively) were initially presented as shown below.

1. A trench semiconductor power device comprising a trench gate disposed in an extended continuous trench surrounding a plurality of transistor cells, wherein:

said trench gate surrounding said transistor cells as closed cells with truncated corners.

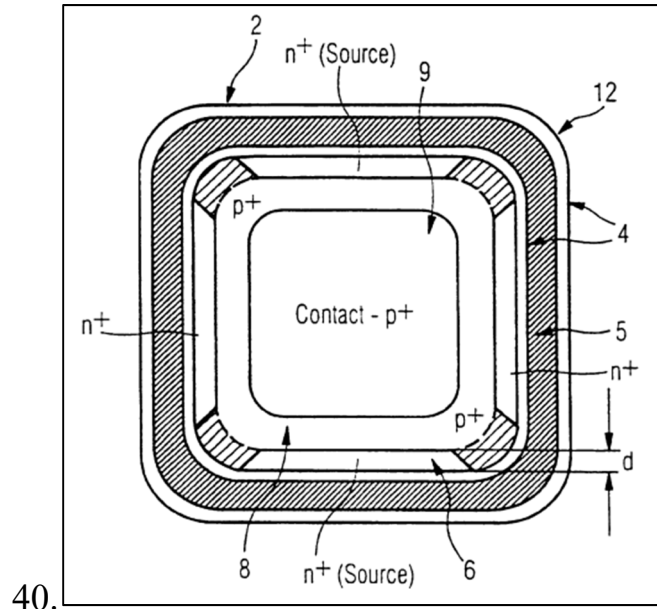
'409 Patent File History - Original Claim 1 (Ex. 1002 at p. 361)

13. A trench semiconductor power device comprising a trench gate disposed in an extended continuous trench surrounding a plurality of transistor cells, wherein:

said trench gate surrounding said transistor cells as closed cells with rounded corners.

'409 Patent File History - Original Claim 13 (Ex. 1002 at p. 363)

39. On January 26, 2009 (Ex. 1002 at p. 307), the USPTO issued an Office Action, rejecting claims 1-13 (Ex. 1002 at p. 308). The examiner stated that “Claims 1 and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Pfirsch et al. (U.S. Patent No. 6,541,818, from hereinafter ‘Pfirsch’).” Ex. 1002 at p. 309. Provided below is Figure 2 of Pfirsch, which is a top down view of a closed cell, showing a substantially square cell with rounded corners having a source contact also with rounded corners:



Pfirsch Fig. 2

41. On April 15, 2009 (Ex. 1002 at p. 293), the Applicant submitted an amendment and response to the Examiner’s Action from January 26, 2009. Ex. 1002 at p. 293. In the Applicant’s amendment, original claims 1 and 13 were amended as shown below.

1.(Currently Amended) A trench semiconductor power device comprising a trench gate disposed in an extended continuous trench surrounding a plurality of transistor cells, wherein:

- said trench gate surrounding said transistor cells as closed cells constituting substantially square-shaped cells with truncated rounded corners;

each of said closed cells further includes a circular trench contact hole disposed substantially in a central portion of said closed cells, penetrating through a source regions surrounding said trench gates and extending into body regions encompassing said source regions;

said circular trench contact hole filled with a contact metal plug to contact said source and body regions; and

said contact metal plug connected to a source metal disposed on top of said circular trench contact hole.

'409 Patent File History - Amended Claim 1 (Ex. 1002 at p. 295)

13. (Currently Amended) A trench semiconductor power device comprising a trench gate disposed in an extended continuous trench surrounding a plurality of transistor cells, wherein:

said trench gate surrounding said transistor cells as closed cells constituting substantially square-shaped cells with rounded truncated corners.

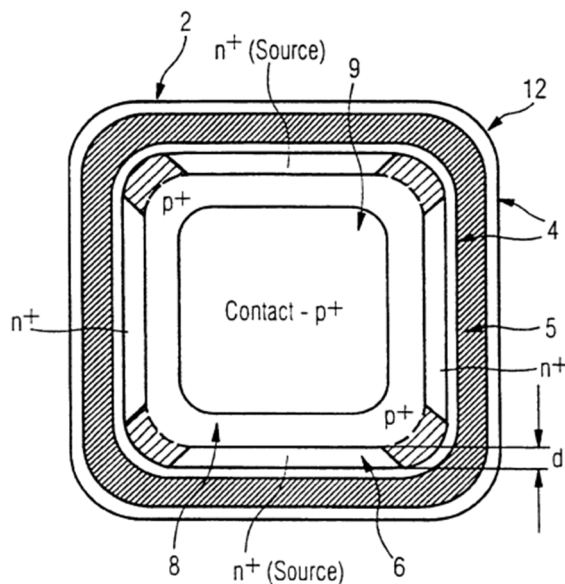
each of said closed cells further includes a circular trench contact hole disposed substantially in a central portion of said closed cells with a diameter at a top of said contact holes less than 1.0 micrometer, penetrating through source regions surrounding said trench gates and extending into body regions encompassing said source regions;

said circular trench contact hole filled with a metal plug composed of a Ti/TiN/W plug to contact said source and body regions and said metal plug contacting a source metal disposed on top of said metal plug wherein said source metal layer composed of Ti/AlCu or Ti/AlSiCu alloys.

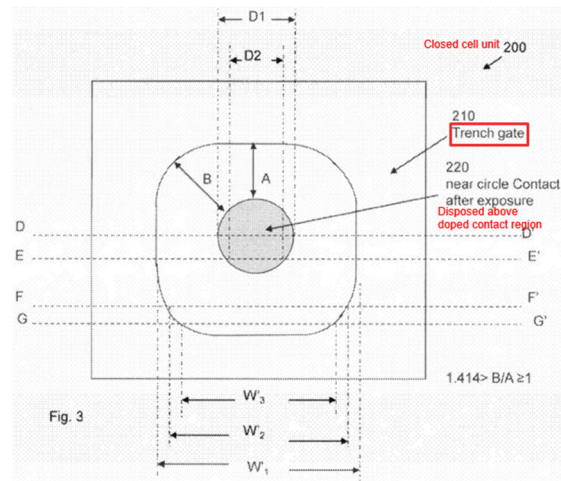
'409 Patent File History - Amended Claim 1 (Ex. 1002 at p. 299)

42. The Applicant stated that these amendments were made in response to the Pfirsch rejection. Ex. 1002 at p. 302. In the Applicant's remarks, the Applicant emphasized that certain structural features have not been shown or suggested by Pfirsch, specifically the circular trench contact hole disposed in the center of a square-shape closed cell with rounded corners or truncated corners as shown in Figure 3 of the application for the '409 Patent. *Id.*

43. Figure 3 of the '409 Patent and Figure 2 of Pfirsch are provided below.



Pfirsch et al Figure 2



'409 Patent Figure 3 (annotated)

44. The key differences between these closed cells are two-fold: (1) the Pfirsch design has a square contact with rounded corners (apparently rounded

through natural rounding), while the '409 Patent has a circular contact; and (2) the Pfirsch cells are designed to be square cells (which apparently have undergone some natural rounding) while the '409 Patent's cells are designed to be rounded by truncating the corners and then the truncated corners undergo natural rounding during lithography.

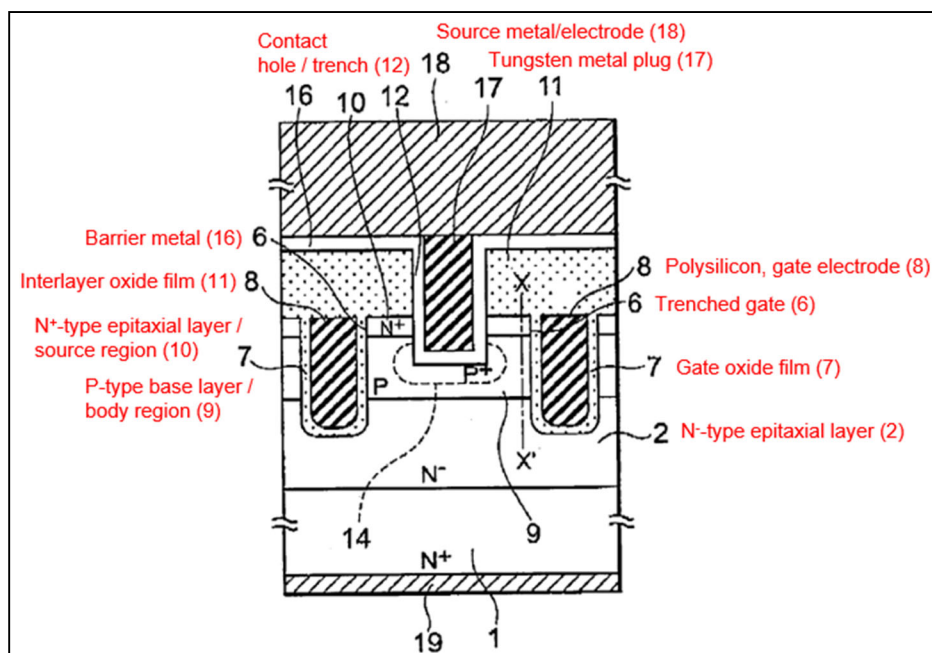
45. I understand that original claims 1 and 13 eventually issued as claims 1 and 6, respectively, in the '409 Patent, and so I have considered these distinctions over Pfirsch in relation to current claims 1 and 6.

VIII. OVERVIEW OF THE PRIOR ART

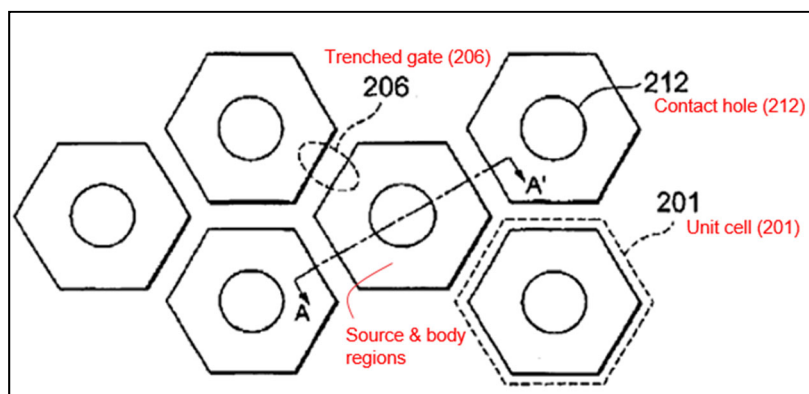
A. U.S. Patent No. 6,888,196 ("Kobayashi")

46. I understand that U.S. Patent No. 6,888,196 to Kobayashi ("Kobayashi") issued on May 3, 2005. Ex. 1005. It has been explained to me that Kobayashi is prior art at least under pre-AIA 35 U.S.C. § 102(b) and that Kobayashi was not considered during the prosecution of the '409 Patent.

47. Kobayashi discloses a trenched semiconductor power device. Ex. 1005, Figs. 3, 4A.



Kobayashi, Figure 3 (Annotated)

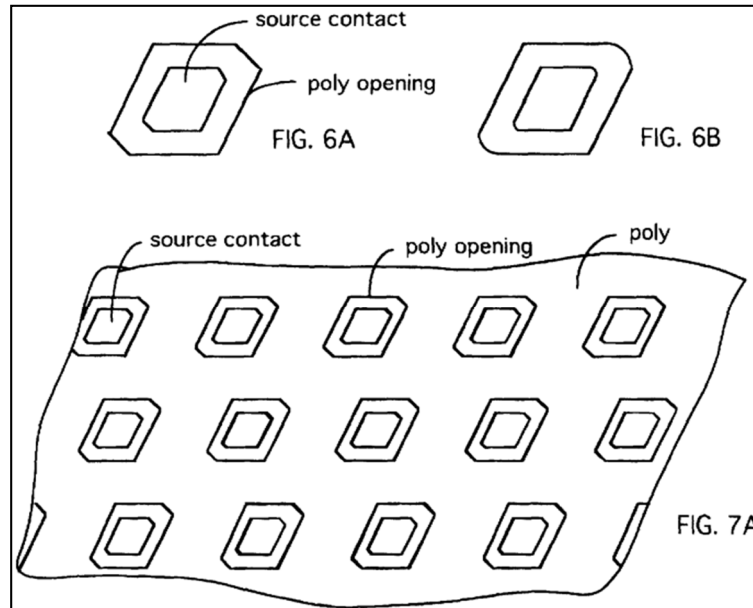


Kobayashi Fig. 4A (annotated)

B. U.S. Patent No. 5,763,914 (“Hshieh”)

48. I understand U.S. Patent No. 5,763,914 to Hshieh et al. (“Hshieh”) was issued on June 9, 1998. Ex. 1006. It has been explained to me that Hshieh is prior art at least under pre-AIA 35 U.S.C. § 102(b) and that Hshieh was not considered during the prosecution of the ’409 Patent.

49. Hshieh discloses trenchless semiconductor power devices. Ex. 1006, Figs. 6A—7A.



Hshieh, Figures 6A, 6B, 7A

C. Kikkawa

50. “A Quarter-Micrometer Interconnection Technology Using a TiN/Al-Si-Cu/TiN/Al-Si-Cu/TiN/Ti Multilayer Structure,” by Kikkawa, T. et al, IEEE Transactions on Electron Devices, Vol. 40, No. 2 (“Kikkawa”) was published and made publicly available in February 1993. Ex. 1007. It has been explained to me that Kikkawa is prior art under at least pre-AIA 35 U.S.C. § 102(b) and that Kikkawa was not considered during the prosecution of the ’409 Patent.

51. Kikkawa describes structures for semiconductor devices. Ex. 1007.

IX. THE QUALIFICATIONS AND BACKGROUND OF THE PERSON OF ORDINARY SKILL IN THE ART

52. A person of ordinary skill in the art (“POSITA”) of the subject matter of the ’409 Patent at the filing date of the ’409 Patent (December 4, 2006) would have a master’s degree in electrical engineering, and at least two years of relevant work experience in the field of integrated circuit design and manufacturing.

X. CLAIM CONSTRUCTION

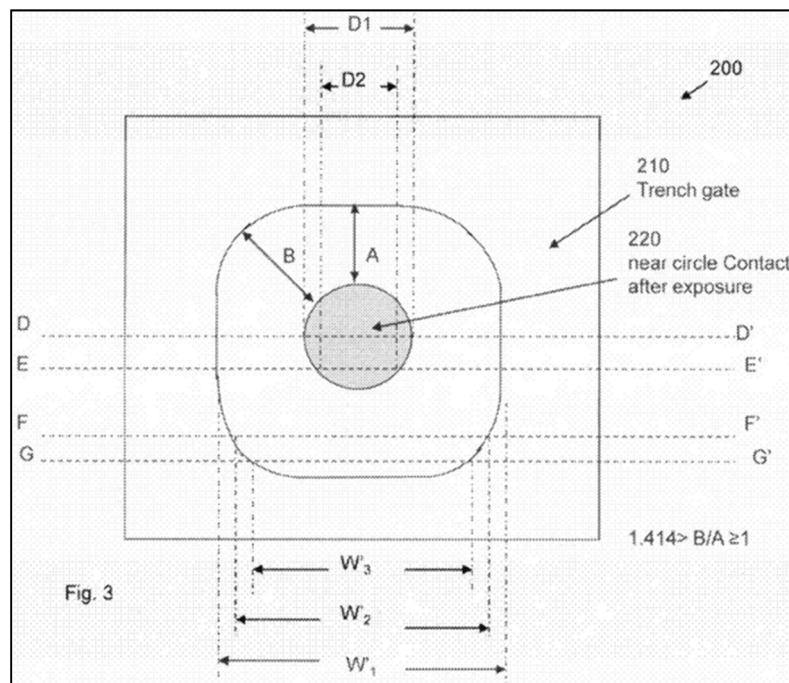
53. I understand claim terms are generally given their ordinary and customary meaning that the term would have to a POSITA.

54. I also understand that because the meaning of a claim term as understood by a POSITA is often not immediately apparent, and because patentees frequently use terms idiosyncratically, the court looks to public sources that show what a person of skill in the art would have understood disputed claim language to mean. I understand those sources include the “intrinsic evidence”, *i.e.*, the patent itself, including the claims, the specification and, if in evidence, the prosecution history (or file history).

A. “Rounded corners” (claim 1)

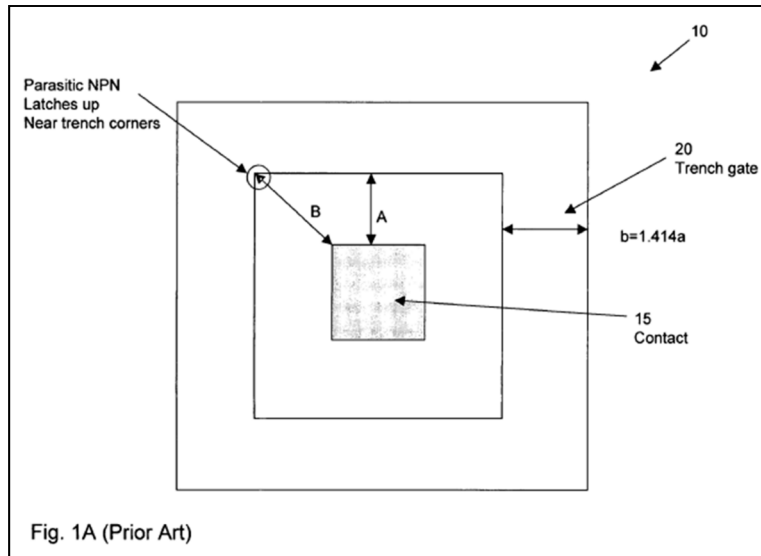
55. Based on the context of the claims, the disclosures of the ’409 patent, and the file history of the ’409 Patent, a POSITA would understand that the term “rounded corners” means “corners that are truncated by design layout and then rounded.” The ’409 Patent shows rounded corners in Figure 3. Ex. 1001, 2:10-20;

4:53-64. The '409 file history describes “rounded corners” as “structural features”. Ex. 1002 at 302. Similarly, the '409 Patent explains that the truncated corners are formed by design layout to later form “rounded corners” in Figure 3. Ex. 1001, 2:10-20; 4:53-64. The truncated corners become rounded corners as a result of exposure during photolithography. *Id.*



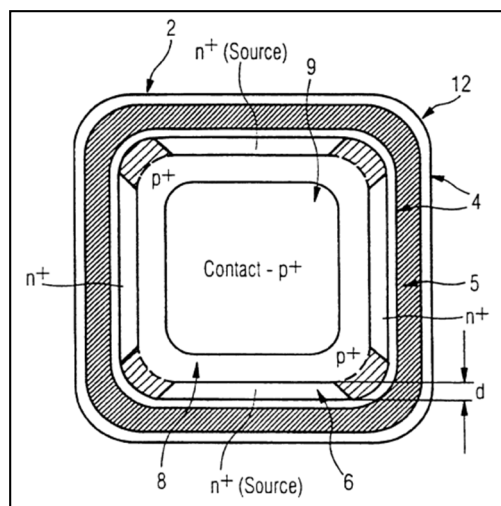
'409 Patent Figure 3

56. I also understand that Figure 1A in the '409 Patent discloses prior art. Figure 1A shows a square-shaped mask layout of a trench gate. The mask layout is square-shaped by design that was well known in the art at the time the '409 Patent was filed (Dec. 4, 2006). It was also well known in the art that the corners would become rounded as a natural or incidental result of lithography.



'409 Patent Figure 1A (Admitted Prior Art)

57. I also understand that claim 1 was amended during prosecution. I understand that the claim term “rounded corners” was added to distinguish the '409 Patent from the Pfirsch reference shown below. *See also supra* ¶¶ 38—45. The Pfirsch “has a closed cell with ***square trench gate with rounded corner . . .*** as shown in Fig. 2 . . . in Pfirsch.” Ex. 1002 at 302 (emphasis added).

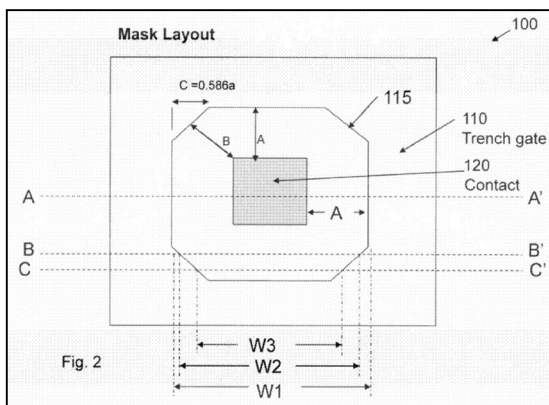


Pfirsch Fig. 2

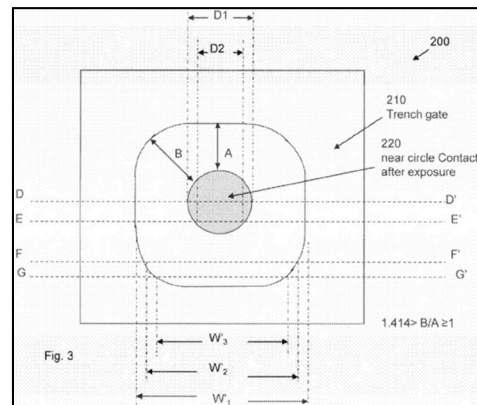
58. It follows that a POSITA at the time of the filing of the '409 Patent (Dec. 4, 2006) would have understood “rounded corners” to mean corners that are *truncated by design and subsequently rounded by lithography*. In contrast, a POSITA would not have understood the “rounded corners” in claim 1 to mean *naturally or incidentally rounded corners of a square cell*. Therefore, a POSITA would understand the “rounded corners” of claim 1 as “corners that are truncated by design layout and then rounded.”

B. “Truncated corners” (claim 13)

59. Based on the context of the claims, the disclosures of the '409 Patent, and the file history of the '409 Patent, a POSITA would understand that the term “truncated corners” means “corners that are truncated by design layout.” The '409 Patent shows truncated corners in Figures 2 and 3. Ex. 1001, 2:10-20; 4:53-64. The '409 patent explains that the “truncated corners are formed by design layout not process.” Ex. 1001, 4:57-58.



'409 Patent, Figure 2



'409 Patent, Figure 3

60. I understand that the Applicant for '409 Patent characterized the “truncated corners in the amended claim 13” as “structural features” of the '409 Patent. Ex. 1002 at 302; *see also supra* ¶¶ 38-45. The '409 Patent further explains that the truncated corners are formed by the truncated mask design layout of Figure 2 and thereafter rounded through natural processes to form the rounded corners in Figure 3. Ex. 1001, 2:10-20; 4:53-64.

61. I also understand that the Applicant for the '409 Patent distinguished prior art that include trenched gates with square-shaped designs that become rounded during the lithography process during prosecution. *See also supra* ¶¶ 38-45. Therefore a POSITA would not understand the “truncated corners” in the '409 Patent to refer to corners of a square-shaped layout that are incidentally or naturally altered or truncated. The “truncated corners” instead refer to corners that are truncated by design. A POSITA would understand that the “truncated corners” of claim 13 as “corners that are truncated by design layout.”

XI. OPINIONS AS TO INVALIDITY OF THE '409 PATENT

A. Claims 1, 3–5 are unpatentable under pre-AIA 35 U.S.C. § 102(b) as anticipated by Kobayashi.

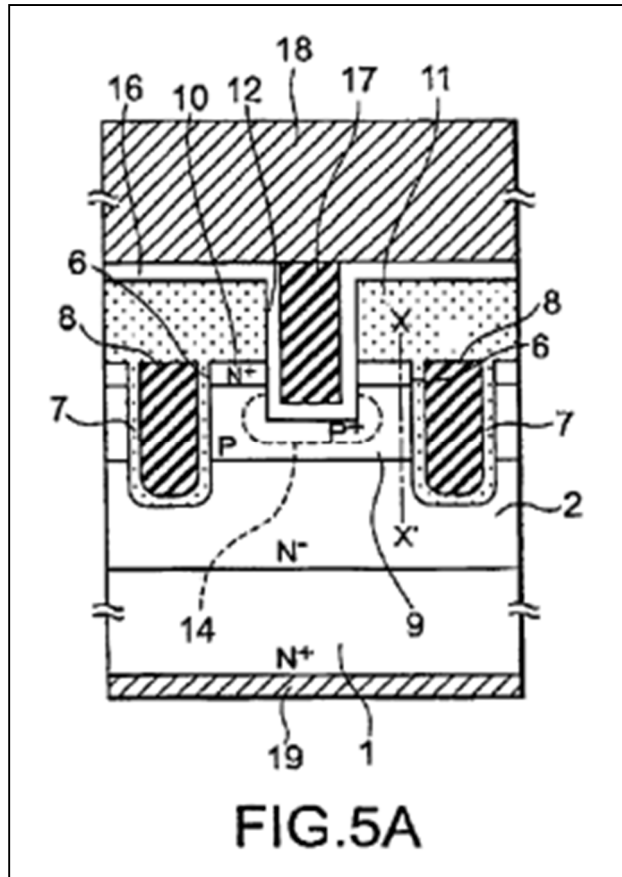
62. Claims 1–6 of the '409 Patent are unpatentable under pre-AIA 35 U.S.C. § 102(b) as anticipated by Kobayashi.

1. Claim 1

63. Kobayashi discloses and anticipates every limitation of claim 1.

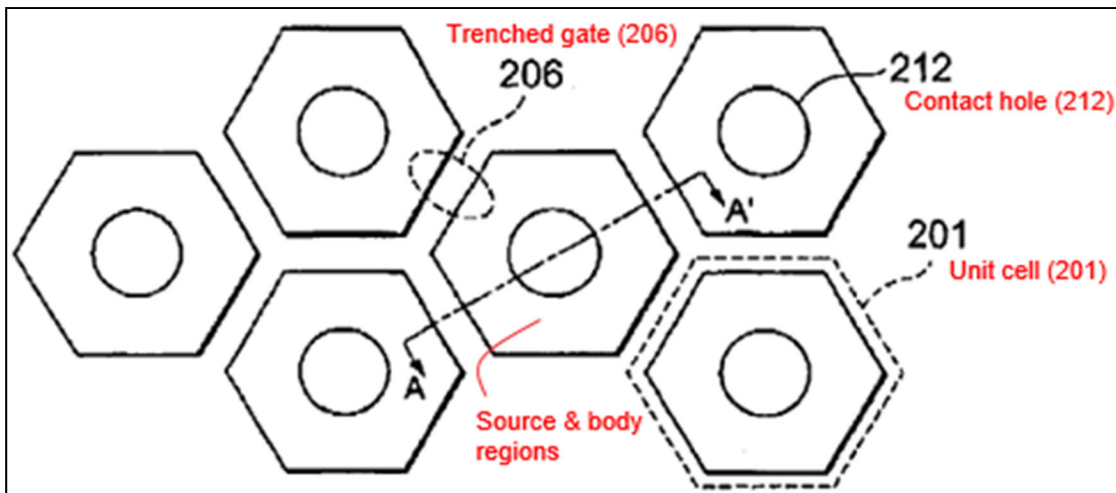
- a. **1 [preamble]: “A trench semiconductor power device comprising a plurality of trench gates surrounding a plurality of transistor cells formed in a semiconductor substrate, wherein:”**

64. The preamble is disclosed in Kobayashi. Kobayashi discloses a trench semiconductor power device with a plurality of trench gates surrounding a plurality of transistor cells formed in a semiconductor substrate. More specifically, Kobayashi discloses “[a] vertical MOSFET (or a UMOSFET) comprising: a semiconductor layer (1, 2, 9, 10) having first and second surfaces opposite to each other and a pair of trenches (6) formed on the first surface” Ex. 1005, 4:12—15, Fig. 5A. The semiconductor layer is comprised of an N⁺-type silicon substrate 1, an N⁻-type silicon substrate 2, a P-type base layer 9, and an N⁺-type source layer. Ex. 1001, 6:46—67. The pair of trenches (6) reach “the N⁻-type epitaxial layer 2 through the P-type base layer”. *Id.*, 6:53—55. The trenches (6) further surround the unit cell. *Id.*, 4:12—19.



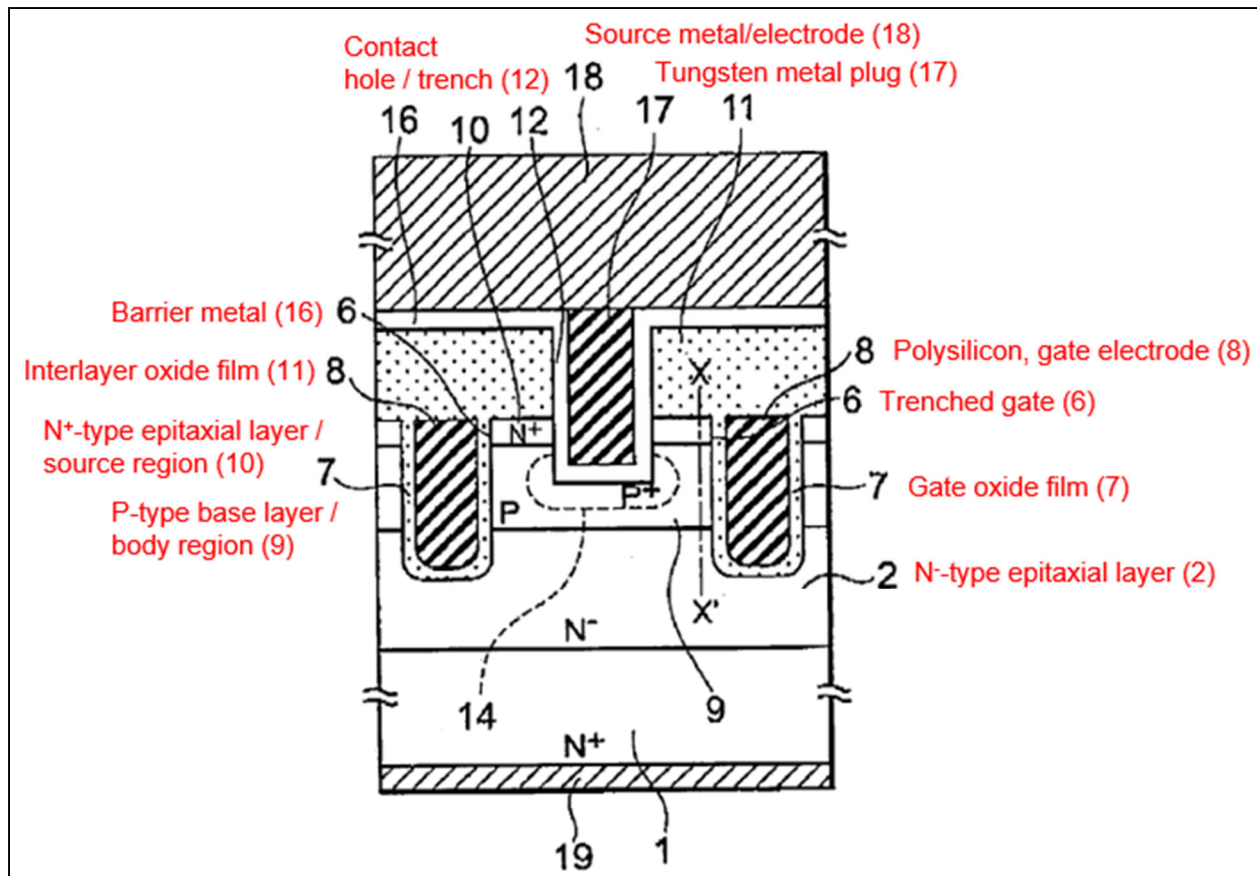
Kobayashi Figure 5A

65. Kobayashi discloses multiple unit cells separated by multiple trenches in Figure 4A. More specifically, the “unit cells 101, 201, and 301 in each figure can be defined as structural units separated by trenches 106, 206, and 306 where gate electrodes are to be formed. At the centers of the unit cells 101, 201, and 301, contact holes 112, 212, and 312 are disposed, respectively.” Ex. 1005, 6:29—37.



Kobayashi, Figure 4A (annotated)

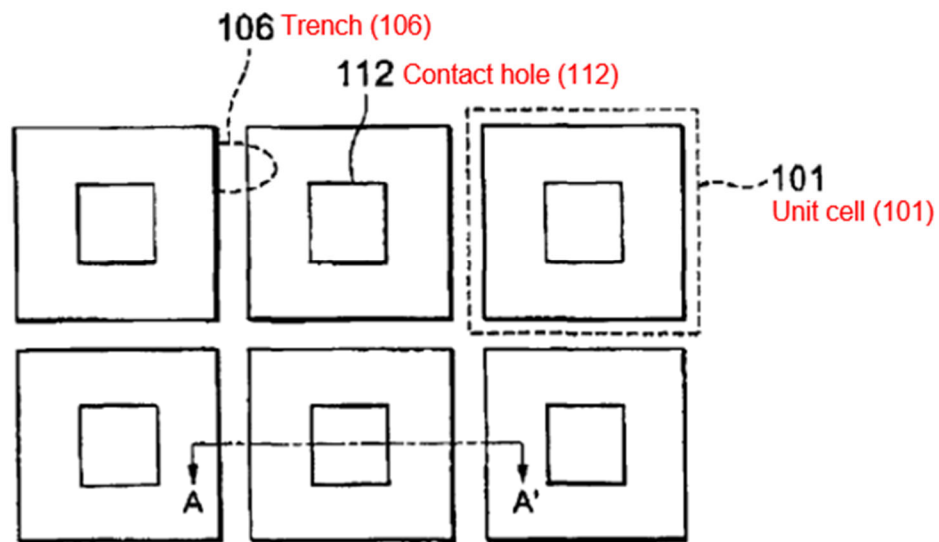
66. Kobayashi further discloses “[a] combination of the substrate 1 and the layers 2, 9, and 10 constitutes a silicon layer having silicon surface opposite to each other.” Ex. 1005, 6:51—53. Each of trenches 6 reach “the N⁻-type epitaxial layer 2 through the P-type base layer 9, [and] a gate oxide film 7 and a polysilicon 8 are filled.” Ex. 1005, 6:53—56. In addition, “The contact holes may have any desired shape, such as a square shape, a hexagonal shape, an octagonal shape, and a circular shape. If the contact hole is sufficiently small, the contact hole has a generally circular shape without any angle, although depending upon the resolution of the photolithography.” Ex. 1005, 6:37—42.



Kobayashi, Figure 5A (annotated)

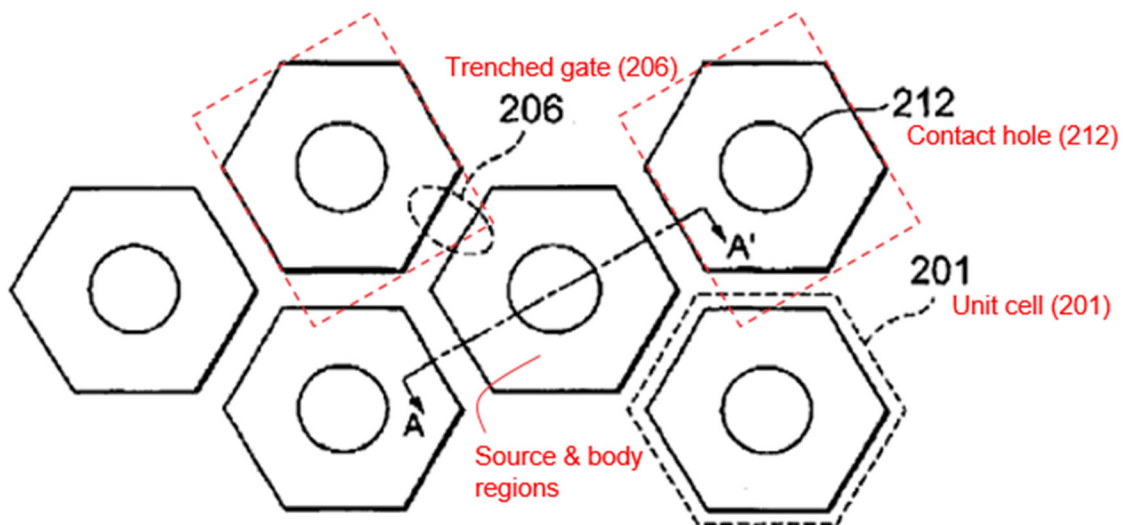
- b. 1[a]: “said trenched gates surrounding said transistor cells as closed cells constituting substantially square-shaped cells with rounded corners;”

67. Element 1[a] is disclosed by Kobayashi. Kobayashi discloses “a plurality of *square cells* [that] are arranged in a matrix” in Figure 3A. Ex. 1005, 6:26—27 (emphasis added).



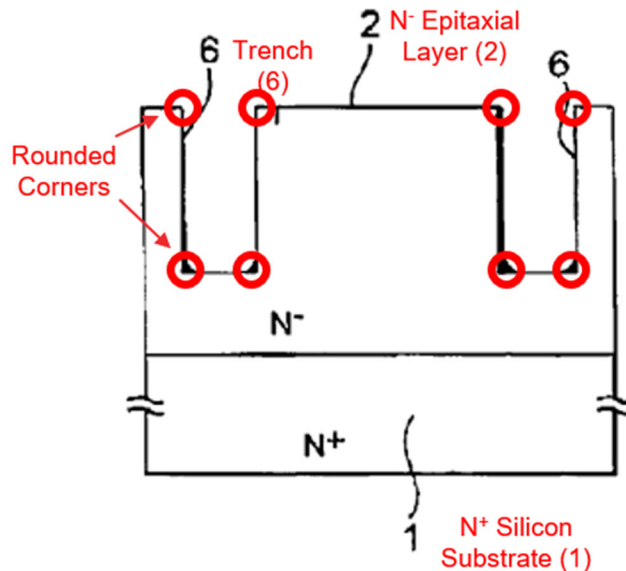
Kobayashi, Figure 3A (annotated)

68. Kobayashi shows “a plurality of hexagonal cells” which can be described as square-shaped cells with truncated corners in Figure 4A. Ex. 1005, 6:30.



Kobayashi, Figure 4A (annotated)

69. Kobayashi shows, in Figure 6C, that the “corners of each trench 6 at the bottom are rounded [and] corners of each trench 6 at an opening portion may also be rounded” Ex. 1005, 7:57—8:4.



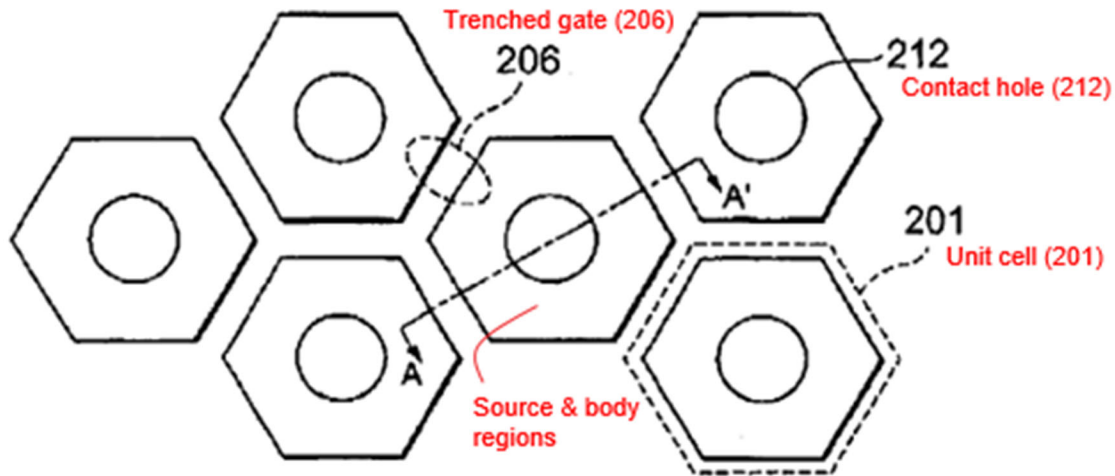
Kobayashi, Figure 6C (annotated)

70. Therefore, Kobayashi discloses closed cells that are substantially square shaped with rounded corners that are formed by truncating the corners by design and then naturally or incidentally rounded by process.

- c. **1[b]: “each of said closed cells further includes a circular trench contact disposed substantially in a central portion of said closed cells, penetrating through a source region surrounding said trenched gates and extending into a body region encompassing said source region;”**

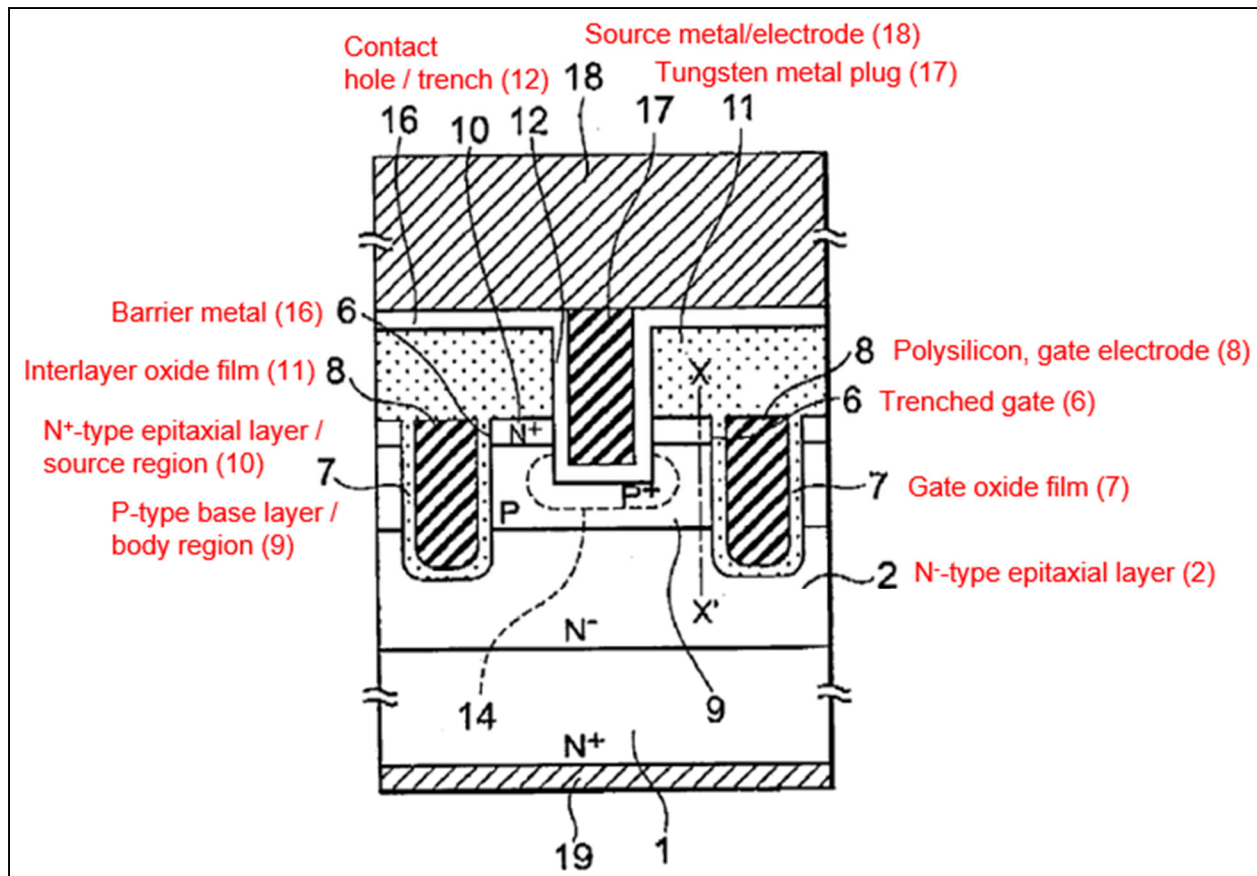
71. Element 1[b] is disclosed in Kobayashi. Kobayashi discloses closed cells that include circular trench contacts 212. Ex. 1005, 6:29—39. Kobayashi

shows a circular trench contact 212 that is disposed substantially in a central portion of the closed cell 201 in Figure 4A.



Kobayashi, Figure 4A (annotated)

72. Kobayashi further described a trench contact 12 that is “is formed to reach the P-type base layer 9 through the N⁺-type source layer 10.” Ex. 1005, 6:58—60. Kobayashi shows that the circular trench contact 12 penetrates through a source region 10 surrounding trapezoidal gates 6 in Figure 5A. Ex. 1005, 6:46—67.



Kobayashi, Figure 5A (annotated)

73. Kobayashi also shows that the trench contact 12 extends into a P-type body region. Ex. 1005, Fig. 5A. The P-type body region encompasses the source region 10. Ex. 1005, 6:46—67, Fig. 5A.

- d. **1[c]: “said circular trench contact comprises a hole opened from a top surface of said semiconductor substrate and is filled with a contact metal plug”**

74. Element 1[c] is disclosed in Kobayashi. Kobayashi, in Figures 4A and 5A, shows that the circular trench contact is “a contact hole 12 having a predetermined length formed to reach the P-type base layer 9 through the N⁺-type source layer 10” from a top surface. Ex. 1005, 6:58-60. Kobayashi further

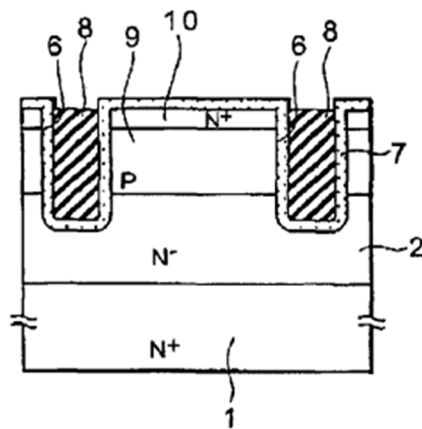


FIG. 7A

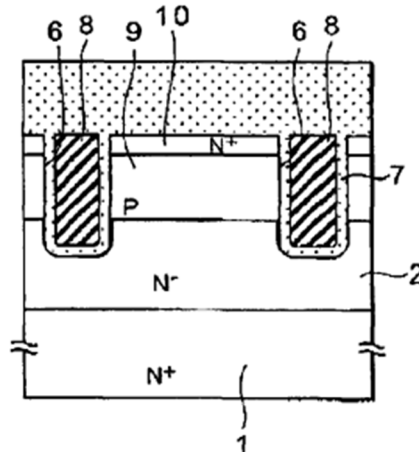


FIG. 7B

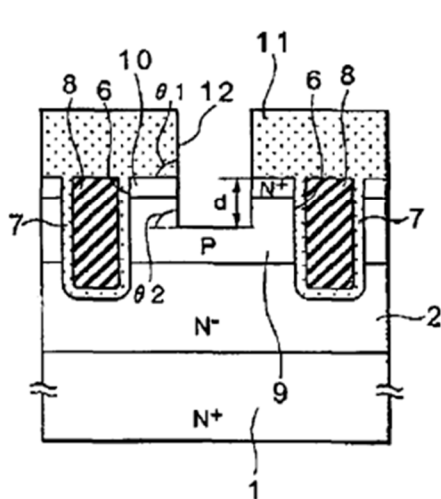


FIG. 7C

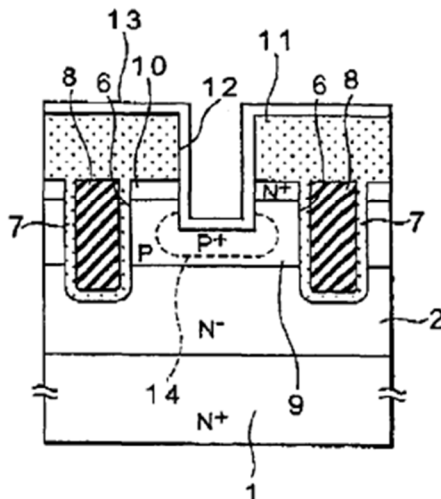
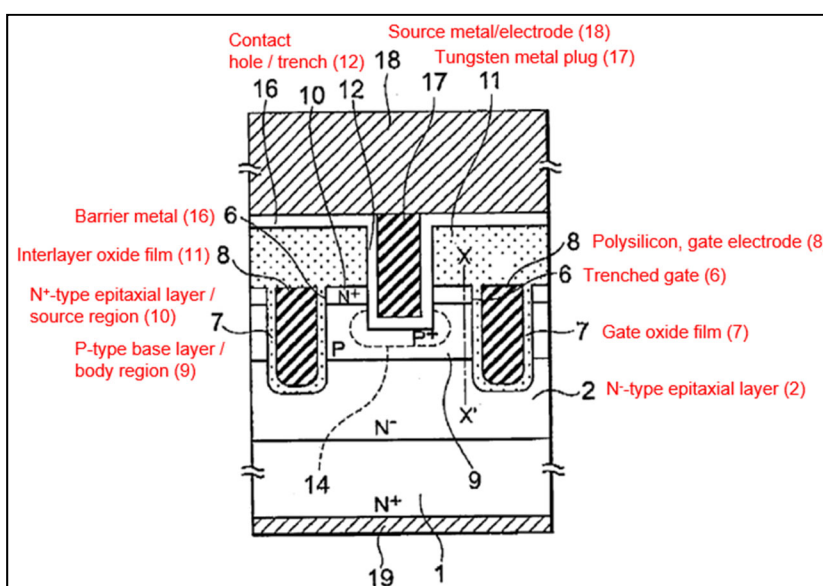
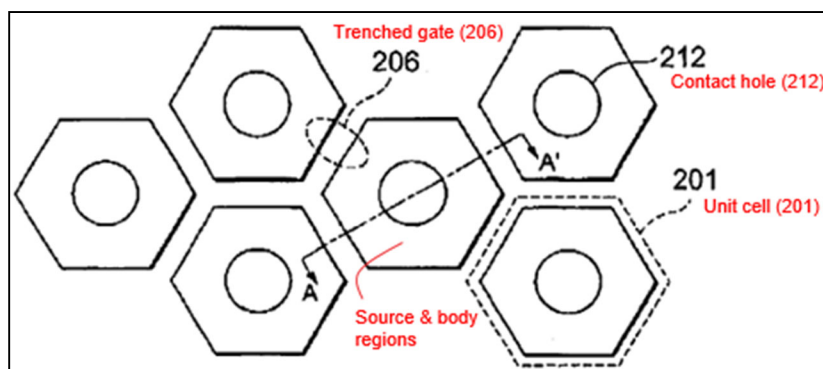


FIG. 7D

Kobayashi, Figure 7A—7D

- e. 1[d]: “wherein sidewalls of said hole are surrounded by and in contact said source and body regions”

75. Element 1[d] is disclosed in Kobayashi. Kobayashi shows that the sidewalls of contact hole 12 are surrounded by and in contact with the source 10 and body 9 regions in Figures 4A and 5A.

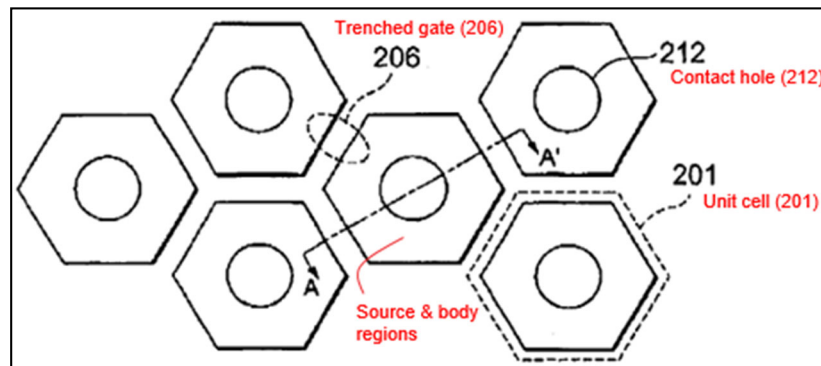


f. 1[e]: “and said circular trench contact is separate from said trenched gates with said source region and body region disposed between a gate oxide lining of said trenched gates and all circumferential points of the circular trench contact;”

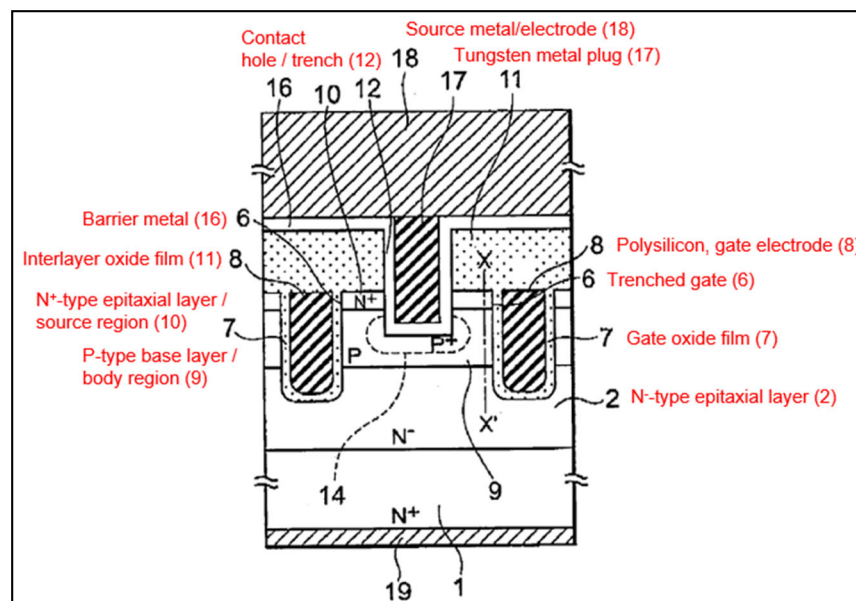
76. Element 1[e] is disclosed in Kobayashi. Kobayashi shows a circular trench contact 12, 212 in Figures 4A and 5A. The circular trench contact 12, 212 “is formed to reach the P-type base layer through the N⁺-type source layer 10” and

is separate from the trench gates 6. Ex. 1005, 6:59—60; Fig. 5. The trench gates are filled with a gate oxide film 7 and a polysilicon 8. Ex, 1005, 6:53—56.

The source 10 and body 9 regions are disposed between the gate oxide film 7 of the trench gates 6 and all circumferential points of the contact hole 12, 212. Ex. 1005, Fig. 5A.



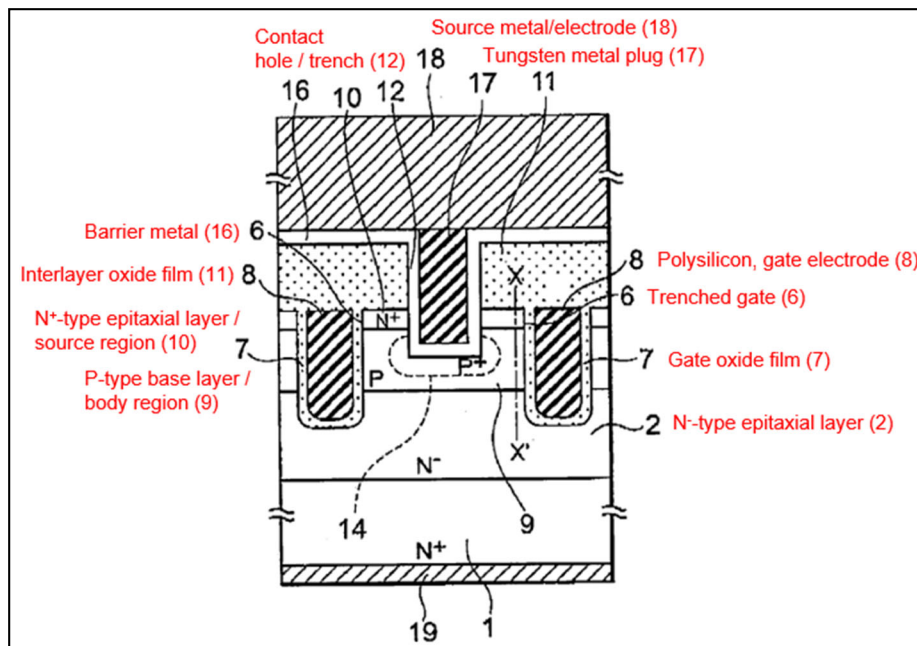
Kobayashi, Figure 4A (annotated)



Kobayashi, Figure 5A (annotated)

- g. 1[f]: “and said contact metal plug connected to a source metal disposed on top of said circular trench contact.”

77. Element 1[f] is disclosed in Kobayashi. Kobayashi shows that a source electrode 18 is formed “on the surface of the [tungsten plug] 17 and the barrier metal 16” in Figure 5A. Ex. 1005, 6:64—67. More specifically, the source electrode 18 is deposited by sputtering AlSi (aluminum silicon or AlSiCu (aluminum copper silicon). Ex. 1005, 9:36—38.

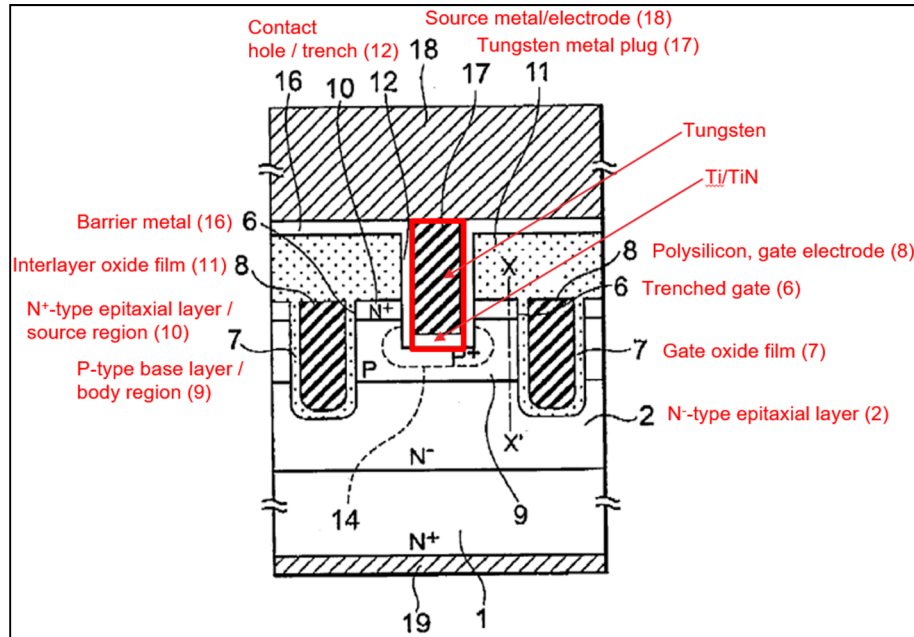


Kobayashi, Figure 5A (annotated)

2. Claim 3

- a. “The trenched semiconductor power device of claim 1 wherein: said contact metal plug disposed in said hole of said circular trench contact further comprising a Ti/TiN/W metal plug.”

78. Claim 3 is disclosed in Kobayashi. Kobayashi shows that a contact metal plug 17 is disposed in a circular trench contact 12 in Figure 5A (*see supra* § XI.A.1.c—d). Kobayashi also discloses a contact metal plug 17 with W (Tungsten) deposited on top of Ti (Titanium) and TiN (Titanium Nitride) within the circular trench contact 12. Ex. 1005, 9:30—33. The W (Tungsten) is etched back to be left in the contact hole 12 in a plug-like shape and is deposited by CVD. Ex. 1005, 9:32—33; 9:35—36.

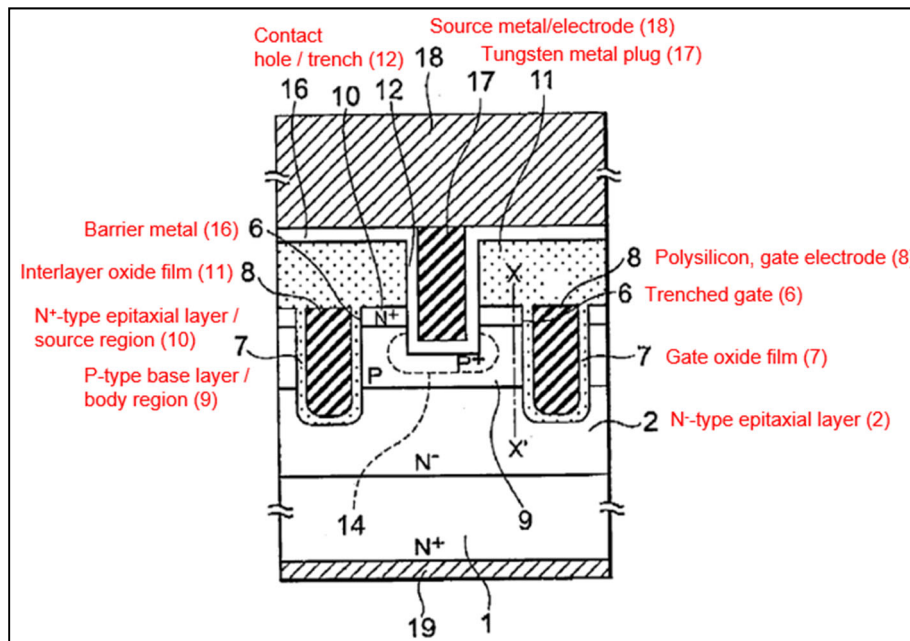


Kobayashi, Figure 5A (annotated)

3. Claim 4

- a. **“The trench semiconductor power device of claim 1 wherein: said source metal disposed on top of and in contact with a top surface of said metal plug further comprising a layer composed of aluminum alloys including alloys of AlCu or AlSiCu.”**

79. Claim 4 is disclosed in Kobayashi. Kobayashi, in Figure 5A, shows that a source metal 18 is disposed on top of a circular trench contact 12 (see § XI.A.1.g). Kobayashi also discloses that “AlSi (aluminum silicon) or AlSiCu (aluminum copper silicon) is deposited by sputtering to form the source electrode 18.” Ex. 1005, 9:36—38.



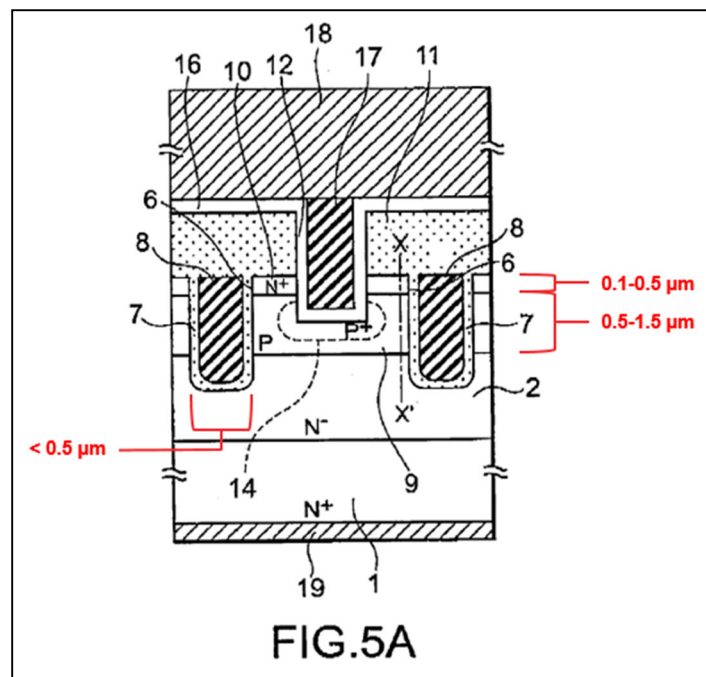
Kobayashi, Figure 5A (annotated)

4. Claim 5

- a. **“The trench semiconductor power device of claim 1 wherein: a diameter of a top surface of said circular trench contact is smaller than 1.0 micrometer.”**

80. Claim 5 is disclosed in Kobayashi. As discussed above and shown below in Figure 5A, a circular trench contact is shown (*see supra* § XI.A.1.c). Kobayashi teaches in relation to the gate trenches (trench 6) that “it is possible to

obtain the trench width not greater than $0.5\ \mu\text{m}$.” Ex. 1005, 7:49—50. Kobayashi discloses the following dimensions: (1) N^+ source layer 10 has a depth of $0.1\text{-}0.5\ \mu\text{m}$; and (2) P base layer 9 has a depth of $0.5\text{-}1.5\ \mu\text{m}$. Ex. 1005, 7:19-21 (explaining that Figs. 6A-6D, 7A-7D, and 8A-8C describe the method of producing the MOSFET in Fig. 5A); 8:21-46. Figure 5A below is annotated to show these dimensions.



Kobayashi, Figure 5A (annotated)

81. When considering these dimensions and the apparent relative proportions of the MOSFET of Figure 5A, the diameter of the circular trench contact is approximately the same as the width as the trench 6. The relevant dimensions I have considered include the regions that do not include the “ $\approx$ ” symbol, which are indicative that those “ $\approx$ ” portions of the drawing are not drawn

to scale. However, the remaining portions of the drawing, which do not have the “≈” symbol, appear to be drawn to relative scale.

82. Accordingly, Kobayashi discloses that it is possible to obtain a circular trench contact width/diameter not greater than 0.5 μm.

B. Claims 2 and 6 are unpatentable under pre-AIA 35 U.S.C. § 103 as obvious over Kobayashi in view of Kikkawa.

83. Claim 2 of the '409 Patent is unpatentable under pre-AIA 35 U.S.C. § 103 as obvious over Kobayashi in view of Kikkawa, T. et al, “A Quarter-Micrometer Interconnection Technology Using a TiN/Al-Si-Cu/TiN/Al-Si-Cu/TiN/Ti Multilayer Structure,” IEEE Transactions on Electron Devices, Vol. 40, No. 2, February 1993 (“Kikkawa”).

1. Claim 2

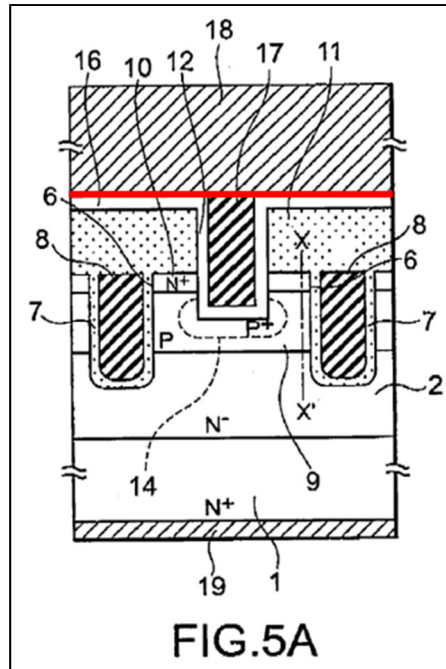
- a. “The trenched semiconductor power device of claim 1 further comprising: a contact resistance reduction metal layer composed of a titanium (Ti) layer disposed above a top surface said contact metal plug and below a bottom surface of said source metal for reducing a contact resistance between said contact metal plug and said source metal.”**

84. Based on Kobayashi in view of Kikkawa, claim 2 would have been obvious to a POSITA at the time of the filing of the '409 Patent. Claim 2 depends from claim 1, and claim 1 is disclosed by Kobayashi as discussed above. *See supra* § XI.A.1. Kobayashi also discloses a contact metal plug 17 connected to a source metal 18 positioned on top of a circular trench contact 12 (*see supra* §

XI.A.1.g). Kobayashi shows a metal layer (source metal layer 18) positioned above a top surface of the contact metal plug in Figure 5A. Ex. 1005 6:61—65. Kobayashi also discloses that a source metal layer 18 made of AlSiCu / AlCu. *See supra* § XI.A.3.

85. Kikkawa shows that it was well known in the art, at least by the time of the filing of the '409 Patent, that an AlCu / AlSiCu metal layer could have a bottom layer made of titanium (e.g., Ti or TiN) designed as both an electro- and stress-migration resistant interconnection structure. Ex. 1007 p. 4. This would also reduce the contact resistance when the device undergoes electro-migration stress, which also would have been appreciated by a POSITA at the time of the filing of the '409 Patent (Dec. 4, 2006). It should be noted that although Ti or TiN may have higher resistivity after undergoing heat treatment during the formation process, the resultant composite interconnect structure with AlSi/AlSiCu will have higher electrical and mechanical endurance in comparison to AlCu/AlSiCu single layer. This would yield a contact resistance that is more stable and lower over time.

86. A POSITA would have easily understood and applied the teachings of Kobayashi and Kikkawa in combination, resulting in a titanium layer disposed below the bottom surface of the source metal (and also above the top surface of the contact metal plug) as discussed below in § XI.B.3. Ex. 1005, Fig. 5A.



Kobayashi, Figure 5A (annotated)

2. Claim 6

87. Kobayashi discloses and anticipates every limitation of claim 6.

a. 6 [preamble]: “A trench semiconductor power device comprising a plurality of trench gates surrounding a plurality of transistor cells formed in a semiconductor substrate, wherein:”

88. The preamble of claim 6 is disclosed in Kobayashi. *See supra* §

XI.A.1.a.

b. 6[a]: “said trench gates surrounding said transistor cells as closed cells constituting substantially square-shaped cells with truncated corners”

89. Element 6[a] is disclosed by Kobayashi. *See supra* § XI.A.1.b.

c. 6[b]: “each of said closed cells further includes a circular trench contact hole disposed substantially in a central portion of said closed cells with a diameter of a

top surface of said circuit trench contact less than 1.0 micrometer, penetrating through source regions surrounding said trenched gates and extending into body regions encompassing said source regions”

90. Element 6[b] is disclosed in Kobayashi. *See supra* §§ XI.A.1.c. and XI.A.4.

d. 6[c]: “said circular trench contact comprises a hole opened from a top surface of said semiconductor substrate”

91. Element 6[c] is disclosed in Kobayashi. *See supra* § XI.A.1.d.

e. 6[d]: “wherein sidewalls of said hole are surrounded by and in contact said source and body regions”

92. Element 6[d] is disclosed in Kobayashi. *See supra* § XI.A.1.e.

f. 6[e]: “said circular trench contact is separate from said trenched gates with said source region and body region disposed between a gate oxide lining of said trenched gates and all circumferential points of the circular trench contact”

93. Element 6[e] is disclosed in Kobayashi. *See supra* § XI.A.1.f.

g. 6[f]: “said circular trench contact hole is filled with a metal plug composed of a Ti/TiN/W plug to contact said source and body regions”

94. Element 6[f] is disclosed in Kobayashi. *See supra* §§ XI.A.1.d, XI.A.1.e., and XI.A.2.

h. 6[g]: “said metal plug contacting a source metal disposed on top of said metal plug wherein said source metal layer composed of Ti/AlCu or Ti/AlSiCu alloys.”

95. Element 6[g] would have been obvious to a POSITA at the time of the filing of the '409 Patent based on Kobayashi in view of Kikkawa. *See supra* §§ XI.A.1.g, XI.A.3, XI.B.1. *See also infra* § XI.B.3.

3. Combining Kobayashi and Kikkawa

96. The combination of Kobayashi and Kikkawa discloses all elements of claims 2 and 6 (*see supra* §§ XI.B.1, XI.B.2).

97. It would have been obvious to a POSITA before the effective filing date of the '409 Patent to combine Kobayashi and Kikkawa to arrive at the trenched semiconductor power device of claims 2 and 6. Therefore, claims 2 and 6 are invalid under 35 U.S.C. § 103.

a. Kobayashi, Kikkawa, and the '409 Patent are analogous art seeking to solve similar problems.

1. Same field of endeavor

98. The '409 Patent, Kobayashi, and Kikkawa are all directed to semiconductor structures. Therefore, both Kobayashi and Kikkawa are analogous art in the same field of endeavor. More specifically, the '409 Patent relates to “the cell structure, device configuration and fabrication process of power semiconductor devices.” Ex. 1001, 1:7-9. Kobayashi also relates to “a vertical MOSFET (Metal Oxide Semiconductor Field Effect Transistor) reduced in cell size . . . and a method of producing the same.” Ex. 1005, 1:7-12–6. Kikkawa also relates to a

“new interconnection structure using a . . . multilayer conductor . . . for DRAM.”

Ex. 1007 at 3.

2. Pertinent to the same problems within the prior art.

99. The '409 Patent, Kobayashi, and Kikkawa are all directed to solutions to similar problems with semiconductor devices (including high power devices). These would include, for example, designing for electro- and stress migration resistant interconnection structures, which also serves to reduce the contact resistance when a device is undergoing electro-migration stress. The '409 Patent claims a titanium metal layer “for reducing a contact resistance between said contact metal plug and said source metal.” Similarly, Kobayashi discloses a TiN and TiN barrier metal layer below the source metal, which serves the purpose of electro-migration resistance. Kikkawa similarly discloses that problems with electro-migration and contact resistance are improved by using Ti and TiN barrier layers on an AlSiCu metal layer in a semiconductor structure. Ex. 1007 at 4.

100. Therefore, the Kobayashi and Kikkawa references are both in the same field of endeavor as claims 2 and 6 of the '409 Patent. Both references are pertinent to the problems addressed by the inventors of the '409 Patent.

b. Known benefits of combining the teachings of Kobayashi and Kikkawa

101. At the time of the filing date of the '409 Patent (Dec. 4, 2006), a POSITA would have recognized several benefits of combining Kobayashi and

Kikkawa as described in this Declaration. For example, it was well known to a POSITA that adding a titanium (Ti) or titanium nitride (TiN) layer to the bottom of Kobayashi's source metal layer would improve the reliability of the metal layer through the reduction of stress-induced electro-migration, which would also result in reduced contact resistance between metal layers and also reinforce the mechanical strength of the source metal layer. Ex. 1007 at 4. A POSITA would know that the resultant composite interconnect structure of adding a titanium (Ti) or titanium nitride (TiN) with AlSi/AlSiCu will have higher electrical and mechanical endurance in comparison to AlCu/AlSiCu single layer. This would yield a contact resistance that is more stable and lower over time.

c. Rationales for combining Kobayashi and Kikkawa

102. At the time of the filing date of the '409 Patent (Dec. 4, 2006), a POSITA would have been motivated to combine Kobayashi and Kikkawa with a reasonable expectation of success.

1. Express teaching

103. Kikkawa expressly teaches that Ti and TiN barrier layers combined with an AlSiCu metal layer in a semiconductor structure reduces contact resistance and addresses problems with electro-migration. Ex. 1007 at 4. As explained in Kikkawa, the addition of the TiN / Ti layers as a bottom layer to the source metal of Kobayashi would further achieve the aim set out by Kikkawa. Kobayashi and

Kikkawa show that the source metal layer, metal plug, and barrier or intermediate TiN / Ti layers were all well known, conventional, familiar elements to a POSITA at the time of the filing of the '409 Patent. *See also supra* ¶¶ 85, 101.

2. Use of known techniques to improve similar devices in the same way

104. A POSITA at the time of the filing of the '409 Patent (Dec. 4, 2006), would have understood how to combine Kobayashi and Kikkawa using known techniques for improving similar devices in the same way. As provided above, Kobayashi and Kikkawa are both in the semiconductor structures field. Also, both references describe known methods for interconnection and other metal layers within semiconductor structures. Ex. 1005, 9:30-53; Ex. 1007 at 3—4. Kobayashi and Kikkawa disclose similar devices, because both are directed to semiconductor structures and layers. E.g., Ex. 1005, 9:30-53; Ex. 1007 at 3—4. The '409 Patent claims that its titanium (Ti) layer reduces contact resistance between a contact metal plug and a source metal (Ex. 1001, claims 2, 6), while Kikkawa explains that the titanium (TiN / Ti) layer below an AlSiCu layer improves electro-migration and contact resistance. Ex. 1007 at 4. Kikkawa also discloses its TiN / Ti layer in a location next to an AlSiCu layer, which makes its combination with Kobayashi's AlSiCu layer a natural fit and common sense choice. Ex. 1005 at Fig. 5A; Ex. 1007 at Fig. 1. A POSITA at the time of the filing of the '409 Patent would have understood how to add Kikkawa's TiN / Ti layer to Kobayashi's source metal

(AlSiCu layer) applying known techniques. This would have been a minor and commonplace modification for a POSITA.

3. Applying a known technique to a known device ready for improvement to yield predictable results

105. A POSITA at the time of the filing of the '409 Patent (Dec. 4, 2006), would have understood combining the teachings of Kobayashi and Kikkawa as a known technique being applied to a known device that was ready for improvement and that the combination would yield predictable results. As discussed above, adding Kikkawa's TiN / Ti layer to Kobayashi's source metal (AlSiCu layer) was well within a POSITA's knowledge of techniques and methods that could be applied to known semiconductor structures (as expressly taught by Kikkawa). A POSITA also would have had a reasonable expectation of success for this combination that it would have achieved a predictable result, that is, to improve electro-migration (which also reduces contact resistance). *Id.*

4. Combining familiar elements according to known methods to yield predictable results

106. To a POSITA, combining Kobayashi and Kikkawa would involve combining familiar elements using known methods for predictable results. Kobayashi and Kikkawa disclose the source metal layers, metal plugs, and barrier layers or intermediate TiN / Ti layers, demonstrating that these elements were all known, conventional, familiar elements to a POSITA. For a POSITA, adding Kikkawa's TiN / Ti layer to Kobayashi's source metal (AlSiCu layer) would

therefore have been use of a known method to achieve a minor modification. The POSITA would have had a reasonable expectation of success for this combination and the combination would have had a predictable result, for example, to improve electro-migration and therefore reduce contact resistance.

5. Known work in the field

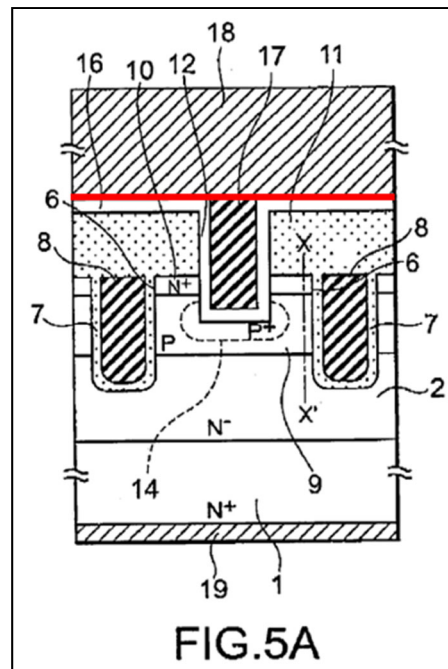
107. Kobayashi describes some of what was known in the field of semiconductor structures at least by April 24, 2003, Kobayashi's filing date, which was well before the '409 Patent filing date (December 2006). A POSITA would have known how to modify Kobayashi in view of Kikkawa's teachings in the same field. And a POSITA would have been motivated to do so based on design incentives or other market forces. Further, this modification would have been predictable to a POSITA. Both Kobayashi and Kikkawa are directed to semiconductor structures and several design incentives are known for adding Kikkawa's TiN / Ti barrier layers into Kobayashi's design. *Id.* ¶¶ 101, 103, 105,

106. A POSITA designing a semiconductor structure would naturally seek to improve electro-migration and contact resistance, to the extent possible in view of other design constraints. Ex. 1001 claims 2, 6; Ex. 1007 at 3—4. In other words, a POSITA considering Kobayashi would have had reasons to modify Kobayashi in view of Kikkawa, and adding a titanium (TiN / Ti) barrier layer to the bottom of

Kobayashi's source metal layer would have been well within the skill of a POSITA. *Id.*

d. The combination of Kobayashi and Kikkawa

108. The combination of Kobayashi and Kikkawa renders obvious claims 2 and 6, as illustrated in the annotated Kobayashi Figure 5A below, which further includes the titanium (TiN and/or Ti) layer(s) for improving electro-migration and contact resistance, as disclosed in Kikkawa.



Kobayashi, Figure 5A (annotated)

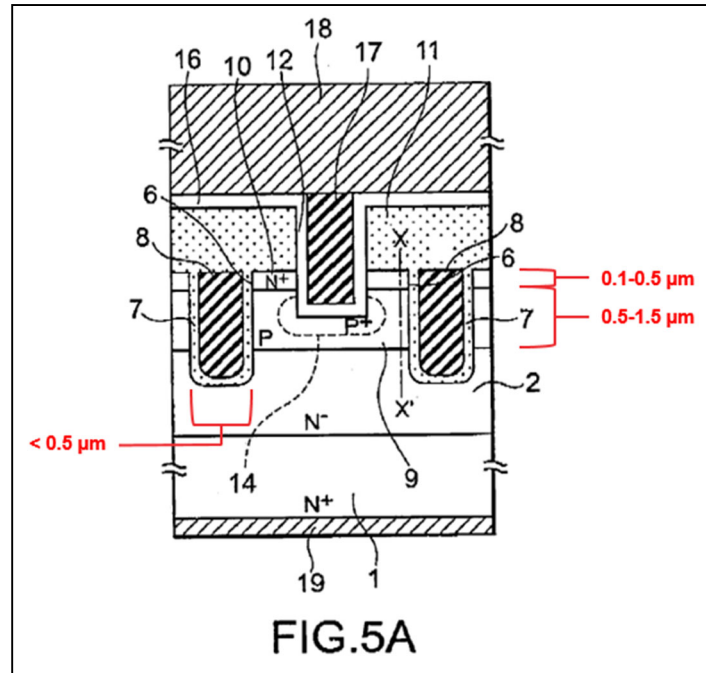
109. Based on reasons explained above, a POSITA would have found it obvious to combine Kobayashi and Kikkawa.

C. **Claim 5 is unpatentable under pre-AIA 35 U.S.C. § 103 as obvious over Kobayashi and the knowledge of a POSITA.**

1. **Claim 5**

- a. **“The trenched semiconductor power device of claim 1 wherein: a diameter of a top surface of said circular trench contact is smaller than 1.0 micrometer.”**

110. Claim 5 is disclosed in Kobayashi. *See supra* ¶¶ 80-82. Claim 5 would have also been obvious to a POSITA at the time of filing the '409 Patent (December 4, 2006) based on Kobayashi and the knowledge of a POSITA at that time. A POSITA would have understood that the diameter of the circular trench contact and the width as the trench 6 are substantially the same based relative proportions of the MOSFET of Figure 5A (annotated below). Kobayashi teaches that the trench 6 can have a width less than 0.5 μm . Ex. 1005, 7:34-55. In other words, based on the relative proportions and scale of Fig. 5A, a POSITA would have understood that the diameter/width of the circular contact trench is less than 1.0 μm . *Id.*; *see also supra* ¶¶ 80-82.



Kobayashi, Figure 5A (annotated)

111. Additionally a POSITA would have understood that there are plethora of other reasons that the width of the source contact trench would be close to the minimum feasible width (diameter) that can be possibly obtained by the given technology capability at the time of invention (which is no greater than 0.5 μm as stated by Kobayashi).

112. For example, a wider width would lead to wider total width of the unit cell for the Power MOSFET, and thus a larger unit cell area. This would lead to less current drive and higher on resistance per a given silicon area, making the device less economical to manufacture.

113. Conversely, for a given unit cell size, which implies a given fixed distance between two gate trenches, a wider source contract trench width in

between the two gate trenches would dictate that the P+ base layer will be closer to its adjacent trench gate on both sides, and would lead to an increase of threshold voltage of the transistor due to the lateral diffusion of the P+ base layer, a problem that Kobayashi was trying to overcome in the first place.

114. One other important consideration for minimizing the width of the source contact trench is the subsequent deposition of the barrier metal layer and the CVD tungsten. A POSITA would have understood that the width of the trench would be not be larger than the thickness of the tungsten deposited. Ex. 1005, 9:33-35. Filling a wider trench contact width would require a thicker tungsten deposition and longer deposition time, and leading to a longer subsequent etch back time to planarize the source contact plug. A POSITA would have known that this is not a desirable manufacturing process flow.

115. At least for these above reasons, a POSITA would understand that the contract trench diameter would be not greater than 0.5 μm (which is less than claim 5's requirement of 1.0 μm).

D. Claims 1, 3—5 are unpatentable under pre-AIA 35 U.S.C. § 103 as obvious over Kobayashi in view of Hsieh.

116. Claims 1, 3-5 of the '409 Patent are unpatentable under at least pre-AIA 35 U.S.C. § 103 as obvious over Kobayashi in view of Hsieh.

1. Claim 1

- a. **1 [preamble] : “A trenched semiconductor power device comprising a plurality of trenched gates surrounding a plurality of transistor cells formed in a semiconductor substrate, wherein:”**

117. The preamble of claim 1 is disclosed in Kobayashi. *See supra* §

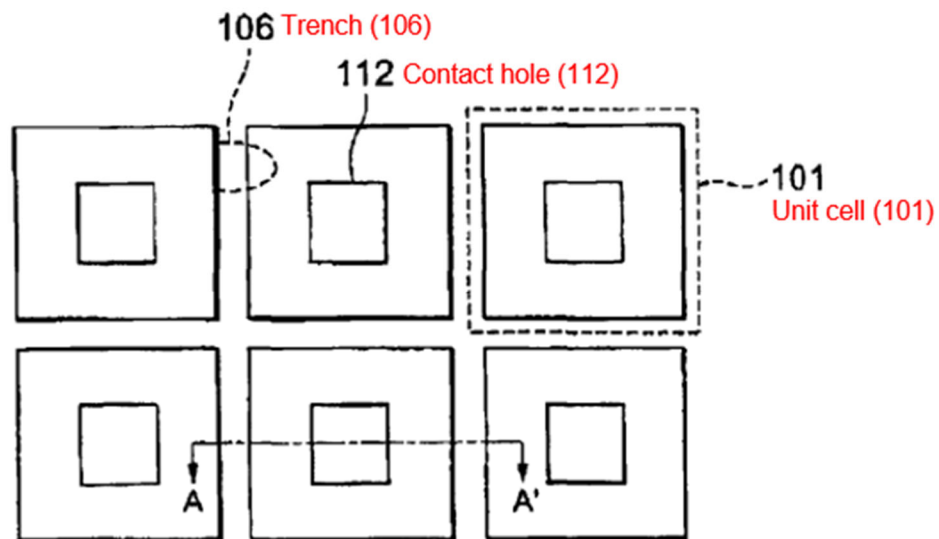
XI.A.1.a.

- b. **1[a]: “said trenched gates surrounding said transistor cells as closed cells constituting substantially square-shaped cells with rounded corners;”**

118. Element 1[a] is disclosed by Kobayashi combined with Hshieh.

Kobayashi show “a plurality of *square cells* are arranged in a matrix” in Figure 3A

Ex. 1005, 6:26—27 (emphasis added).

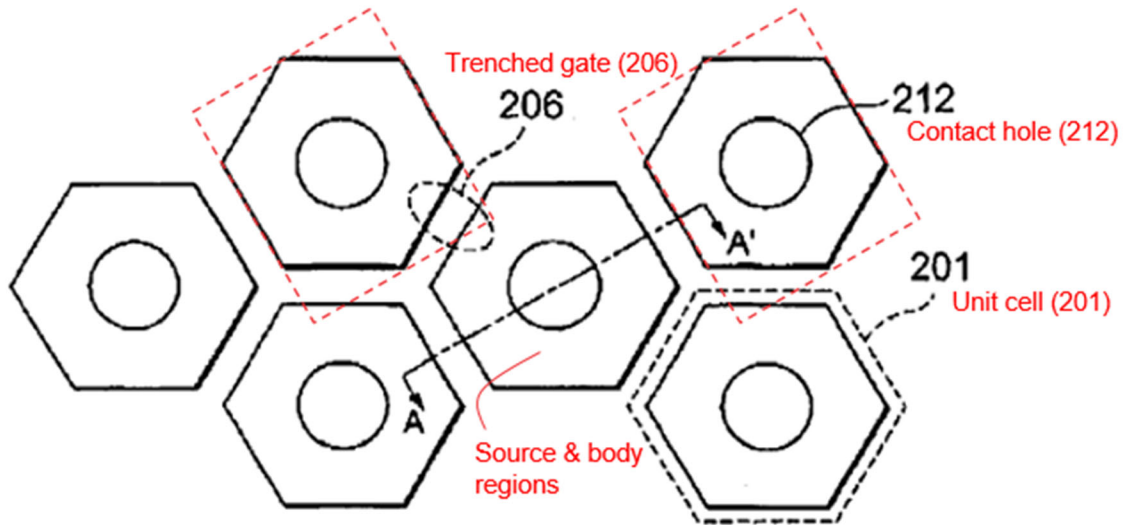


Kobayashi, Figure 3A (annotated)

119. Kobayashi shows “a plurality of hexagonal cells” in Figure 4A

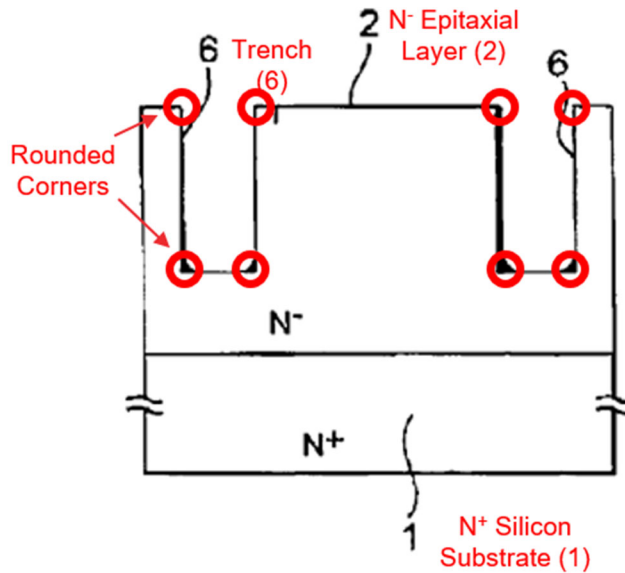
Hexagons are square shapes with the corners removed, as shown in annotated

Figure 4 below. Accordingly, Figure 4A shows substantially square cells with truncated corners. Ex. 1005, 6:30.



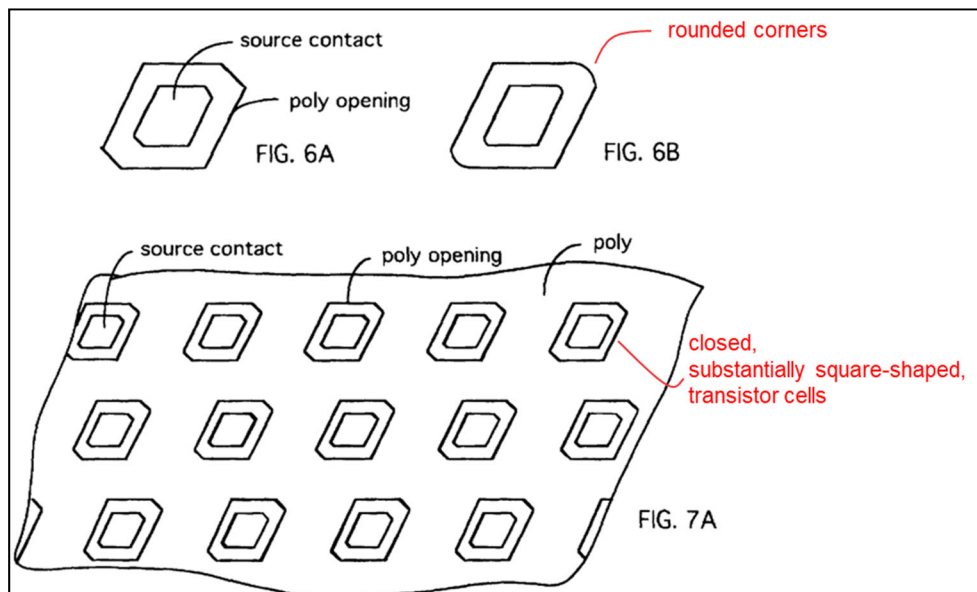
Kobayashi, Figure 4A (annotated)

120. Kobayashi, in Figure 6C, shows that the MOSFETs are made with a process where the “corners of each trench 6 at the bottom are rounded [and] corners of each trench 6 at an opening portion may also be rounded.” Ex. 1005, 7:57—8:4.



Kobayashi, Figure 6C (annotated)

121. Hshieh also discloses rounding the corners of transistor cells. Ex. 1006, 5:3-28. Hshieh Figure 6A—7A (annotated below) shows transistor cells that are closed cells constituting cells with multiple truncated and rounded corners.



Hshieh, Figure 6A—7A (annotated)

122. Kobayashi discloses closed cells that are substantially square shaped with corners that are truncated by design layout. And Hsieh shows that the truncated corners of closed cells can be rounded (and the benefits for doing so). For example, Hsieh discloses addressing the problems of vulnerable punch-through weak points in the corners of square cells, which is due to an undesirable higher peak electric field being reached at the corners. Ex. 1006, 2:19-39. As further explained below in § XI.D.5, it would have been obvious to combine Kobayashi's square shaped cells that are truncated by design layout with Hsieh's rounded corners to arrive at element 1[a] of claim 1.

- c. **1[b]: “each of said closed cells further includes a circular trench contact disposed substantially in a central portion of said closed cells, penetrating through a source region surrounding said trenched gates and extending into a body region encompassing said source region;”**

123. Element 1[b] of claim 1 is disclosed in Kobayashi. *See supra* § XI.A.1.c.

- d. **1[c]: “said circular trench contact comprises a hole opened from a top surface of said semiconductor substrate and is filled with a contact metal plug”**

124. Element 1[c] of claim 1 is disclosed in Kobayashi. *See supra* § XI.A.1.d.

- e. **1[d]: “wherein sidewalls of said hole are surrounded by and in contact said source and body regions”**

125. Element 1[d] of claim 1 is disclosed in Kobayashi. *See supra* §

XI.A.1.e.

- f. **1[e]: “and said circular trench contact is separate from said trenched gates with said source region and body region disposed between a gate oxide lining of said trenched gates and all circumferential points of the circular trench contact;”**

126. Element 1[e] of claim 1 is disclosed in Kobayashi. *See supra* §

XI.A.1.f.

- g. **1[f]: “and said contact metal plug connected to a source metal disposed on top of said circular trench contact.”**

127. Element 1[f] of claim 1 is disclosed in Kobayashi. *See supra* §

XI.A.1.g.

2. Claim 3

- a. **“The trenched semiconductor power device of claim 1 wherein: said contact metal plug disposed in said hole of said circular trench contact further comprising a Ti/TiN/W metal plug.”**

128. Claim 3 is disclosed in Kobayashi. *See supra* § XI.A.2.

3. Claim 4

- a. **“The trenched semiconductor power device of claim 1 wherein: said source metal disposed on top of and in contact with a top surface of said metal plug further comprising a layer composed of aluminum alloys including alloys of AlCu or AlSiCu.”**

129. Claim 4 is disclosed in Kobayashi. *See supra* § XI.A.3.

4. Claim 5

- a. “The trench semiconductor power device of claim 1 wherein: a diameter of a top surface of said circular trench contact is smaller than 1.0 micrometer.”**

130. Claim 5 is disclosed in Kobayashi. *See supra* § XI.A.4.

5. Combining Kobayashi and Hshieh

131. The combination of Kobayashi and Hshieh discloses all elements of claims 1, 3-5 (*see* §§ XI.D.1—4). It would have been obvious to a POSITA before the effective filing date of the '409 Patent to combine Kobayashi and Hshieh to arrive at the trench semiconductor power device of claims 1, 3-5. Therefore, those claims invalid under 35 U.S.C. § 103.

- a. Kobayashi, Hshieh, and the '409 Patent are analogous art seeking to solve similar problems.**

1. Same field of endeavor

132. The '409 Patent, Kobayashi, and Hshieh are all directed to semiconductor structures. Therefore, these references are analogous art in the same field of endeavor. More specifically, the '409 Patent relates to “the cell structure, device configuration and fabrication process of power semiconductor devices.” Ex. 1001, 1:7-9. Kobayashi also relates to “a vertical MOSFET (Metal Oxide Semiconductor Field Effect Transistor) reduced in cell size . . . and a method of producing the same.” Ex. 1005, 1:7-12–6. Hshieh also relates to a

“power transistor cell[s] supported on a semiconductor substrate.” Ex. 1006, Abstract.

2. Pertinent to the same problems within the prior art.

133. The '409 Patent, Kobayashi, and Hshieh are all directed to solutions to similar problems with semiconductor devices (including high power devices). This includes solutions for vulnerabilities at the corners of square cells in semiconductor devices. The corners of such square cells tend to induce higher peak electric fields, leading to a low avalanche breakdown voltage, which is undesirable. The '409 Patent acknowledges that square cell configurations with sharp corners in the prior art cause low avalanche current and reduced device ruggedness due to the parasitic N+PN latches near the corners. Ex. 1001 1:15-62. Kobayashi also discloses rounding corners of trenches in square cells. Ex. 1005, 7:57-8:4. In support of rounding the corners of the trenches in the square cells, Kobayashi cites to Sang-Gi Kim et al's paper (Ex. 1012). In the cited paper, Kim et al discuss the benefits of trench corner rounding leading to higher breakdown voltage and lower leakage current—the same benefits discussed in the '409 Patent. Ex. 1005, 7:57-8:4; Ex. 1012. Hshieh also discloses vulnerable punch-through weak points in the corners of square cell. Again this is due to an undesirable higher peak electric field being reached due to the same corner effect. Ex. 1006, 2:19-39.

134. The Kobayashi and Hshieh references are in the same field of endeavor as claims 1, 3-5 of the '409 Patent and are pertinent to the problems addressed by the inventors of the '409 Patent.

b. Known benefits of combining the teachings of Kobayashi and Hshieh

135. At the time of the filing date of the '409 Patent (Dec. 4, 2006), a POSITA would have recognized several benefits of combining Kobayashi and Hshieh as described in this Declaration. For example, it was well known to a POSITA that rounding the corners of square cells in semiconductor structures had several advantages. Ex. 1006, 2:19-39; Ex. 1005, 7:57-8:4.

c. Rationales for combining Kobayashi and Hshieh

136. At the time of the filing date of the '409 Patent (Dec. 4, 2006), a POSITA would have been able to combine Kobayashi and Hshieh with a reasonable expectation of success, as further discussed below.

1. Express teaching

137. Hshieh expressly teaches the benefits of rounding the corners of square cells. Ex. 1006, 5:3-17, Figs. 6A-8B. A POSITA would have appreciated that combining (1) rounding the corners (as disclosed by Hshieh) with (2) the truncated corners Kobayashi, would further achieve the benefits taught in Hshieh. Kobayashi and Hshieh both show that square-shaped cells, their corners, and methods of truncating, blunting, and rounding the corners (both intentionally by

design and through natural rounding), are all known, conventional, familiar elements and processes to a POSITA.

2. Use of known techniques to improve similar devices in the same way

138. A POSITA at the time of the filing of the '409 Patent (Dec. 4, 2006), would have understood how to combine Kobayashi and Hshieh using known techniques for improving similar devices in the same way. As provided above, Kobayashi and Hshieh are both in the semiconductor structures field. Also, both references describe known methods relating to problems with sharp corners in closed cells within semiconductor structures. Ex. 1005, 9:30-53; Ex. 1006, 2:19-39. Kobayashi and Hshieh disclose similar devices at least because both are directed to semiconductor structures and closed cell layouts. E.g., Ex. 1005, Fig. 4A, 7:57-8:4; Ex. 1006, Figs. 6A-8B. The '409 Patent seeks to address known difficulties that are exaggerated at the corners of trenches in closed cell layouts. Hshieh also teaches that rounding the corners of such devices has advantages. Ex. 1006, 5:3-17, Figs. 6A-8B. Hshieh teaches rounding corners of substantially square cells, which makes its combination with Kobayashi a natural fit and common sense choice. Ex. 1005 at Fig. 5A; Ex. 1006 at Figs. 6A-8B. A POSITA at the time of the filing of the '409 Patent would have understood how to add Hshieh's rounding of corners to Kobayashi's truncated corners of a closed cell

layout as applying known techniques. This would have been a minor and commonplace modification for a POSITA.

3. Applying a known technique to a known device ready for improvement to yield predictable results

139. A POSITA at the time of the filing of the '409 Patent (Dec. 4, 2006), would have understood that combining Kobayashi and Hshieh is a known technique applied to a known device that was ready for improvement and that such combination would yield predictable results. As discussed above, adding Hshieh's rounding of corners to Kobayashi's truncated corners of a closed cell layout was well within a POSITA's knowledge of techniques and methods that could be applied to known structures (as expressly taught by Hshieh). A POSITA also would have had a reasonable expectation of success for this combination that it would have achieved a predictable result: to improve electro-migration and contact resistance. *Id.*

4. Combining familiar elements according to known methods to yield predictable results

140. To a POSITA, combining Kobayashi and Hshieh would involve combining familiar elements using known methods for predictable results. Kobayashi and Hshieh disclose square-shaped cells, their corners, and methods of truncating, blunting, and rounding the corners, demonstrating that these elements and methods were all known, conventional, familiar elements to a POSITA. For a POSITA, adding Hshieh's rounding of corners to Kobayashi's truncated

corners of a closed cell layout would therefore have been use of a known method to achieve a minor modification. The POSITA would have had a reasonable expectation of success for this combination, and this combination would have had a predictable result, for example, to improve electro-migration and contact resistance.

5. Known work in the field

141. Kobayashi and Hshieh disclose known work in the field of semiconductor structures prior to the date of the filing of the '409 Patent (December 4, 2006). A POSITA would have known how to modify Kobayashi in view of Hshieh's teachings in the same field. And a POSITA would have been motivated to do so based on known design incentives or other market forces. Further, this modification would have been predictable to a POSITA. Both Kobayashi and Hshieh are directed to semiconductor structures, and there are several design incentives for adding Hshieh's rounding of corners to Kobayashi's truncated corners of a closed cell layout. *Id.* ¶¶ 133, 138, 139, 140. A POSITA designing a semiconductor structure would naturally seek to eliminate known problems at the corners of closed cells, to the extent possible in view of other design constraints. Ex. 1005, Fig. 4A, 7:57-8:4; Ex. 1006, Figs. 6A-8B; 5:3-17. In other words, a POSITA considering Kobayashi would have had reasons to modify Kobayashi in view of Hshieh, and rounding the truncated corners of closed

cell layouts using known methods of design would have been within the skill of a POSITA. *Id.*

d. The combination of Kobayashi and Hshieh

142. The combination of Kobayashi and Hshieh renders obvious claims 1, 3-5, as described in § XI.D.1.b.

143. Based on reasons explained above, a POSITA would have found it obvious to combine Kobayashi and Hshieh.

E. Claims 2, 6 are unpatentable under pre-AIA 35 U.S.C. § 103 as obvious over Kobayashi, Hshieh, and Kikkawa.

144. Claims 2, 6 of the '409 Patent are unpatentable under pre-AIA 35 U.S.C. § 103 as obvious over the Kobayashi, Hshieh, and Kikkawa.

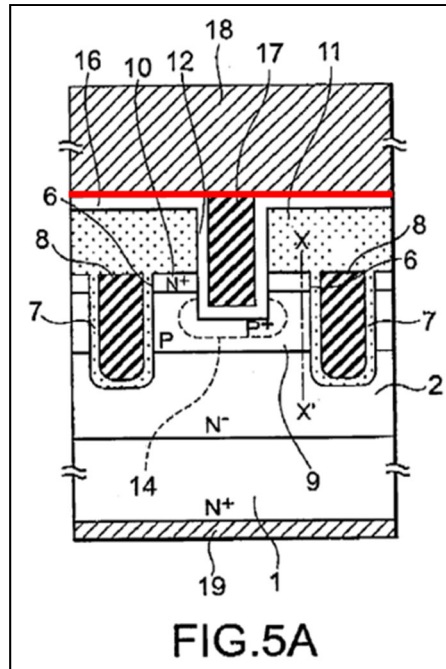
1. Claim 2

- a. “The trenched semiconductor power device of claim 1 further comprising: a contact resistance reduction metal layer composed of a titanium (Ti) layer disposed above a top surface said contact metal plug and below a bottom surface of said source metal for reducing a contact resistance between said contact metal plug and said source metal.”**

145. Claim 2 would have been obvious to a POSITA at the time of the filing of the '409 Patent based on Kobayashi in view of Kikkawa and Hshieh. Specifically, claim 2 depends from claim 1. Claim 1 is disclosed by Kobayashi in view of Hshieh as discussed above. *See supra* § XI.D.1. Kobayashi discloses a contact metal plug 17 connected to a source metal 18 disposed on top of a circular

trench contact 12 (see *supra* § XI.A.1.g). Kobayashi also shows a metal layer (source metal layer 18) disposed above a top surface of the contact metal plug. Ex. 1005 6:61—65, Figure 5A (annotated below); *see also supra* § XI.A.3 (explaining that the source metal layer 18 can be made of AlSiCu / AlCu).

146. Kikkawa teaches an AlCu / AlSiCu metal layer could have a bottom layer made of titanium (e.g., Ti or TiN), and that such a layer would act as an electro- and stress-migration-resistant interconnection structure. Ex. 1007 p. 4. This would also reduce the contact resistance when the device undergoes electro-migration stress, which also would have been appreciated by a POSITA at the time of the filing of the '409 Patent. A POSITA would have been motivated to combine the teachings of Kobayashi and Hsieh as discussed above. *See supra* § XI.D.5. A POSITA would have further been motivated to combine Kobayashi and Hsieh with Kikkawa to include a titanium layer disposed below the bottom surface of the source metal (and therefore above the top surface of the contact metal plug) as discussed in §§ XI.B.3; *see also* Ex. 1005, Fig. 5A (annotated below). Hsieh's design would also benefit from the titanium layers disclosed in Kikkawa.



Kobayashi, Figure 5A (annotated)

2. Claim 6

147. Claim 6 would have been obvious to a POSITA at the time of the filing of the '409 Patent based on Kobayashi in view of Kikkawa and Hshieh.

- a. **6 [preamble]: “A trench semiconductor power device comprising a plurality of trench gates surrounding a plurality of transistor cells formed in a semiconductor substrate, wherein:”**

148. The preamble of claim 6 is limiting, it is disclosed in Kobayashi. *See supra* § XI.A.1.a.

- b. **6[a]: “said trench gates surrounding said transistor cells as closed cells constituting substantially square-shaped cells with truncated corners”**

149. Element 6[a] is disclosed by Kobayashi combined with Hshieh. *See supra* § XI.D.1.b.

- c. **6[b]: “each of said closed cells further includes a circular trench contact hole disposed substantially in a central portion of said closed cells with a diameter of a top surface of said circuit trench contact less than 1.0 micrometer, penetrating through source regions surrounding said trenched gates and extending into body regions encompassing said source regions”**

150. Element 6[b] is disclosed in Kobayashi. *See supra* §§ XI.A.1.c, XI.A.4.

- d. **6[c]: “said circular trench contact comprises a hole opened from a top surface of said semiconductor substrate”**

151. Element 6[c] is disclosed in Kobayashi. *See supra* § XI.A.1.d.

- e. **6[d]: “wherein sidewalls of said hole are surrounded by and in contact said source and body regions”**

152. Element 6[d] is disclosed in Kobayashi. *See supra* § XI.A.1.e.

- f. **6[e]: “said circular trench contact is separate from said trenched gates with said source region and body region disposed between a gate oxide lining of said trenched gates and all circumferential points of the circular trench contact”**

153. Element 6[e] is disclosed in Kobayashi. *See supra* § XI.A.1.f.

- g. **6[f]: “said circular trench contact hole is filled with a metal plug composed of a Ti/TiN/W plug to contact said source and body regions”**

154. Element 6[f] is disclosed in Kobayashi. *See supra* §§ XI.A.1.d, XI.A.1.e., and XI.A.2.

- h. **6[g]: “said metal plug contacting a source metal disposed on top of said metal plug wherein said source**

metal layer composed of Ti/AlCu or Ti/AlSiCu alloys.”

155. Element 6[g] is obvious in view of Kobayashi combined with Hshieh and Kikkawa. *See supra* §§ XI.A.1.g, XI.A.3, XI.B.1, XI.B.3, XI.D.5.

F. Claim 5 is unpatentable under pre-AIA 35 U.S.C. § 103 as obvious over Kobayashi in view of Hshieh and the knowledge of a POSITA.

1. Claim 5

- a. “The trenched semiconductor power device of claim 1 wherein: a diameter of a top surface of said circular trench contact is smaller than 1.0 micrometer.”**

156. Claim 5 depends from claim 1. Claim 1 is obvious over Kobayashi and Hshieh as discussed above. *See supra* § XI.D.1. In addition, “[A] diameter of a top surface of said circular trench contact [that] is smaller than 1.0 micrometer” would have been obvious to a POSITA based on Kobayashi and the knowledge of a POSITA. *See supra* § XI.C.

XII. OBJECTIVE INDICIA OF NON-OBVIOUSNESS

157. Having reviewed the file history and the other exhibits cited in this declaration, I am not aware of any objective indicia of non-obviousness for the claims of the ’409 Patent.

XIII. DECLARATION

158. I understand this declaration will be used as evidence in a contested case before the PTAB.

159. I am aware that willfully false statements in connection with this declaration are punishable by fine or imprisonment, or both under 18 U.S.C. § 1001 and may jeopardize the validity of the Petition. All statements herein are made of my own knowledge true and all statement made on information and belief are believed to be true.

160. I declare under penalty of perjury that the foregoing is true and correct.

Executed this 27 day of October, 2023 at Fremont, CA.

Respectfully Submitted,

A handwritten signature in dark ink, appearing to read 'David Liu', with a stylized flourish at the end.

Dr. David Liu